Performance Benchmark of Parallel SiC and Hybrid GaN-SiC Power Switches

WPI

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Abstract

This project was conducted at Kyoto University of Advanced Sciences(KUAS) for seven weeks to contribute specific new knowledge and understanding in the experimental electrical characterization of modern gallium nitride (GaN) and silicon carbide (SiC) transistors in a parallel and hybrid configuration. The project involved deploying and using the PCB design software Altium and experimental test setups and methodologies such as current and voltage probes, oscilloscopes, and power tests. The project aimed to conduct a performance benchmark of parallel Silicon Carbide (SiC) and hybrid Gallium Nitride-Silicon Carbide (GaN-SiC) power switches, and by conducting a varied of efficiency tests on the GaN-SiC hybrid and the SiC in parallel, we were able to notice that the GaN-SiC hybrid exhibited significantly higher efficiency than the SiC in parallel. This is due to the better switching efficiency that the GaN provides when combined with the SiC, which has greater free-wheeling performance. This project also completed several high-performance designs that can be tested for further research.

Executive Summary:

Semiconductors play a critical role in the functionality of electronic devices. As technology advances, the demand for semiconductors with improved performance and reliability has escalated, requiring higher blocking voltages, switching frequencies, efficiency, and reliability for power applications.

In response to these challenges, the development of Wide Bandgap Semiconductors (WBGs) has the potential to replace traditional silicon(Si) based semiconductors for advantages over Si semiconductors. Silicon Carbide(SiC) and Gallium Nitride(GaN) are identified as promising alternatives, each with distinct properties. SiC is noted for its technological maturity compared to other WBGs, higher thermal conductivity, and breakdown voltage. GaN, on the other hand, stands out for its high switching speeds and efficiency despite lower thermal conductivity.

This study also goes over the emerging technology of GaN-SiC hybrid switches, combining the advantages of GaN's switching performance with SiC's free-wheeling capabilities. The hybrid switch is designed for optimum switching, conduction, and free-wheeling performance, introducing a novel approach to power electronics.

The methodology involves the development of setups, such as a buck converter, half-bridge switches, bidirectional current switch tests, and a thermal analysis setup. The objectives include measuring the efficiency of GaN-SiC hybrid configurations compared to SiC in parallel and designing a versatile PCB for standalone and parallel configurations.

The project aims to contribute new knowledge and understanding in the experimental parametric electro-thermal characterization of modern GaN and SiC transistors by conducting a performance benchmark of parallel Silicon Carbide (SiC) and hybrid Gallium Nitride-Silicon Carbide (GaN-SiC) power switches. The primary focus is determining power efficiency and addressing the evolving needs of power electronics in the future, considering gate frequency, input voltage, and load handling capabilities. Two specific transistors, the SiC Mosfet SCT3120AL, and the GaN HEMT IGO60R070D1, were chosen for testing.

The project compares the efficiency of GaN-SiC hybrid configuration and the SiC in parallel configuration using a buck converter setup. It later involves the design of a versatile PCB for standalone and parallel configurations, incorporating features for conducting a Double Pulse Test and Thermal Analysis that would be useful for future research.

The methods include the development of a buck converter setup to compare power efficiency, considering input and output power measurements at different voltages and frequencies. The design of a standalone and parallel circuit for an HB setup involves using Altium Designer and selecting components for precision and safety.

In conclusion, this research project was able to advance the understanding of Wide Bandgap Semiconductors' applications in power electronics, provide valuable insights into the efficiency of GaN-SiC hybrid configurations, and contribute a design for a versatile PCB for future experimentation. By conducting a varied efficiency test on the GaN-SiC hybrid and the SiC in parallel, we were able to notice that the GaN-SiC hybrid exhibited significantly higher efficiency than the SiC in parallel. This is due to the better switching efficiency that the GaN provides when combined with the SiC, which has greater free-wheeling performance. This project also completed several high-performance designs that can be tested in the future for further research.

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Glossary:

BDS: Bi-directional switch

DC: Direct Current

DPT: Double-Pulse Testers

GaN: Gallium Nitride

HB Switch: Half-bridge switch

HEMT: High Electron Mobility Transistor

MOS: Metal-Oxide-Semiconductor

MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor

PCB: Printed Circuit Board

Si: Silicon

SiC: Silicon Carbide

WBGs: Wide Band-Gap Semiconductors

Acknowledgments

We would like to thank KUAS for allowing us into their campus and providing us with the environment needed to complete this project. We would also like to extend our thanks to Professor Alberto Castellazzi and Mr. Yonghwa Lee for welcoming us into their team and guiding us through these 8 weeks. We would also like to extend our gratitude to Dr. Jaedon Kwak as he laid the foundation on which this work was based. Additionally, we would also like to thank Professor Adam Powell and Professor Bitar for the support during the development of this project.

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Chapter 1: Introduction

Semiconductors play a crucial role in the functionality of electronic devices that have become integral to our daily lives. They are present in most electronic technology, and as technological advancements continue, there is an escalating demand for semiconductors that are not only better but also more reliable.

In recent times, the widely utilized semiconductor Silicon has approached its theoretical limits. Power applications rely on these semiconductors, as outlined by Tolbert. L. et al. (2003) and Sedra. A. et al. (2019) now necessitate higher blocking voltages, switching frequencies, efficiency, and reliability. Faced with these challenges, exploring alternative materials to replace Silicon has propelled the development of Wide Bandgap Semiconductors (WBGs). Among WBGs, Silicon Carbide and Gallium Nitride stand out for their potential to be smaller, faster, more reliable, and more efficient when compared to Silicon.

The objective of this project is to conduct a performance benchmark of parallel Silicon Carbide (SiC) and hybrid Gallium Nitride-Silicon Carbide (GaN-SiC) power switches. The aim is to determine which of these two options would achieve the highest power efficiency and effectively meet the evolving needs of power electronics in the future. The assessment will focus on three primary components: gate frequency, input voltage, and load handling capabilities.

Chapter 2: Background & Literature Review

Chapter 2.1: Wide Band Gap Semiconductors

Semiconductors are solid materials with conductivity between a conductor and an insulator. These materials often change their properties depending on the surrounding conditions. The most common semiconductor used today for microelectronic and power electronics applications is Silicon (Si). Still, due to recent advancements, the material has approached its theoretical limit for power applications, which require higher blocking voltages, switching frequencies, efficiency, and reliability(Tolbert. L. et al., 2003; Sedra. A. et al., 2019). Due to this necessity, multiple research studies on wide bandgap semiconductors(WBGs) were conducted to replace Si technology. These materials have a greater band gap than Si which allows power electronic components to be smaller, faster, more reliable, and more efficient(ADVANCED MANUFACTURING OFFICE, 2013). The most likely candidates for these devices are Silicon Carbide(SiC), Gallium Nitride(GaN) and Diamond. Table 2.1 describes the physical properties of these materials in comparison to Si.

Table 2.1: Physical characteristics of Si and main WBGs. From Tolbert, L. M., Ozpineci, B., Islam, S. K., & Chinthavali, M. S. (2003) WIDE BANDGAP SEMICONDUCTORS FOR UTILITY APPLICATIONS. semiconductors.

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap, Eg (eV)	1.12	1.43	3.03	3.26	3.45	5.45
Dielectric constant, ε_r	11.9	13.1	9.66	10.1	9	5.5
Electric Breakdown Field, E_c (kV/cm)	300	400	2500	2200	2000	10000
Electron Mobility, μ_n ($cm^2/V{\cdot}s$)	1500	8500	500 80	1000	1250	2200
Hole Mobility, μ_p ($cm^2/V{\cdot}s$)	600	400	101	115	850	850
Thermal Conductivity, λ (W/cm·K)	1.5	0.46	4.9	4.9	1.3	22
Saturated Electron Drift Velocity, v_{sat} ($\times 10^7$ cm/s)	1	1	2	2	2.2	2.7

As seen in Table 2.1, diamond is the material that would have the best theoretical performance, but because of the difficulties that come with fabricating devices with diamond, there is not as much research. On the other hand, SiC already has several commercially available power devices, and GaN has become an interest due to its switching performance. Figure 2.1 goes over a summary of the relevant properties of each material and Table 2.2 goes over the merit points of each material in regards to the application and also how many times the different WBG compares with Si.

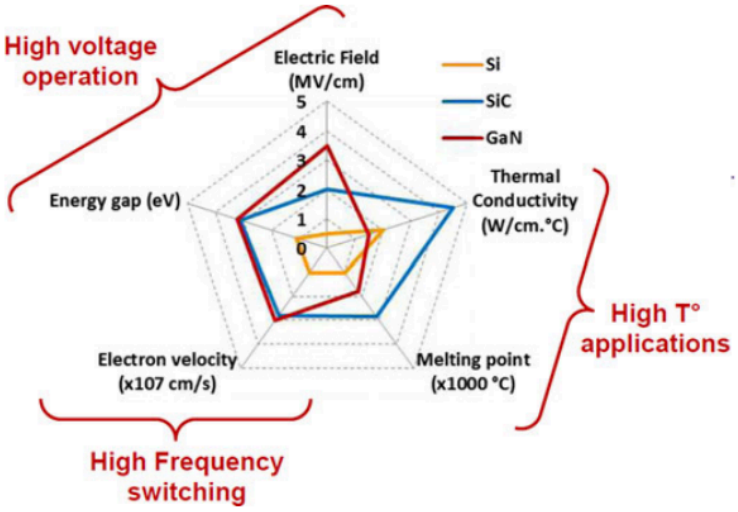

Figure 2.2: Summary of Si, SiC, and GaN relevant material properties. From Millan, J., Godignon, P., Perpina, X., Perez-Tomas, A., & Rebollo, J. (2014). A Survey of Wide Bandgap Power Semiconductor Devices. IEEE Transactions on Power Electronics, 29(5), 2155–2163. https://doi.org/10.1109/tpel.2013.2268900

Table 2.2: Main figures of merit for WBGs compared to Si from Tolbert, L. M., Ozpineci, B., Islam, S. K., & Chinthavali, M. S. (2003) WIDE BANDGAP SEMICONDUCTORS FOR UTILITY APPLICATIONS. semiconductors, 1, 3

	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
JFM	1.0	1.8	277.8	215.1	215.1	81000
BFM	1.0	14.8	125.3	223.1	186.7	25106
FSFM	1.0	11.4	30.5	61.2	65.0	3595
BSFM	1.0	1.6	13.1	12.9	52.5	2402
FPFM	1.0	3.6	48.3	56.0	30.4	1476
FTFM	1.0	40.7	1470.5	3424.8	1973.6	5304459
BPFM	1.0	0.9	57.3	35.4	10.7	594
BTFM	1.0	1.4	748.9	458.1	560.5	1426711

JFM : Johnson's figure of merit is a measure of the ultimate high frequency capability of the material.

BFM : Baliga's figure of merit is a measure of the specific on-resistance of the drift region of a vertical FET

FSFM : FET switching speed figure of merit

BSFM : Bipolar switching speed figure of merit

FPFM : FET power handling capacity figure of merit

FTFM : FET power switching product

BPFM : Bipolar power handling capacity figure of merit

BTFM : Bipolar power switching product

Chapter 2.1.1: Silicon Carbide

As mentioned before, SiC is the WBG with the most commercially available power devices, with multiple researches done to them, making it the most mature technology. There are also two versions for SiC which can be chosen depending on the application but 4H-SiC is preferred because its vertical and horizontal mobility are the same in contrast with 6H-SiC. Millan, J. et al (2014) reported that this technology has blocking voltage capabilities of over 10 kV and it is expected that there could be an increase in their voltage capability up to 20–30 kV in the near future.

Tolbert, L. et al(2003) explained the benefits of SiC include reduced losses, increased efficiency, and reduced size. Increasing the switching frequency when compared to Si. Based

on Figure 2.1, we can see that this material also has the highest thermal conductivity and melting point. Also based on Table 2.1, it also has the highest breakdown voltage out of the available devices. This is why, in Table 2.2, SiC is generally the best for power handling capacity and bipolar power handling capacity. Some of the other aspects alternate because of the differences between 4H and 6H-SiC. However, because of the aspects above it can be said that SiC has the best free-wheeling capabilities among the available technologies (Bayarkhuu et al., 2022).

Chapter 2.1.2: Gallium Nitride

In recent years, GaN research has risen because of the capabilities of this device in comparison to Si. Millan, J. et al. (2014) mention that the GaN direct band gap, large critical electric field, and electron mobility make it attractive for high frequency and voltage performance. Adding to this, Tolbert, L. et al. (2003) explain how it also has the advantage over SiC of its negligible recovery current, high switching speeds, and lower switching loss. Unfortunately, it also has a higher voltage drop. They also mention that the main issue with GaN is the lack of a native oxide required for MOS, which is why it is grown over Sapphire or SiC.

Using the data in Table 2.1, we can further see these comments as Gan is reported to contain the highest bandgap, electron mobility, hole mobility, and saturated electron drift velocity out of the available technologies. Unfortunately, it also has a lower thermal conductivity than of Si. Table 2.2 is the material with the best switching speed and bipolar switching speed.

Chapter 2.1.3 GaN-SiC Hybrid

GaN-SiC hybrid switches are a growing technology that is in development. This switch combines the GaN's switching performance with the SiC's free wheeling. The switch is created by combining one GaN transistor in parallel with a SiC transistor. Bayarkhuu et al.(2022) in the article "Hybrid GaN-SiC Power Switches for Optimum Switching, Conduction and Free-Wheeling Performance," proposed a hybrid that was both able to yield avalanche robustness and was cost competitive, emphasizing the emphasis on a single gate-driver. The key to this hybrid is to

have a slight delay between the GaN and the SiC turning on and off in order to maximize efficiency. In order to do so, the GaN is turned on before the SiC, similarly, it also turns off after the SiC in order for it to handle most of the switching losses.

Chapter 2.2: Double Pulse Test

Levett, D. et al(2020) described the double pulse test(DPT) as a tool that enables a power switch to be turned on and off at different current levels allowing a power stack under worst-case operating conditions early in the design process and reduces risk of unexpected issues appearing later in the project.

Chapter 2.2.1: Half-Bridge Switches Set up

The Half-bridge (HB) switch setup is a setup used to simulate real case scenarios. It contains one High-side transistor (HST) working as a freewheel Mosfet and one Low-side transistor(LST) working as a drive MOSFET. The drive MOSFET's gate is connected to a Piecewise linear voltage source (VPWL). When VPWL turns on the LST, current from Vin will start flowing through the MOSFET, increasing over time as defined by the formula $I = \int \frac{V}{L} dt$. When the LST gets turned off, the current starts freewheeling and going through the HST, and once the LST turns back on, the current will continue to rise from where it was before it was turned off. This is because, while the circuit was in free-wheeling, the inductance of the load stored the current. The main aspect to be considered when doing an HB is to ensure the off time is long enough to ensure that the device(LST) is off and the current is flowing through the HST but not long enough for the inductor to discharge. This setup has power loss in free-wheeling due to the body diode in the MOSFET, and it will also experience a reverse recovery current when turned back on. This setup can be seen in Figure 2.2.

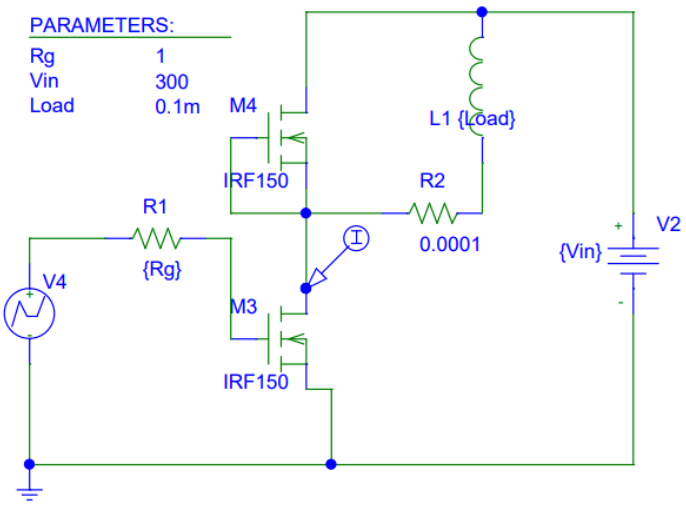

Figure 2.2: HB Set up

Chapter 2.2.2: Bidirectional Current Switch Test Setup

The Bidirectional Current switch setup is a setup used to simulate real case scenarios. Contrary to the HB, this setup has two sets of two transistors as seen in Figure 2.2. In the picture, one of the two transistors on the left act as the driver MOSFETs while the right side set acts as the free-wheeling MOSFETs. The second MOSFET in both sets acts as diodes.

When VPWL turns on the left side set, current from the current source will start flowing through the MOSFET, increasing the voltage over time. When the VPWL gets turned off, the current starts freewheeling and going through the right side set, and once the VPWL turns back on, the voltage will continue to rise from where it was before it was turned off. This is due to the fact that, while the circuit was free-wheeling, the capacitor was storing the voltage. This setup can be seen in Figure 2.3. The voltage through the drain of M3 is defined by $V = \int \frac{I}{C} dt$.

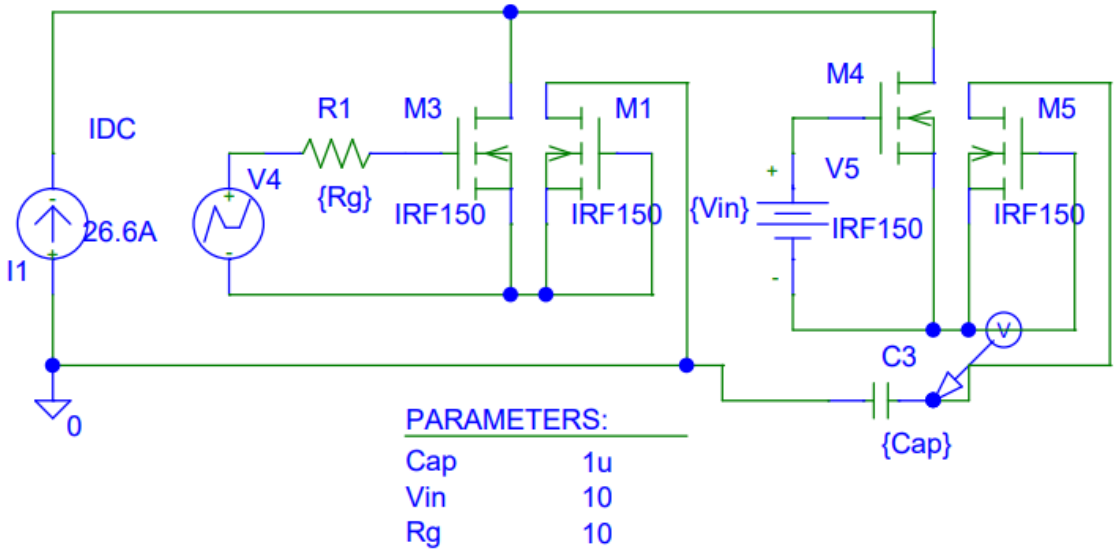

Figure 2.3: BDS Set-up.

Chapter 2.3: Buck Converter

A Buck converter is a DC-to-DC converter that converts high DC voltage into lower DC voltage. The power between the input and output sides is considerably similar, so this voltage change is compensated for by increasing the current in the output. “The buck converter uses a transistor as a switch that alternately connects and disconnects the input voltage to an inductor,” as described by Castaldo, A. (2019). Figure 2.4 shows a typical buck converter circuit and the way current is affected by the PWM.

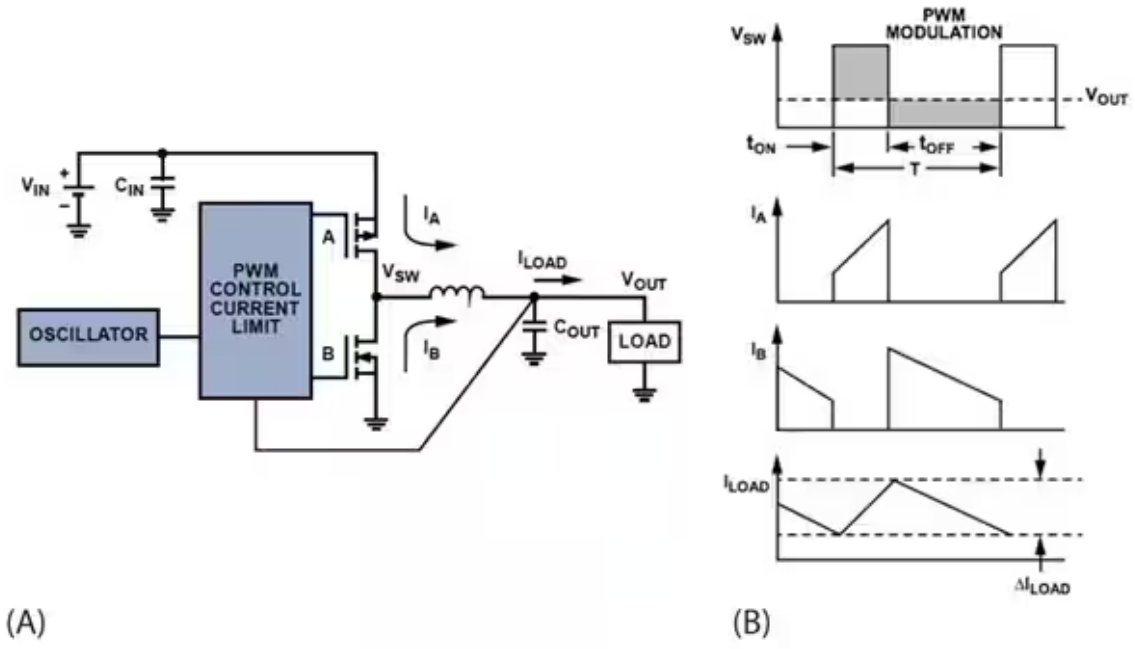

Figure 2.4: Typical buck converter (A), a PWM controller alternates opening and closing a pair of switches to drive current IA to an inductor or current IB from the inductor to main load regulation (B). Evanczuk, S. (2013, May 8). Buck converters simplify energy harvesting from high-input-voltage transducers. DigiKey. https://www.digikey.at/en/articles/buck-converters-simplify-energy-harvesting-from-high-input-voltage-transducers

Chapter 3: Objectives

The aim of this project is to contribute specific new knowledge and understanding in the experimental parametric electro-thermal characterization of modern gallium nitride (GaN) and silicon carbide (SiC) transistors in a parallel and hybrid configuration. We will be using the SiC Mosfet SCT3120AL and another using the GaN HEMT IGO60R070D1 for this test.

Objective 1: Measure the GaN SiC Hybrid configuration efficiency compared to the SiC in parallel configurations.

The first objective is to compare the efficiency of the GaN-SiC hybrid configurations for power electronics compared to SiC in parallel with a buck converter. This test allows us to make a power efficiency comparison between the GaN-SiC Hybrid and the SiC in parallel configurations. It is important to note that while SiC transistors are commonly used today, GaN-SiC hybrids are more theoretical and less studied, so the results could shed light on this relatively new study.

Objective 2: Design an HB setup using GaN or SiC as stand-alone and in parallel.

The second objective is to design a PCB that is capable of stand-alone and parallel configurations while also being able to be used for conducting a Double Pulse Test and Thermal Analysis that could be done in further research.

Chapter 4: Methods

Method 1: Develop a buck converter setup to compare the power efficiency of SiC in parallel and the GaN-SiC Hybrid.

In order to properly make a comparison, it was needed to build a buck converter. With this, we can compare the input power and output power and check which one was higher in between the two. We first designed a buck converter test setup, shown in Figure 4.1, used the gate controller circuit, designed by Dr. Jaedon Kwak and shown in Figure 4.2, and reworked another PCB circuit to make it viable for this experiment by changing the gate resistance to 10 Ohms, soldering film capacitors of value 400 μF and connecting the circuit to the gate driver using a twisted pair connection. These changes can be seen in Figure 4.3; they were meant to keep both circuits operating in as similar conditions as possible. We also used an inductor of 445μH value and an output capacitor of $480\mu F$ value to the circuit in Figure 4.1. After setting up the circuit, we adjusted the PWM to have a duty cycle of 45%, 300 ns dead time between the high and low sides, as well as a 500 ns delay between the GaN and the SiC, where the GaN turned on first and turned off last. This delay was not optimized due to time constraints, but it was still helpful for results. We also attached current and voltage meters on the load side to measure the output power when compared to the input voltage and current by the power supply, ZX-S-1600HAN.

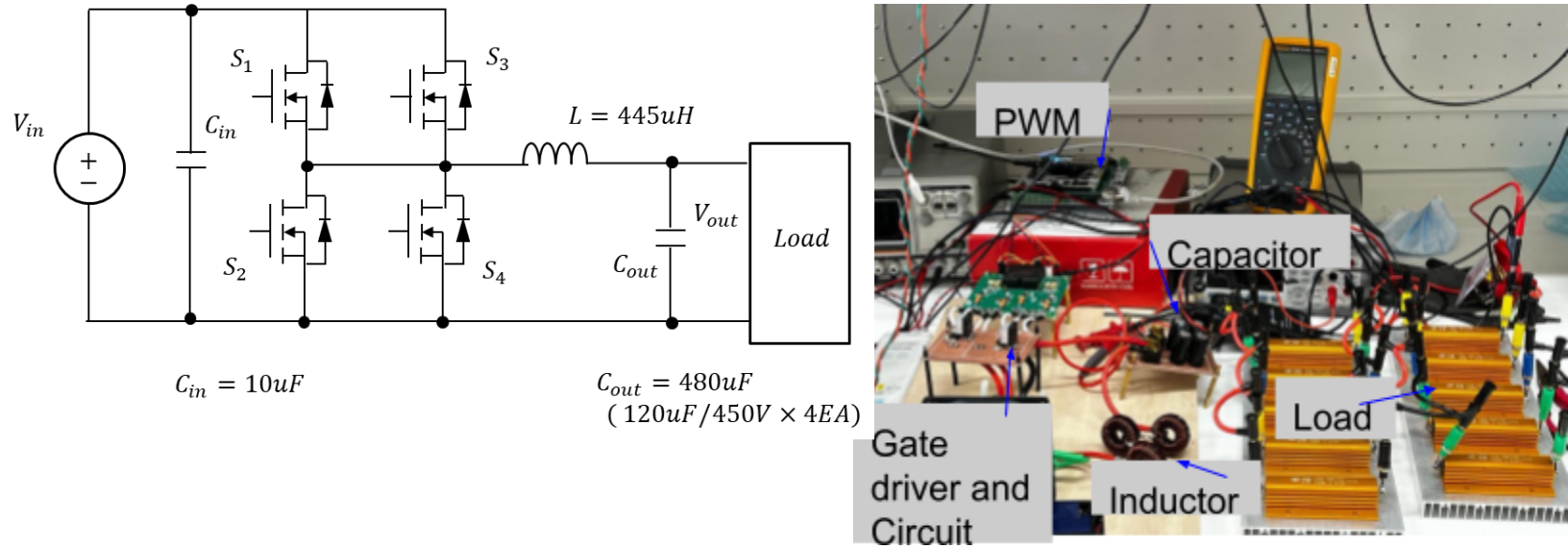

Figure 4.1: Buck Converter Schematic(Left) and Physical(Right)

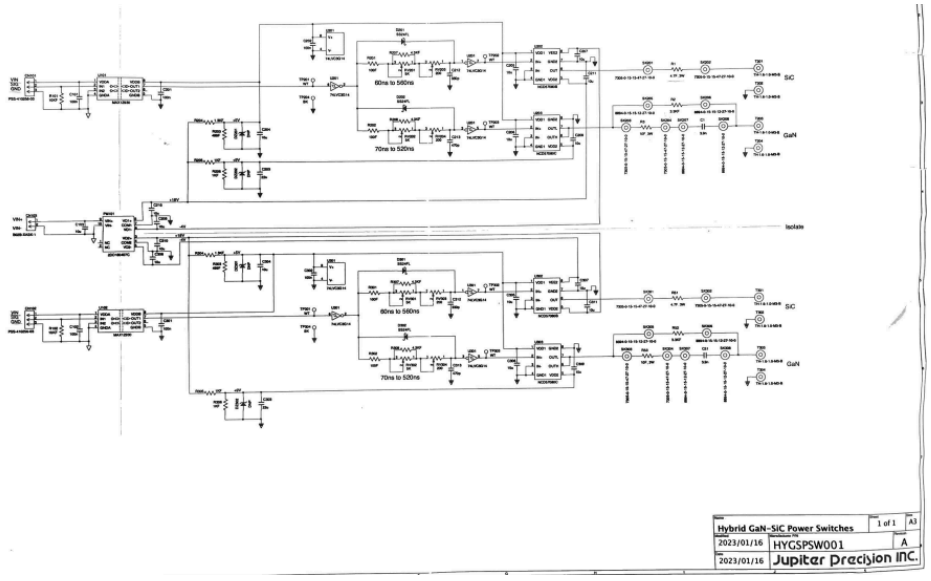

Figure 4.2: Dr Jaedon Kwak's Gate driver schematic

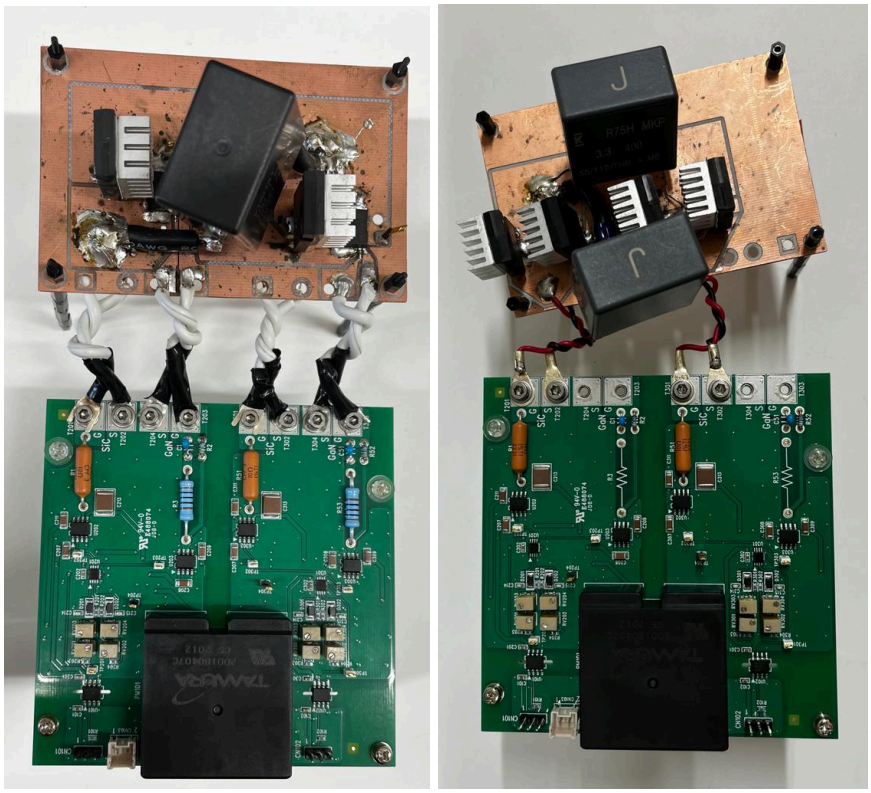

Figure 4.3: GaN-SiC circuit not attached to the Buck (Left) and SiC in parallel not connected to the Buck

After this, we checked the power loss for different scenarios. The first was to measure from 50 V and in increments of 10V up until 100V. After 100V, we changed to increments of 50V until reaching 300V. All of these measurements were taken at different frequencies as well; these frequencies start at 50kHz and go until 150kHz in increments of 25kHz. This was also repeated twice, once with a 45 Ohm load and another with a 25 Ohm load. The team also kept track of the temperature to make sure that none of the devices burned out and kept dedicated cooling fans on the transistors, as well as adding heat sinks to them.

Method 2: Design of a standalone and parallel circuit for an HB setup for SiC configuration.

For this design, we designed a PCB using Altium Designer that would be able to continue the project presented in method one more accurately, run a DPT and thermal analysis, and be able to test higher voltages. Using the website https://www.mouser.com/, we looked into components that could be of use to the PCB in order to order and start to find out the dimensions that would need to be considered for the design. It is expected that the voltages tested of 1.8 kV, so it was important to find electrolytic capacitors, discharge resistors and film capacitors that could be used to increase the precision of the experiment while also taking care of safety. Another consideration to take into account is the ability to run a thermal analysis on the transistors. For this, we would be using power transistor test sockets, as well as arranging the PCB in a way that all transistors are oriented in the same direction with the metal facing down, leaving space for a thermal plate to be added. Not only would the test socket allow a thermal analysis but it would also allow us to change the transistor tested and will also allow the test to run as both standalone and parallel configurations since it would act as an open circuit when no transistor is inside. The other condition would be that this PCB should be able to be used for both a Buck converter and also for a DPT test of an HB setup. For this, we found the similarities between these two circuits and placed spaces for banana plugs that could be removed and changed based on the needs.

Chapter 5: Findings & Data

Findings 1: Hybrid Configuration and Parallel SiC Configuration Power Comparison

Throughout the course of the project, the team conducted a series of experiments to collect data comparing the performance of SiC in parallel configuration and the GaN-SiC hybrid configuration. Notably, the GaN-SiC hybrid exhibited significantly higher efficiency than the SiC in parallel, as evidenced by the results presented in Appendix D.

Figures 5.1-5.3 highlight key data extracted from the results, emphasizing the superior effectiveness of the hybrid configuration, particularly at 100 V, a crucial benchmark for voltage significance. Regardless of frequency and load, the hybrid consistently outperformed the SiC in parallel, except at 100 kHz, where the SiC in parallel closely approached the hybrid at 45 Ohm and surpassed it at 25 Ohm. The advantages persisted at higher voltages, as shown in Figure 5.3, the comparative effectiveness at varying high input voltages for the same frequency and load. A notable data that could be captured by the results in Figure 5.1-5.2 and Appendix D is that as load resistance decreased and load current increased, the performance gap between the two power switch technologies was reduced. However, it is essential to note that the absence of a clear trend resulted from our focus on input voltage and duty cycle rather than controlling the output voltage or output power.

Despite these issues, our data strongly supports the conclusion that the GaN-SiC hybrid holds a substantial advantage in terms of efficiency over the SiC in parallel. For increased accuracy, future measurements could benefit from including power measurements at the input, providing a more precise assessment compared to relying solely on voltage and current readings from the voltage generator, which had limitations in precision because of the significant digits presented. Unfortunately, our testing on high voltages was limited to voltages between 100 V and 200 V due to challenges with the GaN, including stress-induced overheating. The transistor experienced temperatures above 70°C, leading to unstable gate-drain voltages and

output voltage. Attempts to address these issues within the project timeline were unsuccessful, and the continuation of the project would have compromised the component.

Several factors contributed to the temperature spike and instability at higher voltages. The GaN's sensitivity to stray inductance, caused by higher voltage and amplified by the small PCB area and restricted spacing between polygon planes of the PCB, likely led to short circuits. Efforts to address PCB issues could be attempted by redesigning the PCB in Findings 2 with test sockets intended for HEMT instead of the expected MOS. Another potential cause of overheating was the delay between the GaN and the SiC, as detailed in Method 1. The inability to optimize the 500ns delay in SiC turning on and a 500ns delay when they turn off could have resulted in the increased temperatures in the GaN since it was handling the full current load for some nano-seconds. It would be important to optimize the delay in future testing. This can be coupled with the heat dissipation challenges of HEMT when compared to regular MOS. Addressing this thermal issue, particularly with GaN's lower heat conductivity compared to SiC, should be a significant design consideration.

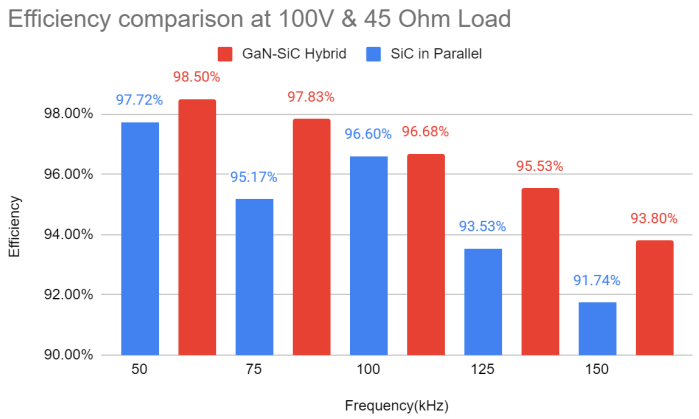

Figure 5.1: Efficiency Comparison of GaN-SiC Hybrid and SiC in Parallel Configuration at 45Ohm Load and 100 V at Different Frequencies

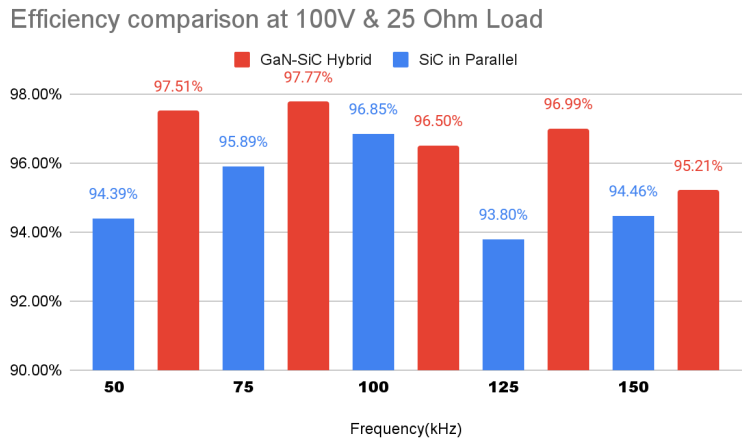

Figure 5.2: Efficiency Comparison of GaN-SiC Hybrid and SiC in Parallel Configuration at 25Ohm Load and 100 V at Different Frequencies

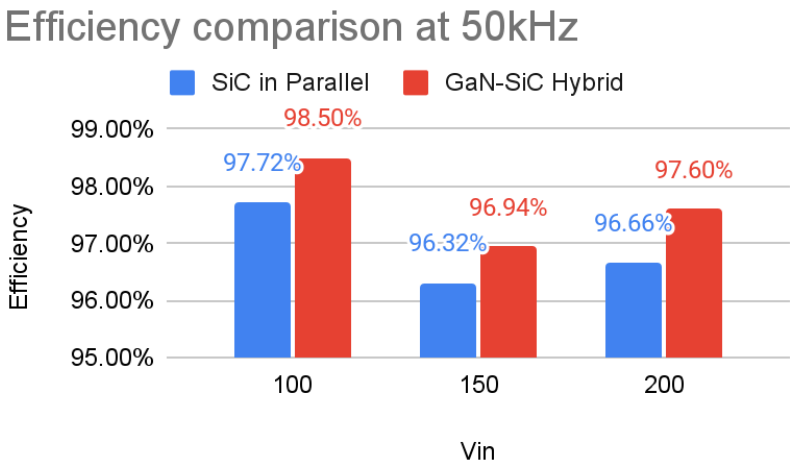

Figure 5.3: Efficiency Comparison of GaN-SiC Hybrid and SiC in Parallel Configuration at 45Ohm Load and 50 kHz at Different High Voltages

One aspect to consider for enhancing performance results involves modifying the PCB design by increasing the area and spacing between the pins on the PCB, which could mitigate issues related to stray inductance and potential short circuits. Additionally, addressing the cooling system for the GaN is important. The lack of a native oxide in GaN transistors, necessary for MOS, and only being able to be a HEMT creates challenges in dissipating heat when internal temperatures rise. Implementing a more efficient cooling system is an important part of the application of power switches at higher voltages for stable operation, but for the GaN, it is even more important because of its usual limited heat dissipation. Furthermore, optimizing

the delay between the GaN and the SiC is also an important consideration. Finding the optimal balance in this delay could enhance the overall system efficiency of the GaN-SiC hybrid. Alternatively, there could be a second GaN in Parallel alongside the SiC in the hybrid configuration. This introduces the possibility of employing two GaNs to support current flow during the delay between GaN activation and SiC activation.

Despite the constraints encountered, our findings demonstrate the promising efficiency of the GaN-SiC hybrid when compared to more common power switch technologies, offering valuable insights for future exploration and optimization of these technologies. The limitations identified in this study provide a foundation for defining experimental approaches in future research and, if properly addressed, could lead to the practical applications of this hybrid technology of power switch technologies in real-world applications.

Findings 2: Standalone & Parallel Configuration Design

In formulating our design strategy, meticulous considerations were essential to ensure the efficacy of our experimental setup. The first is the importance of the spacing between the polygon planes assigned to each pin to prevent parasitics. Simultaneously, the selection of appropriate film and electrolytic capacitors, complemented by suitable discharge resistors, was taken highly into consideration for overall circuit stability. It is also important to get good transistor test sockets and the appropriate layer design and holes. We chose a 3mm spacing between pins and between different spaces within the layer. We also took into consideration that the total of the PCB plate was 30 cm x 20 cm, so the design was built in 26 cm x 16 cm, allowing enough space for an in-house prototype. This approach was made with the purpose of guaranteeing precision and reliability during future experimentations.

For the components, we chose to use four T3P-L214-ST-HT for the transistor test socket and the VISHAY 900V 1848C MKP F1908 for the film capacitor, using two of these. Both of these were already available in the lab. On the Mouser webpage, we got the ALS70A103NT500 Electrolytic Capacitor and the YP1047KJ resistor, four each. This setup will help us get more accurate results by removing as many sources of parasitic inductance as

possible. We also purchased the banana plugs from Amazon and used three on the PCB. These banana plugs will allow more flexibility in changing from HB to Buck if needed, as well as changing which side of the circuit is being tested as freewheeling and which one is working as the driver. The list of components purchased can be found in Appendix E. After having selected the components and set certain parameters, we designed the PCB, which can be seen in Figure 5.4.

A quick explanation of the PCB in Figure 5.4, the red marks the topside layer, the blue marks the bottomside layer, and the gray regions are the ones that are in both. The green components on the top are the test sockets the pins will be soldered to the top layer, and the bottom pins will be bent to make contact with the bottom layer. The small circles seen near the location of the pins are the holes. The greyish circles surrounded by the yellow squares are the banana plug location. The large yellow rectangles are the film capacitors placed on the top layer. The pink squares represent the electrolytic capacitor placed in the bottom layer. The green ovals are the terminals of the capacitor and also the place where the resistor would be screwed in. Also, it is important to note that the left side of the top layer is the positive terminal while the right side is the negative terminal, and although not apparent in the figure, they are isolated in the bottom layer.

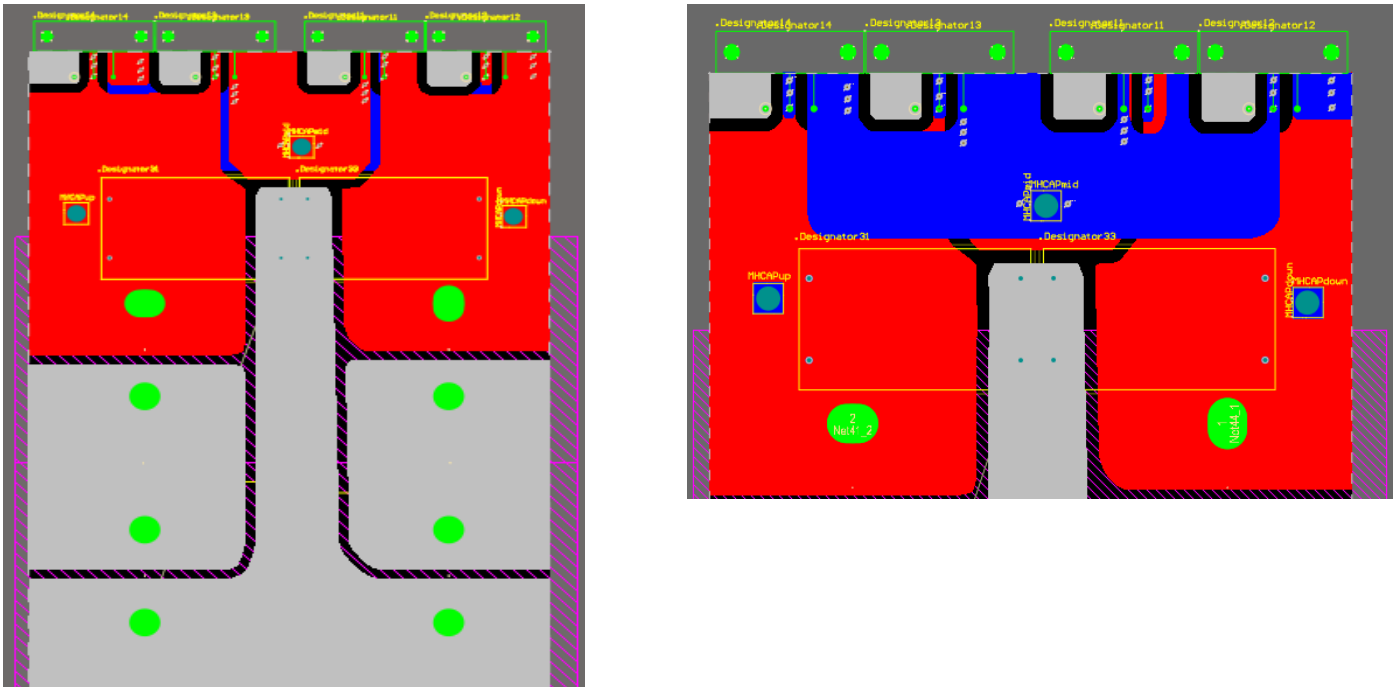

Figure 5.4: PCB Design Top layer(Left) Bottom Layer(Right)

This circuit would, theoretically, be able to do thermal analysis, HB DPT, and Buck converter while also being able to handle voltages up to 1.8kV because of the specifications of the capacitor. Unfortunately, due to time constraints and problems with the machinery, it was impossible to print an in-house prototype to test this PCB.

Chapter 6: Conclusion & Recommendations

The performance benchmark conducted has demonstrated the superior capabilities of the GaN-SiC hybrid configuration over the SiC in parallel configuration. This superiority is attributed to the combination of the SiC's robust free-wheeling performance and the GaN's efficient switching capabilities. However, this advantage is accompanied by the major disadvantage of the GaN for its sensitivity to stray inductances and lower thermal conductivity, which was heightened by the characteristics of the PCB used in the study. For the next steps, conducting a similar study on GaN in parallel would be recommended since this will reinforce the results of the GaN-SiC being a better alternative to the traditional Si semiconductors.

Despite the demonstrated improved performance, addressing certain experimental issues becomes an important step when moving forward. Firstly, optimizing the delay between the SiC and GaN is crucial. This adjustment would enhance the synchronization of the two semiconductors, contributing to overall system efficiency. Another approach would be to introduce an additional GaN in parallel, distributing current loads more effectively during specific time intervals. Secondly, enhancing the thermal dispersion for the GaN is also relevant. Identifying a more efficient heat sink solution is necessary to better manage the thermal challenges associated with GaN's lower heat conductivity. Lastly, modifications to the PCB design are also a point of interest. Increasing the area and spacing between polygon planes assigned to each pin will facilitate better management of parasitic effects.

As for the PCB design in Findings 2, it has the potential to be used for the project's continuation, with the ability to handle higher voltages and implement improved parasitic management. A recommended approach involves developing two different designs for the GaN-SiC hybrid and GaN in parallel. Theoretically, this strategy allows for the repetition of experiments while also enabling testing at higher voltages with fewer parasitics. Furthermore, it enables the exploration of diverse tests, such as Double Pulse Tests (DPT) in a Half-Bridge (HB) configuration and thermal analysis. Taking into account the corrections proposed in Findings 1, these adjustments are expected to provide more accurate, determinate, and varied results, providing a robust foundation for future research on the advantages of the GaN-SiC hybrid in power electronics applications.

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Appendices

Appendix A - HB and BDS mixed configuration design

Objective A: Design a single setup that can be reconfigured to have one test circuit to carry out both HB and BDS tests.

In order to conduct this project, it was necessary to use both HB and BDS setups for the DPT. With this, it is expected to create a single setup that can run both tests that is both practical and convenient while still being able to conduct a thermal analysis on it.

Method A: Design a single setup that can be reconfigured to have one test circuit able to conduct both HB and BDS tests.

Using the knowledge of HB and BDS, the team designed a single setup that integrates the HB and BDS into a unique set up. This should be done by finding the parts of both set ups that overlay with each other. Using PSpice, the team analyzed the different possibilities for this setup. Then designed a PCB using the software Altium.

This was constructed while taking into consideration parasitic inductance that could be caused by adding pieces like jumper cables into the PCB, which led the team to choose a copper line to connect and disconnect different parts in the process of switching test set ups. Another aspect the team wanted to investigate was the cleanliness of the design and the speed in which an error could be identified and resolved.

The team also took into consideration the ability of this PCB to run a thermal analysis. This posed a different problem since SiC and GaN have different physical properties for the MOSFET and HEMT respectively. While for the SiC we can use a Power Transistor Test Socket, the GaN had to be mounted to the board.

Findings A: Mixed HB-BDS design

The team was able to create a setup that is possible to adjust in order to run both HB and BDS in a single PCB by using copper lines to adjust the needed circuit path to the one needed at the moment. This, of course, brought with it a certain degree of stray inductance, which the team tried to minimize. During this process, the team came up with two schematics as the base designs, which could be adjusted depending on the configuration needed. These schematics can be seen in Figures A.1 and A.2. In these figures, the red lines represent the connection needed for the HB setup, and the blue lines represent the connection needed for BDS.

The main difference between these two is the decision of which MOSFET of the BDS will be working as the Freewheeling MOSFET of the HB. The circuit in Figure A.1 has the advantage of using one less copper line, which in turn gives it less parasitic inductance. On the other hand, figure A.2 has the advantage of a cleaner design, limiting more of the parasitic inductance to one side of the circuit regardless of which setup is needed. The cleaner design also allows us to see potential issues easily and simplifies the switches between setups visually. The disadvantage is the addition of one more copper line. The team decided to use the schematic of Figure A.2 through this project as the parasitic inductance was minimal in contrast to the convenience of this configuration.

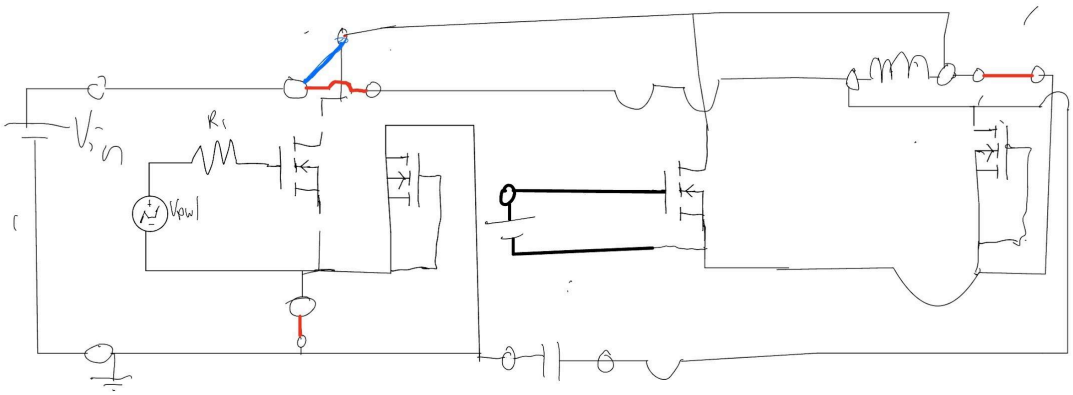

Figure A.1: Schematic of the mixed setups using the rightmost MOSFET of the BDS as the Free-wheeling MOSFET of the HB

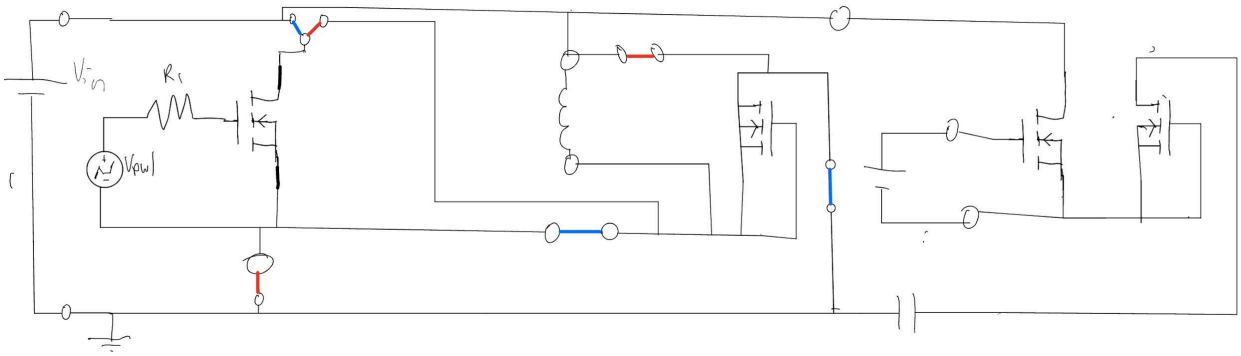

Figure A.2: Schematic of the mixed setups using the MOSFET of the BDS as the Free-wheeling MOSFET of the HB

As a second part, now that a base schematic was chosen, we had to design the PCBs. During the design process of the PCB the team noticed that, by mixing the two set ups, there was a lack of capabilities to do a prototype without compromising stray inductance in the PCB.

Due to a lack of time and problems with the PCB machine, the team was unable to print this prototype. This prototype would allow the team to conduct the tests faster and more conveniently in theory, but it would also run into issues with stray inductance. Adding a film capacitor could possibly offset these issues, but it would be recommended to run a test on stray inductance before testing HB-BDS.

Appendix B - SiC in Parallel and Stand-Alone HB Configuration Development

Objective B: Design an HB setup using GaN or SiC as stand-alone and in parallel.

The next task would be to build the circuit designed in objective 1 of the in parallel to the HB setup. Running tests with different parameters in order to find the fixed values that will optimize the circuit in a DPT, considering that in parallel, the MOS is able to handle twice the amount of current. This is meant to find the values of the inductor(HB), Vin, and resistance that will cause the least amount of power loss and less chance of damaging the devices with current or voltage spikes.

For this, a set of inductors is characterized, and theoretical values are calculated that should be used in order to have a WBG circuit that can handle currents up to 400A and voltages ranging from 200V to 800V for HB setup. This is meant to find the values of the inductor(HB), Vin, and resistance that will cause the least amount of power loss and less chance of damaging the devices with current or voltage spikes.

Method B: Developing the design of a standalone and parallel circuit for a HB set up for SiC configuration.

The team reproduced the setups designed in Method 2 using the SiC using the software PSpice to run simulations of different parameters by using DPT measuring the current in the drain of the driver MOSFET in the HB, while in the BDS, we measured the voltage in the drain of the left-most MOSFET. As seen in Figure B.1.1, where we present the SiC standalone configuration in both BDS and HB setups, and Figure B.2.1, where we can see the GaN standalone configuration in both BDS and HB setups.

The First step was to characterize the inductors. Using the impedance analyzer, characterize different inductor values of inductance, capacitance, and resistance, conducting a frequency domain characterization up to 10MHz. With this characterization, we calculate the total inductance where these values are achieved. This is done to determine the WBG switching frequency when the inductors start to change Rs, capacitance, and inductance. The team conducted the analysis on four inductors, two of 6.2mH and two of 1.8mH. In order to differentiate the inductors of the same rated inductance, the team used electrical tape to mark one and labeled it as 1 or 0 based on whether or not it had tape.

After this is done, set up the inductors in parallel to reduce the amount of internal resistance and total inductance. This would be the inductance to be used in the HB switch setup. In the HB, we would then change the time of the first pulse to achieve a peak current of 300A, then a ten-microsecond deadtime before a second pulse with a width of five microseconds. This will be repeated for the voltage range of 200V-800V in increments of 100V. This is done to check theoretical values and results for current and voltage values on demand in the industry. This was conducted using PSpice simulation software. Using the formula $I = VLdt$ to define the on-time of the driver.

For the HB, the first pulse will be set up to reach a peak current of twice the maximum rated value of the 100°C drain current given in the datasheet of the WBG while using the inductor calculated. Then, after the first pulse, would be a 10 microsecond to make sure that the device is turned off completely, and then a second pulse lasting for 5 microseconds.

We then repeated all of these processes but with additional transistors in parallel and doubled the current since, in parallel configurations, the current is equally divided between the transistors.

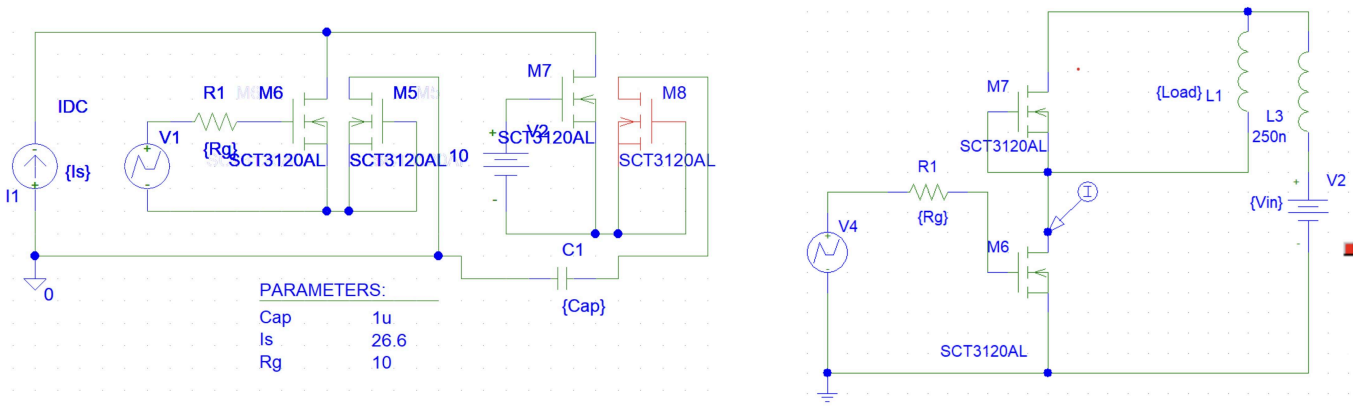

Figure B.1.1: SiC standalone configuration in both BDS(Left) and HB(Right) setups

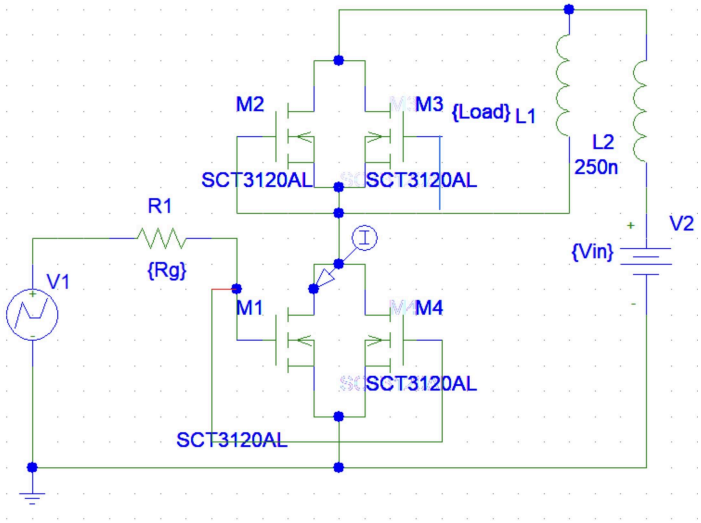

Figure B.1.2: SiC Parallel configuration in HB setups

Findings B: Standalone & Parallel Configuration

The team decided to only use one PCB for both configurations, as seen in figure 5.3. In order to do this PCB, we soldered power transistor test sockets into it. These power sockets act as open circuits if there is no transistor connected, allowing us to alternate between

configurations. The team also decided to add, in parallel to the voltage or current supply, four aluminum electrolytic capacitors in series. These capacitors have a rated voltage of 500VDC which having 4 in series, would allow us to test up to 2kV DC. In parallel to each of these capacitors, there is one resistor to help the capacitor discharge faster and for safety, and a film capacitor to help with stability.

The resistor was chosen based on the formulas of $R = \frac{t*V}{C}$, where t is the time required to discharge the capacitor in seconds, V is the voltage rating of the capacitor and C is the capacitance, and $P = 2 * V^2/R$, this is multiplied by the factor of safety of two to ensure that the resistor will not attain high temperatures that could affect nearby components. Based on the values of the capacitor above, for a discharge time of below 1 second it is needed a resistor of maximum 50 $k\Omega$. For this resistance value, the power rating of the resistor is required to be at least 10W.

For the characterization of the inductors, we had two sets of inductors two large and two small inductors. The small inductors sharply increased in resistance at 0.284 MHz and the large inductors had that spike in resistance at 0.132MHz as seen in Figure B.2.1 and B.2.2. The rest of the characterization can be seen in table B.1

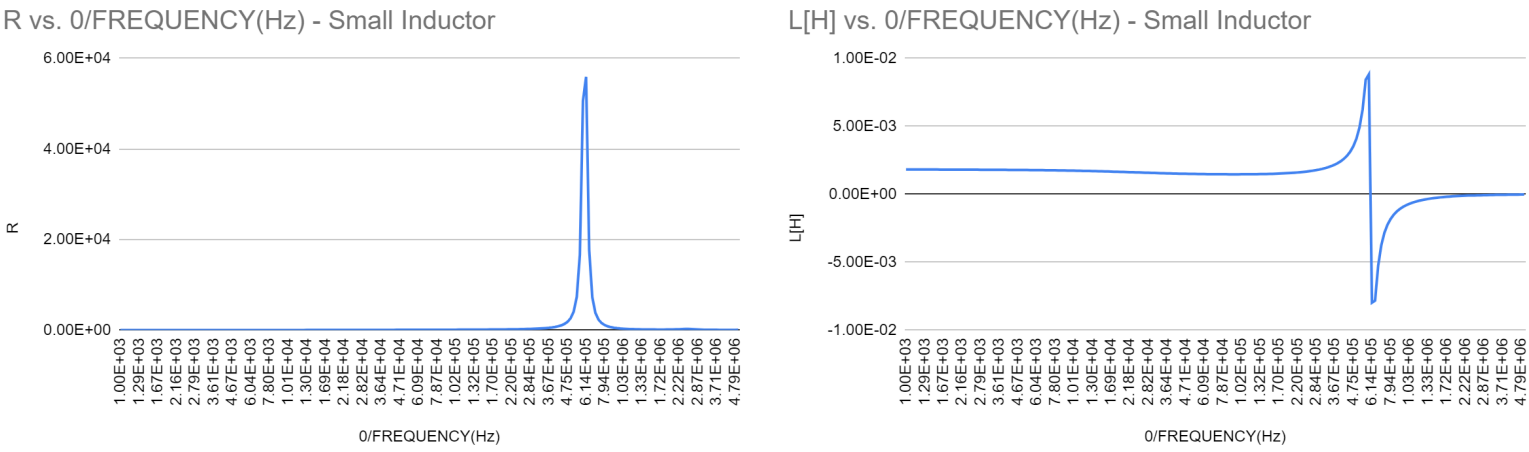

Figure B.2.1: Small inductors Characterization for Resistance and Inductance Vs Frequency

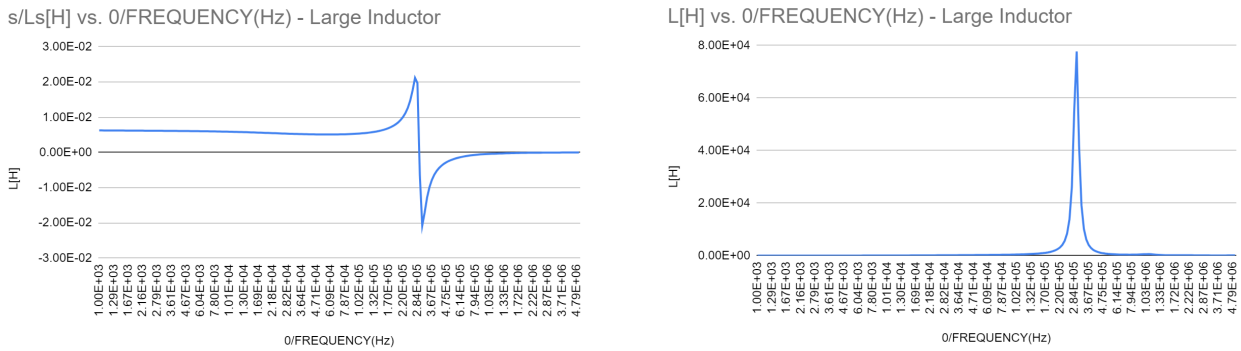

Figure B.2.2: Large inductors Characterization for Resistance and Inductance Vs Frequency

Table B.1: Characterization of the inductors

	Small 1	Small 2	Large 1	Large 2
Ls	1.854mH	1.834 mH	6.253 mH	6.256 mH
Cps	-13.83 μF	.-13.75 μF	-4.039 μF	-4.039 μF
Rs	0.694 Ω	0.684 Ω	2.1 Ω	1.8 Ω

Appendix C -GaN-SiC Hybrid HB Configuration Design and Development

Objective C: Design the HB setup for the GaN-SiC hybrid

The following objective is to add the GaN-SiC hybrid into the mixed setup that was built in objective one. This means the setups will have twice the number of MOS of a SiC in parallel to a GaN. And running simulations with different parameters in order to find the fixed values that will optimize the circuit in a DPT. This is meant to find the values of the capacitor(BDS), inductor(HB), Vin, and resistance that will cause the least amount of power loss and less chance of damaging the devices with current or voltage spikes.

Method C: Designing the hybrid configuration analysis.

The approach is the same as the one for method 2. The main difference is that we need to search for a test socket for the GaN, as it is a HEMT rather than a MOSFET, to be able to test. Since there are a large number of HEMTS with different numbers of pins, this test socket would need to be adjusted based on the needs. After the socket is selected, then it would be needed to readjust the current path to the HEMTS specifications for Gate, Source, and Drain.

Appendix D - Table of Results of Efficiency

Figure D.1: Total data accumulated from Findings 1

Frequency	Load Resistance	Configuration	Input Voltage	Input Current	Input Power	Output voltage	Output Current	Output Power	Power loss	Efficiency
50 kHz	25 Ohm	SiC in Parallel	31	0.24	7.44	13.275	0.529	7.022	0.418	94.39%
			50	0.38	19	21.409	0.853	18.262	0.738	96.12%
			60	0.45	27	25.683	1.023	26.274	0.726	97.31%
			70	0.53	37.1	29.964	1.194	35.777	1.323	96.43%
			80	0.6	48	34.24	1.365	46.738	1.262	97.37%
			90	0.68	61.2	38.52	1.535	59.128	2.072	96.61%
			100	0.75	75	42.813	1.706	73.039	1.961	97.39%
		GaN SiC Hybrid	31	0.24	7.44	13.328	0.532	7.090	0.350	95.30%
			50	0.38	19	21.532	0.859	18.496	0.504	97.35%
			60	0.46	27.6	25.845	1.031	26.646	0.954	96.54%

			70	0.53	37.1	30.157	1.203	36.279	0.821	97.79%
			80	0.61	48.8	34.463	1.375	47.387	1.413	97.10%
			90	0.68	61.2	38.781	1.547	59.994	1.206	98.03%
			100	0.76	76	43.109	1.719	74.104	1.896	97.51%
	45 Ohm	SiC in Parallel	31	0.13	4.03	13.43	0.297	3.989	0.041	98.98%
			50	0.21	10.5	21.613	0.477	10.309	0.191	98.19%
			60	0.26	15.6	25.892	0.571	14.784	0.816	94.77%
			70	0.3	21	30.184	0.667	20.133	0.867	95.87%
			80	0.34	27.2	34.486	0.762	26.278	0.922	96.61%
			90	0.38	34.2	38.787	0.857	33.240	0.960	97.19%
			100	0.42	42	43.112	0.952	41.043	0.957	97.72%
			150	0.64	96	64.66	1.43	92.464	3.536	96.32%
			200	0.85	170	86.21	1.906	164.316	5.684	96.66%
		GaN SiC Hybrid	31	0.13	4.03	13.4	0.297	3.980	0.050	98.75%
			50	0.21	10.5	21.6	0.478	10.325	0.175	98.33%
			60	0.26	15.6	25.94	0.574	14.890	0.710	95.45%
			70	0.3	21	30.27	0.67	20.281	0.719	96.58%
			80	0.34	27.2	34.58	0.765	26.454	0.746	97.26%
			90	0.38	34.2	38.9	0.861	33.493	0.707	97.93%
			100	0.42	42	43.23	0.957	41.371	0.629	98.50%
			150	0.64	96	64.99	1.432	93.066	2.934	96.94%
			200	0.85	170	86.64	1.915	165.916	4.084	97.60%
75 kHz	25 Ohm	SiC in Parallel	31	0.23	7.13	13.098	0.522	6.837	0.293	95.89%
			50	0.37	18.5	21.106	0.84	17.729	0.771	95.83%
			60	0.44	26.4	25.317	1.007	25.494	0.906	96.57%
			70	0.51	35.7	29.528	1.176	34.725	0.975	97.27%
			80	0.59	47.2	33.738	1.344	45.344	1.856	96.07%
			90	0.66	59.4	37.962	1.513	57.437	1.963	96.69%
			100	0.73	73	42.198	1.681	70.935	2.065	97.17%
		GaN SiC Hybrid	31	0.23	7.13	13.083	0.522	6.829	0.301	95.78%
			50	0.37	18.5	21.146	0.844	17.847	0.653	96.47%
			60	0.44	26.4	25.382	1.013	25.712	0.688	97.39%
			70	0.51	35.7	29.17	1.182	34.479	1.221	96.58%

			80	0.59	47.2	33.943	1.35	45.823	1.377	97.08%
			90	0.66	59.4	38.071	1.519	57.830	1.570	97.36%
			100	0.73	73	42.308	1.687	71.374	1.626	97.77%
	45 Ohm	SiC in Parallel	31	0.13	4.03	13.228	0.292	3.863	0.167	95.85%
			50	0.21	10.5	21.34	0.47	10.030	0.470	95.52%
			60	0.25	15	25.371	0.563	14.284	0.716	95.23%
			70	0.29	20.3	29.805	0.657	19.582	0.718	96.46%
			80	0.33	26.4	34.033	0.751	25.559	0.841	96.81%
			90	0.37	33.3	38.264	0.845	32.333	0.967	97.10%
			100	0.42	42	42.523	0.94	39.972	2.028	95.17%
		GaN SiC Hybrid	31	0.13	4.03	13.128	0.29	3.807	0.223	94.47%
			50	0.21	10.5	21.182	0.469	9.934	0.566	94.61%
			60	0.25	15	25.412	0.562	14.282	0.718	95.21%
			70	0.29	20.3	29.815	0.656	19.559	0.741	96.35%
			80	0.33	26.4	34.064	0.749	25.514	0.886	96.64%
			90	0.37	33.3	38.313	0.843	32.298	1.002	96.99%
			100	0.41	41	42.578	0.942	40.108	0.892	97.83%
100 kHz	25 Ohm	SiC in Parallel	31	0.22	6.82	12.875	0.513	6.605	0.215	96.85%
			50	0.36	18	20.725	0.824	17.077	0.923	94.87%
			60	0.43	25.8	24.85	0.988	24.552	1.248	95.16%
			70	0.5	35	28.979	1.153	33.413	1.587	95.47%
			80	0.57	45.6	33.104	1.318	43.631	1.969	95.68%
			90	0.64	57.6	37.237	1.483	55.222	2.378	95.87%
			100	0.71	71	41.379	1.648	68.193	2.807	96.05%
		GaN SiC Hybrid	31	0.22	6.82	12.817	0.511	6.549	0.271	96.03%
			50	0.36	18	20.729	0.827	17.143	0.857	95.24%
			60	0.43	25.8	24.882	0.993	24.708	1.092	95.77%
			70	0.5	35	29.034	1.158	33.621	1.379	96.06%
			80	0.57	45.6	33.179	1.324	43.929	1.671	96.34%
			90	0.64	57.6	37.313	1.488	55.522	2.078	96.39%
			100	0.71	71	41.45	1.653	68.517	2.483	96.50%

	45 Ohm	SiC in Parallel	31	0.13	4.03	13.122	0.29	3.805	0.225	94.43%
			50	0.21	10.5	21.035	0.463	9.739	0.761	92.75%
			60	0.25	15	25.185	0.554	13.952	1.048	93.02%
			70	0.29	20.3	29.342	0.646	18.955	1.345	93.37%
			80	0.33	26.4	33.491	0.739	24.750	1.650	93.75%
			90	0.37	33.3	37.641	0.831	31.280	2.020	93.93%
			100	0.4	40	41.818	0.924	38.640	1.360	96.60%
		GaN SiC Hybrid	31	0.13	4.03	12.97	0.287	3.722	0.308	92.37%
			50	0.2	10	20.918	0.463	9.685	0.315	96.85%
			60	0.24	14.4	25.104	0.556	13.958	0.442	96.93%
			70	0.28	19.6	29.279	0.648	18.973	0.627	96.80%
			80	0.32	25.6	33.45	0.741	24.786	0.814	96.82%
			90	0.36	32.4	37.625	0.833	31.342	1.058	96.73%
			100	0.4	40	41.806	0.925	38.671	1.329	96.68%
125 kHz	25 Ohm	SiC in Parallel	31	0.22	6.82	12.667	0.505	6.397	0.423	93.80%
			50	0.35	17.5	20.371	0.81	16.501	0.999	94.29%
			60	0.42	25.2	24.417	0.97	23.684	1.516	93.99%
			70	0.48	33.6	28.468	1.132	32.226	1.374	95.91%
			80	0.55	44	32.514	1.294	42.073	1.927	95.62%
			90	0.62	55.8	36.566	1.456	53.240	2.560	95.41%
			100	0.69	69	40.651	1.619	65.814	3.186	95.38%
		GaN SiC Hybrid	31	0.21	6.51	12.56	0.501	6.293	0.217	96.66%
			50	0.34	17	20.323	0.811	16.482	0.518	96.95%
			60	0.41	24.6	24.4	0.974	23.766	0.834	96.61%
			70	0.48	33.6	28.466	1.136	32.337	1.263	96.24%
			80	0.55	44	32.525	1.298	42.217	1.783	95.95%
			90	0.62	55.8	36.583	1.459	53.375	2.425	95.65%
			100	0.68	68	40.663	1.622	65.955	2.045	96.99%
	45 Ohm	SiC in Parallel	31	0.13	4.03	12.988	0.287	3.728	0.302	92.50%
			50	0.2	10	20.765	0.456	9.469	0.531	94.69%
			60	0.24	14.4	24.844	0.545	13.540	0.860	94.03%
			70	0.28	19.6	28.927	0.636	18.398	1.202	93.87%
			80	0.32	25.6	32.998	0.727	23.990	1.610	93.71%

			90	0.36	32.4	37.084	0.818	30.335	2.065	93.63%
			100	0.4	40	41.158	0.909	37.413	2.587	93.53%
		GaN SiC Hybrid	31	0.12	3.72	12.75	0.282	3.596	0.125	96.65%
			50	0.2	10	20.567	0.455	9.358	0.642	93.58%
			60	0.24	14.4	24.664	0.546	13.467	0.933	93.52%
			70	0.275	19.25	28.763	0.637	18.322	0.928	95.18%
			80	0.31	24.8	32.856	0.727	23.886	0.914	96.32%
			90	0.35	31.5	36.938	0.818	30.215	1.285	95.92%
			100	0.39	39	41.032	0.908	37.257	1.743	95.53%
150 kHz	25 Ohm	SiC in Parallel	31	0.21	6.51	12.423	0.495	6.149	0.361	94.46%
			50	0.34	17	19.953	0.792	15.803	1.197	92.96%
			60	0.4	24	23.906	0.948	22.663	1.337	94.43%
			70	0.47	32.9	27.865	1.107	30.847	2.053	93.76%
			80	0.53	42.4	31.819	1.265	40.251	2.149	94.93%
			90	0.6	54	35.787	1.424	50.961	3.039	94.37%
			100	0.66	66	39.764	1.581	62.867	3.133	95.25%
		GaN SiC Hybrid	31	0.21	6.51	12.261	0.489	5.996	0.514	92.10%
			50	0.33	16.5	19.829	0.792	15.705	0.795	95.18%
			60	0.4	24	23.8	0.95	22.610	1.390	94.21%
			70	0.46	32.2	27.788	1.109	30.817	1.383	95.70%
			80	0.53	42.4	31.751	1.267	40.229	2.171	94.88%
			90	0.59	53.1	35.713	1.425	50.891	2.209	95.84%
			100	0.66	66	39.695	1.583	62.837	3.163	95.21%
	45 Ohm	SiC in Parallel	31	0.13	4.03	12.818	0.283	3.627	0.403	90.01%
			50	0.2	10	20.437	0.449	9.176	0.824	91.76%
			60	0.24	14.4	24.429	0.538	13.143	1.257	91.27%
			70	0.27	18.9	28.424	0.624	17.737	1.163	93.84%
			80	0.31	24.8	32.412	0.714	23.142	1.658	93.32%
			90	0.35	31.5	36.398	0.803	29.228	2.272	92.79%
			100	0.39	39	40.11	0.892	35.778	3.222	91.74%
		GaN SiC Hybrid	31	0.12	3.72	12.487	0.276	3.446	0.274	92.65%
			50	0.19	9.5	20.13	0.445	8.958	0.542	94.29%
			60	0.23	13.8	24.134	0.534	12.888	0.912	93.39%

			70	0.27	18.9	28.131	0.623	17.526	1.374	92.73%
			80	0.3	24	32.125	0.711	22.841	1.159	95.17%
			90	0.34	30.6	36.123	0.799	28.862	1.738	94.32%
			100	0.38	38	40.139	0.888	35.643	2.357	93.80%

Appendix E - Table of Purchased Components

Table E.1: List of Purchased Components

	Component	Part Name		Quantity	Datasheet	Link
1	Electrolytic Capacitor	ALS70A103NT500	47 kOhm	4	https://www.mouser.jp/datasheet/2/447/KEM_A4075_ALS70_71-3316257.pdf	https://www.mouser.jp/ProductDetail/KEMET/ALS70A103NT500?qs=AQlKX63v8Rt%2FDHfp%252BJsVUQ%3D%3D
2	Discharge resistor	YP1047KJ	10mF	4	https://www.mouser.jp/datasheet/2/418/4/NG_DS_1773300_A-726339.pdf	https://www.mouser.jp/ProductDetail/TE-Connectivity-Holsworthy/YP1047KJ?qs=U0tyJ2PSxbZKZky%2FBHEOdw%3D%3D
3	Banana plug	Hxchen Mini 2mm Banana Female Plug Socket		1	N/A	https://www.amazon.com/Hxchen-Banana-Binding-Terminal-Connector/dp/B07VJC4LB7