High Frequency DC/DC Boost Converter

A Major Qualifying Project

submitted to the Faculty

of the

WORCESTER POLYTECHNIC INSTITUTE

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Degree of Bachelor of Science

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by

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Ina Duka

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Christopher Noble

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APPROVED:

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Professor John A. McNeill, Advisor

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4. Abstract

The goal of this work was to design and test a functional proof of concept of a high frequency DC to DC boost converter. The scope of this work included the design, simulation, part selection, PCB layout, fabrication, and testing of the three major design blocks. The design uses a closed loop error amplifier circuit, a power stage, and a ramp waveform generator circuit. The switching frequency will be adjustable, with a maximum goal of 20MHz.

5. Acknowledgements

The team would like to thank Professor McNeill for all of his support over the course of this project; for introducing us to the concept of a boost converter to examining our circuits for every last detail; and for allowing us to be the best engineers we can be. He was always willing to help and always kept our project in his thoughts.

The team would also like to express our deepest gratitude to the engineers and mentors at Draper Laboratory. The team would like to thank Linda Fuhrman and Peter Miraglia who were champions for the project. The team would like to thank Tim Nougebauer for his power electronics expertise.

And finally, to the people who really made our project a reality: thank you to Jim Huang for your willingness to help us learn and even learn with us along the way. Thank you to Arturo Gossage for your technical expertise and hands-on lab help. And finally, thank you to John Lachapelle for making sure our project was on track from start to finish.

6. Executive Summary

The project dealt with designing a high frequency DC/DC boost converter using commercially available parts. It was conducted on site at Draper Laboratory located in Cambridge, MA with support from Worcester Polytechnic Institute located in Worcester, MA.

Draper Laboratory is a non-profit company that specializes in the development of state-of-the art technology. The project was initialized when a client of Draper Laboratory's contracted them to complete a project involving the design of miniature high-power amplifier. The first step in this process is the creation of high frequency DC/DC boost converter.

A DC/DC boost converter deals with taking in an input voltage and producing a higher voltage. Most commercially available boost converters cannot exceed a frequency of 5MHz. The boost converter required for this project needed to be capable of operating at a frequency of 20MHz, four times larger than what is commercially available.

The project team worked to design, review, lay-out, build, solder and test their boost converter. The final outcome is a fully functional continuous conduction mode boost converter soldered to a printed circuit board. It is capable of achieving a constant 12V output with 50-100Ω loads from a 3.3-5V input. The inductor size is reduced from 680µH to 400nH due to the high frequency. The capacitor was also reduced from 4.7µF to 1.8µF. Finally, the efficiency was calculated to be greater than 55%.

In conclusion, the project was completed successfully with both participating parties, Draper Laboratory and Worcester Polytechnic Institute, having furthered their working relationship and continuing to advance the field of electrical and computer engineering.

7. Introduction

Power management is becoming a very important factor in the electrical engineering industry. With progresses in electronics and technology comes a reduction in available space for circuits, and thus comes a need for reducing the size of power management components of electronic devices.

Draper Laboratory is a not-for-profit company located in Cambridge, MA that specializes in developing state-of-the-art technology for all types of applications. Draper has developed a technology that miniaturizes electronics called Integrated Ultra High Density or iUHD. One of Draper's customers has expressed interest in having the engineers at Draper create a miniaturized high power amplifier. The overall project will take several years to complete, but the first step is to verify the proof of concept of a high frequency DC/DC boost converter for the power management stage. Increasing the switching frequency of the boost converter will allow for smaller passive component values and will allow the whole device to be militarized with minimal additional effort.

The goal of this project was to develop a device and a test plan for verifying the proof of concept of a high frequency DC/DC boost converter using commercially available parts. The overall boost converter consists of three specific modules, the triangle wave generator, the open loop boost converter, and finally, the compensation network.

The scope of this project was to design, review, lay-out, build, solder and test a functional prototype of a high frequency DC/DC boost converter. Because of the time restrictions, the entire process had to be performed at the Draper facilities in Cambridge.

8. Background

The starting point to this project was the table shown below, Table 1. This table lists the parameters that were specified by John Lachapelle, the project sponsor, for the teams' boost converter. The team initiated the research by investigating the current boost converters offered on the market to see whether there was a close match.

Parameter	Minimum	Typical	Maximum	Comment
Input Voltage	3.3V		5V	Lithium ion cell phone battery
Output Voltage		12V		Supply RF power amplifier (PA)
Output Power		2W	2.5W	Allow optimization of PA V_{DD}
Efficiency	50%	70%	90%	
Switching Frequency	1MHz	20Mhz	30MHz	
Ripple V		10mVpk-pk		

Table 1: Range of Boost Converter Specifications

The team searched for comparable boost converters, shown in Table 2. Analog Devices (ADI) and Texas Instruments (TI) have a variety of integrated boost converters (Digikey.com). Many of the TI and ADI boost converters are designed to step up the voltage to power LCD screens. The teams' project called for a higher power application. For the most part, these boost converters have a fixed switching frequency; only a few have an adjustable switching frequency. This provides the team with another reason to build their own boost converter.

Model (Boost)	Vin			Vout			Switch Frequency			Current
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Max
TPS61086	2.0	5.0	5.5	5.0	12.0	18.0	1 MHz		1.4 MHz	2 A
BP5311A	4.5	5.0	5.5	28.0	29.5	31.0				25 mA
ADD8754	3.0		5.5			20.0	650 kHz		1.2 MHz	2.6 A
MAX8758ETG	1.8		5.5	4.5		13.0	990 kHz		1.38 MHz	10 mA
TPS61093	1.6		6.0	1.6		17.0	1.0 MHz		1.4 MHz	.3 A
TPS61241	2.3		5.5	5.0		5.0	3.8 MHz		4.2 MHz	.6 A
TPS61175	2.9		18.0	2.9		38.0	2.0 MHz		2.4 MHz	3 A
UC2577-ADJ	3.0		40.0	5.0		60.0	50 kHz		54 kHz	3 A
ADP5025	2.5		5.5			5.0	2.3 MHz		2.7 MHz	1.2 A

Table 2: Manufactured Boost Converters

A visual of Current Limit vs. Switching Frequency on a log-log scale of the boost converters from the above table is shown below.

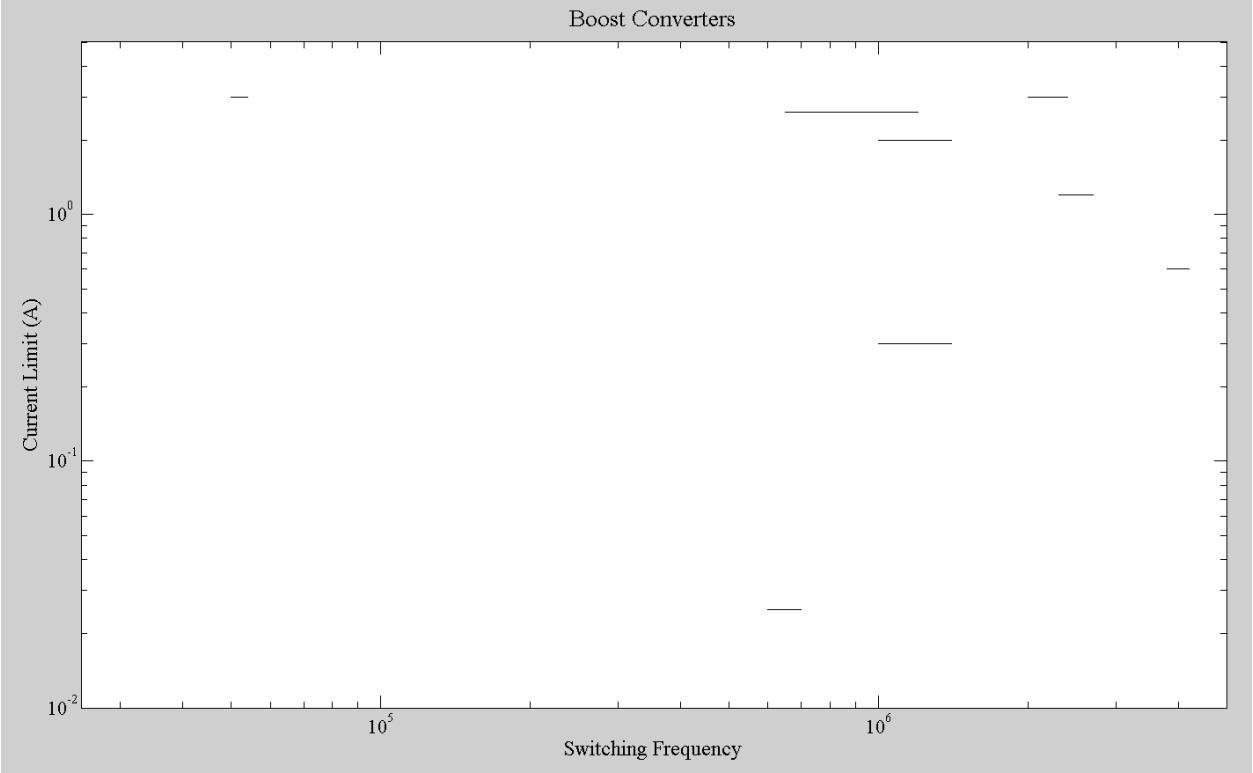

Figure 1: Manufactured Boost Converters Visual (Log-Log Scale)

8.1 What is a DC/DC Boost Converter?

Boost converters are essentially a step-up power converter that take in a low voltage input and provide an output at a much higher voltage. A block diagram of an ideal dc/dc boost converter is shown in the figure below. [7]

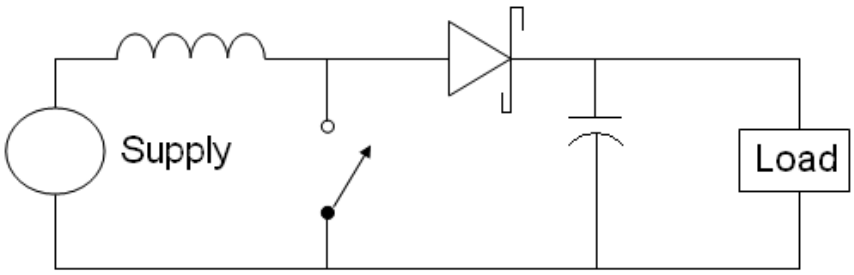

Figure 2: Open Loop Boost Converter [2]

The input and output voltage relationship is controlled by the switch duty cycle, D, according to the equation below. [7]

$$V_{OUT} = \left(\frac{1}{1-D}\right) V_{IN}$$

Equation 1: Input/Output Characteristic of a Boost Converter

An ideal boost converter is lossless in terms of energy, so the input and output power are equal. In practice, there will be losses in the switch and passive elements, but efficiencies better than 90% are still possible through careful selection of system components and operating parameters such as the switch frequency.

The internal operations of a boost converter can be thought of as a charge storage and transfer mechanism. There are two states, on and off. More detail about these operations will be covered in section 8.2.1.

8.2 Different methods for achieving a DC/DC Boost Converter

To build this boost converter that meets the teams' specifications the team needs the power stage that will provide the 12V output from a 3.3V input. This circuit will be the daughterboard of the design. To set the desired frequency for this converter the teams needs to design a pulse width modulation (PWM) circuit up to 20MHz to drive the boost converter. A third circuit is needed to compensate for any variation in the output. This stage is called the error amplifier or control loop and monitors the output for a constant V_{out}. These three different stages make up the design for a high frequency DC/DC boost Converter with a control loop. Figure 3 shows a block diagram for the boost converter.

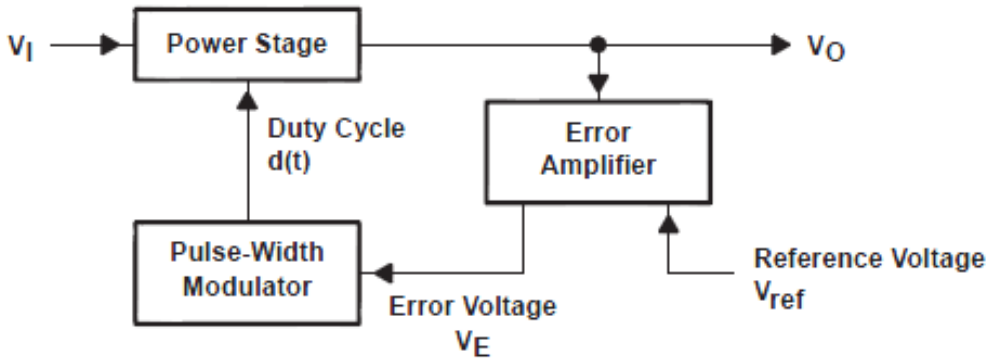

Figure 3: Building Blocks of a Boost Converter System [11]

The power stage has two inputs: the input voltage, V_I and the duty cycle, d(t). The switching is controlled by the duty cycle. It is a logic signal input. This input controls the power stage and, as will be discussed in further detail in the following section, the output voltage. [1]

The only nonlinear components in the power stage are the switching devices. The rest of the components are linear elements. Over the switching cycle, a linear model of just the non-linear components can be obtained if the voltages and currents of such components are to be averaged. As such, a model for the switching devices can be derived. This model is known as the Pulse-Width Modulator switch model.

The power stages operate in two modes: continuous conduction mode and discontinuous conduction mode. The modeling of the PWM switch is discussed in the following section.

8.2.1 Power Stage

The power stage can operate in continuous or discontinuous inductor current mode. In continuous inductor current mode (CCM), current flows continuously in the inductor during the entire switching cycle in steady-state operation. The current never reached zero. In discontinuous inductor current mode (DCM), inductor current is zero for a portion of the switching cycle. It starts at zero, reaches a peak value, and returns to zero during each switching

cycle. To decide which mode the team needed to operate in, the team looked at the input-to-output relationship for the two modes.

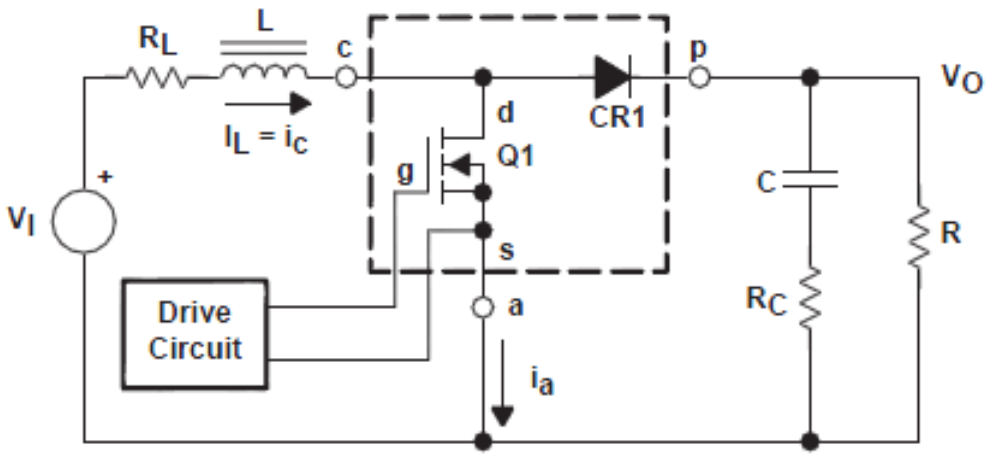

Figure 4: Power Stage of a Boost Converter [11]

The continuous conduction mode of a boost converter assumes two states for each switching cycle. Figure 5 will be used as a reference in the following pages. When in the 'on' state, Q1 will be on and CR1 (diode) will be off. In the 'off' state CR1 will be on. [11]

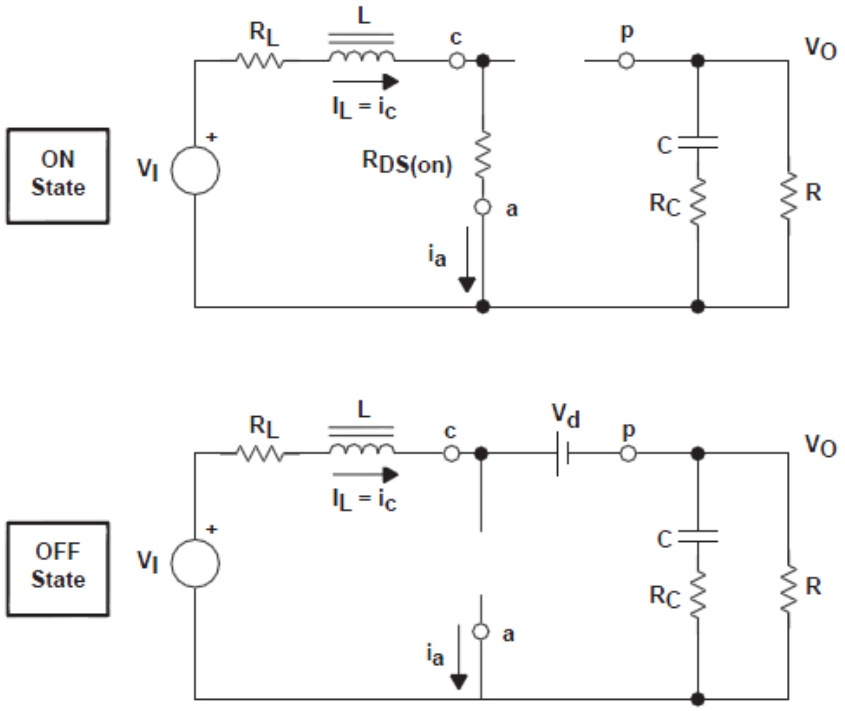

Figure 5: Modes of Switching in a CCM Boost Converter [11]

The duration of each state will vary. The duration of the 'on' state can be found using the expression T_{on} = D x T_s. In the expression, 'D' is the duty cycle. The cycle is set by the control circuit. The duty cycle is set by a ratio of the time 'on' over the complete switching cycle expressed as T_s. The duration of the 'off' state is expressed as T_{off} = (1-D) x T_s. Figure 6 shows waveforms of the two different times, 'on' and 'off'. [11]

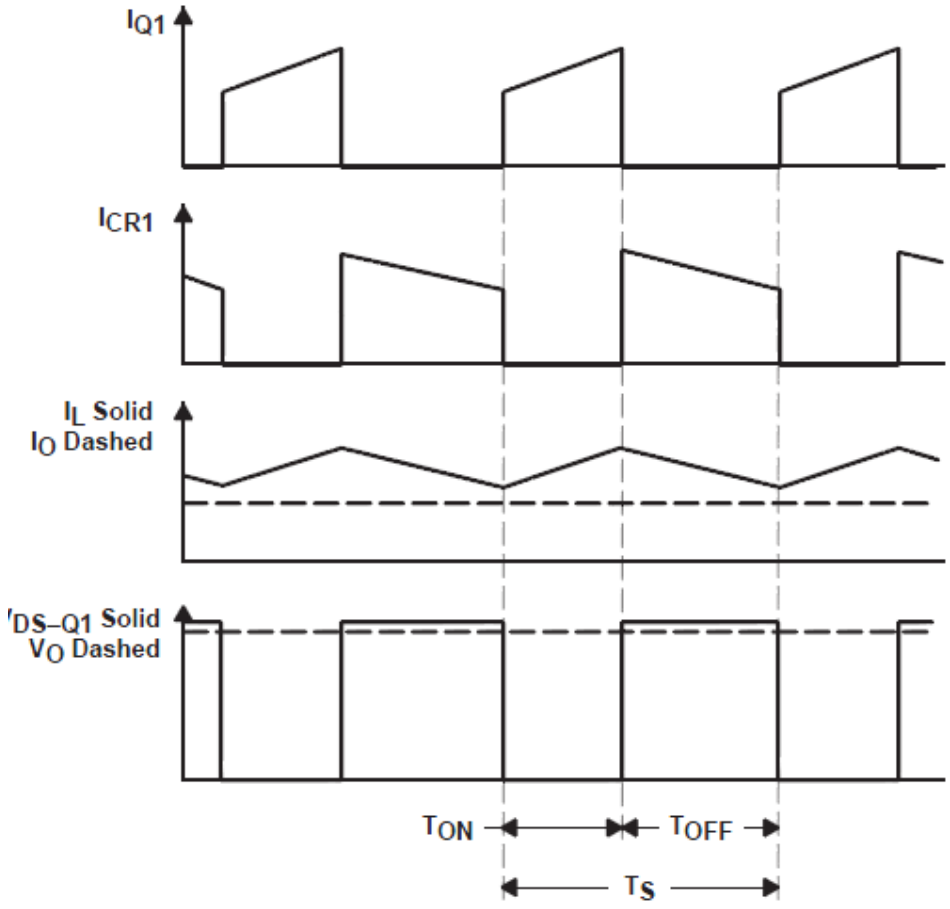

Figure 6: Currents Through the Circuit in Relation to the Duty Cycle [11]

Referring to Figure 4 and the 'on' state in Figure 5, Q1 will have a low drain-to-source resistance, labeled $R_{DS(on)}$, which has a small voltage drop of V_{DS}. The inductor will also experience a small voltage drop equivalent to I_L x R_L. Due to this occurrence the input voltage, labeled V_I, will be applied across the inductor 'L'. During this time the diode CR1 will be in reverse bias, and as such, switched off. Applied to the right side of inductor 'L' is the MOSFET

'on' voltage, V_{DS}. The inductor current will flow from the input source, V_I, through Q1 and then to ground. Using the expression: $V_I-(V_{DS}+I_L \times R_L)$, the voltage across the inductor can be found. This voltage will remain constant. Since the voltage remains constant the current in the inductor will increase linearly.

Referring again to Figure 4 and the 'off' state in Figure 5, assuming Q1 is off, there will be a high drain-to-source impedance. Since the current inside an inductor cannot change instantaneously the current will shift from Q1 to CR1. As the inductor current decreases the voltage across the inductor reverses polarity. It will stay in this state until the rectifier CR1 becomes forward biased and switches on. The voltage to the left of inductor L remains the same as before. However, the voltage applied to the right side of the inductor now becomes the output voltage, V_O. Flowing from the input voltage source, V_I, through CR1 to the output capacitor is the inductor current. The voltage across the inductor will remain constant as in the 'on' state, and will equal to $(V_O + V_d + I_L \times R_L) - V_I$. The applied voltage will be negative. The inductor current will decrease when it is in the off state. The current will decrease linearly.

Under steady state conditions, the current increase during the on state and the current decrease during the off state, $\Delta I_L(-)$ and $\Delta I_L(+)$ respectively, are equal. The expressions for finding $\Delta I_L(-)$ and $\Delta I_L(+)$ are in the equation below. For simplification the output voltage was assumed to be constant and to have no AC ripple. This simplification is justified as the ac ripple voltage is designed to be far smaller than the dc output voltage [11]

$$\Delta I_L(-) = \frac{(V_O + V_d + I_L \times R_L) - V_I}{L} \times T_{OFF}$$

$$\Delta I_L(+) = \frac{V_I - (V_{DS} + I_L \times R_L)}{L} \times T_{ON}$$

Equation 2: Slope of the Current Through the Inductor in CCM

To get the expression for steady state for the voltage out, V_O, use Equation 3. To alter V_O, the duty cycle, D, must be adjusted. The duty cycle will always remain greater than the input.

$$V_O = \frac{V_I - I_L \times R_L}{1-D} - V_d - V_{DS} \times \frac{D}{1-D}$$

Equation 3: Output Voltage of the Open Loop Boost Converter

The expression in Equation 3 can be simplified further. In order to achieve this simplification, set V_{DS}, V_d and R_L to zero. This simplification can be done since it can be assumed that those values are minute enough to be ignored. When this is applied the expression now becomes that of the equation below. [11]

$$V_O = \frac{V_I}{1-D}$$

Equation 4: Simplified Output Voltage of Ideal Boost Converter

A way to look at the operation of the circuit would be to imagine the inductor as an energy storage device. When Q1 is on, there is energy being added to the inductor. Likewise, when Q1 is off, the inductor along with the input voltage source deliver energy to the load and output capacitor. If the 'on' time is left longer the inductor will have more energy delivered to it and then during the 'off' time it will increase the output voltage.

The relationship between the average of the inductor current and the output current is that they are not equal. The average inductor current is equal to the output current over a complete switching cycle. This is due to the current in the output capacitor equaling zero. This relationship is given in the equation below.

$$I_{L(Avg)} = \left(\frac{I_O}{1-D}\right)$$

Equation 5: Average Current Through the Inductor Based on the Duty Cycle

The discontinuous conduction mode will have various different effects on the system. Observing Figure 6, it can be seen that if the output load current is reduced to lower than the critical current level, then the inductor current will be zero. It will remain zero for only part of the switching cycle. If the inductor current was to try and be lower than zero, it would fail and remain at zero until the start of the next switching cycle. Discontinuous conduction mode has three switching stages rather than the two of continuous conduction mode. The figure below shows the boundary between discontinuous and continuous modes, where the inductor current falls to zero and the next switching cycle starts instantaneously.

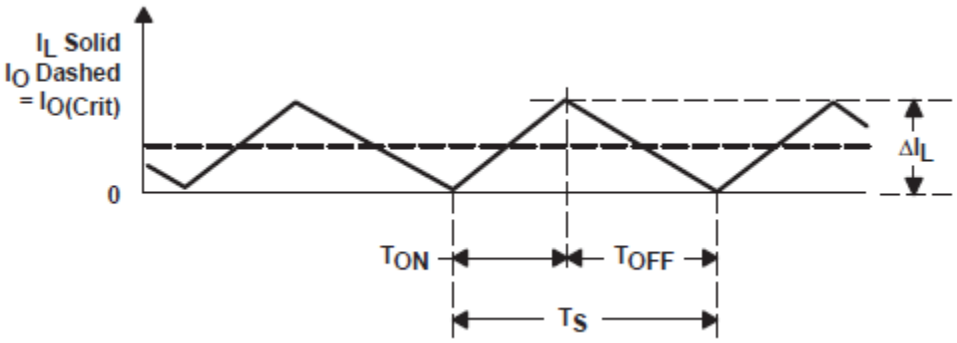

Figure 7: Current Rise and Fall in a CCM Boost Converter [11]

If the output load current is further reduced, the power stage goes into discontinuous current conduction mode. The power stage frequency will be quite different in this mode compared to continuous mode. Furthermore, the input to output relationship will vary drastically. Figure 9 shows this relationship.

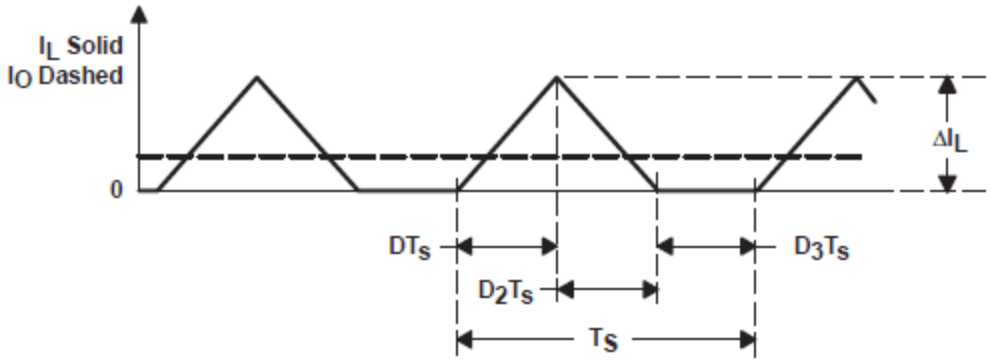

Figure 8: Current Rise and Fall in a DCM Boost Converter [11]

The three states that the power stage assumes in the discontinuous current mode are: 1) 'on' state, when Q1 is on while CR1 is off, 2) 'off' state, where Q1 is off while CR1 is on, and 3) 'idle' state where both Q1 and CR1 are off. Only the third state is unique to the discontinuous current mode, the other two are the same as the continuous current mode.

To find the duration of the 'on' state, the expression $T_{ON} = D \times T_s$. The duration of the 'off' state is found using the expression $T_{OFF} = D2 \times T_S$. The 'idle' state is found by using $T_S - T_{ON} - T_{OFF} = D3 \times T_S$. The time of each state can be seen in Figure 9.

Using the same logic as in the previous section, the conclusion for the inductor current increase and decrease expressions are shown in Equation 6.

$$\Delta I_L\,(+) = \frac{V_I}{L} \times T_{ON} = \frac{V_I}{L} \times D \times T_S = I_{PK}$$

$$\Delta I_L\,(-) = \frac{V_O - V_I}{L} \times T_{OFF} = \frac{V_O - V_I}{L} \times D2 \times T_S$$

Equation 6: Slope of the Current Through the Inductor in DCM

Just as in the continuous conduction mode, the current increase, $\Delta I_L(+)$, and the current decrease, $\Delta I_L(-)$, are equal in the 'on' state. As such, it is possible to find an expression for the voltage conversion ratio. This expression is given in Equation 7.

$$V_O = V_I \times \frac{T_{ON} + T_{OFF}}{T_{OFF}} = V_I \times \frac{D + D2}{D2}$$

Equation 7: Rising Slope of Current Through the Inductor

In order to find the output current the expression in Figure X11 is used.

$$I_O = \frac{V_O}{R} = \frac{V_I \times D \times D2 \times T_S}{2 \times L}$$

Equation 8: Current Output in a DCM Boost Converter

The output voltage can be found by using the expression in Equation 9. Equation 9 demonstrates a major difference between the conduction modes. In the discontinuous conduction mode, the voltage conversion relationship depends on multitude of factors: the input voltage, duty cycle, power stage inductance, switching frequency and the output load resistance. The voltage conversion relationship for the continuous conduction mode is only dependent on two factors: the input voltage and the duty cycle.

$$V_O = V_I \times \frac{1 + \sqrt{1 + \frac{4 \times D^2}{K}}}{2}$$

$$K = \frac{2 \times L}{R \times T_S}$$

Equation 9: Output Voltage Equation of a Boost Converter in DCM

For this project the continuous conduction mode was chosen since it gives more freedom in choosing parts. The project requires a switching frequency boost converter therefore since the CCM depends only on two factors it allows for a variety of operation frequencies and passive component values.

8.2.2 Pulse Width Modulation (PWM)

The fundamental principle involved in making a boost converter is creating a square pulse to control the switching of the MOSFET. This square pulse is called the duty cycle and

this duty cycle (D) controls the output voltage. The transfer function is derived by the following set of equations. Figure 9 is the ideal gate voltage to be able to switch the MOSFET and create a boosted output voltage. The y-axis shows V_{GS} (V) and the x-axis shows the time interval of the signal.

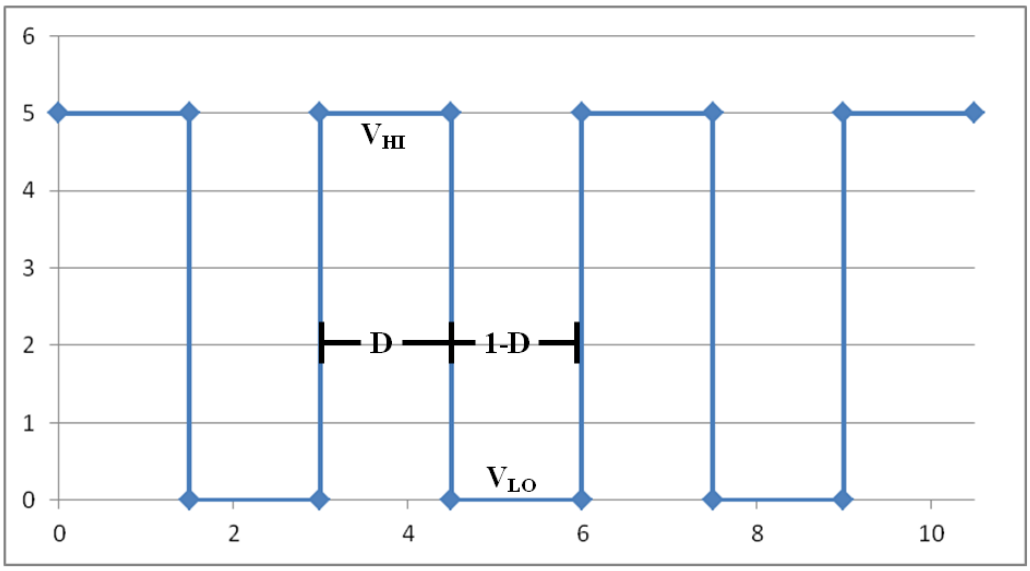

Figure 9: Gate Voltage on MOSFET

As the MOSFET gate switches to 0V, current is no longer sourced directly to ground, thus forcing current to the output. Conversely, when the gate is switched to 5V, the current in the inductor flows directly from the drain to the source which is connected to ground creating different voltages across the inductor. The voltage across the inductor is shown in Figure 10 and the voltage changes with the duty cycle.

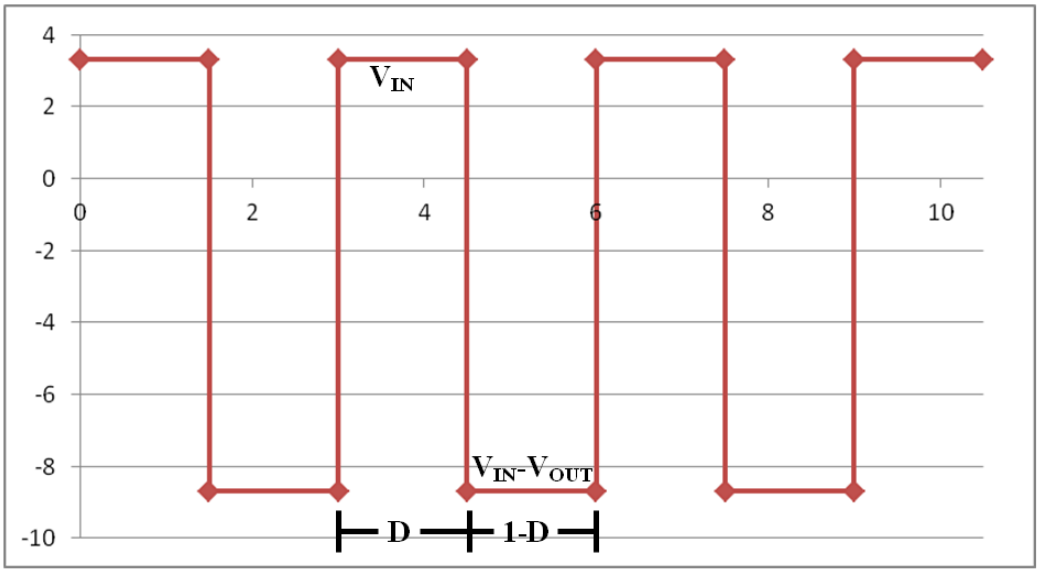

Figure 10: Voltage Across the Inductor

The voltage across the inductor while VGS is at 5V is equal to VIN. The voltage across the inductor while VGS is at 0V is equal to VIN-VOUT. Because the constant voltages are applied to the inductor, the current through the inductor ramps up and down linearly with time according to Equation 10.

$$V_L = L\frac{di}{dt}$$

Equation 10: Voltage Current Relationship in an Inductor

The rising slope of the current through the inductor is show in Equation 11.

$$\frac{V_{IN}}{L}$$

Equation 11: Rising Slope of Current Through the Inductor

The falling slope of the current through the inductor is show in Equation 12.

$$\frac{V_{IN} - V_{OUT}}{L}$$

Equation 12: Falling Slope of Current Through the Inductor

Based on the slope of the rising and falling slopes of the current through the inductor and the fact that the time duration is a known entity, the transfer function can be computed. The

relationship between the slope and time duration is shown in Figure 11 where the y-axis represents an arbitrary current value and the x-axis represents the time interval.

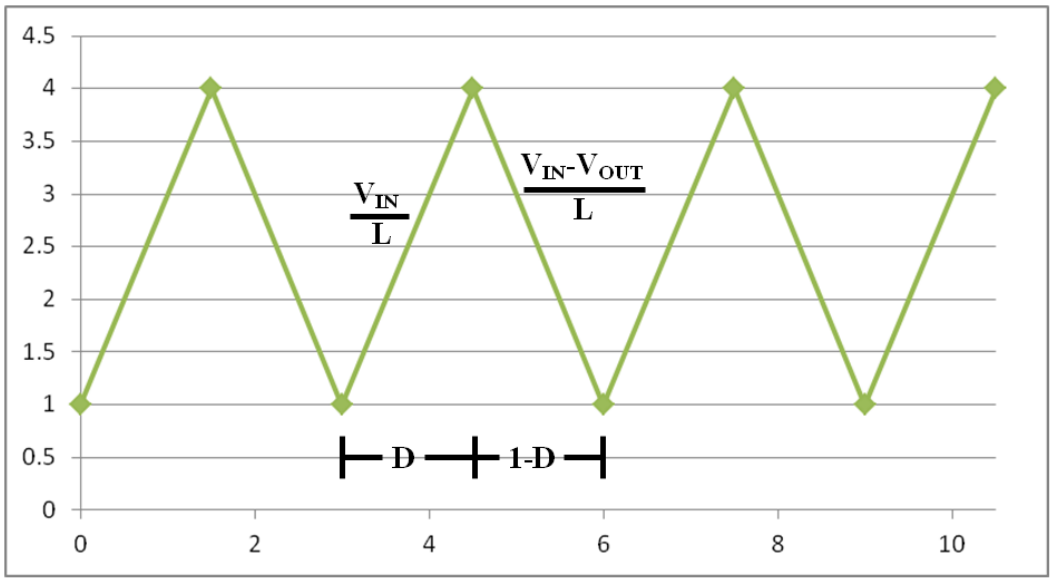

Figure 11: Current Through the Inductor

After determining the slope and time interval, Equation 13 is derived.

$$\frac{V_{IN}}{L}(D) + \frac{V_{IN} - V_{OUT}}{L}(1 - D) = 0$$

Equation 13: Duty Cycle and Current Relationship

Algebraic steps were used to isolate V_{OUT} which yields Equation 14.

$$V_{OUT} = \frac{V_{IN}D}{1 - D} + V_{IN}$$

Equation 14: V_{OUT} of the Boost Converter

Lastly, the transfer function of the whole system is shown in Equation 15 below.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D}$$

Equation 15: Transfer Function of the Boost Converter

The duty cycle of V_{GS} is what allows a boost converter to function. As D increases, the gain also increases. In order to create a duty cycle, a PWM needed to be created. There are several methods of creating a PWM. The first of which is to use a function generator that can

output an adjustable duty cycle square wave at a frequency up to 20MHz. However, most function generators cannot produce square waves up to 20MHz. The next method for creating a PWM is to compare a ramp wave to a DC value. As the DC value decreases or increases, the duty cycle increases or decreases respectively. This method is shown in Figure 12 below.

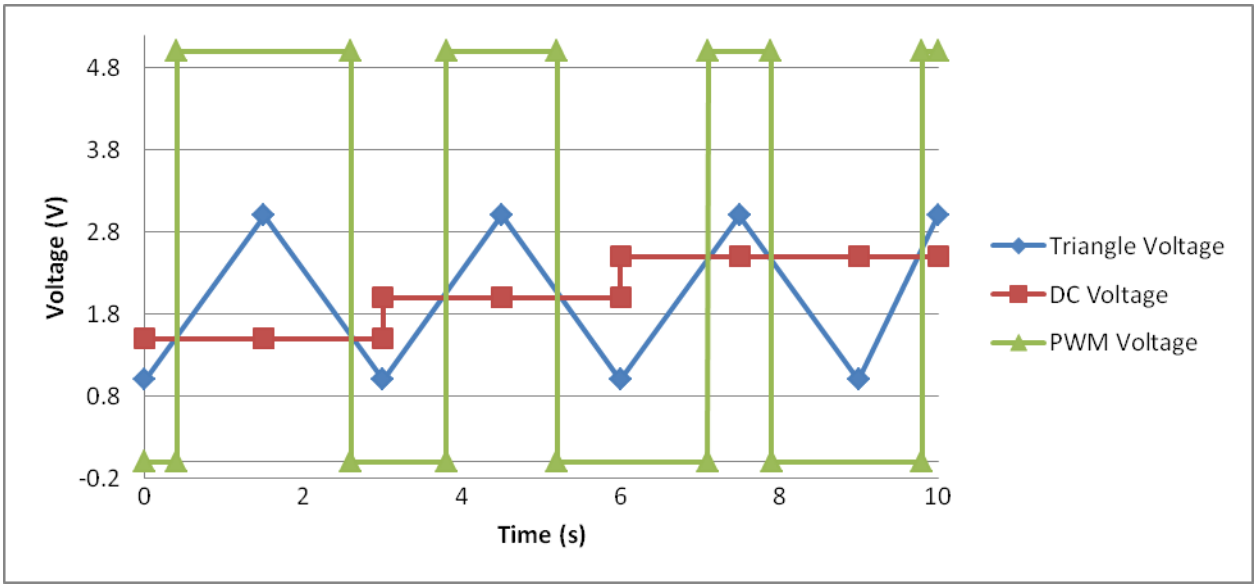

Figure 12: Creating a PWM by Comparing Two Waveforms

A triangle waveform is one wave that can be used to create a PWM. The other waveform is a saw tooth wave. The PWM created by using a saw tooth wave is shown in Figure 13 below.

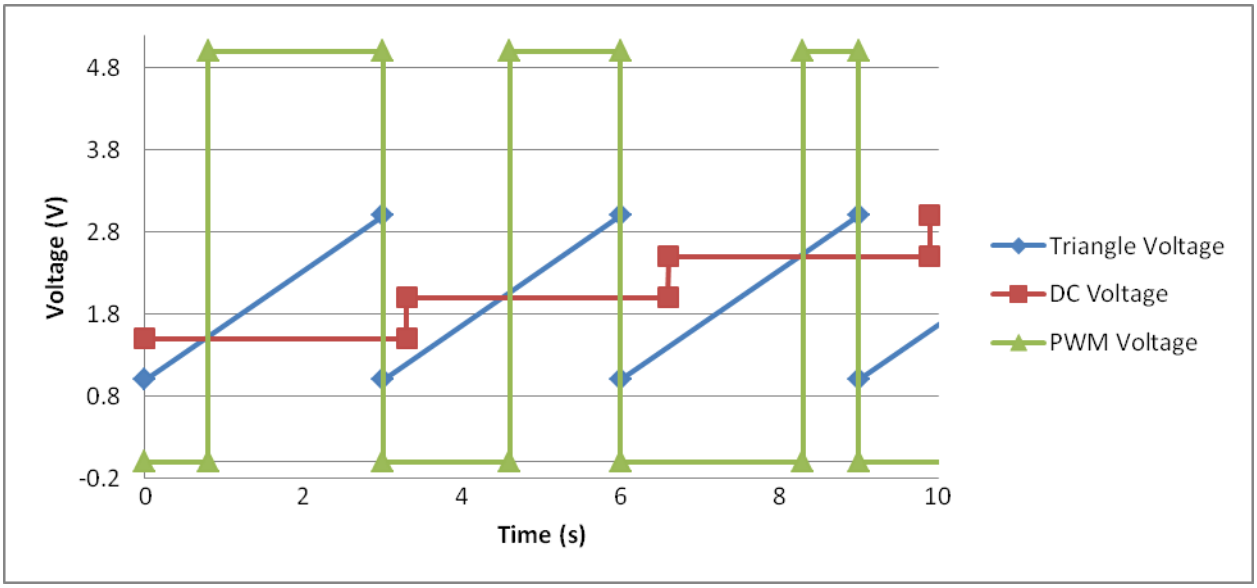

Figure 13: Creating a PWM by Comparing Two Waveforms

Either a saw tooth or a triangle wave would work to create a PWM needed for the boost converter, but the triangle is an easier shape to create and the Triangle has a few distinct advantages over the saw tooth. "An intrinsic advantage of modulation using a triangle carrier wave is that the odd harmonic sideband components around odd multiples of the carrier fundamental and even harmonic sideband components around even multiples of the carrier fundamental are eliminated." [8] Additionally, a small change in the input voltage using the triangle wave will result in a larger change in the PWM than when using a saw tooth.

8.2.3 Control Loop

The stability of the boost converter will depend on the type of control loop. When using the voltage control loop a CCM will have certain complications. Although the DCM will not fall into these problems, it was proved to be insufficient for requirements of the project in section 8.2.1.

A CCM will have a right-half-plane (RHP) zero that is linked to the system transfer function. The RHP zero will be highly responsive to positive feedback. The behavior that it would exhibit would be that if there was an instantaneous and unexpected increase in the load that is drawn from the boost converter, the output voltage would drop. The converter would then respond with a longer duty cycle. Furthermore, if there was a longer switch on time then there will be a shorter diode conduction time which would result in the output capacitor being charged and would initially cause the output voltage to decrease. [2]

There are ways to compensate for this occurrence. A preferable solution is to wait and observe what the long term trend will be prior to adjusting the duty cycle. This is achieved by having the crossover frequency lower than the RHP zero frequency.

Refer to Figure 15 for the following explanations. Figure 15 shows the control-to-output gain of the CCM, The low ESR of the output capacitor, C_{OUT}, results in the frequency of ESR, f_{ESR}, being greater than the right hand pole frequency, f_{RHP}. To help suppress the destabilizing effects of the RHP zero, the crossover frequency, f_C, is required to be one third of f_{RHP}. With this relationship, f_C becomes the upper limit and will thus limit the converter bandwidth.

There is also an existence of the load dependant peaking. This is associated with the double pole at f_{LC}. In order to compensate for the peaking effect on the crossover frequency, f_C is placed at a frequency that is a minimum of three times higher the than that of f_{LC}. With this, f_C is less than one third of f_{RHP}, f_{LC} is less than one ninth of f_{RHP}, the following equations can be written:

$$f_{LC} = (0.1) \times f_{RHP}$$

Equation 16: Compensation Frequency of the LC Network

$$f_C = (0.3) \times f_{RHP}$$

Equation 17: Compensation Frequency of the Crossover Frequency

A type-III compensator has to be designed in such a way that f_C is going to cross over the required frequency. This frequency is (0.3) x f_{RHP}.

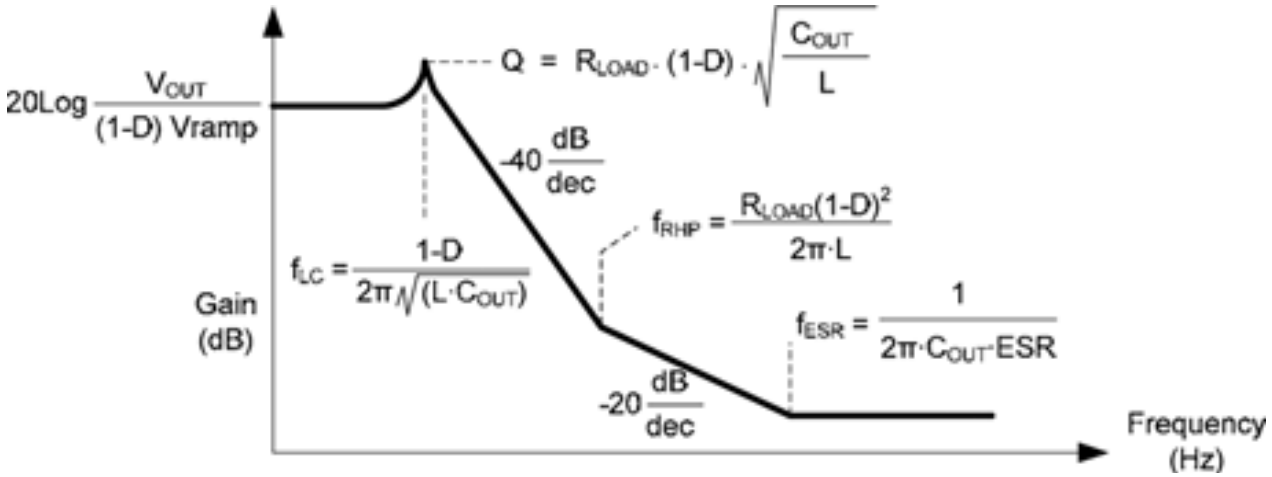

Figure 14: Bode Plot of Open Loop Boost Converter [10]

8.3 Potential Concerns

The boost converter itself has some inherent concerns. The first of which is a zero in the right half plane. Without compensating for this additional zero could lead to an unstable control loop. Additionally, the boost converter draws a significant amount of current in order to boost the voltage at the output. The traces on the board need to be able to carry up to a few amps of current without burning out or inhibiting current flow. Lastly, all of that current drawn by the boost converter will create more heat dissipation than expected because of the higher practical ESR in components on the board, so proper dissipation techniques need to be taken into consideration.

The other concerns lay with the triangle wave generator boards. The original design relies completely on timing delays and capacitor discharge through the on resistance of a MOSFET. The simulations may have used the actual spice model of the part the team ordered for the boards, but the tolerance on the devices vary and can create problems with the rate of charge and discharge. Additionally, MOSFETs turn "on" and "off" by charging gate capacitors. Capacitors charge with current. According to the simulation, in order for the MOSFET to turn "on" or "off" fast enough, it will draw about 160 mA. That amount of current is fairly small but a comparator will be providing the current to charge the gate of the MOSFET, and the comparator the team will be using can only source and sink about 20 mA. So, unless the simulation is wrong or the data sheet for the comparator is underestimating the output current capabilities, there could be a problem with the generated triangle wave.

8.3.1 High Frequency Phenomena

Most commercially produced step-up converters operate at frequencies half or a quarter of what this project would need to operate at in order to shrink the passive values significantly.

However, the idea of shrinking passive values stems from miniaturizing the circuit board and in effect, minimizing the high frequency effects typically seen on regular PCBs.

High frequency signals affect the quality of the signal from start to finish significantly. There are several factors to consider when designing and laying out a PCB used for high frequency signals. "At high frequencies, board layout is governed more by electromagnetic interactions, and less by electronic circuit theory." [5] These parasitics and reflections can interfere with the accuracy and stability of the control loop. For example, for every 1mm of trace, about 1nH of parasitic inductance is added in series on the trace. Trace density or improper ground planes increase the parasitic capacitance in the circuit. Every 1mm of trace adds about 1pF of parasitic capacitance in the circuit. All of these parasitics will affect the stability of the closed loop system and it may cause ringing in the output voltage signal. In power applications such as this, MOSFET arrangement, corners and board density also have a significant effect on the signals in the circuit.

8.3.2 Part Restrictions

Operating this boost converter at 20 MHz is no insignificant task. There are a number of important factors to consider in designing this circuit and selecting parts for this application. Capacitors have a few prominent roles in the step-up converter, and as such, it is important to look at a few things in their datasheet to ensure they fit the needs of our circuit. As has been stated, efficiency is a high priority for this project. Minimizing the capacitors equivalent series resistance or ESR will be important for maximizing efficiency. Most capacitors can only hold so much potential before breakdown occurs, so the voltage rating will be important for this project. Lastly, it is critical to look at the capacitance in relation to frequency. Capacitors characteristic capacitance changes as a function of frequency and it will be important to make sure they

maintain proper capacitance at the operating frequency so as to not have the circuit fall into DCM.

That said, the most important factor associated with making this circuit operate at 20 MHz is in the drive circuitry for the gate of the MOSFET. The propagation delay through the comparator and gate drive isn't critical, but the rise and fall time is a significant factor. The total rise time for a 20 MHz signal is 25ns. The total fall time is the same at 25ns. The comparator which creates the PWM and the gate driver which sources and sinks current to drive the FET need to have rise and fall times that allow for proper operation, otherwise 20 MHz may not be an achievable goal.

8.4 Efficiency

One of the main goals of this project is to maximize the efficiency of the boost converter circuit. Linear Technology has a piece of software that simulates circuits, and more specifically circuits that utilize their IC's. Their software is LTSpiceIV. It is very versatile and is a powerful tool for the project. Some key aspects of the program are that it has the ability to monitor current and voltage waveforms, replicate many intricacies and losses of devices, and calculate the dissipation and efficiency of a circuit.

The circuit schematic that J. Huang provided us with had all of the components of a functional DC/DC Boost Converter in place. The schematic utilizes an LT1310 DC/DC boost converter which contains inside a chip voltage mode controller loop. Using LTSpiceIV, the team executed the simulation and the software provided them with the efficiency report shown in Table 3. The efficiency was 81.9%, and the team identified three components that dissipated the most power and that can be substituted. After finding better components that had fewer losses, the team ended up with a maximum efficiency of 88.3% as shown in Table 4. If V_{IN} was

increased to 5V, the efficiency would jump to a maximum efficiency of 90.7% as shown in Table 5 below.

--- Efficiency Report ---			
Efficiency: 81.9%			
Input: 2.49W @ 3.3V			
Output: 2.04W @ 12.1V			
Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	461mA	2859mA	1mW
C3	0mA	0mA	0mW
C4	1mA	1mA	0mW
C6	34mA	1256mA	0mW
C7	0mA	0mA	0mW
D1	505mA	3286mA	82mW
L1	1040mA	2107mA	74mW
R1	0mA	0mA	664µW
R2	0mA	0mA	76µW
R3	0mA	0mA	0µW
R4	0mA	0mA	359µW
U1	947mA	5269mA	295mW

Table 3: Efficiency Optimization #1

--- Efficiency Report ---			
Efficiency: 88.3%			
Input: 2.31W @ 3.3V			
Output: 2.04W @ 12.1V			
Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	295mA	1252mA	0mW
C3	0mA	0mA	0mW
C4	1mA	1mA	0mW
C6	15mA	337mA	0mW
C7	0mA	0mA	0mW
D1	345mA	1220mA	50mW
L1	684mA	864mA	5mW
R1	0mA	0mA	664µW
R2	0mA	0mA	76µW
R3	0mA	0mA	0µW
R4	0mA	0mA	359µW
U1	618mA	1793mA	214mW

Table 4: Efficiency Optimization #2

--- Efficiency Report ---			
Efficiency: 90.7%			
Input: 2.25W @ 5V			
Output: 2.04W @ 12.1V			
Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	225mA	1161mA	0mW
C3	0mA	0mA	0mW
C4	1mA	1mA	0mW
C6	12mA	283mA	0mW
C7	0mA	0mA	0mW
D1	285mA	1101mA	47mW
L1	451mA	665mA	2mW
R1	0mA	0mA	664µW
R2	0mA	0mA	76µW
R3	0mA	0mA	0µW
R4	0mA	0mA	359µW
U1	370mA	1355mA	160mW

Table 5: Efficiency Optimization #3

The team identified the parts as the most dissipative are C2, D1, and L1. The actual inductor, L1, on the LT526A Demo Board, mentioned in the next section, is a Toko A915AY-6R8M, and the capacitor, C2, has an 0603 footprint. The team replaced each of those parts individually and let the simulation run again. This determined the new efficiency and power dissipation reduction with each replaced part. Table 6 below shows the original parts used in the schematic and the different components that were used to increase efficiency.

Parts Exchange Comparison		
Ref	Old	New
D1	SS24 Schottky I_{AVE}: 2A; V_{BRKDN}: 40V	DFLS220L Schottky I_{AVE}: 2A; V_{BRKDN}: 20V
L1	6.8µF R_{RES}: 0.068Ω	6.8µF R_{RES}: 0.0116Ω
C2	3.3µC; 16V; 0.050Ω	5.6µC; 16V; 0.003Ω

Table 6: Part Changes in Efficiency Optimization Simulations

The schematic used in the simulation is shown in the figure below. The diode has been replaced, along with the inductor and capacitor. Each of those parts will have lower equivalent series resistances.

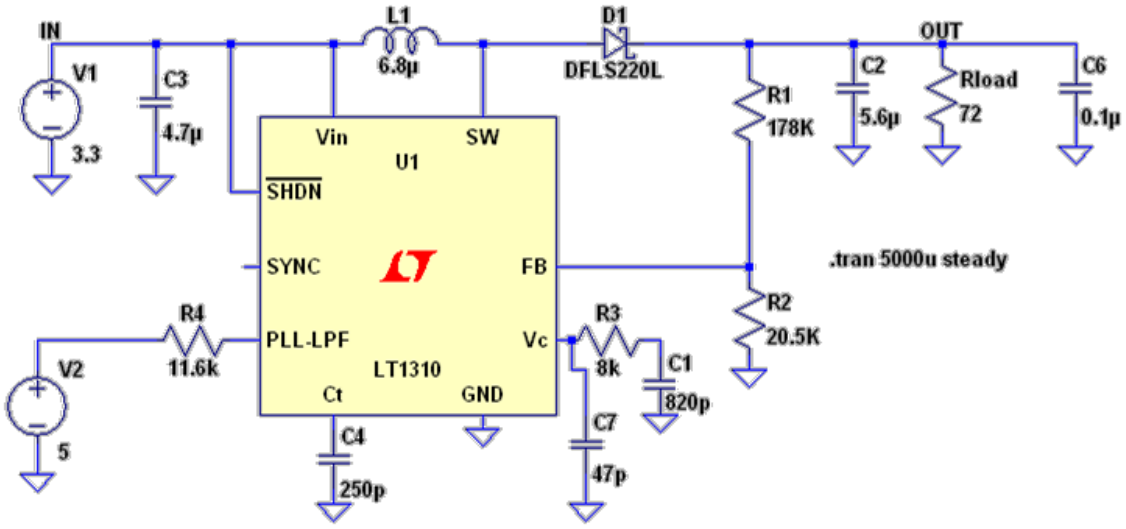

Figure 15: Optimized Efficiency Schematic Used in Simulation

The LT1310 is a boost converter made by Linear Technology. The IC is rated for 1.5A and it is known as a DC/DC Boost Converter. LT makes a demo board called the LT526A for testing the LT1310 in a real world application. There are several posts on the board to allow for easy access to certain test points. The board takes about 5V in and produces a steady 12V output. The switching frequency is adjustable from 1.2MHz to 2.4MHz via a dial on the board. The frequency can actually be adjusted up to 4.5MHz assuming some passive components were replaced. The general outline of the board is shown in the figure below. The figure below is on the Linear Technology website.

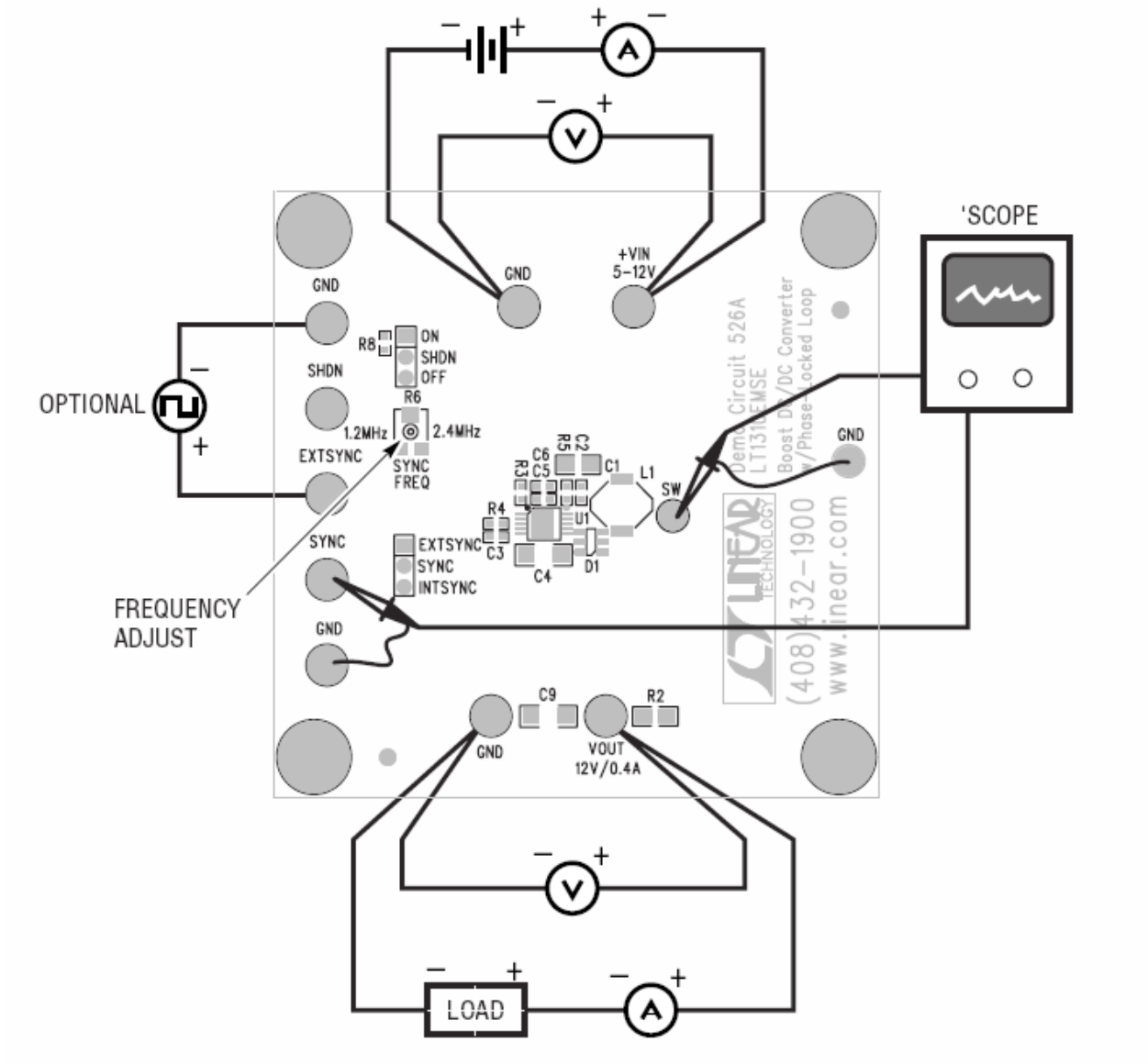

Figure 16: LT526A Demo Board

Draper provided this board for efficiency testing purposes. The idea was to test the overall efficiency of this device and compare it to the simulated efficiency of the same device, and draw comparisons on accuracy of measurements and real vs. simulated data.

For the projects' purposes, the team drove the board with an input voltage of 3.3V with a load resistance of 91Ω. The load resistance is 91Ω because of the amount of power that is

dissipated by the resistor at the output. This resistor was readily available and could handle up to 2W of power.

The LT526A Demo Board was modeled in the simulation software. The schematic is shown in Figure 17.

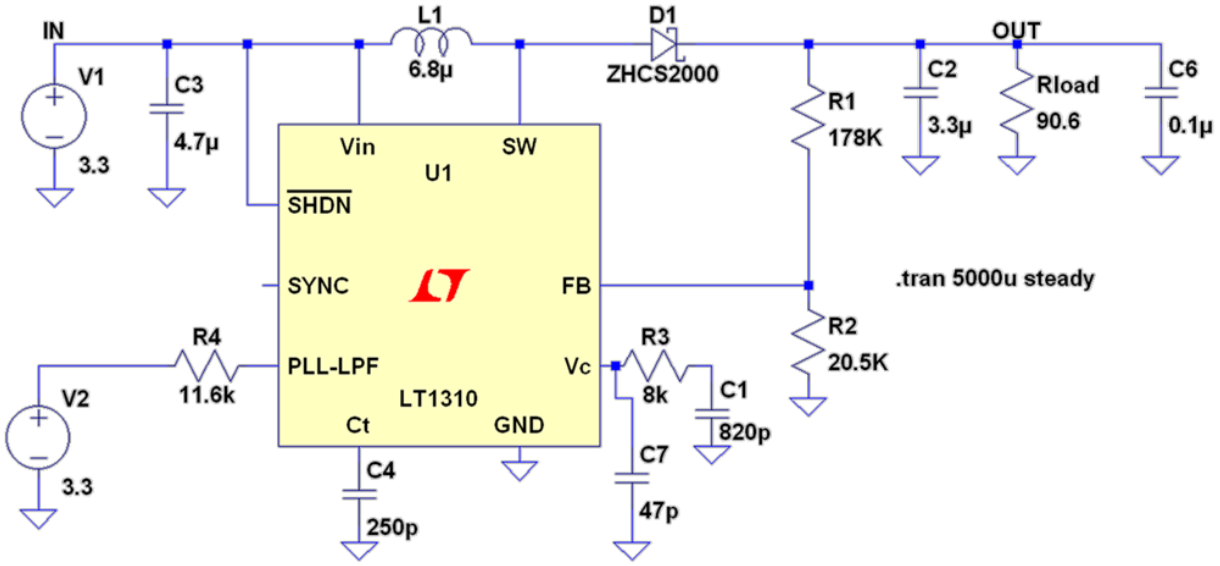

Figure 17: LT526A Demo Board Schematic

The diode seen in the schematic above was entered as a spice directive because the program did not have the model for the ZHCS2000 Schottky diode which is the actual part on the LT526 Demo Board. The method of entering a new spice model into LTSpiceIV is simple. First, one must find the directory which contains the spice directives of the existing models. Typically, the directory is located at C:\Program Files\LTC\LTSpiceIV\lib\cmp. The next objective is to locate the text file which contains the type of part you would like to add. For our purpose, the team chose the diode text file. Next, you copy an existing model into a new line and change the model name. The spice directive entered for the ZHCS2000 diode is ".model ZHCS2000 D(Is=.5u Rs=0.088 N=.59 Nr=1.8 Cjo=370p bv=60 Isr=0.01m Ibv=.3m M=.5231 Eg=.58 Xti=2 Iave=2 mfg=DIODES type=Schottky)." Using other lines of text and the

manufacturer datasheet or readymade spice directive, the team adapted the data and entered it into its own spice model.

The efficiency of the simulated demo board is about 83.2% with an input voltage of 3.3V. The results of the simulation are shown in the table below.

--- Efficiency Report ---			
Efficiency: 83.2%			
Input: 1.95W @ 3.3V			
Output: 1.62W @ 12.1V			
Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	399mA	1902mA	1mW
C3	0mA	0mA	0mW
C4	1mA	1mA	0mW
C6	21mA	902mA	0mW
C7	0mA	0mA	0mW
D1	433mA	2094mA	47mW
L1	893mA	2107mA	54mW
R1	0mA	0mA	664µW
R2	0mA	0mA	76µW
R3	0mA	0mA	0µW
R4	0mA	0mA	110µW
U1	808mA	3645mA	226mW

Table 7: Efficiency Report of Simulation of LT526A

--- Efficiency Report ---			
Efficiency: 81.3%			
Input: 2.04W @ 3.3V			
Output: 1.66W @ 12.27V			
	V	R or I	Power
V_{IN}	3.22 V	.635 A	2.04 W
V_{OUT}	12.27 V	90.6 Ω	1.66 W

Table 8: Efficiency Report of Measurements of LT526A

Using a Tektronix MSO4054 Oscilloscope and an Agilent E3631A Power Supply, the team measured the voltage at the input, and the current that the board was drawing. The team also measured the output voltage and the load resistance. From these, the team calculated the power at the input and the power at the output. The calculated efficiency of the LT526A board was 81.3%. The mismatch between the simulation and reality results from measurement error are some inaccuracies in the simulated losses of the parts L1 and C2.

8.5 Test Measurement Methodology

There are two different types of tests that are conducted. The first test is to check the functionality of each individual part of the circuit. These parts are the: power state, triangle wave and the control loop. Once each part has passed its functionality, testing is conducted on the entire assembled circuit.

Once the functionality of the design has been confirmed, then the second test can be conducted. This testing is for the efficiency. The efficiency testing has three factors that need to be considered. These three factors are: switching frequency, input voltage and load resistance. The test is conducted on three different frequencies, 5MHz, 10MHz and 20MHz. For each frequency range, the design is tested with two different input voltages, 3.3V and 5V. Furthermore, for each frequency and input voltage, the efficiency of the design is tested in a wide range of loads from 50Ω to 100Ω.

9. Design

The overall design process of the project spanned about five weeks of the eight weeks total. There were a large number of simulations and calculations to perform before ordering parts or laying out the boards. The design process had to foresee almost all of the possible issues so that the team would have enough time to troubleshoot if the need arose. The specifications which the project needs to be designed for are shown in Table 1.

9.1 CCM Boost Converter

In this section the function of the main components of the boost converter power stage are discussed and the individual component values are determined to meet the project specifications. The analysis for the boost converter in section 8.2.1 shows that the conduction mode of the power stage is determined by the input voltage, output voltage, output current and the value of the inductor. The input voltage range, output voltage and load current are defined by the project specification, Table 1. These requirements are as follows: a minimum 3.3V input voltage, and a 12V output voltage with 167mA output current. The calculations for the output current are shown below, given the requirements for 12V output voltage and 2W output power.

$$P = V \times I$$

Equation 18: Power Equation

$$I_{OUT} = \frac{P_{OUT}}{V_{OUT}} = \frac{2\ W}{12V} = 0.1\overline{66}A$$

Equation 19: Needed Output Current to Supply 2W of Power to the Load

The load resistor is:

$$V = I \times R$$

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT}} = \frac{12V}{0.166A} = 72\Omega$$

Equation 20: Load Resistor Calculated by Ohm's Law

Since three out of four of mode determining parameters are given, the inductor value is the only design parameter to maintain continuous conduction mode. To solve for the minimum value of indictor, the $I_{O(crit)}$ as shown in Figure 7 must be defined as the minimum output current to maintain continuous conduction mode. The relationships derived in section 8.2.1 are used to solve for the minimum inductor value. After derivations are performed, using the inductor current, the minimum average inductor current can be obtained by: [11]

$$I_{(\min-\text{ave})} = \frac{\Delta I_L}{2}$$

$\Delta I_L(+)$ is the relationship for continuous conduction mode is used to substitute for ΔI_L:

$$\Delta I_L(+) = \frac{V_I - (V_{DS} + (I_L \times R_L)}{L} \times T_{ON}$$

Equation 21: Critical Inductor Current Relationship for CCM

$$I_{(\min-\text{ave})} = \frac{(V_I - (V_{DS} + (I_L \times R_L)) \times T_{ON}}{2L}$$

Equation 22: Minimum Average Inductor Current

Next, L_{MIN} is solved for algebraically.

$$L_{min} \geq \frac{(V_I - (V_{DS} + (I_L \times R_L)) \times T_{ON}}{2I_{Lmin}}$$

Equation 23: Derived Minimum Inductor Size Equation

Simplifying this expression yields Equation 24 below.

$$L_{min} \geq \frac{V_O \times T_S}{16 \times I_{O(crit)}}$$

Equation 24: Simplified Minimum Inductor Size Equation

T_S is the time of one complete switching cycle. The minimum inductor value should be great than 224nH to keep the circuit functioning in continuous conduction mode..

$$L_{min} \geq \frac{V_O \times T_S}{16 \times I_{O(crit)}} = \frac{12 \times (50n)}{16 \times 0.167} = 224nH$$

Equation 25: Minimum Inductor Size for 20 MHz Switching Frequency to Maintain CCM

The functionality of the output capacitance is to store energy and maintain a constant voltage. In a boost converter the output capacitance is selected to limit the output voltage ripple to meet the project specifications. The output voltage ripple is determined by the series impedance of the capacitor and the output current.

The following equation is used to determine the output capacitance for the power stage operating in CCM.

$$C \geq \frac{I_O \times D}{f_S \times \Delta V_O}$$

Equation 26: Minimum Output Capacitor Size Equation

The necessary capacitance value is determined as a function of the calculated output load current of 0.167A, switching frequency of 20MHz and an output voltage ripple of $10mV_{peak\ to\ peak}$ to meet the project goals. The duty cycle is calculated using the following equation. [6]

$$D = 1 - \frac{3.3V}{12V} = 0.725.$$

Equation 27: Duty Cycle Equation

Solving for the minimum output capacitor value:

$$C \geq \frac{(0.167A) \times (0.725)}{(20MHz) \times (5mV)} = 1.2\mu F$$

Equation 28: Minimum Output Capacitor Value

The output capacitor must be greater than 1.2µF in order for the desired output voltage ripple of 10mVpk-pk to be met. [11]

The power switch is used to control energy flow from the input to the output source. When the switch is on it must conduct current in the inductor. And when it is off, it must prevent

the output voltage from flowing. Furthermore, the switch must change from the on and off states rapidly in order to prevent a large amount of power dissipation.

The most common switch that is used is a metal oxide semiconductor field effect transmitter, a.k.a. MOSFET. There are two types of MOSFETs, p-channel and n-channel. N-channel MOSFETs are most commonly used for boost converters.

Switching loss occurs when the MOSFET changes states. During the switching time, typically micro or nanoseconds in duration, power can be lost. Even the short periods of power loss that occur are added together to form an average. This average can add up to be quite devastating on a circuit.

Another form of loss that occurs is conduction loss. Conduction loss occurs as the current is fed through resistors. Conduction loss affects the inductor, diode, and MOSFET the most. The inductor is heavily affected by it as it is comprised of wires, which, in and of itself, has a resistance.

When the power switch is off, the output diode will conduct. When the output diode is conducting, it is creating a path for the inductor current to flow. The breakdown voltage that the diode must have should be greater than the max output voltage. The losses in the diode can be attributed to the conducting state.

9.1.1 Rationale for Part Selection

The input and output capacitors were selected based on their tolerance, ESR, current rating factor and capacitance for different operating frequencies. The N-channel MOSFET was selected based on gate charge and on resistance. This MOSFET has a lower on resistance than the gate charge to minimize the switching loss. The inductor was selected based on current saturation, ripple current and DC resistance and switching frequency. The diode was selected

based on the breakdown voltage and average current. The output resistance was selected based on the power dissipation rating and tolerance. The parts that were selected for the power stage are shown in the table below.

Parts List for Power Stage							
Daughter							
Ref Name	Name	DigiKey Part Number	DigiKey Description	Package	Unit Price	Quantity	Total Price
Cin	1µ	399-5775-1-ND	CAP CER 1UF 50V X8L 1210	1210	$1.30	25	$32.38
Cout	1.8µ	399-4933-1-ND	CAP CERM 1.8UF 16V X7R 0805	805	$0.80	10	$ 8.04
Rload	75Ω	PWR5322W75R0JECT-ND	RES 75 OHM 5% 3W WW 5322 SMD	5322	$0.89	10	$ 8.88
D1	DFLS220L	DFLS220LDICT-ND	DIODE SCHOTTKY 2A 20V PWRDI 123	123	$0.68	10	$ 6.84
M1	IRF8910	IRF8910PBFCT-ND	HEX/MOS N-CH DUAL 20V 10A 8SOIC	8 Pin	$0.97	10	$ 9.72
L1	400n	513-1639-1-ND	INDUCTOR LO PROFLE 400NH 42A SMD	FlatPAK	$2.01	10	$20.09
						Total	$85.95

Table 9: Parts List for Power Stage

9.2 Triangle Wave

The first major part of implementing a successful compensation loop was creating a triangle wave that had a $V_{pk\text{-}pk}$ of about 2V or more and a frequency up to 20 MHz. The original design used a current mirror consisted of two 2N3906 BJTs that supplied current to charge a capacitor. Once the capacitor reached a voltage above the comparison level, the comparator drove to a logic high and turned the MOSFET "on." With the MOSFET in the "on" state, current from the capacitor discharged through the on resistance of the MOSFET. After the capacitor discharged to a voltage below the comparison level, the MOSFET would turn "off" and allow the capacitor to charge up again and let the whole cycle continue. The schematic of this circuit is shown in Figure 18.

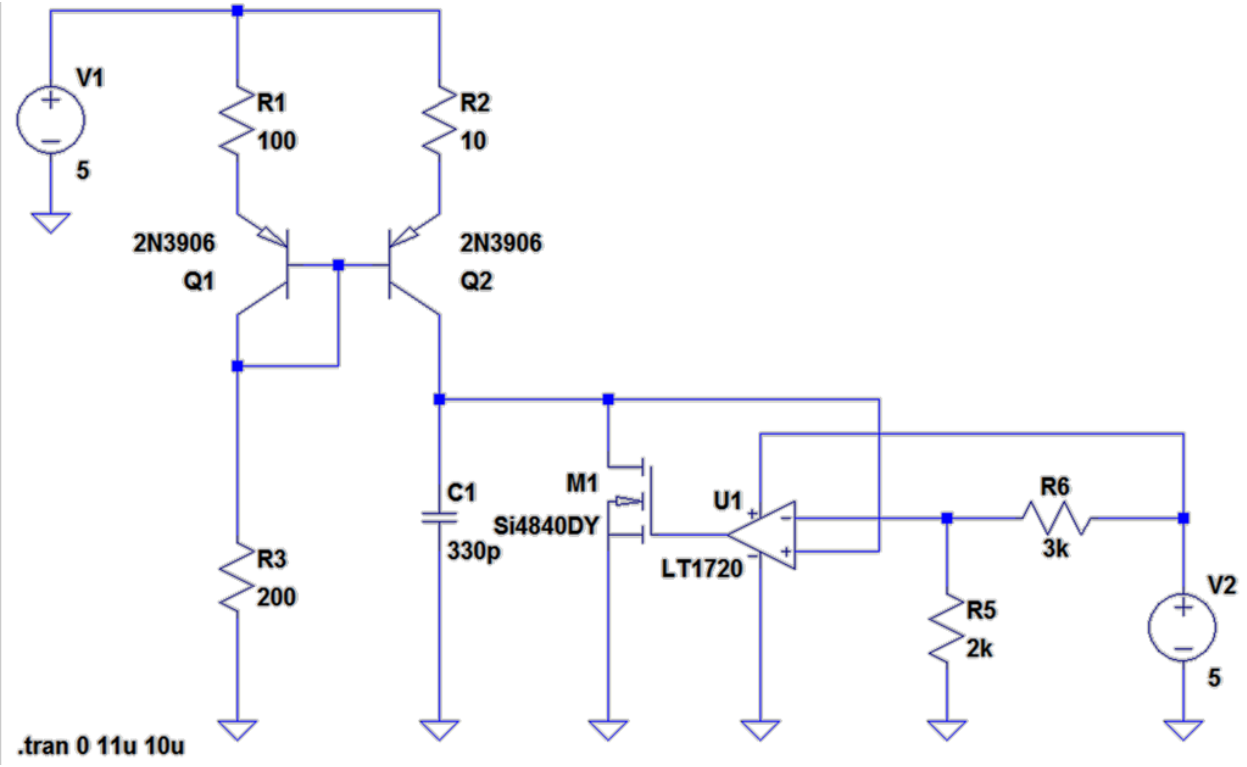

Figure 18: First Iteration of Triangle Wave Generator

This triangle wave generator worked very well in simulation. The design only required three component changes in order to change the operating frequency. The MOSFET, capacitor and R3 resistor needed to change to ensure proper operation at three distinct frequencies, 5, 10 and 20 MHz. Changing R3 changed the output current at the collector of Q2. The capacitor size changed so that the capacitor would charge and discharge more quickly or slowly depending on the frequency. The MOSFET changed because of the on resistance; the different on resistances allowed for a faster or slower discharge of the capacitor. Unfortunately, the triangle wave generator did not work as well in reality as it did in simulation. The circuit was constructed as seen with and without a gate driver, and only the 10 MHz board functioned properly. The 5, 10 and 20 MHz generator board results are shown in the screenshots below.

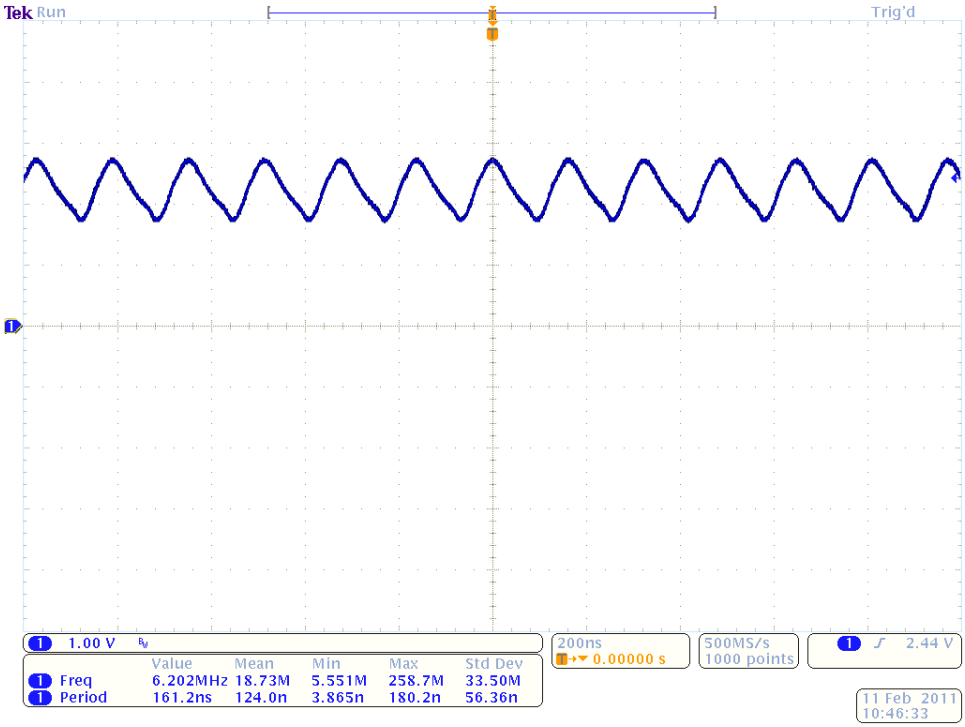

Figure 19: 5MHz Design without Gate Driver

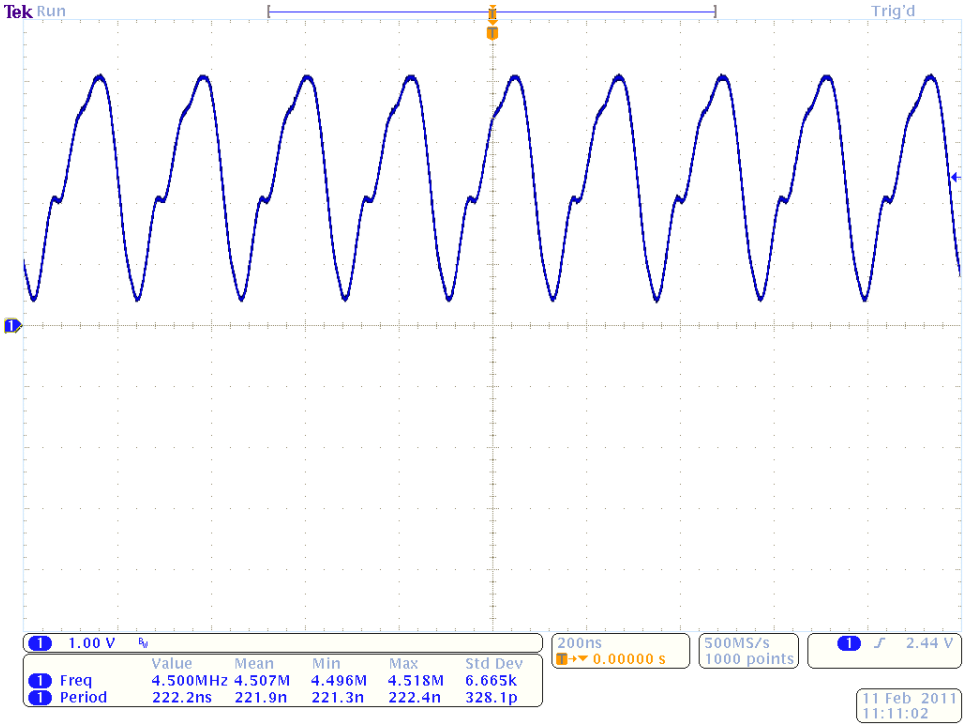

Figure 20: 5MHz Design with Gate Driver

As seen in the figures above, both circuits worked at 5 MHz, but the gate drive IC enabled the circuit to operate at a higher $V_{pk\text{-}pk}$, but added some problems in the rising slope.

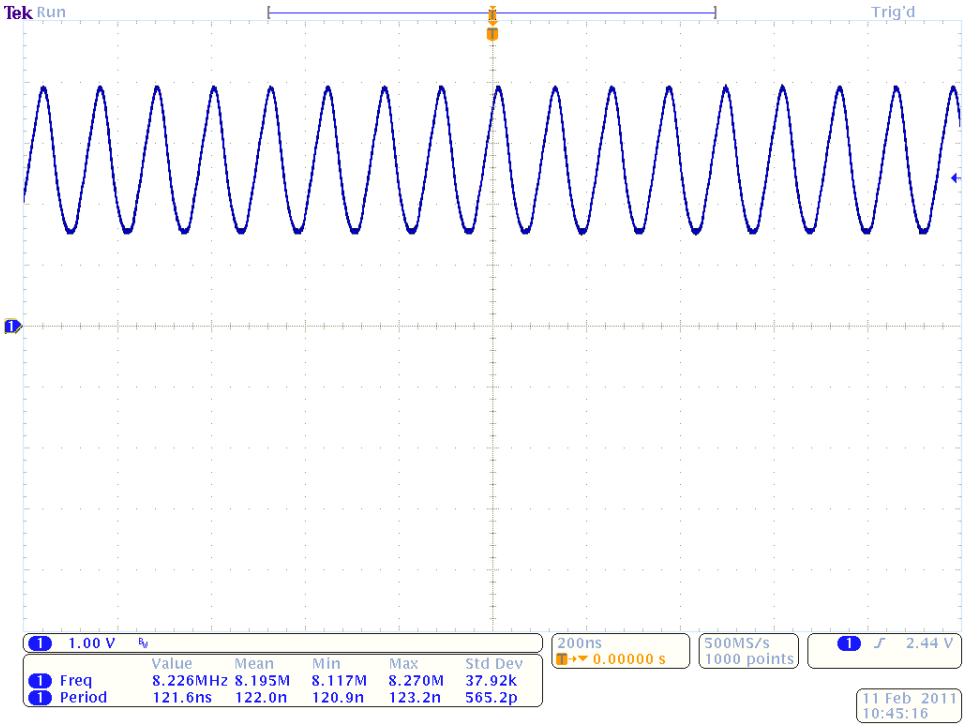

Figure 21: 10MHz Design without Gate Driver

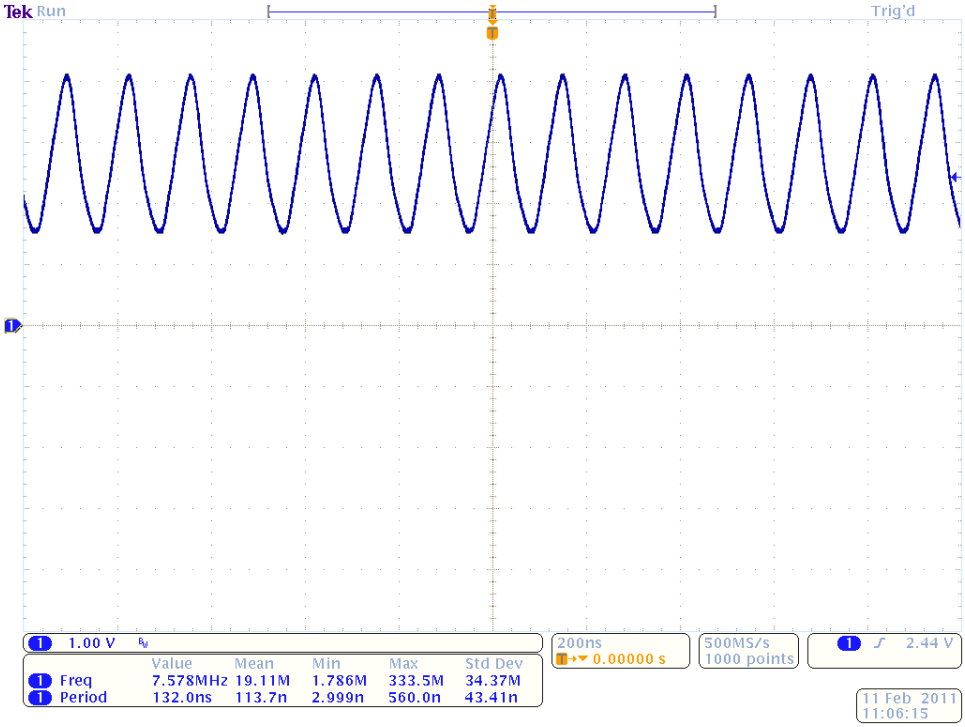

Figure 22: 10MHz Design with Gate Driver

As seen in the figures above, both circuits worked at 10 MHz, but the gate drive IC actually made the frequency of the triangle wave decrease a small amount.

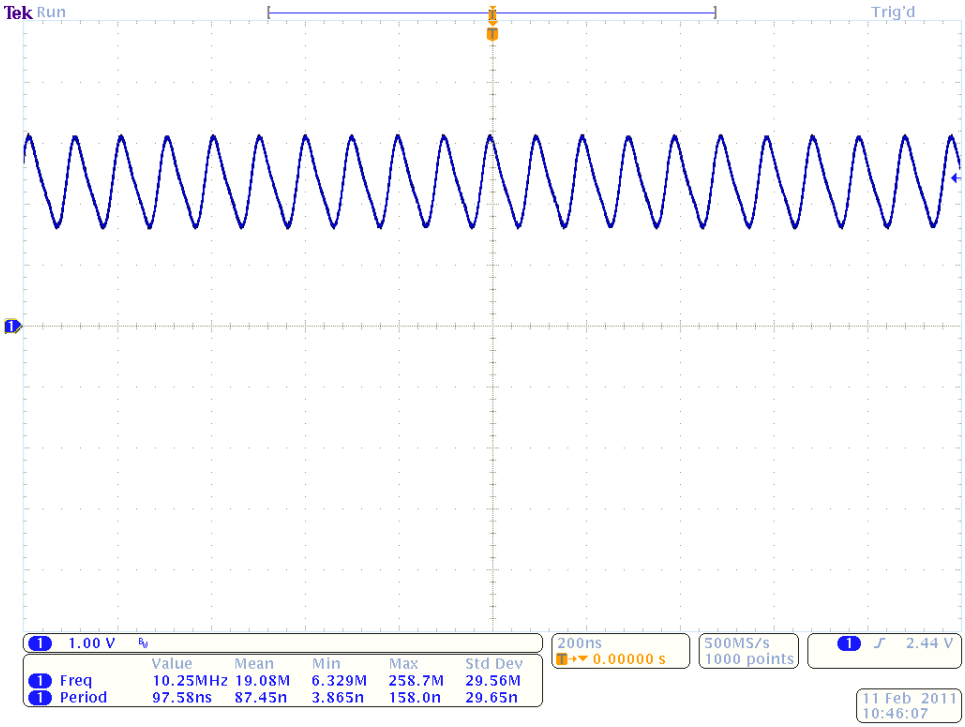

Figure 23: 20MHz Design without Gate Driver

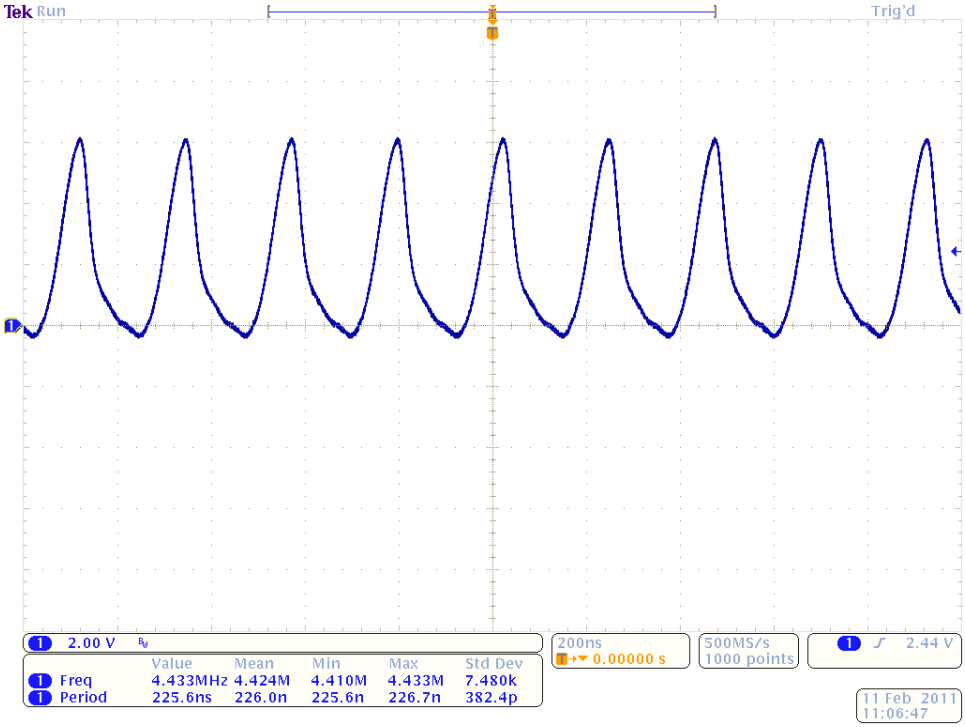

Figure 24: 20MHz Design with Gate Driver

As seen in the figures above, both circuits failed to operate at 20 MHz, because the on resistance couldn't discharge the capacitor fast enough and the gate driver added rise time.

After going through a few redesigns of the PCB to reduce the trace lengths, the only board that functioned correctly was still the 10 MHz triangle board. It then became necessary to design a new circuit that could create a triangle wave at three discrete values, 5, 10 and 20 MHz with a V_{pk-pk} of about 2V. The schematic of the new design is shown below in Figure 25.

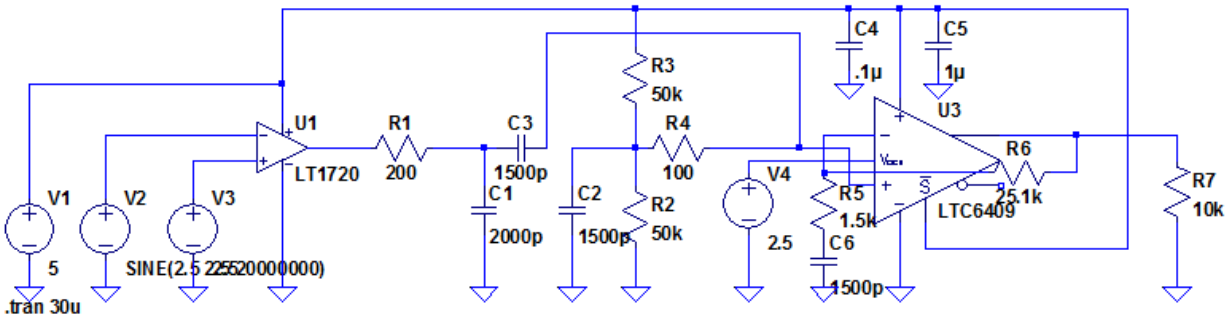

Figure 25: Final Triangle Wave Generator Schematic

This circuit utilizes a precision voltage IC that is compared to a sine wave from a function generator. The comparator creates a square wave. This square wave is then fed into a passive integrator. The output of the integrator is a triangle wave of the frequency equal to the input sine wave from the function generator. The small triangle wave is about 20 mV_{pk-pk} and thus must be amplified to a $2V_{pk-pk}$. Using a single supply op-amp with a slew rate of 3300V/µs, the output of the integrator was amplified to create a working triangle wave up to 20 MHz. The only part that needed to be change to change frequency was the capacitor in the integrator, C1. Higher frequencies required smaller capacitors, and lower frequencies required larger capacitors.

9.2.1 Rationale for Part Selection

Careful consideration went into every selected component for not only the first, but also the second iteration of the triangle wave generator boards. The resistors were selected based on tolerance and their power dissipation ability. The capacitors were selected based on their tolerance, ESR, voltage rating, and capacitance over a range of frequencies. The MOSFETs were selected based on their gate charge and their on resistances. The LT1720 was selected due

to its fast rise and fall time and its voltage requirements. The op-amp was selected based on its voltage supplies, output current, and slew rate. The following tables list the parts used in both designs of the triangle wave generator board. The first is to old iteration and the second is the final iteration.

Parts List for 20M, 10M, 5M Triangle (6 Boards)							
20M Triangle							
Ref Name	Name	DigiKey Part Number	DigiKey Description	Package	Unit Price	Quantity	Total Price
R1	100	P100FCT-ND	RES 100 OHM 1/4W 1% 1206 SMD	1206	$0.10	20	$ 2.00
R2	10	RNCP1206FTD10R0CT-ND	RES 10 OHM 1/2W 1% 1206 SMD	1206	$0.07	20	$ 1.30
R3	200	P200FCT-ND	RES 200 OHM 1/4W 1% 1206 SMD	1206	$0.10	12	$ 1.20
R4	2k	P2.00KFCT-ND	RES 2.00K OHM 1/4W 1% 1206 SMD	1206	$0.10	20	$ 2.00
R5	3k	P3.00KFCT-ND	RES 3.00K OHM 1/4W 1% 1206 SMD	1206	$0.10	20	$ 2.00
C1	330p	478-6045-1-ND	CAP CER 330PF 50V NP0 0805	0805	$0.77	20	$ 15.40
M1	Si4840DY	SI4840DY-T1-E3CT-ND	MOUSER	8 Pin	$3.11	8	$ 24.88
U1	LT1720	LT1720IS8#PBF-ND	IC COMP R-RINOUT DUAL 8-SOIC	8 Pin	$7.00	10	$ 70.00
Q1,Q2	2N3906	2N3906-APCT-ND	TRANSISTOR PNP GP 40V TO92	TO-92	$0.28	24	$ 6.62
U2	ZXGD3002E6	ZXGD3002E6CT-ND	IC GATE DRVR IGBT/MOSFET SOT23-6	6 Pin	$0.76	12	$ 9.17
R6, R7	0	541-0.0SBCT-ND	RES 0.0 OHM .25W 0603 SMD	0603	$0.19	30	$ 5.64
10M Triangle							
C1	1500p	445-1295-1-ND	CAP CER 1500PF 50V C0G 5% 0603	0603	$0.11	20	$ 2.20
M1	SiR426DP	SIR426DP-T1-GE3CT-ND	MOSFET N-CH 40V 15.9A 8-SOIC	PPAK	$1.05	8	$ 8.40
5M Triangle							
R3	226	P226FCT-ND	RES 226 OHM 1/4W 1% 1206 SMD	1206	$0.10	20	$ 2.00
C1	3900p	445-2683-1-ND	CAP CER 3900PF 50V C0G 5% 0805	0805	$0.33	20	$ 6.60
M1	STD95N04	497-5106-1-ND	MOSFET N-CH 40V 80A DPAK	DPAK	$2.57	8	$ 20.56
						Total	$179.97

Table 10: Parts List for Original Triangle Wave Boards

Parts List for Triangle Wave Generation							
Other Triangle							
Ref Name	Name	DigiKey Part Number	DigiKey Description	Package	Unit Price	Quantity	Total Price
U1	LT1720	LT1720IS8#PBF-ND	IC COMP R-RINOUT DUAL 8-SOIC	8SOIC	$ 7.00	6	$ 42.00
U1	LT1715	LT1715CMS#PBF-ND	IC COMPARATOR 150MHZ DUAL 10MSOP	10 Pin	$ 6.88	6	$ 41.28
U2	LTC6409	LTC6409CUDB#TRMPBFCT-ND	IC AMP/DRIVER DIFF 10-QFN	11 Pin	$10.84	4	$ 43.36
U3,U4	ADR121	ADR121AUJZ-REEL7CT-ND	IC V-REF PREC 2.5V TSOT-23-6	TSOT23-6	$ 2.00	14	$ 28.00
R1	200	P200FCT-ND	RES 200 OHM 1/4W 1% 1206 SMD	1206	$ 0.10	10	$ 1.00
C1	2n	478-6042-1-ND	CAP CER 2000PF 100V X7R 0805	0805	$ 0.23	10	$ 2.31
C1	3.9n	478-5157-1-ND	CAP CER 3900PF 100V X7R 0805	0805	$ 0.17	10	$ 1.65
C1	7.5n	490-1639-1-ND	CAP CER 7500PF 50V 5% C0G 0805	0805	$ 0.31	10	$ 3.09
C2,C3,C6	1500p	445-2321-1-ND	CAP CER 1500PF 100V C0G 5% 0805	0805	$ 0.12	10	$ 1.21
C4	.1µ	445-1349-1-ND	CAP CER .10UF 50V X7R 10% 0805	0805	$ 0.07	20	$ 1.32
C5	1µ	311-1365-1-ND	CAP CERAMIC 1UF 16V X7R 0805	0805	$ 0.07	20	$ 1.38
R2,R3	50K	PNM0805-50KBCT-ND	RES 50K OHM .2W 0.1% 0805 SMD	0805	$ 1.40	10	$ 14.00
R4	100	P100FCT-ND	RES 100 OHM 1/4W 1% 1206 SMD	1206	$ 0.10	10	$ 1.00
R5	1.5K	RNCP0805FTD1K50CT-ND	RES 1.5K OHM 1/4W 1% 0805 SMD	0805	$ 0.05	10	$ 0.46
R6	25K	PNM0805-25KBCT-ND	RES 25K OHM .2W 0.1% 0805 SMD	0805	$ 1.40	10	$ 14.00
R7	10K	P10.0KFCT-ND	RES 10.0K OHM 1/4W 1% 1206 SMD	1206	$ 0.10	10	$ 1.00
						Total	$197.06

Table 11: Parts List for Final Triangle Wave Boards

9.3 Type III Compensation Network

The team is designing a boost converter operating in CCM that needs to compile the following requirements: V_{IN}=3.3V, V_{OUT}=12V, P_{OUT}=2W, f_{SW}=20MHz, V_{RIPPLE}=20mV_{pk-pk}. Using the CCM design process, the team selected the input inductor. The output capacitor was selected based on the desired output V_{RIPPLE}. The standard values for the inductor (L) and the output capacitor (C_{OUT}) are 400nH and 1.8µF respectively.

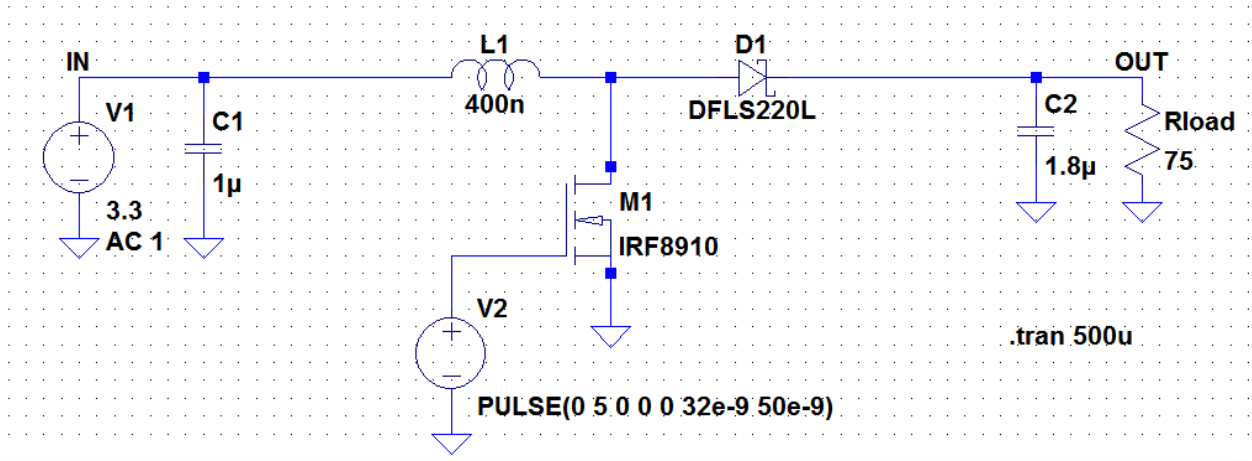

Figure 26: Our Open Loop Boost Converter Schematic

The most important factors to a voltage controlled gain of a CCM boost converter are the input inductor L, output capacitor C_{OUT}, duty cycle D and the load resistance R_{LOAD}. Duty cycle is 0.72 and the R_{LOAD} is 75Ω for this boost converter. These four terms determine the frequencies of the double pole (f_{LC}) and the right half plane zero (f_{RHP}). The f_{RC} and the f_{RHP} are calculated using the formulas below. [6]

$$f_{LC} = \frac{1-D}{2\pi\sqrt{L * C_{OUT}}} = \frac{1-0.72}{2\pi\sqrt{400e^{-9} * 1.8e^{-6}}} = 52\,518Hz$$

Equation 29: LC Double Pole Frequency

$$f_{RHP} = \frac{R_{LOAD}(1-D)^2}{2\pi L} = \frac{75(1-0.72)^2}{2\pi(400e^{-9})} = 2\,339\,577Hz$$

Equation 30: Right Half Plane Zero Frequency

The double pole frequency is about 52 kHz and the right half plane zero is at about 2.3MHz.

The RHP zero makes the boost converter unstable, therefore to balance this effect the crossover frequency f_C has to be at least one third less than f_{RHC}. The team does not want f_C to be close to the load dependent peaking associated with the double pole at f_{LC}. For that reason f_C has to be places at a frequency at least three times higher than f_{LC}. As a result for compensating the loop, the team had to satisfy two requirements: [2]

$$f_C = 3 * f_{LC} f_C = {}^{1}/_{3}\, f_{RHP}$$

Equation 31: Crossover Frequency Equation of Our Circuit

Solving the two equations above, $f_{LC} \leq 0.1 * f_{RHP}$. The boost converter satisfies this requirement since f_{LC} is much less then 230 kHz ($0.1*f_{RHP}$). Next the team attempted to satisfy the second requirement:

$$f_C = 0.33 * 2.3e^6 = 759KHz$$

Equation 32: Crossover Frequency of Our Circuit

After simulating the boost converter in MATLAB, the magnitude and phase plots are shown below.

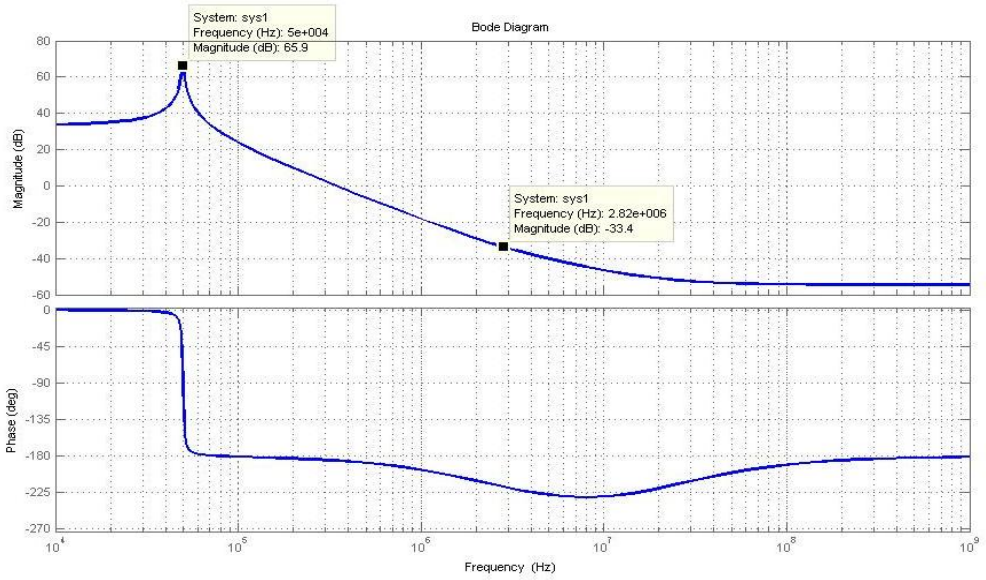

Figure 27: The Boost Converter Gain, Showing f_{RC} and f_{RHP}

Next the team solved the equations for the generic type III network; the equations are shown in the figure below. Type III network has two zeros and two poles. The zeros should be placed at 70% of f_{LC} to counter the sharp decrease in phase after the high peak at f_{LC}. The two poles should be places at the f_{RHC}. [10]

The type III compensation network configuration and the equations to solve for the poles and zeros are shown in Figure 28.

Letting R_1=37.4kΩ, the corresponding values for the other passives are R_2=37.4kΩ, R_3=1.15kΩ, C_1=4pF, C_2=62pF and C_3=62pF. These values were selected after many calculations for the best set of values that would optimize the unity gain and phase margin.

The transfer function formula of the network is:

$$Gain_{TYPE\ III} = \frac{1.35e9s^2 - 6.12e14s + 6.9e19}{s^3 + 3.5e7^2 + 3.08e14s}$$

Equation 33: Gain of the Type III Compensation Network

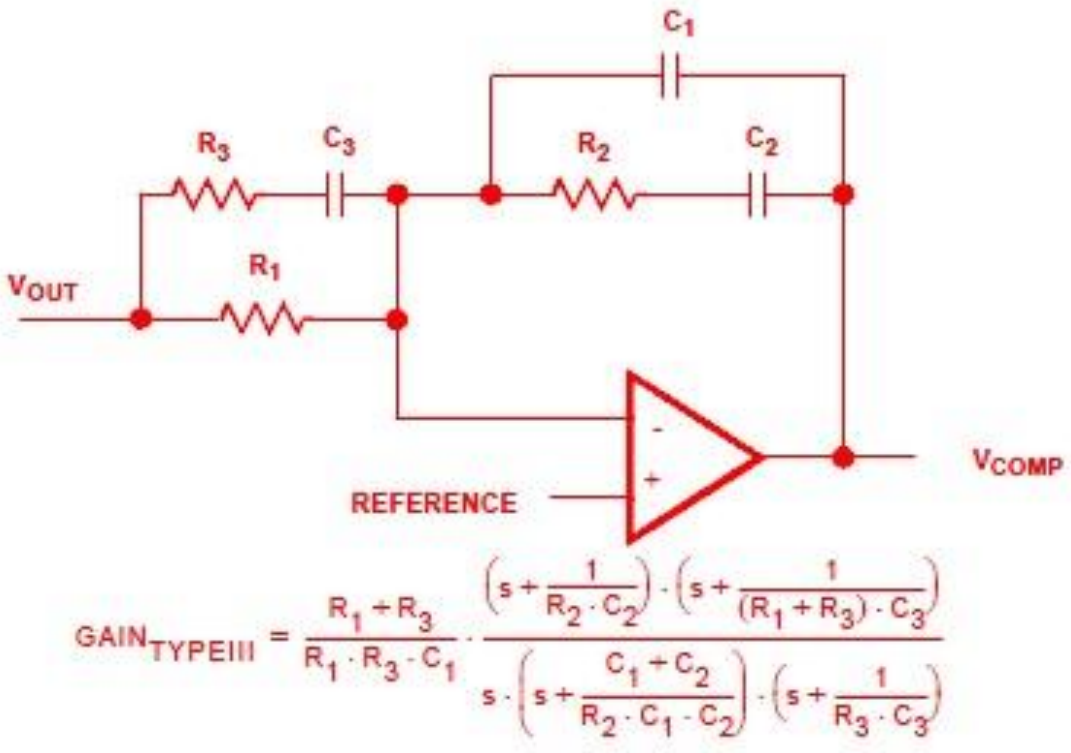

Figure 28: Transfer Function of Generic Type III Compensation Network [6]

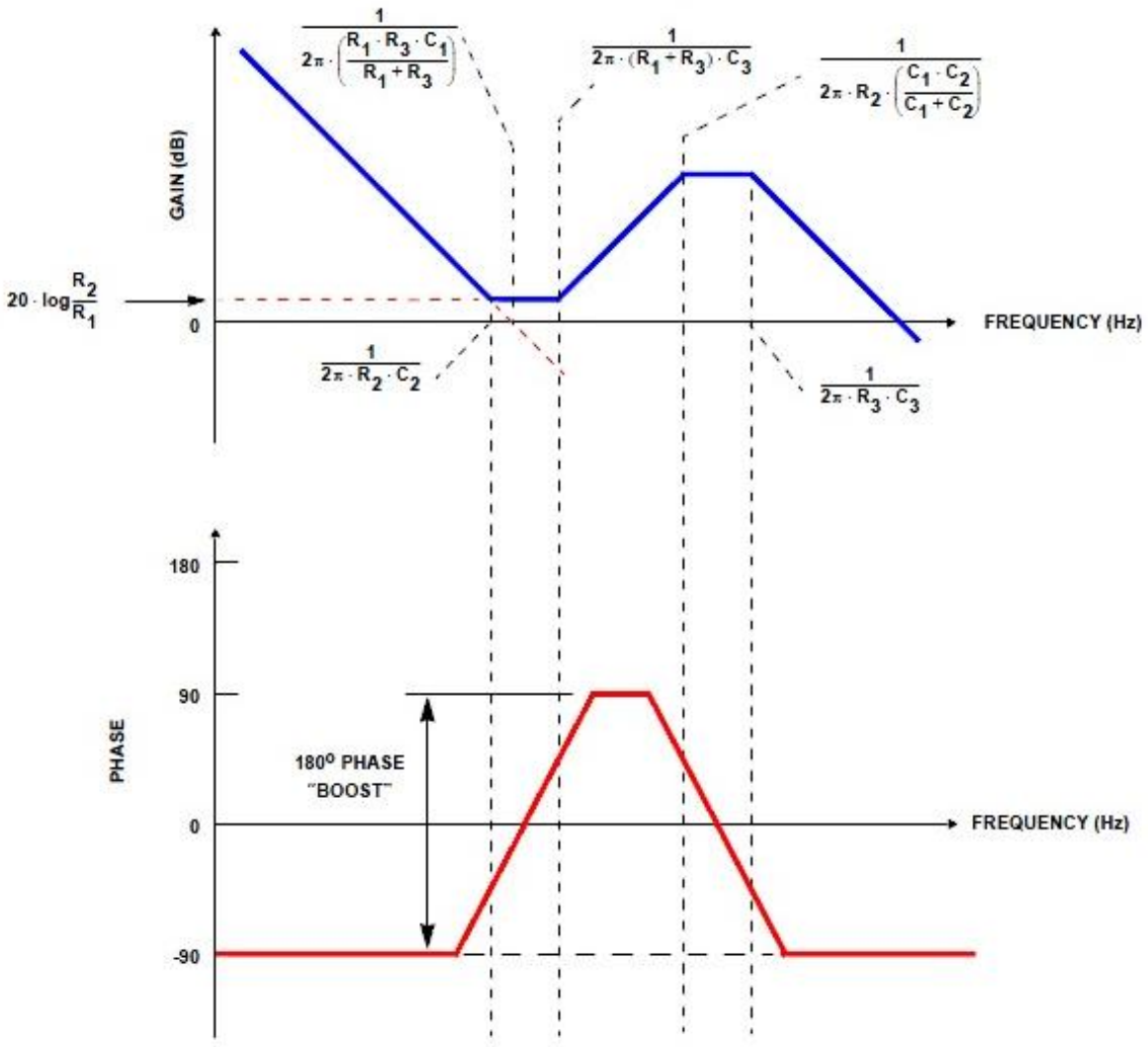

Figure 29: Bode Plot of Generic Type III Compensation Network [6]

After calculating the values of the passive components for our compensation network, the team plotted the bode diagram of the required type III compensation network for our circuit. This bode plot is shown below in Figure 30. [6]

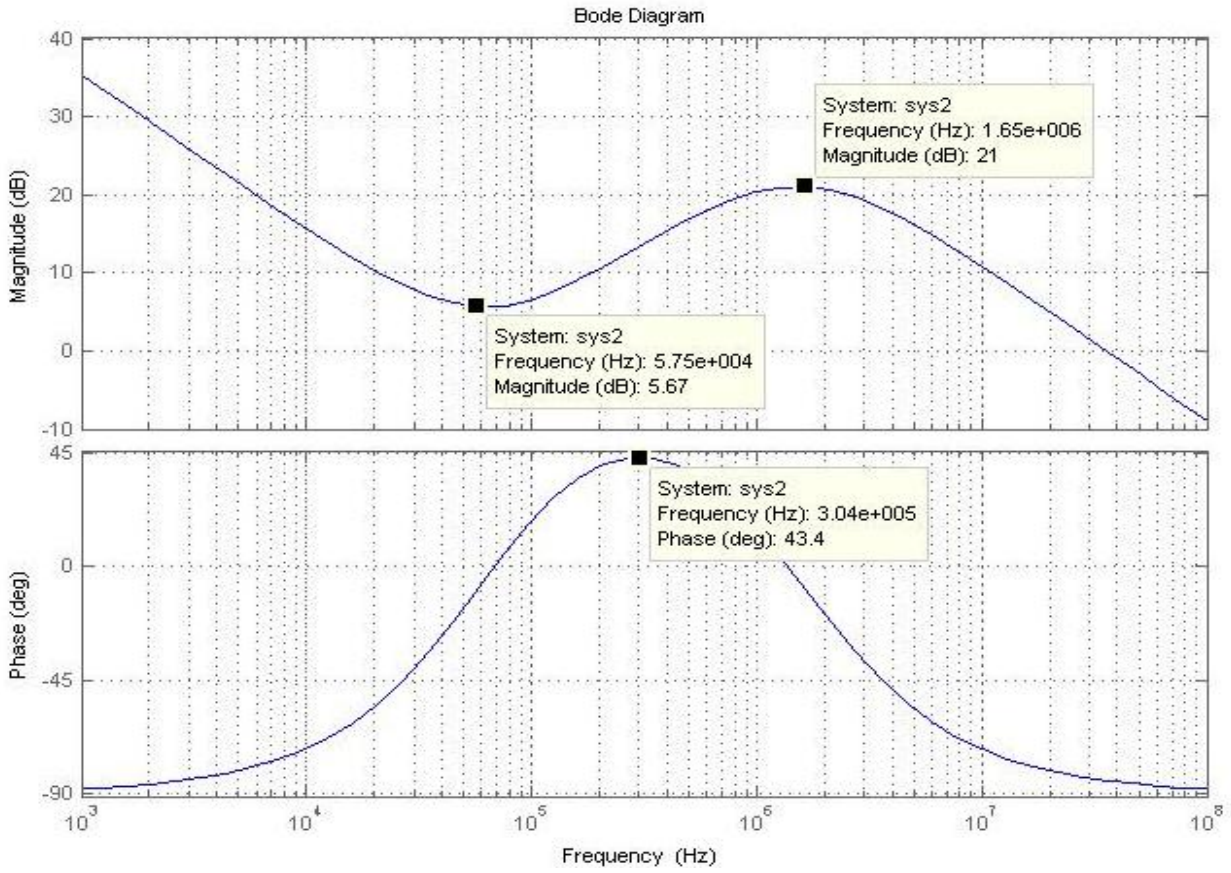

Figure 30: Bode Plot of Our Type III Compensation Network

Next, the two bode plots, the power stage and the type III compensator, are combined for the resultant voltage controlled boost converter. The three bode plots are shown below in Figure 31. The control loop improves the magnitude and phase of the boost converter. The crossover frequency shifted from 350 KHz to 1.17MHz, while the phase margin improved. The power stage was unstable with a phase margin of -6 degrees and the type III control loop boost the phase to make the system stable with a phase margin of 74 degrees.

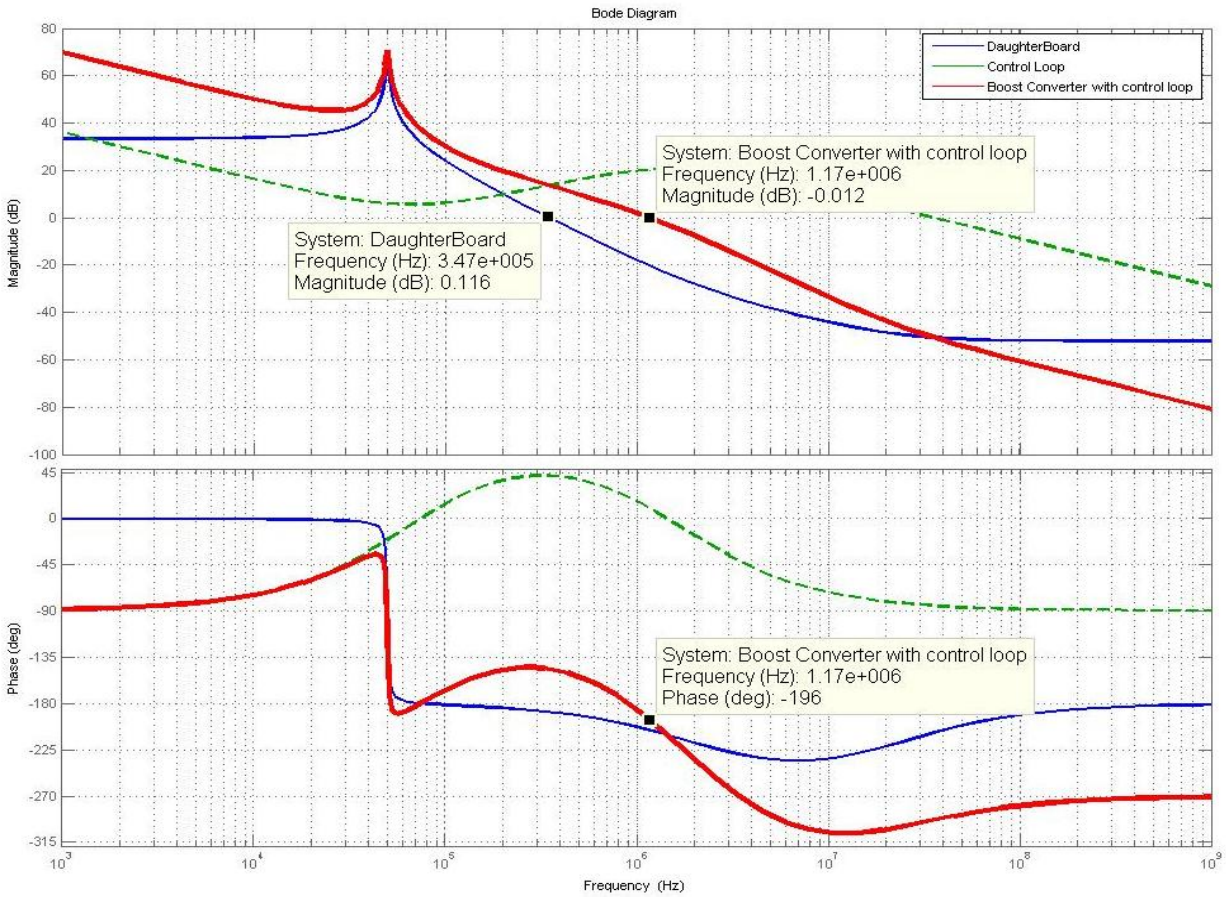

Figure 31: Bode Plot with Optimized Unity Gain and 74 Degrees of Phase Margin

9.3.1 Rationale for Part Selection

The resistors and capacitors were selected based on the same criteria as in Section 9.2.1 The OPA301 was selected based on its voltage supplies, output current, and slew rate and unity gain. The reference voltage was selected based on the precision of its output voltage. The parts used for the control loop are shown below.

Control							
Ref Name	Name	DigiKey Part Number	DigiKey Description	Package	Price Unit	Quantity	Total Price
C1	4p	311-1093-1-ND	CAP CERAMIC 4.0PF 50V NP0 0805	805	$ 0.06	20	$ 1.24
C2,C3	62p	478-6215-1-ND	CAP CER 62PF 100V NP0 0805	805	$ 0.23	30	$ 6.93
U1	OPA301	296-16905-1-ND	IC OPAMP VFB 150MHZ SGL SOT23-5	8 Pin	$ 3.15	6	$ 18.90
U2	ADR121	ADR121BUJZ-REEL7CT-ND	IC V-REF PREC 2.5V TSOT-23-6	TSOT23-6	$ 2.95	6	$ 17.70
R1,R2	37.4K	RMCF0805FT37K4CT-ND	RES 37.4K OHM 1/8W 1% 0805 SMD	805	$ 0.04	40	$ 1.60
R3	1.15K	RMCF0805FT1K15CT-ND	RES 1.15K OHM 1/8W 1% 0805 SMD	805	$ 0.04	20	$ 0.80
R4	1K	RMCF0805FT1K00CT-ND	RES 1K OHM 1/8W 1% 0805 SMD	805	$ 0.03	15	$ 0.44
R3	3.79K	PAT3.79KBCT-ND	RES 3.79K OHM 0.20W 0.1% 0803	803	$ 1.15	15	$ 17.25
C_{BP}	.1µ	445-1349-1-ND	CAP CER .10UF 50V X7R 10% 0805	805	$ 0.07	30	$ 1.98
						Total	$ 66.84

Table 12: Parts List for Compensation Network

9.4 PCB Layout

The PCBs were laid out in a program called FreePCB so the team could have access and control over the Gerber files. These Gerber files were then exported to an LPKF PCB rapid prototyping machine. The holes for the vias were drilled and then the holes were plated so there would be several unobstructed paths to the ground plane on the bottom layer. The boards were then milled out using a counter cutter and router.

9.4.1 Power Stage and Control Loop

The very last board that the team designed was the power stage and control loop board. The power stage components are located at the top of the layout as shown in the figure below. The control loop is comprised of the lower half of the layout as seen in the figure below. The trace widths in the power stage are 40mils to accommodate the large amount of current drawn. The distance in the ground return between the output capacitor and the MOSFET was minimized to reduce parasitic inductance and minimize output ringing in the circuit. There is also a jumper pin between the output of the power stage and the control loop so the boost converter could be tested in both open and closed loop configurations.

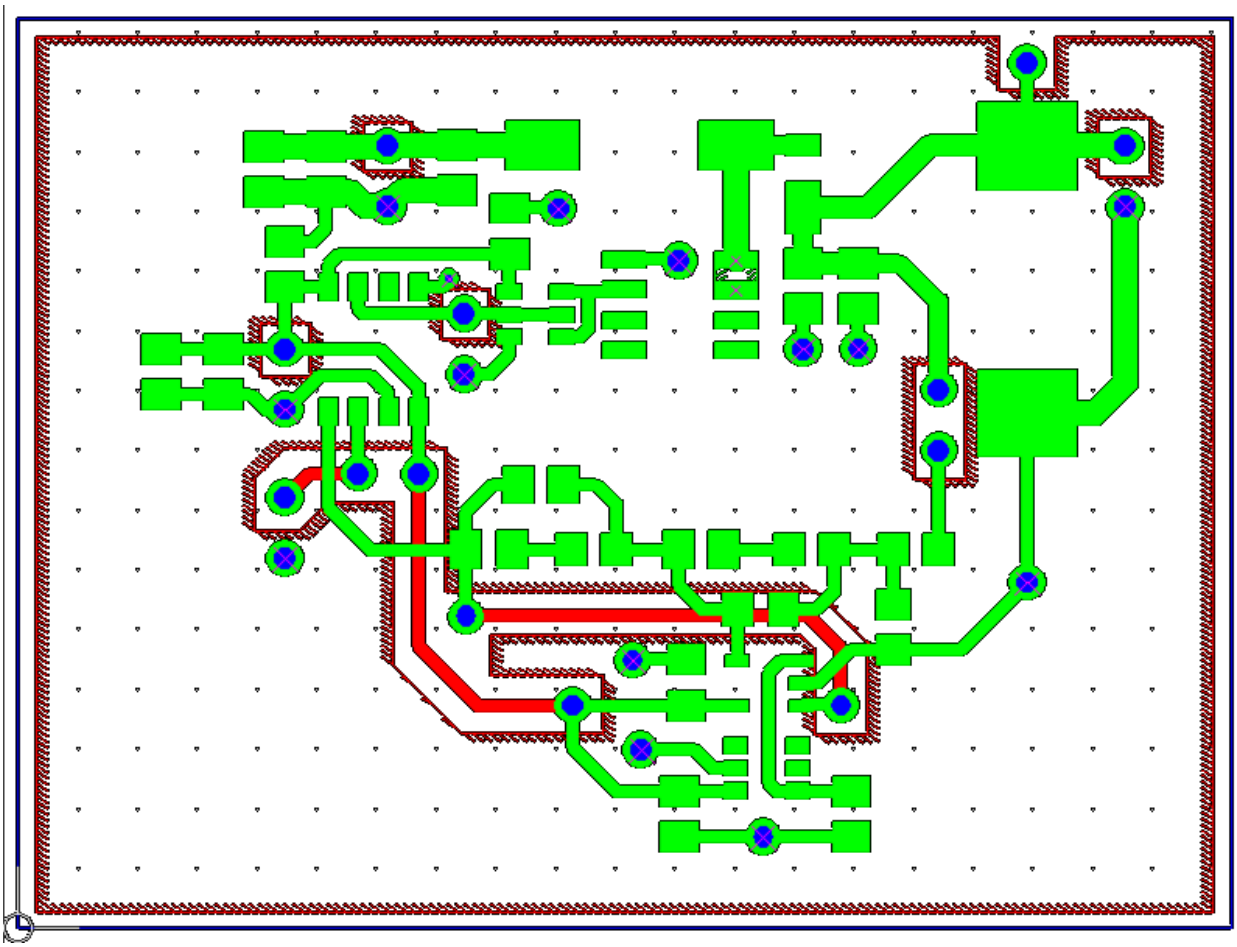

Figure 32: PCB Layout for Power Stage and Control Loop

9.4.2 Triangle Generator First Revision

The triangle wave generator board was the very first board that the team laid out. The board was 2” by 3” and there was no ground plane. Every component was on the top layer and trace length was not taken into consideration. However, an additional bit of copper was added to the drain of the MOSFET to aid in heat dissipation. In general the board worked, but it had some significant flaws, especially at the higher frequencies. The first iteration is shown in the layout below.

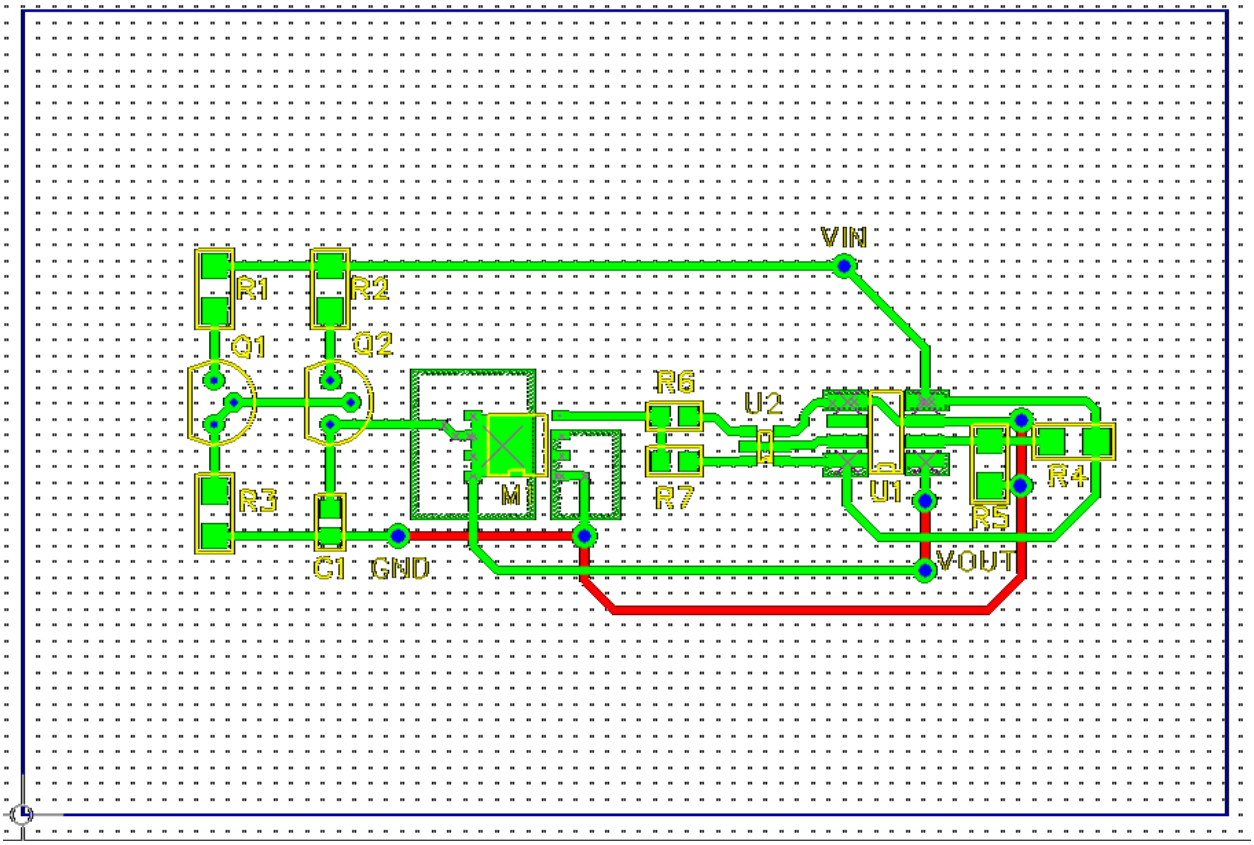

Figure 33: PCB Layout for First Iteration of Triangle Wave Generator

The second iteration was the exact same configuration but with a different layout taking high frequency effects into consideration. The second iteration utilized both sides of the FR4 material to reduce trace length. Large copper areas were used to reduce restrictions in current flow. And the circuit ground return was placed next to the "dirtiest" ground. The second iteration is shown in the figure below.

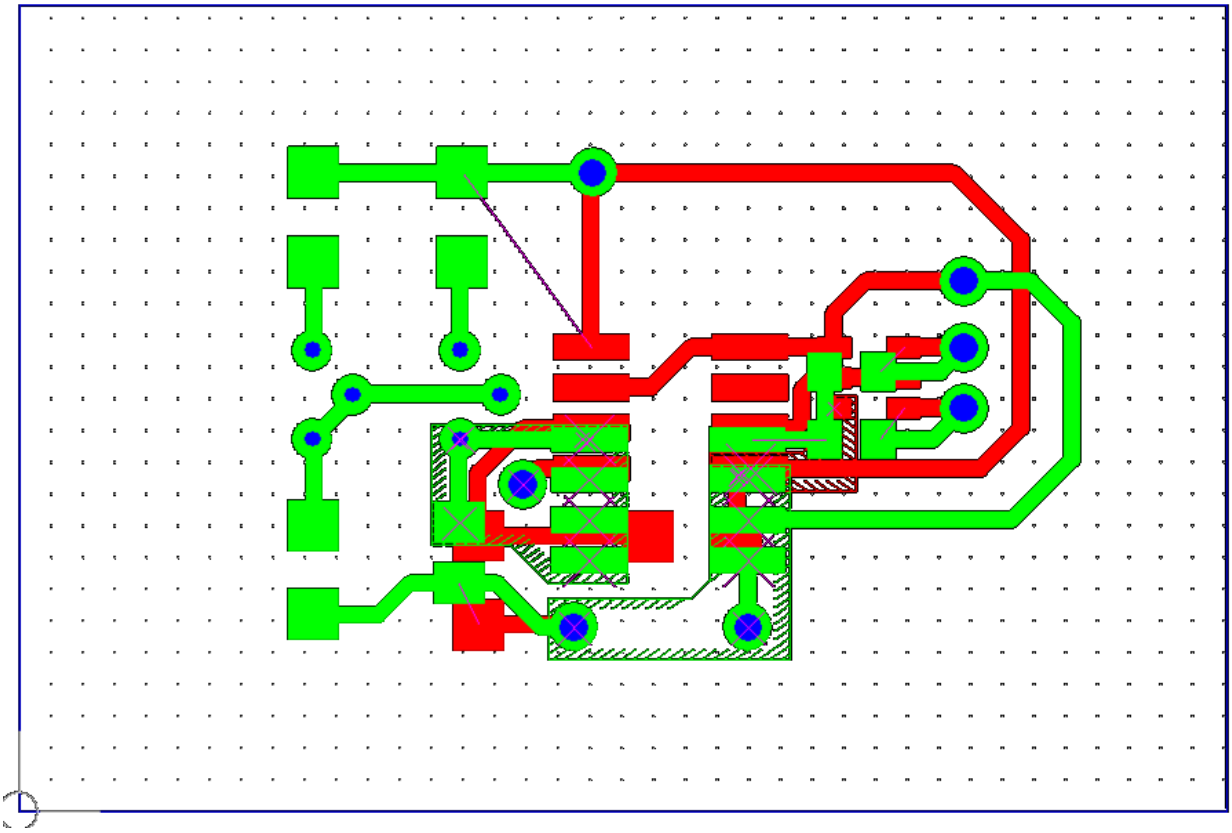

Figure 34: Condensed PCB Layout for First Iteration of Triangle Wave Generator

This iteration reduced some significant problems associated with high frequency effects on PCBs, but the varying characteristics of the MOSFETs made this circuit difficult to control up to 20 MHz.

9.4.3 Triangle Generator Final

The final iteration of the triangle wave generator board is shown in the figure below. The schematic utilized to create the layout was the final revision of the triangle wave circuit. This circuit can be seen in Figure 25. Both sides of the board were used for part placement and traces in order to reduce the overall size. The figure below shows two circuits on one piece of 31mil FR4. All the vias were plated which provided an easy path to the ground plane

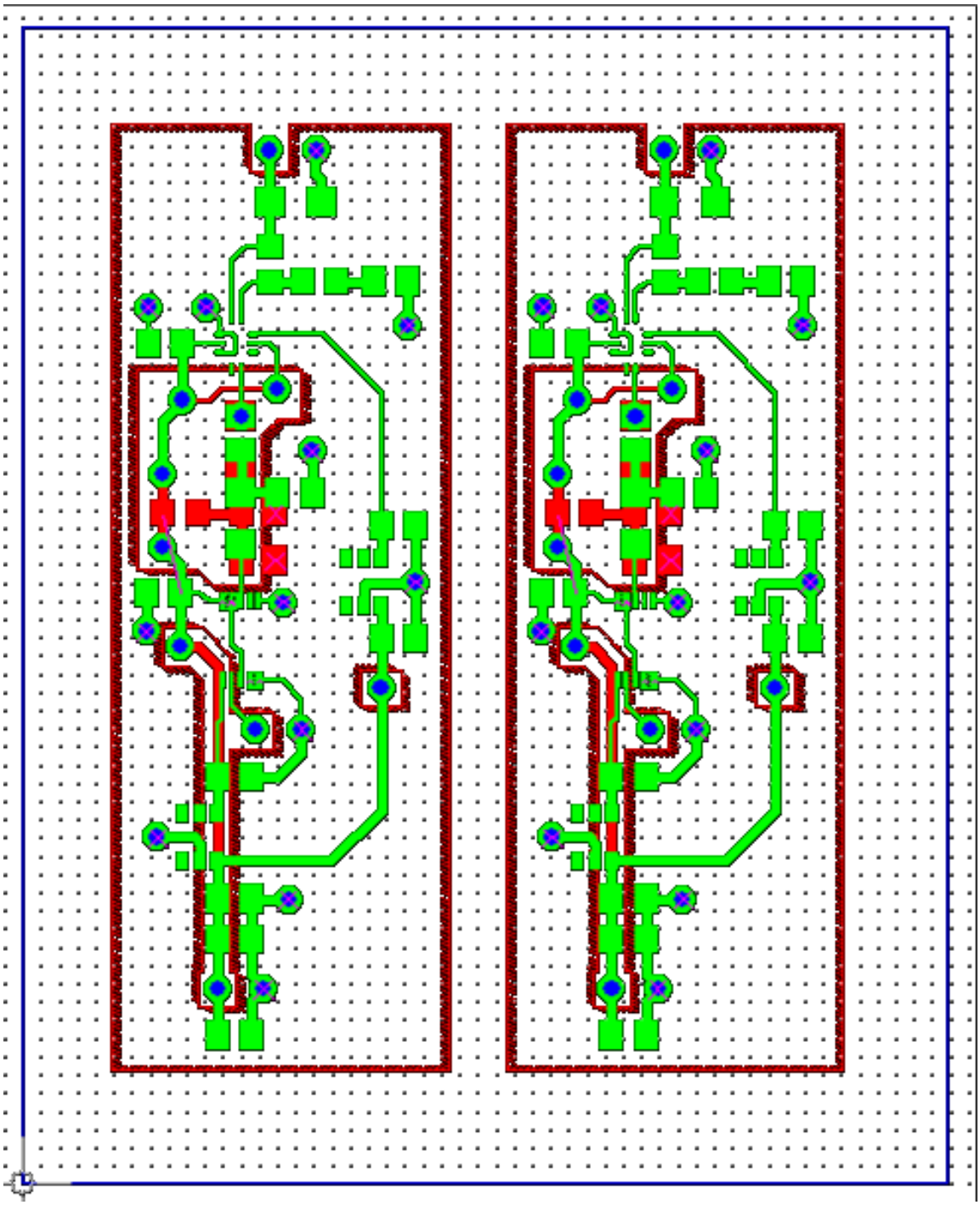

Figure 35: PCB Layout for Final Version of Triangle Wave Generator Board

This board works was simple to make and layout. The most difficult part is in soldering the LTC6409 Op-Amp which is in a QFN package.

10. Testing and Results

The functionality of the three individual building blocks separately is critical to the success of the whole system. The three building blocks to test are the triangle wave generator, the open loop boost converter, and the control loop.

The completed triangle wave board has two sets of pins on the left side and one set of pins on the right side. The two on the left are the inputs and the one on the right is the output of the triangle wave generator. Below is a picture of the finished triangle wave board.

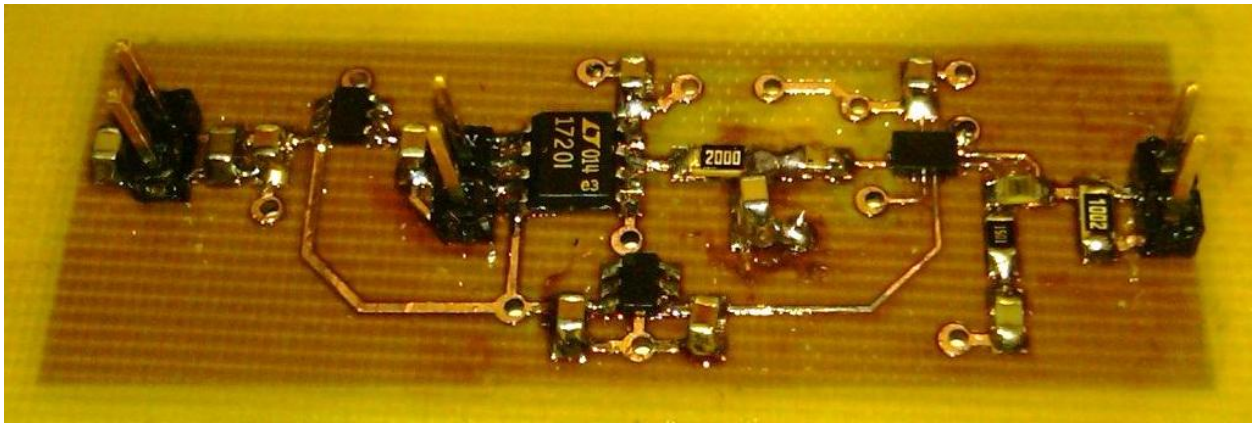

Figure 36: Top View of Triangle Wave Generator Board

Since a single supply op-amp was used in this board, the back of the PCB contained the biasing circuitry to center the triangle around 2.5V, or half of the supply voltage. The back of the board is shown in the picture below

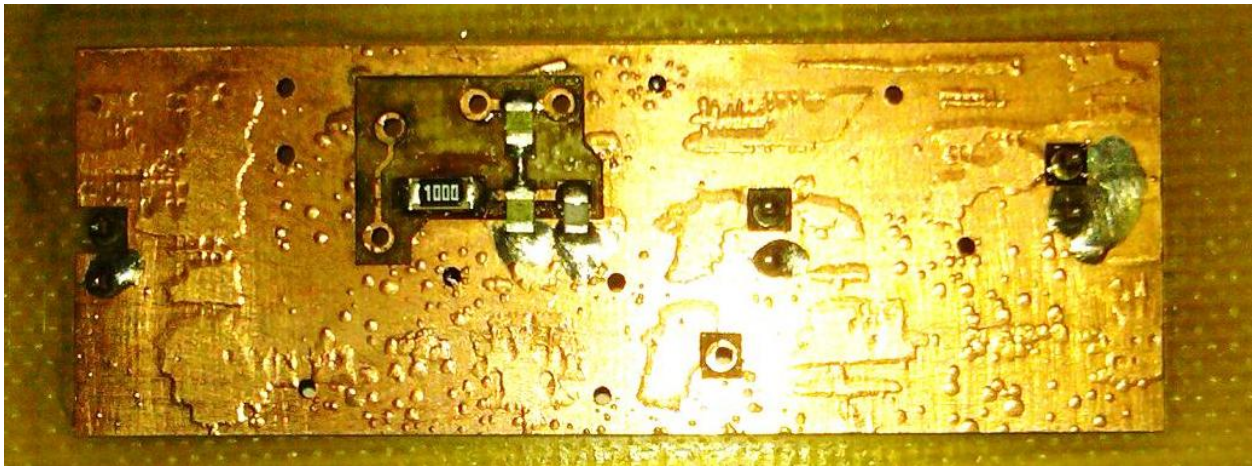

Figure 37: Bottom View of Triangle Wave Generator Board

The power stage and control loop were created on the same board for ease of use and diagnostic purposes. There are three inputs and one output on the whole board. The three inputs are located on the left side of the board and from top to bottom are, 3.3V, 5V from a power supply, and the connection for the triangle wave. The output is located on the right side of the board next to the load resistor. The completed board is shown in the figure below.

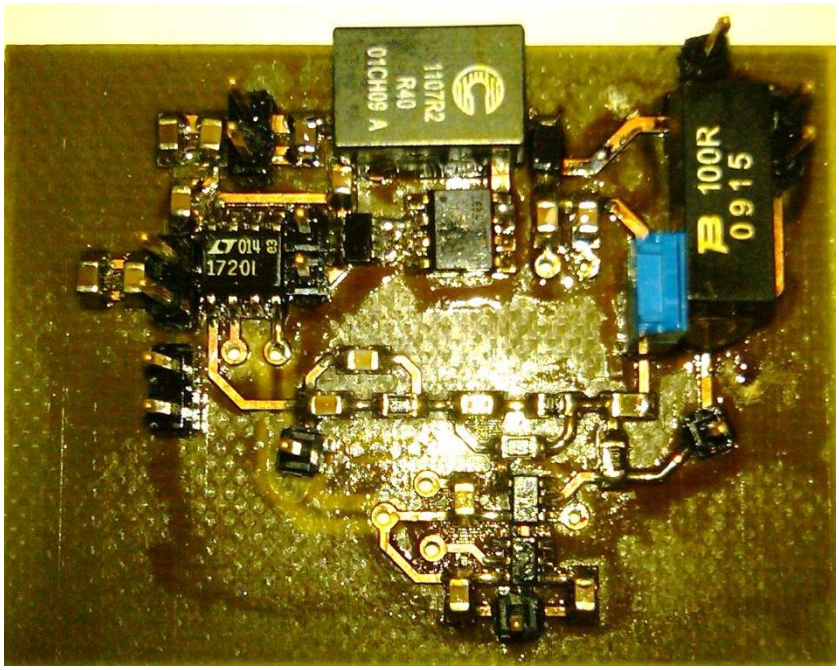

Figure 38: Completed Power Stage and Control Loop on FR4

There is a jumper pin located on the board on the left side of the load resistor. This jumper pin allows the user to disconnect the control loop and test the boost converter in open loop configuration. In order to test the device in open loop configuration, there must be a pulse applied directly to the input of the gate driver and the jumper removed from the board.

The two figures below shows the configuration for connecting the triangle board to the input of the comparator on the power stage PCB. The black wire connecting the two boards is made up of well insulated 18 gauge wire. The wires are soldered to female 100 mil pin jacks. The whole wire assembly is then wrapped in heat shrink to increase the amount of shielding to minimize noise in the environment.

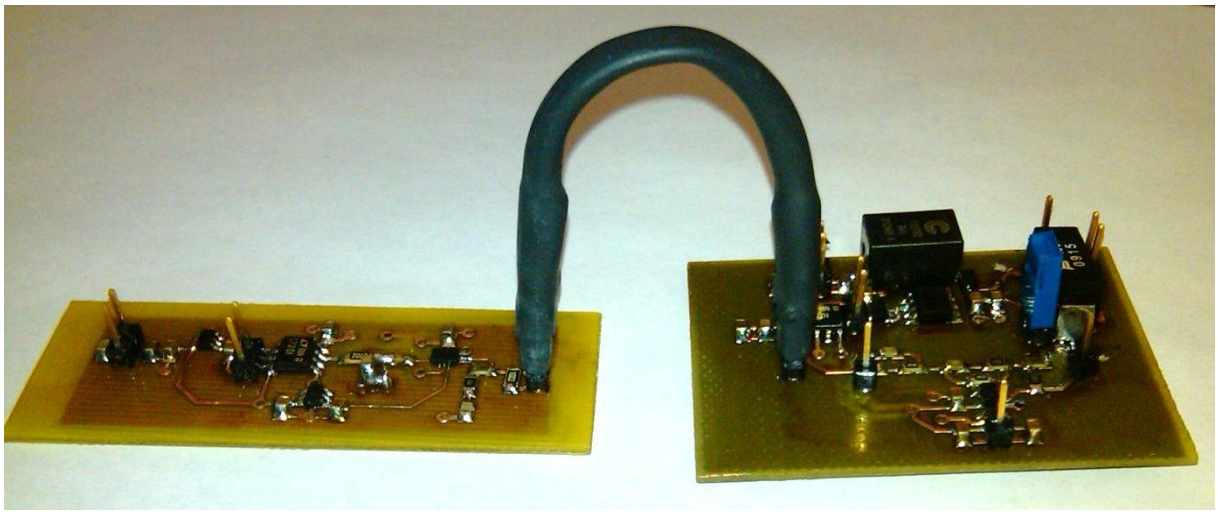

Figure 39: Connected Triangle Wave and Power Stage Board Configuration

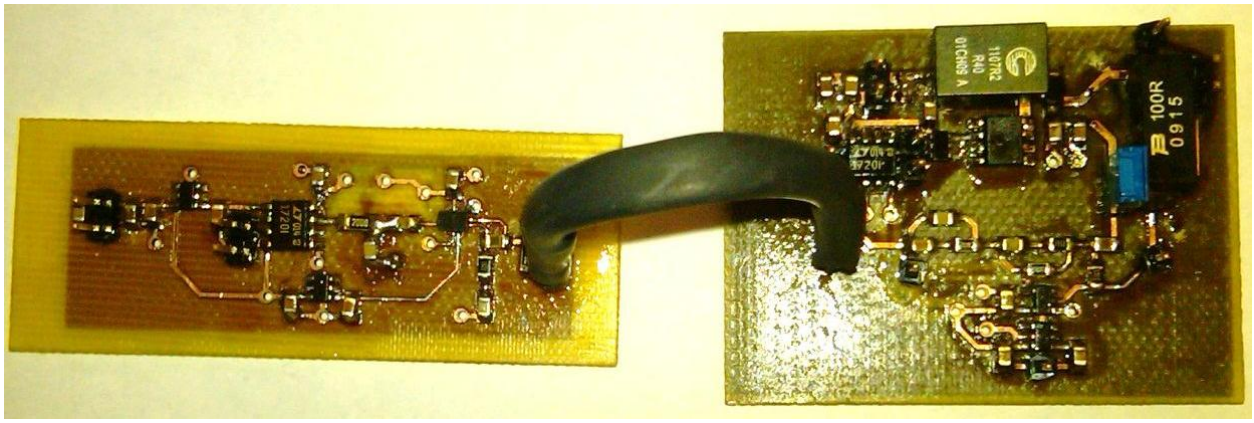

Figure 40: Connected Triangle Wave and Power Stage Board Configuration (Top View)

10.1 Overall Functionality of the Triangle Wave and the Boost Converter

In order to test the functionality of the triangle wave generator, the team had to determine what the proper inputs are for an expected output signal. The output signal should always be a triangle wave because the output of a comparator is a square wave and the integral of a square wave is a triangle wave. The inputs required for proper operation of this circuit are 5V from a power supply and a sine wave with an amplitude of $5V_{pk\text{-}pk}$ and a DC Offset of 2.5V. The frequency should be set to whatever frequency is needed for the boost converter testing, either 5, 10, or 20 MHz.

The figure below shows the output of the triangle wave generator with an input sine wave of 5MHz.

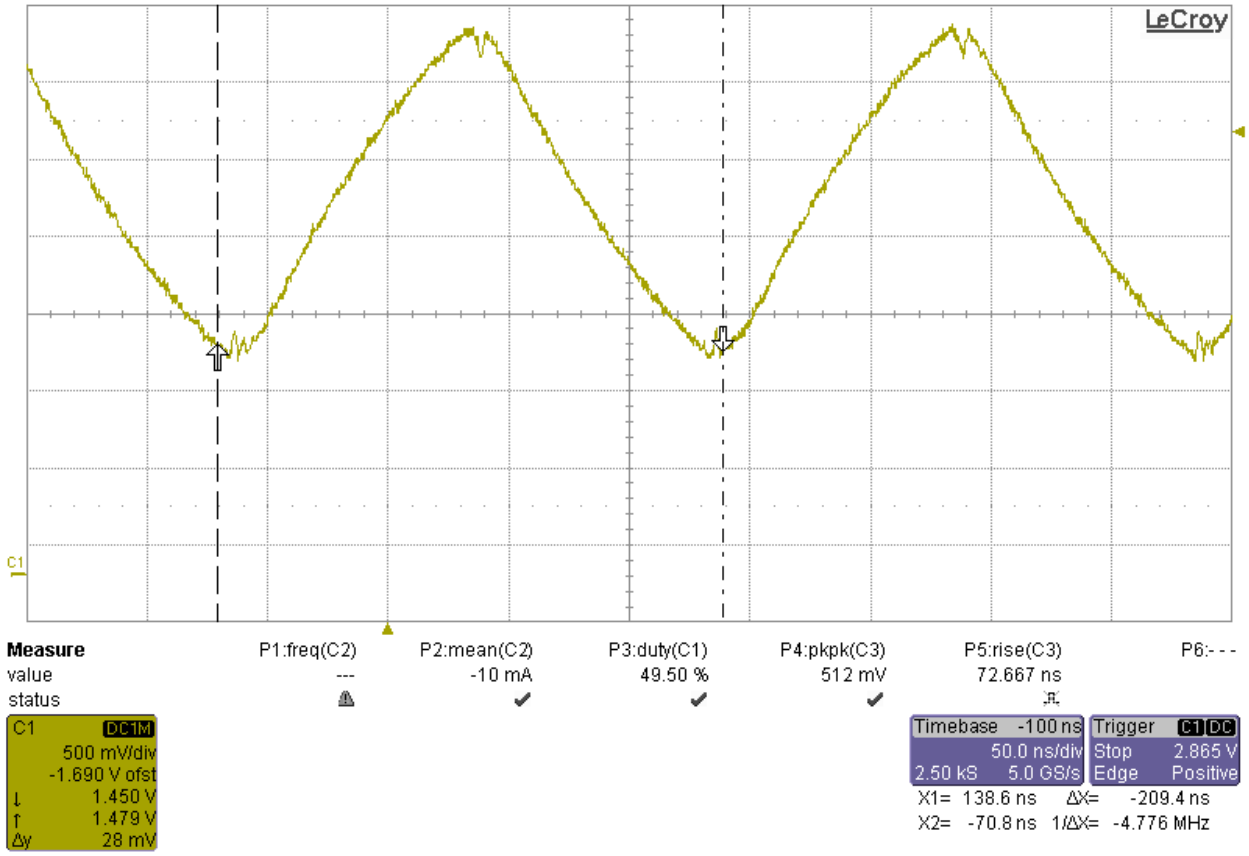

Figure 41: Condensed PCB Layout for First Iteration of Triangle Wave Generator

As seen in the figure above, the output very nearly resembles a triangle wave with a slight curve due to the typical charging of a capacitor via a resistor. The measured frequency is 4.776MHz which is very close to the 5MHz input. There are a lot of possibilities for error in this result including measurement error, error from the function generator, or parasitic capacitance from the oscilloscope probe. The output peak to peak voltage was measured to be 2.1V centered about 2.5V DC.

The figure below shows the output of the triangle wave generator with an input sine wave of 10MHz.

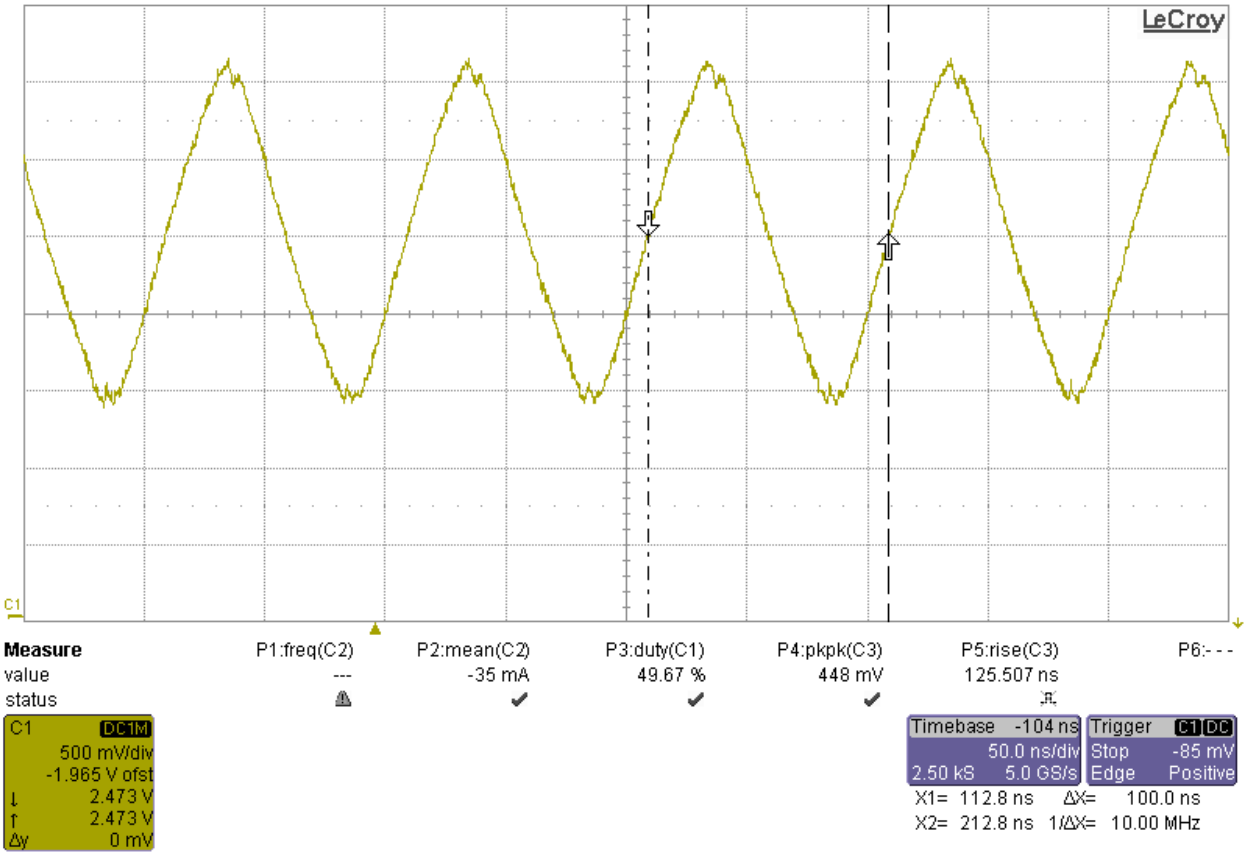

Figure 42: Condensed PCB Layout for First Iteration of Triangle Wave Generator

As seen in the figure above, the output is a triangle wave with minimal curve due to the typical charging of a capacitor via a resistor. The measured frequency is 10.1MHz which is very close to the 10MHz input. There are a lot of possibilities for error in this result including measurement error, error from the function generator, or parasitic capacitance from the oscilloscope probe. The output peak to peak voltage was measured to be 2.2V centered about 2.5V DC.

The figure below shows the output of the triangle wave generator with an input sine wave of 20MHz.

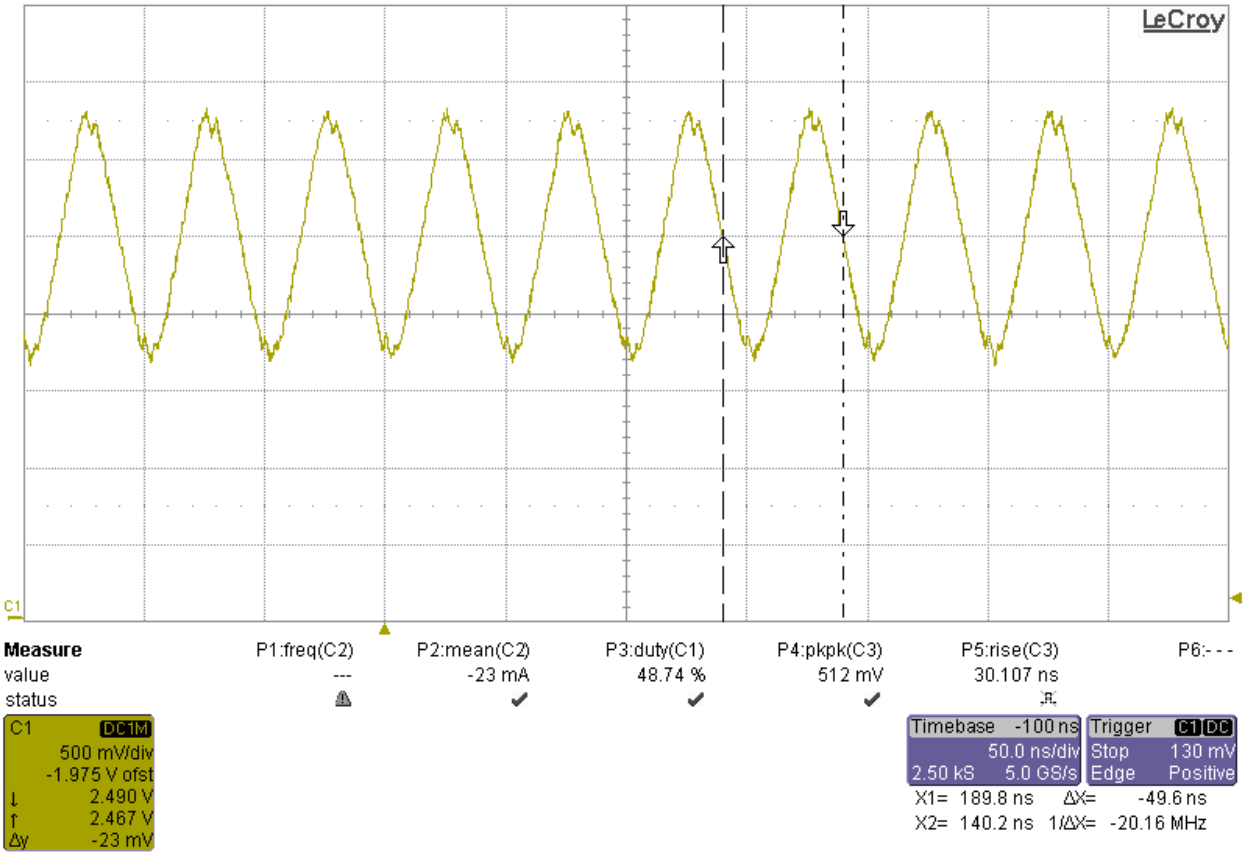

Figure 43: Condensed PCB Layout for First Iteration of Triangle Wave Generator

As seen in the figure above, the output is a triangle wave with almost no curve due to the typical charging of a capacitor via a resistor. The measured frequency is 20.18MHz which is very close to 20MHz. There are a lot of possibilities for error in this result including measurement error, error from the function generator, or parasitic capacitance from the oscilloscope probe. The output peak to peak voltage was measured to be 1.58V centered about 2.5V DC.

With the functionality of the triangle wave board confirmed, the next step was to verify the functionality of the open loop boost converter. To verify the functionality, the team applied a variable duty cycle pulse voltage from a function generator to the input of the gate drive IC. The voltage pulse had a peak to peak voltage of 5V with a DC offset of 2.5V. The team then varied the duty cycle on the function generator to change the output voltage.

The following oscilloscope screenshot shows the waveform applied to the gate of the MOSFET in magenta and the output voltage of the circuit in blue.

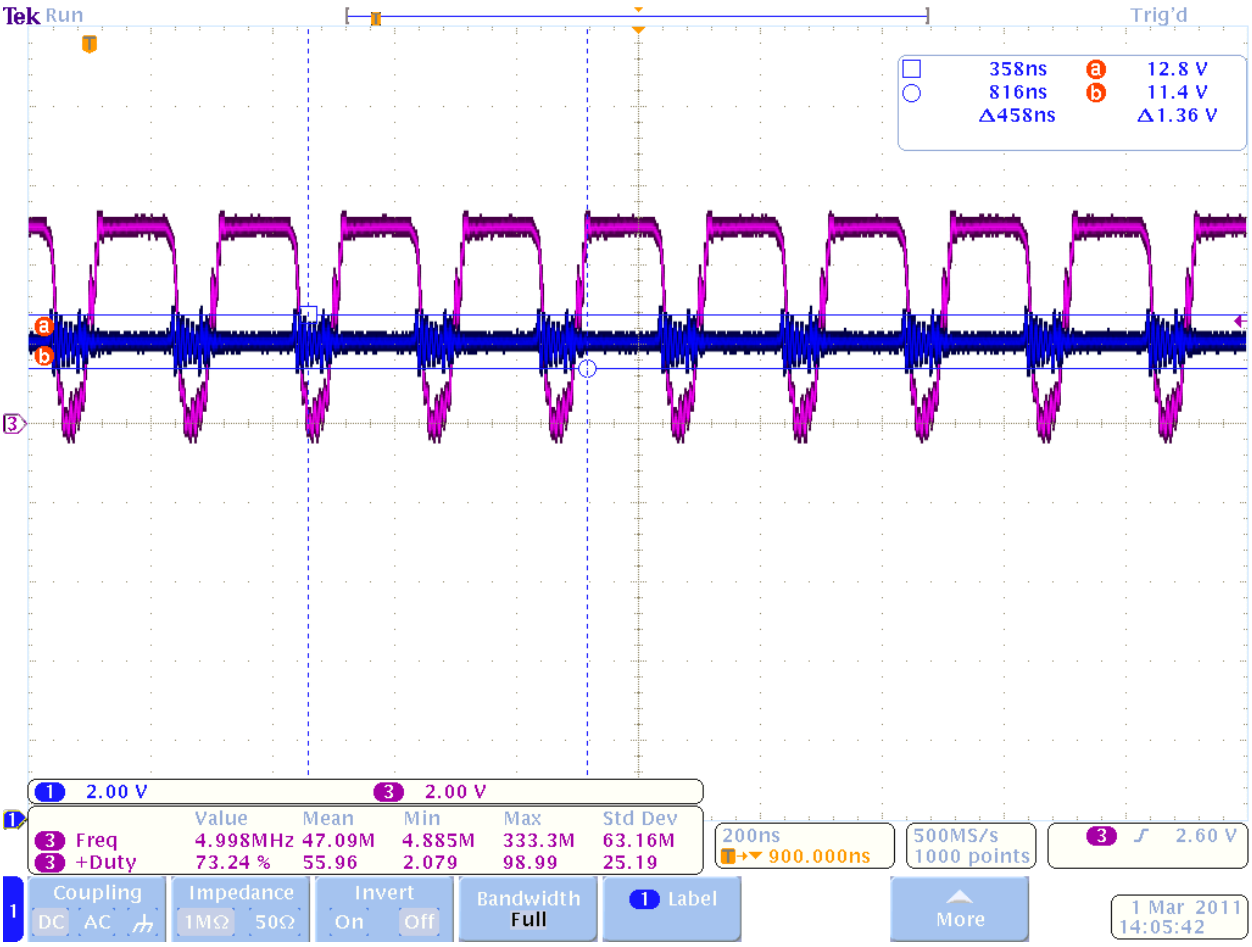

Figure 44: Condensed PCB Layout for First Iteration of Triangle Wave Generator

As seen from the screenshot above, a duty cycle of about 73% produces an output voltage of about 12V. The ringing on the output makes the output voltage have a minimum of about 11.4V and a maximum of about 12.8V.

The following table shows the current drawn and voltage created by the circuit in open loop configuration in simulation and experimentation. The gate drive signal applied in simulation and experimentation was a pulse with a $5V_{pk\text{-}pk}$, a 2.5V DC offset, a frequency of 5MHz and a varied duty cycle.

Open Loop Boost Converter				
Duty Cycle	**V_{OUT} (V)**	**V_{OUT} (SIM) (V)**	**I_{IN} (A)**	**I_{IN} (SIM) (A)**
30.0%	4.84	5.29	0.188	0.130
35.0%	5.16	5.636	0.214	0.238
40.0%	5.48	6.039	0.245	0.270
45.0%	5.84	6.571	0.286	0.288
50.0%	6.40	7.291	0.340	0.349
55.0%	7.10	8.124	0.416	0.440
60.0%	7.90	9.15	0.519	0.550
65.0%	8.80	10.49	0.663	0.690
70.0%	9.90	12.19	0.877	1.050
75.0%	11.40	14.57	1.213	1.560
78.0%	12.50	16.46	1.494	1.970

Table 13: Manufactured Boost Converters

As can be seen from the table above, the voltage and current at lower duty cycles in simulation matched closely with the measured results. As the duty cycle increased above 60%, the current and voltage values differed by a greater amount.

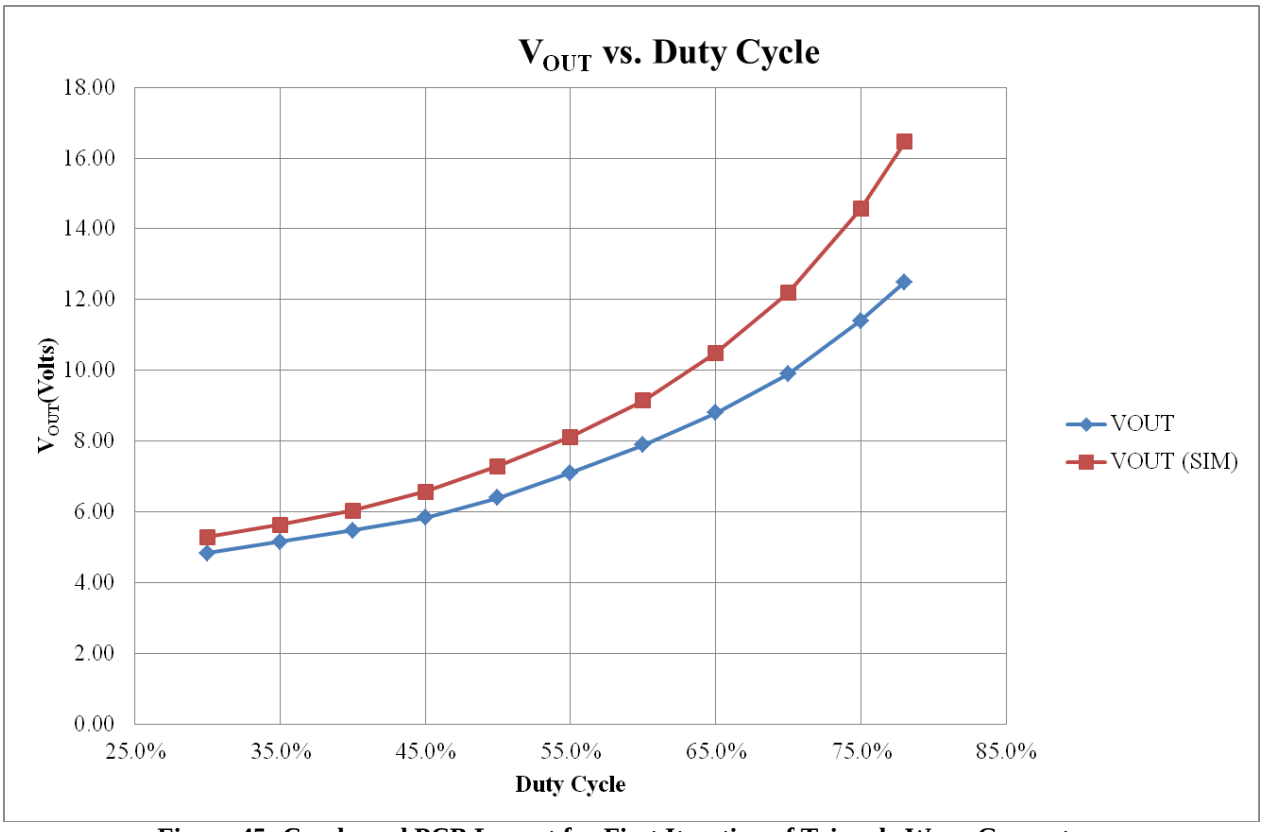

Figure 45: Condensed PCB Layout for First Iteration of Triangle Wave Generator

The figure above is a visual plot of the output voltage in simulation and experimentation as a function of the applied duty cycle to the gate of the MOSFET.

The last part was to verify the functionality of the compensation network. To test this functionality, the team applied a $20mV_{pk-pk}$ sine wave with a 12V DC offset to the input of the network. Then using the bode plot of the compensation network, the team determined the output voltage by observing the gain and multiplying it by the input voltage. The team did this for a range of frequencies from 5-20MHz at three discrete points, 5, 10 and 20MHz. The output of the compensation network was exactly what the team expected from the transfer function and the input voltage. All three components work separately as expected.

10.2 Closed Loop Feedback Functionality Testing

All three parts of the boost converter were connected to test the functionality and the performance of the design. The design did not contain a soft start so a jump start was required. To jump start, a voltage of 12V was inserted at the output of the power stage so that the control loop could start. Then the control loop output and the triangle wave generator create a PWM to turn on the MOSFET in the power stage. The 12V is removed and the closed loop boost converter design operates on its own.

Below are screen shots of input and output waveforms of the closed loop boost converter. The first waveform is of the input of 3.3V, the boost converter is operating at 5MHz and the load resistance is 100Ω. The waveform has 120.05mV of ripple which is caused by noise. The output is shown in Figure 46. The output is 11.99V with an output ripple of 1V.

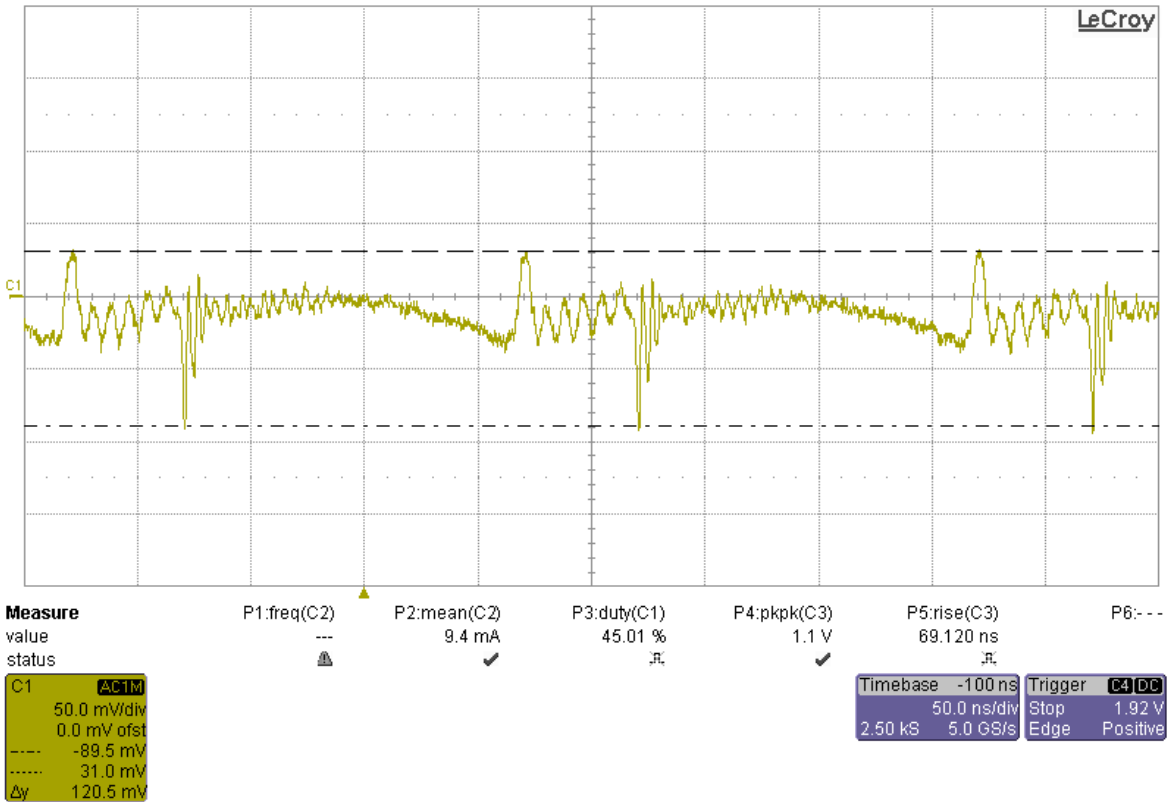

Figure 46: Vin=3.3V, 5MHz, 100R_load

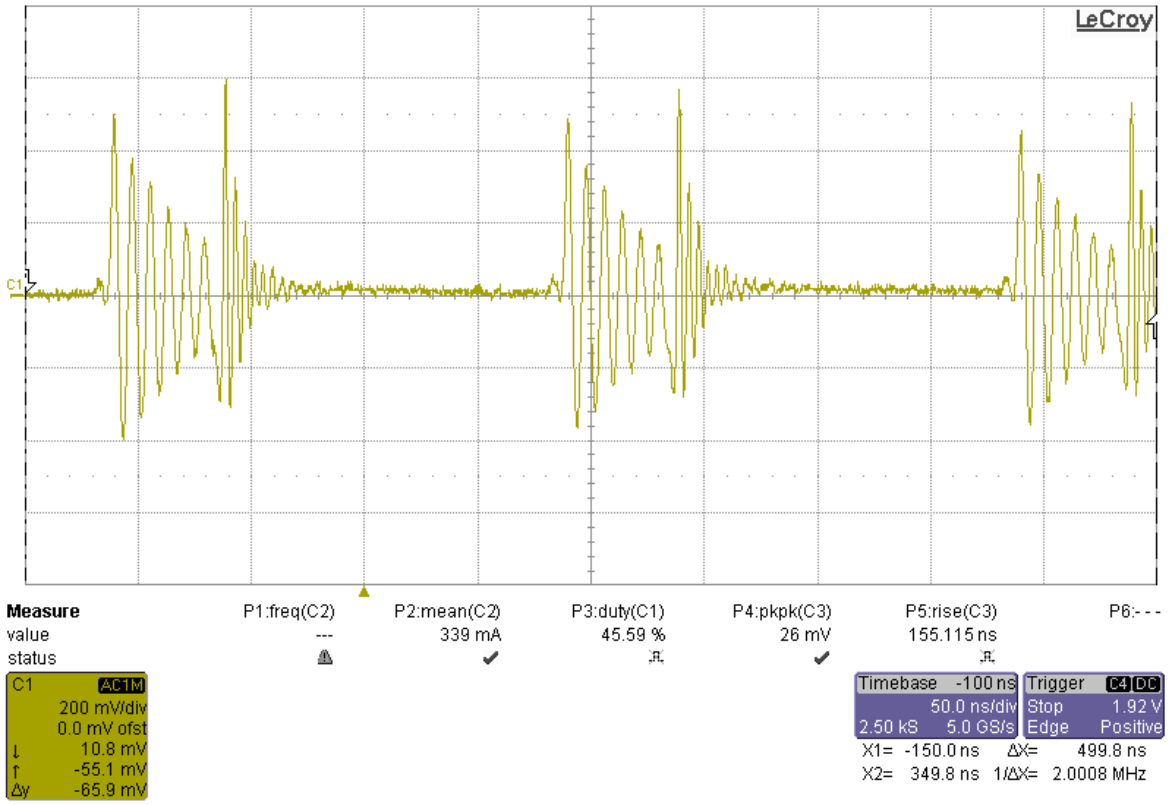

Figure 47: Vout=11.99V, 5MHz, 100R_load, Vin 3.3V

The waveform in Figure 48 is of a 5V, the boost converter is operating at 5MHz and the load resistance is 100Ω. The waveform has 62mV of ripple. This ripple is caused by noise. The output is shown in Figure 49. The output is 11.99V with an output ripple of 600mV.

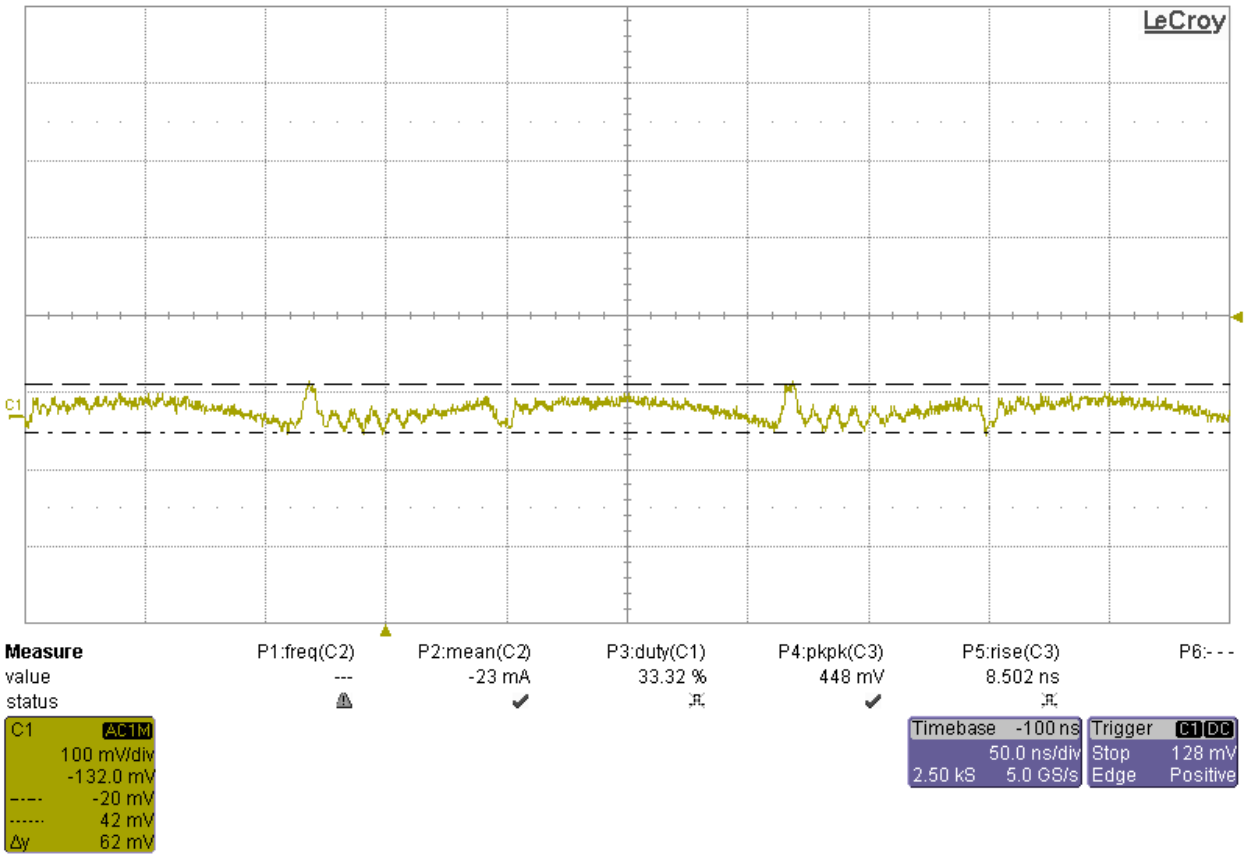

Figure 48: 5V, 5MHz, 100R_LoadVout 11.99

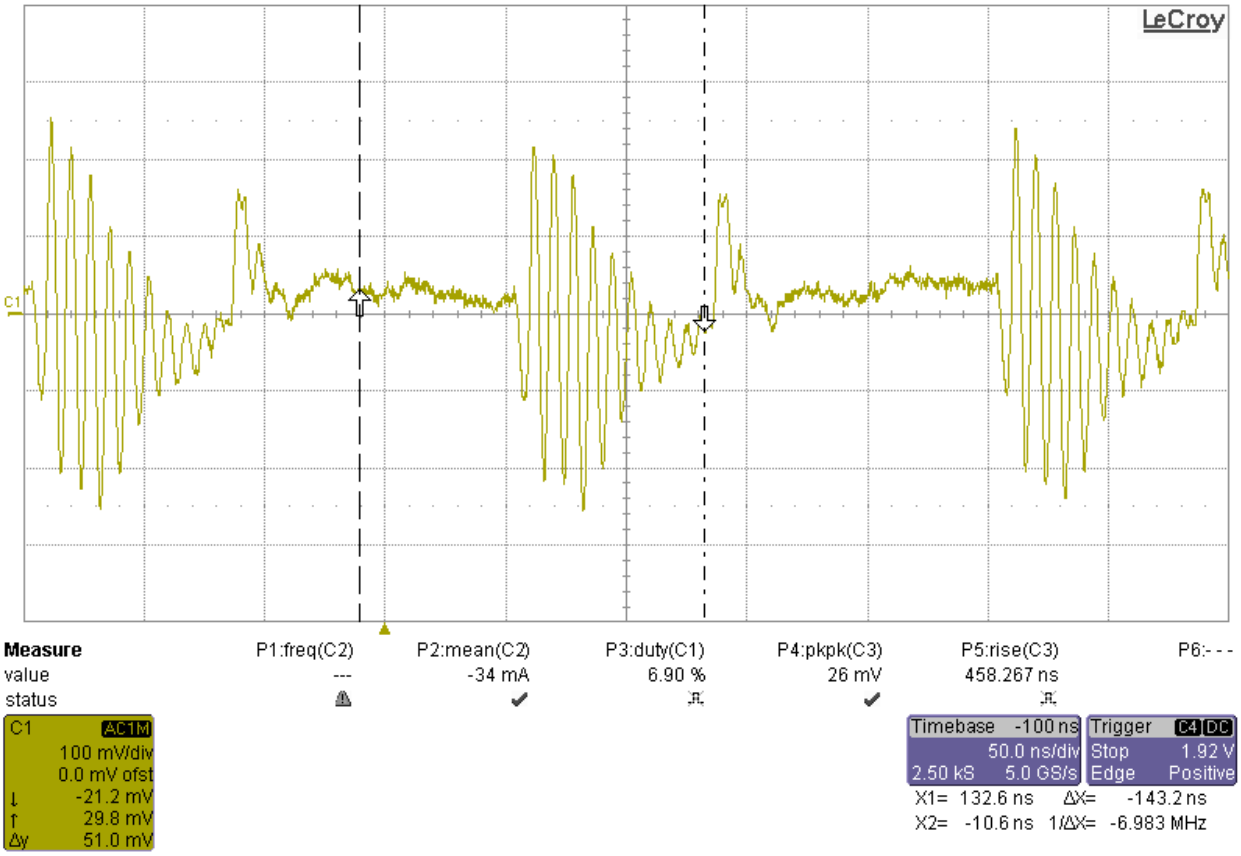

Figure 49: Vout=11.99V, 5MHz, 100R_load

The ringing in the output is greater than the project specifications of only 10mV because of the parasitic inductance in the ground plane of the PCB. There is 6mm between ground of FET and ground of output capacitor. The output ripple measured was smaller than the simulation predictions of $2V_{pk\text{-}pk}$.

The waveform shown below is measured at the gate drive output. The duty is approximately 72% as expected for the boost converter MOSFET.

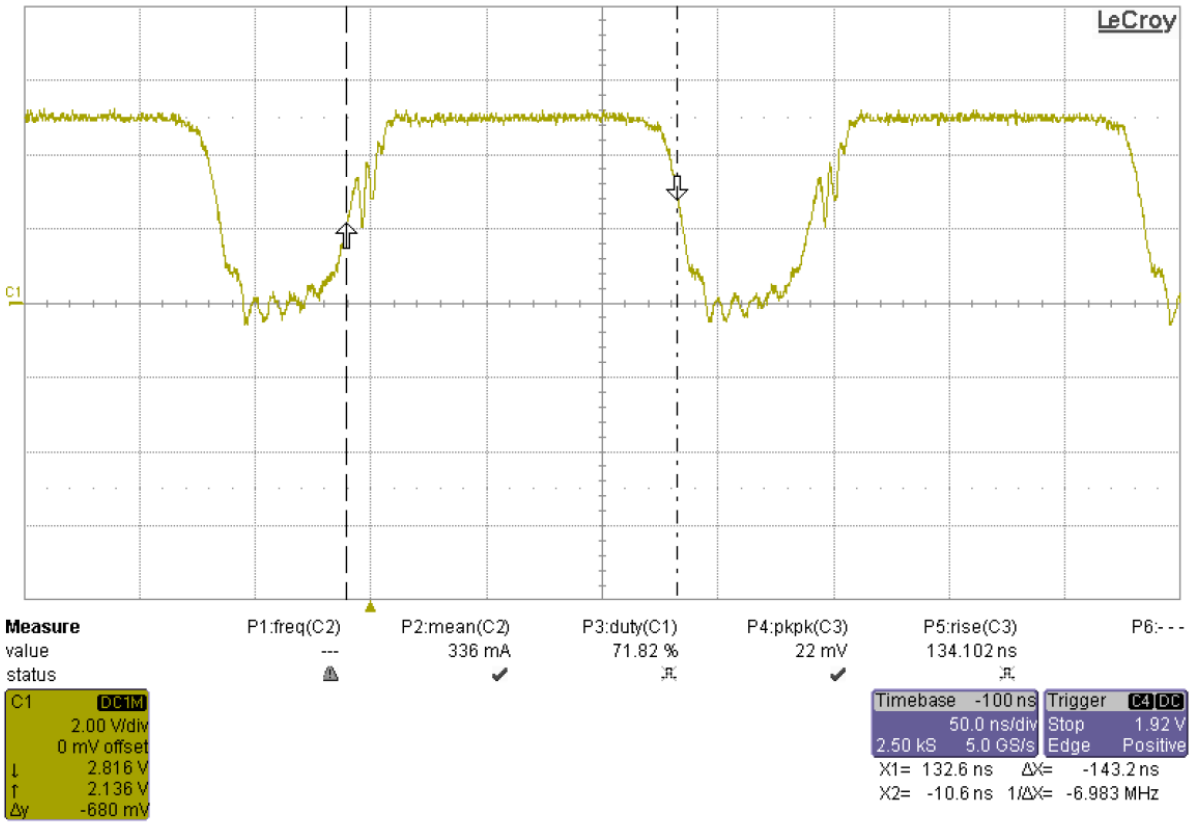

Figure 50: Gate Drive output at 5MHz

10.3 Efficiency Testing

The following efficiency testing was conducted in a closed loop configuration. The efficiency was calculated by the total power out divided by total power into the circuit. The equations used are shown below. [5]

$$P_{OUT}/P_{IN} = \text{Efficiency Percentage}$$

Equation 34: Efficiency Percentage Equation

$$P_{OUT} = V_{OUT}^2/R_{LOAD}$$

Equation 35: Output Power Calculation

$$P_{IN} = V_{IN} * I_{IN}$$

Equation 36: Input Power Calculation

The boost converter was tested at an operating frequency of 5MHz and 10MHz and an input voltage of 3.3V and 5V. The load resistance was varied from 50 - 100Ω and the efficiency

was then calculated. The figure below shows three curves based on the collected data; the raw data is included in the Appendix 15.2. The high efficiency of 66% is achieved from the boost converter operating at 5MHz with the maximum input voltage and load resistance of 50Ω. As the load resistance is increased the efficiency is linearly decreased. Operating at 5MHz, the boost converter maintains an efficiency above 50%.

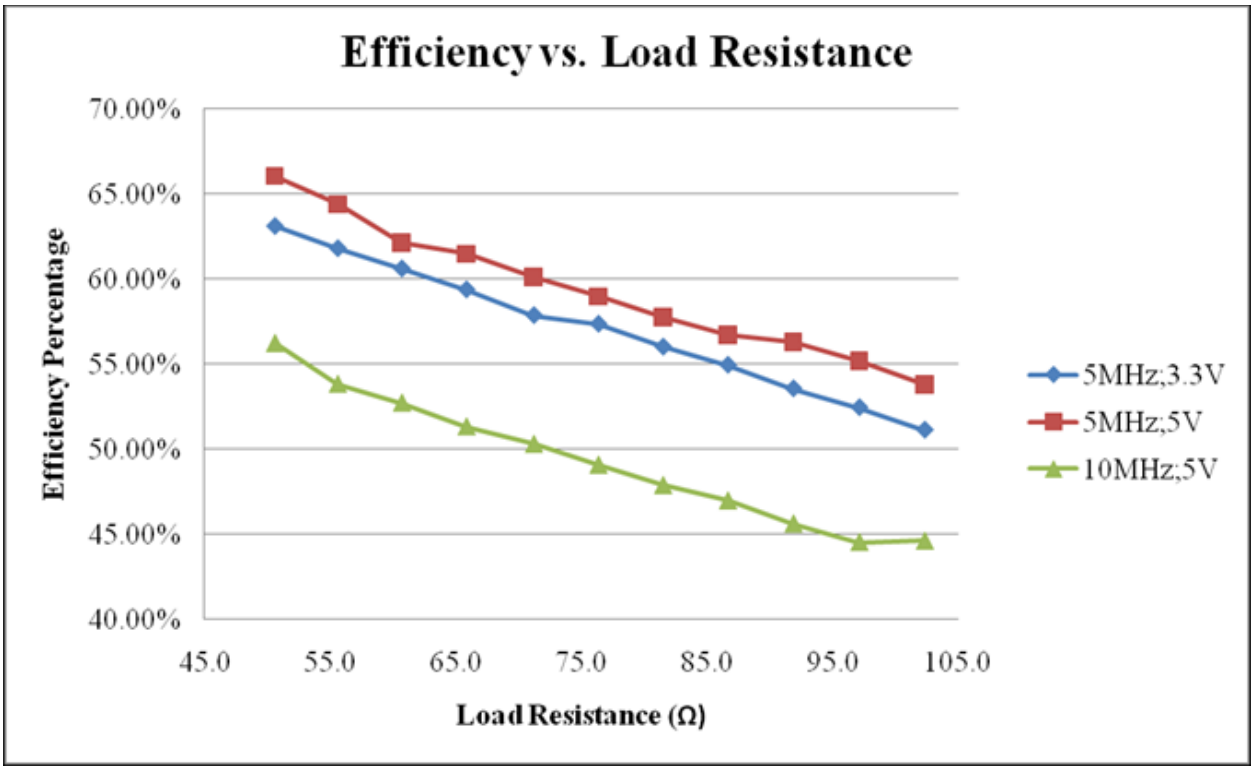

Figure 51: Efficiency vs. Load Resistance Plot

11. Project Evaluation

The team had some great successes in this project, but many challenges were overcome in order to achieve the original goal of the project. The challenges included creating a ramping waveform with a frequency up to 20MHz, overall part selection, board layout, and passive component sizes in the compensation network.

The first iteration of the triangle wave generator relied completely on the timing of the comparator and the discharge of the capacitor through an "on" resistance of a MOSFET. This method of triangle wave generation created a lot of problems because of poor rise and fall times in the comparator and a lack of ability to source and sink enough current to the gate of the MOSFET. Even with board redesigns to reduce parasitic effects, the triangle wave generation wasn't working. The first idea that came as a solution was to make a window comparator, but the only way to make that function properly was to have two comparators that fed into a D-Latch. All of those components had significant rise and fall times which would severely limit the ability to achieve a triangle wave up to 20MHz. Finally, the decision to make an integrator and use an external function generator was made, and the team had a functioning triangle wave generator.

Part selection was an unbelievable long, arduous task for this project because of the high frequency and the high current demand. The high frequency became an issue when parts had poor rise and fall times which limited the ability to make the boost converter function at 20MHz. Additionally, capacitors act almost like short circuits at high frequency, and 20MHz is enough to make some ceramic capacitors act as short circuits, so it was necessary to examine data sheets for functionality up to 20MHz and beyond. The high current demand made it difficult to select passive components with a high ESR. The high ESR would decrease the overall efficiency, but

it would also generate a lot of heat, and some parts lose linear functionality over significant temperature changes. The part selection process proved to be a very difficult challenge for the success of the project.

High frequency PCB's are difficult to design because of the additional parasitics created by the electromagnetic interaction among the components. The first board laid out had a large distance between the ground of the MOSFET and the ground of the output capacitor, and this distance created parasitic inductance in the ground plane. This parasitic inductance would have caused even larger ripples in the output voltage. Minimizing the trace lengths and maximizing the board density allowed the project to function even on a large board like the 31 mil FR4 PCB.

The last major challenge the team faced was the design of the compensation loop. The value of the capacitor in one of the stages was originally about 0.4pF. The trace on the PCB in and of itself has about 3pF or parasitic capacitance, so a component valued less than the parasitic capacitance would be infeasible for the success of the compensation loop. The compensation loop component values needed to be reselected in order to maintain the proper gain and phase corrections, but achieving large passive component values.

This MQP was a challenge to say the least, but without these challenges and redesigns, this project would not have worked as well as it did. The struggles and late nights were all well worth the effort for the team.

12. Future Recommendations

Although a significant amount of work was completed on this project, there is still a large amount left to do to achieve the goal that Draper has set for the project. The most important piece of future work is to minimize the rise and the fall times of the comparator and the gate driver in order to achieve switching frequencies above the 13MHz that our team achieved. The next step is to miniaturize the whole design in either the MCM-D or iUHD form to decrease the parasitic effects of having long traces on a PCB. This will also reduce the large ripple voltage in the output which is caused by the parasitic inductance in the ground plane of the PCB that our team made.

Another action item that needs to be done to make this project stand-alone is to design a new method for a ramping waveform generation. The design used in this project worked very well for the proof-of-concept, but the final product cannot rely on an external function generator. The whole goal is to make this device as small as possible, so having a function generator attached to it would be detrimental to the overall goal.

Other tests that need to be performed on the proof-of-concept in order to show functionality to the customer include testing different load types, like inductive and capacitive loads. Additionally, the whole system needs to be tested under transient load conditions to show the robustness of the compensation network.

Lastly, some sort of soft-start method needs to be created for this boost converter. The proof-of-concept created in this MQP needed a "jump-start" of 12V at the output to force the control loop to start to regulate the output voltage. One method for achieving such a mechanism is to create a variable reference voltage for the op-amp in the compensation network that ramps from a small voltage to the voltage needed for the desired 12V output.

13. Conclusion

The final outcome of the project was a fully functioning CCM boost converter. The boost converter is capable of operating at 13MHz. The reason for it not being able to operate at the projects' initial goal of 20MHz is that the necessary parts could not be obtained or created in the narrow time frame. The boost converter achieves a constant 12V output when it is experiences loads of 50-100Ω and has voltage inputs of 3.3-5V. Furthermore, the boost converter minimized the necessary inductor from 680µH to 400nH, and the necessary output capacitor from 4.7µF to 1.8µF. As a whole, the boost converter achieved an efficiency above 50% at an operating frequency of 5MHz. In conclusion, the project is considered to be a great success by everyone involved, and praised for furthering the advancement of boost converters and power electronic circuits.

14. References

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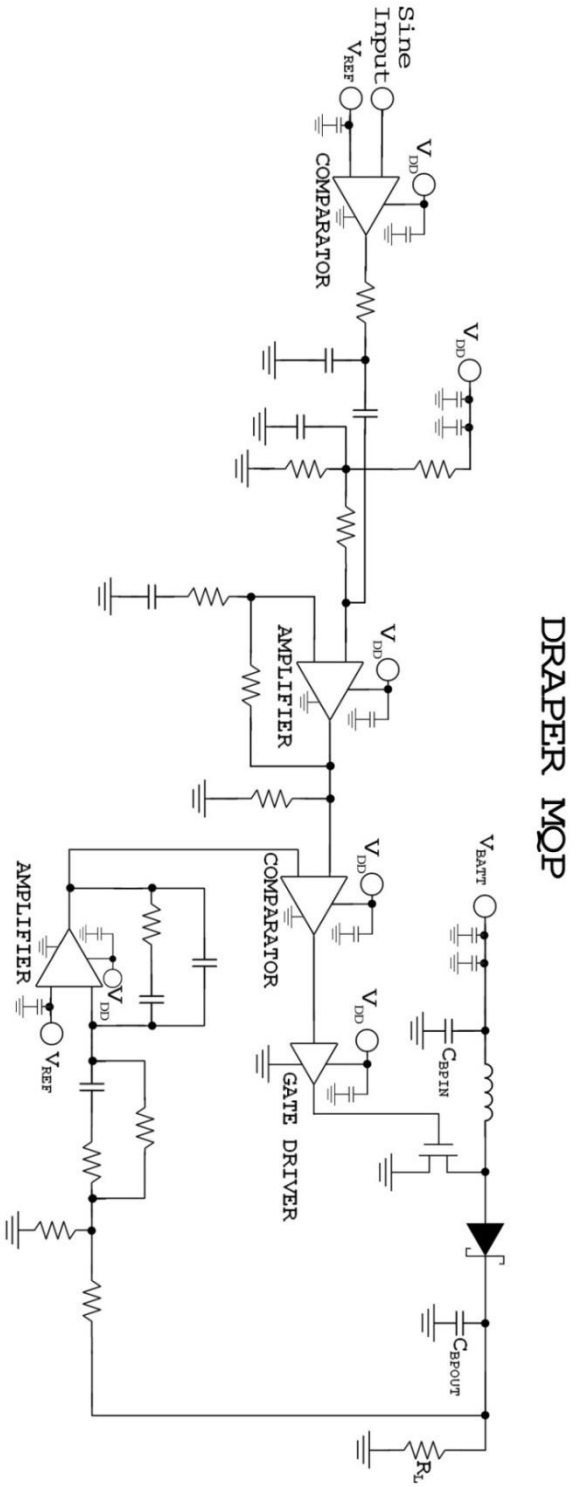
15. Appendices

15.1 Overall Block Diagram



15.2 Raw Data

Closed Loop

100 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.304	4.937		4.907
I_{IN}	0.832	0.529		0.642
R_{LOAD}	102.3	102.3		102.3
V_{OUT}	11.99	11.99		11.99
P_{IN}	2.749	2.612	0.000	3.150
P_{OUT}	1.405	1.405	#DIV/0!	1.405
Efficiency	51.12%	53.81%	#DIV/0!	44.61%

80 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.285	4.925		4.913
I_{IN}	0.959	0.620		0.750
R_{LOAD}	81.5	81.5		81.5
V_{OUT}	11.99	11.99		11.99
P_{IN}	3.150	3.054	0.000	3.685
P_{OUT}	1.764	1.764	#DIV/0!	1.764
Efficiency	56.01%	57.78%	#DIV/0!	47.88%

95 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.294	4.932		4.911
I_{IN}	0.857	0.544		0.677
R_{LOAD}	97.1	97.1		97.1
V_{OUT}	11.99	11.99		11.99
P_{IN}	2.823	2.683	0.000	3.325
P_{OUT}	1.481	1.481	#DIV/0!	1.481
Efficiency	52.45%	55.18%	#DIV/0!	44.53%

75 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.267	4.919		4.913
I_{IN}	1.005	0.649		0.781
R_{LOAD}	76.3	76.3		76.3
V_{OUT}	11.99	11.99		11.99
P_{IN}	3.283	3.192	0.000	3.837
P_{OUT}	1.883	1.883	#DIV/0!	1.883
Efficiency	57.35%	58.99%	#DIV/0!	49.08%

90 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.291	4.927		4.915
I_{IN}	0.888	0.564		0.698
R_{LOAD}	91.9	91.9		91.9
V_{OUT}	11.99	11.99		11.99
P_{IN}	2.922	2.779	0.000	3.431
P_{OUT}	1.565	1.565	#DIV/0!	1.565
Efficiency	53.56%	56.32%	#DIV/0!	45.62%

70 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.298	4.922		4.907
I_{IN}	1.058	0.682		0.818
R_{LOAD}	71.2	71.2		71.2
V_{OUT}	11.99	11.99		11.99
P_{IN}	3.489	3.357	0.000	4.014
P_{OUT}	2.019	2.019	#DIV/0!	2.019
Efficiency	57.87%	60.15%	#DIV/0!	50.30%

85 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.279	4.926		4.913
I_{IN}	0.921	0.594		0.719
R_{LOAD}	86.6	86.6		86.6
V_{OUT}	11.99	11.99		11.99
P_{IN}	3.020	2.926	0.000	3.532
P_{OUT}	1.659	1.659	#DIV/0!	1.659
Efficiency	54.94%	56.71%	#DIV/0!	46.97%

65 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.295	4.918		4.901
I_{IN}	1.116	0.722		0.868
R_{LOAD}	65.8	65.8		65.8
V_{OUT}	11.99	11.99		11.99
P_{IN}	3.677	3.551	0.000	4.254
P_{OUT}	2.183	2.183	#DIV/0!	2.183
Efficiency	59.38%	61.49%	#DIV/0!	51.33%

60 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.251	4.912		4.893
I_{IN}	1.202	0.776		0.918
R_{LOAD}	60.7	60.7		60.7
V_{OUT}	11.99	11.99		11.99
P_{IN}	3.908	3.812	0.000	4.492
P_{OUT}	2.368	2.368	#DIV/0!	2.368
Efficiency	60.61%	62.13%	#DIV/0!	52.73%

55 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.251	4.901		4.891
I_{IN}	1.287	0.819		0.982
R_{LOAD}	55.6	55.6		55.6
V_{OUT}	11.99	11.99		11.99
P_{IN}	4.184	4.014	0.000	4.803
P_{OUT}	2.586	2.586	#DIV/0!	2.586
Efficiency	61.80%	64.42%	#DIV/0!	53.83%

50 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.239	4.898		4.789
I_{IN}	1.390	0.878		1.055
R_{LOAD}	50.6	50.6		50.6
V_{OUT}	11.99	11.99		11.99
P_{IN}	4.502	4.300	0.000	5.052
P_{OUT}	2.841	2.841	#DIV/0!	2.841
Efficiency	63.10%	66.07%	#DIV/0!	56.23%

Open Loop

100 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.198	4.952	3.240	
I_{IN}	0.630	0.403	0.411	
R_{LOAD}	102.3	102.3	102.3	
V_{OUT}	12.02	12.02	8.23	
Duty Cycle	73.39%	58.80%	60.63%	
P_{IN}	2.015	1.996	1.332	0.000
P_{OUT}	1.412	1.412	0.662	#DIV/0!
Efficiency	70.10%	70.77%	49.72%	#DIV/0!

80 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.201	4.951	3.229	
I_{IN}	0.752	0.502	0.494	
R_{LOAD}	81.5	81.5	81.5	
V_{OUT}	12.03	12.03	8.57	
Duty Cycle	73.39%	58.84%	62.32%	
P_{IN}	2.407	2.485	1.595	0.000
P_{OUT}	1.776	1.776	0.901	#DIV/0!
Efficiency	73.79%	71.46%	56.51%	#DIV/0!

95 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.179	4.957	3.241	
I_{IN}	0.683	0.425	0.457	
R_{LOAD}	97.1	97.1	97.1	
V_{OUT}	12.15	12.03	8.76	
Duty Cycle	73.84%	58.79%	63.00%	
P_{IN}	2.171	2.107	1.481	0.000
P_{OUT}	1.520	1.490	0.790	#DIV/0!
Efficiency	70.02%	70.75%	53.36%	#DIV/0!

75 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.179	4.951	3.211	
I_{IN}	0.813	0.527	0.522	
R_{LOAD}	76.3	76.3	76.3	
V_{OUT}	12.02	12.00	8.60	
Duty Cycle	73.55%	58.74%	62.66%	
P_{IN}	2.585	2.609	1.676	0.000
P_{OUT}	1.893	1.886	0.969	#DIV/0!
Efficiency	73.23%	72.29%	57.80%	#DIV/0!

90 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.198	4.955	3.218	
I_{IN}	0.698	0.447	0.469	
R_{LOAD}	91.9	91.9	91.9	
V_{OUT}	12.09	12.01	8.77	
Duty Cycle	73.55%	58.74%	63.31%	
P_{IN}	2.232	2.215	1.509	0.000
P_{OUT}	1.591	1.570	0.837	#DIV/0!
Efficiency	71.29%	70.90%	55.48%	#DIV/0!

70 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.166	4.953	3.239	
I_{IN}	0.857	0.568	0.534	
R_{LOAD}	71.2	71.2	71.2	
V_{OUT}	12.11	12.02	8.59	
Duty Cycle	73.86%	58.79%	62.29%	
P_{IN}	2.713	2.813	1.730	0.000
P_{OUT}	2.060	2.029	1.036	#DIV/0!
Efficiency	75.91%	72.13%	59.92%	#DIV/0!

85 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.208	4.952	3.227	
I_{IN}	0.729	0.474	0.476	
R_{LOAD}	86.6	86.6	86.6	
V_{OUT}	12.14	12.04	8.64	
Duty Cycle	73.57%	58.87%	62.65%	
P_{IN}	2.339	2.347	1.536	0.000
P_{OUT}	1.701	1.673	0.862	#DIV/0!
Efficiency	72.74%	71.28%	56.09%	#DIV/0!

65 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.196	4.939	3.237	
I_{IN}	0.913	0.608	0.549	
R_{LOAD}	65.8	65.8	65.8	
V_{OUT}	12.09	12.00	8.53	
Duty Cycle	73.56%	58.84%	62.05%	
P_{IN}	2.918	3.003	1.777	0.000
P_{OUT}	2.220	2.187	1.105	#DIV/0!
Efficiency	76.08%	72.83%	62.19%	#DIV/0!

60 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.184	4.930	3.234	
I_{IN}	0.998	0.660	0.577	
R_{LOAD}	60.7	60.7	60.7	
V_{OUT}	12.05	12.01	8.51	
Duty Cycle	73.58%	58.95%	62.00%	
P_{IN}	3.178	3.254	1.866	0.000
P_{OUT}	2.392	2.376	1.193	#DIV/0!
Efficiency	75.28%	73.03%	63.94%	#DIV/0!

55 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.177	4.922	3.229	
I_{IN}	1.114	0.712	0.609	
R_{LOAD}	55.6	55.6	55.6	
V_{OUT}	12.13	12.01	8.47	
Duty Cycle	73.81%	59.02%	61.88%	
P_{IN}	3.539	3.504	1.966	0.000
P_{OUT}	2.646	2.594	1.290	#DIV/0!
Efficiency	74.77%	74.03%	65.62%	#DIV/0!

50 OHM Load	5 MHz		10 MHz	
Measured	V_{IN}=3.3V	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=5V
V_{IN}	3.149	4.915	3.229	
I_{IN}	1.192	0.778	0.642	
R_{LOAD}	50.6	50.6	50.6	
V_{OUT}	12.09	12.02	8.39	
Duty Cycle	73.95%	59.11%	61.51%	
P_{IN}	3.754	3.824	2.073	0.000
P_{OUT}	2.889	2.855	1.391	#DIV/0!
Efficiency	76.96%	74.67%	67.11%	#DIV/0!

15.3 Data Sheets of Components Used

Dual/Quad, 4.5ns, Single Supply 3V/5V Comparators with Rail-to-Rail Outputs

FEATURES

- **UltraFast: 4.5ns at 20mV Overdrive**
  7ns at 5mV Overdrive
- **Low Power: 4mA per Comparator**
- Optimized for 3V and 5V Operation
- Pinout Optimized for High Speed Ease of Use
- Input Voltage Range Extends 100mV Below Negative Rail
- TTL/CMOS Compatible Rail-to-Rail Outputs
- Internal Hysteresis with Specified Limits
- Low Dynamic Current Drain; 15µA/(V-MHz), Dominated by Load In Most Circuits
- Tiny 3mm × 3mm × 0.75mm DFN Package (LT1720)

APPLICATIONS

- High Speed Differential Line Receiver
- Crystal Oscillator Circuits
- Window Comparators
- Threshold Detectors/Discriminators
- Pulse Stretchers
- Zero-Crossing Detectors
- High Speed Sampling Circuits

DESCRIPTION

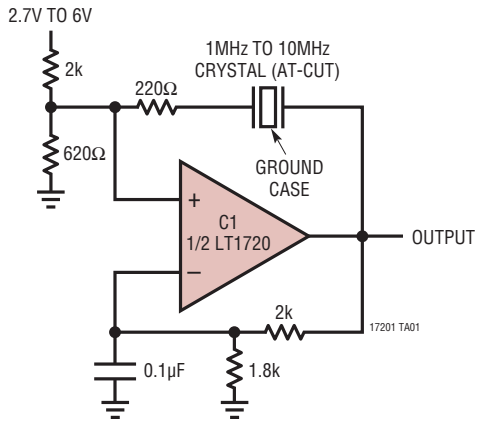
The LT®1720/LT1721 are UltraFast™ dual/quad comparators optimized for single supply operation, with a supply voltage range of 2.7V to 6V. The input voltage range extends from 100mV below ground to 1.2V below the supply voltage. Internal hysteresis makes the LT1720/LT1721 easy to use even with slow moving input signals. The rail-to-rail outputs directly interface to TTL and CMOS. Alternatively, the symmetric output drive can be harnessed for analog applications or for easy translation to other single supply logic levels.

The LT1720 is available in three 8-pin packages; three pins per comparator plus power and ground. In addition to SO and MSOP packages, a 3mm × 3mm low profile (0.8mm) dual fine pitch leadless package (DFN) is available for space limited applications. The LT1721 is available in the 16-pin SSOP and S packages.

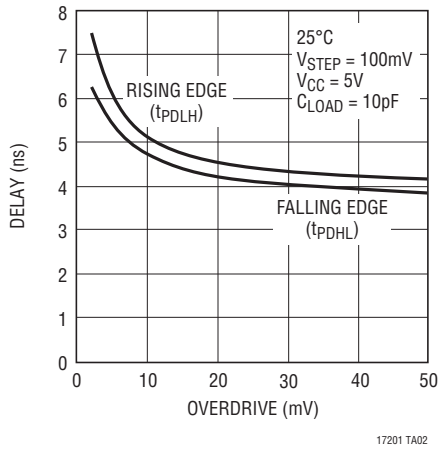
The pinouts of the LT1720/LT1721 minimize parasitic effects by placing the most sensitive inputs (inverting) away from the outputs, shielded by the power rails. The LT1720/LT1721 are ideal for systems where small size and low power are paramount.

TYPICAL APPLICATION

2.7V to 6V Crystal Oscillator with TTL/CMOS Output



Propagation Delay vs Overdrive

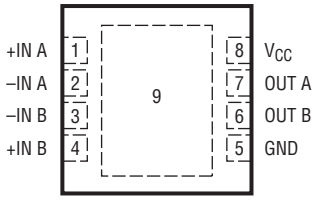


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC} to GND 7V
Input Current ..... ±10mA
Output Current (Continuous) ..... ±20mA
Junction Temperature ..... 150°C
(DD Package) ..... 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

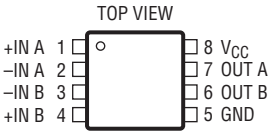
Storage Temperature Range ..... –65°C to 150°C
(DD Package) ..... –65°C to 125°C
Operating Temperature Range
C Grade ..... 0°C to 70°C
I Grade ..... –40°C to 85°C

PIN CONFIGURATION



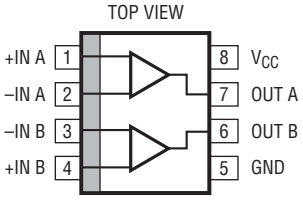
DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 160°C/W
UNDERSIDE METAL INTERNALLY CONNECTED TO GND



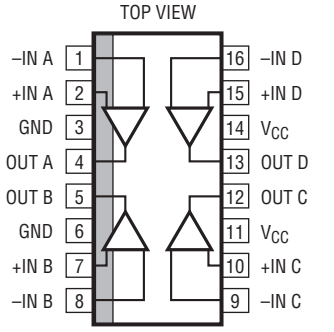
MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 230°C/W



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 200°C/W



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP

S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 135°C/W (GN)
T_{JMAX} = 150°C, θ_{JA} = 115°C/W (S)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1720CDD#PBF	LT1720CDD#TRPBF	LAAV	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT1720IDD#PBF	LT1720IDD#TRPBF	LAAV	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT1720CMS8#PBF	LT1720CMS8#TRPBF	LTDS	8-Lead Plastic MSOP	0°C to 70°C
LT1720IMS8#PBF	LT1720IMS8#TRPBF	LTACW	8-Lead Plastic MSOP	–40°C to 85°C
LT1720CS8#PBF	LT1720CS8#TRPBF	1720	8-Lead Plastic SO	0°C to 70°C
LT1720IS8#PBF	LT1720IS8#TRPBF	1720I	8-Lead Plastic SO	–40°C to 85°C
LT1721CGN#PBF	LT1721CGN#TRPBF	1721	16-Lead Narrow Plastic SSOP	0°C to 70°C
LT1721IGN#PBF	LT1721IGN#TRPBF	1721I	16-Lead Narrow Plastic SSOP	–40°C to 85°C
LT1721CS#PBF	LT1721CS#TRPBF	1721	16-Lead Plastic SO	0°C to 70°C
LT1721IS#PBF	LT1721IS#TRPBF	1721I	16-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{CM} = 1V, C_{OUT} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		6	V
I_{CC}	Supply Current (Per Comparator)	V_{CC} = 5V V_{CC} = 3V	● ●		4 3.5	7 6	mA mA
V_{CMR}	Common Mode Voltage Range	(Note 2)	●	–0.1		V_{CC} – 1.2	V
V_{TRIP}^+	Input Trip Points	(Note 3)	 ●	–2.0 –3.0		5.5 6.5	mV mV
V_{TRIP}^-	Input Trip Points	(Note 3)	 ●	–5.5 –6.5		2.0 3.0	mV mV
V_{OS}	Input Offset Voltage	(Note 3)	 ●		1.0	3.0 4.5	mV mV
V_{HYST}	Input Hysteresis Voltage	(Note 3)	●	2.0	3.5	7.0	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift		●		10		µV/°C
I_B	Input Bias Current		●	–6		0	µA
I_{OS}	Input Offset Current		●			0.6	µA
CMRR	Common Mode Rejection Ratio	(Note 4)	●	55	70		dB
PSRR	Power Supply Rejection Ratio	(Note 5)	●	65	80		dB
A_V	Voltage Gain	(Note 6)			∞		
V_{OH}	Output High Voltage	I_{SOURCE} = 4mA, V_{IN} = V_{TRIP}^+ + 10mV	●	V_{CC} – 0.4			V
V_{OL}	Output Low Voltage	I_{SINK} = 10mA, V_{IN} = V_{TRIP}^- – 10mV	●			0.4	V
t_{PD20}	Propagation Delay	$V_{OVERDRIVE}$ = 20mV (Note 7)	 ●		4.5	6.5 8.0	ns ns
t_{PD5}	Propagation Delay	$V_{OVERDRIVE}$ = 5mV (Notes 7, 8)	 ●		7	10 13	ns ns

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{CM} = 1V, C_{OUT} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Δt_{PD}	Differential Propagation Delay	(Note 9) Between Channels			0.3	1.0	ns
t_{SKEW}	Propagation Delay Skew	(Note 10) Between t_{PDLH}/t_{PDHL}			0.5	1.5	ns
t_r	Output Rise Time	10% to 90%			2.5		ns
t_f	Output Fall Time	90% to 10%			2.2		ns
t_{JITTER}	Output Timing Jitter	V_{IN} = 1.2V_{P-P} (6dBm), Z_{IN} = 50Ω t_{PDLH} V_{CM} = 2V, f = 20MHz t_{PDHL}			15 11		ps_{RMS} ps_{RMS}
f_{MAX}	Maximum Toggle Frequency	$V_{OVERDRIVE}$ = 50mV, V_{CC} = 3V $V_{OVERDRIVE}$ = 50mV, V_{CC} = 5V			70.0 62.5		MHz MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: If one input is within these common mode limits, the other input can go outside the common mode limits and the output will be valid.

Note 3: The LT1720/LT1721 comparators include internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of V_{TRIP}^+ and V_{TRIP}^-, while the hysteresis voltage is the difference of these two.

Note 4: The common mode rejection ratio is measured with V_{CC} = 5V and is defined as the change in offset voltage measured from V_{CM} = –0.1V to V_{CM} = 3.8V, divided by 3.9V.

Note 5: The power supply rejection ratio is measured with V_{CM} = 1V and is defined as the change in offset voltage measured from V_{CC} = 2.7V to V_{CC} = 6V, divided by 3.3V.

Note 6: Because of internal hysteresis, there is no small-signal region in which to measure gain. Proper operation of internal circuity is ensured by measuring V_{OH} and V_{OL} with only 10mV of overdrive.

Note 7: Propagation delay measurements made with 100mV steps. Overdrive is measured relative to $V_{TRIP}^{\pm}$.

Note 8: t_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1720/LT1721 are 100% tested with a 100mV step and 20mV overdrive. Correlation tests have shown that t_{PD} limits can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct.

Note 9: Differential propagation delay is defined as the larger of the two:

$\Delta t_{PDLH} = t_{PDLH(MAX)} - t_{PDLH(MIN)}$

$\Delta t_{PDHL} = t_{PDHL(MAX)} - t_{PDHL(MIN)}$

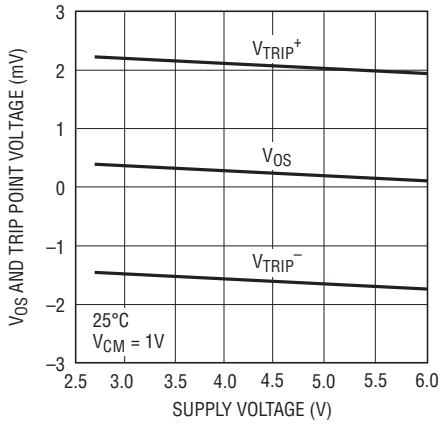
where (MAX) and (MIN) denote the maximum and minimum values of a given measurement across the different comparator channels.

Note 10: Propagation Delay Skew is defined as:

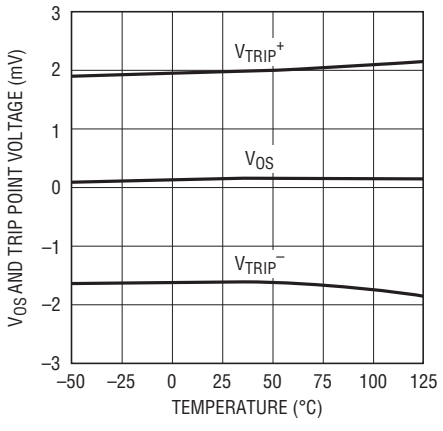
$t_{SKEW} = |t_{PDLH} - t_{PDHL}|$

TYPICAL PERFORMANCE CHARACTERISTICS

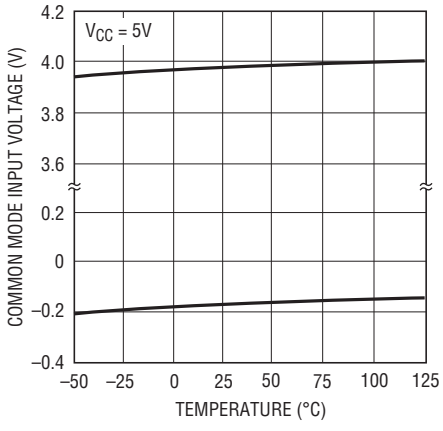
Input Offset and Trip Voltages vs Supply Voltage



Input Offset and Trip Voltages vs Temperature

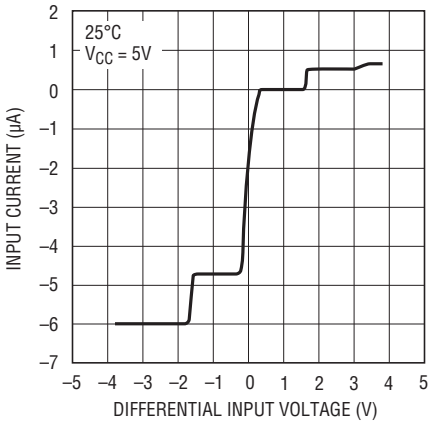


Input Common Mode Limits vs Temperature



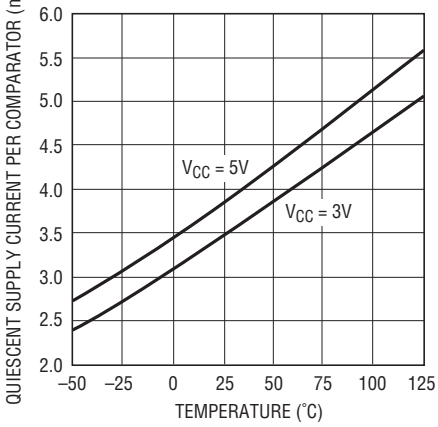
TYPICAL PERFORMANCE CHARACTERISTICS

Input Current vs Differential Input Voltage



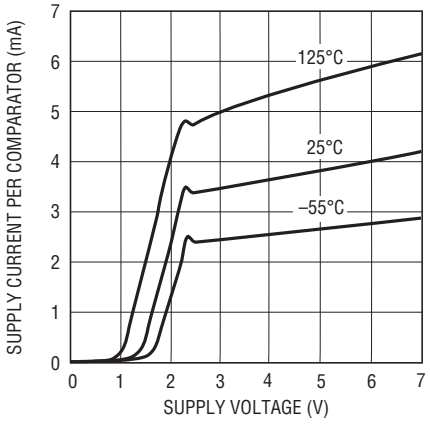
17201 G04

Quiescent Supply Current vs Temperature



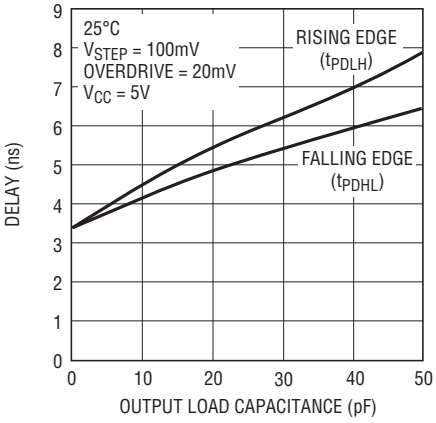
17201 G05

Quiescent Supply Current vs Supply Voltage



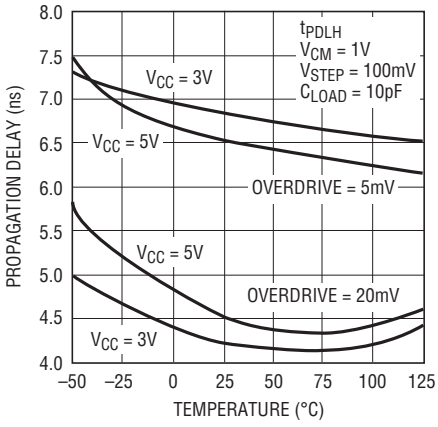
17201 G06

Propagation Delay vs Load Capacitance



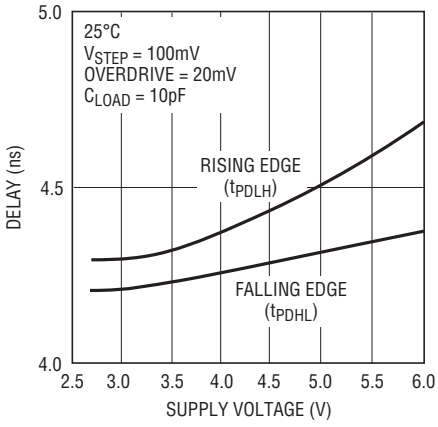
17201 G07

Propagation Delay vs Temperature



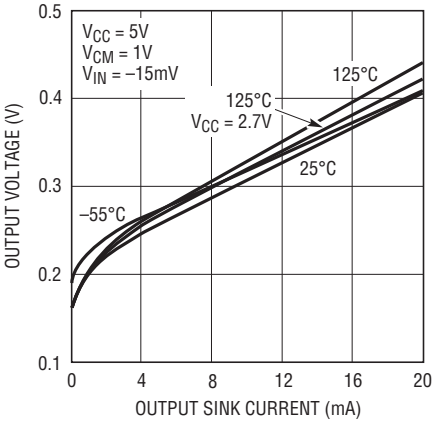
17201 G08

Propagation Delay vs Supply Voltage



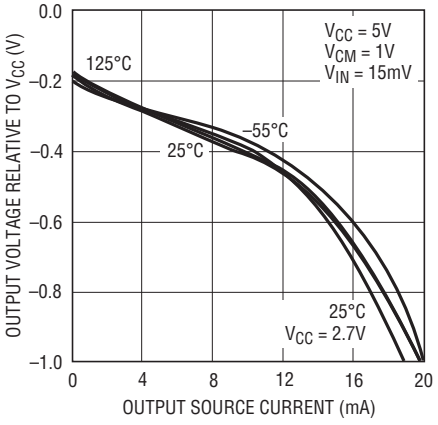
17201 G09

Output Low Voltage vs Load Current



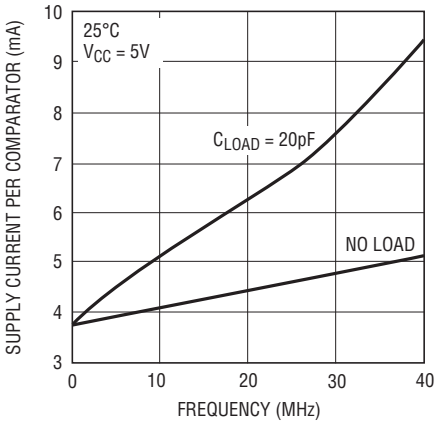
17201 G10

Output High Voltage vs Load Current



17201 G11

Supply Current vs Frequency



17201 G12

PIN FUNCTIONS

LT1720

+IN A (Pin 1): Noninverting Input of Comparator A.

–IN A (Pin 2): Inverting Input of Comparator A.

–IN B (Pin 3): Inverting Input of Comparator B.

+IN B (Pin 4): Noninverting Input of Comparator B.

GND (Pin 5): Ground.

OUT B (Pin 6): Output of Comparator B.

OUT A (Pin 7): Output of Comparator A.

V_{CC} (Pin 8): Positive Supply Voltage.

LT1721

–IN A (Pin 1): Inverting Input of Comparator A.

+IN A (Pin 2): Noninverting Input of Comparator A.

GND (Pins 3, 6): Ground.

OUT A (Pin 4): Output of Comparator A.

OUT B (Pin 5): Output of Comparator B.

+IN B (Pin 7): Noninverting Input of Comparator B.

–IN B (Pin 8): Inverting Input of Comparator B.

–IN C (Pin 9): Inverting Input of Comparator C.

+IN C (Pin 10): Noninverting Input of Comparator C.

V_{CC} (Pins 11, 14): Positive Supply Voltage.

OUT C (Pin 12): Output of Comparator C.

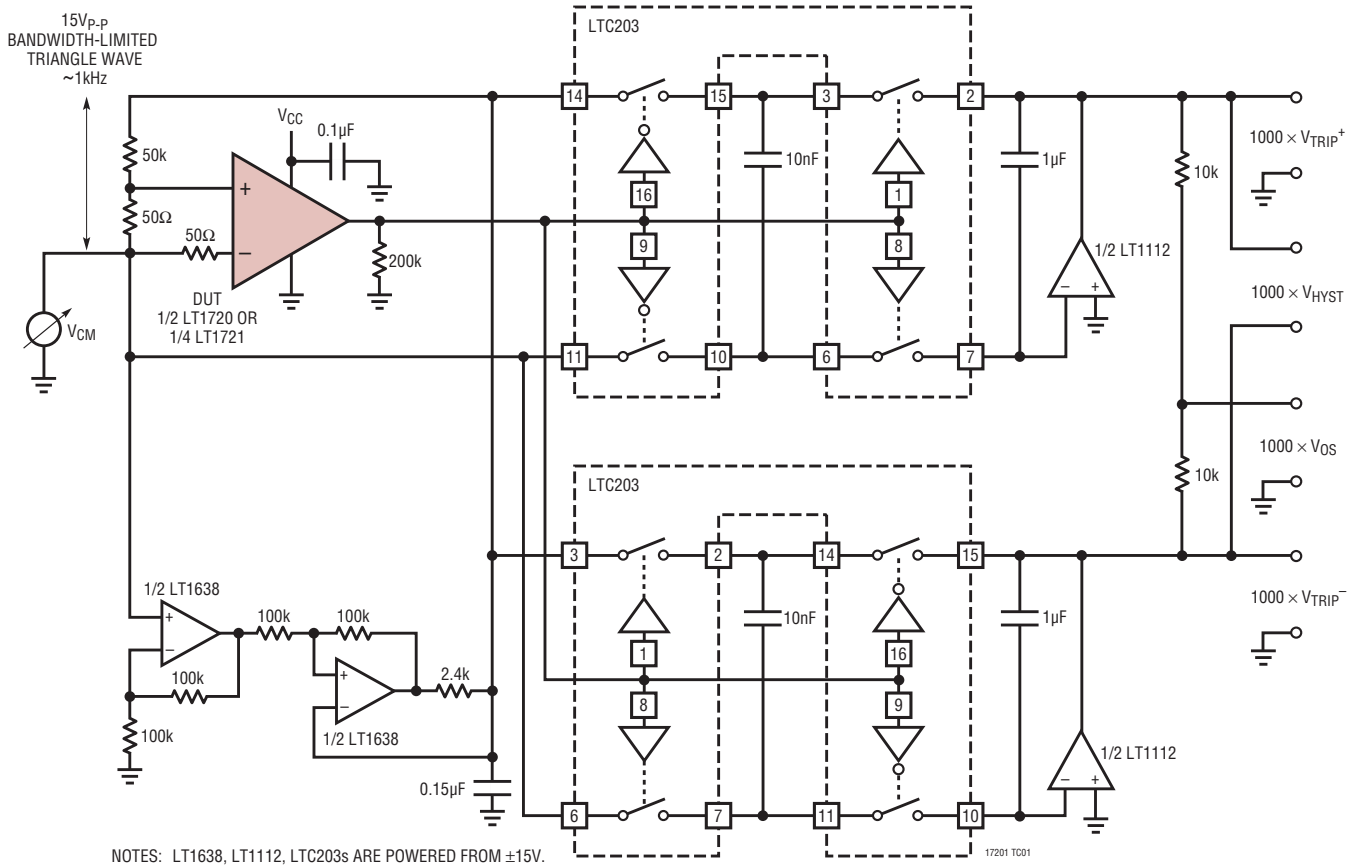
OUT D (Pin 13): Output of Comparator D.

+IN D (Pin 15): Noninverting Input of Comparator D.

–IN D (Pin 16): Inverting Input of Comparator D.

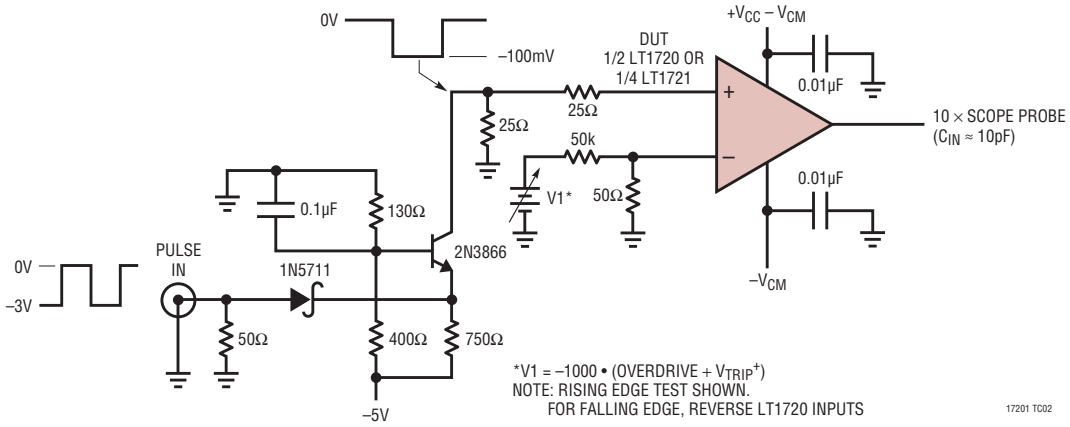
TEST CIRCUITS

$\pm V_{TRIP}$ Test Circuit



NOTES: LT1638, LT1112, LTC203s ARE POWERED FROM ±15V.
200kW PULL-DOWN PROTECTS LTC203 LOGIC INPUTS
WHEN DUT IS NOT POWERED

Response Time Test Circuit



*V1 = –1000 • (OVERDRIVE + V_{TRIP}^+)
NOTE: RISING EDGE TEST SHOWN.
FOR FALLING EDGE, REVERSE LT1720 INPUTS

APPLICATIONS INFORMATION

Input Voltage Considerations

The LT1720/LT1721 are specified for a common mode range of –100mV to 3.8V when used with a single 5V supply. In general the common mode range is 100mV below ground to 1.2V below V_{CC}. The criterion for this common mode limit is that the output still responds correctly to a small differential input signal. Also, if one input is within the common mode limit, the other input signal can go outside the common mode limits, up to the absolute maximum limits (a diode drop past either rail at 10mA input current) and the output will retain the correct polarity.

When either input signal falls below the negative common mode limit, the internal PN diode formed with the substrate can turn on, resulting in significant current flow through the die. An external Schottky clamp diode between the input and the negative rail can speed up recovery from negative overdrive by preventing the substrate diode from turning on.

When both input signals are below the negative common mode limit, phase reversal protection circuitry prevents false output inversion to at least –400mV common mode. However, the offset and hysteresis in this mode will increase dramatically, to as much as 15mV each. The input bias currents will also increase.

When both input signals are above the positive common mode limit, the input stage will become debiased and the output polarity will be random. However, the internal hysteresis will hold the output to a valid logic level, and because the biasing of each comparator is completely independent, there will be no impact on any other comparator. When at least one of the inputs returns to within the common mode limits, recovery from this state will take as long as 1µs.

The propagation delay does not increase significantly when driven with large differential voltages. However, with low levels of overdrive, an apparent increase may be seen with large source resistances due to an RC delay caused by the 2pF typical input capacitance.

Input Protection

The input stage is protected against damage from large differential signals, up to and beyond a differential voltage equal to the supply voltage, limited only by the absolute maximum currents noted. External input protection circuitry is only needed if currents would otherwise exceed these absolute maximums. The internal catch diodes can conduct current up to these rated maximums without latchup, even when the supply voltage is at the absolute maximum rating.

The LT1720/LT1721 input stage has general purpose internal ESD protection for the human body model. For use as a line receiver, additional external protection may be required. As with most integrated circuits, the level of immunity to ESD is much greater when residing on a printed circuit board where the power supply decoupling capacitance will limit the voltage rise caused by an ESD pulse.

Unused Inputs

The inputs of any unused compartor should be tied off in a way that defines the output logic state. The easiest way to do this is to tie IN^+ to V_{CC} and IN^- to GND.

Input Bias Current

Input bias current is measured with both inputs held at 1V. As with any PNP differential input stage, the LT1720/LT1721 bias current flows out of the device. With a differential input voltage of even just 100mV or so, there will be zero bias current into the higher of the two inputs, while the current flowing out of the lower input will be twice the measured bias current. With more than two diode drops of differential input voltage, the LT1720/LT1721's input protection circuitry activates, and current out of the lower input will increase an additional 30% and there will be a small bias current into the higher of the two input pins, of 4µA or less. See the Typical Performance curve "Input Current vs Differential Input Voltage."

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High Speed Design Considerations

Application of high speed comparators is often plagued by oscillations. The LT1720/LT1721 have 4mV of internal hysteresis, which will prevent oscillations as long as parasitic output to input feedback is kept below 4mV. However, with the 2V/ns slew rate of the LT1720/LT1721 outputs, a 4mV step can be created at a 100Ω input source with only 0.02pF of output to input coupling. The pinouts of the LT1720/LT1721 have been arranged to minimize problems by placing the most sensitive inputs (inverting) away from the outputs, shielded by the power rails. The input and output traces of the circuit board should also be separated, and the requisite level of isolation is readily achieved if a topside ground plane runs between the outputs and the inputs. For multilayer boards where the ground plane is internal, a topside ground or supply trace should be run between the inputs and outputs, as illustrated in Figure 1.

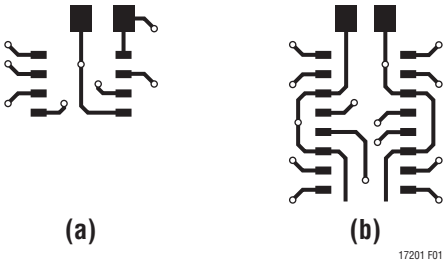

Figure 1. Typical Topside Metal for Multilayer PCB Layouts

Figure 1a shows a typical topside layout of the LT1720 on such a multilayer board. Shown is the topside metal etch including traces, pin escape vias, and the land pads for an SO-8 LT1720 and its adjacent X7R 10nF bypass capacitor in a 1206 case.

The ground trace from Pin 5 runs under the device up to the bypass capacitor, shielding the inputs from the outputs. Note the use of a common via for the LT1720 and the bypass capacitor, which minimizes interference from high frequency energy running around the ground plane or power distribution traces.

Figure 1b shows a typical topside layout of the LT1721 on a multilayer board. In this case, the power and ground traces have been extended to the bottom of the device solely to act as high frequency shields between input and output traces.

Although both V_{CC} pins are electrically shorted internal to the LT1721, they must be shorted together externally as well in order for both to function as shields. The same is true for the two GND pins.

The supply bypass should include an adjacent 10nF ceramic capacitor and a 2.2µF tantalum capacitor no farther than 5cm away; use more capacitance if driving more than 4mA loads. To prevent oscillations, it is helpful to balance the impedance at the inverting and noninverting inputs; source impedances should be kept low, preferably 1kΩ or less.

The outputs of the LT1720/LT1721 are capable of very high slew rates. To prevent overshoot, ringing and other problems with transmission line effects, keep the output traces shorter than 10cm, or be sure to terminate the lines to maintain signal integrity. The LT1720/LT1721 can drive DC terminations of 250Ω or more, but lower characteristic impedance traces can be driven with series termination or AC termination topologies.

Hysteresis

The LT1720/LT1721 include internal hysteresis, which makes them easier to use than many other comparable speed comparators.

The input-output transfer characteristic is illustrated in Figure 2 showing the definitions of V_{OS} and V_{HYST} based upon the two measurable trip points. The hysteresis band makes the LT1720/LT1721 well behaved, even with slowly moving inputs.

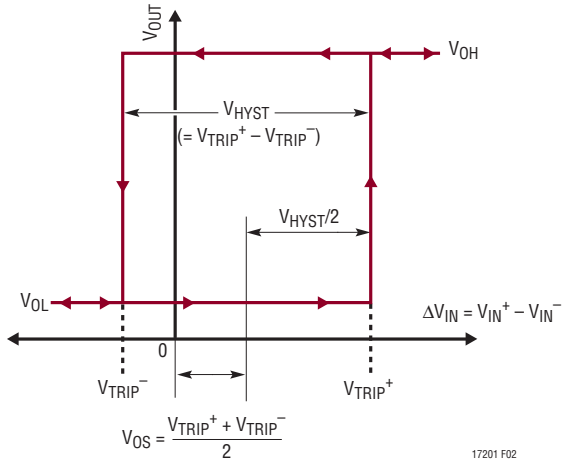

Figure 2. Hysteresis I/O Characteristics

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The exact amount of hysteresis will vary from part to part as indicated in the specifications table. The hysteresis level will also vary slightly with changes in supply voltage and common mode voltage. A key advantage of the LT1720/LT1721 is the significant reduction in these effects, which is important whenever an LT1720/LT1721 is used to detect a threshold crossing in one direction only. In such a case, the relevant trip point will be all that matters, and a stable offset voltage with an unpredictable level of hysteresis, as seen in competing comparators, is of little value. The LT1720/LT1721 are many times better than prior comparators in these regards. In fact, the CMRR and PSRR tests are performed by checking for changes in either trip point to the limits indicated in the specifications table. Because the offset voltage is the average of the trip points, the CMRR and PSRR of the offset voltage is therefore guaranteed to be at least as good as those limits. This more stringent test also puts a limit on the common mode and power supply dependence of the hysteresis voltage.

Additional hysteresis may be added externally. The rail-to-rail outputs of the LT1720/LT1721 make this more predictable than with TTL output comparators due to the LT1720/LT1721's small variability of V_{OH} (output high voltage).

To add additional hysteresis, set up positive feedback by adding additional external resistor R3 as shown in Figure 3. Resistor R3 adds a portion of the output to the threshold set by the resistor string. The LT1720/LT1721 pulls the outputs to the supply rail and ground to within 200mV of the rails with light loads, and to within 400mV with heavy loads. For the load of most circuits, a good model for the voltage on the right side of R3 is 300mV or V_{CC} – 300mV, for a total voltage swing of (V_{CC} – 300mV) – 300mV = V_{CC} – 600mV.

With this in mind, calculation of the resistor values needed is a two-step process. First, calculate the value of R3 based on the additional hysteresis desired, the output voltage swing, and the impedance of the primary bias string:

$$R3 = (R1 \parallel R2)(V_{CC} - 0.6V)/(\text{additional hysteresis})$$

Additional hysteresis is the desired overall hysteresis less the internal 3.5mV hysteresis.

The second step is to recalculate R2 to set the same average threshold as before. The average threshold before was set at $V_{TH} = (V_{REF})(R1)/(R1 + R2)$. The new R2 is calculated based on the average output voltage ($V_{CC}/2$) and the simplified circuit model in Figure 4. To assure that the comparator's noninverting input is, on average, the same V_{TH} as before:

$$R2' = (V_{REF} - V_{TH})/(V_{TH}/R1 + (V_{TH} - V_{CC}/2)/R3)$$

For additional hysteresis of 10mV or less, it is not uncommon for R2′ to be the same as R2 within 1% resistor tolerances.

This method will work for additional hysteresis of up to a few hundred millivolts. Beyond that, the impedance of R3 is low enough to effect the bias string, and adjustment of R1 may also be required. Note that the currents through the R1/R2 bias string should be many times the input currents of the LT1720/LT1721. For 5% accuracy, the current must be at least 120μA(6μA $I_B \div 0.05$); more for higher accuracy.

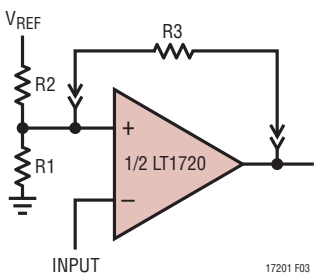

Figure 3. Additional External Hysteresis

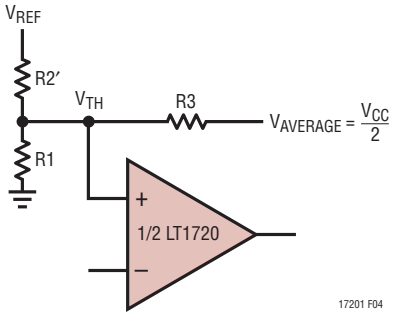

Figure 4. Model for Additional Hysteresis Calculations

APPLICATIONS INFORMATION

Interfacing the LT1720/LT1721 to ECL

The LT1720/LT1721 comparators can be used in high speed applications where Emitter-Coupled Logic (ECL) is deployed. To interface the outputs of the LT1720/LT1721 to ECL logic inputs, standard TTL/CMOS to ECL level translators such as the 10H124, 10H424 and 100124 can be used. These components come at a cost of a few nanoseconds additional delay as well as supply currents of 50mA or more, and are only available in quads. A faster, simpler and lower power translator can be constructed with resistors as shown in Figure 5.

Figure 5a shows the standard TTL to Positive ECL (PECL) resistive level translator. This translator cannot be used for the LT1720/LT1721, or with CMOS logic, because it depends on the 820Ω resistor to limit the output swing (V_{OH}) of the all-NPN TTL gate with its so-called totem-pole output. The LT1720/LT1721 are fabricated in a complementary bipolar process and their output stage has a PNP driver that pulls the output nearly all the way to the supply rail, even when sourcing 10mA.

Figure 5b shows a three resistor level translator for interfacing the LT1720/LT1721 to ECL running off the same supply rail. No pull-down on the output of the LT1720/LT1721 is needed, but pull-down R3 limits the V_{IH} seen by the PECL gate. This is needed because ECL inputs have both a minimum and maximum V_{IH} specification for proper operation. Resistor values are given for both ECL interface types; in both cases it is assumed that the LT1720/LT1721 operates from the same supply rail.

Figure 5c shows the case of translating to PECL from an LT1720/LT1721 powered by a 3V supply rail. Again, resistor values are given for both ECL interface types. This time four resistors are needed, although with 10KH/E, R3 is not needed. In that case, the circuit resembles the standard TTL translator of Figure 5a, but the function of the new resistor, R4, is much different. R4 loads the LT1720/LT1721 output when high so that the current flowing through R1 doesn't forward bias the LT1720/LT1721's internal ESD clamp diode. Although this diode can handle 20mA without damage, normal operation and performance of the output stage can be impaired above 100µA of forward current. R4 prevents this with the minimum additional power dissipation.

Finally, Figure 5d shows the case of driving standard, negative-rail, ECL with the LT1720/LT1721. Resistor values are given for both ECL interface types and for both a 5V and 3V LT1720/LT1721 supply rail. Again, a fourth resistor, R4 is needed to prevent the low state current from flowing out of the LT1720/LT1721, turning on the internal ESD/substrate diodes. Not only can the output stage functionality and speed suffer, but in this case the substrate is common to all the comparators in the LT1720/LT1721, so operation of the other comparator(s) in the same package could also be affected. Resistor R4 again prevents this with the minimum additional power dissipation.

For all the dividers shown, the output impedance is about 110Ω. This makes these fast, less than a nanosecond, with most layouts. Avoid the temptation to use speedup capacitors. Not only can they foul up the operation of the ECL gate because of overshoots, they can damage the ECL inputs, particularly during power-up of separate supply configurations.

The level translator designs assume one gate load. Multiple gates can have significant I_{IH} loading, and the transmission line routing and termination issues also make this case difficult.

ECL, and particularly PECL, is valuable technology for high speed system design, but it must be used with care. With less than a volt of swing, the noise margins need to be evaluated carefully. Note that there is some degradation of noise margin due to the ±5% resistor selections shown. With 10KH/E, there is no temperature compensation of the logic levels, whereas the LT1720/LT1721 and the circuits shown give levels that are stable with temperature. This will degrade the noise margin over temperature. In some configurations it is possible to add compensation with diode or transistor junctions in series with the resistors of these networks.

For more information on ECL design, refer to the ECLiPS data book (DL140), the 10KH system design handbook (HB205) and PECL design (AN1406), all from ON Semiconductor (www.onsemi.com).

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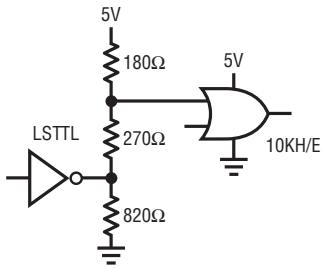
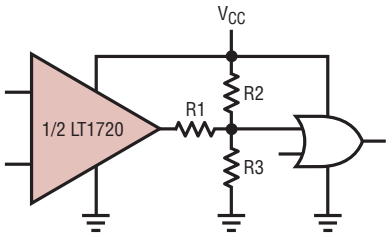


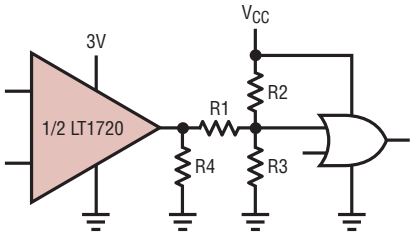
DO NOT USE FOR LT1720/LT1721
LEVEL TRANSLATION. SEE TEXT

(a) STANDARD TTL TO PECL TRANSLATOR



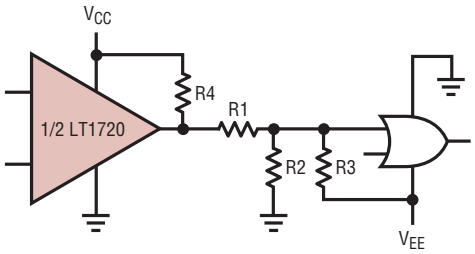
	V_{CC}	R1	R2	R3
10KH/E	5V OR 5.2V	510Ω	180Ω	750Ω
100K/E	4.5V	620Ω	180Ω	510Ω

(b) LT1720/LT1721 OUTPUT TO PECL TRANSLATOR



	V_{CC}	R1	R2	R3	R4
10KH/E	5V OR 5.2V	300Ω	180Ω	OMIT	560Ω
100K/E	4.5V	330Ω	180Ω	1500Ω	1000Ω

(c) 3V LT1720/LT1721 OUTPUT TO PECL TRANSLATOR



ECL FAMILY	V_{EE}	V_{CC}	R1	R2	R3	R4
10KH/E	–5.2V	5V	560Ω	270Ω	330Ω	1200Ω
		3V	270Ω	510Ω	300Ω	330Ω
100K/E	–4.5V	5V	680Ω	270Ω	300Ω	1500Ω
		3V	330Ω	390Ω	270Ω	430Ω

17201 F05

(d) LT1720/LT1721 OUTPUT TO STANDARD ECL TRANSLATOR

Figure 5

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Circuit Description

The block diagram of one comparator in the LT1720/LT1721 is shown in Figure 6. There are differential inputs (+IN/–IN), an output (OUT), a single positive supply (V_{CC}) and ground (GND). All comparators are completely independent, sharing only the power and ground pins. The circuit topology consists of a differential input stage, a gain stage with hysteresis and a complementary common-emitter output stage. All of the internal signal paths utilize low voltage swings for high speed at low power.

The input stage topology maximizes the input dynamic range available without requiring the power, complexity and die area of two complete input stages such as are found in rail-to-rail input comparators. With a 2.7V supply, the LT1720/LT1721 still have a respectable 1.6V of input common mode range. The differential input voltage range is rail-to-rail, without the large input currents found in competing devices. The input stage also features phase reversal protection to prevent false outputs when the inputs are driven below the –100mV common mode voltage limit.

The internal hysteresis is implemented by positive, nonlinear feedback around a second gain stage. Until this point, the signal path has been entirely differential. The signal path is then split into two drive signals for the upper and lower output transistors. The output transistors are connected common emitter for rail-to-rail output operation. The Schottky clamps limit the output voltages at about 300mV from the rail, not quite the 50mV or 15mV of Linear Technology's rail-to-rail amplifiers and other products. But the output of a comparator is digital, and this output stage can drive TTL or CMOS directly. It can also drive ECL, as described earlier, or analog loads as demonstrated in the applications to follow.

The bias conditions and signal swings in the output stages are designed to turn their respective output transistors off faster than on. This nearly eliminates the surge of current from V_{CC} to ground that occurs at transitions, keeping the power consumption low even with high output-toggle frequencies.

The low surge current is what keeps the power consumption low at high output-toggle frequencies. The frequency dependence of the supply current is shown in the Typical Performance Characteristics. Just 20pF of capacitive load on the output more than triples the frequency dependent rise. The slope of the no-load curve is just 32µA/MHz. With a 5V supply, this current is the equivalent of charging and discharging just 6.5pF. The slope of the 20pF load curve is 133µA/MHz, an addition of 101µA/MHz, or 20µA/MHz-V, units that are equivalent to picoFarads.

The LT1720/LT1721 dynamic current can be estimated by adding the external capacitive loading to an internal equivalent capacitance of 5pF to 15pF, multiplied by the toggle frequency and the supply voltage. Because the capacitance of routing traces can easily approach these values, the dynamic current is dominated by the load in most circuits.

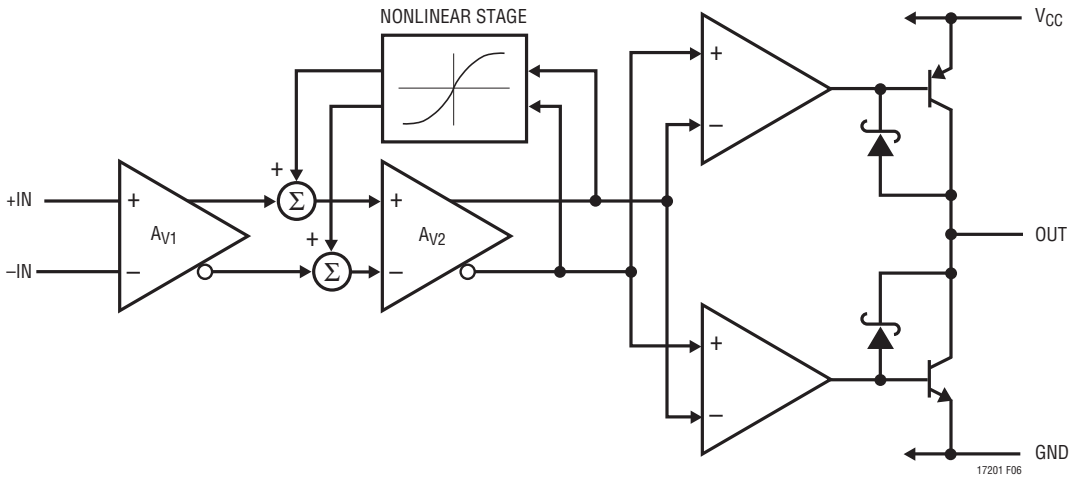

Figure 6. LT1720/LT1721 Block Diagram

APPLICATIONS INFORMATION

Speed Limits

The LT1720/LT1721 comparators are intended for high speed applications, where it is important to understand a few limitations. These limitations can roughly be divided into three categories: input speed limits, output speed limits, and internal speed limits.

There are no significant input speed limits except the shunt capacitance of the input nodes. If the 2pF typical input nodes are driven, the LT1720/LT1721 will respond.

The output speed is constrained by two mechanisms, the first of which is the slew currents available from the output transistors. To maintain low power quiescent operation, the LT1720/LT1721 output transistors are sized to deliver 25mA to 45mA typical slew currents. This is sufficient to drive small capacitive loads and logic gate inputs at extremely high speeds. But the slew rate will slow dramatically with heavy capacitive loads. Because the propagation delay (t_{PD}) definition ends at the time the output voltage is halfway between the supplies, the fixed slew current actually makes the LT1720/LT1721 faster at 3V than 5V with 20mV of input overdrive.

Another manifestation of this output speed limit is skew, the difference between t_{PDLH} and t_{PDHL}. The slew currents of the LT1720/LT1721 vary with the process variations of the PNP and NPN transistors, for rising edges and falling edges respectively. The typical 0.5ns skew can have either polarity, rising edge or falling edge faster. Again, the skew will increase dramatically with heavy capacitive loads.

The skews of comparators in a single package are correlated, but not identical. Besides some random variability, there is a small (100ps to 200ps) systematic skew due to physical parasitics of the packages. For the LT1720 SO-8, comparator A, whose output is adjacent to the V_{CC} pin, will have a relatively faster rising edge than comparator B. Likewise, comparator B, by virtue of an output adjacent to the ground pin will have a relatively faster falling edge. Similar dependencies occur in the LT1721 S16, while the systemic skews in the smaller MSOP and SSOP packages are half again as small. Of course, if the capacitive loads on the two comparators of a single package are not identical, the differential timing will degrade further.

The second output speed limit is the clamp turnaround. The LT1720/LT1721 output is optimized for fast initial response, with some loss of turnaround speed, limiting the toggle frequency. The output transistors are idled in a low power state once V_{OH} or V_{OL} is reached by detecting the Schottky clamp action. It is only when the output has slewed from the old voltage to the new voltage, and the clamp circuitry has settled, that the idle state is reached and the output is fully ready to transition again. This clamp turnaround time is typically 8ns for each direction, resulting in a maximum toggle frequency of 62.5MHz, or a 125MB data rate. With higher frequencies, dropout and runt pulses can occur. Increases in capacitive load will increase the time needed for slewing due to the limited slew currents and the maximum toggle frequency will decrease further. For higher toggle frequency applications, refer to the LT1715, whose output stage can toggle at 150MHz typical.

The internal speed limits manifest themselves as dispersion. All comparators have some degree of dispersion, defined as a change in propagation delay versus input overdrive. The propagation delay of the LT1720/LT1721 will vary with overdrive, from a typical of 4.5ns at 20mV overdrive to 7ns at 5mV overdrive (typical). The LT1720/LT1721's primary source of dispersion is the hysteresis stage. As a change of polarity arrives at the gain stage, the positive feedback of the hysteresis stage subtracts from the overdrive available. Only when enough time has elapsed for a signal to propagate forward through the gain stage, backwards through the hysteresis stage and forward through the gain stage again, will the output stage receive the same level of overdrive that it would have received in the absence of hysteresis.

With 5mV of overdrive, the LT1720/LT1721 are faster with a 5V supply than with a 3V supply, the opposite of what is true with 20mV overdrive. This is due to the internal speed limit, because the gain stage is faster at 5V than 3V due primarily to the reduced junction capacitances with higher reverse voltage bias.

In many applications, as shown in the following examples, there is plenty of input overdrive. Even in applications providing low levels of overdrive, the LT1720/LT1721 are fast enough that the absolute dispersion of 2.5ns (= 7 – 4.5) is often small enough to ignore.

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The gain and hysteresis stage of the LT1720/LT1721 is simple, short and high speed to help prevent parasitic oscillations while adding minimum dispersion. This internal "self-latch" can be usefully exploited in many applications because it occurs early in the signal chain, in a low power, fully differential stage. It is therefore highly immune to disturbances from other parts of the circuit, either in the same comparator, on the supply lines, or from the other comparator(s) in the same package. Once a high speed signal trips the hysteresis, the output will respond, after a fixed propagation delay, without regard to these external influences that can cause trouble in nonhysteretic comparators.

$\pm V_{TRIP}$ Test Circuit

The input trip points are tested using the circuit shown in the Test Circuits section that precedes this Applications Information section. The test circuit uses a 1kHz triangle wave to repeatedly trip the comparator being tested. The LT1720/LT1721 output is used to trigger switched capacitor sampling of the triangle wave, with a sampler for each direction. Because the triangle wave is attenuated 1000:1 and fed to the LT1720/LT1721's differential input, the sampled voltages are therefore 1000 times the input trip voltages. The hysteresis and offset are computed from the trip points as shown.

Crystal Oscillators

A simple crystal oscillator using one comparator of an LT1720/LT1721 is shown on the first page of this data sheet. The 2k-620Ω resistor pair set a bias point at the comparator's noninverting input. The 2k-1.8k-0.1µF path sets the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. Although the LT1720/LT1721 will give the correct logic output when one input is outside the common mode range, additional delays may occur when it is so operated, opening the possibility of spurious operating modes. Therefore, the DC bias voltages at the inputs are set near the center of the LT1720/LT1721's common mode range and the 220Ω resistor attenuates the feedback to the noninverting input. The circuit will operate with any AT-cut crystal from 1MHz to 10MHz over a 2.7V to 6V supply range. As the power is applied, the circuit remains off until the LT1720/LT1721 bias circuits activate, at a typical V_{CC} of 2V to 2.2V (25°C), at which point the desired frequency output is generated.

The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and, to a lesser extent, by comparator offsets and timings. If a 50% duty cycle is required, the circuit of Figure 7 creates a pair of complementary outputs with a forced 50% duty cycle. Crystals are narrow-band elements, so the feedback to the noninverting input is a filtered analog version of the square wave output. Changing the noninverting reference level can therefore vary the duty cycle. C1 operates as in the previous example, whereas C2 creates a complementary output by comparing the same two nodes with the opposite input polarity. A1 compares band-limited versions of the outputs and biases C1's negative input. C1's only degree of freedom to respond is variation of pulse width; hence the outputs are forced to 50% duty cycle. Again, the circuit operates from 2.7V to 6V, and the skew between the edges of the two outputs are shown in Figure 8. There is a slight duty cycle dependence on comparator loading, so equal capacitive and resistive loading should be used in critical applications. This circuit works well because of the two matched delays and rail-to-rail style outputs of the LT1720.

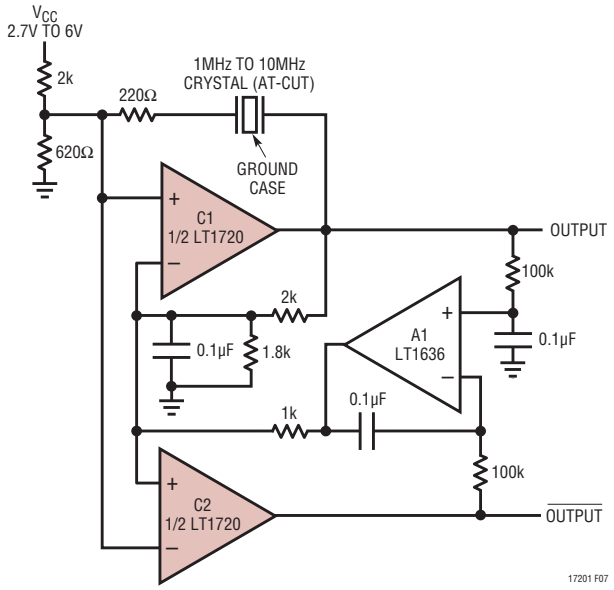

Figure 7. Crystal Oscillator with Complementary Outputs and 50% Duty Cycle

APPLICATIONS INFORMATION

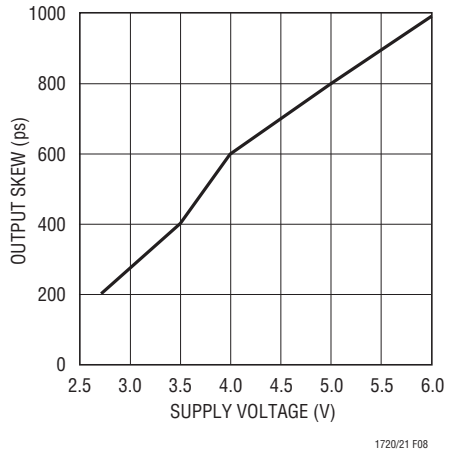

Figure 8. Timing Skew of Figure 7's Circuit

The circuit in Figure 9 shows a crystal oscillator circuit that generates two nonoverlapping clocks by making full use of the two independent comparators of the LT1720. C1 oscillates as before, but with a lower reference level, C2's output will toggle at different times. The resistors set the degree of separation between the output's high pulses. With the values shown, each output has a 44% high and 56% low duty cycle, sufficient to allow 2ns between the high pulses. Figure 10 shows the two outputs.

The optional A1 feedback network shown can be used to force identical output duty cycles. The steady state duty cycles of both outputs will be 44%. Note, though, that the addition of this network only adjusts the percentage of time each output is high to be the same, which can be important in switching circuits requiring identical settling times. It cannot adjust the relative phases between the two outputs to be exactly 180° apart, because the signal at the input node driven by the crystal is not a pure sinusoid.

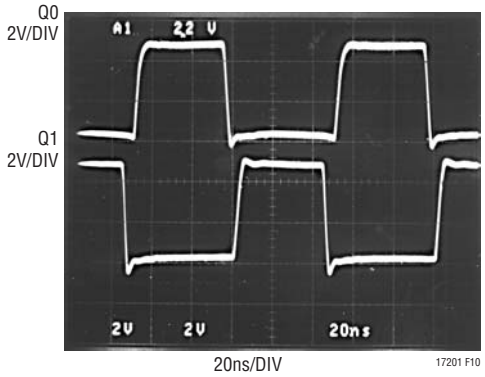

Figure 10. Nonoverlapping Outputs of Figure 9's Circuit

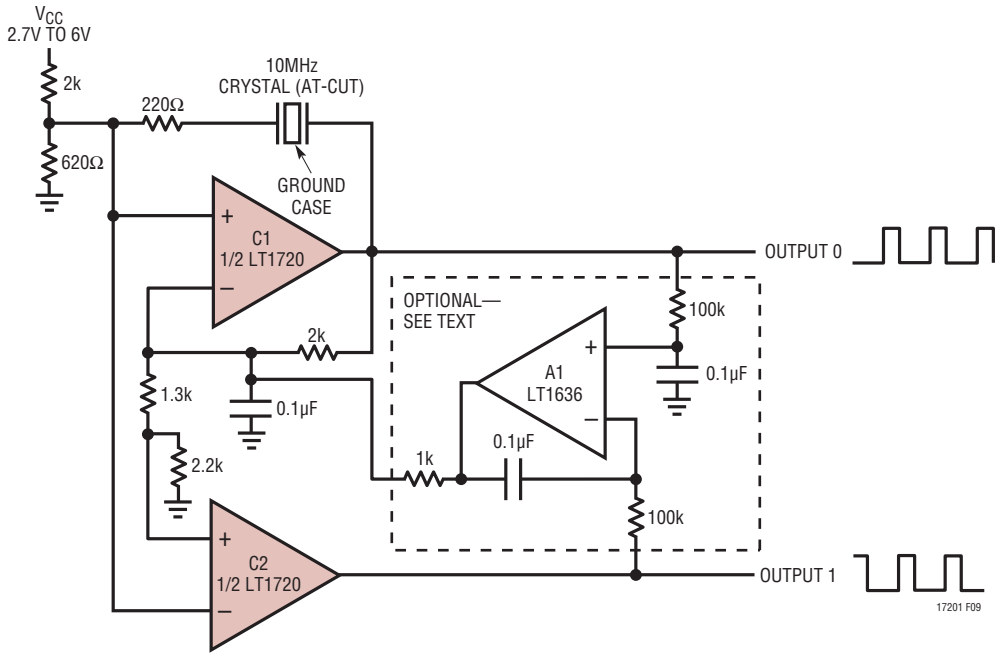

Figure 9. Crystal-Based Nonoverlapping 10MHz Clock Generator

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Timing Skews

For a number of reasons, the LT1720/LT1721's superior timing specifications make them an excellent choice for applications requiring accurate differential timing skew. The comparators in a single package are inherently well matched, with just 300ps Δt_{PD} typical. Monolithic construction keeps the delays well matched vs supply voltage and temperature. Crosstalk between the comparators, usually a disadvantage in monolithic duals and quads, has minimal effect on the LT1720/LT1721 timing due to the internal hysteresis, as described in the Speed Limits section.

The circuits of Figure 11 show basic building blocks for differential timing skews. The 2.5k resistance interacts with the 2pF typical input capacitance to create at least ±4ns delay, controlled by the potentiometer setting. A differential and a single-ended version are shown. In the differential configuration, the output edges can be smoothly scrolled through $\Delta t = 0$ with negligible interaction.

3ns Delay Detector

It is often necessary to measure comparative timing of pulse edges in order to determine the true synchronicity of clock and control signals, whether in digital circuitry or in high speed instrumentation. The circuit in Figure 12 is a delay detector which will output a pulse when signals X and Y are out of sync (specifically, when X is high and Y is low). Note that the addition of an identical circuit to detect the opposite situation (X low and Y high) allows for full skew detection.

Comparators U1A and U1B clean up the incoming signals and render the circuit less sensitive to input levels and slew rates. The resistive divider network provides level shifting for the downstream comparator's common mode input range, as well as offset to keep the output low except during a decisive event. When the upstream comparator's outputs can overcome the resistively generated offset (and hysteresis), comparator U1C performs a Boolean "X*_Y" function and produces an output pulse (see Figure 13). The circuit will give full output response with input delays down to 3ns and partial output response with input delays down to 1.8ns. Capacitor C1 helps ensure that an imbalance of parasitic capacitances in the layout will not cause common mode excursions to result in differential mode signal and false outputs.[1]

[1] Make sure the input levels at X and Y are not too close to the 0.5V threshold set by the R8–R9 divider. If you are still getting false outputs, try increasing C1 to 10pF or more. You can also look for the problem in the impedance balance (R5 || R6 = R7) at the inputs of U1C. Increasing the offset by lowering R5 will help reject false outputs, but R7 should also be lowered to maintain impedance balance. For ease of design and parasitic matching, R7 can be replaced by two parallel resistors equal to R5 and R6.

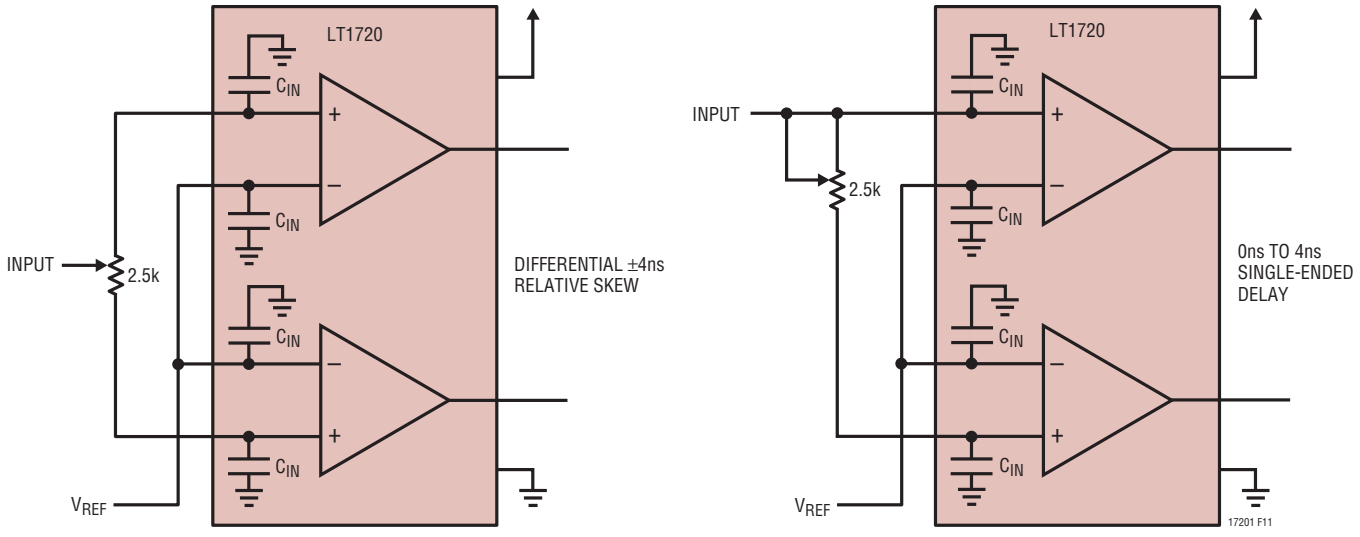


Figure 11. Building Blocks for Timing Skew Generation with the LT1720

APPLICATIONS INFORMATION

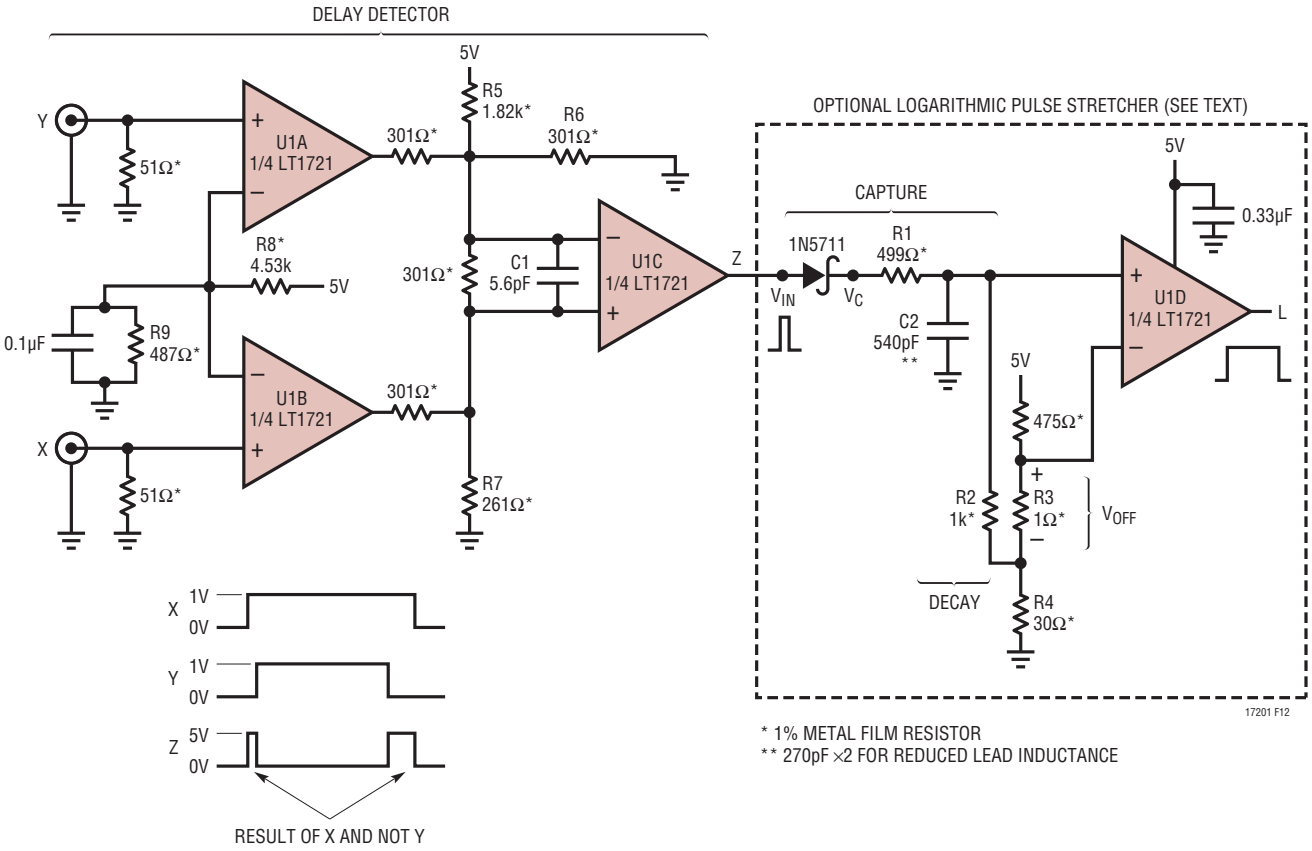


Figure 12. 3ns Delay Detector with Logarithmic Pulse Stretcher

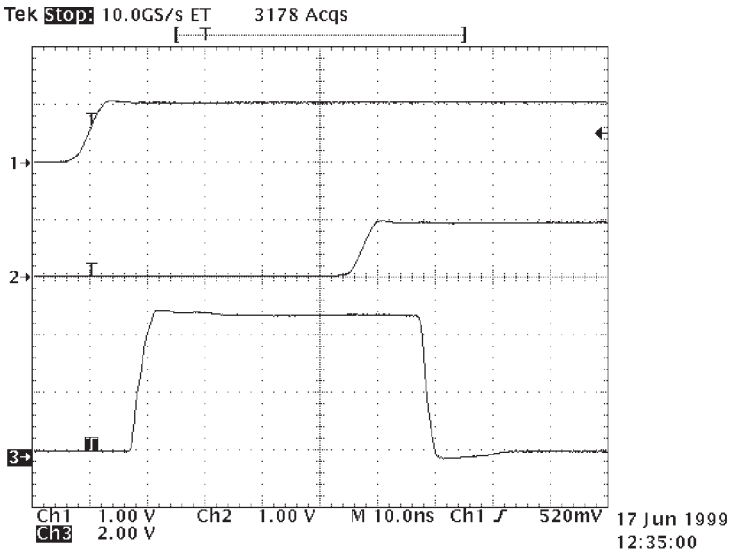


Figure 13. Output Pulse Due to Delay of Y Input Pulse

APPLICATIONS INFORMATION

Optional Logarithmic Pulse Stretcher

The fourth comparator of the quad LT1721 can be put to work as a logarithmic pulse stretcher. This simple circuit can help tremendously if you don't have a fast enough oscilloscope (or control circuit) to easily capture 3ns pulse widths (or faster). When an input pulse occurs, C2 is charged up with a 180ns capture[2] time constant. The hysteresis and 10mV offset across R3 are overcome within the first nanosecond[3], switching the comparator output high. When the input pulse subsides, C2 discharges with a 540ns time constant, keeping the comparator on until the decay overrides the 10mV offset across R3 minus hysteresis. Because of this exponential decay, the output pulse width will be proportional to the logarithm of the input pulse width. It is important to bypass the circuit's V_{CC} well to avoid coupling into the resistive divider. R4 keeps the quiescent input voltage in a range where forward leakage of the diode due to the 0.4V V_{OL} of the driving comparator is not a problem.

Neglecting some effects[4], the output pulse is related to the input pulse as:

$$t_{OUT} = \tau_2 \bullet \ell n \{V_{CH} \bullet [1 - \exp(-t_P/\tau_1)]/(V_{OFF} - V_H/2)\} - \tau_1 \bullet \ell n [V_{CH}/(V_{CH} - V_{OFF} - V_H/2)] + t_P \quad (1)$$

where

t_P = input pulse width

t_{OUT} = output pulse width

$\tau_1 = R1 \,||\, R2 \bullet C2$	the capture time constant
$\tau_2 = R2 \bullet C2$	the decay time constant
$V_{OFF} = 10mV$	the voltage drop across R1
$V_H = 3.5mV$	LT1721 hysteresis
$V_C = V_{IN} - V_{FDIODE}$	the input pulse voltage after the diode drop
$V_{CH} = V_C \bullet R2/(R1 + R2)$	the effective source voltage for the charge

For simplicity, with $t_P < \tau_1$, and neglecting the very slight delay in turn-on due to offset and hysteresis, the equation can be approximated by:

$$t_{OUT} = \tau_2 \bullet \ell n [(V_{CH} \bullet t_P/\tau_1)/(V_{OFF} - V_H/2)] \quad (2)$$

For example, an 8ns input pulse gives a 1.67µs output pulse. Doubling the input pulse to 16ns lengthens the output pulse by 0.37µs. Doubling the input pulse again to 32ns adds another 0.37µs to the output pulse, and so on. The rate of 0.37µs per octave falls out of the above equation as:

$$\Delta t_{OUT}/octave = \tau_2 \bullet \ell n(2) \quad (3)$$

There is ±0.01µs jitter[5] in the output pulse which gives an uncertainty referred to the input pulse of less than 2% (60ps resolution on a 3ns pulse with a 60MHz oscilloscope—not bad!). The beauty of this circuit is that it gives resolution precisely where it's hardest to get. The jitter is due to a combination of the slow decay of the last few millivolts on C2 and the 4nV/$\sqrt{Hz}$ noise and 400MHz bandwidth of the LT1721 input stage. Increasing the offset across R3 or decreasing τ_2 will decrease this jitter at the expense of dynamic range.

The circuit topology itself is extremely fast, limited theoretically only by the speed of the diode, the capture time constant τ_1 and the pulse source impedance. Figure 14 shows results achieved with the implementation shown, compared to a plot of Equation (1). The low end is limited by the delivery time of the upstream comparators. As the input pulse width is increased, the log function is constrained by the asymptotic RC response but, rather than becoming clamped, becomes time linear. Thus, for very long input pulses the third term of Equation (1) dominates and the circuit becomes a 3µs pulse stretcher.

[2] So called because the very fast input pulse is "captured," for later examination, as a charge on the capacitor.

[3] Assuming the input pulse slew rate at the diode is infinite. This effective delay constant, about 0.4% of τ_1 or 0.8ns, is the second term of equation 1, below. Driven by the 2.5ns slew-limited LT1721, this effective delay will be 2ns.

[4] V_C is dependent on the LT1721 output voltage and nonlinear diode characteristics. Also, the Thevenin equivalent charge voltage seen by C2 is boosted slightly by R2 being terminated above ground.

[5] Output jitter increases with inputs pulse widths below ~3ns.

APPLICATIONS INFORMATION

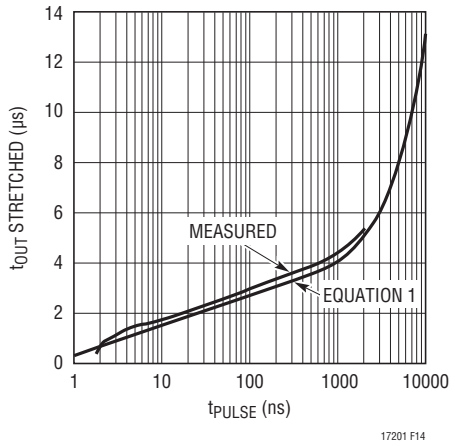


Figure 14. Log Pulse Stretcher Output Pulse vs Input Pulse

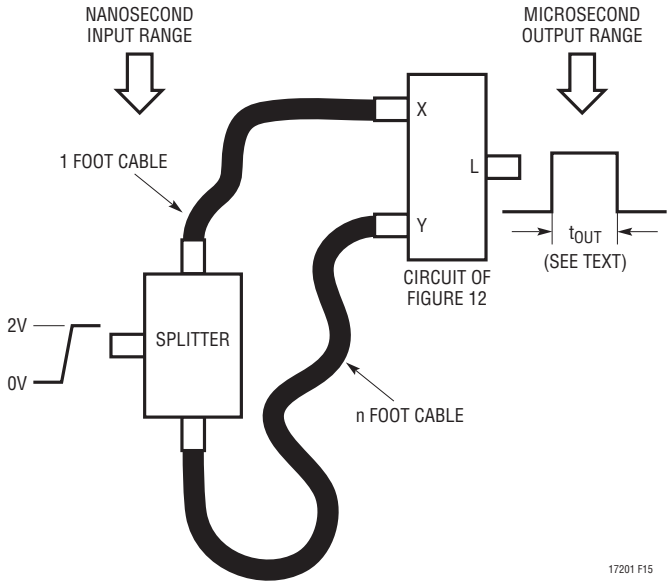


Figure 15. RG-58 Cable with Velocity of Propogation = 66%; Delay at Y = (n – 1) • 1.54ns

You don't need expensive equipment to confirm the actual overall performance of this circuit. All you need is a respectable waveform generator (capable of >~100kHz), a splitter, a variety of cable lengths and a 20MHz or 60MHz oscilloscope. Split a single pulse source into different cable lengths and then into the delay detector, feeding the longer cable into the Y input (see Figure 15). A 6 foot cable length difference will create a ~9.2ns delay (using 66% propagation speed RG-58 cable), and should result in easily measured 1.70µs output pulses. A 12 foot cable length difference will result in ~18.4ns delay and 2.07µs output pulses. The difference in the two output pulse widths is the per-octave response of your circuit (see Equation (3)). Shorter cable length differences can be used to get a plot of circuit performance down to 1.5ns (if any), which can then later be used as a lookup reference when you have moved from quantifying the circuit to using the circuit. (Note there is a slight aberration in performance below 10ns. See Figure 14.) As a final check, feed the circuit with identical cable lengths and check that it is not producing any output pulses.

10ns Triple Overlap Generator

The circuit of Figure 16 utilizes an LT1721 to generate three overlapping outputs whose pulse edges are separated by 10ns as shown. The time constant is set by the RC network on the output of comparator A. Comparator B and D trip at fixed percentages of the exponential voltage decay across the capacitor. The 4.22kΩ feed-forward to the C comparator's inverting input keeps the delay differences the same in each direction despite the exponential nature of the RC network's voltage.

There is a 15ns delay to the first edge in both directions, due to the 4.5ns delay of two LT1721 comparators, plus 6ns delay in the RC network. This starting delay is shortened somewhat if the pulse was shorter than 40ns because the RC network will not have fully settled; however, the 10ns edge separations stay constant.

The values shown utilize only the lowest 75% of the supply voltage span, which allows it to work down to 2.7V supply. The delay differences grow a couple nanoseconds from 5V to 2.7V supply due to the fixed V_{OL}/V_{OH} drops which grow as a percentage at low supply voltage. To keep this effect to a minimum, the 1kΩ pull-up on comparator A provides equal loading in either state.

Fast Waveform Sampler

Figure 17 uses a diode-bridge-type switch for clean, fast waveform sampling. The diode bridge, because of its inherent symmetry, provides lower AC errors than other semiconductor-based switching technologies. This circuit features 20dB of gain, 10MHz full power bandwidth and 100µV/°C baseline uncertainty. Switching delay is less than 15ns and the minimum sampling window width for full power response is 30ns.

APPLICATIONS INFORMATION

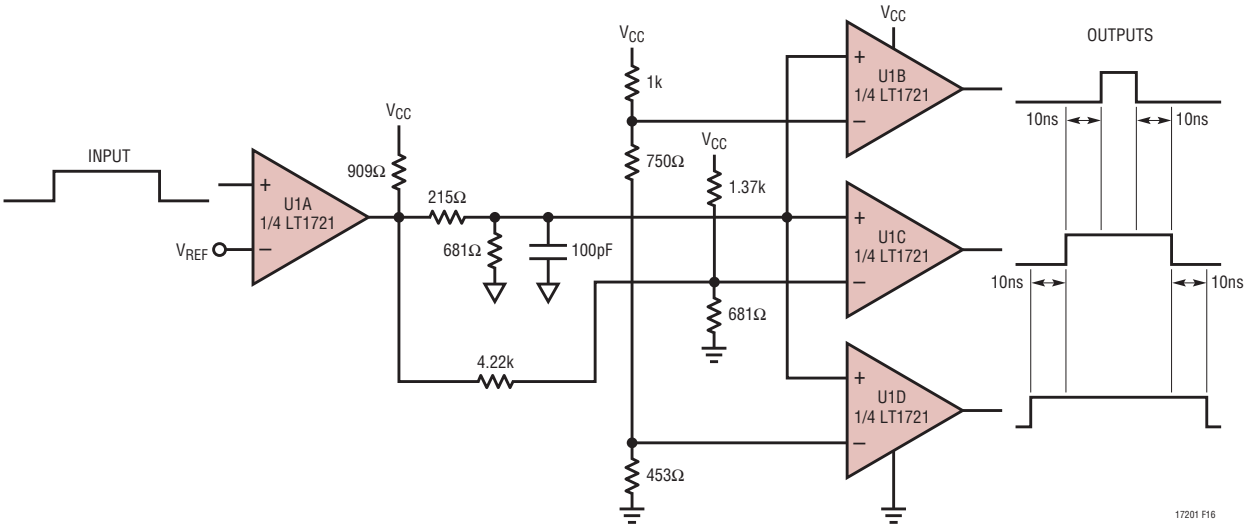


Figure 16. 10ns Triple Overlap Generator

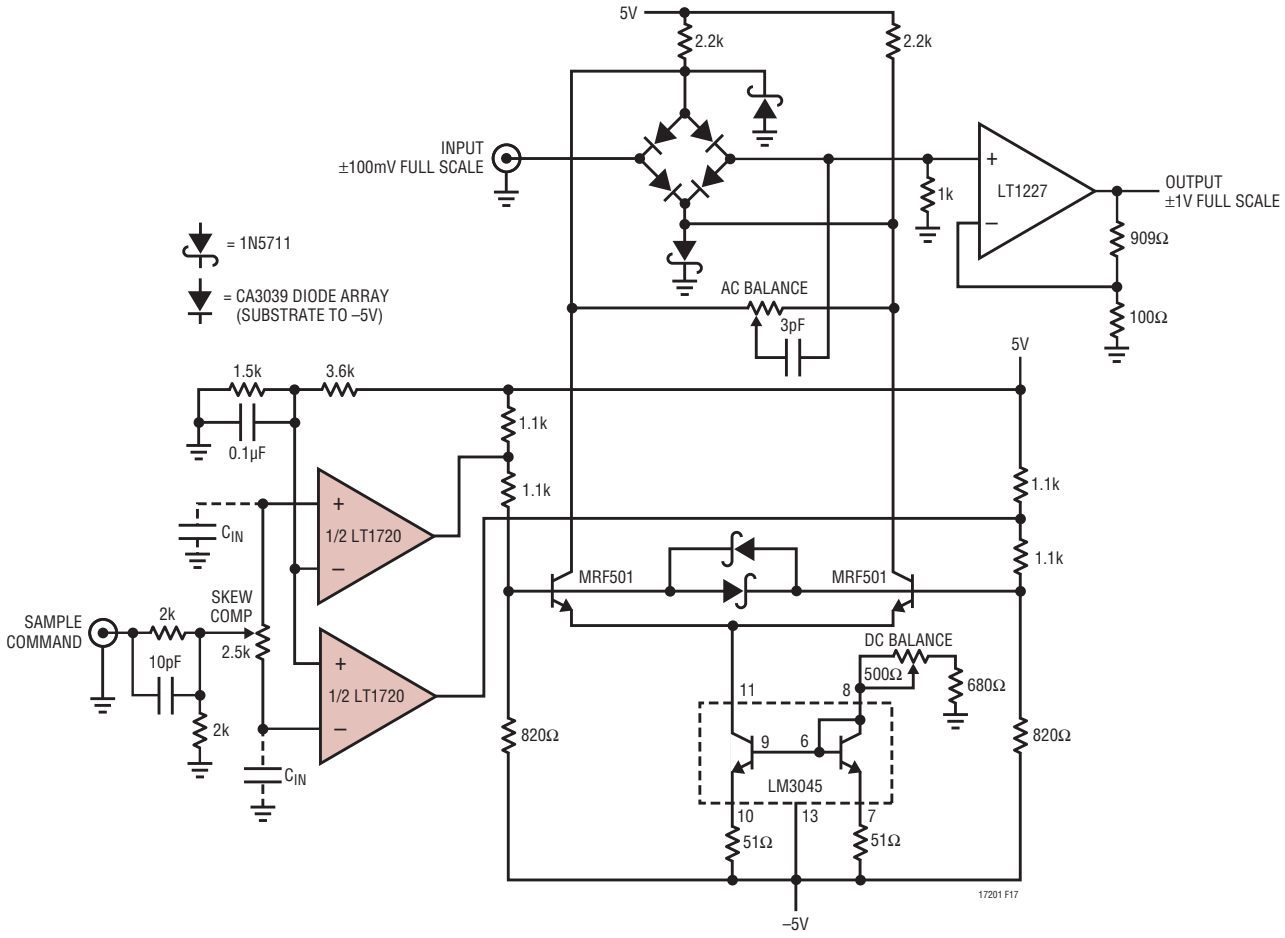


Figure 17. Fast Waveform Sampler Using the LT1720 for Timing-Skew Compensation

APPLICATIONS INFORMATION

The input waveform is presented to the diode bridge switch, the output of which feeds the LT1227 wideband amplifier. The LT1720 comparators, triggered by the sample command, generate phase-opposed outputs. These signals are level shifted by the transistors, providing complementary bipolar drive to switch the bridge. A skew compensation trim ensures bridge-drive signal simultaneity within 1ns. The AC balance corrects for parasitic capacitive bridge imbalances. A DC balance adjustment trims bridge offset.

The trim sequence involves grounding the input via 50Ω and applying a 100kHz sample command. The DC balance is adjusted for minimal bridge ON vs OFF variation at the output. The skew compensation and AC balance adjustments are then optimized for minimum AC disturbance in the output. Finally, unground the input and the circuit is ready for use.

Voltage-Controlled Clock Skew Generator

It is sometimes necessary to generate pairs of identical clock signals that are phase skewed in time. Further, it is desirable to be able to set the amount of time skew via a tuning voltage. Figure 18's circuit does this by utilizing the LT1720 to digitize phase information from a varactor-tuned time domain bridge. A 0V to 2V control signal provides ≈±10ns of output skew. This circuit operates from a 2.7V to 6V supply.

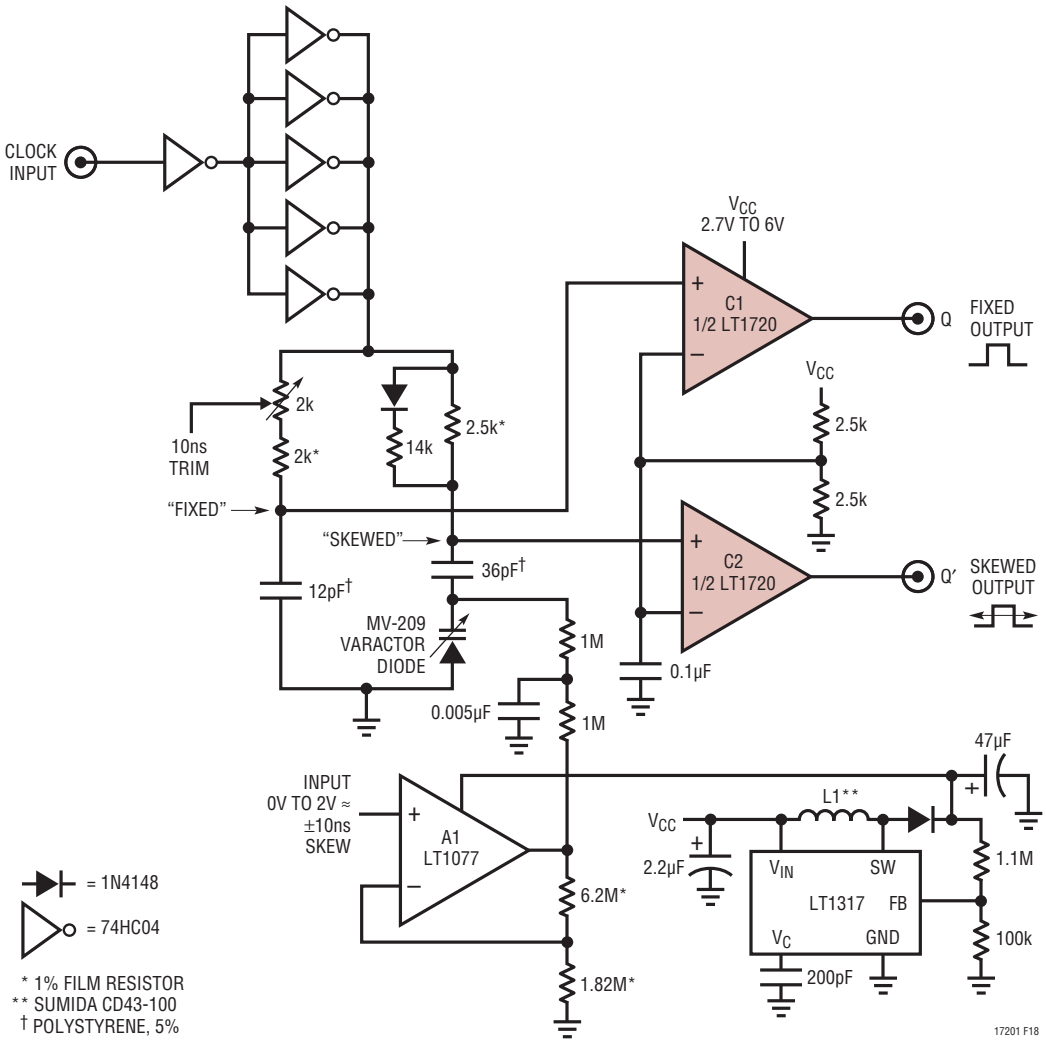


Figure 18. Voltage-Controlled Clock Skew

APPLICATIONS INFORMATION

Coincidence Detector

High speed comparators are especially suited for interfacing pulse-output transducers, such as particle detectors, to logic circuitry. The matched delays of a monolithic dual are well suited for those cases where the coincidence of two pulses needs to be detected. The circuit of Figure 19 is a coincidence detector that uses an LT1720 and discrete components as a fast AND gate.

The reference level is set to 1V, an arbitrary threshold. Only when both input signals exceed this will a coincidence be detected. The Schottky diodes from the comparator outputs to the base of the MRF-501 form the AND gate, while the other two Schottkys provide for fast turn-off. A logic AND gate could instead be used, but would add considerably more delay than the 300ps contributed by this discrete stage.

This circuit can detect coincident pulses as narrow as 3ns. For narrower pulses, the output will degrade gracefully, responding, but with narrow pulses that don't rise all the way to "high" before starting to fall. The decision delay is 4.5ns with input signals 50mV or more above the reference level. This circuit creates a TTL compatible output but it can typically drive CMOS as well.

For a more detailed description of the operation of this circuit, see Application Note 75, pages 10 and 11.

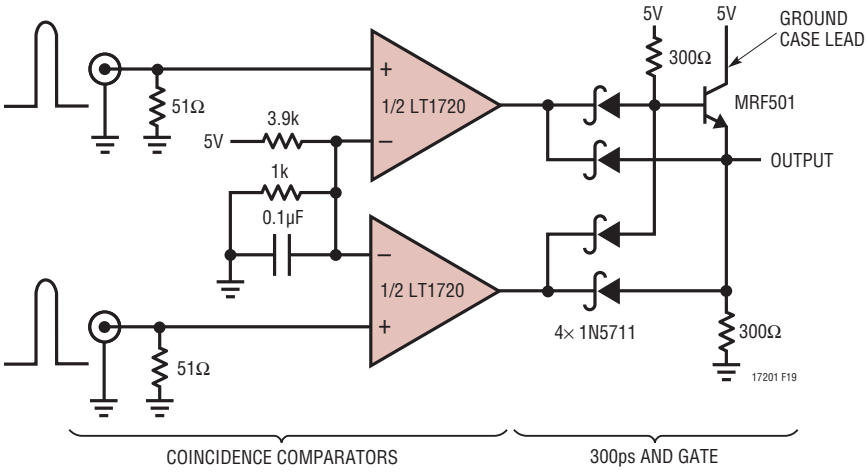
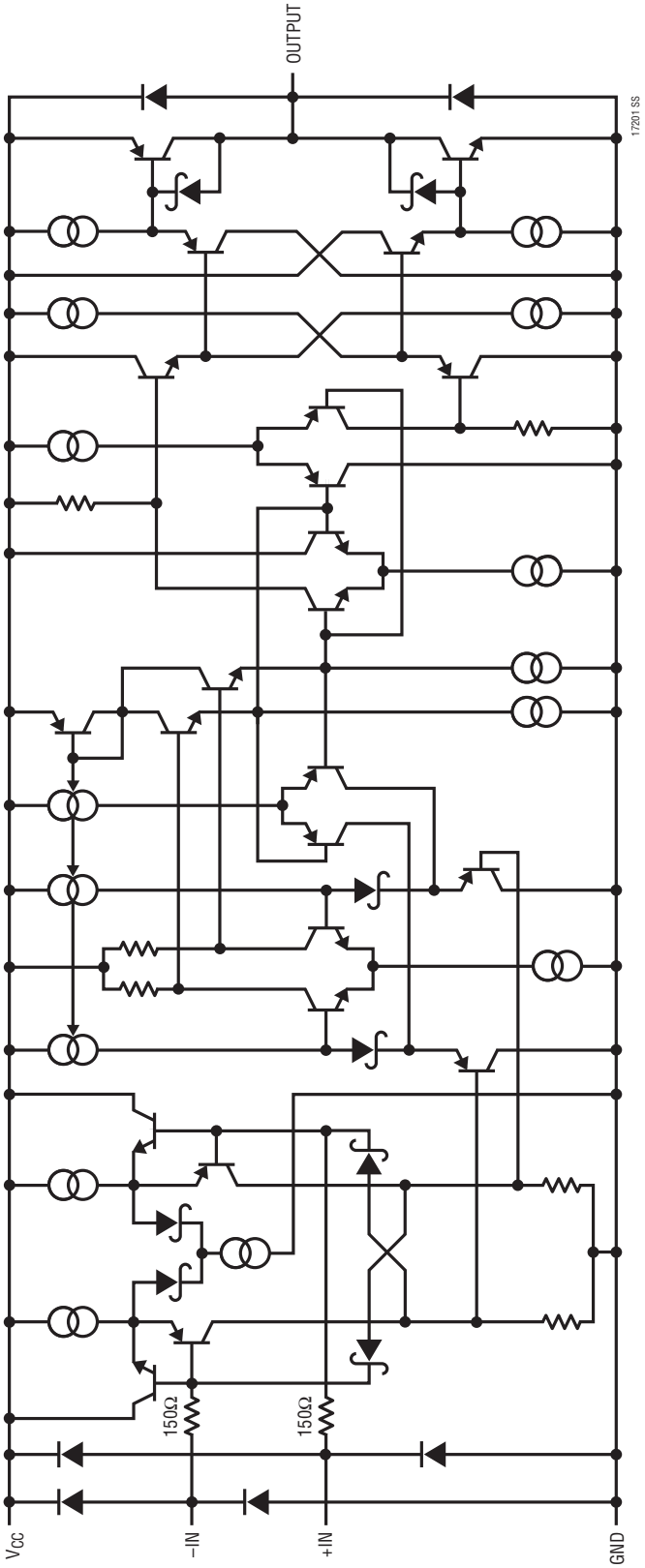


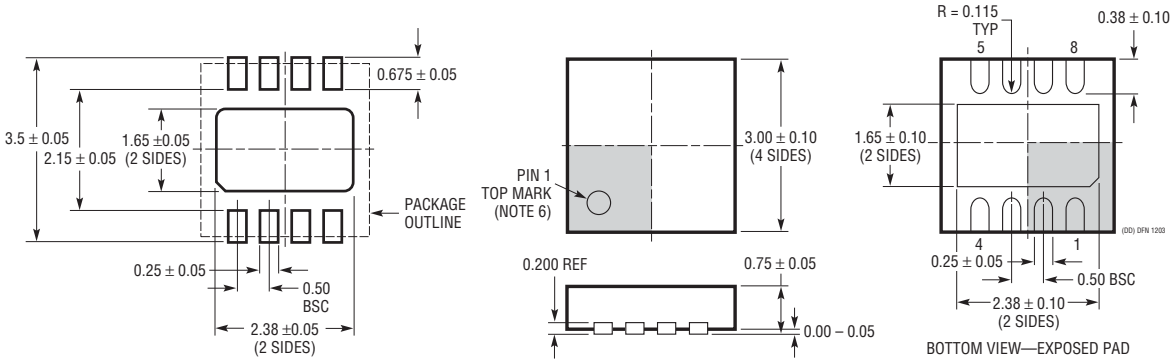
Figure 19. A 3ns Coincidence Detector

SIMPLIFIED SCHEMATIC



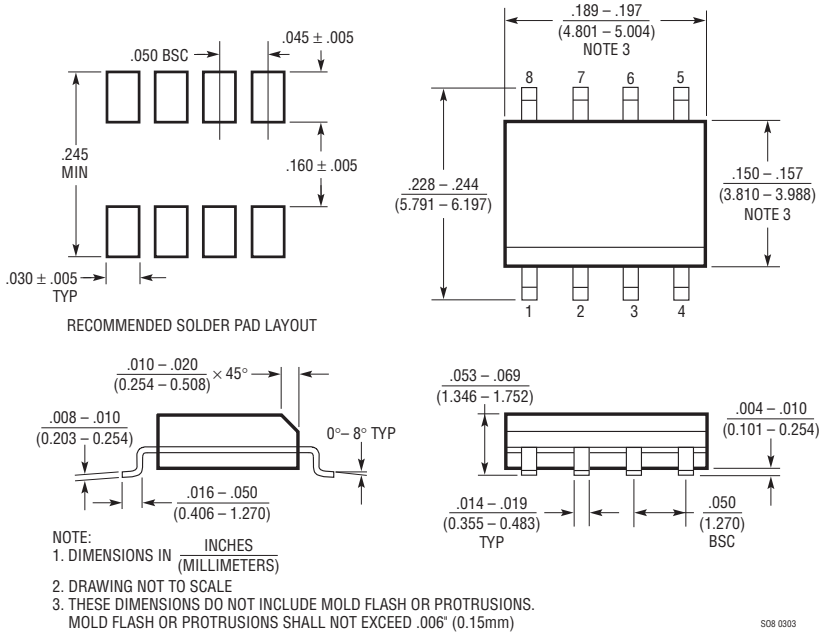
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

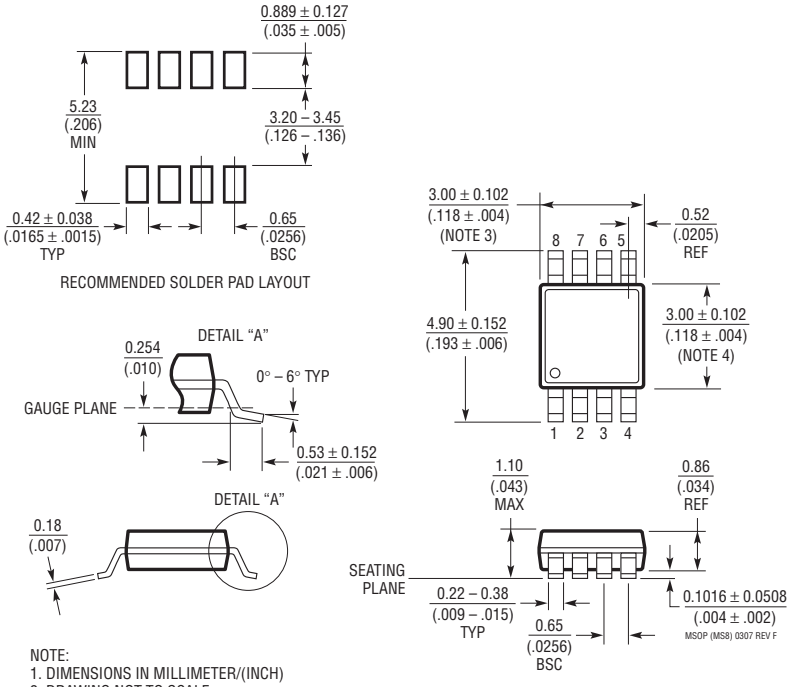


NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

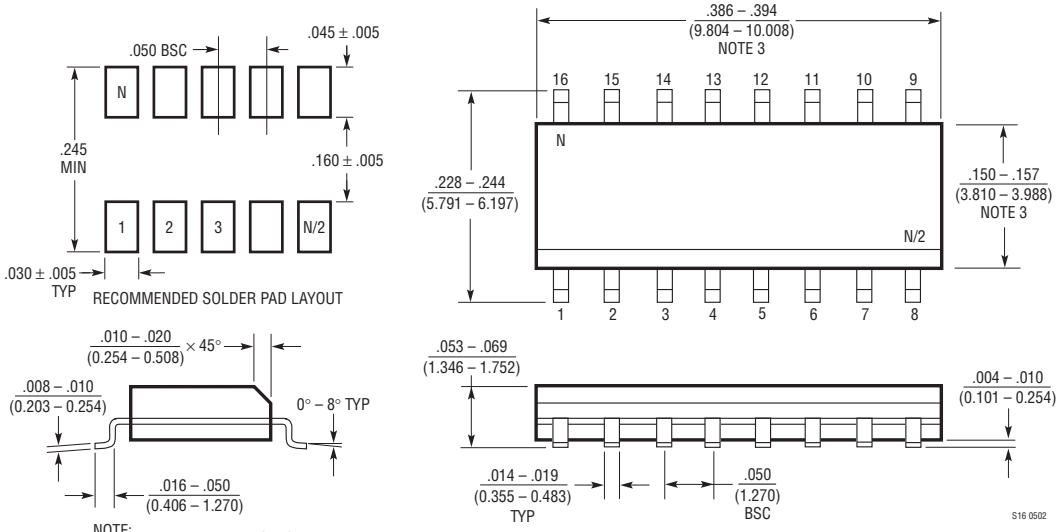
PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

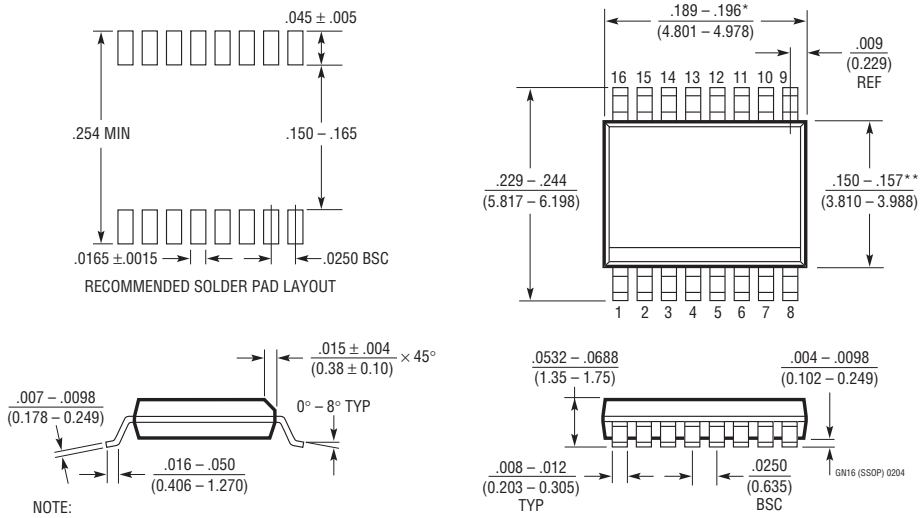
S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Pulse Stretcher

For detecting short pulses from a single sensor, a pulse stretcher is often required. The circuit of Figure 20 acts as a one-shot, stretching the width of an incoming pulse to a consistent 100ns. Unlike a logic one-shot, this LT1720-based circuit requires only 100pV-s of stimulus to trigger.

The circuit works as follows: Comparator C1 functions as a threshold detector, whereas comparator C2 is configured as a one-shot. The first comparator is prebiased with a threshold of 8mV to overcome comparator and system offsets and establish a low output in the absence of an input signal. An input pulse sends the output of C1 high, which in turn latches C2's output high. The output of C2 is fed back to the input of the first comparator, causing regeneration and latching both outputs high. Timing capacitor C now begins charging through R and, at the end of 100ns, C2 resets low. The output of C1 also goes low, latching both outputs low. A new pulse at the input of C1 can now restart the process. Timing capacitor C can be increased without limit for longer output pulses.

This circuit has an ultimate sensitivity of better than 14mV with 5ns to 10ns input pulses. It can even detect an avalanche generated test pulse of just 1ns duration with sensitivity better than 100mV.[6] It can detect short events better than the coincidence detector of Figure 14 because the one-shot is configured to catch just 100mV of upward movement from C1's V_{OL}, whereas the coincidence detector's 3ns specification is based on a full, legitimate logic high, without the help of a regenerative one-shot.

[6] See Linear Technology Application Note 47, Appendix B. This circuit can detect the output of the pulse generator described after 40dB attenuation.

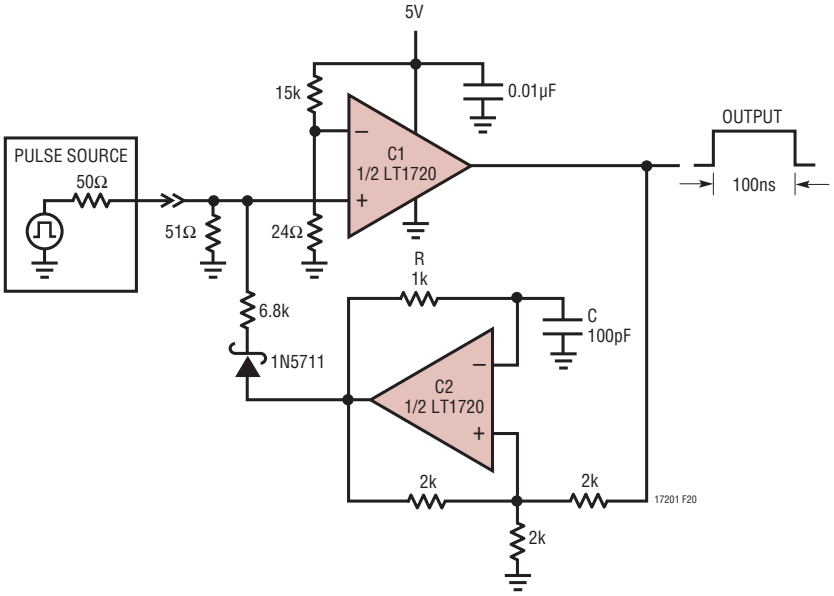


Figure 20. A 1ns Pulse Stretcher

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1016	UltraFast Precision Comparator	Industry Standard 10ns Comparator
LT1116	12ns Single Supply Ground-Sensing Comparator	Single Supply Version of LT1016
LT1394	7ns, UltraFast, Single Supply Comparator	6mA Single Supply Comparator
LT1671	60ns, Low Power, Single Supply Comparator	450µA Single Supply Comparator
LT1715	4ns, 150MHz Dual Comparator	Similar to the LT1720 with Independent Input/Output Supplies
LT1719	4.5ns Single Supply 3V/5V Comparator	Single Comparator Similar to the LT1720/LT1721

Linear Technology Corporation
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SBOS271D − MAY 2003 − REVISED JUNE 2007

Low-Noise, High-Speed, 16-Bit Accurate, CMOS OPERATIONAL AMPLIFIER

FEATURES

- **High Bandwidth: 150MHz**
- **16-Bit Settling in 150ns**
- **Low Noise: 3nV/√Hz**
- **Low Distortion: 0.003%**
- **Low Power: 9.5mA (typ) on 5.5V**
- **Shutdown to 5μA**
- **Unity-Gain Stable**
- **Excellent Output Swing: (V+) − 100mV to (V−) + 100mV**
- **Single Supply: +2.7V to +5.5V**
- **Tiny Packages: MSOP and SOT23**

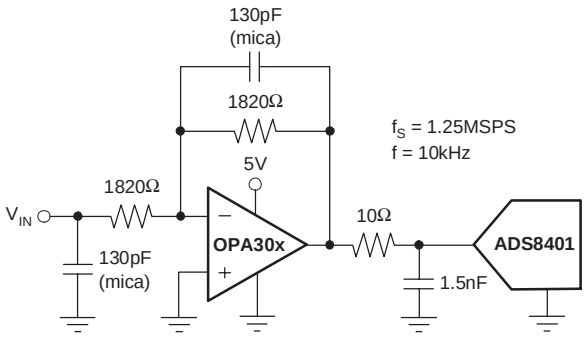
APPLICATIONS

- **16-Bit ADC Input Drivers**
- **Low-Noise Preamplifiers**
- **IF/RF Amplifiers**
- **Active Filtering**

DESCRIPTION

The OPA300 and OPA301 series high-speed, voltage-feedback, CMOS operational amplifiers are designed for 16-bit resolution systems. The OPA300/OPA301 series are unity-gain stable and feature excellent settling and harmonic distortion specifications. Low power applications benefit from low quiescent current. The OPA300 and OPA2300 feature a digital shutdown (Enable) function to provide additional power savings during idle periods. Optimized for single-supply operation, the OPA300/OPA301 series offer superior output swing and excellent common-mode range.

The OPA300 and OPA301 series op amps have 150MHz of unity-gain bandwidth, low 3nV/√Hz voltage noise, and 0.1% settling within 30ns. Single-supply operation from 2.7V (±1.35V) to 5.5V (±2.75V) and an available shutdown function that reduces supply current to 5μA are useful for portable low-power applications. The OPA300 and OPA301 are available in SO-8 and SOT-23 packages. The OPA2300 is available in MSOP-10, and the OPA2301 is available in SO-8 and MSOP-8. All versions are specified over the industrial temperature range of −40°C to +125°C.



Typical Application

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA300	SO-8	D	300A
OPA300	SOT23-6	DBV	A52
OPA301	SO-8	D	301A
OPA301	SOT23-5	DBV	AUP
OPA2300	MSOP−10	DGS	C01
OPA2301	SO−8	D	OPA2301A
OPA2301	MSOP−8	DGK	OAWM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

Power Supply V+	7V
Signal Input Terminals(2), Voltage	0.5V to (V+) + 0.5V
Current	±10mA
Open Short-Circuit Current(3)	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−60°C to +150°C
Junction Temperature	+150°C
ESD Ratings	
Human Body Model (HBM)	4kV
Charged-Device Model (CDM)	500V

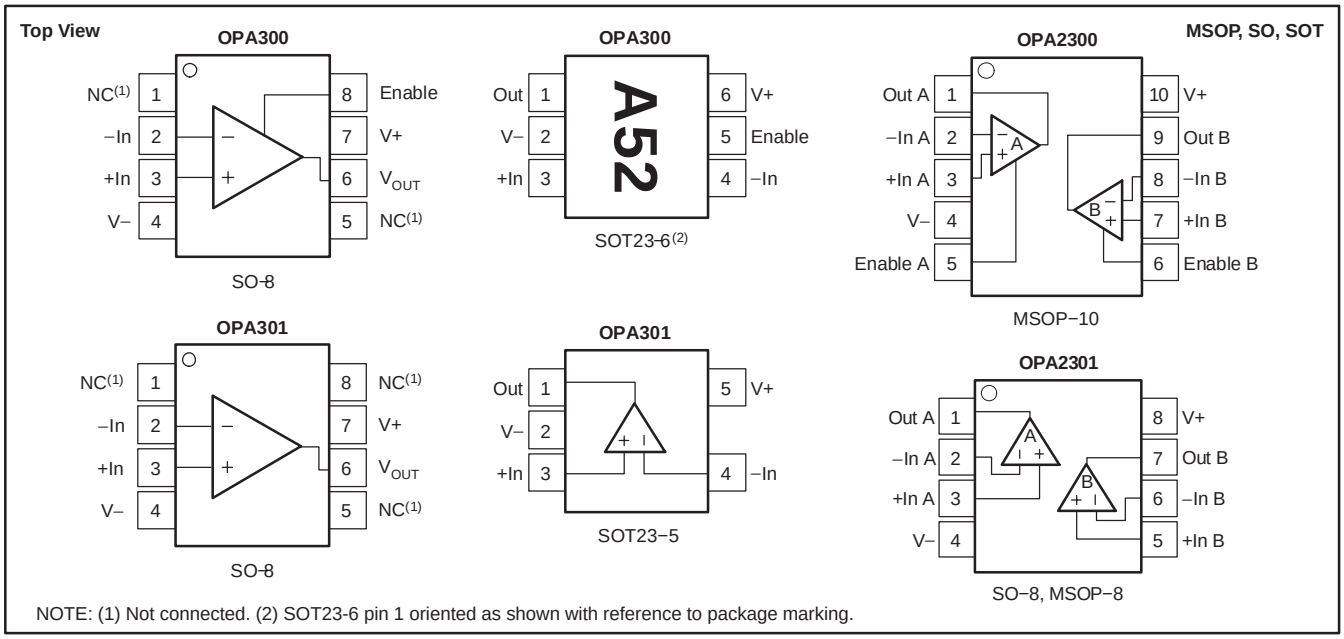
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground; one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN ASSIGNMENTS



NOTE: (1) Not connected. (2) SOT23-6 pin 1 oriented as shown with reference to package marking.

ELECTRICAL CHARACTERISTICS: V_S = 2.7V to 5.5V

Boldface limits apply over the temperature range, **T_A = −40°C to +125°C**.

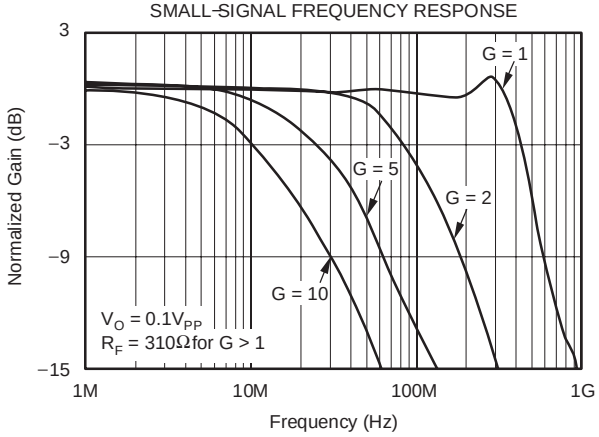
All specifications at T_A = +25°C, R_L = 2kΩ connected to V_S/2, V_{OUT} = V_S/2, and V_{CM} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA300, OPA301 OPA2300, OPA2301 MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 5V		1	5	mV
Over Temperature					**7**	**mV**
Drift	**dV_{OS}/dT**			**2.5**		**µV/°C**
vs. Power Supply	**PSRR**	**V_S = 2.7V to 5.5V, V_{CM} < (V+) −0.9V**		**50**	**200**	**µV/V**
Channel Separation, dc				140		dB
f = 5MHz				100		dB
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) − 0.2		(V+) − 0.9	V
Common-Mode Rejection Ratio	**CMRR**	**(V−) − 0.2V < V_{CM} < (V+) − 0.9V**	**66**	**80**		**dB**
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.1	±5	pA
Input Offset Current	I_{OS}			±0.5	±5	pA
INPUT IMPEDANCE						
Differential				10^{13} || 3		Ω || pF
Common-Mode				10^{13} || 6		Ω || pF
NOISE						
Input Voltage Noise, f = 0.1Hz to 1MHz				40		μV_{PP}
Input Voltage Noise Density, f > 1MHz	e_n			3		$nV/\sqrt{Hz}$
Input Current Noise Density, f < 1kHz	i_n			1.5		$fA/\sqrt{Hz}$
Differential Gain Error		NTSC, R_L = 150Ω		0.01		%
Differential Phase Error		NTSC, R_L = 150Ω		0.1		°
OPEN-LOOP GAIN						
Open−Loop Voltage Gain	A_{OL}	V_S = 5V, R_L = 2kΩ, 0.1V < V_O < 4.9V	95	106		dB
Over Temperature		**V_S = 5V, R_L = 2kΩ, 0.1V < V_O < 4.9V**	**90**			**dB**
		V_S = 5V, R_L = 100Ω, 0.5V < V_O < 4.5V	95	106		dB
Over Temperature		**V_S = 5V, R_L = 100Ω, 0.5V < V_O < 4.5V**	**90**			**dB**
OUTPUT						
Voltage Output Swing from Rail		R_L = 2kΩ, A_{OL} > 95dB		75	100	mV
		R_L = 100Ω, A_{OL} > 95dB		300	500	mV
Short-Circuit Current	I_{SC}			70		mA
Open-Loop Output Impedance	R_O	I_O = 0, f = 1MHz		20		Ω
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			150		MHz
Slew Rate	SR	G = +1		80		V/µs
Settling Time, 0.01%	t_S	V_S = 5V, 2V Step, G = +1		90		ns
0.1%				30		ns
Overload Recovery Time		Gain = −1		30		ns
Total Harmonic Distortion + Noise	THD+N	V_S = 5V, V_O = $3V_{PP}$, G = +1, f = 1kHz		0.003		%
POWER SUPPLY						
Specified Voltage Range	V_S		2.7		5.5	V
Operating Voltage Range				2.7 to 5.5		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		9.5	12	mA
Over Temperature					**13**	**mA**
SHUTDOWN						
t_{OFF}				40		ns
t_{ON}				5		µs
V_L (shutdown)			(V−) − 0.2		(V−) + 0.8	V
V_H (amplifier is active)			(V−) + 2.5		(V+) + 0.2	V
I_{QSD} (per amplifier)				3	10	µA
TEMPERATURE RANGE						
Specified Range			−40		+125	°C
Operating Range			−55		+125	°C
Storage Range			−60		+150	°C
Thermal Resistance	θ_{JA}					°C/W
SO-8, MSOP−8, MSOP-10				150		°C/W
SOT23-5, SOT23-6				200		°C/W

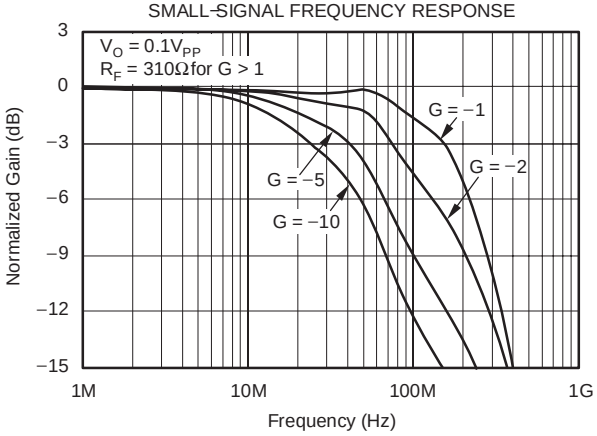
TYPICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_S = 5V, and R_L = 150Ω connected to V_S/2 unless otherwise noted.

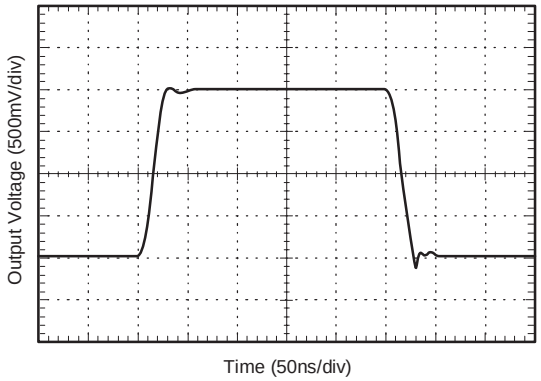
NONINVERTING GAIN
SMALL−SIGNAL FREQUENCY RESPONSE



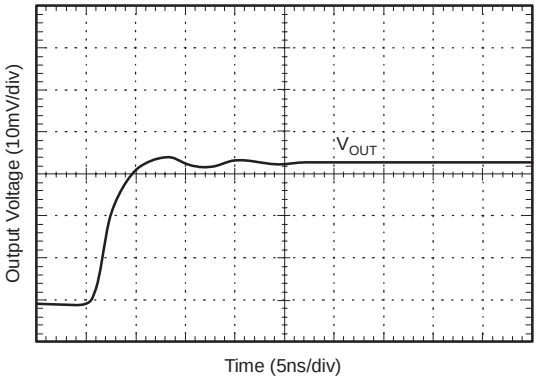
INVERTING GAIN
SMALL−SIGNAL FREQUENCY RESPONSE



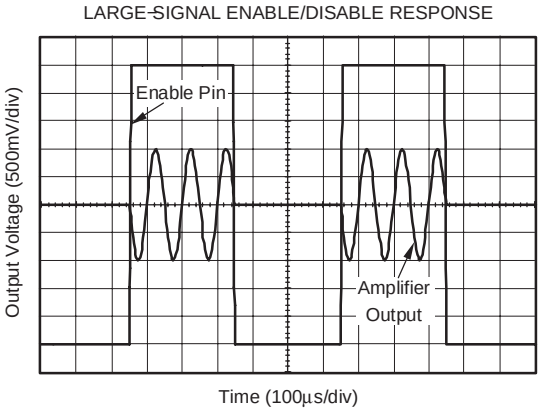
LARGE−SIGNAL STEP RESPONSE



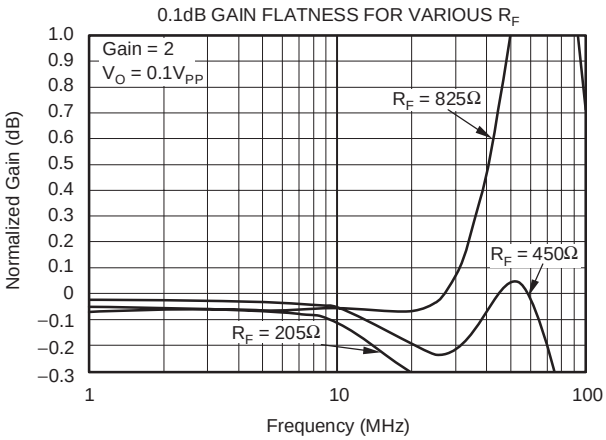
SMALL−SIGNAL STEP RESPONSE



LARGE−SIGNAL ENABLE/DISABLE RESPONSE



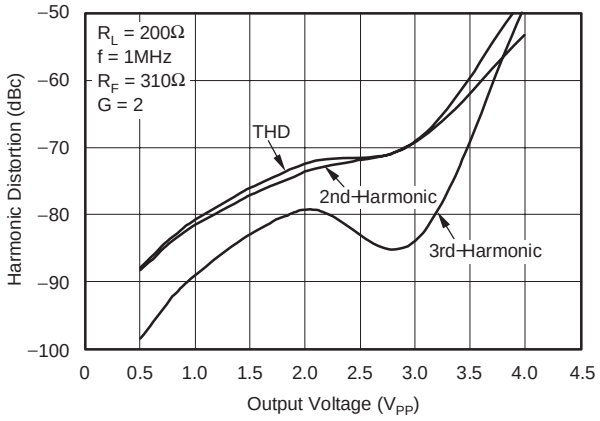
0.1dB GAIN FLATNESS FOR VARIOUS R_F



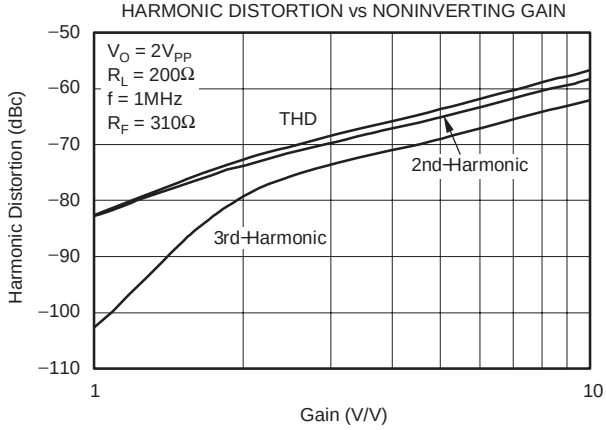
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_S = 5V, and R_L = 150Ω connected to V_S/2 unless otherwise noted.

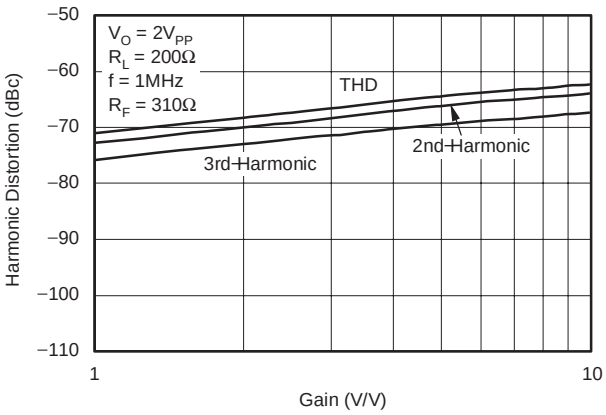
HARMONIC DISTORTION vs OUTPUT VOLTAGE



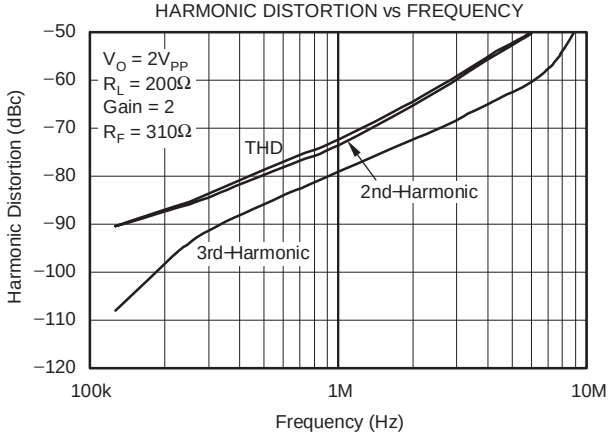
HARMONIC DISTORTION vs NONINVERTING GAIN



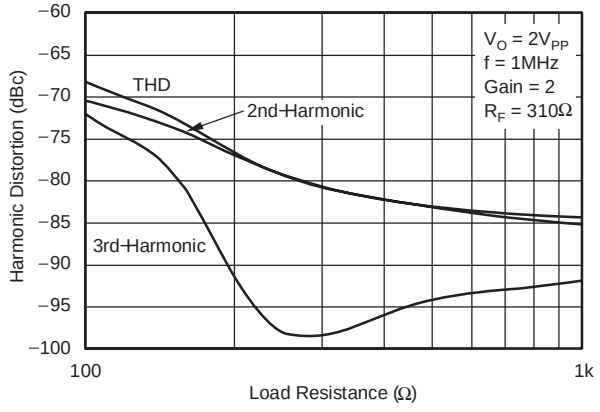
HARMONIC DISTORTION vs INVERTING GAIN



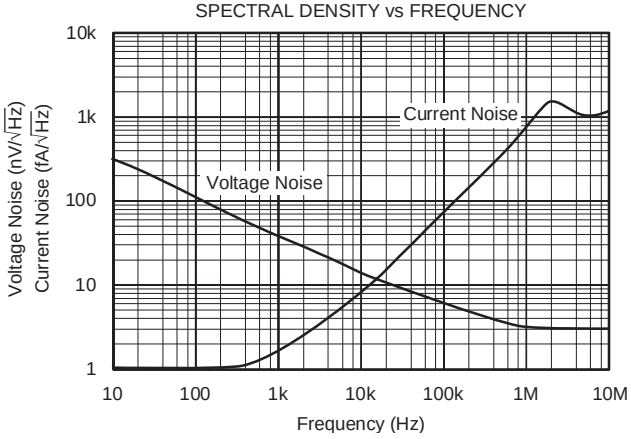
HARMONIC DISTORTION vs FREQUENCY



HARMONIC DISTORTION vs LOAD RESISTANCE



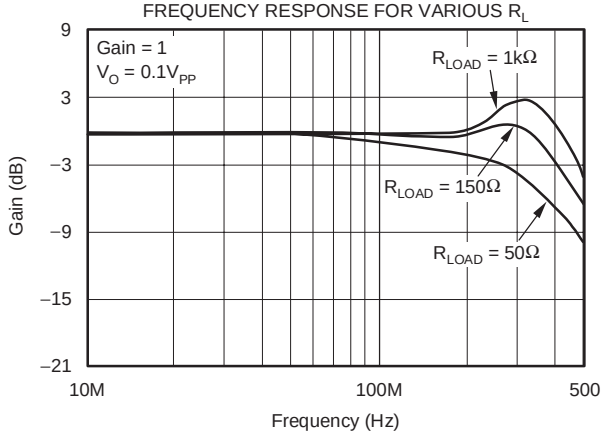
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



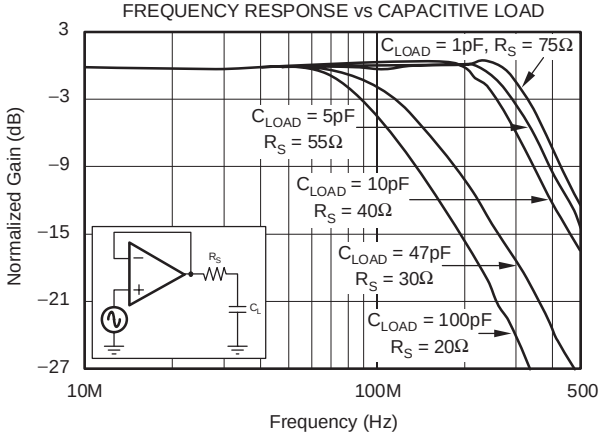
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_S = 5V, and R_L = 150Ω connected to V_S/2 unless otherwise noted.

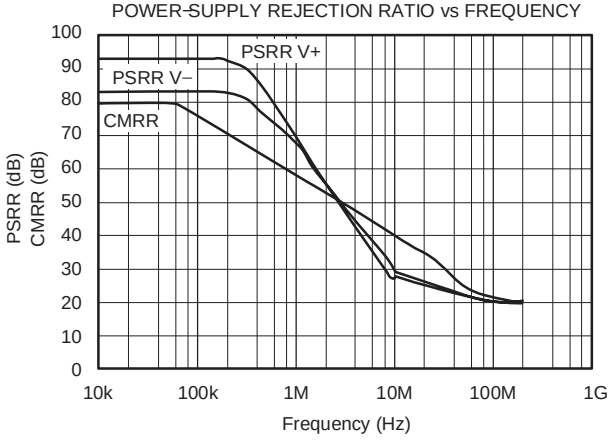
FREQUENCY RESPONSE FOR VARIOUS R_L



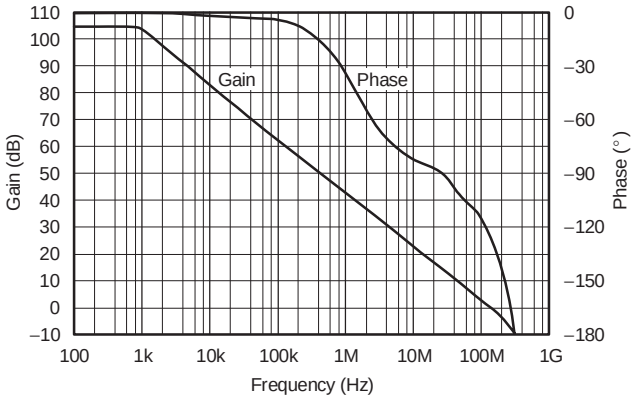
FREQUENCY RESPONSE vs CAPACITIVE LOAD



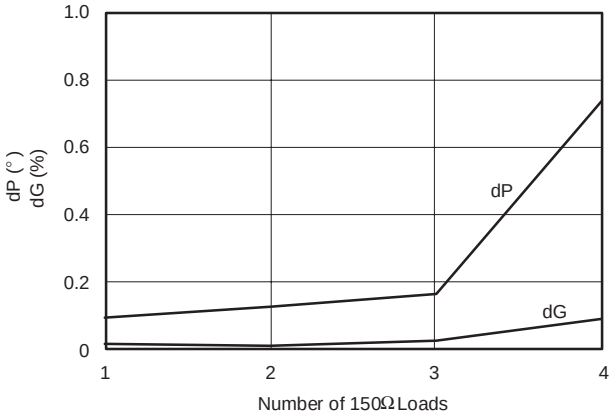
COMMON-MODE REJECTION RATIO AND
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



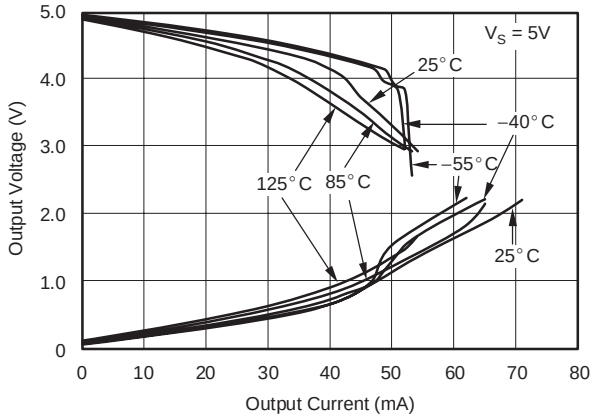
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



COMPOSITE VIDEO
DIFFERENTIAL GAIN AND PHASE



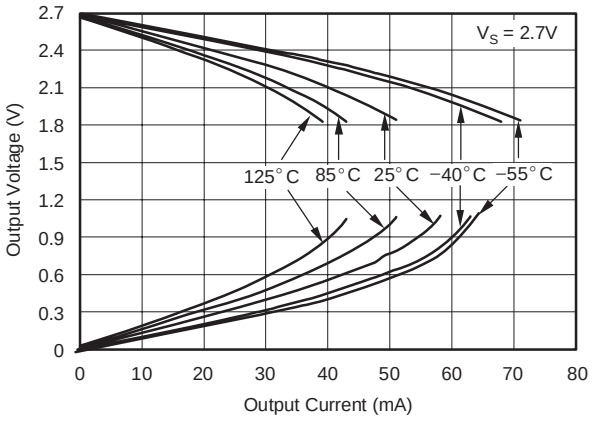
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



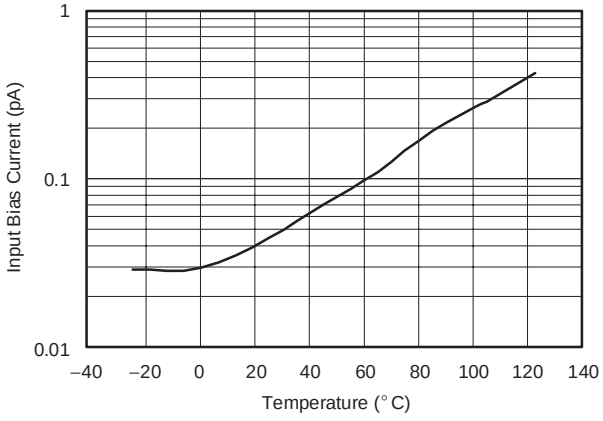
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_S = 5V, and R_L = 150Ω connected to V_S/2 unless otherwise noted.

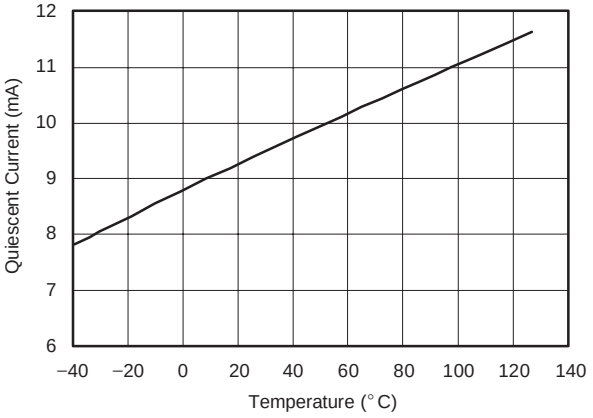
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



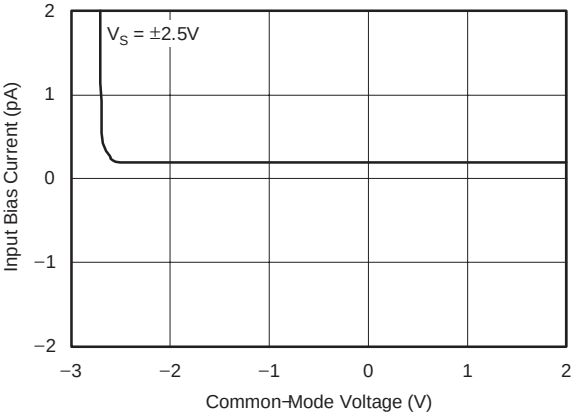
INPUT BIAS CURRENT vs TEMPERATURE



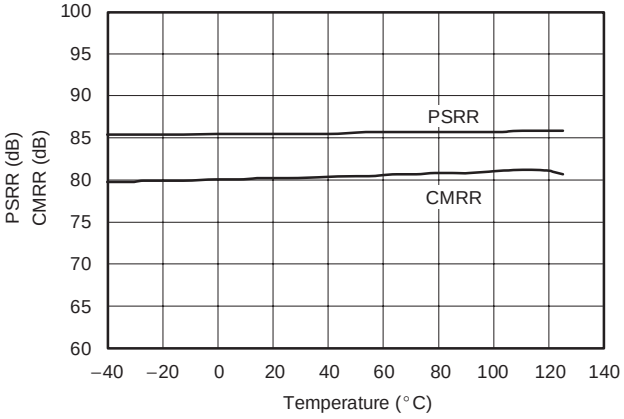
QUIESCENT CURRENT vs TEMPERATURE



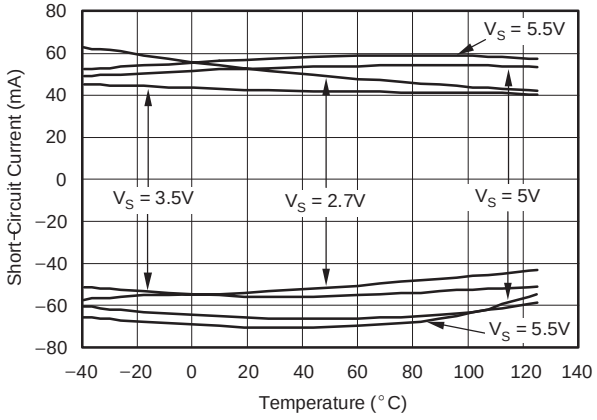
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



POWER-SUPPLY REJECTION RATIO AND
COMMON-MODE REJECTION RATIO vs TEMPERATURE



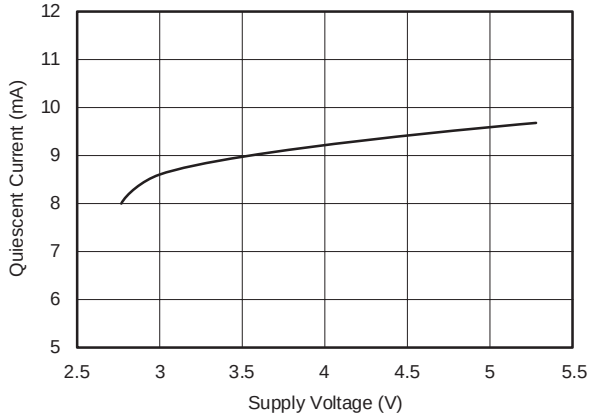
SHORT-CIRCUIT CURRENT vs TEMPERATURE



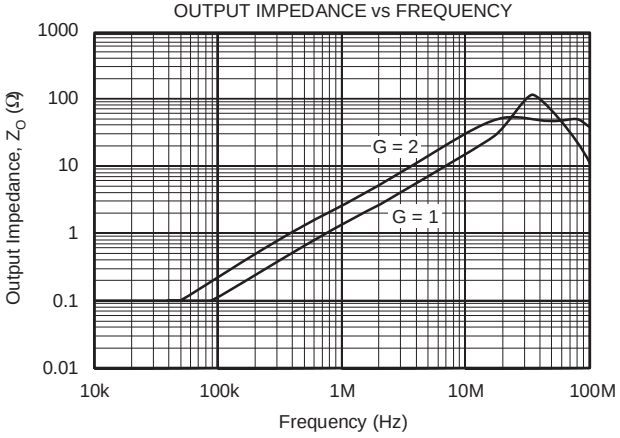
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_S = 5V, and R_L = 150Ω connected to V_S/2 unless otherwise noted.

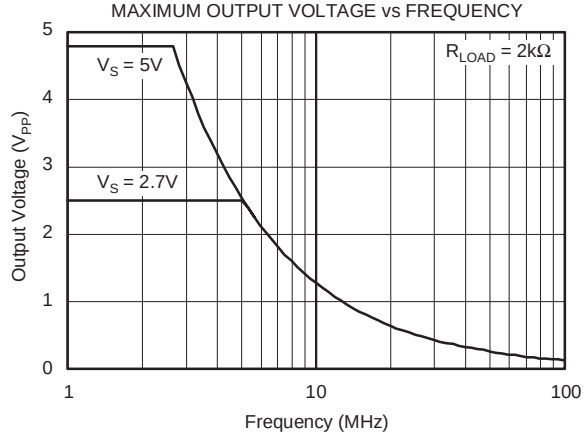
QUIESCENT CURRENT vs SUPPLY VOLTAGE



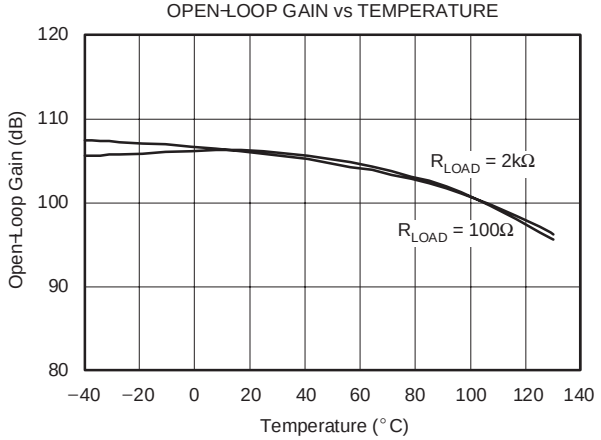
OUTPUT IMPEDANCE vs FREQUENCY



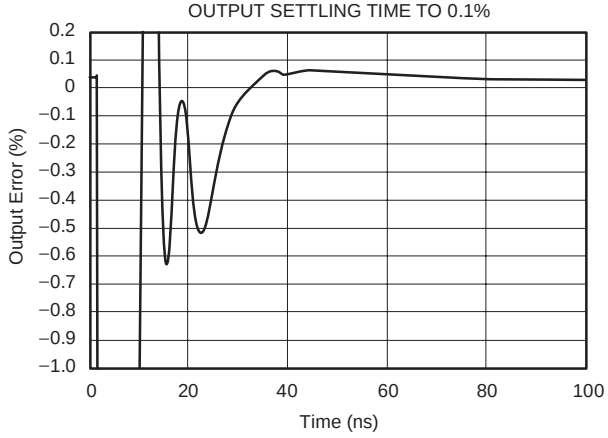
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



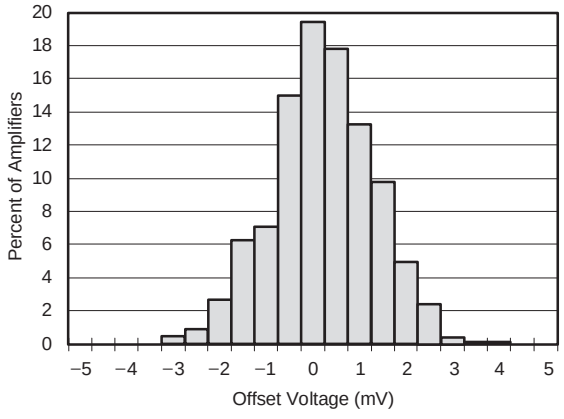
OPEN-LOOP GAIN vs TEMPERATURE



OUTPUT SETTLING TIME TO 0.1%

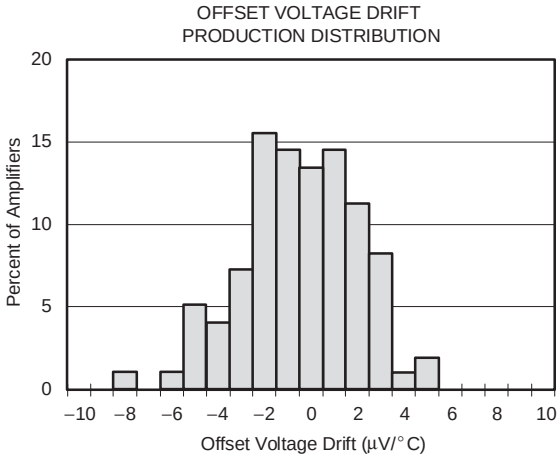


OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_S = 5V, and R_L = 150Ω connected to V_S/2 unless otherwise noted.



APPLICATIONS INFORMATION

The OPA300 and OPA301 series of single-supply CMOS op amps are designed to interface with high-speed 16-bit analog-to-digital converters (ADCs). Featuring wide 150MHz bandwidth, fast 150ns settling time to 16 bits, and high open loop gain, this series offers excellent performance in a small SO-8 and tiny SOT23 packages.

THEORY OF OPERATION

The OPA300 and OPA301 series op amps use a classic two-stage topology, shown in Figure 1. The differential input pair is biased to maximize slew rate without compromising stability or bandwidth. The folded cascode adds the signal from the input pair and presents a differential signal to the class AB output stage. The class AB output stage allows rail- to-rail output swing, with high-impedance loads (> 2kΩ), typically 100mV from the supply rails. With 10Ω loads, a useful output swing can be achieved and still maintain high open-loop gain. See the typical characteristic *Output Voltage Swing vs Output Current.*

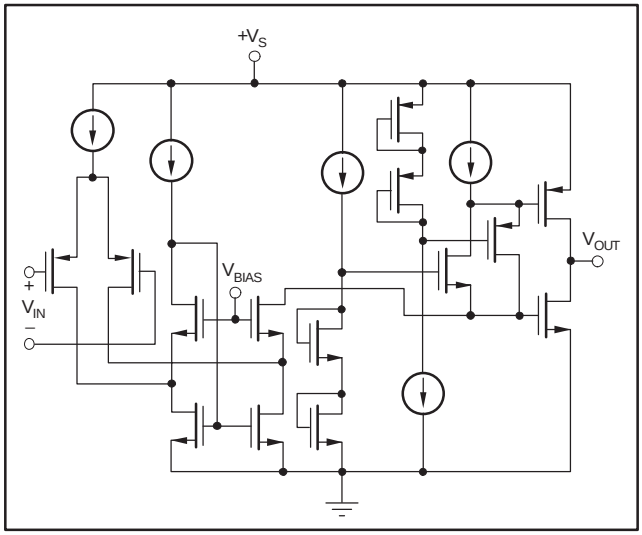


Figure 1. OPA30x Classic Two-Stage Topology

OPERATING VOLTAGE

OPA300/OPA301 series op amp parameters are fully specified from +2.7V to +5.5V. Supply voltages higher than 5.5V (absolute maximum) can cause permanent damage to the amplifier. Many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

PCB LAYOUT

As with most high-speed operational amplifiers, board layout requires special attention to maximize AC and DC performance. Extensive use of ground planes, short lead lengths, and high-quality bypass capacitors will minimize leakage that can compromise signal quality. Guard rings applied with potential as near to the input pins as possible help minimize board leakage.

INPUT AND ESD PROTECTION

All OPA300/OPA301 series op amps' pins are static-protected with internal ESD protection diodes tied to the supplies, as shown in Figure 2. These diodes will provide overdrive protection if the current is externally limited to 10mA, as stated in the Absolute Maximum Ratings. Any input current beyond the Absolute Maximum Ratings, or long-term operation at maximum ratings, will shorten the lifespan of the amplifier.

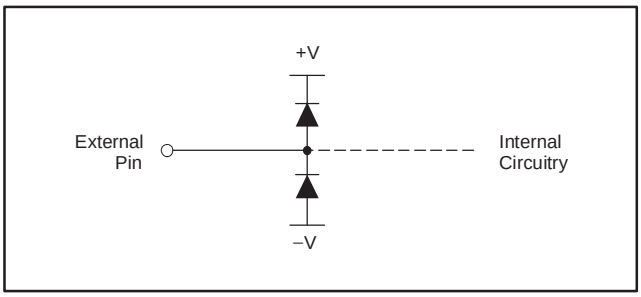


Figure 2. ESD Protection Diodes

ENABLE FUNCTION

The shutdown function of the OPA300 and OPA2300 is referenced to the negative supply voltage of the operational amplifier. A logic level HIGH enables the op amp. A valid logic HIGH is defined as 2.5V above the negative supply applied to the enable pin. A valid logic LOW is defined as < 0.8V above the negative supply pin. If dual or split power supplies are used, care should be taken to ensure logic input signals are properly referred to the negative supply voltage. If this pin is not connected to a valid high or low voltage, the internal circuitry will pull the node high and enable the part to function.

The logic input is a high-impedance CMOS input. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10μs; disable time is 1μs. When disabled, the output assumes a high-impedance state. This allows the OPA300 to be operated as a gated amplifier, or to have its output multiplexed onto a common analog output bus.

DRIVING CAPACITIVE LOADS

When using high-speed operational amplifiers, it is extremely important to consider the effects of capacitive loading on amplifier stability. Capacitive loading will interact with the output impedance of the operational amplifier, and depending on the capacitor value, may significantly decrease the gain bandwidth, as well as introduce peaking. To reduce the effects of capacitive loading and allow for additional capacitive load drive, place a series resistor between the output and the load. This will reduce available bandwidth, but permit stable operation with capacitive loading. Figure 3 illustrates the recommended relationship between the resistor and capacitor values.

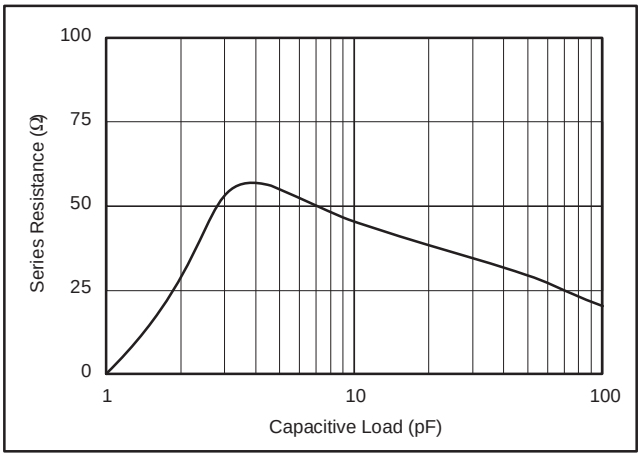


Figure 3. Recommended R_S and C_L Combinations

Amplifiers configured in unity gain are most susceptible to stability issues. The typical characteristic, *Frequency Response vs Capacitive Load,* describes the relationship between capacitive load and stability for the OPA300/OPA301 series. In unity gain, the OPA300/OPA301 series is capable of driving a few picofarads of capacitive load without compromising stability. Board level parasitic capacitance can often fall into the range of a picofarad or more, and should be minimized through good circuit-board layout practices to avoid compromising the stability of the OPA300/OPA301. For more information on detecting parasitics during testing, see the Application Note *Measuring Board Parasitics in High-Speed Analog Design* (SBOA094), available at the TI web site www.ti.com.

DRIVING A 16-BIT ADC

The OPA300/OPA301 series feature excellent THD+noise, even at frequencies greater than 1MHz, with a 16-bit settling time of 150ns. Figure 4 shows a total single supply solution for high-speed data acquisition. The OPA300/OPA301 directly drives the ADS8401, a 1.25 mega sample per second (MSPS) 16-bit data converter. The OPA300/OPA301 is configured in an inverting gain of 1, with a 5V single supply. Results of the OPA300/OPA301 performance are summarized in Table 1.

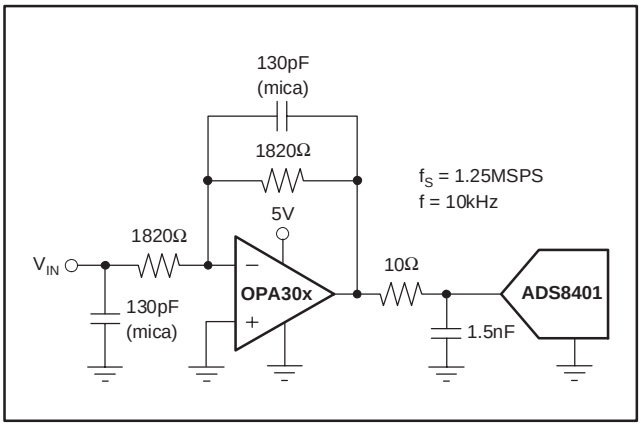


Figure 4. The OPA30x Drives the 16-Bit ADS8401

PARAMETER	RESULTS (f = 10kHz)
THD	−99.3dB
SFDR	101.2dB
THD+N	84.2dB
SNR	84.3dB

Table 1. OPA30x Performance Results Driving a 1.25MSPS ADS8401

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA2300AIDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	Purchase Samples
OPA2300AIDGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	Purchase Samples
OPA2300AIDGST	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	Request Free Samples
OPA2300AIDGSTG4	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	Request Free Samples
OPA2301AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA2301AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA2301AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA2301AIDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA2301AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	Request Free Samples
OPA2301AIDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	Request Free Samples
OPA2301AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA2301AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA300AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA300AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA300AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA300AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA300AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA300AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA301AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA301AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA301AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA301AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA301AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA301AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA301AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA301AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples

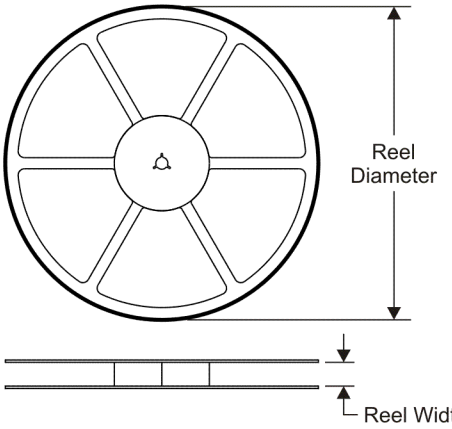
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

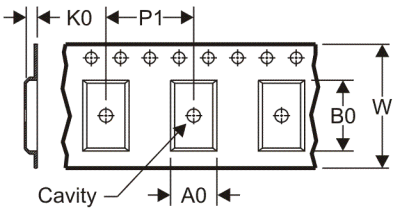
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

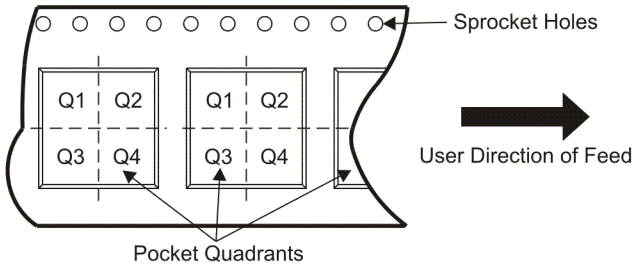


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

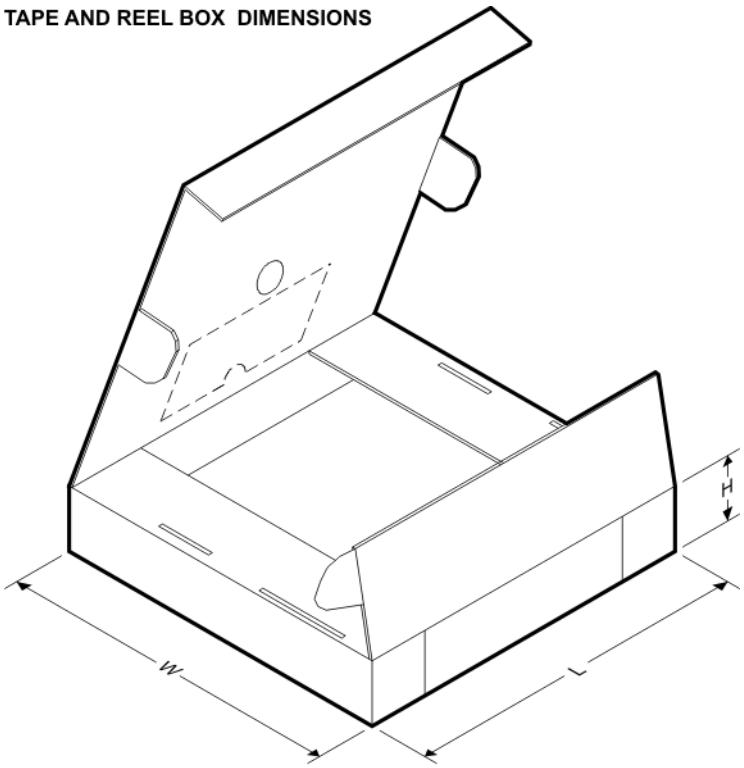
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2300AIDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2300AIDGST	MSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2301AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2301AIDGKT	MSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2301AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA300AIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA300AIDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA301AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA301AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA301AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

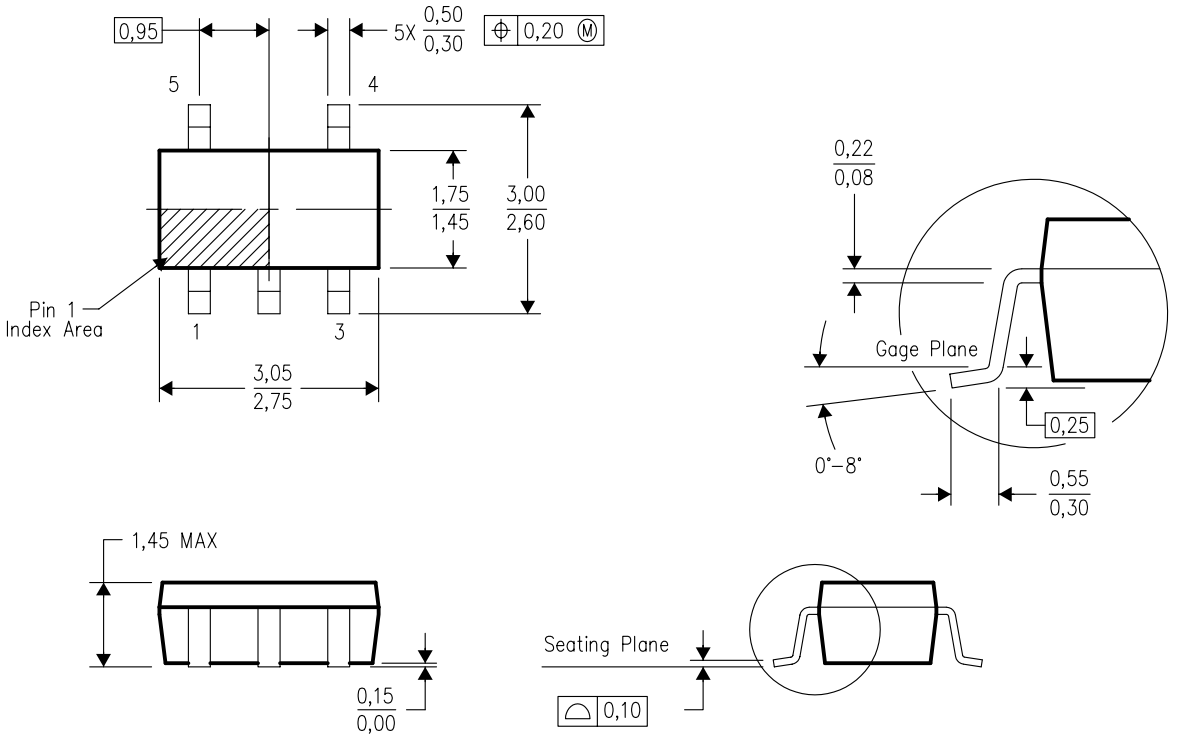
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2300AIDGSR	MSOP	DGS	10	2500	346.0	346.0	29.0
OPA2300AIDGST	MSOP	DGS	10	250	190.5	212.7	31.8
OPA2301AIDGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
OPA2301AIDGKT	MSOP	DGK	8	250	190.5	212.7	31.8
OPA2301AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA300AIDBVR	SOT-23	DBV	6	3000	190.5	212.7	31.8
OPA300AIDBVT	SOT-23	DBV	6	250	190.5	212.7	31.8
OPA301AIDBVR	SOT-23	DBV	5	3000	190.5	212.7	31.8
OPA301AIDBVT	SOT-23	DBV	5	250	190.5	212.7	31.8
OPA301AIDR	SOIC	D	8	2500	346.0	346.0	29.0

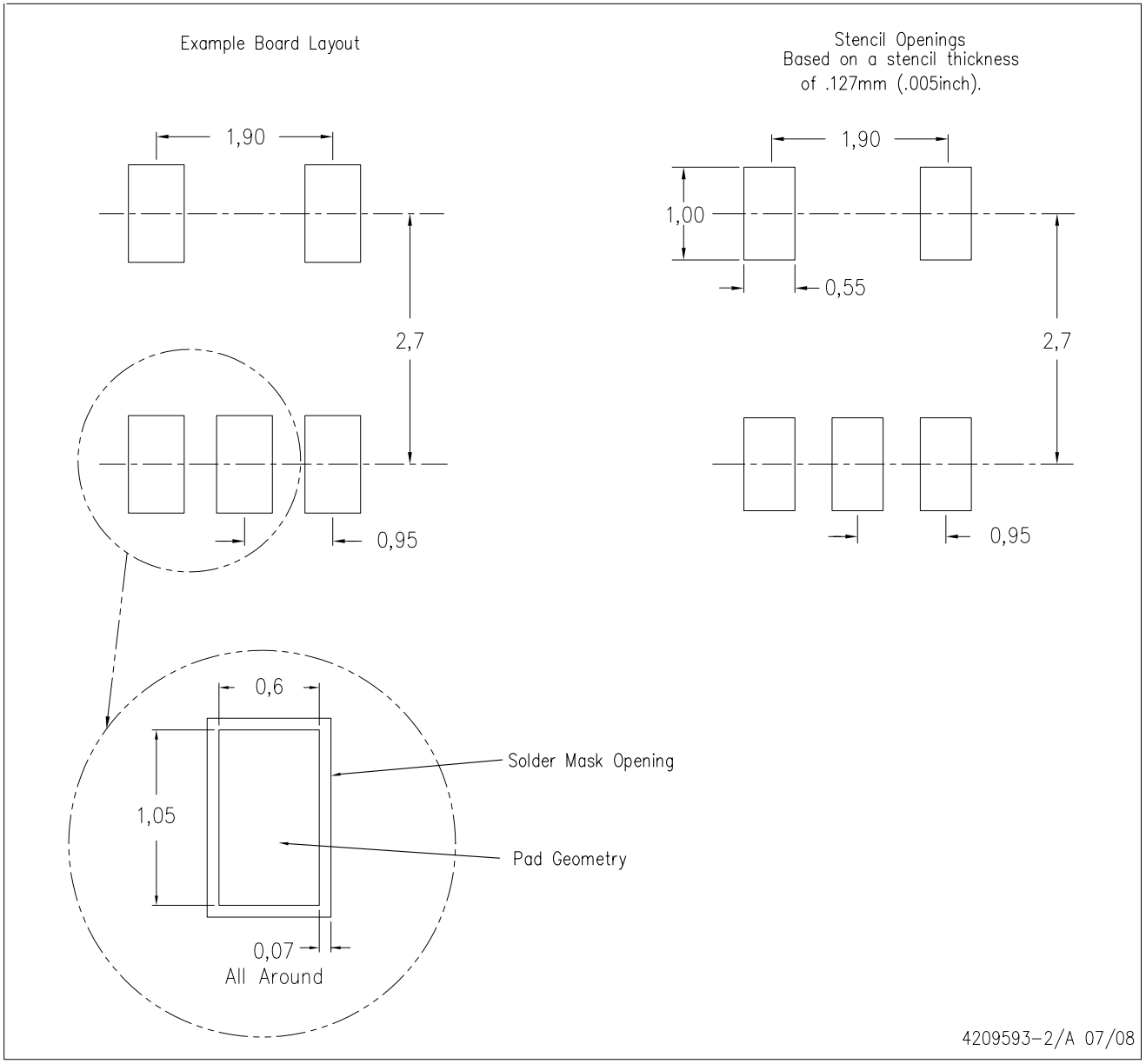
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

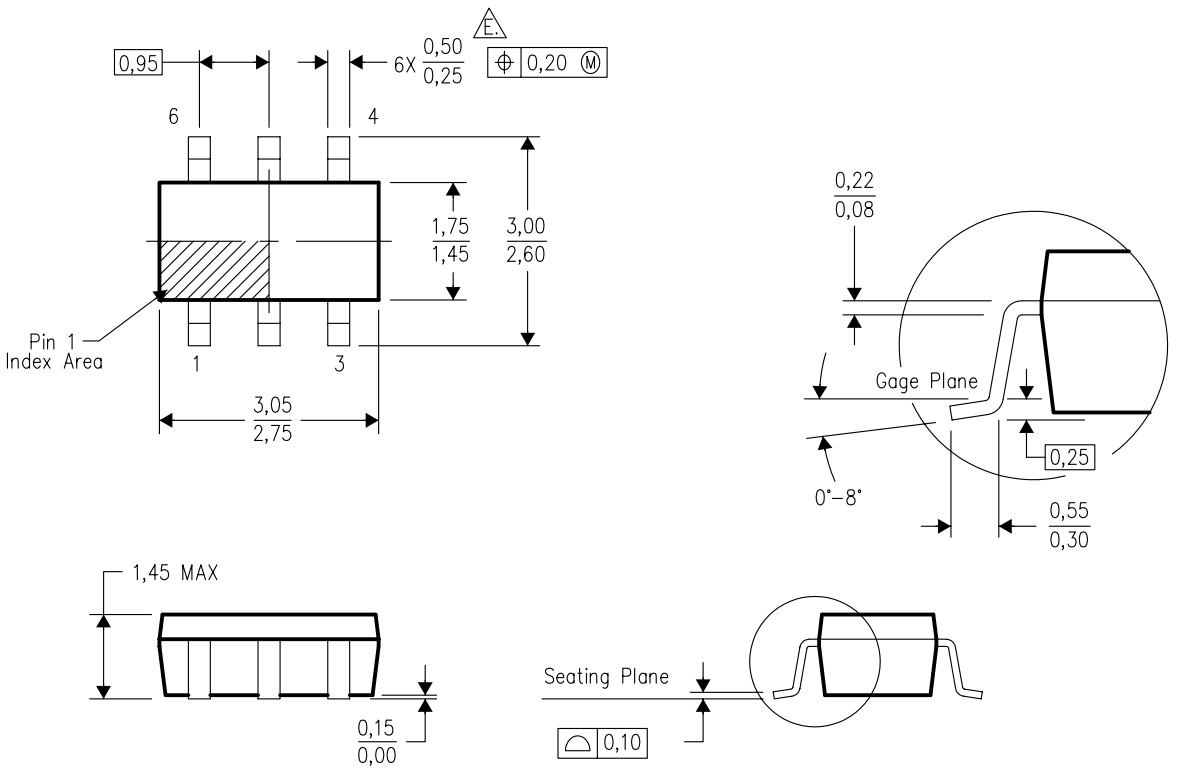
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R-PDSO-G5)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

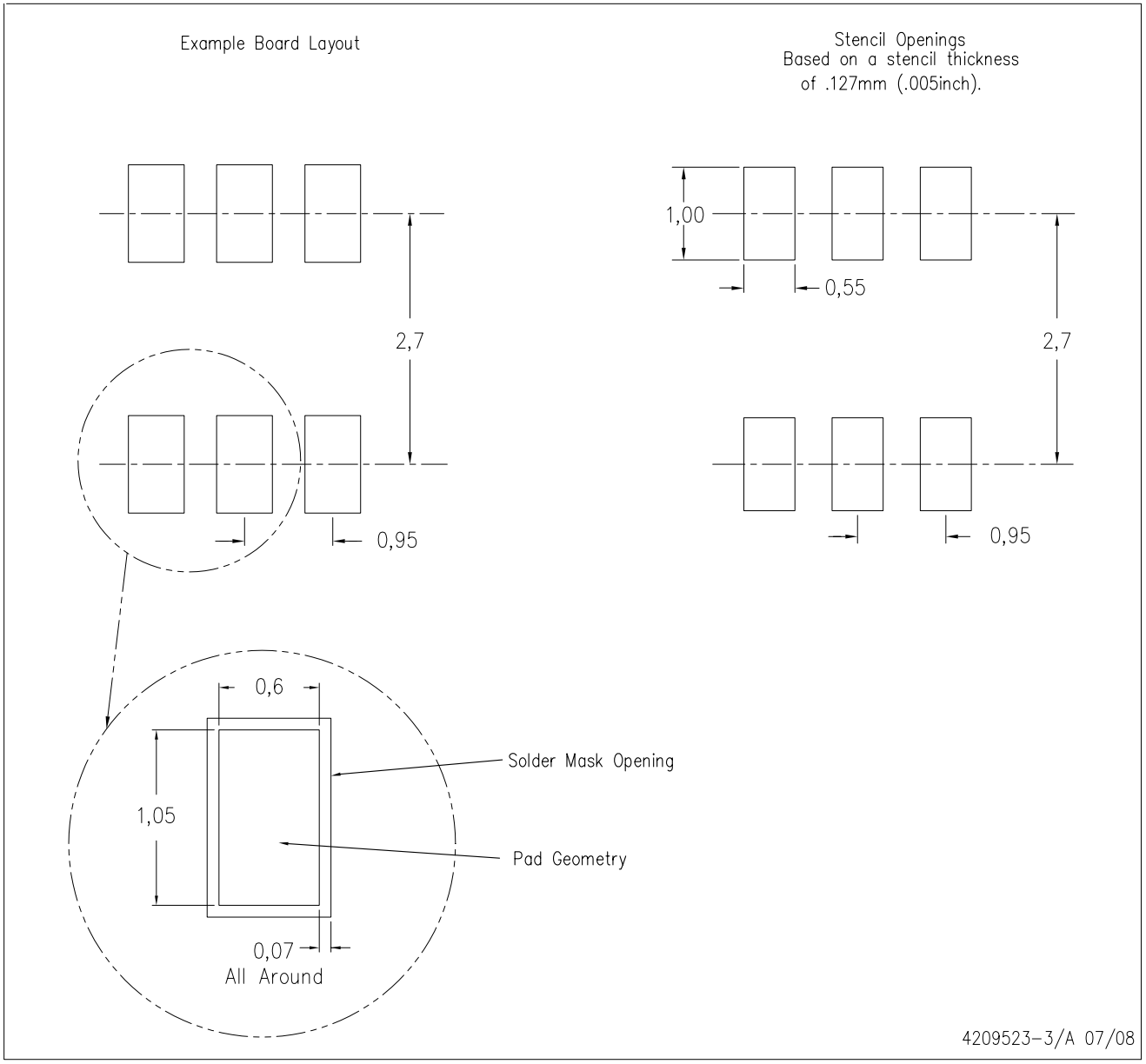
DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4073253–5/K 03/2006

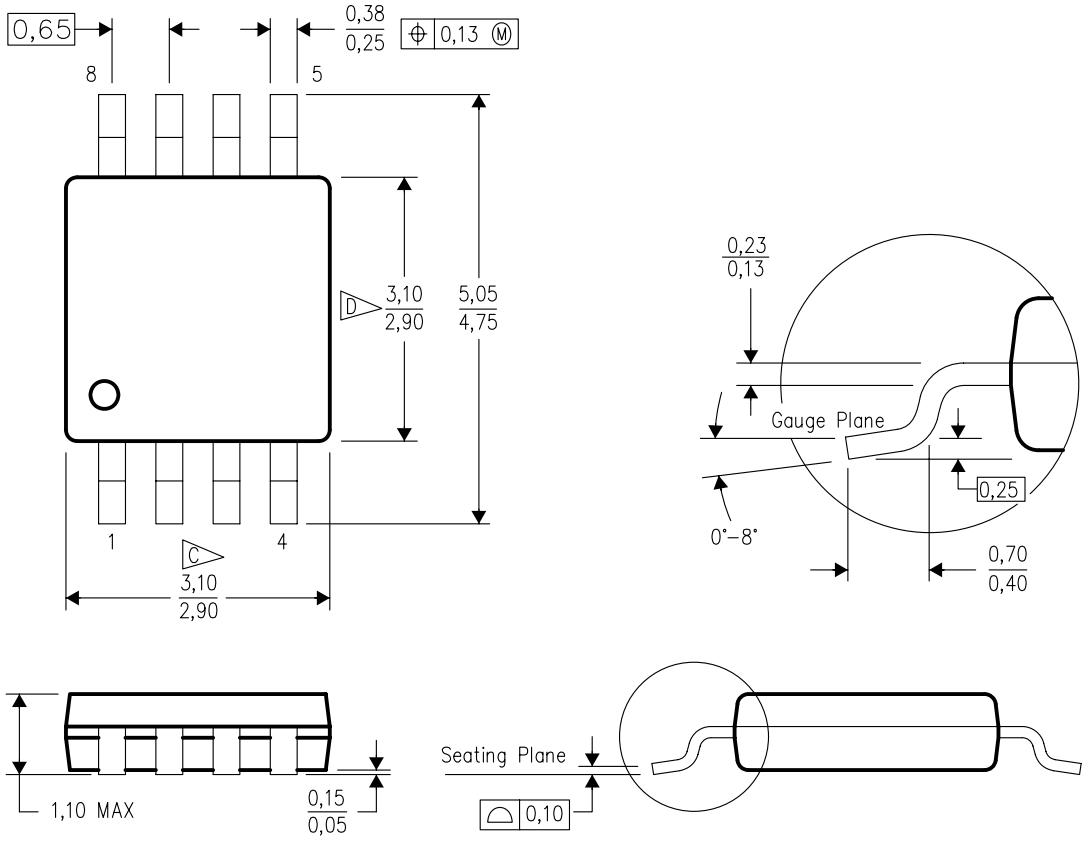
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

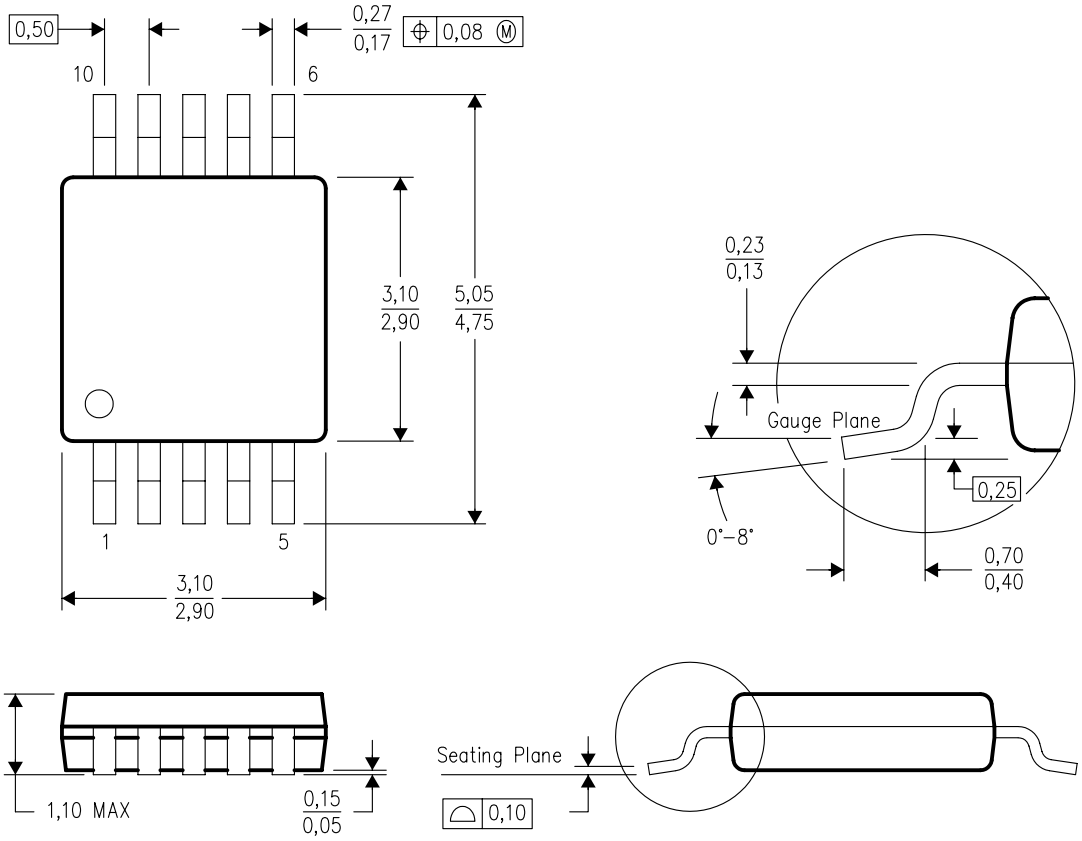
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

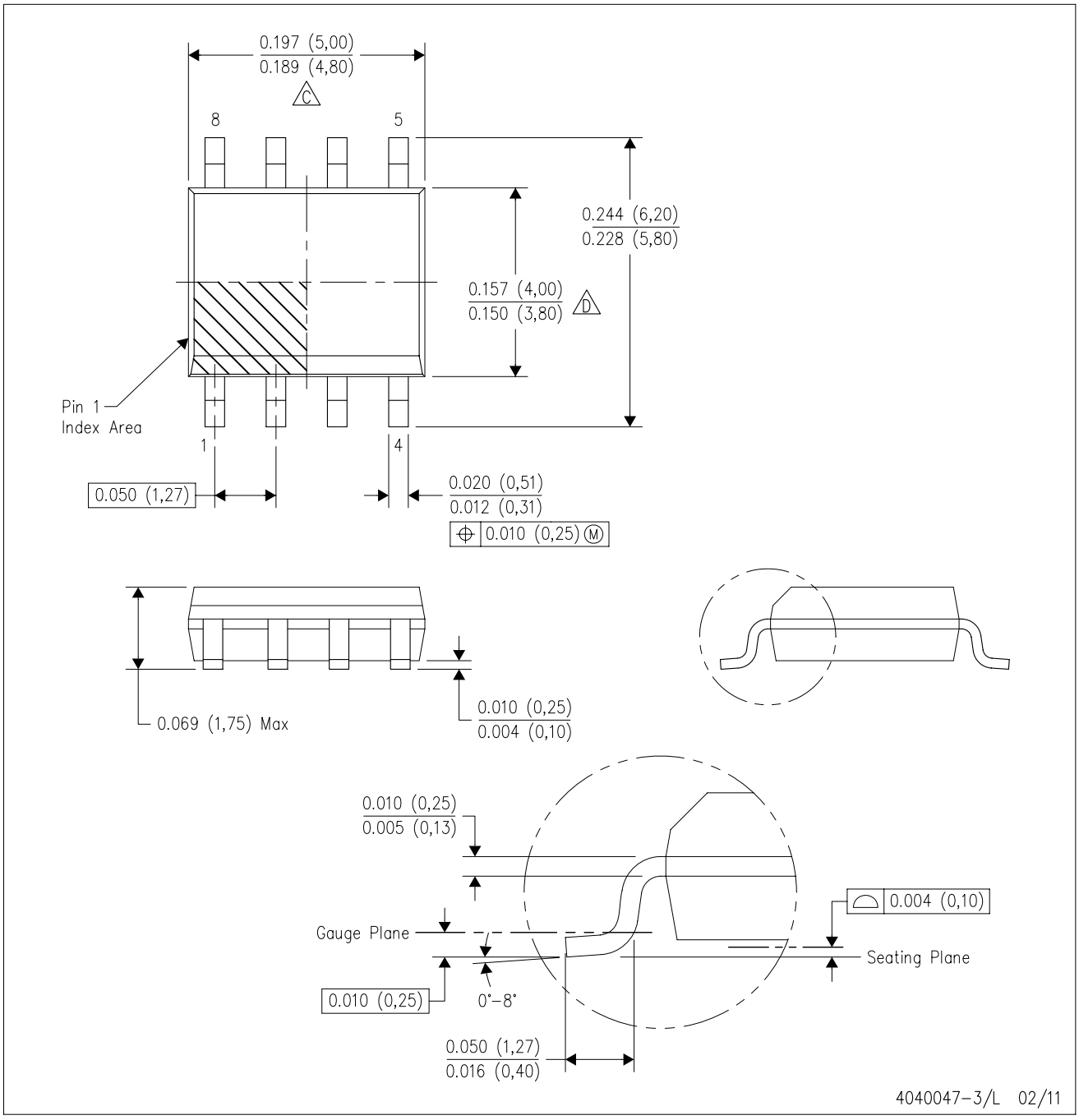
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

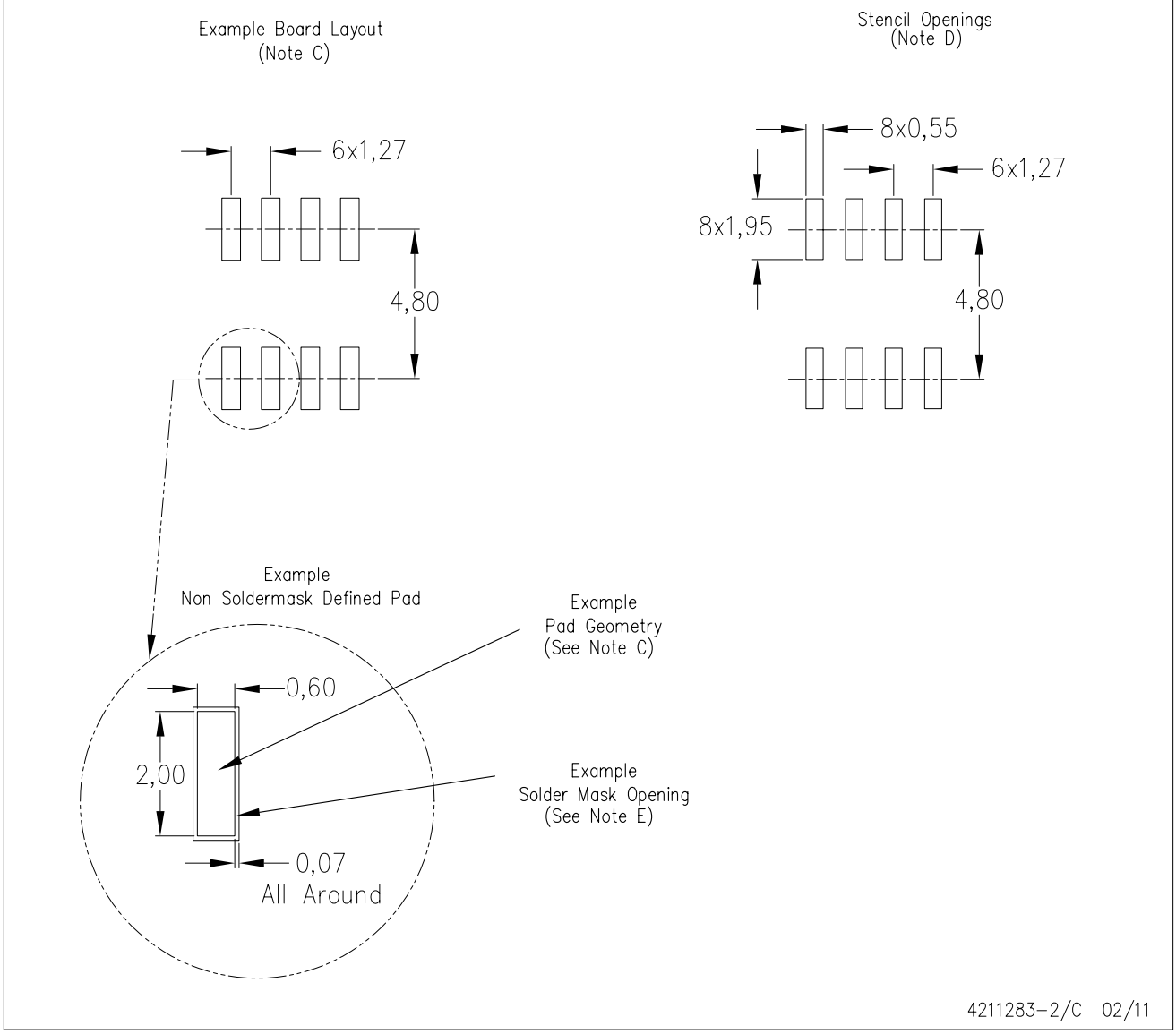
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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RF/IF and ZigBee® Solutions	www.ti.com/lprf		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

10GHz GBW, 1.1nV/√Hz Differential Amplifier/ADC Driver

FEATURES

- **10GHz Gain-Bandwidth Product**
- **88dB SFDR at 100MHz, $2V_{P-P}$**
- **1.1nV/√Hz Input Noise Density**
- Input Range Includes Ground
- External Resistors Set Gain (Min 1V/V)
- 3300V/µs Differential Slew Rate
- 52mA Supply Current
- 2.7V to 5.25V Supply Voltage Range
- Fully Differential Input and Output
- Adjustable Output Common Mode Voltage
- Low Power Shutdown
- Small 10-Lead 3mm × 2mm × 0.75mm QFN Package

APPLICATIONS

- Differential Pipeline ADC Driver
- High-Speed Data-Acquisition Cards
- Automated Test Equipment
- Time Domain Reflexometry
- Communications Receivers

DESCRIPTION

The LTC®6409 is a very high speed, low distortion, differential amplifier. Its input common mode range includes ground, so that a ground-referenced input signal can be DC-coupled, level-shifted, and converted to drive an ADC differentially.

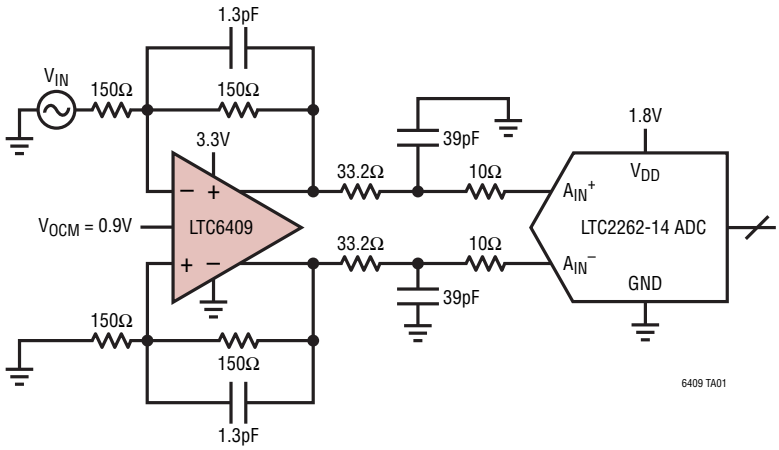
The gain and feedback resistors are external, so that the exact gain and frequency response can be tailored to each application. For example, the amplifier could be externally compensated in a no-overshoot configuration, which is desired in certain time-domain applications.

The LTC6409 is stable in a differential gain of 1. This allows for a low output noise in applications where gain is not desired. It draws 52mA of supply current and has a hardware shutdown feature which reduces current consumption to 100µA.

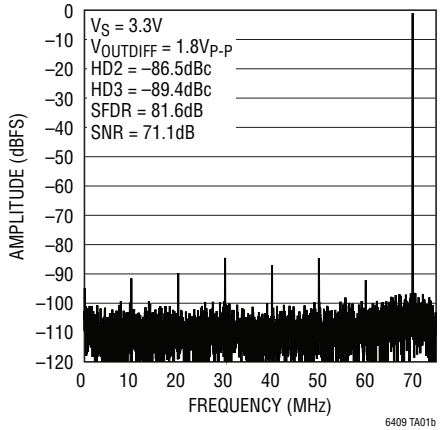
The LTC6409 is available in a compact 3mm × 2mm 10-pin leadless QFN package and operates over a –40°C to 125°C temperature range.

TYPICAL APPLICATION

DC-Coupled Interface from a Ground-Referenced Single-Ended Input to an LTC2262-14 ADC



LTC6409 Driving LTC2262-14 ADC, f_{IN} = 70MHz, –1dBFS, f_S = 150MHz, 4096-Point FFT

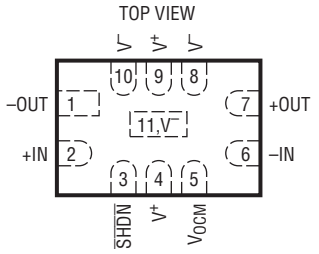


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage ($V^+ – V^–$) 5.5V
Input Current (+IN, –IN, V_{OCM}, $\overline{SHDN}$)
(Note 2).....±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range
(Note 4).....–40°C to 125°C
Specified Temperature Range
(Note 5).....–40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UDB PACKAGE
10-LEAD (3mm × 2mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 138°C/W, θ_{JC} = 5.2°C/W
EXPOSED PAD (PIN 11) CONNECTED TO $V^–$

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6409CUDB#TRMPBF	LTC6409CUDB#TRPBF	LFPF	10-Lead (3mm × 2mm) Plastic QFN	0°C to 70°C
LTC6409IUDB#TRMPBF	LTC6409IUDB#TRPBF	LFPF	10-Lead (3mm × 2mm) Plastic QFN	–40°C to 85°C
LTC6409HUDB#TRMPBF	LTC6409HUDB#TRPBF	LFPF	10-Lead (3mm × 2mm) Plastic QFN	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, $V^–$ = 0V, $V_{CM} = V_{OCM} = V_{ICM}$ = 1.25V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ – V^–$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OSDIFF}	Differential Offset Voltage (Input Referred)	V_S = 3V V_S = 3V V_S = 5V V_S = 5V	 ● ●		±300 ±300 	±1000 ±1200 ±1100 ±1400	µV µV µV µV
$\frac{\Delta V_{OSDIFF}}{\Delta T}$	Differential Offset Voltage Drift (Input Referred)	V_S = 3V V_S = 5V	● ●		2 2		µV/°C µV/°C
I_B	Input Bias Current (Note 6)	V_S = 3V V_S = 5V	● ●	–140 –160	–62 –70	0 0	µA µA
I_{OS}	Input Offset Current (Note 6)	V_S = 3V V_S = 5V	● ●		±2 ±2	±10 ±10	µA µA
R_{IN}	Input Resistance	Common Mode Differential Mode			165 860		kΩ Ω
C_{IN}	Input Capacitance	Differential Mode			0.5		pF
e_n	Differential Input Noise Voltage Density	f = 1MHz, Not Including R_I/R_F Noise			1.1		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1MHz, Not Including R_I/R_F Noise			8.8		$pA/\sqrt{Hz}$
NF	Noise Figure at 100MHz	Shunt-Terminated to 50Ω, R_S = 50Ω, R_I = 25Ω, R_F = 10kΩ			6.9		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 1.25V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{-OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{-IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} - V_{-OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
e_{nVOCM}	Common Mode Noise Voltage Density	f = 10MHz			12		nV/√Hz
V_{ICMR} (Note 7)	Input Signal Common Mode Range	V_S = 3V V_S = 5V	● ●	0 0		1.5 3.5	V V
CMRRI (Note 8)	Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{ICM}/\Delta V_{OSDIFF}$	V_S = 3V, V_{ICM} from 0V to 1.5V V_S = 5V, V_{ICM} from 0V to 3.5V	● ●	75 75	90 90		dB dB
CMRRIO (Note 8)	Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$	V_S = 3V, V_{OCM} from 0.5V to 1.5V V_S = 5V, V_{OCM} from 0.5V to 3.5V	● ●	55 60	80 85		dB dB
PSRR (Note 9)	Differential Power Supply Rejection ($\Delta V_S/\Delta V_{OSDIFF}$)	V_S = 2.7V to 5.25V	●	60	85		dB
PSRRCM (Note 9)	Output Common Mode Power Supply Rejection ($\Delta V_S/\Delta V_{OSCM}$)	V_S = 2.7V to 5.25V	●	55	70		dB
V_S	Supply Voltage Range (Note 10)		●	2.7		5.25	V
G_{CM}	Common Mode Gain ($\Delta V_{OUTCM}/\Delta V_{OCM}$)	V_S = 3V, V_{OCM} from 0.5V to 1.5V V_S = 5V, V_{OCM} from 0.5V to 3.5V	● ●		1 1		V/V V/V
ΔG_{CM}	Common Mode Gain Error, 100 × (G_{CM} – 1)	V_S = 3V, V_{OCM} from 0.5V to 1.5V V_S = 5V, V_{OCM} from 0.5V to 3.5V	● ●		±0.1 ±0.1	±0.3 ±0.3	% %
BAL	Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$)	$\Delta V_{OUTDIFF}$ = 2V Single-Ended Input Differential Input	 ● ●		 –65 –70	 –50 –50	 dB dB
V_{OSCM}	Common Mode Offset Voltage ($V_{OUTCM} - V_{OCM}$)	V_S = 3V V_S = 5V	● ●		±1 ±1	±5 ±6	mV mV
$\frac{\Delta V_{OSCM}}{\Delta T}$	Common Mode Offset Voltage Drift		●		4		µV/°C
V_{OUTCMR} (Note 7)	Output Signal Common Mode Range (Voltage Range for the V_{OCM} Pin)	V_S = 3V V_S = 5V	● ●	0.5 0.5		1.5 3.5	V V
R_{INVOCM}	Input Resistance, V_{OCM} Pin		●	30	40	50	KΩ
V_{OCM}	Self-Biased Voltage at the V_{OCM} Pin	V_S = 3V, V_{OCM} = Open V_S = 5V, V_{OCM} = Open	 ●	 0.9	0.85 1.25	 1.6	V V
V_{OUT}	Output Voltage, High, Either Output Pin	V_S = 3V, I_L = 0 V_S = 3V, I_L = –20mA V_S = 5V, I_L = 0 V_S = 5V, I_L = –20mA	● ● ● ●	1.85 1.8 3.85 3.8	2 1.95 4 3.95		V V V V
	Output Voltage, Low, Either Output Pin	V_S = 3V, 5V; I_L = 0 V_S = 3V, 5V; I_L = 20mA	● ●		0.06 0.2	0.15 0.4	V V
I_{SC}	Output Short-Circuit Current, Either Output Pin (Note 11)	V_S = 3V V_S = 5V	● ●	±50 ±70	±70 ±95		mA mA
A_{VOL}	Large-Signal Open Loop Voltage Gain				65		dB
I_S	Supply Current		 ●		52	56 58	mA mA
$I_{\overline{SHDN}}$	Supply Current in Shutdown	$V_{\overline{SHDN}} \le 0.6V$	●		100	500	µA
$R_{\overline{SHDN}}$	$\overline{SHDN}$ Pull-Up Resistor	$V_{\overline{SHDN}}$ = 0V to 0.5V	●	115	150	185	KΩ
V_{IL}	$\overline{SHDN}$ Input Logic Low		●			0.6	V
V_{IH}	$\overline{SHDN}$ Input Logic High		●	1.4			V
t_{ON}	Turn-On Time				160		ns
t_{OFF}	Turn-Off Time				80		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 1.25V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{-OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{-IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} - V_{-OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SR	Slew Rate	Differential Output, $V_{OUTDIFF}$ = $4V_{P-P}$ +OUT Rising (–OUT Falling) +OUT Falling (–OUT Rising)			3300 1720 1580		V/µs V/µs V/µs
GBW	Gain-Bandwidth Product	R_I = 25Ω, R_F = 10kΩ, f_{TEST} = 100MHz	 ●	9.5 8	10		GHz GHz
f_{-3dB}	–3dB Frequency	R_I = R_F = 150Ω, R_{LOAD} = 400Ω, C_F = 1.3pF			2		GHz
$f_{0.1dB}$	Frequency for 0.1dB Flatness	R_I = R_F = 150Ω, R_{LOAD} = 400Ω , C_F = 1.3pF			600		MHz
FPBW	Full Power Bandwidth	$V_{OUTDIFF}$ = $2V_{P-P}$			550		MHz
HD2 HD3	25MHz Distortion	Differential Input, $V_{OUTDIFF}$ = $2V_{P-P}$, R_I = R_F = 150Ω, R_{LOAD} = 400Ω 2nd Harmonic 3rd Harmonic			 –104 –106		 dBc dBc
	100MHz Distortion	Differential Input, $V_{OUTDIFF}$ = $2V_{P-P}$, R_I = R_F = 150Ω, R_{LOAD} = 400Ω 2nd Harmonic 3rd Harmonic			 –93 –88		 dBc dBc
HD2 HD3	25MHz Distortion	Single-Ended Input, $V_{OUTDIFF}$ = $2V_{P-P}$, R_I = R_F = 150Ω, R_{LOAD} = 400Ω 2nd Harmonic 3rd Harmonic			 –101 –103		 dBc dBc
	100MHz Distortion	Single-Ended Input, $V_{OUTDIFF}$ = $2V_{P-P}$, R_I = R_F = 150Ω, R_{LOAD} = 400Ω 2nd Harmonic 3rd Harmonic			 –88 –93		 dBc dBc
IMD3	3rd Order IMD at 25MHz f1 = 24.9MHz, f2 = 25.1MHz	$V_{OUTDIFF}$ = $2V_{P-P}$ Envelope, R_I = R_F = 150Ω, R_{LOAD} = 400Ω			–110		dBc
	3rd Order IMD at 100MHz f1 = 99.9MHz, f2 = 100.1MHz	$V_{OUTDIFF}$ = $2V_{P-P}$ Envelope, R_I = R_F = 150Ω, R_{LOAD} = 400Ω			–98		dBc
	3rd Order IMD at 140MHz f1 = 139.9MHz, f2 = 140.1MHz	$V_{OUTDIFF}$ = $2V_{P-P}$ Envelope, R_I = R_F = 150Ω, R_{LOAD} = 400Ω			–88		dBc
OIP3	Equivalent OIP3 at 25MHz (Note 12) Equivalent OIP3 at 100MHz (Note 12) Equivalent OIP3 at 140MHz (Note 12)				59 53 48		dBm dBm dBm
t_S	Settling Time	$V_{OUTDIFF}$ = $2V_{P-P}$ Step, R_I = R_F = 150Ω, R_{LOAD} = 400Ω 1% Settling			 1.9		 ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input pins (+IN, –IN, V_{OCM}, and $\overline{SHDN}$) are protected by steering diodes to either supply. If the inputs should exceed either supply voltage, the input current should be limited to less than 10mA. In addition, the inputs +IN, –IN are protected by a pair of back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LTC6409C/LTC6409I are guaranteed functional over the temperature range of –40°C to 85°C. The LTC6409H is guaranteed functional over the temperature range of –40°C to 125°C.

Note 5: The LTC6409C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6409C is designed, characterized and expected to meet specified performance from –40°C to 85°C, but is not tested or QA sampled at these temperatures. The LTC6409I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6409H is guaranteed to meet specified performance from –40°C to 125°C.

Note 6: Input bias current is defined as the average of the input currents flowing into the inputs (–IN and +IN). Input offset current is defined as the difference between the input currents (I_{OS} = $I_B^+ - I_B^-$).

ELECTRICAL CHARACTERISTICS

Note 7: Input common mode range is tested by testing at both V_{ICM} = 1.25V and at the Electrical Characteristics table limits to verify that the differential offset (V_{OSDIFF}) and the common mode offset (V_{OSCM}) have not deviated by more than ±1mV and ±2mV respectively from the V_{ICM} = 1.25V case.

The voltage range for the output common mode range is tested by applying a voltage on the V_{OCM} pin and testing at both V_{OCM} = 1.25V and at the Electrical Characteristics table limits to verify that the common mode offset (V_{OSCM}) has not deviated by more than ±6mV from the V_{OCM} = 1.25V case.

Note 8: Input CMRR is defined as the ratio of the change in the input common mode voltage at the pins +IN or –IN to the change in differential input referred offset voltage. Output CMRR is defined as the ratio of the change in the voltage at the V_{OCM} pin to the change in differential input referred offset voltage. This specification is strongly dependent on feedback ratio matching between the two outputs and their respective inputs and it is difficult to measure actual amplifier performance (See Effects of Resistor Pair Mismatch in the Applications Information section of this data sheet). For a better indicator of actual amplifier performance independent of feedback component matching, refer to the PSRR specification.

Note 9: Differential power supply rejection (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred offset voltage. Common mode power supply rejection (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the output common mode offset voltage.

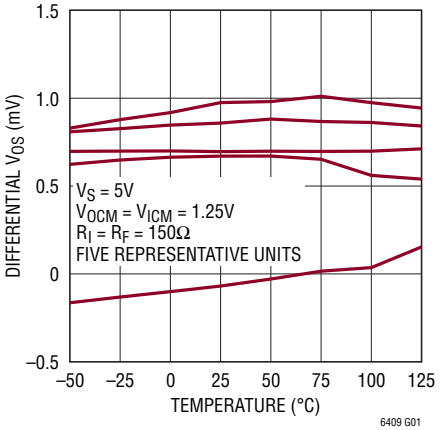
Note 10: Supply voltage range is guaranteed by power supply rejection ratio test.

Note 11: Extended operation with the output shorted may cause the junction temperature to exceed the 150°C limit.

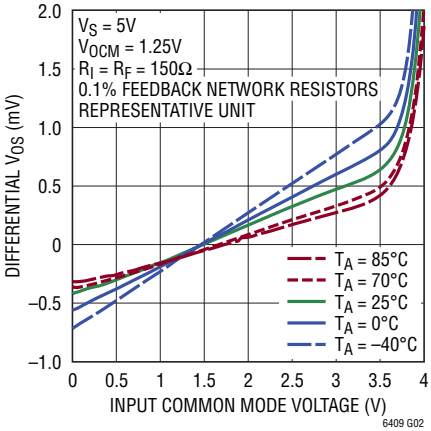
Note 12: Refer to Relationship Between Different Linearity Metrics in the Applications Information section of this data sheet for information on how to calculate an equivalent OIP3 from IMD3 measurements.

TYPICAL PERFORMANCE CHARACTERISTICS

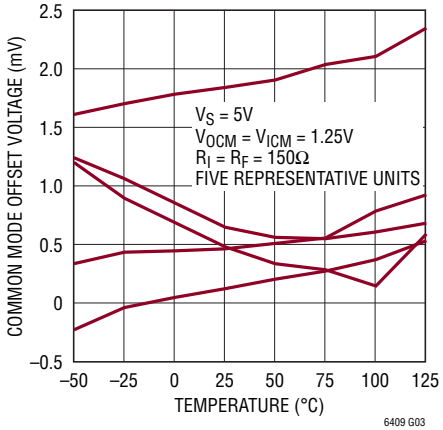
Differential Input Offset Voltage vs Temperature



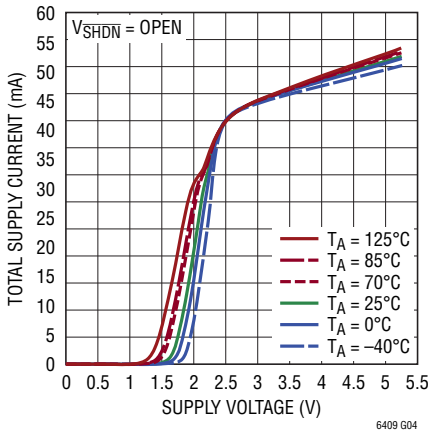
Differential Input Offset Voltage vs Input Common Mode Voltage



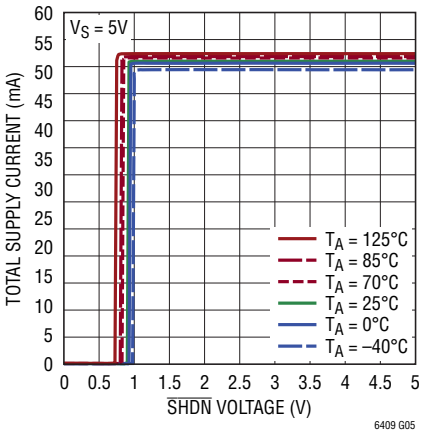
Common Mode Offset Voltage vs Temperature



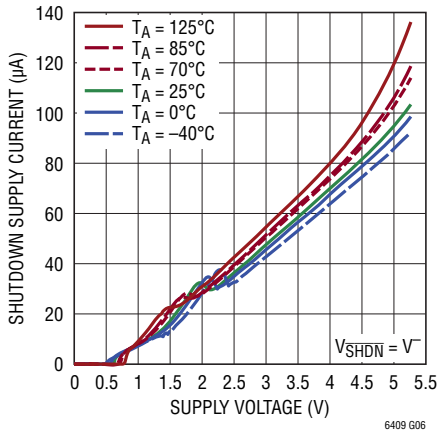
Supply Current vs Supply Voltage



Supply Current vs $\overline{SHDN}$ Voltage

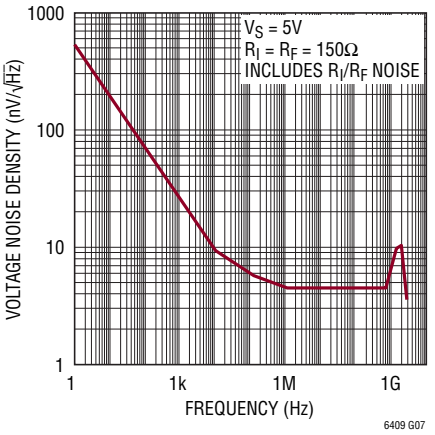


Shutdown Supply Current vs Supply Voltage

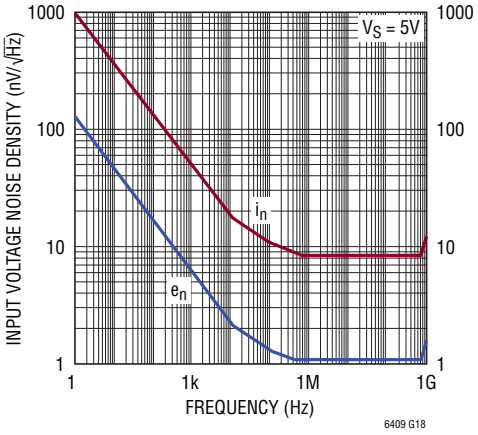


TYPICAL PERFORMANCE CHARACTERISTICS

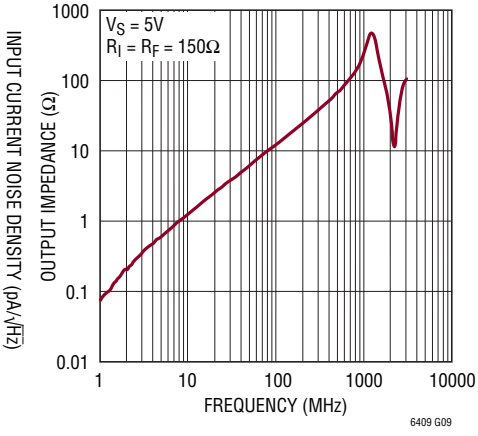
Differential Output Voltage Noise vs Frequency



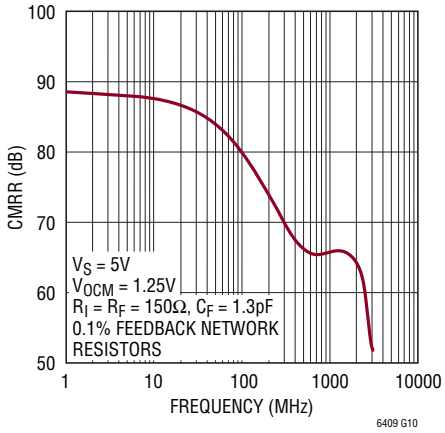
Input Noise Density vs Frequency



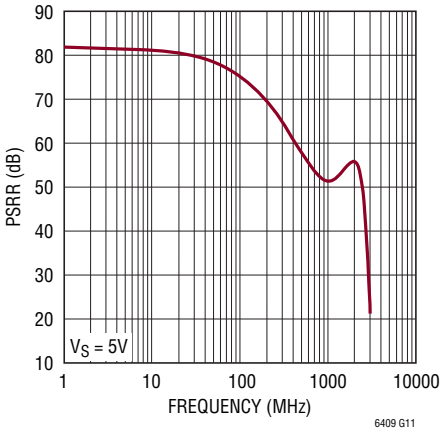
Differential Output Impedance vs Frequency



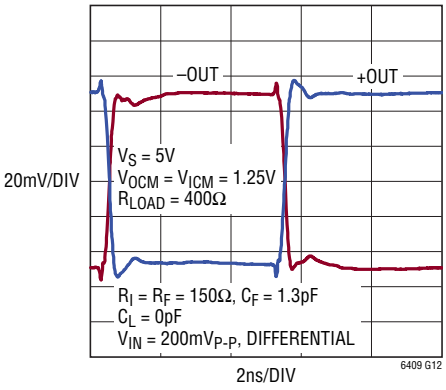
CMRR vs Frequency



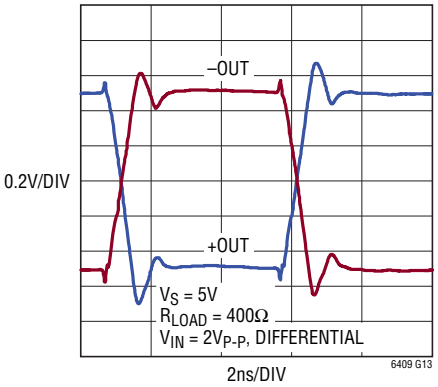
Differential PSRR vs Frequency



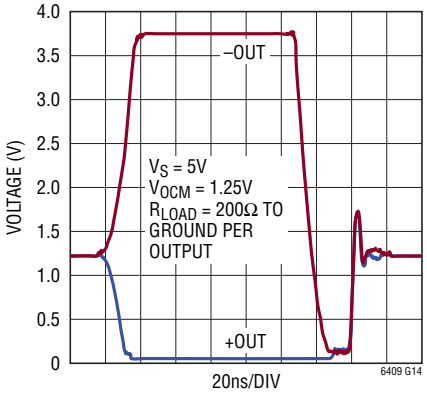
Small Signal Step Response



Large Signal Step Response

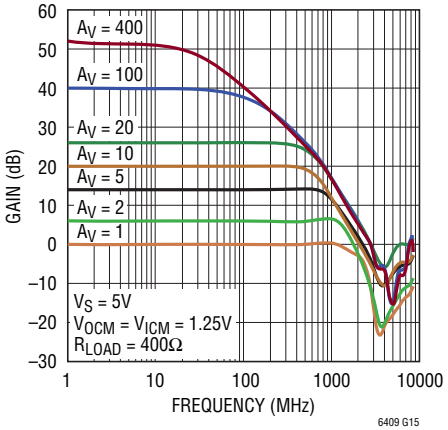


Overdriven Output Transient Response



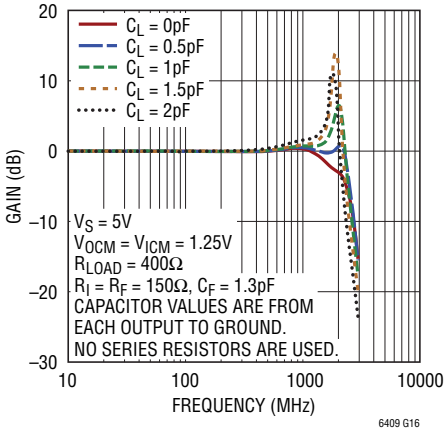
TYPICAL PERFORMANCE CHARACTERISTICS

Frequency Response vs Closed Loop Gain

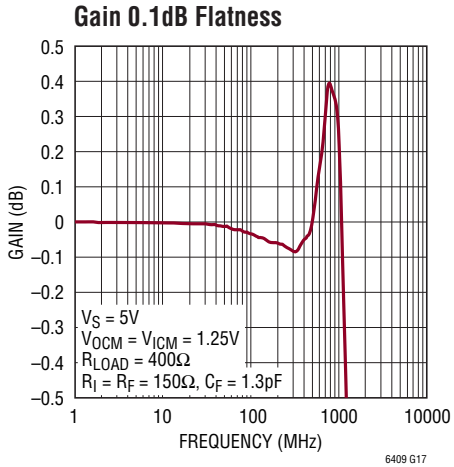


A_V (V/V)	R_I (Ω)	R_F (Ω)	C_F (pF)
1	150	150	1.3
2	100	200	1
5	50	250	0.8
10	50	500	0.4
20	25	500	0.4
100	25	2.5k	0
400	25	10k	0

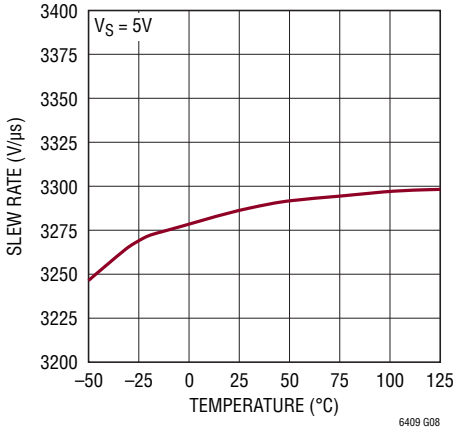
Frequency Response vs Load Capacitance



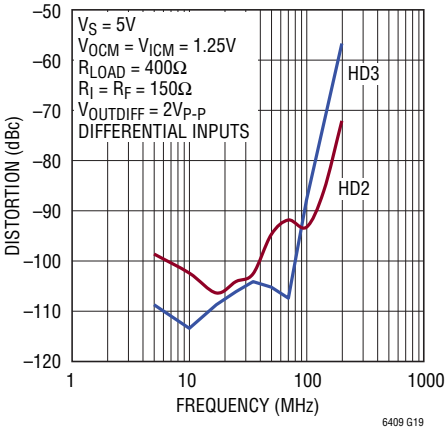
Gain 0.1dB Flatness



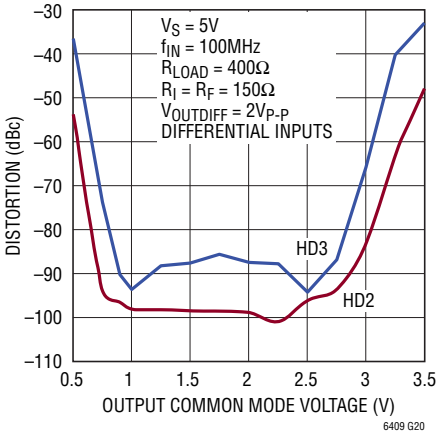
Slew Rate vs Temperature



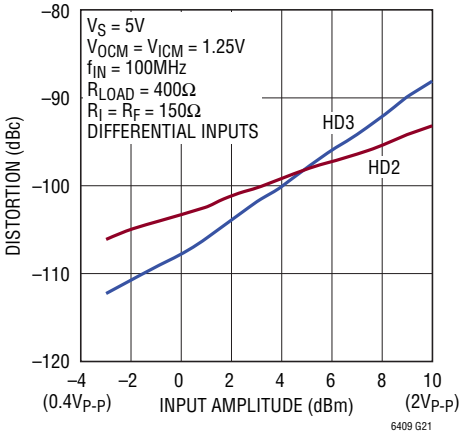
Harmonic Distortion vs Frequency



Harmonic Distortion vs Output Common Mode Voltage

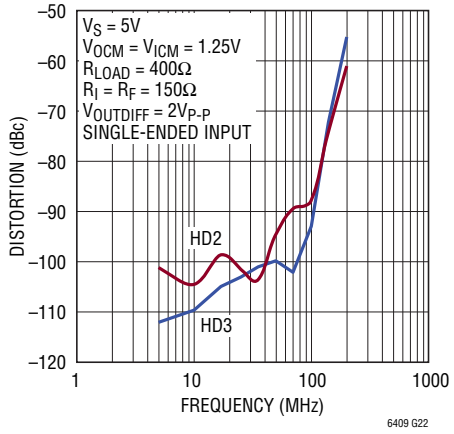


Harmonic Distortion vs Input Amplitude

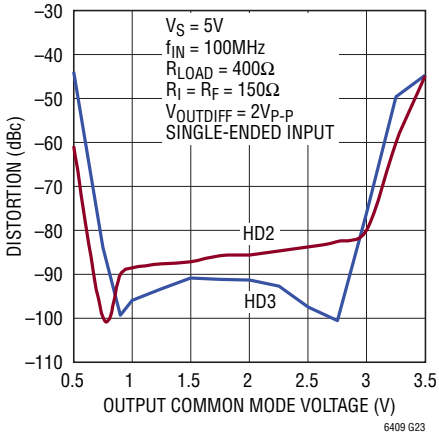


TYPICAL PERFORMANCE CHARACTERISTICS

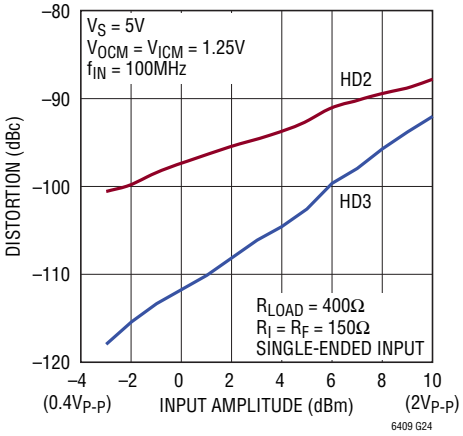
Harmonic Distortion vs Frequency



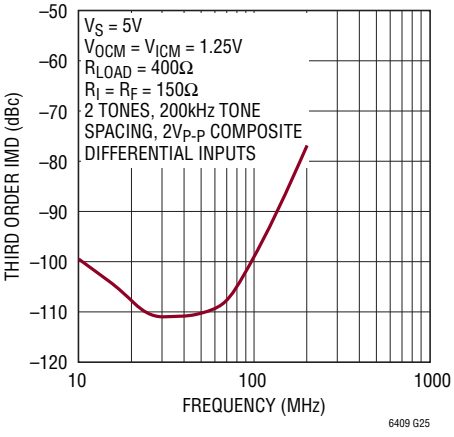
Harmonic Distortion vs Output Common Mode Voltage



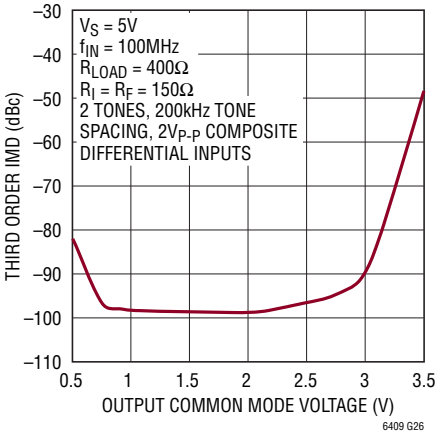
Harmonic Distortion vs Input Amplitude



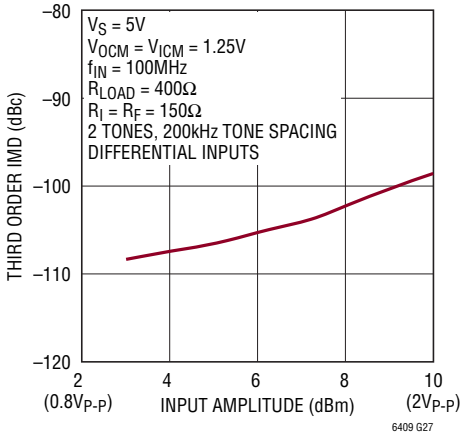
Intermodulation Distortion vs Frequency



Intermodulation Distortion vs Output Common Mode Voltage



Intermodulation Distortion vs Input Amplitude



PIN FUNCTIONS

+IN, –IN (Pins 2, 6): Non-Inverting and Inverting Input Pins.

$\overline{\text{SHDN}}$ (Pin 3): When $\overline{\text{SHDN}}$ is floating or directly tied to V^+, the LTC6409 is in the normal (active) operating mode. When the $\overline{\text{SHDN}}$ pin is connected to V^-, the part is disabled and draws approximately 100µA of supply current.

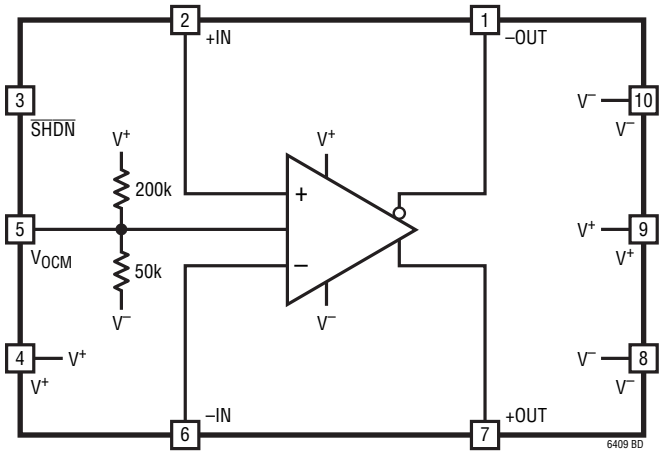
V^+, V^- (Pins 4, 9 and Pins 8, 10): Positive and Negative Power Supply Pins. Similar pins should be connected to the same voltage.

V_{OCM} (Pin 5): Output Common Mode Reference Voltage. The voltage on this pin sets the output common mode voltage level. If left floating, an internal resistor divider develops a default voltage of 1.25V with a 5V supply.

+OUT, –OUT (Pins 7, 1): Differential Output Pins.

Exposed Pad (Pin 11): Tie the bottom pad to V^-. If split supplies are used, DO NOT tie the pad to ground.

BLOCK DIAGRAM



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Functional Description

The LTC6409 is a small outline, wideband, high speed, low noise, and low distortion fully-differential amplifier with accurate output phase balancing. The amplifier is optimized to drive low voltage, single-supply, differential input analog-to-digital converters (ADCs). The LTC6409 input common mode range includes ground, which makes it ideal to DC-couple and convert ground-referenced, single-ended signals into differential signals that are referenced to the user-supplied output common mode voltage. This is ideal for driving these differential ADCs. The balanced differential nature of the amplifier also provides even-order harmonic distortion cancellation, and low susceptibility to common mode noise (like power supply noise). The LTC6409 can operate with a single-ended input and differential output, or with a differential input and differential output.

The outputs of the LTC6409 are capable of swinging from close-to-ground to 1V below V^+. They can source or sink up to approximately 70mA of current. Load capacitances should be decoupled with at least 10Ω of series resistance from each output.

Input Pin Protection

The LTC6409 input stage is protected against differential input voltages which exceed 1.4V by two pairs of series diodes connected back to back between +IN and –IN. Moreover, the input pins, as well as V_{OCM} and $\overline{SHDN}$ pins, have clamping diodes to either power supply. If these pins are driven to voltages which exceed either supply, the current should be limited to 10mA to prevent damage to the IC.

$\overline{SHDN}$ Pin

The $\overline{SHDN}$ pin is a CMOS logic input with a 150k internal pull-up resistor. If the pin is driven low, the LTC6409 powers down. If the pin is left unconnected or driven high, the part is in normal active operation. Some care should be taken to control leakage currents at this pin to prevent inadvertently putting the LTC6409 into shutdown. The turn-on and turn-off time between the shutdown and active states is typically less than 200ns.

General Amplifier Applications

In Figure 1, the gain to $V_{OUTDIFF}$ from V_{INP} and V_{INM} is given by:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx \frac{R_F}{R_I} \bullet \left(V_{INP} - V_{INM}\right) \quad (1)$$

Note from Equation (1), the differential output voltage (V_{+OUT} – V_{-OUT}) is completely independent of input and output common mode voltages, or the voltage at the common mode pin. This makes the LTC6409 ideally

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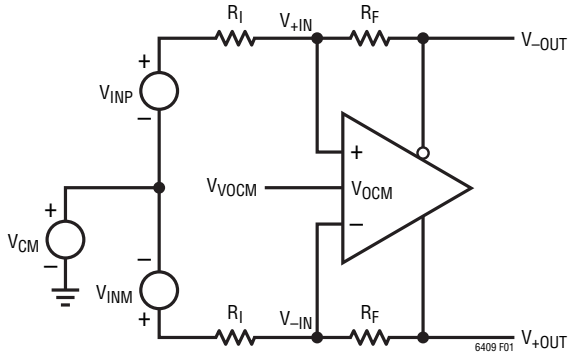

Figure 1. Circuit for Common Mode Range

suited for pre-amplification, level shifting and conversion of single-ended signals to differential output signals for driving differential input ADCs.

Output Common Mode and V_{OCM} Pin

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = V_{OCM} = \frac{V_{+OUT} + V_{-OUT}}{2}$$

As the equation shows, the output common mode voltage is independent of the input common mode voltage, and is instead determined by the voltage on the V_{OCM} pin, by means of an internal common mode feedback loop.

If the V_{OCM} pin is left open, an internal resistor divider develops a default voltage of 1.25V with a 5V supply. The V_{OCM} pin can be overdriven to another voltage if desired. For example, when driving an ADC, if the ADC makes a reference available for setting the common mode voltage, it can be directly tied to the V_{OCM} pin, as long as the ADC is capable of driving the 40k input resistance presented by the V_{OCM} pin. The Electrical Characteristics table specifies the valid range that can be applied to the V_{OCM} pin (V_{OUTCMR}).

Input Common Mode Voltage Range

The LTC6409's input common mode voltage (V_{ICM}) is defined as the average of the two input pins, V_{+IN} and V_{-IN}. The valid range that can be used for V_{ICM} has been specified in the Electrical Characteristics table (V_{ICMR}). However, due to external resistive divider action of the gain and feedback resistors, the effective range of signals that can be processed is even wider. The input common mode range at the op amp inputs depends on the circuit configuration (gain), V_{OCM} and V_{CM} (refer to Figure 1). For fully differential input applications, where $V_{INP} = -V_{INM}$, the common mode input is approximately:

$$V_{ICM} = \frac{V_{+IN} + V_{-IN}}{2} \approx V_{OCM} \bullet \frac{R_I}{R_I + R_F} + V_{CM} \bullet \frac{R_F}{R_I + R_F}$$

With single-ended inputs, there is an input signal component to the input common mode voltage. Applying only V_{INP} (setting V_{INM} to zero), the input common mode voltage is approximately:

$$V_{ICM} = \frac{V_{+IN} + V_{-IN}}{2} \approx V_{OCM} \bullet \frac{R_I}{R_I + R_F} + \quad (2)$$

$$V_{CM} \bullet \frac{R_F}{R_I + R_F} + \frac{V_{INP}}{2} \bullet \frac{R_F}{R_I + R_F}$$

This means that if, for example, the input signal (V_{INP}) is a sine, an attenuated version of that sine signal also appears at the op amp inputs.

Input Impedance and Loading Effects

The low frequency input impedance looking into the V_{INP} or V_{INM} input of Figure 1 depends on how the inputs are driven. For fully differential input sources ($V_{INP} = -V_{INM}$), the input impedance seen at either input is simply:

$$R_{INP} = R_{INM} = R_I$$

For single-ended inputs, because of the signal imbalance at the input, the input impedance actually increases over the balanced differential case. The input impedance looking into either input is:

$$R_{INP} = R_{INM} = \frac{R_I}{1 - \frac{1}{2} \bullet \frac{R_F}{R_I + R_F}}$$

Input signal sources with non-zero output impedances can also cause feedback imbalance between the pair of feedback networks. For the best performance, it is recommended that the input source output impedance be compensated. If input impedance matching is required by the source,

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a termination resistor R_T should be chosen (see Figure 2) such that:

$$R_T = \frac{R_{INM} \bullet R_S}{R_{INM} - R_S}$$

According to Figure 2, the input impedance looking into the differential amp (R_{INM}) reflects the single-ended source case, given above. Also, R2 is chosen as:

$$R2 = R_T \,||\, R_S = \frac{R_T \bullet R_S}{R_T + R_S}$$

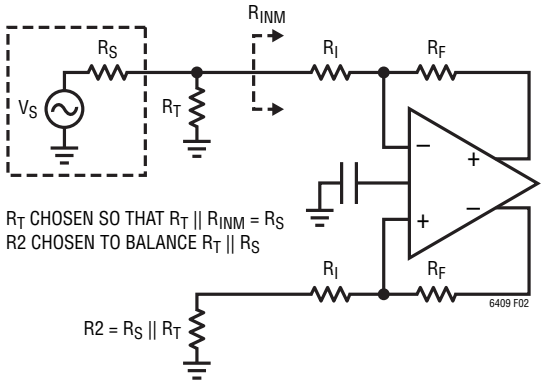

Figure 2. Optimal Compensation for Signal Source Impedance

Effects of Resistor Pair Mismatch

Figure 3 shows a circuit diagram which takes into consideration that real world resistors will not match perfectly. Assuming infinite open loop gain, the differential output relationship is given by the equation:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx V_{INDIFF} \bullet \frac{R_F}{R_I} + V_{CM} \bullet \frac{\Delta\beta}{\beta_{AVG}} - V_{OCM} \bullet \frac{\Delta\beta}{\beta_{AVG}}$$

where R_F is the average of R_{F1}, and R_{F2}, and R_I is the average of R_{I1}, and R_{I2}.

β_{AVG} is defined as the average feedback factor from the outputs to their respective inputs:

$$\beta_{AVG} = \frac{1}{2} \bullet \left(\frac{R_{I1}}{R_{I1} + R_{F1}} + \frac{R_{I2}}{R_{I2} + R_{F2}} \right)$$

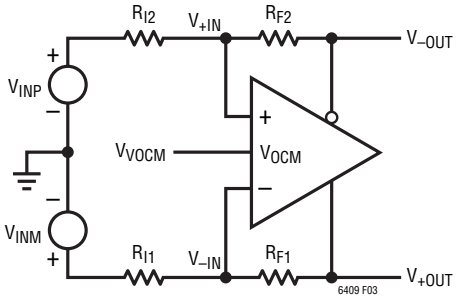

Figure 3. Real-World Application with Feedback Resistor Pair Mismatch

$\Delta\beta$ is defined as the difference in the feedback factors:

$$\Delta\beta = \frac{R_{I2}}{R_{I2} + R_{F2}} - \frac{R_{I1}}{R_{I1} + R_{F1}}$$

Here, V_{CM} and V_{INDIFF} are defined as the average and the difference of the two input voltages V_{INP} and V_{INM}, respectively:

$$V_{CM} = \frac{V_{INP} + V_{INM}}{2}$$

$$V_{INDIFF} = V_{INP} - V_{INM}$$

When the feedback ratios mismatch ($\Delta\beta$), common mode to differential conversion occurs. Setting the differential input to zero ($V_{INDIFF} = 0$), the degree of common mode to differential conversion is given by the equation:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx (V_{CM} - V_{OCM}) \bullet \frac{\Delta\beta}{\beta_{AVG}} \quad (3)$$

In general, the degree of feedback pair mismatch is a source of common mode to differential conversion of both signals and noise. Using 0.1% resistors or better will mitigate most problems and will provide about 54dB worst case of common mode rejection. A low impedance ground plane should be used as a reference for both the input signal source and the V_{OCM} pin.

There may be concern on how feedback factor mismatch affects distortion. Feedback factor mismatch from using 1% resistors or better, has a negligible effect on distortion. However, in single supply level shifting applications where there is a voltage difference between the input common mode voltage and the output common mode voltage,

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resistor mismatch can make the apparent voltage offset of the amplifier appear worse than specified.

The apparent input referred offset induced by feedback factor mismatch is derived from Equation (3):

$V_{OSDIFF(APPARENT)} \approx (V_{CM} - V_{OCM}) \bullet \Delta\beta$

Using the LTC6409 in a single 5V supply application with 0.1% resistors, the input common mode grounded, and the V_{OCM} pin biased at 1.25V, the worst case mismatch can induce 1.25mV of apparent offset voltage.

Noise and Noise Figure

The LTC6409's differential input referred voltage and current noise densities are 1.1nV/√Hz and 8.8pA/√Hz, respectively. In addition to the noise generated by the amplifier, the surrounding feedback resistors also contribute noise. A simplified noise model is shown in Figure 4. The output noise generated by both the amplifier and the feedback components is given by the equation:

$$e_{no} = \sqrt{\left[e_{ni} \bullet \left(1 + \frac{R_F}{R_I}\right)\right]^2 + 2 \bullet \left(i_n \bullet R_F\right)^2 + 2 \bullet \left(e_{nRI} \bullet \frac{R_F}{R_I}\right)^2 + 2 \bullet e_{nRF}^2}$$

If the circuits surrounding the amplifier are well balanced, common mode noise (e_{nVOCM}) of the amplifier does not appear in the differential output noise equation given above. A plot of this equation and a plot of the noise generated by the feedback components for the LTC6409 are shown in Figure 5.

The LTC6409's input referred voltage noise contributes the equivalent noise of a 75Ω resistor. When the feedback network is comprised of resistors whose values are larger than this, the output noise is resistor noise and amplifier current noise dominant. For feedback networks consisting of resistors with values smaller than 75Ω, the output noise is voltage noise dominant (see Figure 5).

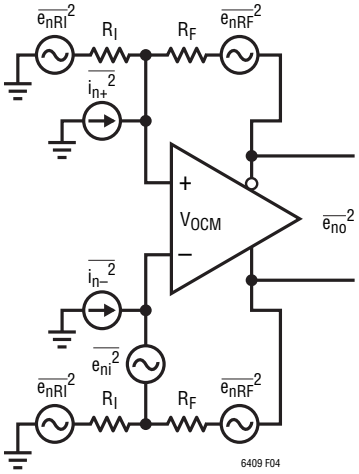

Figure 4. Simplified Noise Model

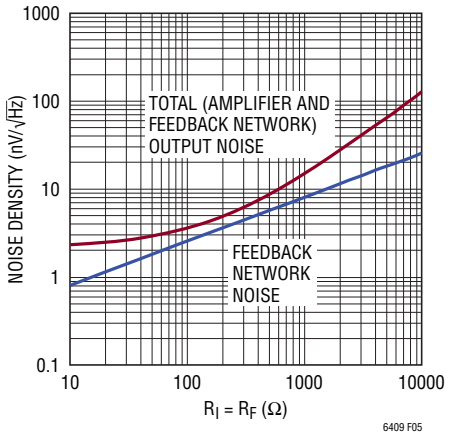

Figure 5. LTC6409 Output Noise vs Noise Contributed by Feedback Network Alone

Lower resistor values always result in lower noise at the penalty of increased distortion due to increased loading by the feedback network on the output. Higher resistor values will result in higher output noise, but typically improved distortion due to less loading on the output. For this reason, when LTC6409 is configured in a differential gain of 1, using feedback resistors of at least 150Ω is recommended.

To calculate noise figure (NF), a source resistance and the noise it generates should also come into consideration. Figure 6 shows a noise model for the amplifier which includes the source resistance (R_S). To generalize the

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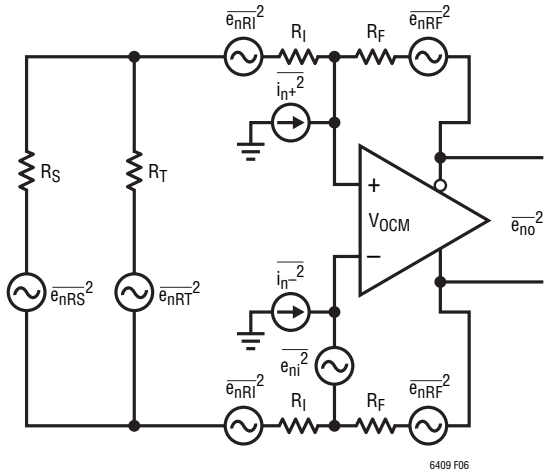

Figure 6. A More General Noise Model Including Source and Termination Resistors

calculation, a termination resistor (R_T) is included and its noise contribution is taken into account.

Now, the total output noise power (excluding the noise contribution of R_S) is calculated as:

$$e_{no}^2 = \left[e_{ni} \bullet \left(1 + \frac{R_F}{R_I + \left(\frac{R_T \| R_S}{2} \right)} \right) \right]^2 + 2 \bullet \left(i_n \bullet R_F \right)^2 +$$

$$2 \bullet \left(e_{nRI} \bullet \frac{R_F}{R_I + \left(\frac{R_T \| R_S}{2} \right)} \right)^2 + 2 \bullet e_{nRF}^2 +$$

$$\left[e_{nRT} \bullet \frac{R_F}{R_I} \bullet \left(\frac{2R_I \| R_S}{R_T + \left(2R_I \| R_S \right)} \right) \right]^2$$

Meanwhile, the output noise power due to noise of R_S is given by:

$$e_{no\,(RS)}^2 = \left[e_{nRS} \bullet \frac{R_F}{R_I} \bullet \left(\frac{2R_I \| R_T}{R_S + \left(2R_I \| R_T \right)} \right) \right]^2$$

Finally, noise figure can be obtained as:

$$NF = 10 \log \left(1 + \frac{e_{no}^2}{e_{no\,(RS)}^2} \right)$$

Figure 7 specifies the measured total output noise (e_{no}), excluding the noise contribution of source resistance, and noise figure (NF) of LTC6409 configured at closed loop gains ($A_V = R_F/R_I$) of 1V/V, 2V/V and 5V/V. The circuits in the left column use termination resistors and transformers to match to the 50Ω source resistance, while the circuits in the right column do not have such matching. For simplicity, DC-blocking and bypass capacitors have not been shown in the circuits, as they do not affect the noise results.

Relationship Between Different Linearity Metrics

Linearity is, of course, an important consideration in many amplifier applications. This section relates the intermodulation distortion of fully differential amplifiers to other linearity metrics commonly used in RF style blocks.

Intercept points are specifications that have long been used as key design criteria in the RF communications world as a metric for the intermodulation distortion performance of a device in the signal chain (e.g., amplifiers, mixers, etc.). Intercept points, like noise figures, can be easily cascaded back and forth through a signal chain to determine the overall performance of a receiver chain, thus resulting in simpler system-level calculations. Traditionally, these systems use primarily single-ended RF amplifiers as gain blocks designed to operate in a 50Ω environment, just like the rest of the receiver chain. Since intercept points are given in dBm, this implies an associated impedance of 50Ω.

However, for LTC6409 as a differential feedback amplifier with low output impedance, a 50Ω resistive load is not required (unlike an RF amplifier). This distinction is important when evaluating the intercept point for LTC6409. In fact, the LTC6409 yields optimum distortion performance when loaded with 200Ω to 1kΩ (at each output), very similar to the input impedance of an ADC. As a result, terminating

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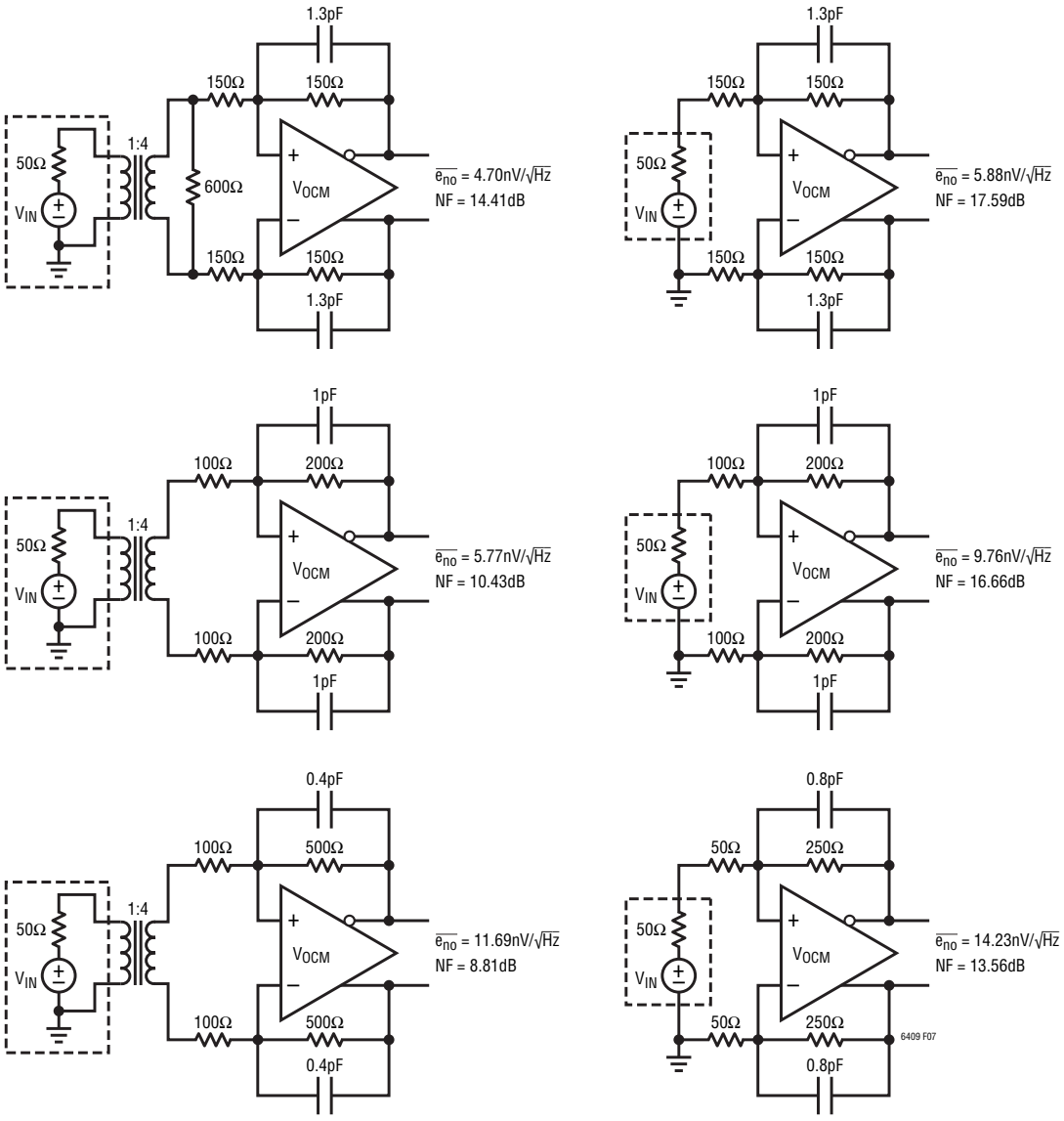

Figure 7. LTC6409 Measured Output Noise and Noise Figure at Different Closed Loop Gains with and without Source Impedance Matching

the input of the ADC to 50Ω can actually be detrimental to system performance.

The definition of 3rd order intermodulation distortion (IMD3) is shown in Figure 8. Also, a graphical representation of how to relate IMD3 to output/input 3rd order intercept points (OIP3/IIP3) has been depicted in Figure 9. Based on this figure, Equation (4) gives the definition of the intercept point, relative to the intermodulation distortion.

$$OIP3 = P_O + \frac{|IMD3|}{2} \quad (4)$$

P_O is the output power of each of the two tones at which IMD3 is measured, as shown in Figure 9. It is calculated in dBm as:

$$P_O = 10\log\left(\frac{V^2_{PDIFF}}{2 \bullet R_L \bullet 10^{-3}}\right) \quad (5)$$

where R_L is the differential load resistance, and V_{PDIFF} is the differential peak voltage for a single tone. Normally, intermodulation distortion is specified for a benchmark composite differential peak of $2V_{P-P}$ at the output of the

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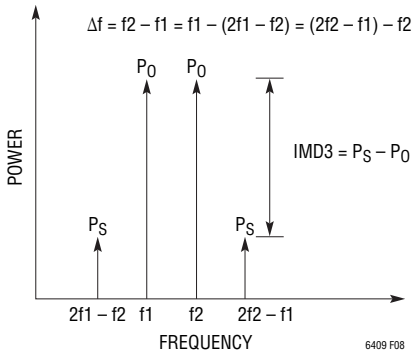

Figure 8. Definition of IMD3

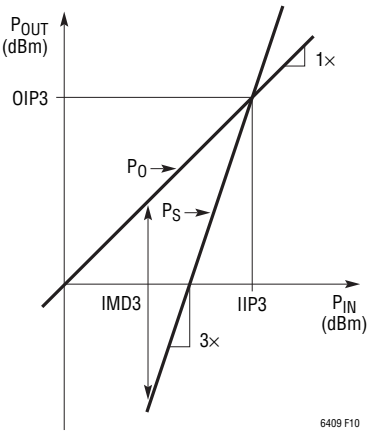

Figure 9. Graphical Representation of the Relationship between IMD3 and OIP3

amplifier, implying that each single tone is $1V_{P-P}$, resulting in V_{PDIFF} = 0.5V. Using R_L = 50Ω as the associated impedance, P_O is calculated to be close to 4dBm.

As seen in Equation (5), when a higher impedance is used, the same level of intermodulation distortion performance results in a lower intercept point. Therefore, it is important to consider the impedance seen by the output of the LTC6409 when working with intercept points.

Comparing linearity specifications between different amplifier types becomes easier when a common impedance level is assumed. For this reason, the intercept points for LTC6409 are reported normalized to a 50Ω load impedance. This is the reason why OIP3 in the Electrical Characteristics table is 4dBm more than half the absolute value of IMD3.

If the top half of the LTC6409 demo board (DC1591A, shown in Figure 12) is used to measure IMD3 and OIP3, one should make sure to properly convert the power seen at the differential output of the amplifier to the power that appears at the single-ended output of the demo board. Figure 10 shows an equivalent representation of the top half of the demo board. This view ignores the DC-blocking and bypass capacitors, which do not affect the analysis here. The transmission line transformers (used mainly for impedance matching) are modeled here as ideal 4:1 impedance transformers together with a –1dB block. This separates the insertion loss of the transformer from its ideal behavior. The 100Ω resistors at the LTC6409 output create a differential 200Ω resistance, which is an impedance match for the reflected R_L.

As previously mentioned, IMD3 is measured for $2V_{P-P}$ differential peak (i.e. 10dBm) at the output of the LTC6409, corresponding to $1V_{P-P}$ (i.e. 4dBm) at each output alone. From LTC6409 output (location A in Figure 10) to the input of the output transformer (location B), there is a voltage attenuation of 1/2 (or –6dB) formed by the resistive divider

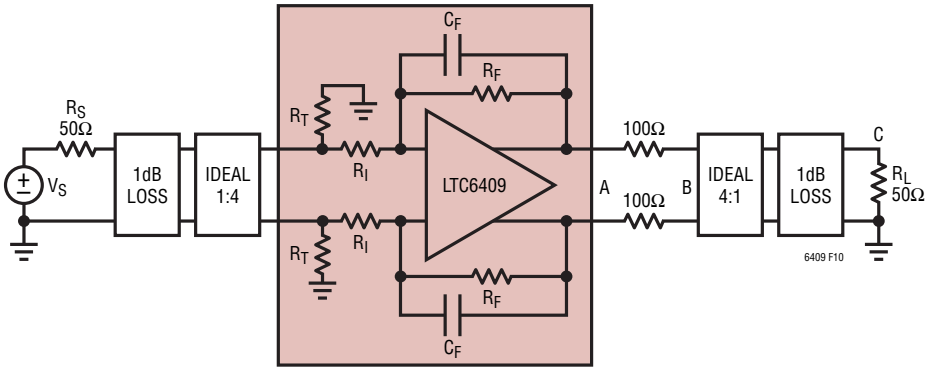

Figure 10. Equivalent Schematic of the Top Half of the LTC6409 Demo Board

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between the R_L • 4 = 200Ω differential resistance seen at location B and the 200Ω formed by the two 100Ω matching resistors at the LTC6409 output. Thus, the differential power at location B is 10 – 6 = 4dBm. Since the transformer ratio is 4:1 and it has an insertion loss of about 1dB, the power at location C (across R_L) is calculated to be 4 – 6 – 1 = –3dBm. This means that IMD3 should be measured while the power at the output of the demo board is –3dBm which is equivalent to having $2V_{P-P}$ differential peak (or 10dBm) at the output of the LTC6409.

GBW vs f_{-3dB}

Gain-bandwidth product (GBW) and –3dB frequency (f_{-3dB}) have been both specified in the Electrical Characteristics table as two different metrics for the speed of the LTC6409. GBW is obtained by measuring the gain of the amplifier at a specific frequency (f_{TEST}) and calculate gain • f_{TEST}. To measure gain, the feedback factor (i.e. $\beta = R_I/(R_I + R_F)$) is chosen sufficiently small so that the feedback loop does not limit the available gain of the LTC6409 at f_{TEST}, ensuring that the measured gain is the open loop gain of the amplifier. As long as this condition is met, GBW is a parameter that depends only on the internal design and compensation of the amplifier and is a suitable metric to specify the inherent speed capability of the amplifier.

f_{-3dB}, on the other hand, is a parameter of more practical interest in different applications and is by definition the frequency at which the gain is 3dB lower than its low frequency value. The value of f_{-3dB} depends on the speed of the amplifier as well as the feedback factor. Since the LTC6409 is designed to be stable in a differential signal gain of 1 (where $R_I = R_F$ or $\beta = 1/2$), the maximum f_{-3dB} is obtained and measured in this gain setting, as reported in the Electrical Characteristics table.

In most amplifiers, the open loop gain response exhibits a conventional single-pole roll-off for most of the frequencies before crossover frequency and the GBW and f_{-3dB} numbers are close to each other. However, the LTC6409 is intentionally compensated in such a way that its GBW is significantly larger than its f_{-3dB}. This means that at lower frequencies (where the input signal frequencies typically lie, e.g. 100MHz) the amplifier's gain and the thus the feedback loop gain is larger. This has the important advantage of further linearizing the amplifier and improving distortion at those frequencies.

Looking at the Frequency Response vs Closed Loop Gain graph in the Typical Performance Characteristics section of this data sheet, one sees that for a closed loop gain (A_V) of 1 (where $R_I = R_F = 150\Omega$), f_{-3dB} is about 2GHz. However, for A_V = 400 (where $R_I = 25\Omega$ and $R_F = 10k\Omega$), the gain at 100MHz is close to 40dB = 100V/V, implying a GBW value of 10GHz.

Feedback Capacitors

When the LTC6409 is configured in low differential gains, it is often advantageous to utilize a feedback capacitor (C_F) in parallel with each feedback resistor (R_F). The use of C_F implements a pole-zero pair (in which the zero frequency is usually smaller than the pole frequency) and adds positive phase to the feedback loop gain around the amplifier. Therefore, if properly chosen, the addition of C_F boosts the phase margin and improves the stability response of the feedback loop. For example, with $R_I = R_F = 150\Omega$, it is recommended for most general applications to use C_F = 1.3pF across each R_F. This value has been selected to maximize f_{-3dB} for the LTC6409 while keeping the peaking of the closed loop gain versus frequency response under a reasonable level (<1dB). It also results in the highest frequency for 0.1dB gain flatness ($f_{0.1dB}$).

However, other values of C_F can also be utilized and tailored to other specific applications. In general, a larger value for C_F reduces the peaking (overshoot) of the amplifier in both frequency and time domains, but also decreases the closed loop bandwidth (f_{-3dB}). For example, while for a closed loop gain (A_V) of 5, C_F = 0.8pF results in maximum f_{-3dB} (as previously shown in the Frequency Response vs Closed Loop Gain graph of this data sheet), if C_F = 1.2pF is used, the amplifier exhibits no overshoot in the time domain which is desirable in certain applications. Both the circuits discussed in this section have been shown in the Typical Applications section of this data sheet.

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Board Layout and Bypass Capacitors

For single supply applications, it is recommended that high quality 0.1µF||1000pF ceramic bypass capacitors be placed directly between each V^+ pin and its closest $V^–$ pin with short connections. The $V^–$ pins (including the Exposed Pad) should be tied directly to a low impedance ground plane with minimal routing.

For dual (split) power supplies, it is recommended that additional high quality 0.1µF||1000pF ceramic capacitors be used to bypass V^+ pins to ground and $V^–$ pins to ground, again with minimal routing.

For driving heavy differential loads (<200Ω), additional bypass capacitance may be needed for optimal performance. Keep in mind that small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self-resonant frequency than do leaded capacitors, and perform best in high speed applications.

To prevent degradation in stability response, it is highly recommended that any stray capacitance at the input pins, +IN and –IN, be kept to an absolute minimum by keeping printed circuit connections as short as possible. This becomes especially true when the feedback resistor network uses resistor values greater than 500Ω in circuits with $R_I = R_F$.

At the output, always keep in mind the differential nature of the LTC6409, because it is critical that the load impedances seen by both outputs (stray or intended), be as balanced and symmetric as possible. This will help preserve the balanced operation of the LTC6409 that minimizes the generation of even-order harmonics and maximizes the rejection of common mode signals and noise.

The V_{OCM} pin should be bypassed to the ground plane with a high quality ceramic capacitor of at least 0.01µF. This will prevent common mode signals and noise on this pin from being inadvertently converted to differential signals and noise by impedance mismatches both externally and internally to the IC.

Driving ADCs

The LTC6409's ground-referenced input, differential output and adjustable output common mode voltage make it ideal for interfacing to differential input ADCs. These ADCs are typically supplied from a single-supply voltage and have an optimal common mode input range near mid-supply. The LTC6409 interfaces to these ADCs by providing single-ended to differential conversion and common mode level shifting.

The sampling process of ADCs creates a transient that is caused by the switching in of the ADC sampling capacitor. This momentarily shorts the output of the amplifier as charge is transferred between amplifier and sampling capacitor. The amplifier must recover and settle from this load transient before the acquisition period has ended, for a valid representation of the input signal. The LTC6409 will settle quickly from these periodic load impulses. The RC network between the outputs of the driver and the inputs of the ADC decouples the sampling transient of the ADC (see Figure 11). The capacitance serves to provide the bulk of the charge during the sampling process, while the two resistors at the outputs of the LTC6409 are used to dampen and attenuate any charge injected by the ADC. The RC filter gives the additional benefit of band limiting broadband output noise. Generally, longer time constants improve SNR at the expense of settling time. The resistors in the decoupling network should be at least 10Ω. These resistors also serve to decouple the LTC6409 outputs from load capacitance. Too large of a resistor will leave insufficient settling time. Too small of a resistor will not properly dampen the load transient of the sampling process, prolonging the time required for settling. In 16-bit applications, this will typically require a minimum of eleven RC time constants. For lowest distortion, choose capacitors with low dielectric absorption (such as a C0G multilayer ceramic capacitor).

APPLICATIONS INFORMATION

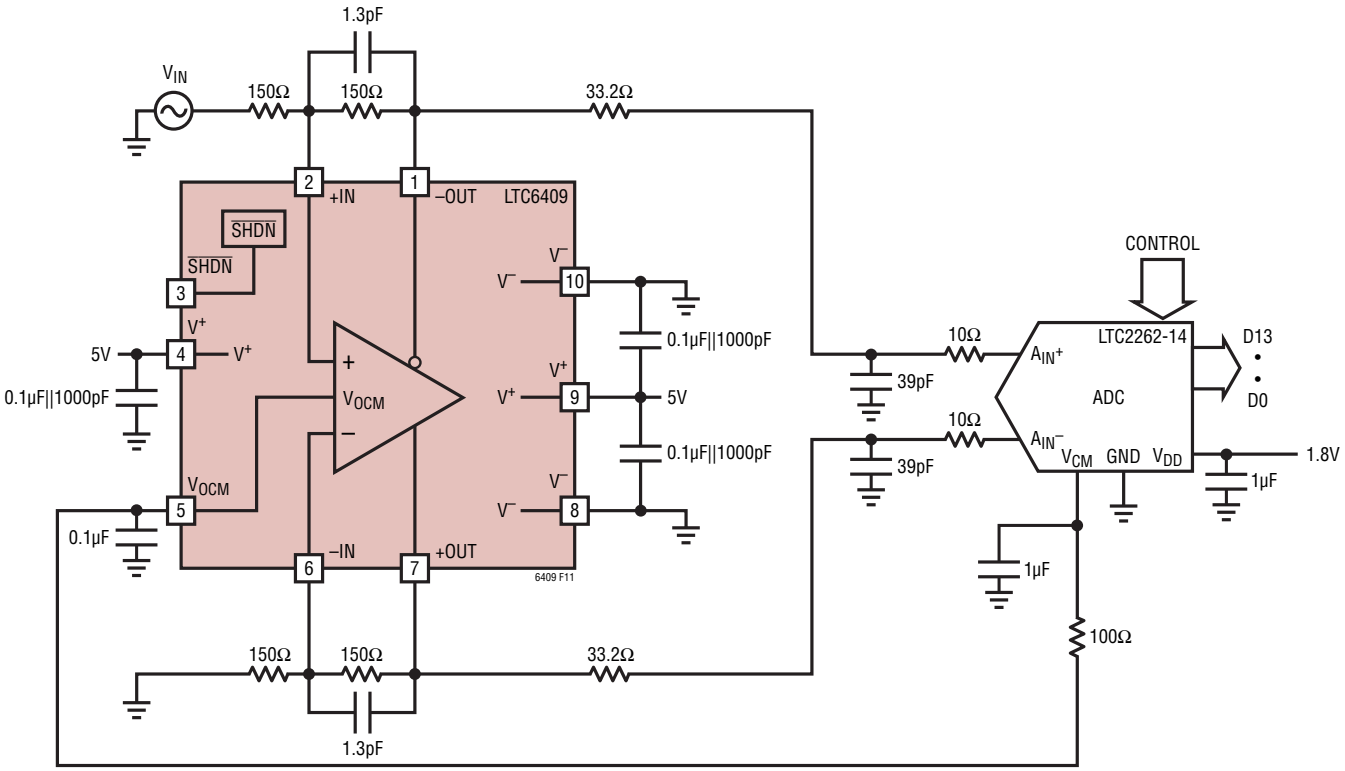


Figure 11. Driving an ADC

APPLICATIONS INFORMATION

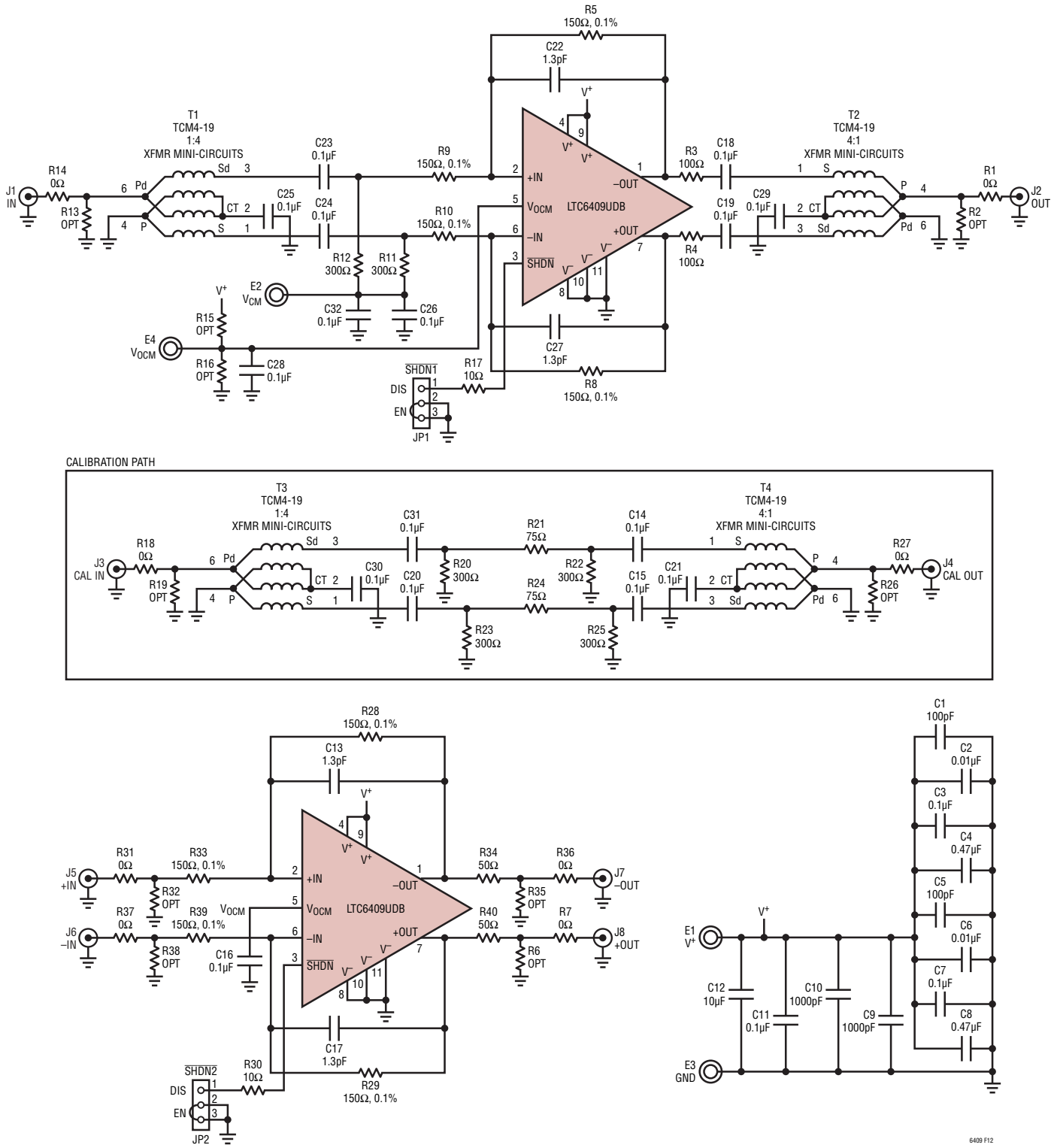


Figure 12. Demo Board DC1591A Schematic

APPLICATIONS INFORMATION

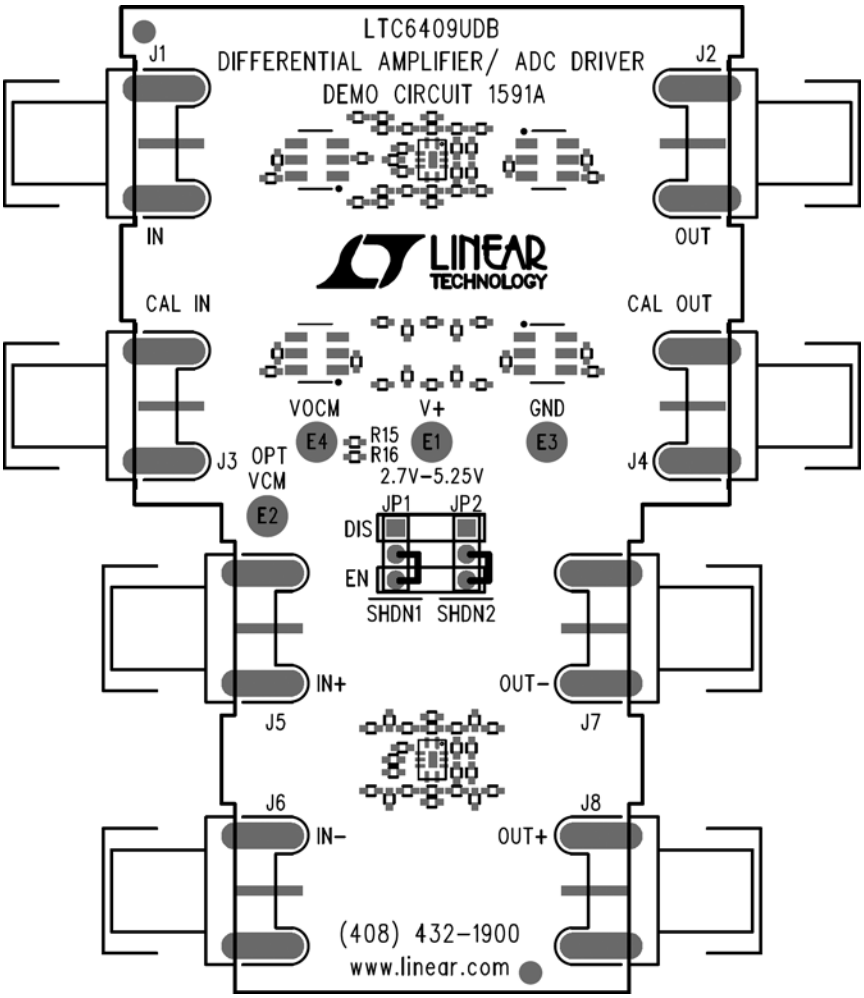
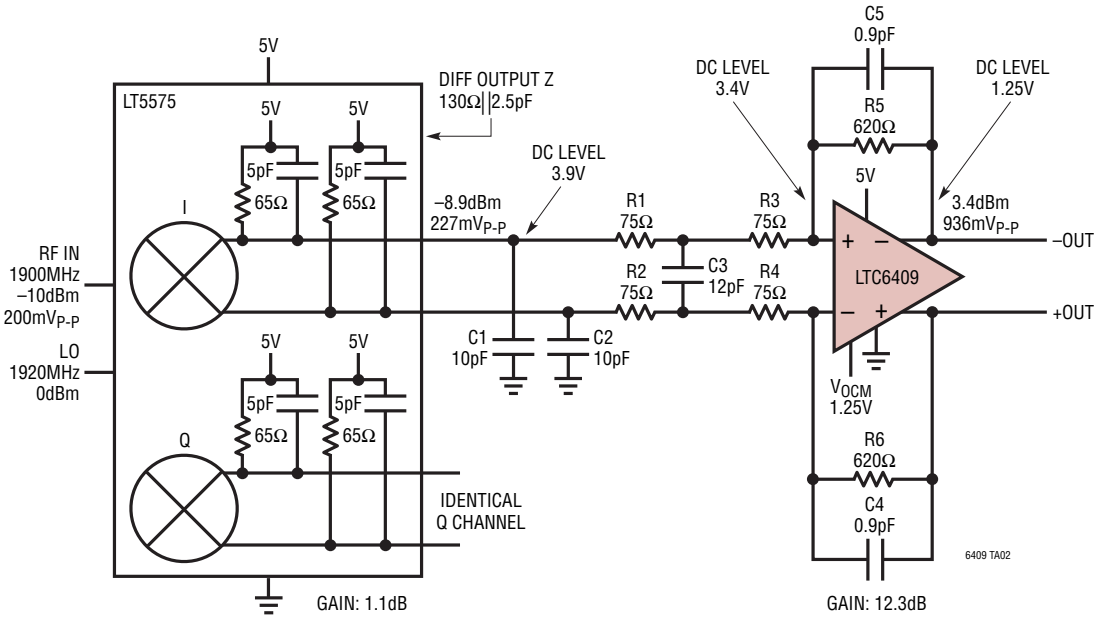


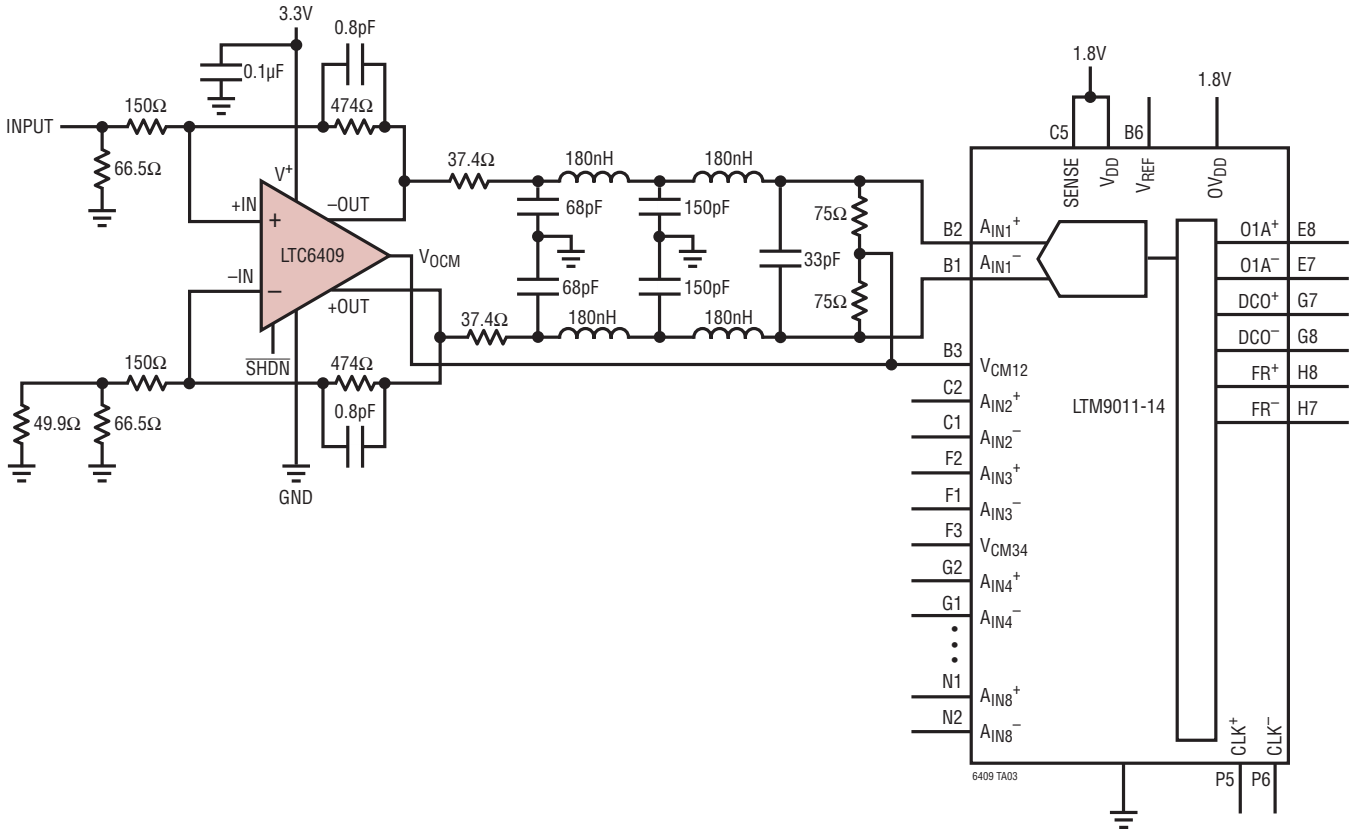
Figure 13. Demo Board DC1591A Layout

TYPICAL APPLICATIONS

DC-Coupled Level Shifting of an I/Q Demodulator Output

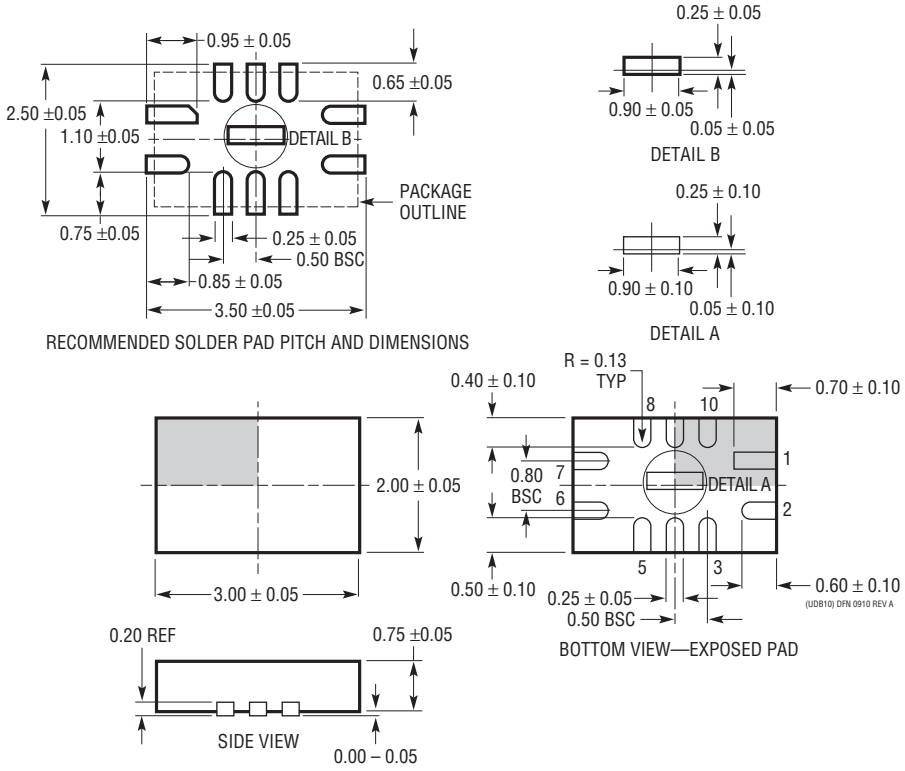


Single-Ended to Differential Conversion Using LTC6409 and 50MHz Lowpass Filter (Only One Channel Shown)



PACKAGE DESCRIPTION

UDB Package
10-Lead Plastic QFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1848 Rev A)



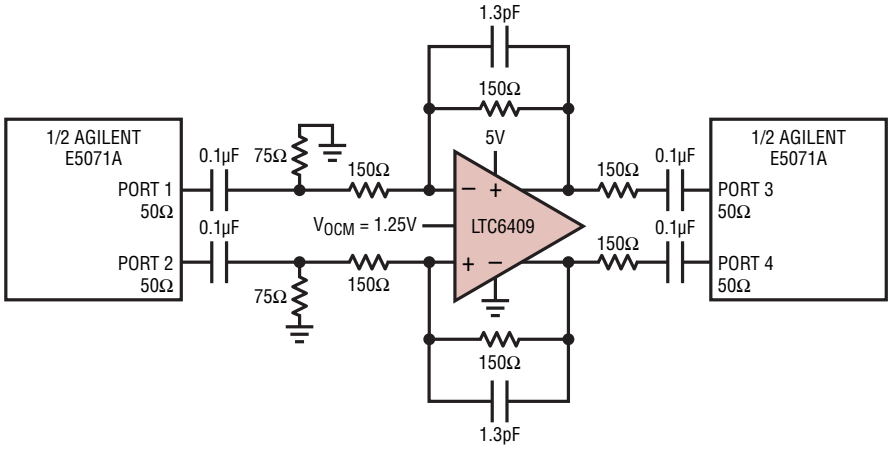
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

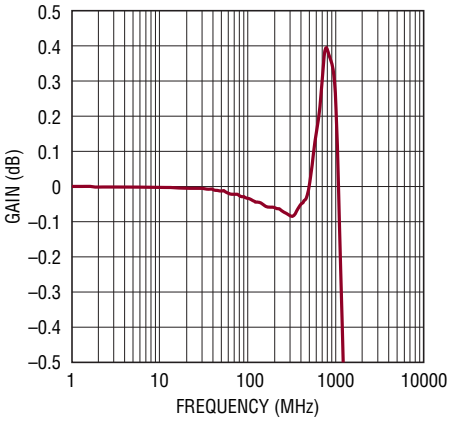
REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/10	Revised Typical Application drawing	21

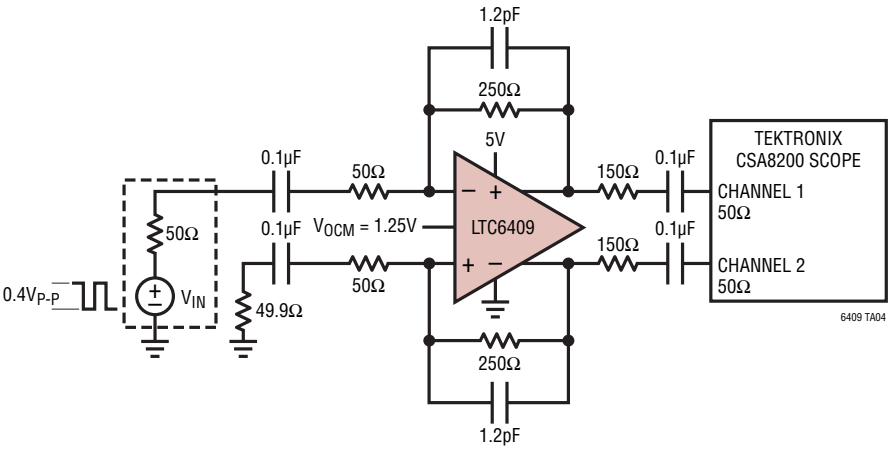
TYPICAL APPLICATIONS

LTC6409 Externally Compensated for Maximum Gain Flatness and for No-Overshoot Time-Domain Response

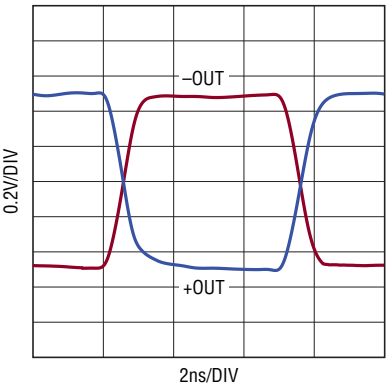


Gain 0.1dB Flatness





No-Overshoot Step Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6400-8/LTC6400-14/ LTC6400-20/LTC6400-26	1.8GHz Low Noise, Low Distortion, Differential ADC Drivers	–71dBc IM3 at 240MHz $2V_{P-P}$ Composite, I_S = 90mA, A_V = 8dB/14dB/20dB/26dB
LTC6401-8/LTC6401-14/ LTC6401-20/LTC6401-26	1.3GHz Low Noise, Low Distortion, Differential ADC Drivers	–74dBc IM3 at 140MHz $2V_{P-P}$ Composite, I_S = 50mA, A_V = 8dB/14dB/20dB/26dB
LTC6406/LTC6405	3GHz/2.7GHz Low Noise, Rail-to-Rail Input Differential Amplifier/Driver	–70dBc/–65dBc Distortion at 50MHz, I_S = 18mA, 1.6nV/$\sqrt{Hz}$ Noise, 3V/5V Supply
LTC6416	2GHz Low Noise, Differential 16-Bit ADC Buffer	–72.5dBc IM3 at 300MHz $2V_{P-P}$ Composite, 150mW on 3.6V Supply
LTC2209	16-Bit, 160Msps ADC	100dB SFDR, V_{DD} = 3.3V, V_{CM} = 1.25V
LTC2262-14	14-Bit, 150Msps Ultralow Power 1.8V ADC	88dB SFDR, 149mW, V_{DD} = 1.8V, V_{CM} = 0.9V

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 1210 REV A • PRINTED IN USA

Precision, Micropower LDO Voltage References in TSOT

ADR121/ADR125/ADR127

FEATURES

- **Initial accuracy**
  - **A grade: ±0.24%**
  - **B grade: ±0.12%**
- **Maximum temperature coefficient**
  - **A grade: 25 ppm/°C**
  - **B grade: 9 ppm/°C**
- **Low dropout: 300 mV for ADR121/ADR125**
- **High output current: +5 mA/−2 mA**
- **Low typical operating current: 85 µA**
- **Input range: 2.7 V to 18 V for ADR127**
- **Temperature range: −40°C to +125°C**
- **Tiny TSOT (UJ-6) package**

APPLICATIONS

- **Battery-powered instrumentation**
- **Portable medical equipment**
- **Data acquisition systems**
- **Automotive**

PIN CONFIGURATION

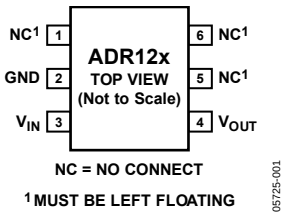


Figure 1.

GENERAL DESCRIPTION

The ADR121/ADR125/ADR127 are a family of micropower, high precision, series mode, band gap references with sink and source capability. The parts feature high accuracy and low power consumption in a tiny package. The ADR12x design includes a patented temperature-drift curvature correction technique that minimizes the nonlinearities in the output voltage vs. temperature characteristics.

The ADR12x is a low dropout voltage reference, requiring only 300 mV for the ADR121/ADR125 and 1.45 V for the ADR127 above the nominal output voltage on the input to provide a stable output voltage. This low dropout performance, coupled with the low 85 µA operating current, makes the ADR12x ideal for battery-powered applications.

Available in an extended industrial temperature range of −40°C to +125°C, the ADR121/ADR125/ADR127 are housed in the tiny TSOT (UJ-6) package.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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Added Thermal Hysteresis Equation ... 7
Changes to Ordering Guide ... 18

6/06—Revision 0: Initial Version

SPECIFICATIONS

ADR121 ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 2.8 V to 18 V, I_{OUT} = 0 mA, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
B Grade			2.497	2.5	2.503	V
A Grade			2.494	2.5	2.506	V
INITIAL ACCURACY ERROR	V_{OERR}					
B Grade			−0.12		+0.12	%
A Grade			−0.24		+0.24	%
TEMPERATURE COEFFICIENT	TCV_{OUT}	−40°C < T_A < +125°C				
B Grade				3	9	ppm/°C
A Grade				15	25	ppm/°C
DROPOUT (V_{OUT} – V_{IN})	V_{DO}	I_{OUT} = 0 mA	300			mV
LOAD REGULATION		−40°C < T_A < +125°C; V_{IN} = 5.0 V, 0 mA < I_{OUT} < 5 mA		80	300	ppm/mA
		−40°C < T_A < +125°C; V_{IN} = 5.0 V, −2 mA < I_{OUT} < 0 mA		50	300	ppm/mA
LINE REGULATION		2.8 V to 18 V, I_{OUT} = 0 mA	−50	+3	+50	ppm/V
PSRR		f = 60 Hz		−90		dB
QUIESCENT CURRENT	I_Q	−40°C < T_A < +125°C, no load				
		V_{IN} = 18 V		95	125	µA
		V_{IN} = 2.8 V		80	95	µA
SHORT-CIRCUIT CURRENT TO GROUND		V_{IN} = 2.8 V		18		mA
		V_{IN} = 18 V		40		mA
VOLTAGE NOISE		f = 10 kHz		500		nV/√Hz
		f = 0.1 Hz to 10 Hz		18		µV p-p
TURN-ON SETTLING TIME		To 0.1%, C_L = 0.2 µF		100		µs
LONG-TERM STABILITY		1000 hours @ 25°C		150		ppm/1000 hrs
OUTPUT VOLTAGE HYSTERESIS		See the Terminology section		300		ppm

ADR125 ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 5.3 V to 18 V, I_{OUT} = 0 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
B Grade			4.994	5.0	5.006	V
A Grade			4.988	5.0	5.012	V
INITIAL ACCURACY ERROR	V_{OERR}					
B Grade			−0.12		+0.12	%
A Grade			−0.24		+0.24	%
TEMPERATURE COEFFICIENT	TCV_{OUT}	−40°C < T_A < +125°C				
B Grade				3	9	ppm/°C
A Grade				15	25	ppm/°C
DROPOUT (V_{OUT} – V_{IN})	V_{DO}	I_{OUT} = 5 mA	300			mV
LOAD REGULATION		−40°C < T_A < +125°C; V_{IN} = 6.0 V, 0 mA < I_{OUT} < 5 mA		35	200	ppm/mA
		−40°C < T_A < +125°C; V_{IN} = 6.0 V, −2 mA < I_{OUT} < 0 mA		35	200	ppm/mA
LINE REGULATION		5.3 V to 18 V, I_{OUT} = 0 mA			30	ppm/V
PSRR		f = 60 Hz		−90		dB
QUIESCENT CURRENT	I_Q	−40°C < T_A < +125°C, no load				
		V_{IN} = 18 V		95	125	µA
		V_{IN} = 5.3 V		80	95	µA
SHORT-CIRCUIT CURRENT TO GROUND		V_{IN} = 5.3 V		25		mA
		V_{IN} = 18 V		40		mA
VOLTAGE NOISE		f = 10 kHz		900		nV/√Hz
		f = 0.1 Hz to 10 Hz		36		µV p-p
TURN-ON SETTLING TIME		To 0.1%, C_L = 0.2 µF		100		µs
LONG-TERM STABILITY		1000 hours @ 25°C		150		ppm/1000 hrs
OUTPUT VOLTAGE HYSTERESIS		See the Terminology section		300		ppm

ADR127 ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 2.7 V to 18 V, I_{OUT} = 0 mA, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
B Grade			1.2485	1.25	1.2515	V
A Grade			1.2470	1.25	1.2530	V
INITIAL ACCURACY ERROR	V_{OERR}					
B Grade			−0.12		+0.12	%
A Grade			−0.24		+0.24	%
TEMPERATURE COEFFICIENT	TCV_{OUT}	−40°C < T_A < +125°C				
B Grade				3	9	ppm/°C
A Grade				15	25	ppm/°C
DROPOUT (V_{OUT} − V_{IN})	V_{DO}	I_{OUT} = 0 mA	1.45			V
LOAD REGULATION		−40°C < T_A < +125°C; V_{IN} = 3.0 V, 0 mA < I_{OUT} < 5 mA		85	400	ppm/mA
		−40°C < T_A < +125°C; V_{IN} = 3.0 V, −2 mA < I_{OUT} < 0 mA		65	400	ppm/mA
LINE REGULATION		2.7 V to 18 V, I_{OUT} = 0 mA		30	90	ppm/V
PSRR		f = 60 Hz		−90		dB
QUIESCENT CURRENT	I_Q	−40°C < T_A < +125°C, no load				
		V_{IN} = 18 V		95	125	µA
		V_{IN} = 2.7 V		80	95	µA
SHORT-CIRCUIT CURRENT TO GROUND		V_{IN} = 2.7 V		15		mA
		V_{IN} = 18 V		30		mA
VOLTAGE NOISE		f = 10 kHz		300		nV/√Hz
		f = 0.1 Hz to 10 Hz		9		µV p-p
TURN-ON SETTLING TIME		To 0.1%, C_L = 0.2 µF		80		µs
LONG-TERM STABILITY		1000 hours @ 25°C		150		ppm/1000 hrs
OUTPUT VOLTAGE HYSTERESIS		See the Terminology section		300		ppm

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{IN} to GND	20 V
Internal Power Dissipation	
TSOT (UJ-6)	40 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5.

Package Type	θ_{JA}	θ_{JC}	Unit
6-Lead TSOT (UJ-6)	230	146	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

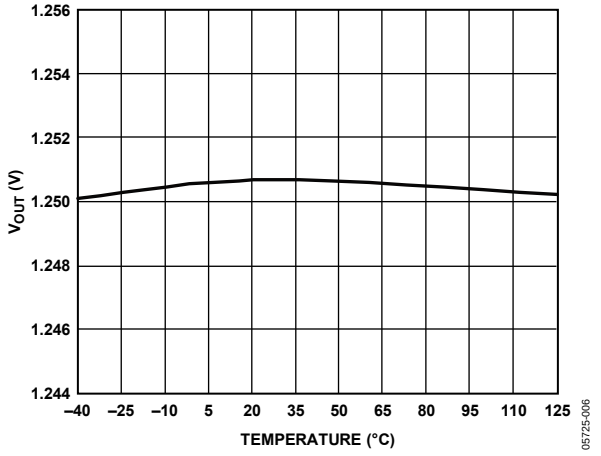


Figure 2. ADR127 V_{OUT} vs. Temperature

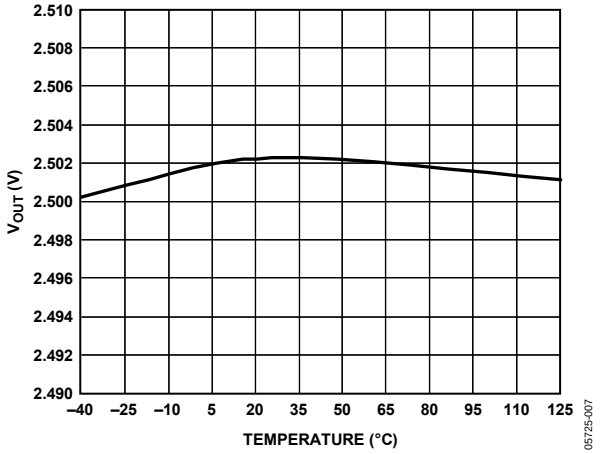


Figure 3. ADR121 V_{OUT} vs. Temperature

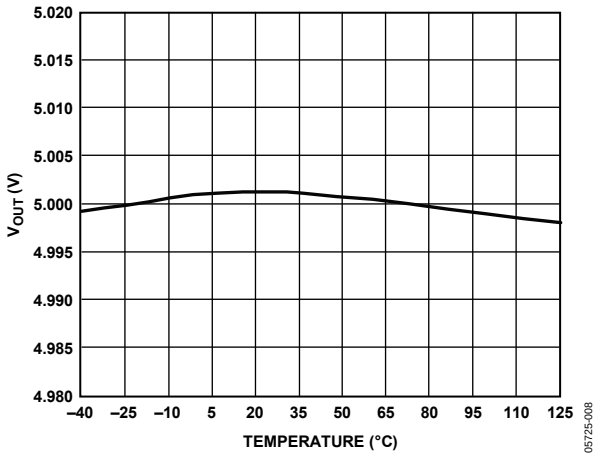


Figure 4. ADR125 V_{OUT} vs. Temperature

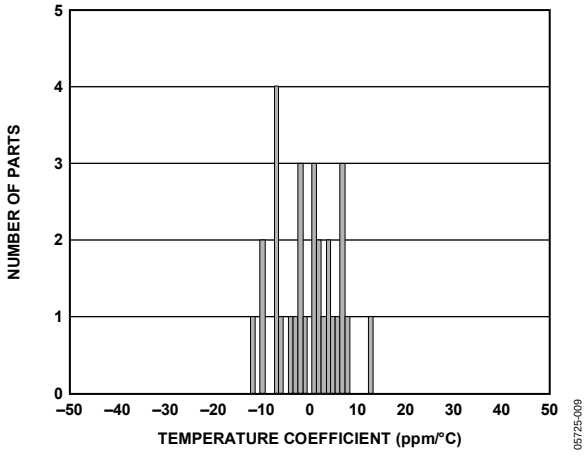


Figure 5. ADR127 Temperature Coefficient

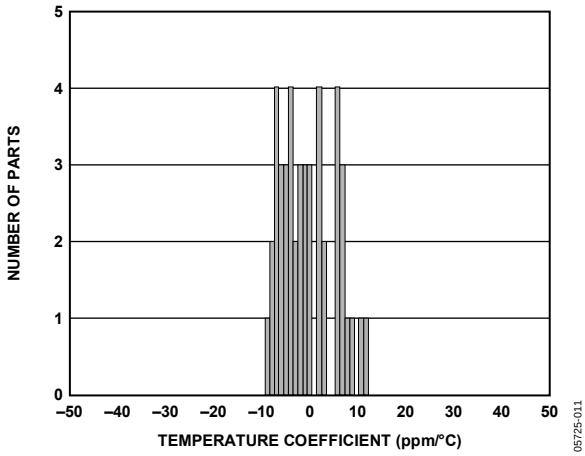


Figure 6. ADR121 Temperature Coefficient

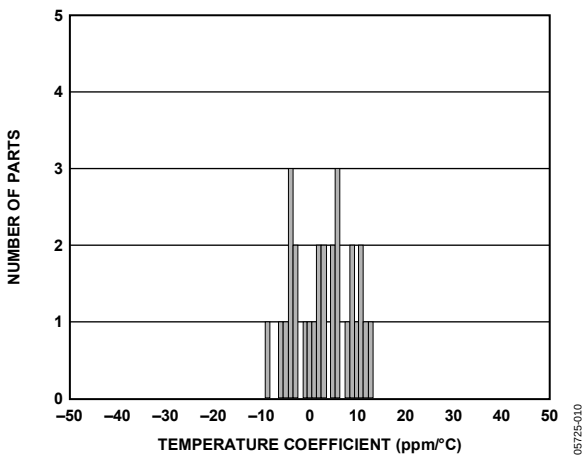


Figure 7. ADR125 Temperature Coefficient

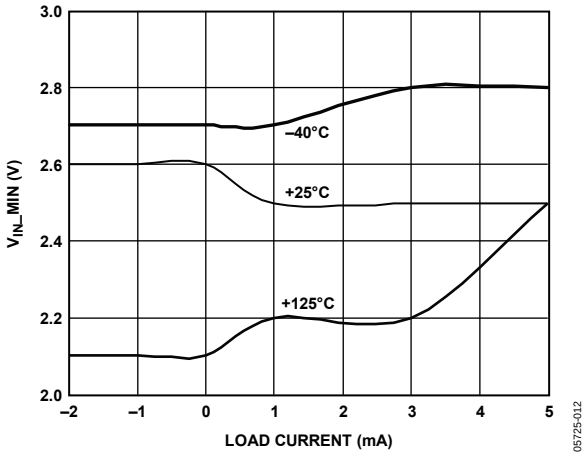


Figure 8. ADR127 Minimum Input Voltage vs. Load Current

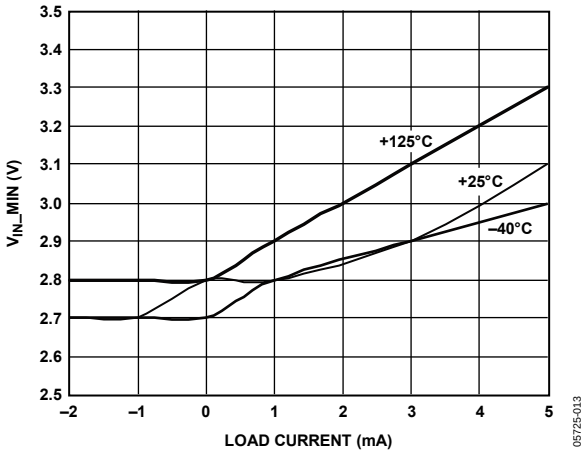


Figure 9. ADR121 Minimum Input Voltage vs. Load Current

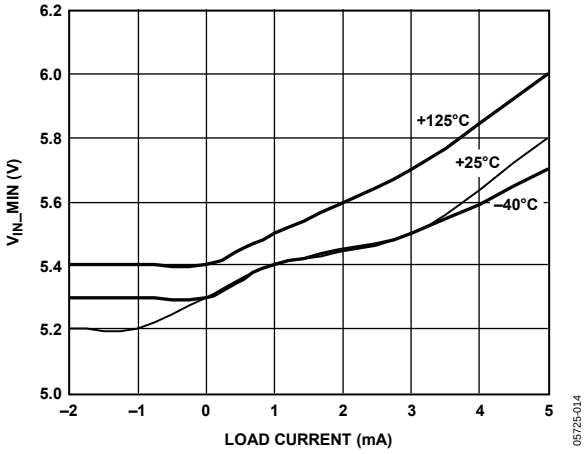


Figure 10. ADR125 Minimum Input Voltage vs. Load Current

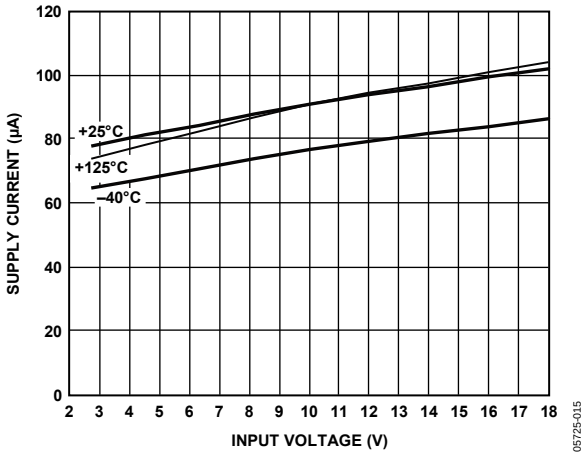


Figure 11. ADR127 Supply Current vs. Input Voltage

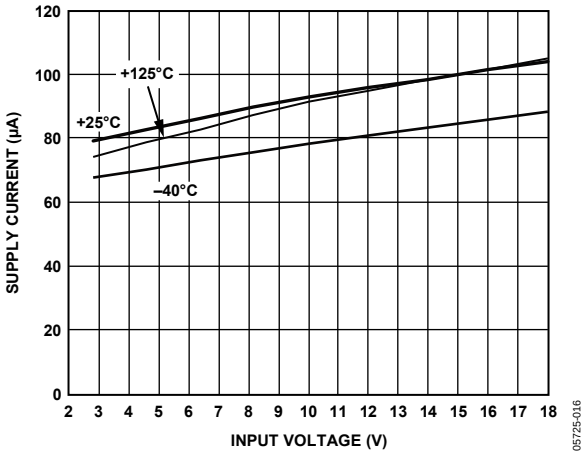


Figure 12. ADR121 Supply Current vs. Input Voltage

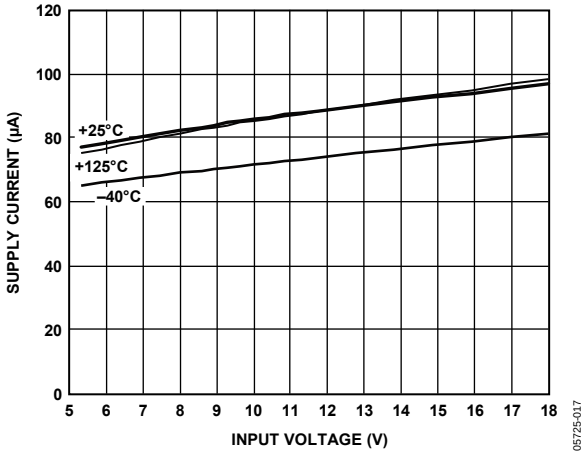


Figure 13. ADR125 Supply Current vs. Input Voltage

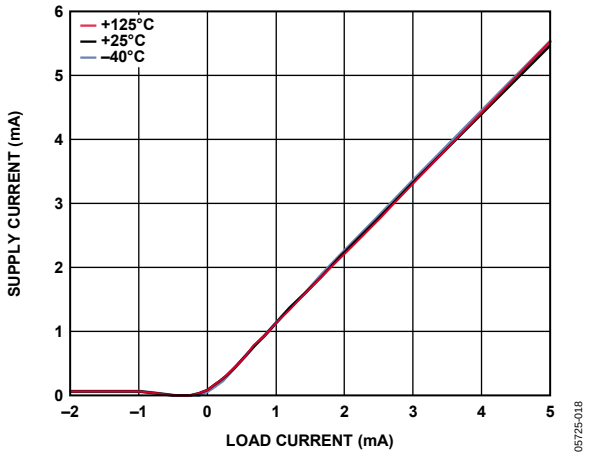


Figure 14. ADR127 Supply Current vs. Load Current

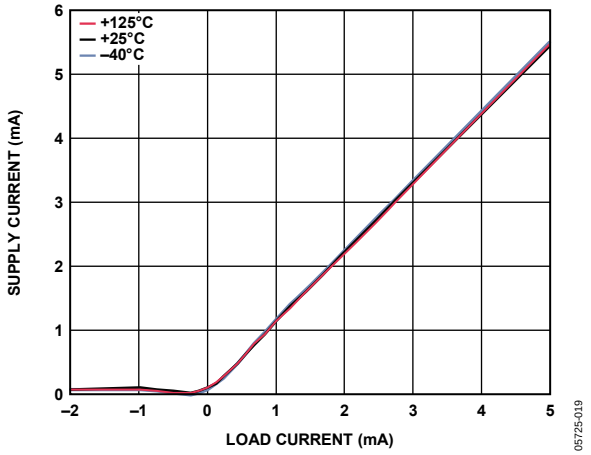


Figure 15. ADR121 Supply Current vs. Load Current

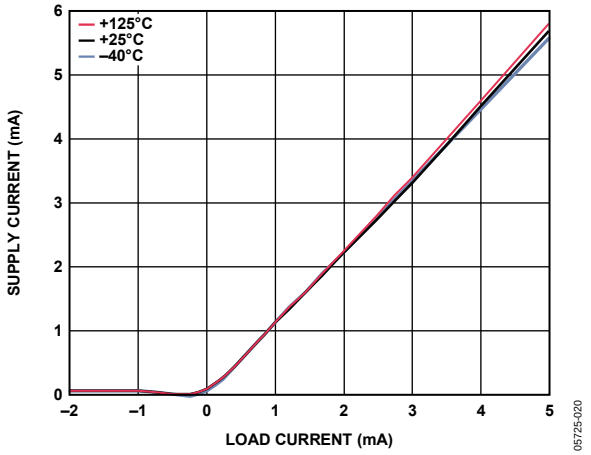


Figure 16. ADR125 Supply Current vs. Load Current

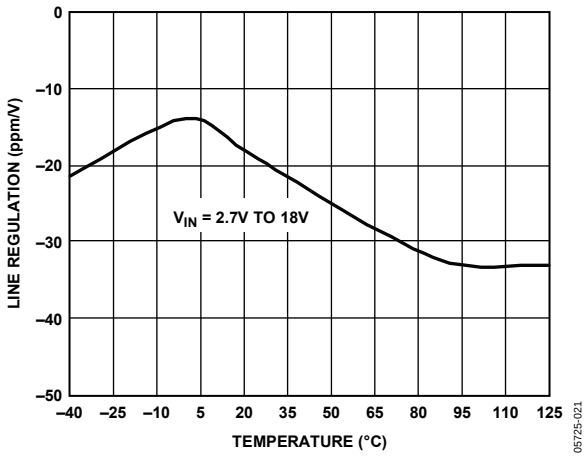


Figure 17. ADR127 Line Regulation vs. Temperature

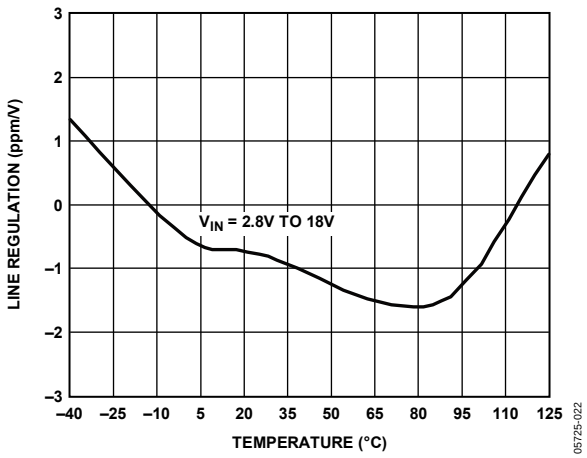


Figure 18. ADR121 Line Regulation vs. Temperature

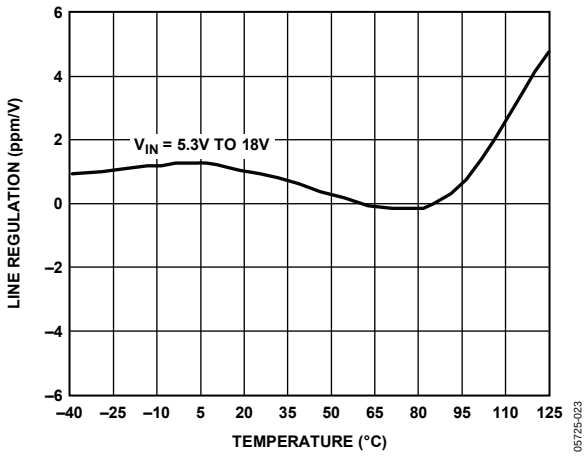


Figure 19. ADR125 Line Regulation vs. Temperature

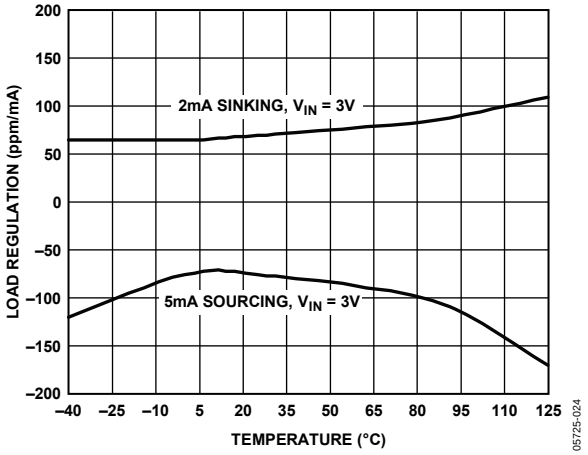


Figure 20. ADR127 Load Regulation vs. Temperature

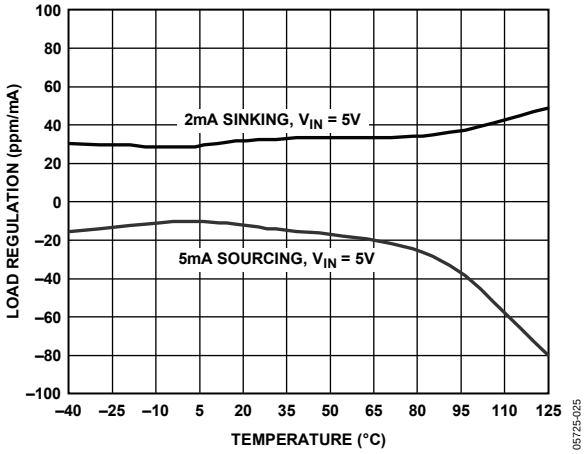


Figure 21. ADR121 Load Regulation vs. Temperature

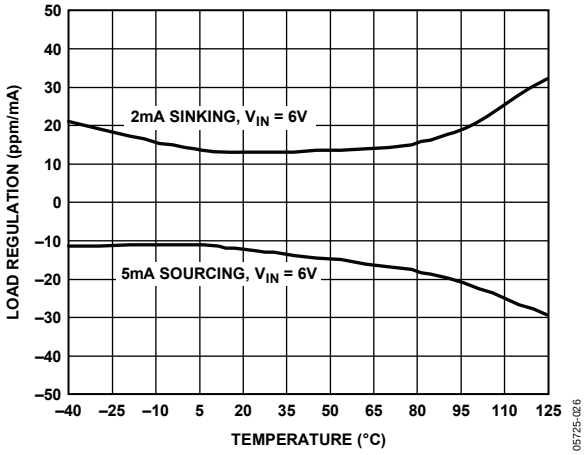


Figure 22. ADR125 Load Regulation vs. Temperature

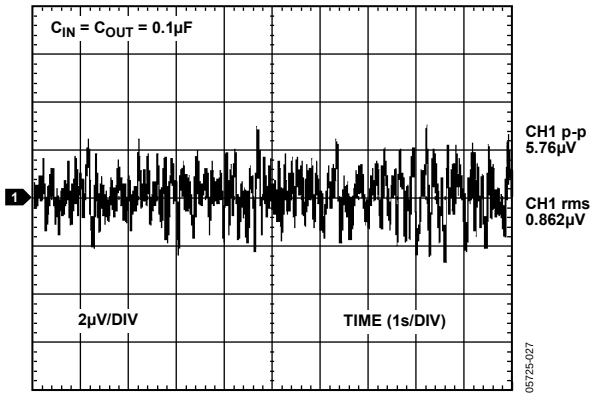


Figure 23. ADR127 0.1 Hz to 10 Hz Noise

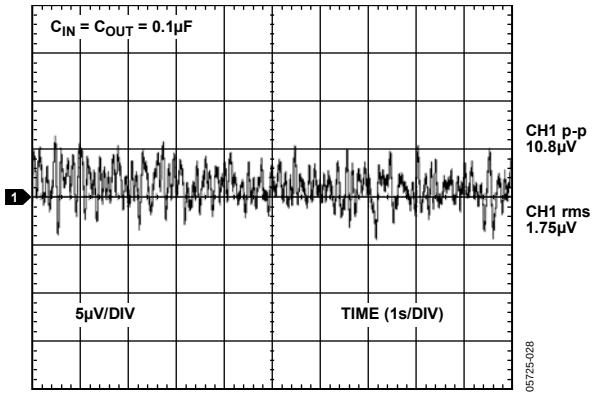


Figure 24. ADR121 0.1 Hz to 10 Hz Noise

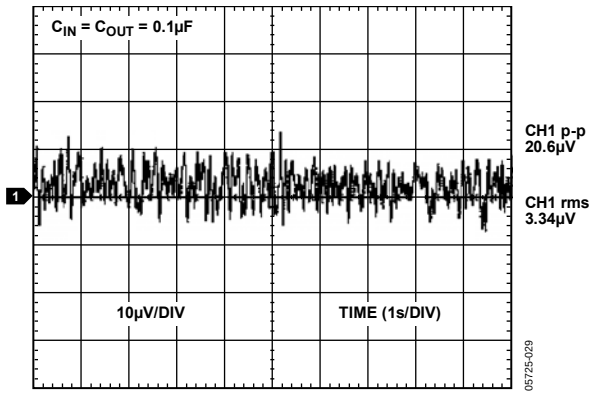


Figure 25. ADR125 0.1 Hz to 10 Hz Noise

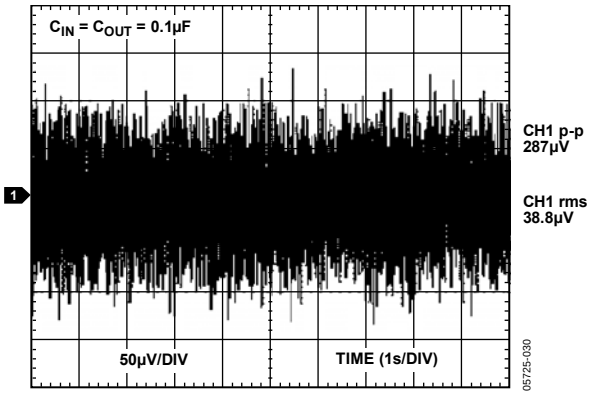


Figure 26. ADR127 10 Hz to 10 kHz Noise

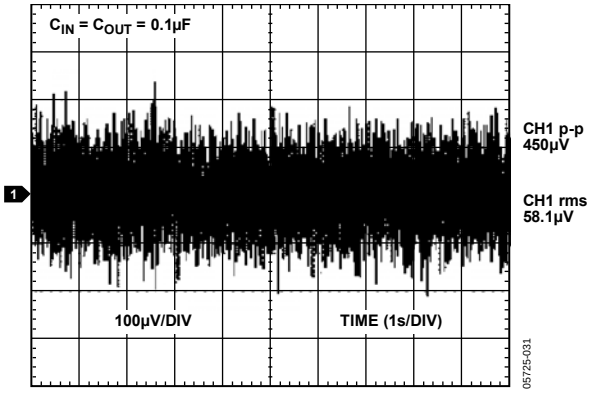


Figure 27. ADR121 10 Hz to 10 kHz Noise

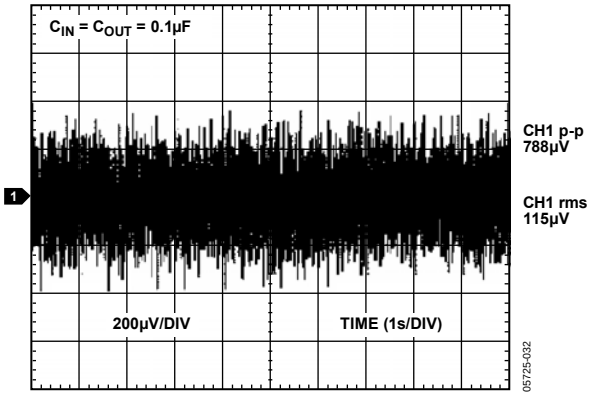


Figure 28. ADR125 10 Hz to 10 kHz Noise

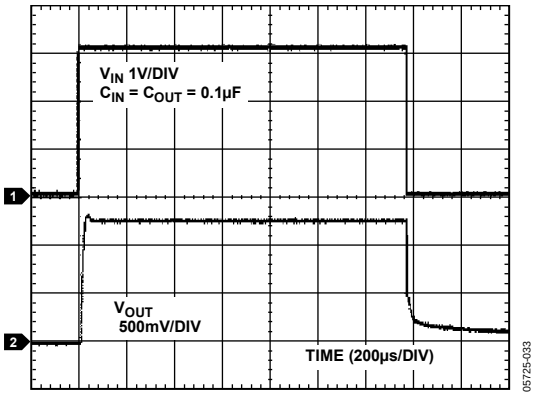


Figure 29. ADR127 Turn-On Response

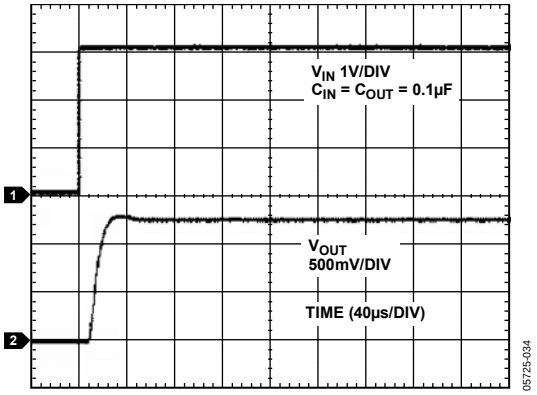


Figure 30. ADR127 Turn-On Response

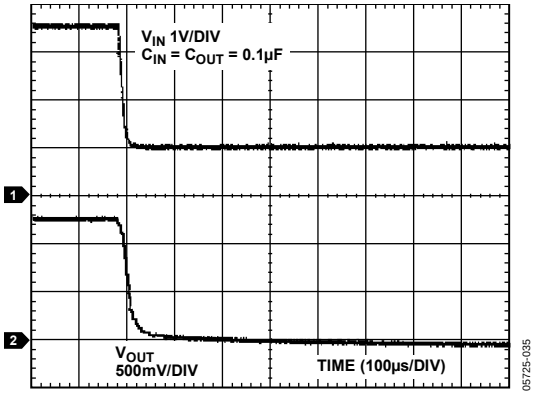


Figure 31. ADR127 Turn-Off Response

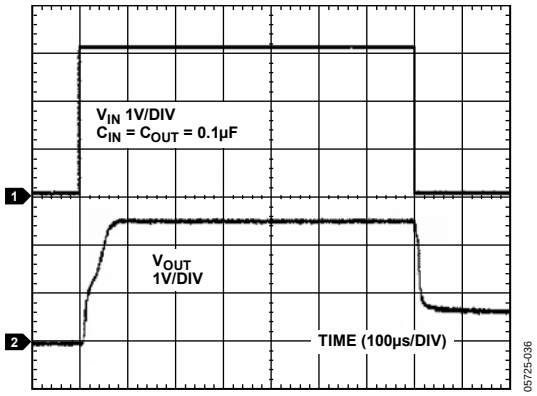


Figure 32. ADR121 Turn-On Response

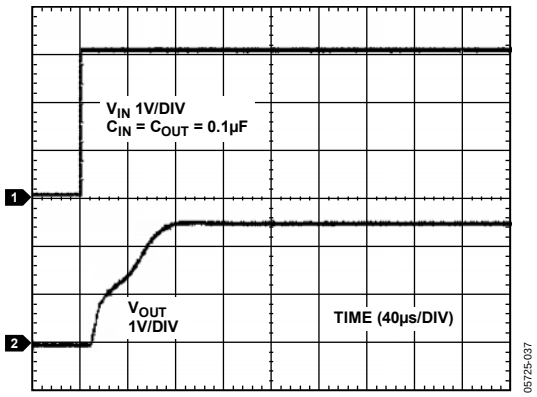


Figure 33. ADR121 Turn-On Response

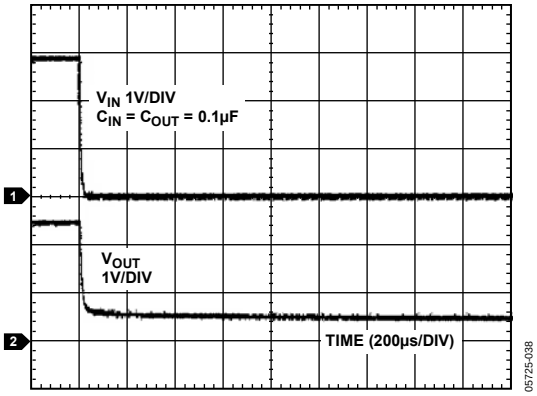


Figure 34. ADR121 Turn-Off Response

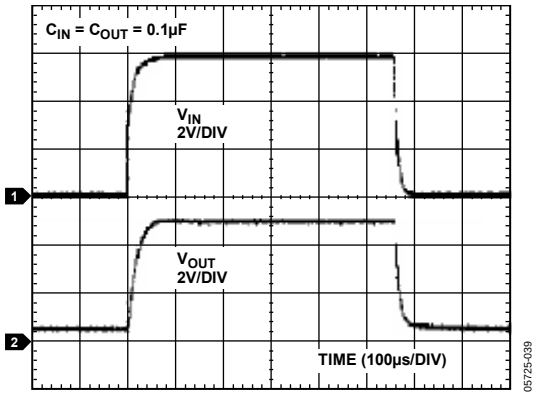


Figure 35. ADR125 Turn-On Response

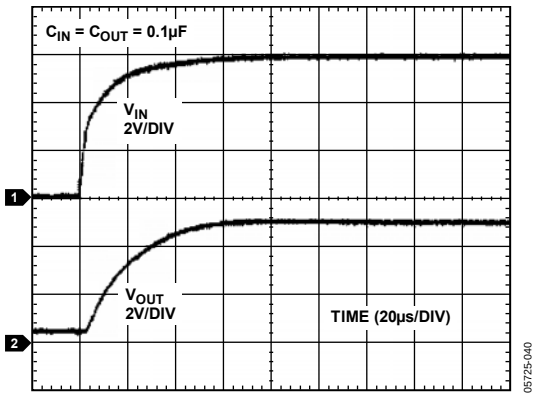


Figure 36. ADR125 Turn-On Response

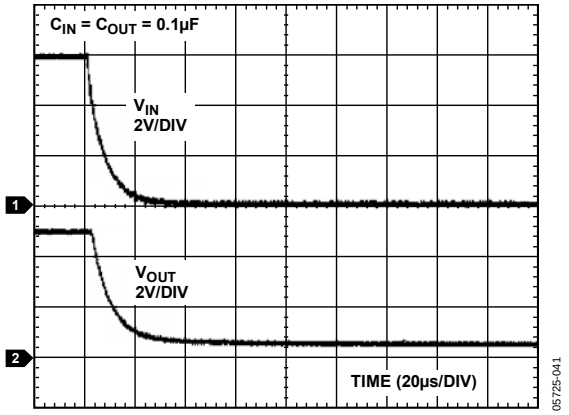


Figure 37. ADR125 Turn-Off Response

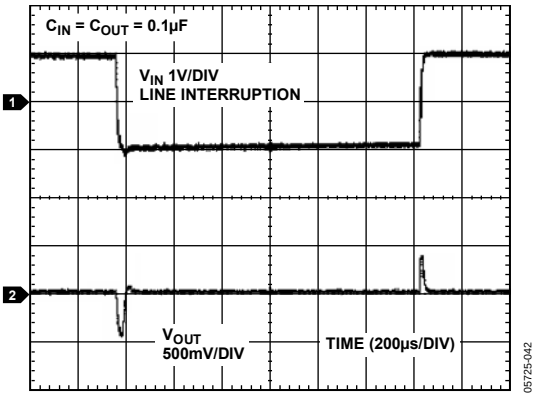


Figure 38. ADR127 Line Transient Response

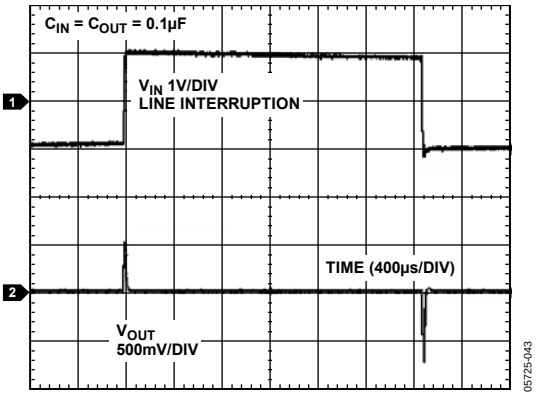


Figure 39. ADR121 Line Transient Response

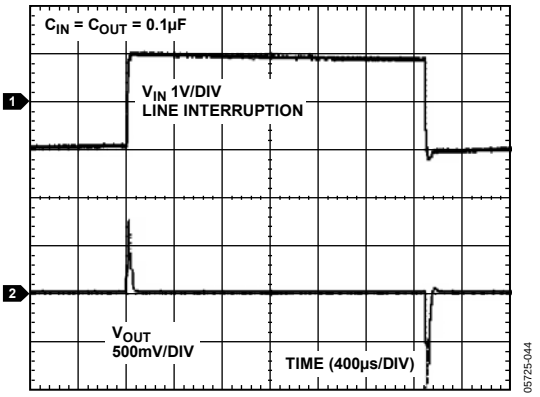


Figure 40. ADR125 Line Transient Response

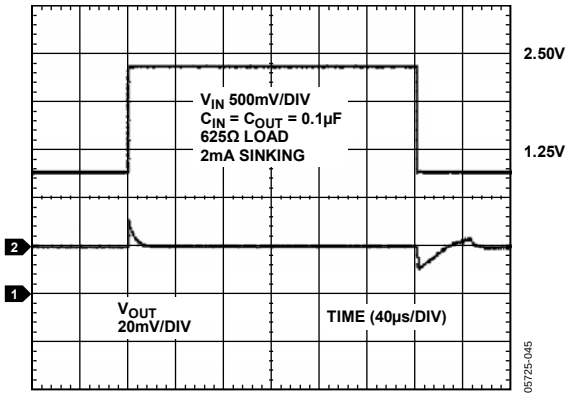


Figure 41. ADR127 Load Transient Response (Sinking)

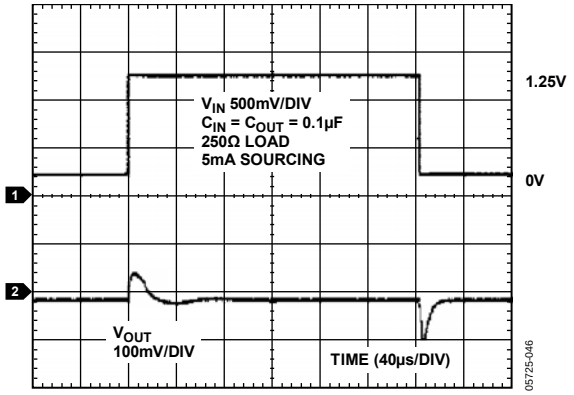


Figure 42. ADR127 Load Transient Response (Sourcing)

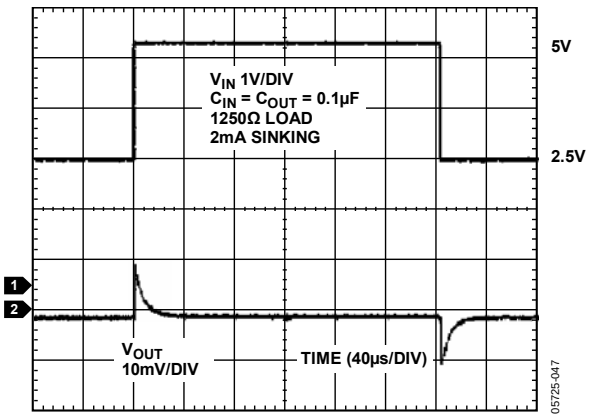


Figure 43. ADR121 Load Transient Response (Sinking)

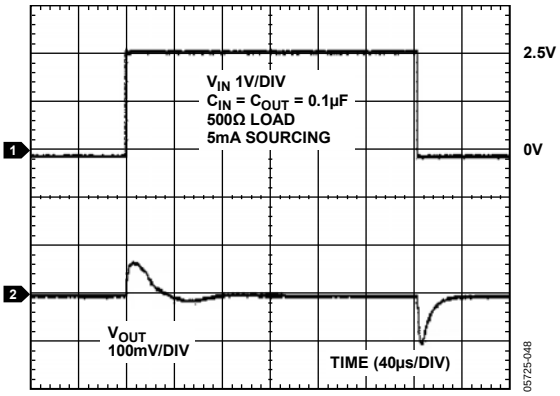


Figure 44. ADR121 Load Transient Response (Sourcing)

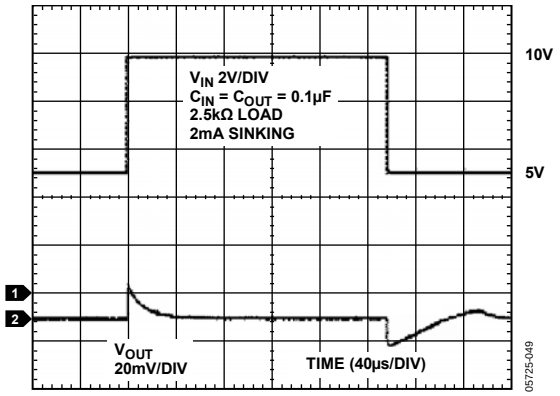


Figure 45. ADR125 Load Transient Response (Sinking)

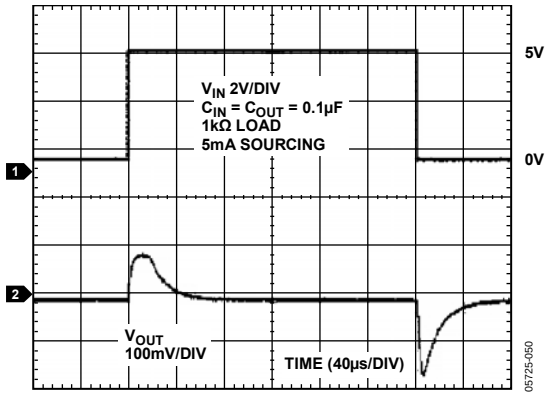


Figure 46. ADR125 Load Transient Response (Sourcing)

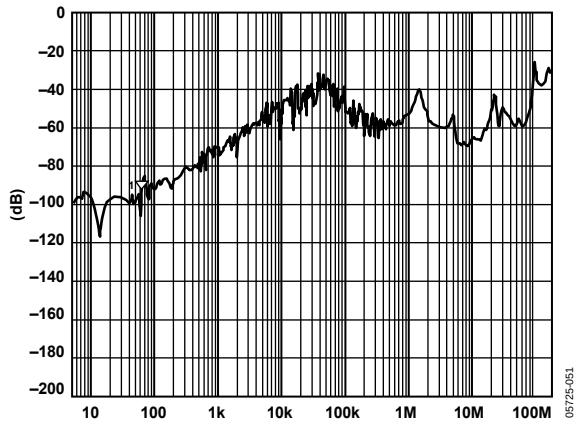


Figure 47. ADR121/ADR125/ADR127 PSRR

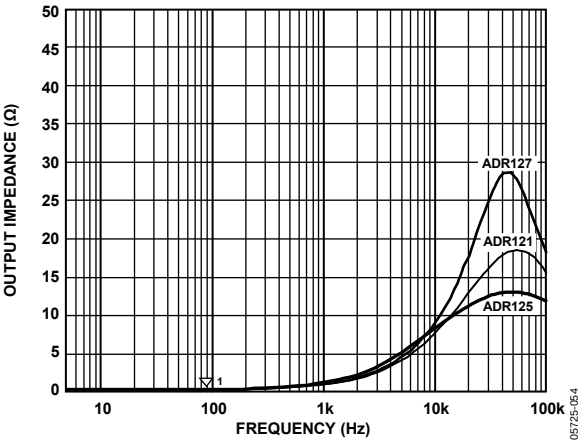


Figure 48. ADR121/ADR125/ADR127 Output Impedance vs. Frequency

TERMINOLOGY

Temperature Coefficient
The change in output voltage with respect to operating temperature change normalized by the output voltage at 25°C. This parameter is expressed in ppm/°C and can be determined as follows:

$$TCV_{OUT}[\text{ppm/°C}] = \frac{V_{OUT}(T_2) - V_{OUT}(T_1)}{V_{OUT}(25°\text{C}) \times (T_2 - T_1)} \times 10^6 \quad (1)$$

where:
V_{OUT}(25°C) = V_{OUT} at 25°C.
$V_{OUT}(T_1)$ = V_{OUT} at Temperature 1.
$V_{OUT}(T_2)$ = V_{OUT} at Temperature 2.

Line Regulation
The change in the output voltage due to a specified change in input voltage. This parameter accounts for the effects of self-heating. Line regulation is expressed in percent per volt, parts-per-million per volt, or microvolts per voltage change in input voltage.

Load Regulation
The change in output voltage due to a specified change in load current. This parameter accounts for the effects of self-heating. Load regulation is expressed in microvolts per milliampere, parts-per-million per milliampere, or ohms of dc output resistance.

Long-Term Stability
Typical shift of output voltage at 25°C on a sample of parts subjected to a test of 1000 hours at 25°C.

$$\Delta V_{OUT}\ V_{OUT}(t_0) - V_{OUT}(t_1)$$
$$\Delta V_{OUT}[\text{ppm}] = \frac{V_{OUT}(t_0) - V_{OUT}(t_1)}{V_{OUT}(t_0)} \times 10^6 \quad (2)$$

where:
$V_{OUT}(t_0)$ = V_{OUT} at 25°C at Time 0.
$V_{OUT}(t_1)$ = V_{OUT} at 25°C after 1000 hours operating at 25°C.

Thermal Hysteresis
The change in output voltage after the device is cycled through temperatures from +25°C to −40°C to +125°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle.

$$V_{OUT\_HYS} = V_{OUT}(25°\text{C}) - V_{OUT\_TC} \quad (3)$$
$$V_{OUT\_HYS}[\text{ppm}] = \frac{V_{OUT}(25°\text{C}) - V_{OUT\_TC}}{V_{OUT}(25°\text{C})} \times 10^6$$

where:
V_{OUT}(25°C) = V_{OUT} at 25°C.
V_{OUT_TC} = V_{OUT} at 25°C after temperature cycle at +25°C to −40°C to +125°C and back to +25°C.

THEORY OF OPERATION

The ADR12x band gap references are the high performance solution for low supply voltage and low power applications. The uniqueness of these products lies in their architecture.

POWER DISSIPATION CONSIDERATIONS

The ADR12x family is capable of delivering load currents up to 5 mA with an input range from 3.0 V to 18 V. When this device is used in applications with large input voltages, care must be taken to avoid exceeding the specified maximum power dissipation or junction temperature because this could result in premature device failure.

Use the following formula to calculate a device's maximum junction temperature or dissipation:

$$P_D = \frac{T_J - T_A}{\theta_{JA}} \quad (4)$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
P_D is the device power dissipation.
θ_{JA} is the device package thermal resistance.

INPUT CAPACITOR

Input capacitors are not required on the ADR12x. There is no limit for the value of the capacitor used on the input, but a 1 µF to 10 µF capacitor on the input may improve transient response in applications where there is a sudden supply change. An additional 0.1 µF capacitor in parallel also helps reduce noise from the supply.

OUTPUT CAPACITOR

The ADR12x requires a small 0.1 µF capacitor for stability. Additional 0.1 µF to 10 µF capacitance in parallel can improve load transient response. This acts as a source of stored energy for a sudden increase in load current. The only parameter affected with the additional capacitance is turn-on time.

APPLICATIONS INFORMATION

BASIC VOLTAGE REFERENCE CONNECTION

The circuit in Figure 49 illustrates the basic configuration for the ADR12x family voltage reference.

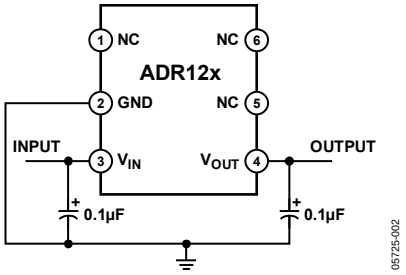


Figure 49. Basic Configuration for the ADR12x Family

STACKING REFERENCE ICs FOR ARBITRARY OUTPUTS

Some applications may require two reference voltage sources that are a combined sum of the standard outputs. Figure 50 shows how this stacked output reference can be implemented.

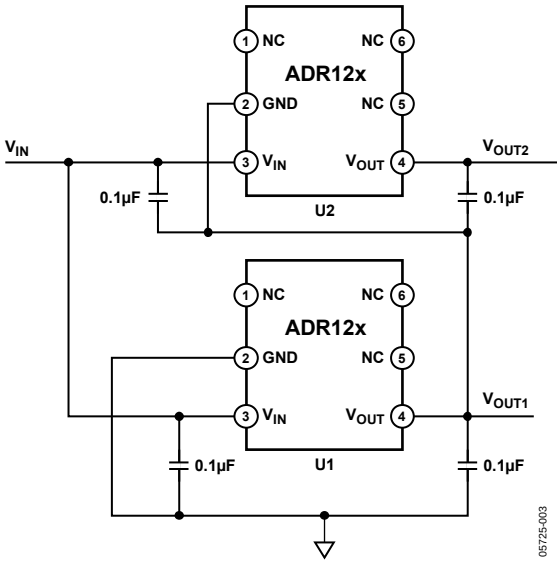


Figure 50. Stacking References with the ADR12x

Two reference ICs are used and fed from an unregulated input, V_{IN}. The outputs of the individual ICs are connected in series, which provides two output voltages, V_{OUT1} and V_{OUT2}. V_{OUT1} is the terminal voltage of U1, whereas V_{OUT2} is the sum of this voltage and the terminal of U2. U1 and U2 are chosen for the two voltages that supply the required outputs (see Table 6). For example, if U1 and U2 are ADR127s and $V_{IN} \geq 3.95$ V, V_{OUT1} is 1.25 V and V_{OUT2} is 2.5 V.

Table 6. Required Outputs

U1/U2	V_{OUT2}	V_{OUT1}
ADR127/ADR121	1.25 V	3.75 V
ADR127/ADR125	1.25 V	6.25 V
ADR121/ADR125	2.5 V	7.5 V

NEGATIVE PRECISION REFERENCE WITHOUT PRECISION RESISTORS

A negative reference is easily generated by adding an op amp, for example, the AD8603, and is configured as shown in Figure 51. V_{OUT} is at virtual ground and, therefore, the negative reference can be taken directly from the output of the op amp. The op amp must be dual-supply, low offset, and rail-to-rail if the negative supply voltage is close to the reference output.

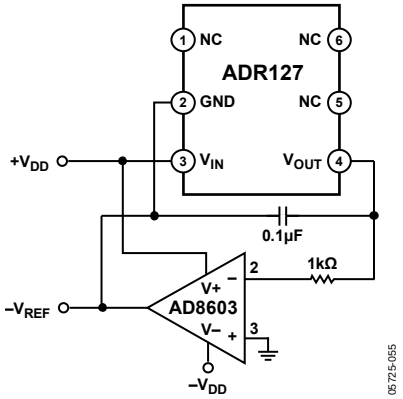


Figure 51. Negative Reference

GENERAL-PURPOSE CURRENT SOURCE

In low power applications, the need can arise for a precision current source that can operate on low supply voltages. The ADR12x can be configured as a precision current source (see Figure 52). The circuit configuration shown is a floating current source with a grounded load. The reference's output voltage is bootstrapped across R_{SET}, which sets the output current into the load. With this configuration, circuit precision is maintained for load currents ranging from the reference's supply current, typically 85 µA, to approximately 5 mA.

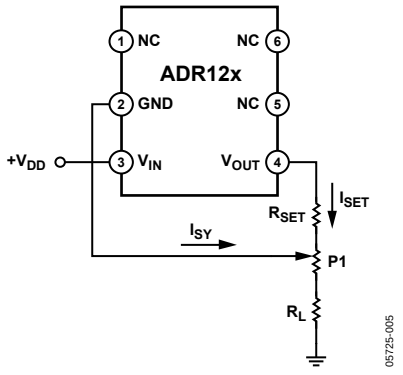


Figure 52. ADR12x Trim Configuration

OUTLINE DIMENSIONS

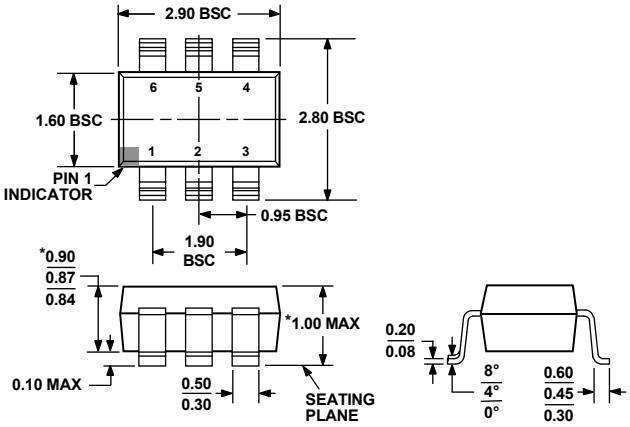


Figure 53. 6-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Output Voltage (V_{OUT})	Initial Accuracy		Temperature Coefficient (ppm/°C)	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
		mV	±%						
ADR121AUJZ-REEL7[1]	2.5	2.5	0.24	25	−40°C to +125°C	6-Lead TSOT	UJ-6	3,000	R0N
ADR121AUJZ-R2[1]	2.5	2.5	0.24	25	−40°C to +125°C	6-Lead TSOT	UJ-6	250	R0N
ADR121BUJZ-REEL7[1]	2.5	2.5	0.12	9	−40°C to +125°C	6-Lead TSOT	UJ-6	3,000	R0P
ADR125AUJZ-REEL7[1]	5.0	5.0	0.24	25	−40°C to +125°C	6-Lead TSOT	UJ-6	3,000	R0Q
ADR125AUJZ-R2[1]	5.0	5.0	0.24	25	−40°C to +125°C	6-Lead TSOT	UJ-6	250	R0Q
ADR125BUJZ-REEL7[1]	5.0	5.0	0.12	9	−40°C to +125°C	6-Lead TSOT	UJ-6	3,000	R0R
ADR127AUJZ-REEL7[1]	1.25	3	0.24	25	−40°C to +125°C	6-Lead TSOT	UJ-6	3,000	R0S
ADR127AUJZ-R2[1]	1.25	3	0.24	25	−40°C to +125°C	6-Lead TSOT	UJ-6	250	R0S
ADR127BUJZ-REEL7[1]	1.25	1.5	0.12	9	−40°C to +125°C	6-Lead TSOT	UJ-6	3,000	R0T

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D05725-0-1/08(B)

International
IOR Rectifier

IRF8910PbF

HEXFET® Power MOSFET

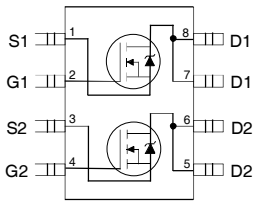
V_{DSS}	$R_{DS(on)}$ max	I_D
20V	13.4mΩ@V_{GS} = 10V	10A

Applications

- Dual SO-8 MOSFET for POL converters in desktop, servers, graphics cards, game consoles and set-top box
- Lead-Free

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- 20V V_{GS} Max. Gate Rating



Top View


SO-8

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	10	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	8.3	
I_{DM}	Pulsed Drain Current ①	82	
P_D @T_A = 25°C	Power Dissipation	2.0	W
P_D @T_A = 70°C	Power Dissipation	1.3	
	Linear Derating Factor	0.016	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	⎯⎯	42	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④⑤	⎯⎯	62.5	

Notes ① through ⑤ are on page 10

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.015	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	10.7	13.4	mΩ	V_{GS} = 10V, I_D = 10A ③
		—	14.6	18.3		V_{GS} = 4.5V, I_D = 8.0A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.65	—	2.55	V	V_{DS} = V_{GS}, I_D = 250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.8	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	µA	V_{DS} = 16V, V_{GS} = 0V
		—	—	150		V_{DS} = 16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	24	—	—	S	V_{DS} = 10V, I_D = 8.2A
Q_g	Total Gate Charge	—	7.4	11		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	2.4	—		V_{DS} = 10V
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	0.80	—	nC	V_{GS} = 4.5V
Q_{gd}	Gate-to-Drain Charge	—	2.5	—		I_D = 8.2A
Q_{godr}	Gate Charge Overdrive	—	1.7	—		See Fig. 6
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	3.3	—		
Q_{oss}	Output Charge	—	4.4	—	nC	V_{DS} = 10V, V_{GS} = 0V
$t_{d(on)}$	Turn-On Delay Time	—	6.2	—		V_{DD} = 10V, V_{GS} = 4.5V
t_r	Rise Time	—	10	—	ns	I_D = 8.2A
$t_{d(off)}$	Turn-Off Delay Time	—	9.7	—		Clamped Inductive Load
t_f	Fall Time	—	4.1	—		
C_{iss}	Input Capacitance	—	960	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	300	—	pF	V_{DS} = 10V
C_{rss}	Reverse Transfer Capacitance	—	160	—		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	19	mJ
I_{AR}	Avalanche Current ①	—	8.2	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	82		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 8.2A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	17	26	ns	T_J = 25°C, I_F = 8.2A, V_{DD} = 10V
Q_{rr}	Reverse Recovery Charge	—	6.5	9.7	nC	di/dt = 100A/µs ③

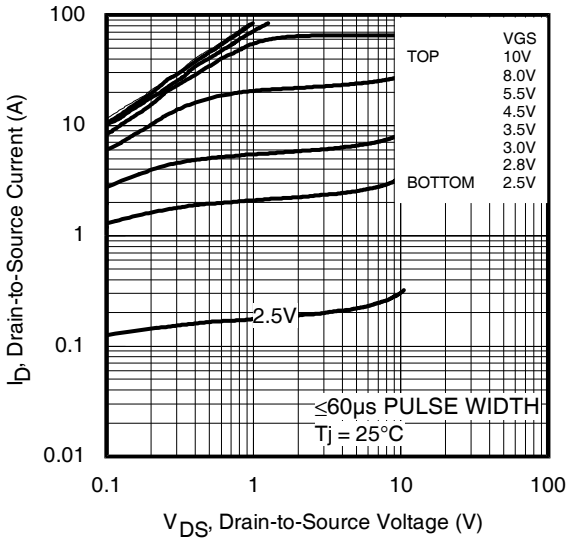


Fig 1. Typical Output Characteristics

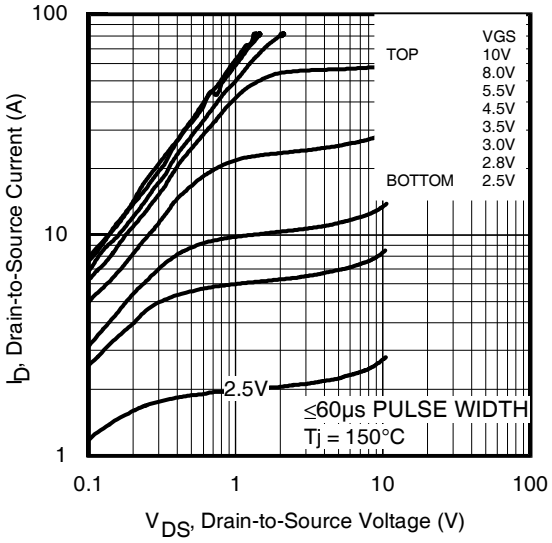


Fig 2. Typical Output Characteristics

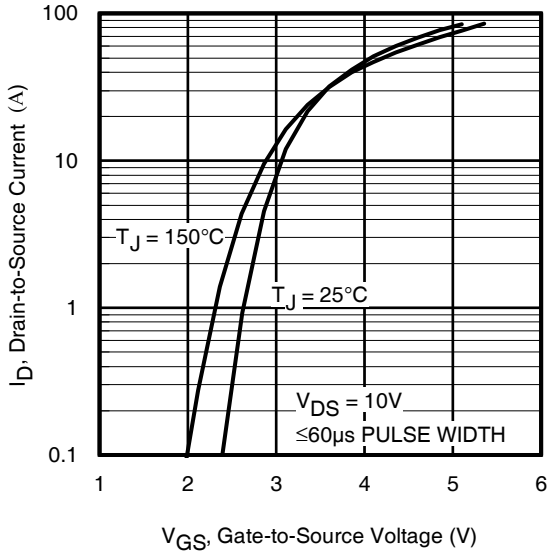


Fig 3. Typical Transfer Characteristics

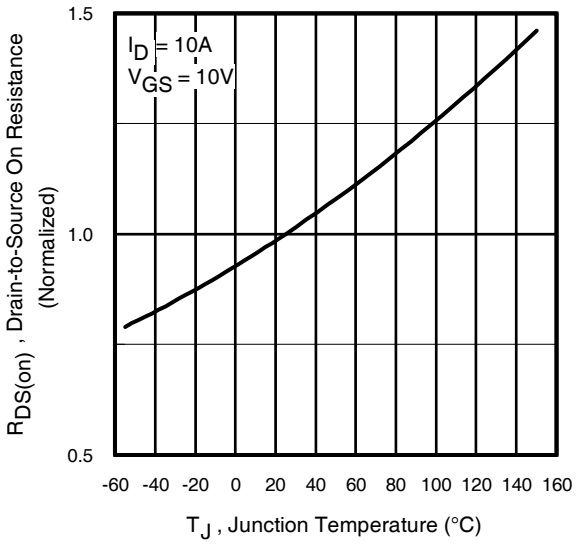


Fig 4. Normalized On-Resistance vs. Temperature

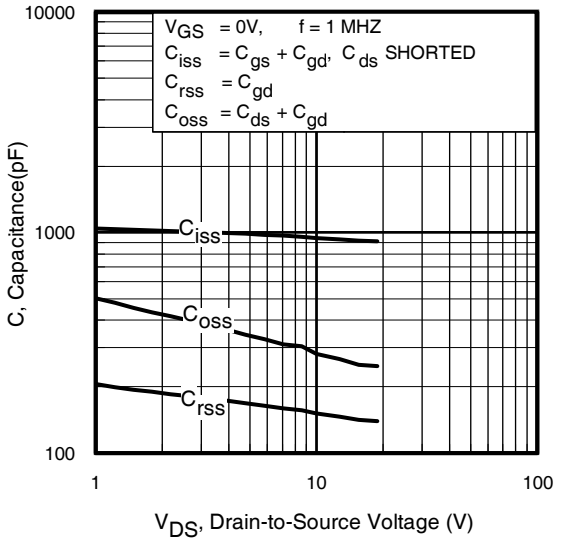


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

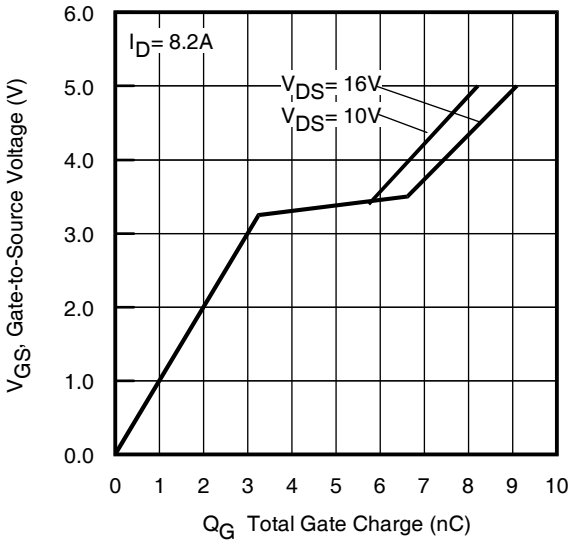


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

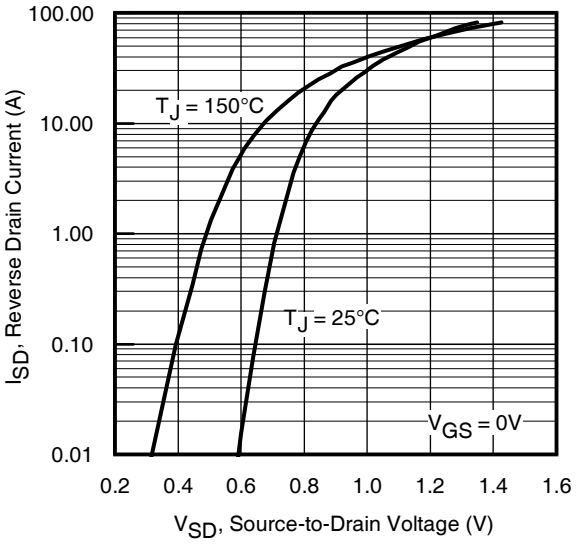


Fig 7. Typical Source-Drain Diode Forward Voltage

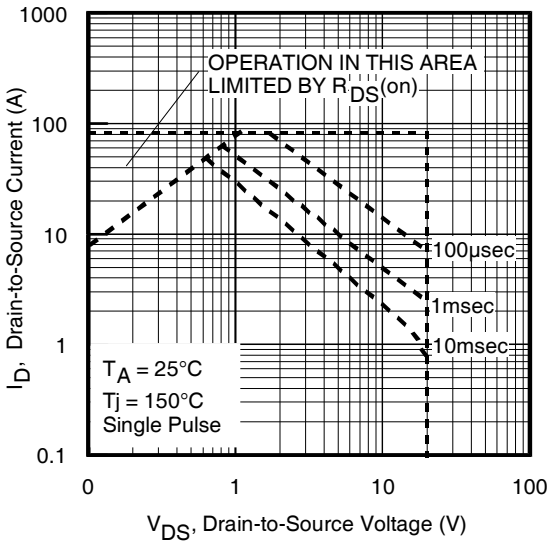


Fig 8. Maximum Safe Operating Area

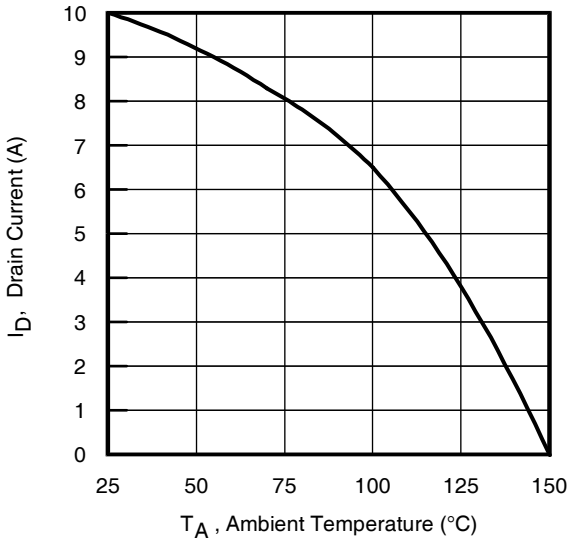


Fig 9. Maximum Drain Current vs. Ambient Temperature

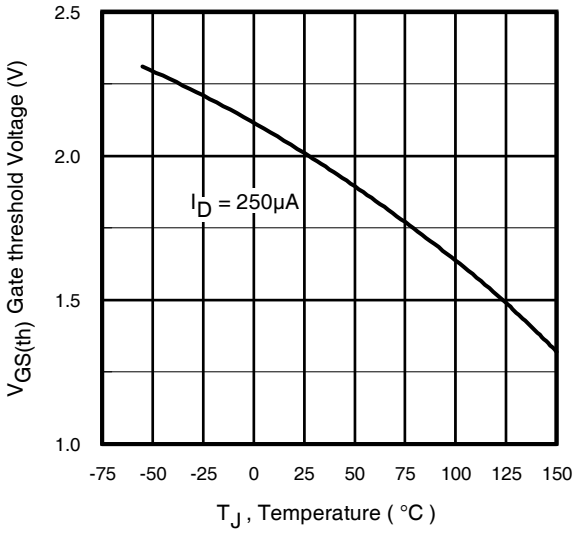


Fig 10. Threshold Voltage vs. Temperature

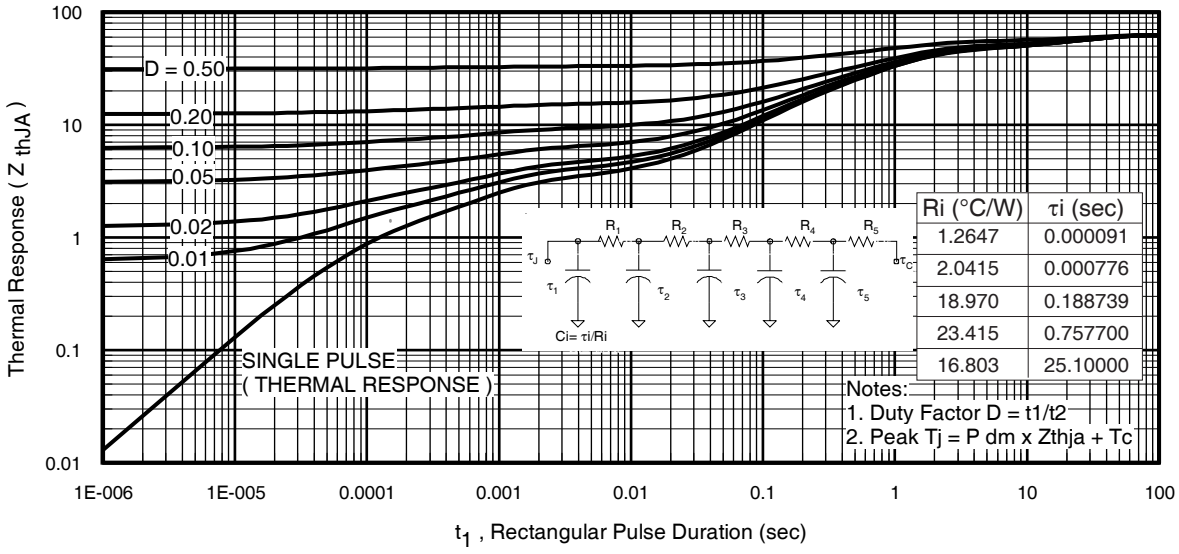


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

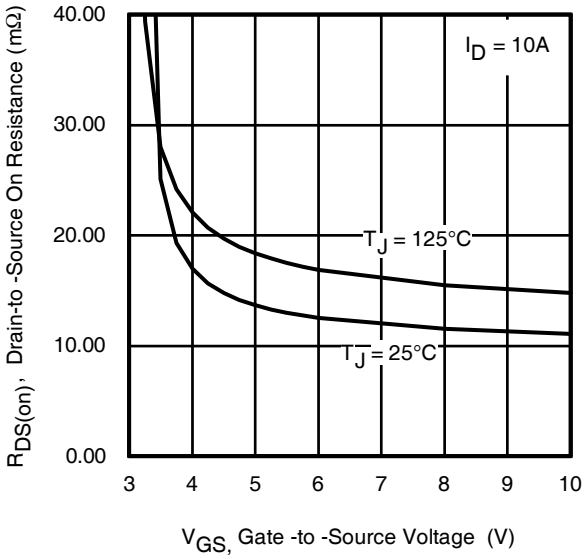


Fig 12. On-Resistance vs. Gate Voltage

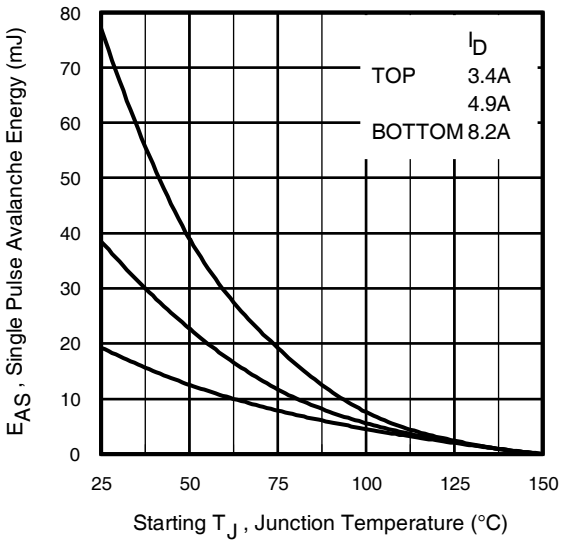


Fig 13. Maximum Avalanche Energy vs. Drain Current

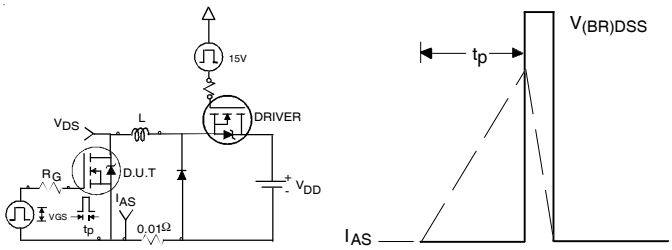


Fig 14. Unclamped Inductive Test Circuit and Waveform

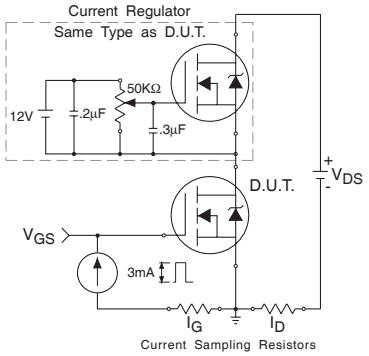


Fig 15. Gate Charge Test Circuit

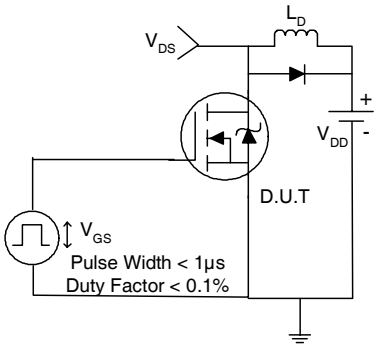


Fig 16. Switching Time Test Circuit

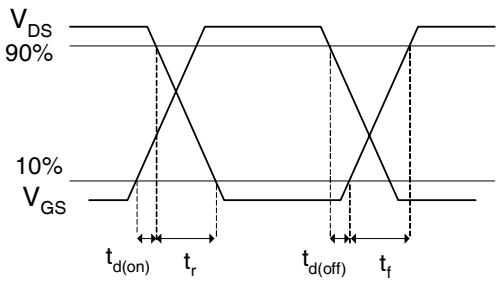


Fig 17. Switching Time Waveforms

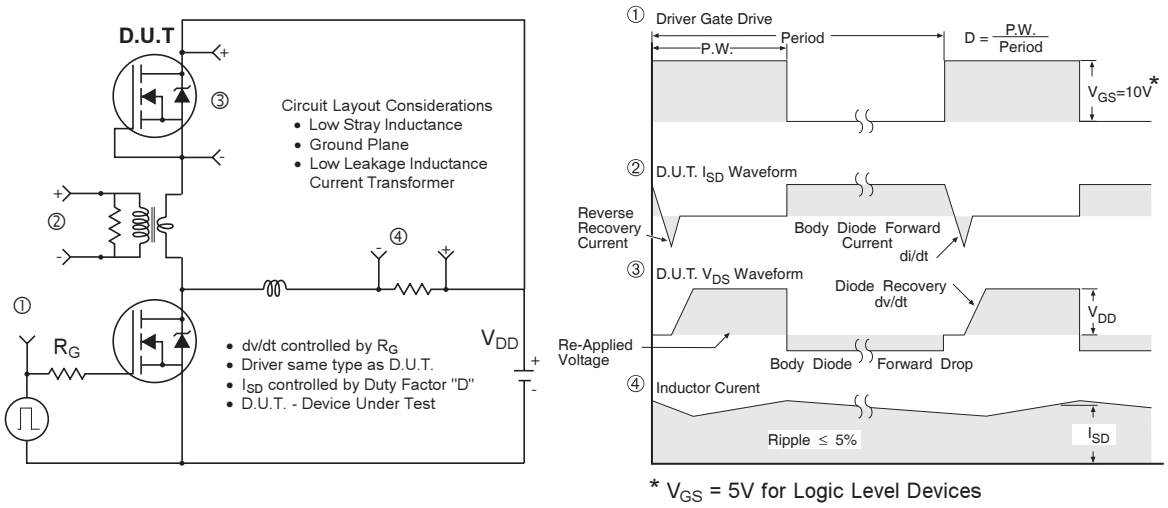


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

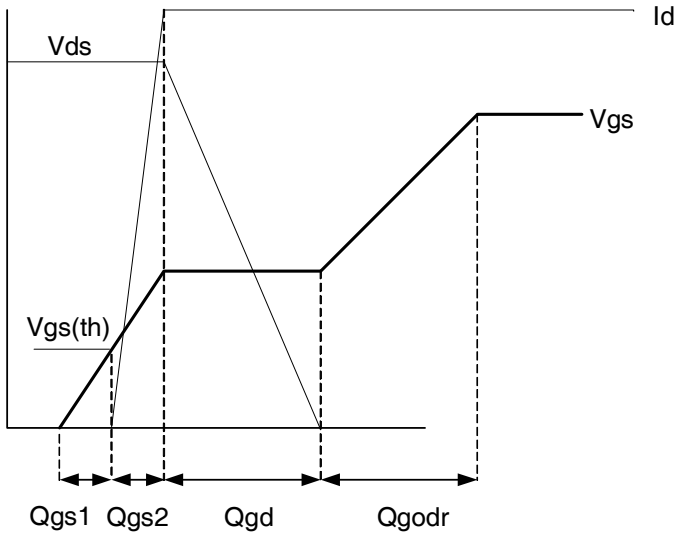


Fig 16. Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P^*_{output}$$

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

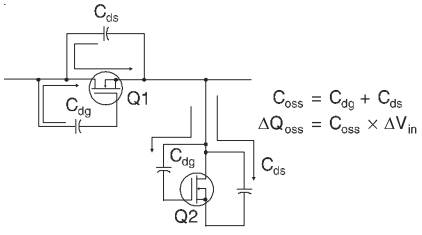
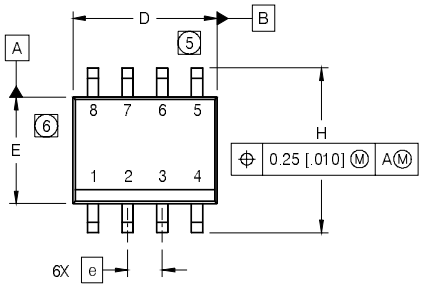


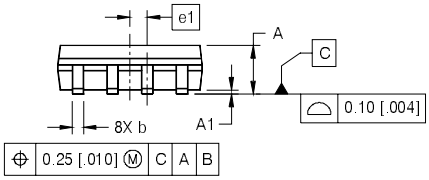
Figure A: Q_{oss} Characteristic

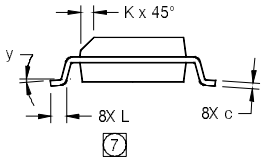
SO-8 Package Outline(Mosfet & Fetky)

Dimensions are shown in milimeters (inches)

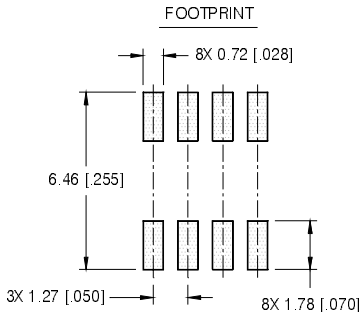


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



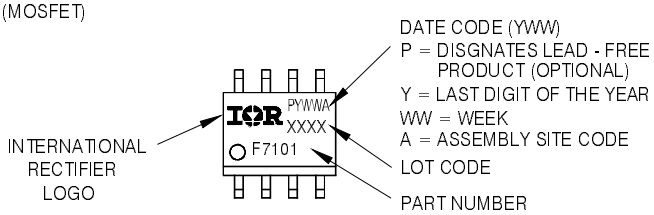


NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



SO-8 Part Marking Information

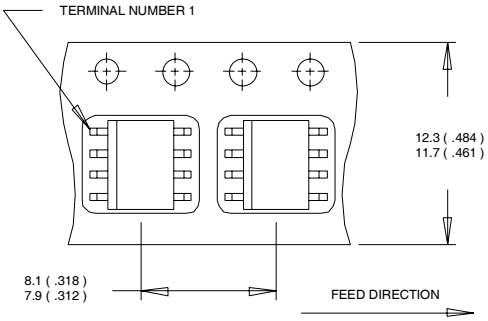
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



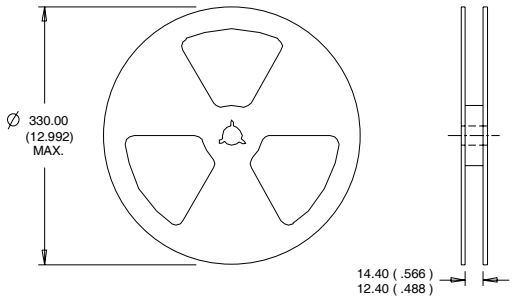
Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

SO-8 Tape and Reel

Dimensions are shown in milimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.57mH, R_G = 25Ω, I_{AS} = 8.2A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board.

⑤ R_θ is measured at T_J of approximately 90°C.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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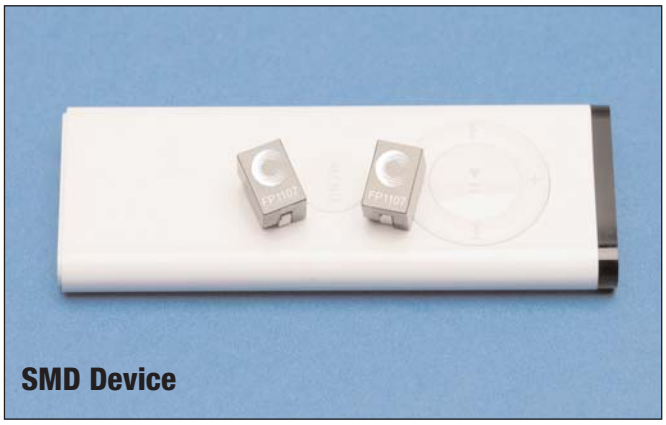


SMD Device

Description:

- Halogen free
- 125°C maximum total temperature operation
- 7.2 x 11.0 x 7.5mm surface mount package
- Ferrite core material
- High current carrying capacity, low core losses
- Controlled DCR tolerance for sensing circuits
- Inductance range from 70nH to 510nH
- Current range from 18 amps to 140 amps
- Frequency range up to 2MHz
- RoHS compliant

Applications:

- Multi-phase regulators
- Voltage Regulator Module (VRM)
- Desktop and server VRMs and EVRDs
- Data networking and storage systems
- Notebook regulators
- Graphics cards and battery power systems
- Point-of-load modules
- DCR sensing

Environmental Data:

- Storage temperature range: -40°C to +125°C
- Operating temperature range: -40°C to +125°C (ambient plus self-temperature rise)
- Solder reflow temperature: J-STD-020D compliant

Packaging:

- Supplied in tape and reel packaging, 640 parts per reel, 13" diameter reel

Product Specifications

Part Number[7]	OCL[1] ± 10% (nH)	FLL[2] Min. (nH)	I_{rms}[3] (Amps)	$I_{sat}1$[4] @ 25°C (Amps)	$I_{sat}2$[5] @ 125°C (Amps)	DCR (mΩ) @ 20°C	K-factor[6]
R1 Version							
FP1107R1-R07-R	70	50	55	140	123	0.29 ± 8%	361.1
FP1107R1-R12-R	120	86		90	72		361.1
FP1107R1-R15-R	150	108		70	56		361.1
FP1107R1-R23-R	230	166		45	36		361.1
FP1107R1-R30-R	300	217		35	28		361.1
FP1107R1-R40-R	400	288		25	20		361.1
FP1107R1-R51-R	510	364		18	14.5		361.1
R2 Version							
FP1107R2-R07-R	70	50	42	140	123	0.47 ± 6.4%	363.3
FP1107R2-R12-R	120	86		90	72		363.3
FP1107R2-R15-R	150	108		70	56		363.3
FP1107R2-R23-R	230	166		45	36		363.3
FP1107R2-R30-R	300	217		35	28		363.3
FP1107R2-R40-R	400	288		25	20		363.3
FP1107R2-R51-R	510	364		18	14.5		363.3

1 Open Circuit Inductance (OCL) Test Parameters: 100kHz, 0.10V_{rms}, 0.0Adc

2 Full Load Inductance (FLL) Test Parameters: 100kHz, 0.1V_{rms}, $I_{sat}1$

3 I_{rms}: DC current for an approximate temperature rise of 40°C without core loss. Derating is necessary for AC currents. PCB pad layout, trace thickness and width, air-flow and proximity of other heat generating components will affect the temperature rise. It is recommended the part temperature not exceed 125°C under worst case operating conditions verified in the end application.

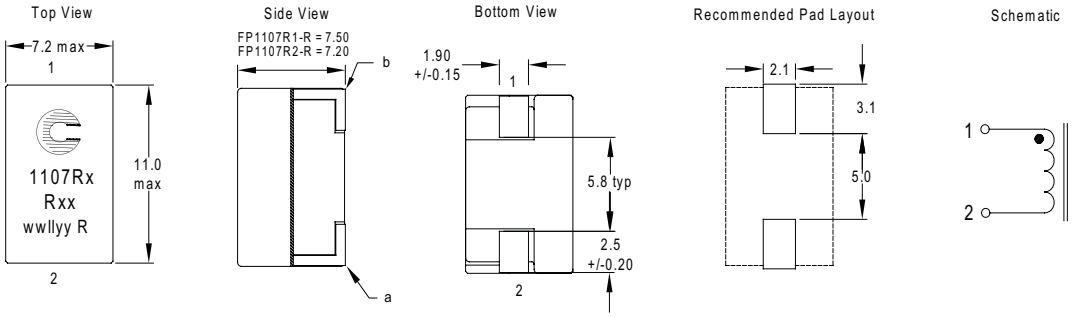
4 $I_{sat}1$: Peak current for approximately 20% rolloff at +25°C.

5 $I_{sat}2$: Peak current for approximately 20% rolloff at +125°C.

6 K-factor: Used to determine B_{p-p} for core loss (see graph). $B_{p-p} = K * L * \Delta I * 10^{-3}$, B_{p-p} : (Gauss), K: (K-factor from table), L: (inductance in nH), ΔI (peak-to-peak ripple current in amps).

7 Part Number Definition: FP1107Rx-Rxx-R
- FP1107 = Product code and size
- Rx is the DCR indicator
- Rxx= Inductance value in µH, R = decimal point
- "-R" suffix = RoHS compliant

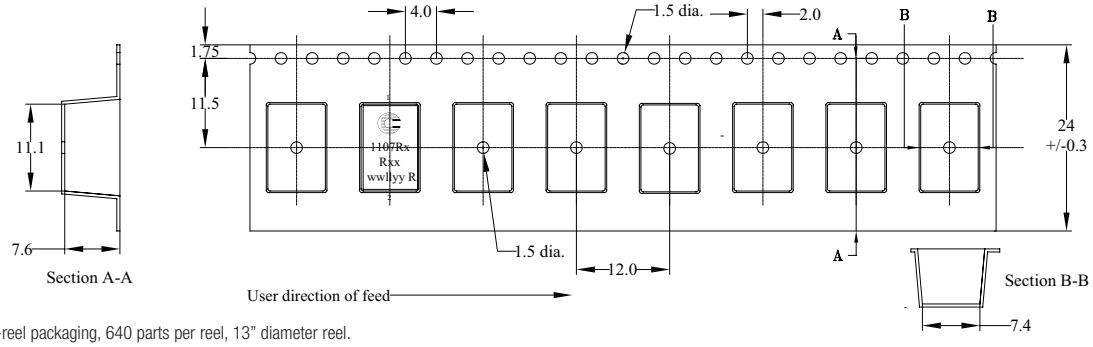
Dimensions - mm



The nominal DCR is measured from point "a" to point"b."

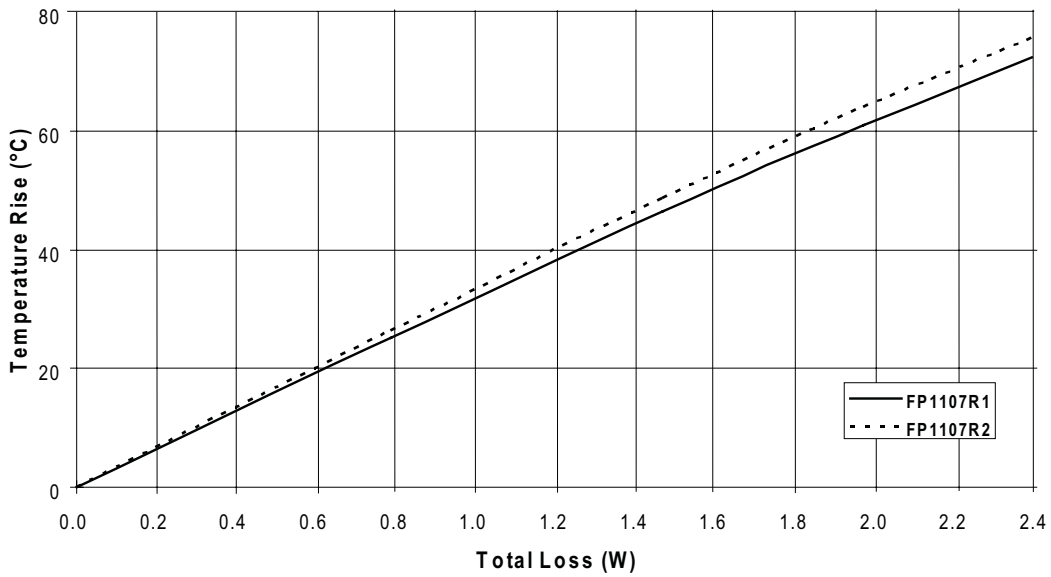
Part Marking: Coiltronics Logo 1107Rx (Rx = DCR Indicator) Rxx = Inductance value in µH. (R = Decimal point) wwllyy = Date code R = Revision level

Packaging Information - mm

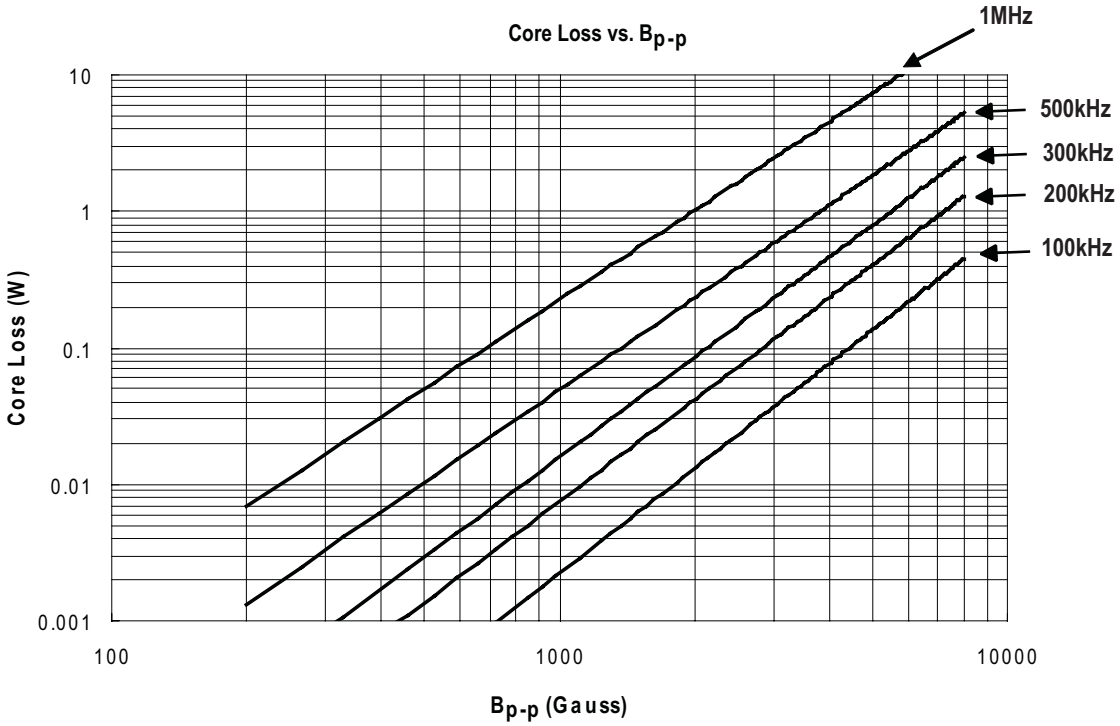


Supplied in tape-and-reel packaging, 640 parts per reel, 13" diameter reel.

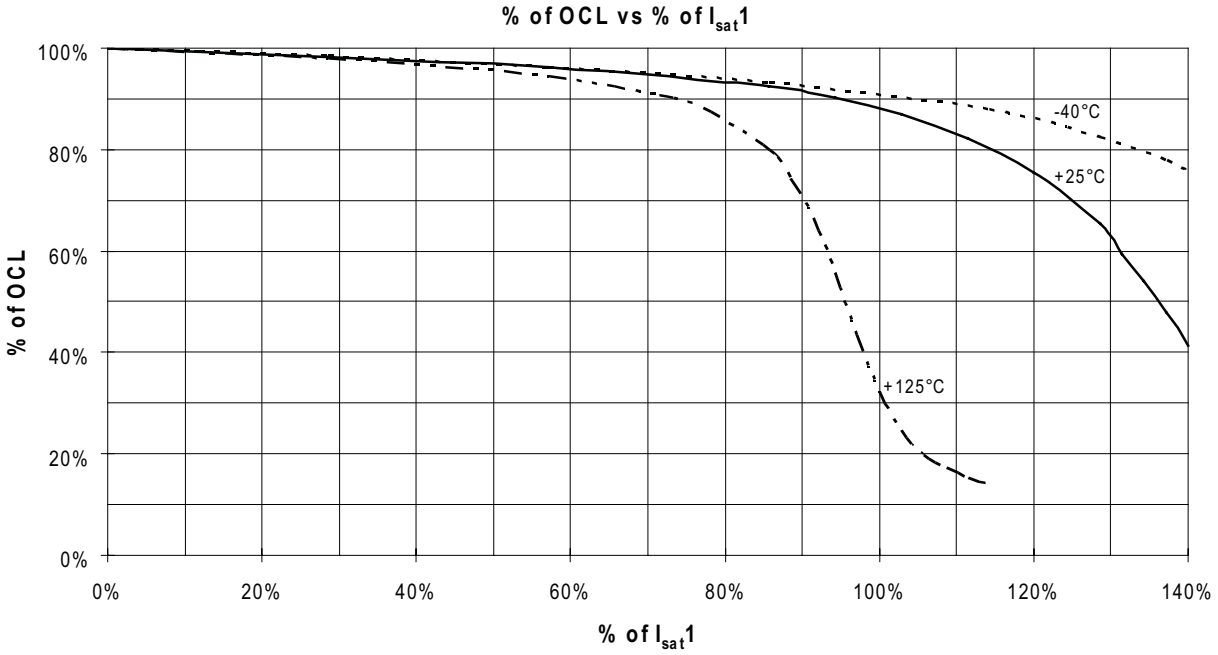
Temperature Rise vs.Total Loss



Core Loss



Inductance Characteristics



Solder Reflow Profile

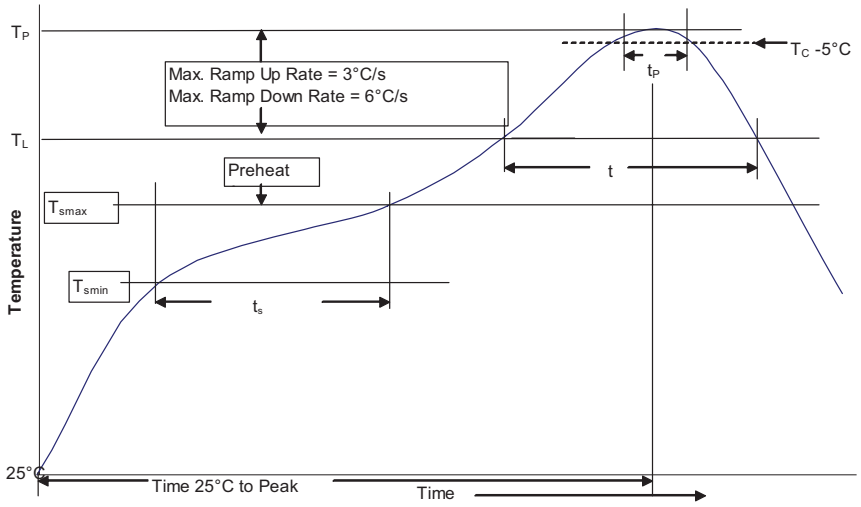


Table 1 - Standard SnPb Solder (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5mm	235°C	220°C
≥2.5mm	220°C	220°C

Table 2 - Lead (Pb) Free Solder (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6mm	260°C	260°C	260°C
1.6 – 2.5mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

Reference JDEC J-STD-020D

Profile Feature		Standard SnPb Solder	Lead (Pb) Free Solder
Preheat and Soak	• Temperature min. (T_{smin})	100°C	150°C
	• Temperature max. (T_{smax})	150°C	200°C
	• Time (T_{smin} to T_{smax}) (t_s)	60-120 Seconds	60-120 Seconds
Average ramp up rate T_{smax} to T_p		3°C/ Second Max.	3°C/ Second Max.
Liquidous temperature (T_L) Time at liquidous (t_L)		183°C 60-150 Seconds	217°C 60-150 Seconds
Peak package body temperature (T_P)*		Table 1	Table 2
Time (t_p)** within 5 °C of the specified classification temperature (T_C)		20 Seconds**	30 Seconds**
Average ramp-down rate (T_p to T_{smax})		6°C/ Second Max.	6°C/ Second Max.
Time 25°C to Peak Temperature		6 Minutes Max.	8 Minutes Max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

North America
Cooper Electronic Technologies
1225 Broken Sound Parkway NW
Suite F
Boca Raton, FL 33487-3533
Tel: 1-561-998-4100
Fax: 1-561-241-6640
Toll Free: 1-888-414-2645

Cooper Bussmann
P.O. Box 14460
St. Louis, MO 63178-4460
Tel: 1-636-394-2877
Fax: 1-636-527-1607

Europe
Cooper Electronic Technologies
Cooper (UK) Limited
Burton-on-the-Wolds
Leicestershire • LE12 5TH UK
Tel: +44 (0) 1509 882 737
Fax: +44 (0) 1509 882 786

Cooper Electronic Technologies
Avda. Santa Eulalia, 290
08223
Terrassa, (Barcelona), Spain
Tel: +34 937 362 812
+34 937 362 813
Fax: +34 937 362 719

Asia Pacific
Cooper Electronic Technologies
1 Jalan Kilang Timor
#06-01 Pacific Tech Centre
Singapore 159303
Tel: +65 278 6151
Fax: +65 270 4160

DFLS220L

2.0A SURFACE MOUNT SCHOTTKY BARRIER RECTIFIER

PowerDI®123

Please click here to visit our online spice models database.

Features

- Guard Ring Die Construction for Transient Protection
- Low Power Loss, High Efficiency
- Patented Interlocking Clip Design for High Surge Current Capacity
- High Current Capability and Low Forward Voltage Drop
- **Lead Free Finish, RoHS Compliant (Note 5)**
- **"Green" Molding Compound (No Br, Sb)**

Mechanical Data

- Case: PowerDI®123
- Plastic Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020D
- Terminal Connections: Cathode Band
- Terminals: Finish – Matte Tin Annealed Over Copper leadframe. Solderable per MIL-STD-202, Method 208 e3
- Marking Information: See Page 2
- Ordering Information: See Page 2
- Weight: 0.01 grams (approximate)

Top View

Maximum Ratings @T_A = 25°C unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load.
For capacitance load, derate current by 20%.

Characteristic	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	V
RMS Reverse Voltage	$V_{R(RMS)}$	14	V
Average Forward Current	$I_{F(AV)}$	2.0	A
Non-Repetitive Peak Forward Surge Current 8.3ms Single Half Sine-Wave Superimposed on Rated Load	I_{FSM}	40	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 1)	P_D	1.67	W
Power Dissipation (Note 2)	P_D	556	mW
Thermal Resistance Junction to Ambient (Note 1)	$R_{\theta JA}$	60	°C/W
Thermal Resistance Junction to Ambient (Note 2)	$R_{\theta JA}$	180	°C/W
Thermal Resistance Junction to Soldering (Note 3)	$R_{\theta JS}$	10	°C/W
Operating Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Breakdown Voltage (Note 4)	$V_{(BR)R}$	20	—	—	V	I_R = 1.0mA
Forward Voltage	V_F	— —	0.32 0.375	0.36 0.42	V	I_F = 1.0A I_F = 2.0A
Leakage Current (Note 4)	I_R	— —	0.26 —	— 1.0	mA	V_R = 5V, T_A = 25°C V_R = 20V, T_A = 25°C
Total Capacitance	C_T	—	75	—	pF	V_R = 10V, f = 1.0MHz

Notes:
1. Part mounted on 50.8mm X 50.8mm GETEK board with 25.4mm X 25.4mm copper pad, 25% anode, 75% cathode. T_A = 25°C.
2. Part mounted on FR-4 board with 1.8mm X 2.5mm cathode and 1.8mm X 1.2mm anode, 1 oz. copper pads. T_A = 25°C.
3. Theoretical $R_{\theta JS}$ calculated from the top center of the die straight down to the PCB/cathode tab solder junction.
4. Short duration pulse test used to minimize self-heating effect.
5. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied, see *EU Directive 2002/95/EC Annex Notes.*

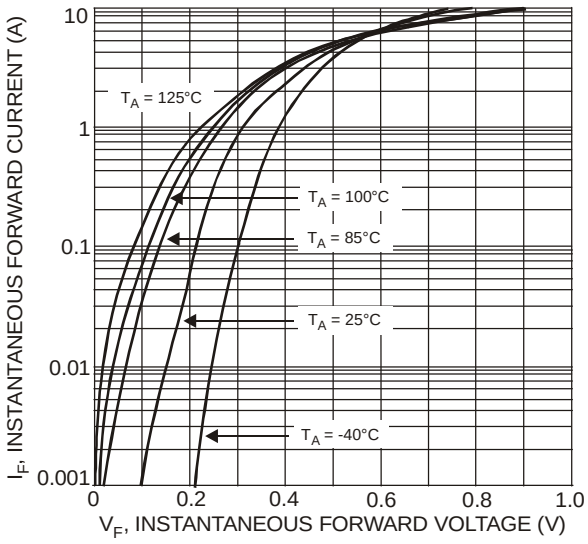


Fig. 1 Typical Forward Characteristics

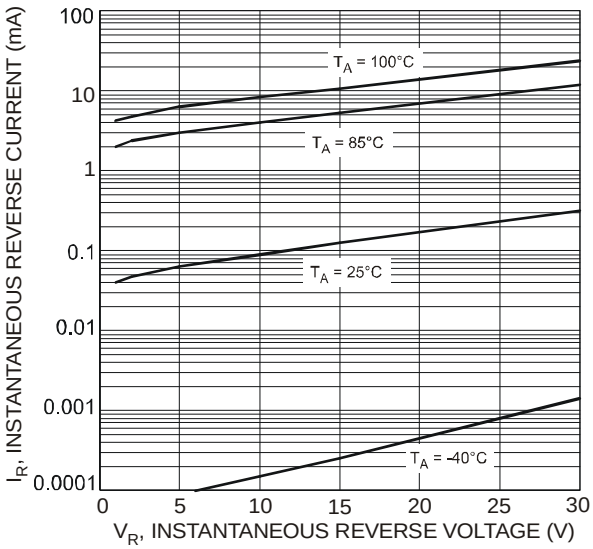


Fig. 2 Typical Reverse Characteristics

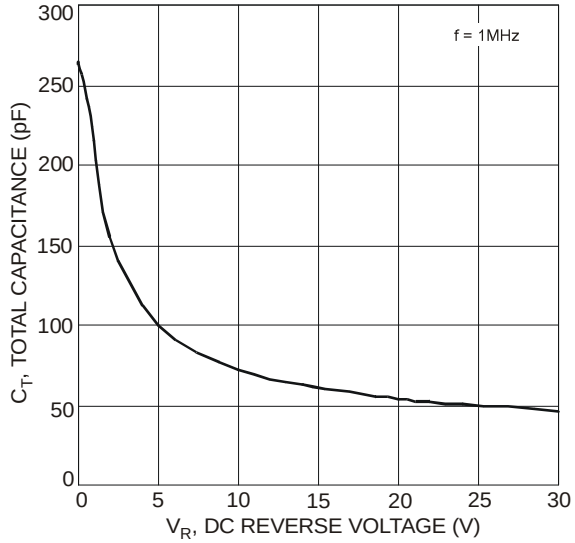


Fig. 3 Total Capacitance vs. Reverse Voltage

Ordering Information (Note 6)

Part Number	Case	Packaging
DFLS220L-7	PowerDI®123	3000/Tape & Reel

Notes: 6. For packaging details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information

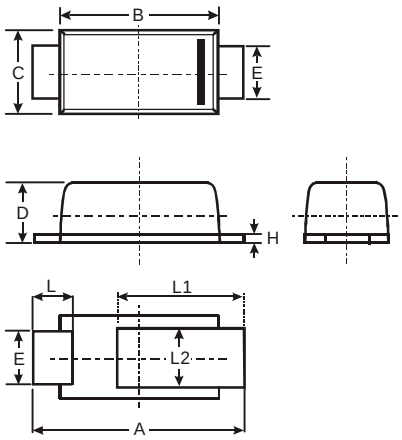
F02A = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: T = 2006)
M = Month (ex: 9 = September)

Date Code Key

Year	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
Code	R	S	T	U	V	W	X	Y	Z	A	B	C

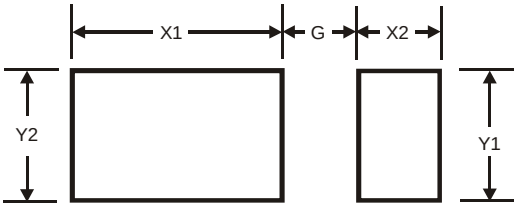
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Package Outline Dimensions



PowerDI®123			
Dim	**Min**	**Max**	**Typ**
A	3.50	3.90	3.70
B	2.60	3.00	2.80
C	1.63	1.93	1.78
D	0.93	1.00	0.98
E	0.85	1.25	1.00
H	0.15	0.25	0.20
L	0.55	0.75	0.65
L1	1.80	2.20	2.00
L2	0.95	1.25	1.10
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
G	1.0
X1	2.2
X2	0.9
Y1	1.4
Y2	1.4

Features

- Power ratings from 0.5 - 3 watts
- Large terminals and optimized body shape for power dissipation
- Excellent surge capabilities
- Low TCR
- RoHS compliant*

Applications

- Telecommunications
- Audio equipment
- Medical equipment
- Base stations
- Industrial equipment

PWR2010/3014/4318/5322 - Surface Mount Wirewound Resistors

General Information

The PWR2010/3014/4318/5322 Series surface mount wirewound resistors boast a high power density and excellent pulse power characteristics. They can be used in a wide range of applications where surge voltages or inrush currents are present.

Electrical Characteristics

Parameter	PWR2010	PWR3014	PWR4318	PWR5322
Power	0.5 W	1.0 W	2.0 W	3.0 W
Resistance Range	0.1 Ω - 1K Ω	0.1 Ω - 4K Ω	0.1 Ω - 8K Ω	0.1 Ω - 15K Ω
Tolerance	0.5 % / 1 % / 5 %			
Temperature Coefficient 0.1 - 0.99 Ω 1.0 - 10 Ω >10 Ω	 ±90 PPM/˚C ±50 PPM/˚C ±20 PPM/˚C			
Operating Temperature	-55 ˚ to 155 ˚C			
Maximum Voltage	√P*R			

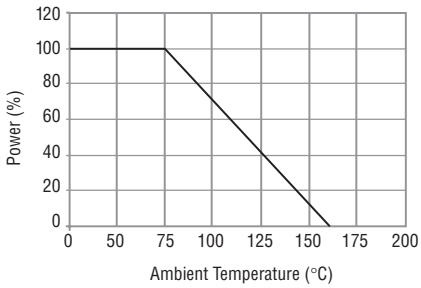
Environmental Characteristics

Test	Description	Specification
Thermal Shock	-55 +0 °C/-3 °C to 150 °C +3 °C/-0 °C, 5 cycles, with minimum 15 minutes at each cycle	ΔR ±(2.0 % +0.05 Ω)
Short Time Overload	Five times rated power for 5 seconds	ΔR ±(0.5 % +0.05 Ω)
Solderability	Immersion in solder 260 °C ±5 ˚C for 5 ±0.5 seconds	90 % of contact covered in solder
Resistance to Solder Heat	Immersion in solder 260 °C ±5 ˚C for 5 ±0.5 seconds	ΔR ±(0.5 % +0.05 Ω)
Dielectric Strength	Test voltage >500 Vrms for greater than 1 minute	Pass
Insulation Resistance	Test voltage greater than 500 Vrms for one minute	>1000 GΩ
High Temperature Exposure	Ambient temperature of 175 °C +5 ˚C/-0 ˚C for 250 ±8 hours	ΔR ±(2.0 % +0.05 Ω)
Low Temperature Exposure	Ambient Temperature of -65C ±2C for 24 hours ±4 hours	ΔR ±(2.0 % +0.05 Ω)
Load Life	Rated continuous voltage for 1000 hours (1 hour on and 0.5 hours off) at a test temperature of 70°C ±2 °C	ΔR ±(2.0 % +0.05 Ω)

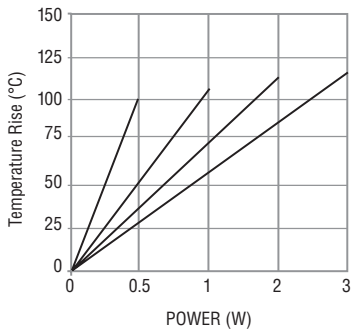
Physical Characteristics

Body Material ..... Epoxy resin
Lead Frame ....100 % Sn Plated Copper

Power Derating Curve



Temperature Rise



Asia-Pacific:
Tel: +886-2 2562-4117
Fax: +886-2 2562-4116

Europe:
Tel: +41-41 768 5555
Fax: +41-41 768 5510

The Americas:
Tel: +1-951 781-5500
Fax: +1-951 781-5700

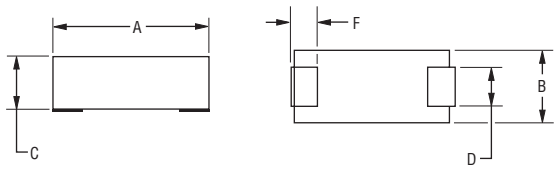
www.bourns.com

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex.
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications

PWR2010/3014/4318/5322 - Surface Mount Wirewound Resistors

BOURNS®

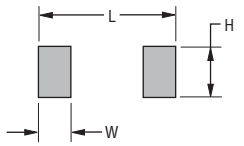
Product Dimensions



DIMENSIONS: MM (INCHES)

TOLERANCE: ± 0.508 (0.02)

Recommended Pad Layout

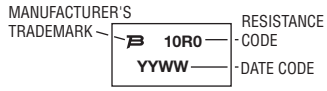


Model	A	F	L	C	B	D	W	H
PWR2010	5.08 (0.20)	1.28 (0.05)	6.48 (0.255)	3.25 (0.128)	2.54 (0.10)	1.663 (0.065)	1.98 (0.078)	2.16 (0.085)
PWR3014	7.5 (0.29)	1.75 (0.069)	8.9 (0.35)	4.64 (0.183)	3.50 (0.138)	2.405 (0.095)	2.45 (0.096)	2.95 (0.116)
PWR4318	11.0 (0.43)	2.00 (0.079)	12.5 (0.49)	4.65 (0.189)	4.50 (0.177)	3.590 (0.141)	3.20 (0.126)	3.70 (0.146)
PWR5322	13.5 (0.53)	2.50 (0.098)	14.9 (0.587)	5.65 (0.229)	5.50 (0.217)	4.20 (0.165)	3.70 (0.146)	4.20 (0.165)

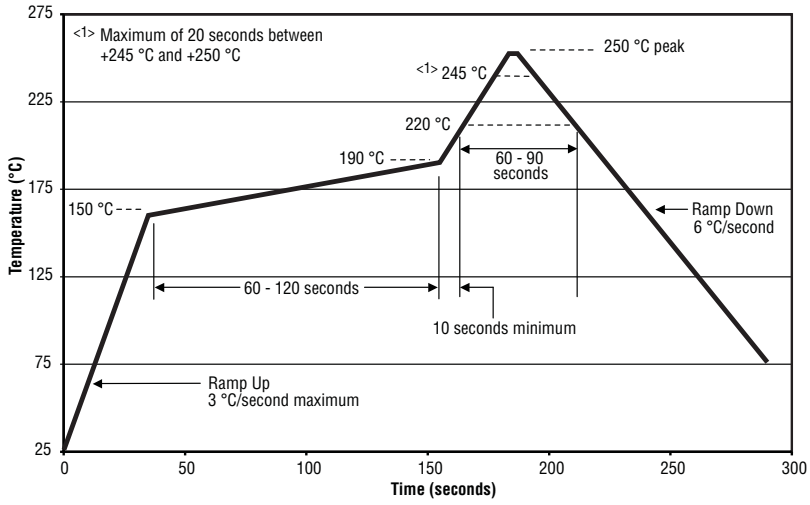
Packaging Specifications

Model	Tape Width	Reel Diameter	Pieces per Reel	Bulk Pkg. Quantity
PWR2010	12.0 (0.472)	330 (13.0)	2500	200
PWR3014	16.0 (0.629)		1500	200
PWR4318	24.0 (0.945)		1500	100
PWR5322	24.0 (0.945)		1500	100

Typical Part Marking



Soldering Profile



How to Order

PWR4318 W __ 10R0 J E

Model
- PWR2010
- PWR3014
- PWR4318
- PWR5322

Type
- W = Wirewound

Special Version
- Blank = Default

Resistance Value
- <100 ohms ... "R" represents decimal point (examples: 7R50 = 7.5 Ω; R050 = 0.050 Ω)
- ≥100 ohms ... First three digits are significant, fourth digit represents number of zeros to follow (examples: 2000 = 200 ohms; 2002 = 20K ohms)

Resistance Tolerance
- J = 5 %
- F = 1 %
- D = 0.5 %

Packaging
- E = Tape & Reel
- Blank = Bulk

REV. 07/09