DIGITALLY ASSISTED TECHNIQUES FOR NYQUIST RATE ANALOG-to-DIGITAL CONVERTERS

by

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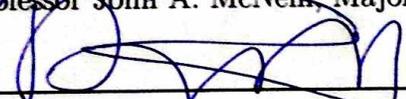Electrical and Computer Engineering

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Abstract

With the advance of technology and rapid growth of digital systems, low power high speed analog-to-digital converters with great accuracy are in demand. To achieve high effective number of bits Analog-to-Digital Converter(ADC)calibration as a time consuming process is a potential bottleneck for designs. This dissertation presents a fully digital background calibration algorithm for a 7-bit redundant flash ADC using split structure and look-up table based correction.

Redundant comparators are used in the flash ADC design of this work in order to tolerate large offset voltages while minimizing signal input capacitance. The split ADC structure helps by eliminating the unknown input signal from the calibration path. The flash ADC has been designed in 180nm IBM CMOS technology and fabricated through MOSIS. This work was supported by Analog Devices, Wilmington,MA.

While much research on ADC design has concentrated on increasing resolution and sample rate, there are many applications (e.g. biomedical devices and sensor networks) that do not require high performance but do require low power energy efficient ADCs. This dissertation also explores on design of a low quiescent current 100kS/s Successive Approximation (SAR) ADC that has been used as an error detection ADC for an automotive application in 350nm CD (CMOS-DMOS) technology. This work was supported by ON Semiconductor Corp, East Greenwich, RI.

Acknowledgments

It has been a great experience for me to study at Worcester Polytechnic Institute and a great honor to be a student of Professor John McNeill for almost five years. Over this period of time, I have gained experience in both teaching and doing research. His special method of guiding his students without providing them with immediate solutions for their problems helped me in becoming an independent researcher. I also was a teaching assistant for the major analog courses that Professor McNeill teaches at WPI and I think I have learned a lot from him during that time. His support for attending the International Solid-State Circuits Conference (ISSCC) which is a great conference about leading edge research in analog IC design has motivated me to pursue a high professional standard during my PhD research.

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My special thanks go to ON Semiconductor, East Greenwich RI, for supporting my PhD dissertation. I have been working at ON Semiconductor as an internship-Co-op employee and have taped-out the ultra-low power SAR ADC under direct supervision of Robert Davis, design manager in switching mode power supply group. I would like to thank him for his significant help in explaining the application of this ADC and all his help through implementation, tape-out and test chip evaluation. I also had the experience of working at ON Semiconductor as an Analog DFT validation Engineering Intern and have become familiar with various test methods under supervision of Andrew Laidler which gave me much insight into making a robust design. Many thanks to him for all his support on evaluating my test chip. I must say thank you to my other colleagues who were available to help me to manage this work. Thanks to: Shelby Raymond, Andrew Tarlan, Paul Gunaratnam, Alpha Diallo for the analog design advice, Wai Yung for digital design advice, Jon Buzzi for helping with the layout of SAR ADC, Justin Yerger for his help with using a microscope with laser to remove passivation layer and burn trim fuses, Betty Podgorski for bonding out the test chip, Marie Crowley for help with Mentor graphic software maintenance, Jayson Busila for his advice on PCB design, and Robert Cushing for his help with using the needle probes and all the test set up.

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Chapter 1

Introduction

1.1 Motivation

Analog-to-Digital Converters (ADCs) are employed to digitize continues analog signals into digital form with a certain number of bits of resolution. With the fast shrinking of CMOS process and rapid advance of digital integrated circuit technologies, high-performance low-cost ADCs are needed in many mixed-signal applications such as communications, software radio, audio, video and sensors [10]. Particularly, wireless receivers as well as high-density disk drives [11] require efficient, high speed, low-to-moderate resolution (5-8 bits) data conversion with a low jitter sample clock. Flash ADCs are typically excellent candidates for these types of applications [11] as the simple analog structure of flash ADCs enhances the feasibility to data converter design with technology scaling.

Designing in a deep submicron process enables high speed but at the price of increasing variation and device mismatch, which leads to decreasing the ADC effective number of bits (ENOB) and affecting the ADC accuracy. Increasing the device size will help with recovering the ENOB by improving matching, at the cost of increasing area and power consumption. Flash ADCs are composed of multiple comparators working in parallel, and device mismatch can cause offset error in each comparator and affect differential and integral nonlinearity (DNL and INL)of the ADC. There are several techniques for calibration found in Flash converters in order to mitigate the offset errors of comparators such as averaging and digitally controlled trimming [11] and combinations of analog and digital techniques have been used to calibrate and correct the output of the ADCs.

Technology scaling has a great impact on area and power consumption of integrated circuits. The power consumption of ADCs is a function of the technology node, the linearity and bandwidth [12]. In general, ADC design methods, that preserve the signal-to-noise ratio with scaling will increase the power consumption and area [12].Flash architectures with moderate resolutions are not challenged by noise requirements due to their low resolution [12]. However, power consumption of the multiple comparators and calibration circuits increase ADC power consumption

and on-chip error correction circuits increase the design complexity. This has lead to a motivation of the first part of this research on calibration of flash ADCs and improving the performance and accuracy of this type of data converter.

In some applications such as wireless sensor networks and biomedical devices [13] and electronic features in modern vehicles, power consumption is the primary concern while speed is of a secondary importance. The second half of this research focuses on a portion of the SAR ADC design that has moderate resolution and speed, but is ultra low power. This SAR ADC has been used as an error detection ADC in a feedback loop. This work explores the opportunity for further improvement in power with a new algorthim using capacitive DAC and area savings by eliminating the differential approach in favor of a single-ended architecture.

1.2 Goals

The goal of the first part of this work is to develop a digital background calibration algorithm applying a "Split-ADC" calibration structure and lookup-table-based correction. Traditional methods used for offset improvements in comparators are based on increasing the size of the device according to Pelgrom matching formula [14]; while in this work small, power efficient comparators are used to design 7-bit flash ADC in order to minimize the ADC input capacitance. Redundancy is used to tolerate the large offset voltage of digital regenerative comparators. Digital background calibration is used to reduce analog complexity. The background approach estimates the error iteratively using least mean squares procedure and can be useful for any changes in threshold voltage of the comparators due to temperature variations or device mismatch.

The goal of the second part of this work is to present the design of a 7-bit SAR ADC that is used as a regulation ADC in a switching mode voltage regulator that uses a digital algorithm. The ADC is used as an error detection in a feedback loop. This design only has $4\mu A$ current budget for this ADC. The ADC has been designed and fabricated at ON Semiconductor Corp.

1.3 Dissertation Organization

The remainder of this dissertation is organized as follows: Chapter 2 will describe flash ADC, SAR ADC and split ADC structures and address ADC characterization and nonidealities while summarizes some previous flash ADC calibration, SAR ADC low power design methods and split ADC techniques. In chapter 3 digital calibration of flash ADC will be discussed. Chapter 4 will present design aspects of the flash ADC designed for the test chip. Evaluation board for the test chip and measurement results are given in chapter 5. The proposed algorithm for the ultra low power SAR ADC and details on implementation of SAR ADC are presented in chapter 6. Testing and measurement results of the SAR ADC are shown in chapter 7. Chapter

8 summarizes and concludes this dissertation and proposes the directions for future research.

Chapter 2

Background

2.1 ADC Characterization

An analog-to-digital converter (ADC) is used to convert a continuous-time signal to a digital number that represents its discrete amplitude. Any method of digitizing the analog signal introduces some error. The quantization error and ADC nonidealities are discussed in section 2.2. ADC performs the conversion by sampling the real world analog signal periodically. The number of conversions that ADC is needed to convert analog input to the digital code within a specific time is called sampling rate. For example, 100kS/sec ADC collects hundred thousand samples in a second of time.

Resolution of an ADC is the number of output levels of quantizing an analog signal and it is given in powers of 2 as the output of a ADC comes in binary format. A 7-bit ADC represents the analog input using 2^7 or 128 quantization levels. ADC needs a reference voltage to digitize the analog signal and divides the reference voltage into small quantization levels. The smallest quantization level that ADC can resolve called the least significant bit (LSB) and it is defined as [5]:

$$LSB = \frac{V_{ref}}{2^N} \tag{2.1}$$

For an ADCs with a differential voltage reference LSB is defined as [15]:

$$LSB = \frac{V_{ref(+)} - V_{ref(-)}}{2^N} \tag{2.2}$$

where $V_{ref(+)}$ and $V_{ref(-)}$ are the non-inverting voltage reference and the inverting voltage reference respectively. Full scale of an ADC is defined as:

$$V_{FS} = V_{ref} - 1LSB \tag{2.3}$$
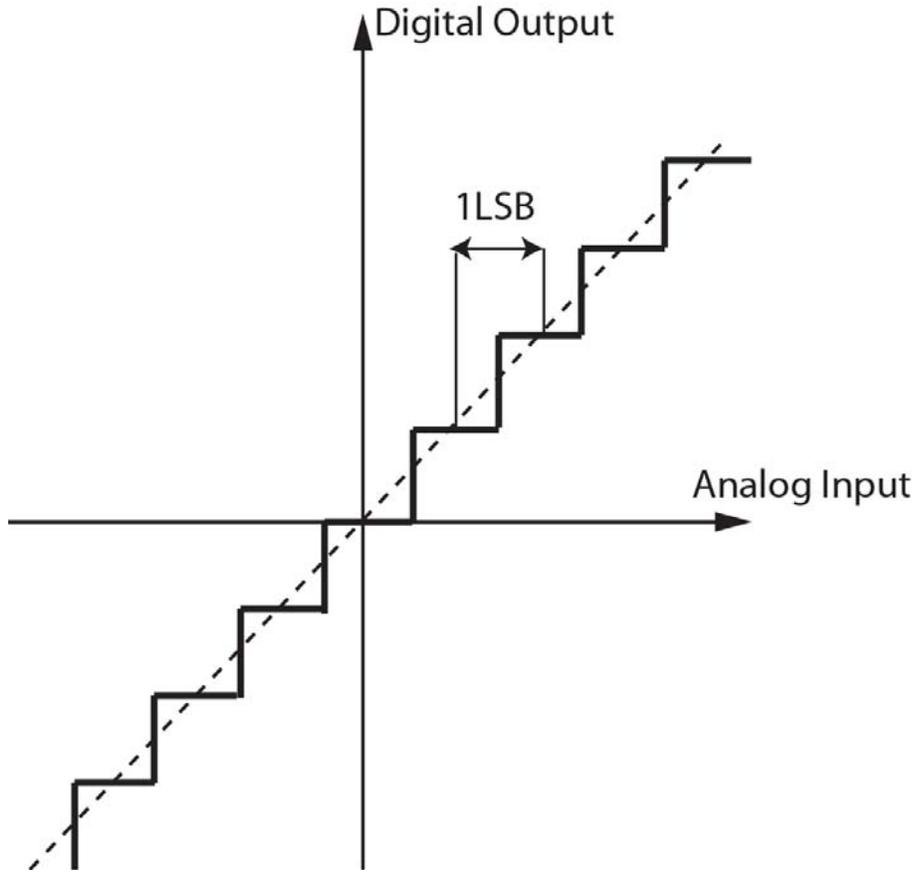
Figure 2.1: Ideal ADC transfer function

Meaning that ADC input can get very close to V_{ref} but it never reaches its reference

voltage [15]. The LSB in terms of FS using (2.1) and (2.3) is:

$$LSB = \frac{V_{FS}}{2^N - 1} \tag{2.4}$$

An ideal ADC transfer function is illustrated in Fig 2.1. The Y-axis shows the ADC digital output and X-axis is the analog input. The quantized value of the analog input is represented by the diagonal staircase [16]. The distance between two successive transition points is defined as $1LSB$ as shown in Fig 2.1.

The ADC is also characterized by its bandwidth and signal-to-noise ratio (SNR). The former is the frequency range that ADC can measure and defines the sampling rate of the ADC; the latter is the ratio of the measured signal to its introduced noise. Accuracy and linearity limit how well the quantizatized output can match the real world signal. The dynamic range of an ADC is specified by its

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effective number of bits (ENOB). ENOB is equal to the ADC resolution in an ideal condition. The ideal dynamic range can be defined as the ratio of the full scale input to the smallest quantization level. Assuming most of the input signals are sinusoidal, dynamic range for an ideal N-bit converter can be calculated as [5]:

$$Dynamic\ Range(dB) \approx 6.02N + 1.76 \qquad (2.5)$$

More details on deriving (2.5) are presented in Section 2.2. Further details on using this equation are outlined in [1].

2.2 ADC Nonidealities

The ideal ADC has a linear transfer function as shown in Fig 2.1. However, real ADC performance is degraded by several error sources. Quantization, offset, gain, timing and non-linearity are common type of those errors.

2.2.1 Quantization Error

If changes in the input signal applied to the ADC are very small (¡1LSB) and cannot be detected by the converter, quantization error is occurred. Fig 2.2 illustrates the quantization error of ideal N-bit ADC. This sawtooth waveform as error signal $e(t)$ is the difference between the analog input signal and the quantized output signal [16]. The maximum error an ideal ADC makes during the conversion is $\pm\frac{1}{2}$ LSB.

The root-mean-square quantization error is [1]:

$$rms \quad quantization \quad error = \sqrt{\overline{e^2(t)}} = \frac{q}{\sqrt{12}} \qquad (2.6)$$

From (2.6)and (2.7)the SNR for N-bit ADC can be calculated (assuming a full-scale input sine wave) as:

$$full-scale \ sinewave = v(t) = \frac{q \times 2^N}{2} sin(2\pi ft) \qquad (2.7)$$

$$SNR = 20log_{10}\left(\frac{rms \ full-scale \ input \ power}{rms \ quantization \ noise \ power}\right) = 20log_{10}\left(\frac{\frac{q2^N}{2\sqrt{2}}}{\frac{q}{\sqrt{12}}}\right) \qquad (2.8)$$

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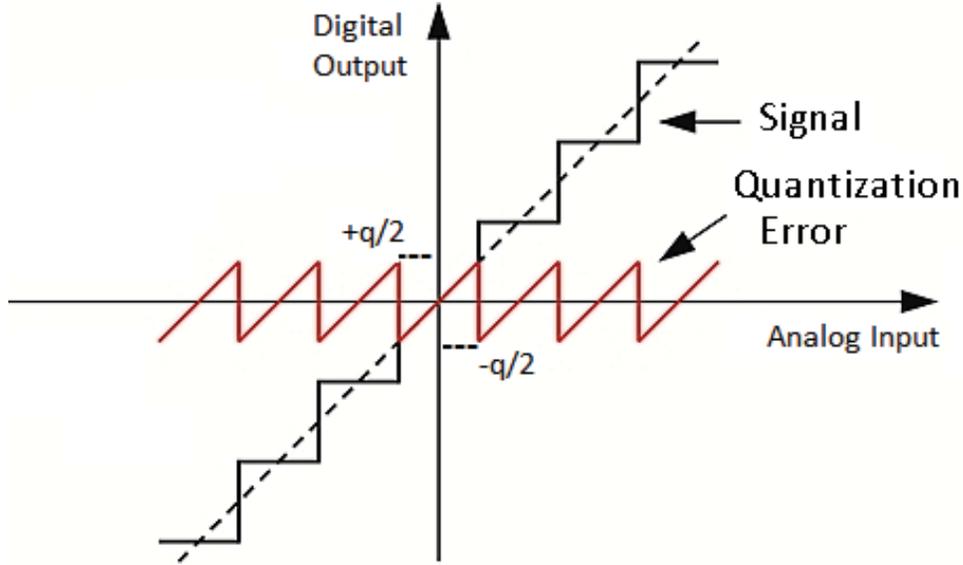
Figure 2.2: Quantization Error as a function of input voltage [1]

$$SNR = 6.02N + 1.76dB \qquad (2.9)$$

It is important to know that in (2.9) rms quantization error is estimated over the full Nyquist bandwidth, dc to $\frac{f_s}{2}$ where f_s is the sampling frequency. If the signal of interest has a smaller bandwidth (BW)or any noise shaping method is used to filter out the noise components, then a correction factor(called process gain) [1] needs to be added to rms quantization error equation. Therefore this correction factor results in increased SNR and we have [1]:

$$SNR = 6.02N + 1.76dB + 10log_{10}\left(\frac{f_s}{2 \times BW}\right) \qquad (2.10)$$

ENOB can be calculated from (2.9) as:

$$ENOB = \frac{SNR - 1.76 \ dB}{6.02} \qquad (2.11)$$

2.2.2 Offset and Gain Error

The fixed difference between input and output signals due to device mismatch or other nonidealities of the components of the ADC shifts the transfer function and
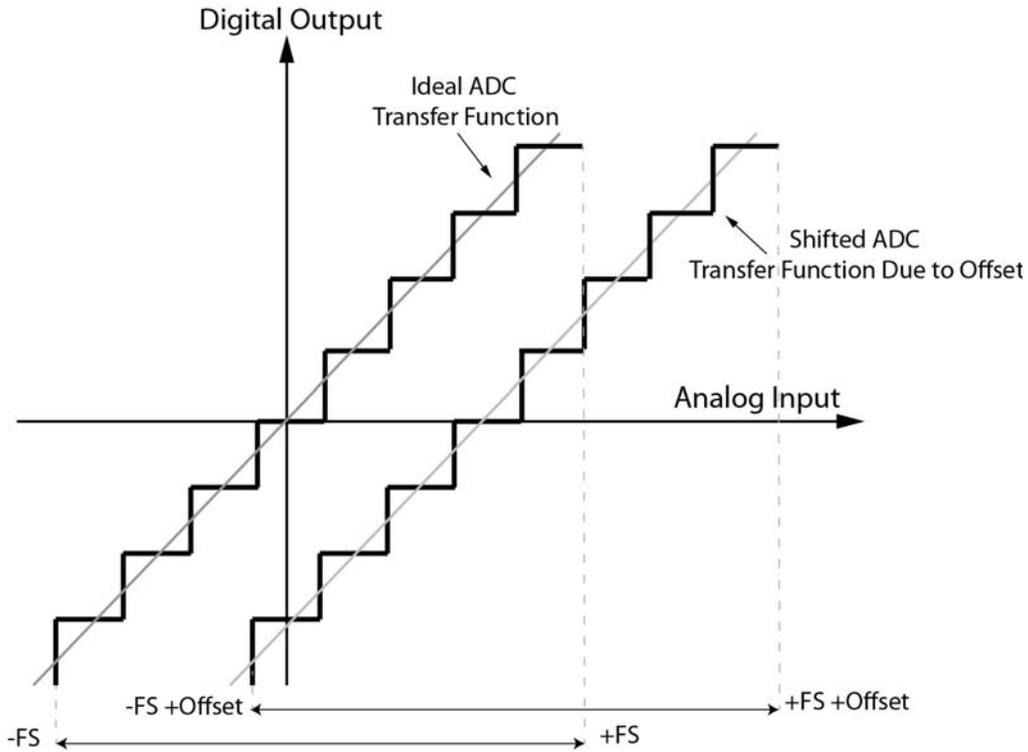
Figure 2.3: ADC Offset error

causes offset error. If the slope of the real ADC transfer function varies from the slope of the ideal ADC transfer function, gain error has occured, as typically happens when an on-chip reference is used. In an ideal ADC when the full-scale input is applied the result of the conversion is all ones. In an ADC with gain error, all ones is the result of applying a voltage greater than full-scale (negative gain error) or a voltage less than full-scale (positive gain error). The ADC transfer function with offset and gain errors is shown in Fig.2.3 and 2.4.

Offset and gain errors can be calibrated by shifting the x and y axes of the transfer function to align the zero points of the real and ideal ADC transfer function and that will remove the offset error and then by rotating the transfer function about the new zero point the gain error can be adjusted.

2.2.3 Nonlinearity Error

Integral nonlinearity (INL) and differential nonlinearity (DNL) are two of the accuracy parameters for testing ADC performance. DNL error reveals how far an actual quantization step width is from the ideal value of $1LSB$, as in an ideal ADC each quantization step of a converter are spaced exactly $1LSB$ apart. The distance between an actual step width and the ideal value is measured in a form of a change in input-voltage magnitude and represents in LSB units after removing static gain

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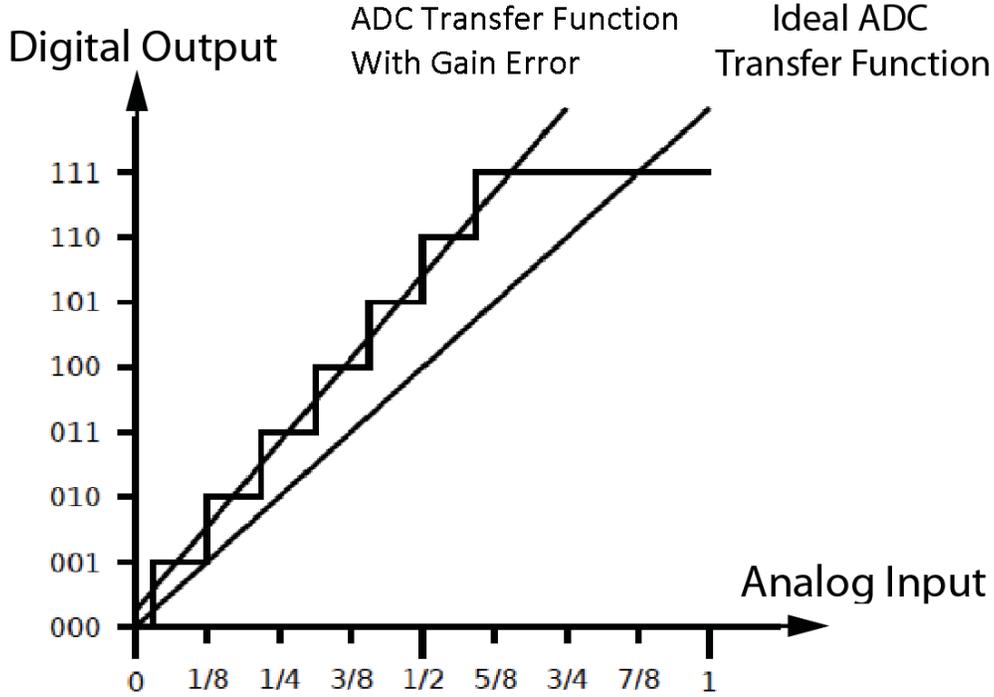
Figure 2.4: ADC Gain error

errors,therefore for an ideal ADC DNL is equal to $0LSB$. For example, if the input signals increases only $\frac{7}{8}LSB$ and the output changes levels, the DNL error is $-\frac{1}{8}LSB$ for this transition. Any DNL error of less than or equal to $1LSB$ guarantees a monotonic transfer function with no missing codes. If DNL reaches $-1LSB$, quantization step is skipped and a missing code (is also known as missing-transition levels [17] (MTLs)is occured [1]. Positive DNL values gives rise to wide codes, or missing-decision levels (MDLs). In an ideal case, for every $1LSB$ interval, only one decision level (transition voltage) exists. Therefore a positive DNL resembles as one or more decision level in the code's input range [17]. Large values of DNL can limit the ADC performance in terms of signal-to-noise ratio (SNR). The DNL for an N-bit ADC is calculated as:

$$DNL[i] = \frac{V_{i+1} - V_i}{V_{LSB-Ideal}} - 1, \quad where \ 0 < i < 2N - 2 \tag{2.12}$$

i corresponds to the quantization code level and $V_{LSB-Ideal}$ is the ideal distance for two adjacent digital codes [1].

Integral nonlinearity (INL) error is defined as the summation of DNL errors and appears as deviation in LSB or percent of full-scale range (FSR) of the real transfer

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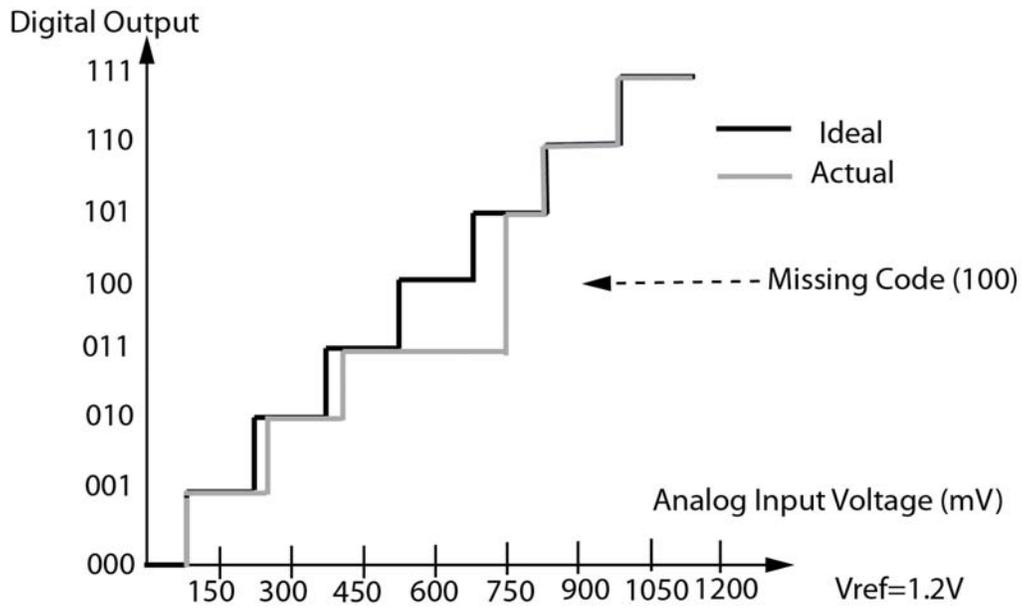
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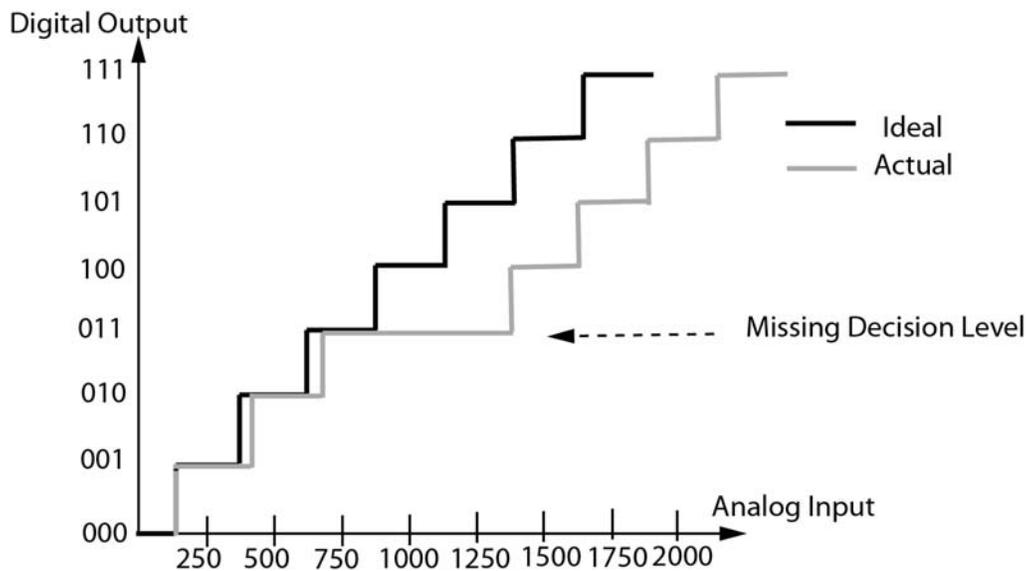
Figure 2.6: DNL error in a 3-bit ADC with missing Decision Levels

function from a straight line in two forms: "best straight-line INL" and "end-point INL". The former determines the closest linearity approximation to the ADC's actual transfer function and the latter is defined by the position of the all zeros and all ones (full-scale) outputs. Fig 2.5, 2.6 and 2.7 show the DNL and INL error examples for of 3-bit ADC respectively.

Best straight-line INL provides information about offset (intercept) and gain (slope) error, plus the position of the transfer function. It determines, in the form
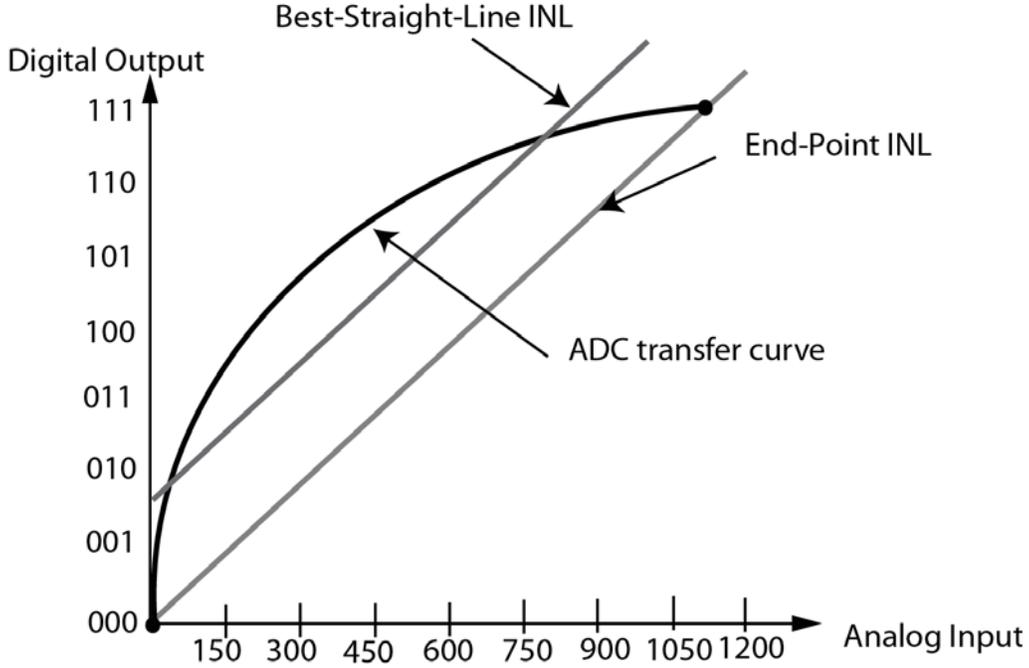
Figure 2.7: INL error in a 3-bit ADC

of a straight line, the closest approximation to the ADC's actual transfer function. End-point INL passes the straight line through end points of the converter's transfer function, thereby defining a precise position for the line. Thus, the straight line for an N-bit ADC is defined by its zero (all zeros) and its full-scale (all ones) outputs. The best straight-line approach produces lower peak error results and is often preferred [1]. INL for an N-bit ADC is calculated as:

$$INL[k] = \sum_{i=0}^{k} DNL[i] = \frac{V_i - V_{zero}}{V_{LSB-Ideal}} - i, \quad where \ 0 < i < 2N - 1 \qquad (2.13)$$

V_i is the analog value corresponding to the digital output code i, N is the ADC resolution, V_{zero} is the minimum analog input representing the all-zero output code, and $V_{LSB-Ideal}$ is the ideal distance between two adjacent output codes.

2.2.4 Timing Error

Timing errors also limit ADC performance. Sampling clock jitter, clock skew, and input skew are known as typical timing erros whether from random sources or deterministic sources like clock distribution layout [5].

Sampling clock jitter also known as "aperture jitter" giving rise to sampling-time uncertainty and this error is more significant at the maximum slope of the input signal; meaning that a small Δt change in sampling time while the $\frac{\Delta V}{\Delta t}$ is large causes a large ΔV error. Assuming a sinusoidal input waveform (a full-scale signal V_{in}) with input frequency f_{in} is applied to an N-bit ADC, the maximum slope is at the zero crossing [2,5]:

$$V_{in} = \frac{V_{ref}}{2} sin(2\pi f_{in} t) \tag{2.14}$$

$$\frac{\Delta V}{\Delta t} \mid_{max} = \pi f_{in} V_{ref} \tag{2.15}$$

If Δt represents the sampling time uncertainty, then in order to keep ΔV error less than $1LSB$ the Δt has a upper bound limitation [2,5], therefore:

$$\Delta t < \frac{1\, LSB}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}} \tag{2.16}$$

For example, a 7-bit ADC sampling a 200MHz full-scale sinusoidal signal must keeps its aperture jitter under 12 ps to maintain 7-bit accuracy. In order to calculate the signal-to-noise (SNR) ratio affected by jitter-induced noise, we need to calculate the power of ΔV error at any point in time. For a sinusoidal input signal $v(t) = A sin(2\pi f_{in} t)$ the ΔV error is:

$$\Delta V(t) = A(2\pi f_{in})\Delta t\; cos(2\pi f_{in} t) \tag{2.17}$$

The power of the ΔV error is calculated as:

$$\langle \Delta V(t)^2 \rangle = \langle [A(2\pi f_{in})\; cos(2\pi f_{in} t)]^2 \rangle \langle \Delta t^2 \rangle = \frac{A^2}{2}(2\pi f_{in})^2 \langle \Delta t^2 \rangle \tag{2.18}$$

The SNR from jitter-induced noise is expressed as:

$$SNR = \frac{\frac{A^2}{2}}{\frac{A^2}{2}(2\pi f_{in})^2 \langle \Delta t^2 \rangle} = \frac{1}{(2\pi f_{in})^2 \langle \Delta t^2 \rangle} \tag{2.19}$$

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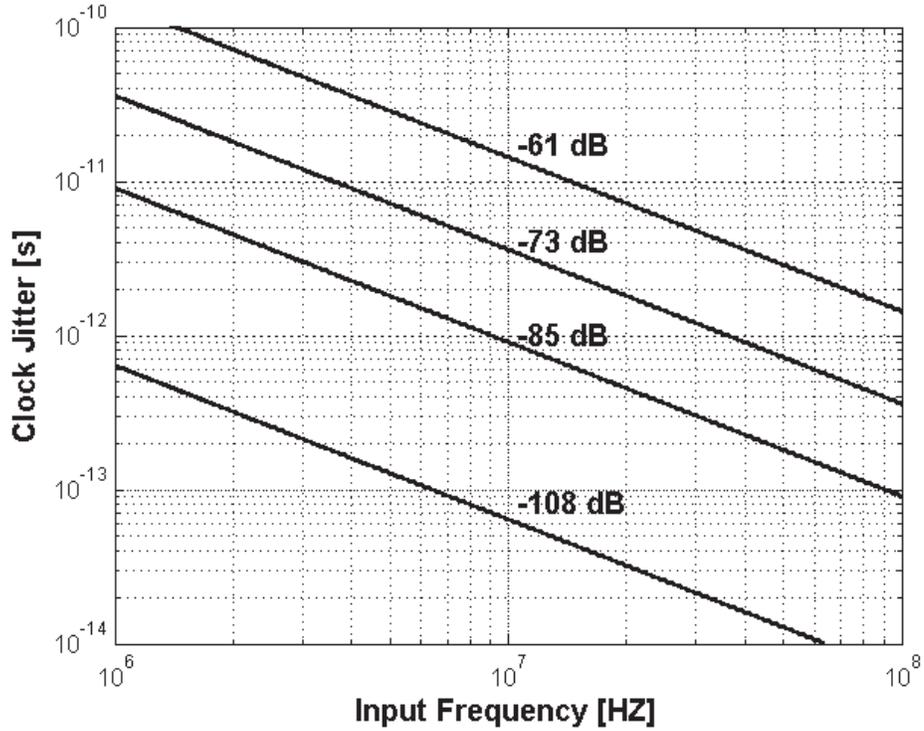
Figure 2.8: Sampling Jitter at different SNR and input frequency [2]

$$SNR_{dB} = -20log_{10}(2\pi f_{in}\langle\Delta t\rangle)or\langle\Delta t\rangle = \frac{10^{\frac{-SNR_{dB}}{20}}}{2\pi f_{in}} \tag{2.20}$$

This means that for a 200MHz sinusoidal input applied to an ADC, in order to achieve 40dB SNR the aperture jitter must be less than 8 pS. Therefore a low jitter clock is essential to proper ADC performance. Jitter versus the input frequency for a specific SNR is shown in Fig 2.8. As is shown in the figure, at high frequencies in order to achieve large SNR very low jitter clock in the order of *ps* is needed.

Clock signal path needs careful layout in order to avoid clock skew. Different wiring passes near clock signal wires can affect the capacitance of the clock distribution wires and causes unwanted delays. Random mismatch of transistor devices in buffers on clock signal path can also create clock skew. Input skew happens when input signal arrives with delay to the blocks. For example, in a case of flash ADC design, the input signal to the comparators sees some delay between comparators. Therefore some errors will br associated with the sampled voltage. A front-end sample and hold circuits (at the cost of power consumption and limited input bandwidth) can solve this problem.

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2.3 Figures of Merit and Performance Trends

When ADCs with different specifications are compared, figure-of-merit (FOM) can combine the various parameters that are important for design [10]. Several FOM has been defined so far [3]:

- Walden FOM

$$FOM_W = \frac{P}{f_s \times 2^{ENOB}} \tag{2.21}$$

- Schreier FOM (DR)

$$FOM_{S-DR} = DR + 10log(\frac{BW}{P}) \tag{2.22}$$

- Schreier FOM (SNDR)

$$FOM_S = SNDR + 10log(\frac{\frac{f_s}{2}}{P}) \tag{2.23}$$

In Fig 2.9, the dashed line shows the schreier FOM which is the borderline for high resolution ADCs [3], in 2014. For low resolution ADCs, it is still appropriate to use the walden FOM (doted line in Fig 2.9) [3].

2.4 ADC Architectures

ADCs cover a wide range of resolutions and speed with different architectures. There are two main types of analog-to-digital converters: Nyquist rate and oversampling converters. In Nyquist rate converters like flash and Successive Approximation ADCs, output values have a one-to-one correspondence with input values [5]. However, they are designed to operate at 1.5 to 10 times the input signal Nyquist rate in order to have a reliable anti-aliasing and reconstruction filter [5]. Oversampling data converters such as Delta-Sigma ADC typically operates 20 to 512 times the input signal Nyquist rate. Fig 2.10 shows several ADC architures for different sampling rates and resolutions [4].

Scaling of CMOS IC technology into nanometer area has noticeable improvement in cost, performance, and system integration. Although scaling is very beneficial for digital systems, analog functions are degraded with shrinking the transistor sizes, and analog design is challenging in nanometer technologies. However, the
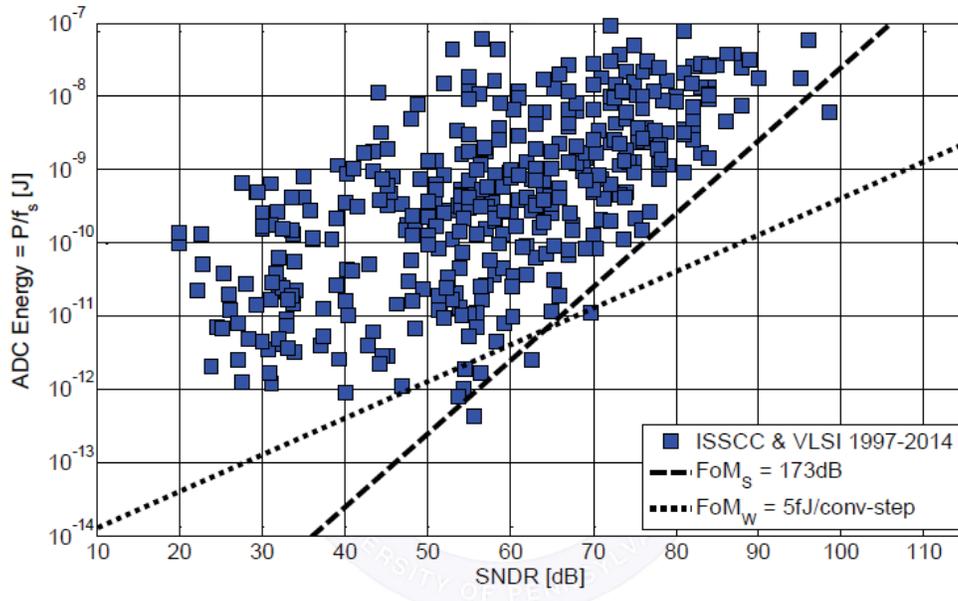
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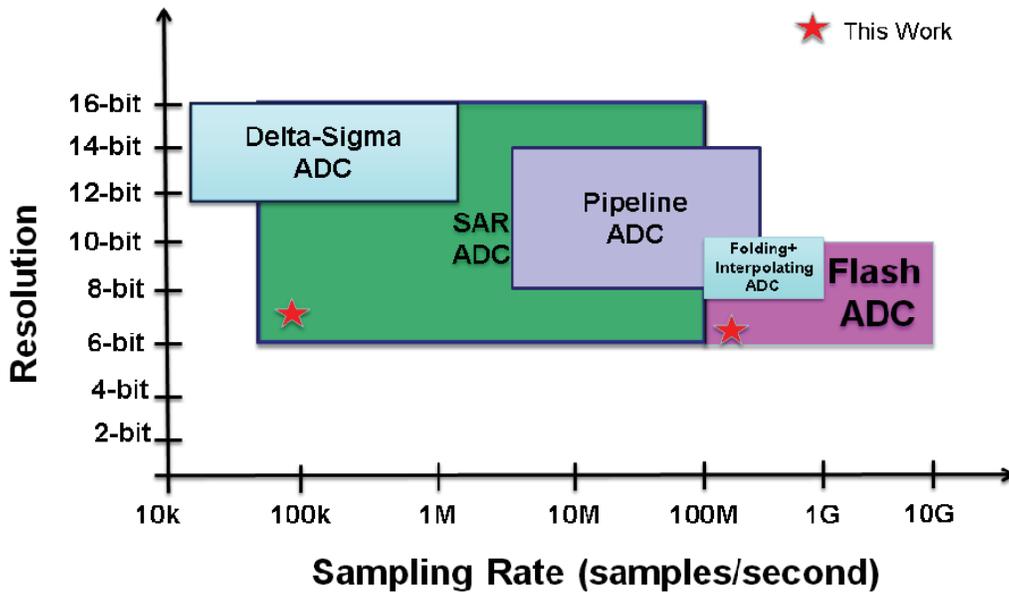
Figure 2.10: Different ADC architectures comparison [4]

cost advantages of integrating systems with technology scaling has made analog and mixed signal design attractive to the designers yet. In comparison to other types of analog-to-digital converters, the simple analog structure of flash ADCs makes them attractive in the speed-power-complexity trade off in deep submicron CMOS. This work presents a redundant flash ADC using a "Split-ADC" calibration structure

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and lookup-table-based correction and an ultra low power SAR-ADC design.

2.4.1 Flash ADC Structure

In nanometer scale CMOS high speed low power analog-to-digital converters with high effective number of bits (ENOBs) are in demand. Wireless receivers and high density disk drives are examples of applications that flash ADCs are typically used in [18]. A flash ADC has a simple structure that includes an array of comparators, a resistor ladder in order to generate the reference voltages, and a thermometer-to-binary converter block. Fig 2.11 shows block digram of a simple flash ADC.

The high conversion rate of flash ADC comes at the cost of high number of comparators. A basic flash ADC employs an individual comparator for every quantization level in order to compare an input voltage with a series of reference voltages. For an N-bit flash ADC, typically $2^N - 1$ comparators are needed. The analog input signal is applied to the negative input of each comparator while the reference voltage coming from a voltage divider resistor ladder is applied to the positive comparator input. The results is a thermometer code output, since all comparators connected to as resistor string will generate a 1 output if the reference voltage is larger than input signal or generate a 0 output if input signal is greater than the related reference voltage. A "$2^N - 1$ to N" digital decoder can convert the thermometer code into a binary weighted output code [5].

Although designing in in a deep submicron process gives us the advantage of higher speed, increasing variation and device mismatch will decrease the ADC effective number of bits (ENOB). Especially in flash ADCs, device mismatch results in offset error in each comparator, affecting differential and integral nonlinearity (DNL and INL) of the ADC and degrading ENOB performance.

2.4.2 Redundant Flash ADC

Redundancy has been shown to be a practical method of yield enhancement in integrated circuit designs [7, 18–20]. In order to reduce the matching problem of transistors, one can increase the device size [14]; however this approach results in increased area and power consumption costs. In flash ADC design, comparator

Architecture	Speed	Accuracy
Flash	High	Low
SAR	Low-Medium	Medium-High
Folding-interpolating	Medium-High	Medium
Delta-Sigma	Low	High
Pipeline	Medium-High	Medium-High

Table 2.1: Comparison of different ADC Architectures

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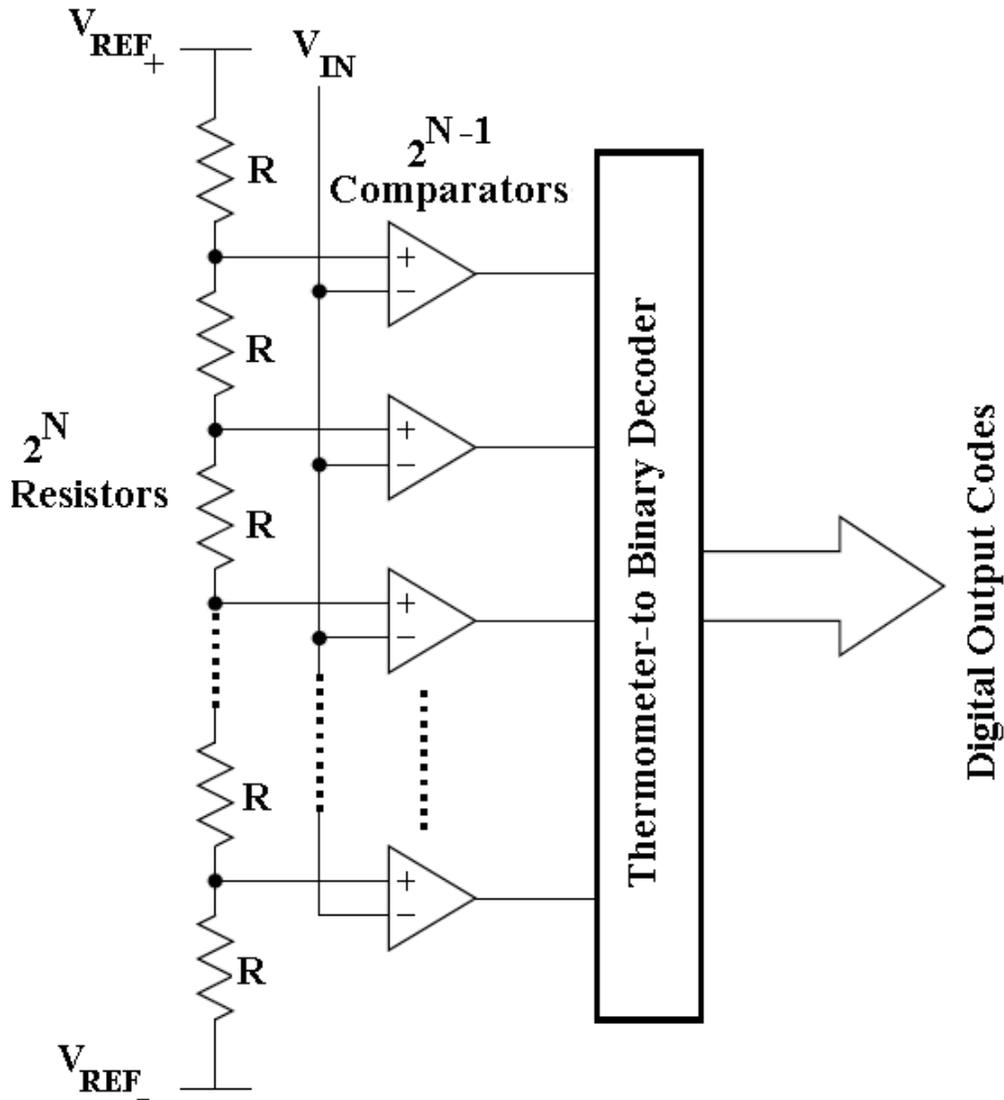
Figure 2.11: Block diagram of a flash ADC

redundancy tolerates the large comparator offsets due to small device sizes essential to reduce input capacitance and provides the high speed flash ADC with acceptable fan-in.

In a traditional N-bit flash ADC, comparators with monotonically increasing, trip-voltages have the responsibility of quantizing the analog input signal applied to the ADC. In a redundant flash ADC, instead of $2^N - 1$ comparators, a bank of $R \times (2^N - 1)$ comparators are used to quantize the input signal; meaning that each code are associated with R comparators [7]. More details on the application of redundant flash ADC are addressed in 2.6.1.
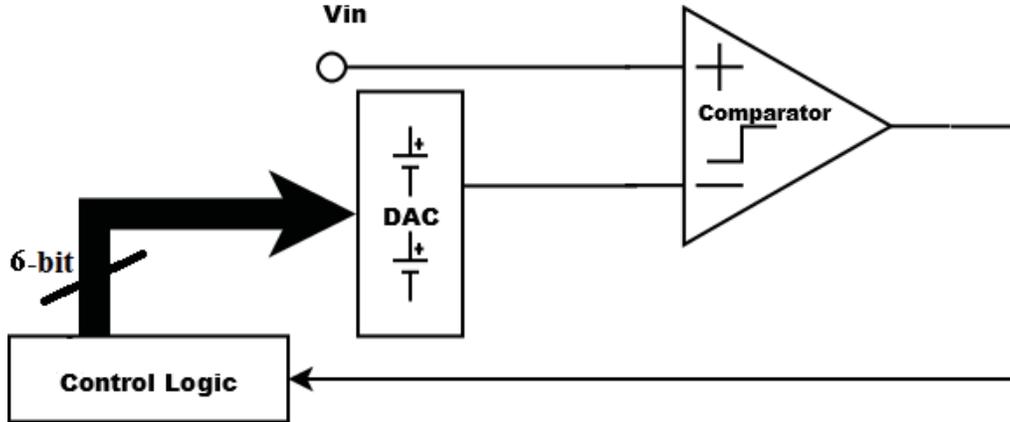
Figure 2.12: SAR ADC architecture

2.4.3 SAR ADC Structure

Successive approximation ADCs are widely used as medium-to-high resolution and medium speed data converters. For high resolution SAR ADCs, fully differential techniques provide the best common mode noise rejection and lowest distortion [21]. For medium resolution ADCs in power-critical applications such as battery management, the lower power consumption of simpler single-ended architectures are attractive.

Unlike the flash ADC in previous section, Successive Approximation Register(SAR) ADC does not use so many comparators for decision making, instead it only has a single comparator that uses a binary search algorithm and a full resolution DAC. Fig 2.12 shows the block diagram of a conventional SAR ADC, consisting of control logic, comparator, and capacitive DAC (CDAC). The sampled analog input voltage is compared with DAC voltage in an iterative process until an analog voltage that is approximately equal to the input voltage is found. A binary weighted capacitor network is used for the DAC architecture in most SAR ADCs since capacitors are better than resistors for device matching [22]. The conversion cycle begins when the Most Significant Bit (MSB) is set to digital value 1 and the rest of the bits are set to zero. The equivalent analog value of this digital code $\frac{V_{ref}}{2}$ at the output of DAC is compared to original input voltage by the comparator. If the comparison shows the analog output from the DAC is greater than the original sampled input, the MSB will reset to digital value 0 as the comparator output is zero. Otherwise, the MSB is left to 1. The binary search will continue for the rest of the bits and the last digital code of control logic will be the the digital representation of the original analog input [23]. Fig 2.13 shows the first three steps of conversion in a single ended SAR ADC. During the sampling mode the top plates of all capacitors are connected to ground and the bottom plates are connected to the input voltage V_{in}. In the second step which is the "hold mode" the top palates are disconnected from the ground while the bottom plates are connected to ground and due to the charge

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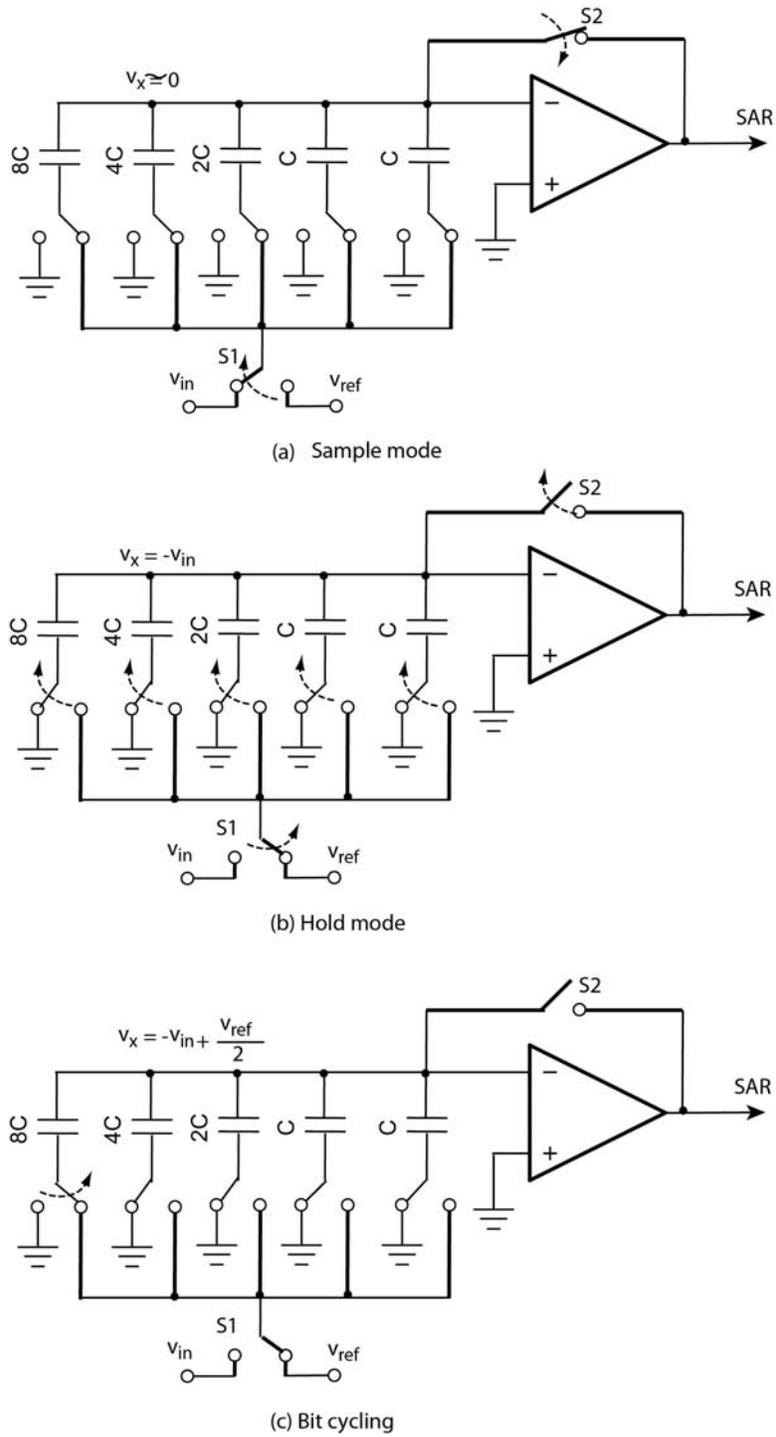
Figure 2.13: A 4-bit charge-redistribution SAR ADC [5]

conservation, the top plates voltage will be $-V_{in}$. In bit cycling step, the bottom plate of the largest capacitor is connected to the reference voltage V_{ref}. This makes

the negative input to the comparator (V_x) increase by $\frac{V_{ref}}{2}$ as:

$$V_x = -V_{in} + \frac{V_{ref}}{2} \qquad (2.24)$$

if the $(V_x) < 0$ which corresponds to $V_{in} > \frac{V_{ref}}{2}$, the comparator output will set the MSB to logic 1; otherwise the MSB will be reset to 0 which means the capacitor corresponding to the MSB will be grounded again. To determine the next bit, the next largest capacitor is connected to V_{ref} and the related (V_x) will increase by $\frac{V_{ref}}{4}$. This procedure is repeated until all of the bits are determined [23].

2.5 Calibration Techniques Overview

2.5.1 Flash ADC Calibration

Most calibration methods of flash ADCs are designed to correct the comparator offsets which can be due to device mismatch inherent in the design [5]. Variations in resistors value due to random mismatch along the reference ladder, temperature variation or the variation in polysilicon thickness in polysilicon resistors can cause error in reference voltages [2]. However,this error is not significant in flash ADC design with less than 10 bit resolution [2]. Any input offset voltage of comparators can lead to a shift in flash ADC's linear transfer function and cause an nonlinearity. Several foreground and background calibration methods have been proposed in literature to deal with comparator's offset in flash ADC design. Some of these methods are:

- Auto-Zeroing: This method helps to reduce the offset of preamplifiers and comparators by sampling the unwanted offset voltage and then subtracting the amount of offset voltage from the input or output of the preamplifier [24].

- Averaging, Interpolation, and Folding: Averaging method connects the outputs of the preamplifier array of comparators with resistors and thus effectively averages the offset of the central preamplifier with its neighbors and will improve the DNL/INL [25].

  Interpolation produces voltages that are in between two other voltages and thus a new reference voltage will be created (interpolation factor of 2). This method can reduce the number of preamplifiers required which is also beneficial in terms of input capacitance of flash ADC, power and area [5].

  Folding method also reduces the number of comparators needed in flash ADC design by generating multiple zero crossing for each comparators [5, 26].

- Redundancy: Redundancy is the technique that deliberately uses an excess of "cheap and imprecise comparators [27], selects the best ones, and deactivates the others. More detail is explained in 2.6.1.

- Digitally controlled and DAC based calibration: Digital calibration of the comparators is usually applied in the DAC. Input-referred offset of the comparators is controlled with extra circuitry, which increases the power consumption and area of ADC [28].

- Stochastic ADC: Random distribution of comparator offsets is used to create reference voltages, and the ADC output is the sum of the comparator outputs [29]. The cumulative distribution function (CDF) of the comparator offset will generate the flash ADC transfer function [29]. More detail is explained in 2.6.1.

2.5.2 SAR ADC Calibration

Calibration methods of the SAR converters are mostly aimed to correct the errors of DAC due to capacitive mismatch inside the capacitor network which is one of the primary sources of power dissipation in this type of ADC. Some of these methods are:

- Capacitor Splitting: In this method the MSB capacitor splits into two capacitors of value C_0, and then switches down one of them when it is needed. Thus, the capacitor splitting approach uses the same energy for an up and a down transition [30].

- Redundancy: Redundancy in the search algorithm that is used in typical SAR ADCs can relax the settling constraints to a tolerable error corresponding to the step size. Inaccurate decisions in early conversion steps are tolerated and corrected afterward [31].

- DAC trimming: Some matching techniques (such as dummy capacitor placement) are used to improve matching [32]. Some level of reference trimming also can be used to trim the voltage reference that is applied to capacitor network.

Among these methods of calibrations that have been explained in this chapter, split ADC calibration is known as a promising method of calibration for improving the ADC nonlinearities which is explained in more detail in 2.5.3.

2.5.3 The Split ADC Structure

Fig.2.14 shows the split ADC concept [6,33]. The ADC is split into two channels. The same input is applied to both channels and individual output codes x_A and x_B are produced by each ADC. The ADC output code x is the average of the output of the two channels.

The background calibration signal is derived from the difference Δx between two output codes x_A and x_B. If both ADCs are precisely calibrated, the two outputs

agree and the difference Δx is zero; otherwise if Δx is a nonzero value, calibration parameters in each ADC are adjusted until Δx and the ADC errors approaches to zero.

2.6 Previous Works

2.6.1 Flash ADC Research

Comparator offset has been a significant problem for flash ADC design and so far several methods has been proposed in literature to deal with it. Auto-zeroing, averaging, redundancy, DAC-based calibration, digitally controlled trimming and stochastic ADCs are the known techniques to mitigate the effects of comparator offsets. Among all methods, digital calibration was a promising method which results in less FOM (Figure-of-Merit). Table 2.2 outlines various calibration methods and design of flash ADCs published in the IEEE International Solid-State Circuits Conference (ISSCC), IEEE Journal of Solid-State Circuits (JSSC), IEEE Custom Integrated Circuits Conference (CICC), IEEE Symposium on VLSI Circuits (VLSI) and IEEE Asian Solid-State Circuits Conference (A-SSCC). In this table, calibration techniques, the sampling rate, the power, the effective number-of-bits (ENOB), and the resolution of different flash ADC structure in different process technology are
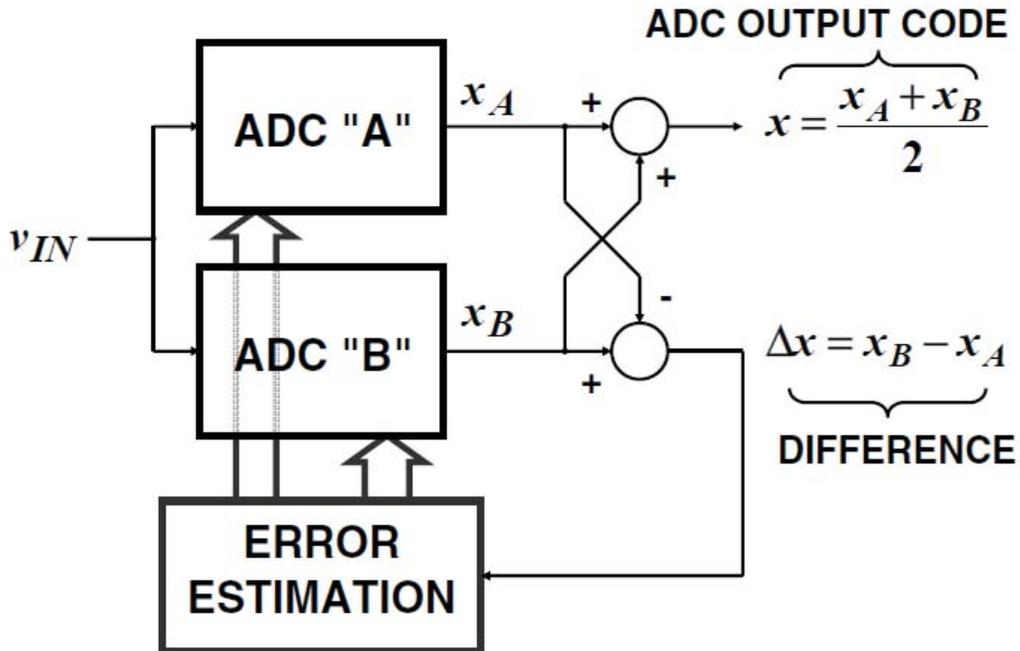
Figure 2.14: Split ADC Architecture [6]

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(a) Nominal Comparator Trip Voltages   (b) Actual Comparator Trip Voltages
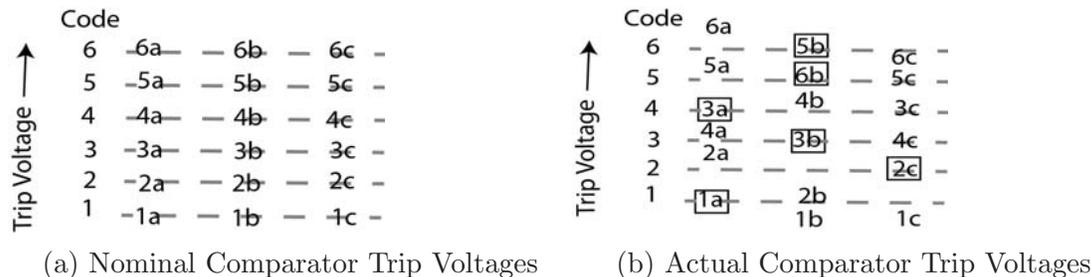
Figure 2.15: The basic principle of redundancy method [7]. Selected comparators are highlighted.

compared.

Among the papers listed in Table 2.2 [19, 34, 35], use a redundancy calibration method. Redundancy is a technique that deliberately uses excess of "cheap and imprecise comparators [27], selects the best ones, and deactivates the others. In case of flash ADC, the identical redundant comparators are spread over the reference voltages and since the offset of comparators span over $1LSB$, there will be a chance of overlapping probability distribution functions (PDFs) of the comparator offsets which is good for comparator reassignment. Instead of $2^N - 1$ comparators, a bank of $R \times (2^N - 1)$ comparators are used to quantize the input signal; meaning that each code are associated with R comparators [7] and a calibration engine [7] will select the best comparator for each code. The basic principle of redundancy method for flash ADC is depicted in Fig 2.15a and 2.15b. In this case, redundancy factor, R is equal to 3. Nominal trip voltages of the group of R comparators for each code is shown in Fig 2.15a. These are the ideal trip points. In reality, the actual trip points are comparators are different from the ones in this figure and they are shown in Fig 2.15b. The trip voltage of the most suitable comparators for each code is highlighted in this figure. For example, comparator 5b is reassigned to designate the code 6. The comparators which are not assigned to any code are disabled to save on power consumption. A problem with this method is the large area cost of disabled comparators. Another difficulty with selection requirement in redundancy method is the "edge effects" [7] which can reduce yield. One can add extra comparators to recover the selection of suitable comparators at lowest and highest codes.

Large capacitive loading is a big challenge in designing a fast sample and hold for a high speed flash [36]. In [36] a two stage track and hold (T/H) is used, while the second stage works as a buffer between the first stage and the capacitive loading of comparators. With clock duty cycle control SNDR improves. However, the extra T/H stage implies extra power consumption and extra area. In [29, 40] a large number of comparators are used in parallel, while removing the reference ladder from the ADC structure and providing the trip points with random offsets. A statistical selection technique is used as a redundancy method to deal variation in comparator offset. This scheme limits the ADC resolution and also consumes a large
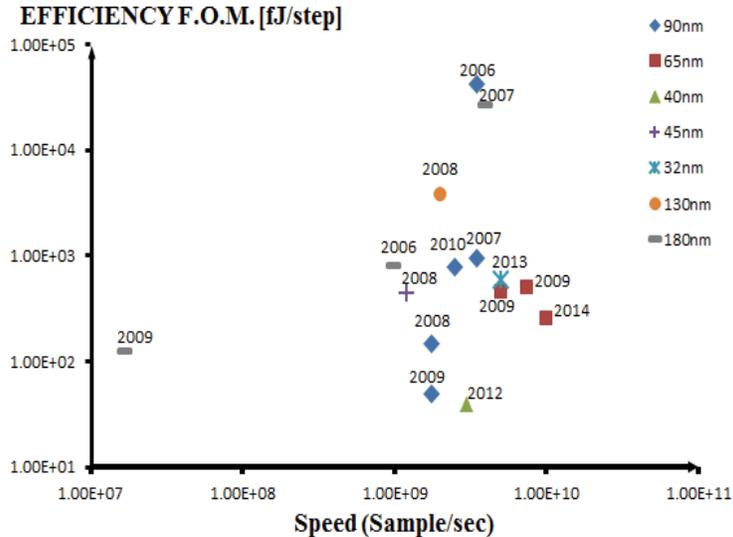
Figure 2.16: Survey of Flash ADCs.

area and any changes in trip points due to temperature drift require recalibration for proper ADC operation [18].

In [25, 39, 42, 46] resistive averaging is used to lower the impact of offset. Speed and linearity is improved with interpolation in [41,43]. In [26] interpolation is used in a folding flash structure and foreground offset calibration is expanded to use digitally controlled DACs for folding-interpolating stages. In [44], analog input is sampled and rectified by a 1-bit folding stage and a 4-bit flash sub-converter converts the folding signal. The nonlinearity of the folding stage is calibrated using additional input pairs in comparators. The combination of a simple folding technique with DAC-based comparator calibration seems to be very practical in reducing the flash ADCs power. In [47]a dynamic technique is used that adds binary-scaled variable capacitors at the drain node of input pair of dynamic comparators. DAC-based calibration has been used in [48–50]. Fig 2.16 plots the reported efficiency FOM as a function of speed in (GS/s). It is evident that recent designs have a wide performance range (20 MS/s to tens of GS/s) and achieve good power-efficiency in high speed conversion.

2.6.2 SAR ADC Research

In recent years, there has been a significant progress in designing energy efficient SAR ADCs. Recent ADC surveys [51] show the conversion speed and power consumption of SAR ADCs have dramatically improved. Process scaling is beneficial for this type of ADC that uses MOS switches, digital logic and capacitance network. Table 2.3 outlines various SAR ADC designs in recent years.

This survey show there has been significant improvement in capacitive DAC

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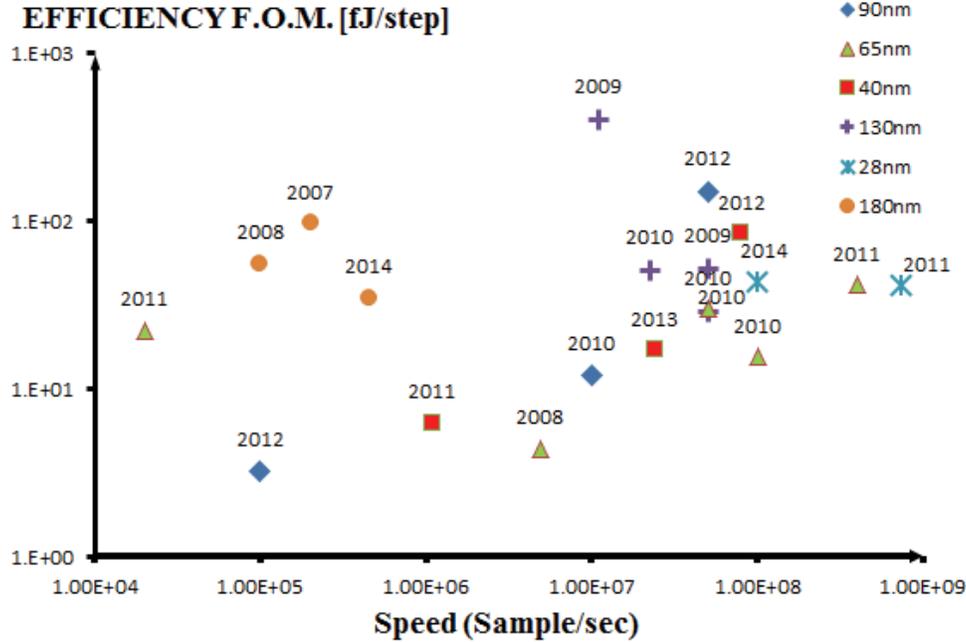
Figure 2.17: Survey of SAR ADCs.

switching energy. Monotonic switching [63], capacitance splitting [30] and arbitrary weight capacitor array [67] has been the promising methods of energy saving in SAR ADC design. Eliminating the MSB capacitance switching [63], using a separate coarse-ADC to calculate the MSBs, dual supply ADC that uses lower supply voltage for power hungry digital portion of ADC and taking the advantage of unary-wighted DAC [59] are some of the energy efficient design schemes that has been proposed in recent years. Fig 2.17 shows a plot of Walden efficiency FOM vs. conversion speed for SAR ADCs in 28nm, 40nm, 65nm, 90nm, 130nm, 180nm process nodes from 2007 to 2014. As it comes from the graph, recent designs that has conversion speed $< 100MS/s$ benefits from process scaling and reports better efficiency FOM.

2.6.3 Split ADC Research

The "Split ADC" was originally developed by my advisor Professor John A. McNeill with collaborators Coln and Larrivee from Analog Devices [73, 78, 79]; a similar technique was developed independently by Moon and Li at Oregon State [80]. An indication impact of this technique is the broad range of published work using the Split ADC approach developed by other investigators. While the original work [73, 78, 79] was for an algorithmic (cyclic) ADC architecture, work has also been published applying the split ADC concept to architectures such as flash [18], folding [77], interleaved [74, 81], and SAR [60, 75, 76, 82] ADCs. For work with numerical results, Fig 2.18 shows the speed and resolution reported. Over a broad
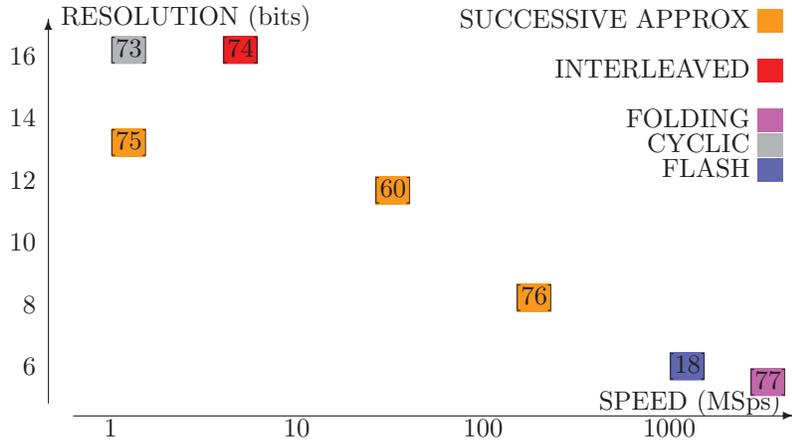
Figure 2.18: Survey of ADCs using "Split ADC" approach.

range of the speed-resolution-architecture ADC trade off space, there are examples in the literature in which the "split ADC" approach enables fast digital background self-calibration. This will enable drastically improved power efficiency by moving all calibration and correction into the digital domain, allowing flash ADCs (first part of this dissertation) to fully realize the promise of nanometer scaled CMOS while avoiding the performance trade offs and disadvantages of the calibration techniques described in 2.6.1.

2.7 Summary

ADC characterization and different ADC architectures were explained in this chapter. An overview of ADC calibration for flash and SAR ADC were presented and split ADC structure was explained. A brief literature review of flash, SAR and split ADC were presented.

Reference	Technology (nm)	Sampling-Rates	Calibration	Resolution (bits)	ENOB	Power (mW)	FOM (pJ/-conv)
[19]	180	2KS/s to 17.5 MS/s	Redundancy	6	5.05	0.00166	0.125
[34]	180	4GS/s	Redundancy and DAC-controlled trimming	4	3.48	608	27
[35]	90	2.5 GS/s	Comparator reassignment	4	4	30.2	0.79
[36]	65	7.5 GS/s	clock duty-cycle control	4.5	3.8	52	0.497
[37]	180	18MS/s	Stochastic ADC	6	4.9	0.631	N/A
[38]	90	3.5GS/s	voltage trimable offset-canceling buffer	5	3.6	227	42
[39]	90	3.5GS/s	Averaging and Interpolation	6	5.19	98	0.95
[40]	90	210MS/s	Stochastic ADC	N/A	5.9	34.8	N/A
[25]	350	1.3GS/s	resistive averaging	6	5.3	500	N/A
[41]	45	1.2GS/s	Interpolation	6	5.7	28.5	0.45
[42]	65	5GS/s	resistive averaging	6	5.1	320	N/A
[43]	180	24GS/s	Interpolation	5	4.4	3300	11
[26]	180	1GS/s	Folding	10	9.1	1260	N/A
[44]	90	1.75GS/s	Folding and DAC calibration	5	4.7	2.2	0.05
[45]	32	5GS/s	Dynamic-offset calibration	6	5.1	8.5	0.594
[28]	40	3GS/s	digital offset trim	6	5.1	11	0.040
[46]	180	1.6GS/s	resistive averaging	6	5.7	328	N/A
[47]	180	1GS/s	Threshold Calibration	4	3.6	10.6	0.8
[48]	90	1.75GS/s	DAC-based Calibration	5	4.7	2.2	0.05
[49]	65	800MS/s	DAC-based Calibration	6	5.63	12	0.40
[50]	130	3.5GS/s	DAC-based Calibration	6	5.11	170	3.79

Table 2.2: Comparison of different flash ADCs in previous works

Reference	Technology	Sampling Rates	Resolution (bits)	ENOB	Power (mW)	FOM (fJ/-conv)
[52]	180nm	200KS/s	8	7.31	0.00615	97
[53]	90nm	10MS/s	8	7.7	0.0263	12
[54]	65nm	4.9MS/s	10	8	0.0019	4.4
[55]	180nm	100KS/s	10	9.4	0.0038	56
[56]	130nm	50MS/s	10	8.48	0.92	52
[57]	90nm	50MS/s	6	5.02	0.24	150
[58]	130nm	11MS/s	12	10.46	3.57	400
[59]	130nm	100KS/s	10	9.2	0.001	17
[60]	130nm	22.5MS/s	12	11.8	2.8	50.8
[61]	65nm	50MS/s	10	9.3	0.82	30
[62]	65nm	100MS/s	10	9.51	1.13	15.5
[63]	130nm	50MS/s	10	9.18	0.826	29
[64]	65nm	400MS/s	8	7.39	4	42
[65]	40nm	1.1MS/s	8	7.5	0.0012	6.3
[66]	40nm	80MS/s	10	9.15	5.45	85
[67]	90nm	100KS/s	10	9.46	0.00017	3.2
[68]	28nm	750MS/s	8	7.2	4.5	41
[69]	40nm	24MS/s	8	7	0.0546	17
[70]	65nm	20KS/s	10	8.84	0.00026	22.4
[71]	180nm	450KS/s	10	9.82	0.013	35
[72]	28nm	100MS/s	15	11.5	4.2	43.2

Table 2.3: Comparison of different SAR-ADCs in previous works

Chapter 3

FLASH ADC Calibration

Fig 3.1 shows a block diagram of the flash ADC designed for this work. Each of the "A" and "B" ADCs is composed of 127 comparators, for a redundancy factor [7, 83] of $R = 2$ compared with the $2^6 - 1$ comparators required for a 6b ADC with no redundancy. To tolerate nonmonotonic comparator outputs caused by large threshold variation, the raw digital output n is simply the number of comparators with a logic "high" output. Each of the n_A, n_B is realized with a Wallace tree decoder. To correct the DNL and INL errors due to threshold variation, the raw code n is used as the index to a LUT which provides the corrected output code x. In the ideal case, each entry x_i in the lookup table corresponds to the best fit code for the range of analog input voltages corresponding to each raw code n_i. Note that the digital precision of the x_i can be greater than the number of bits in n_i to avoid quantization effects in correction and calibration.

3.1   Using Split-ADC for calibration

Fig 3.2 shows the split ADC concept [73, 78, 79] applied to the design of this flash ADC. The ADC from Fig 3.1 is used for each of the "A" and "B" ADCs in Fig 3.2, for an overall redundancy factor of $R = 4$. The overall ADC output code x_{OUT} is the average of the individual output codes x_A and x_B . To enable background calibration as described in 3.2, a small pseudo random voltage shift $\pm \Delta V$ is introduced in the analog buffer at each ADC input. The $\pm \Delta V$ shift is derived from the ADC reference voltage, and for an ideal converter would cause a known shift in output code of $\pm \Delta C$. Since the $\pm \Delta V$ is equal in magnitude but opposite in sign for the two channels, the shift cancels in the averaging process and the output code x_{OUT} is unaffected.

As shown in Fig 3.2, the difference Δx between the x_A and x_B outputs provides information for the background calibration process. If both ADC lookup tables were calibrated correctly, the Δx would be equal to $\pm 2 \Delta C$ LSB corresponding to the (known) shift ΔV which was introduced in each analog input. Any difference
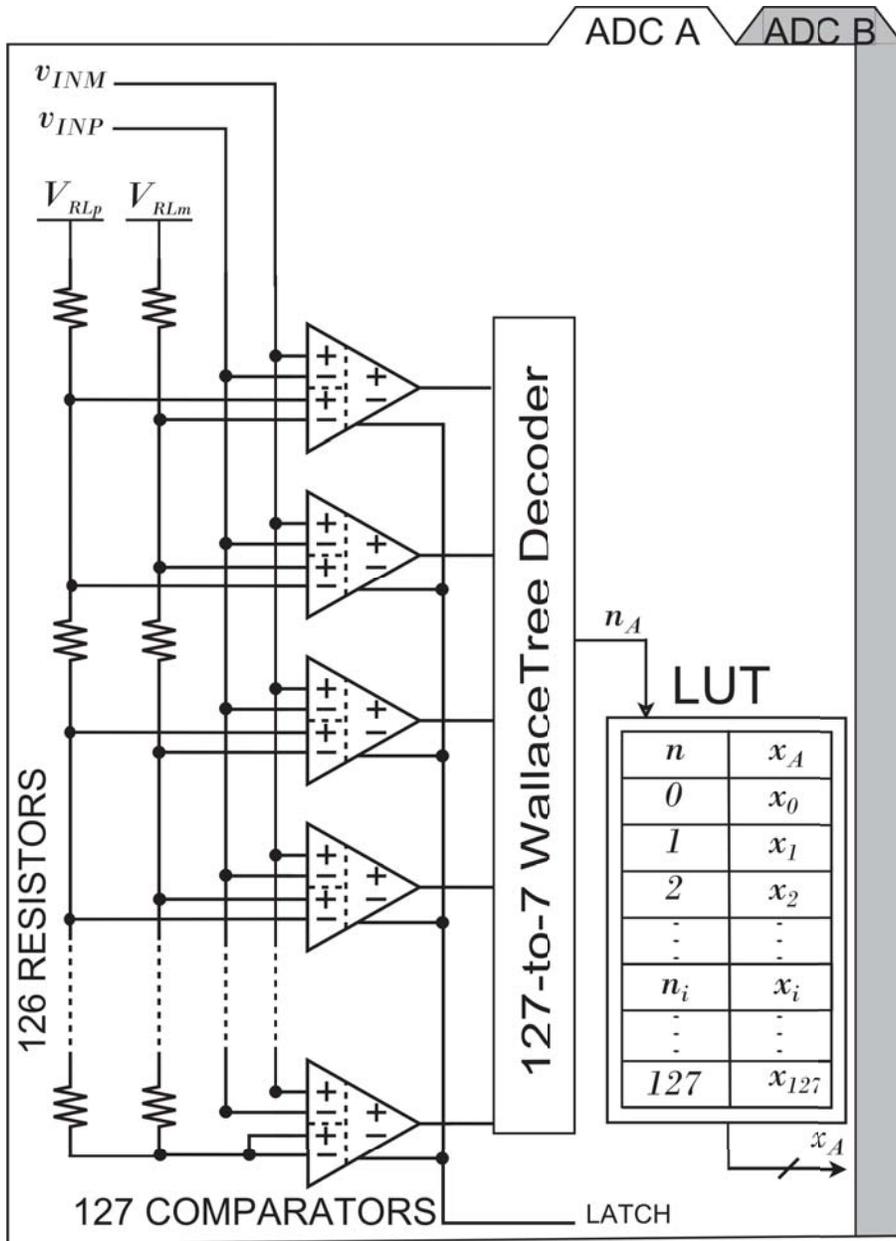
Figure 3.1: Block diagram of split redundant flash ADC

in Δx from the expected $\pm 2\Delta C$ LSB value provides information needed to update the x_A and x_B values in the LUTs corresponding to each of the n_A and n_B raw codes. As the input exercises the ADC inputs over their signal range, information is accumulated to calibrate the LUTs for all entries used. The advantage of using the split ADC is in the differencing operation, which removes the unknown input from the background calibration signal path [73, 78, 79]. The following section describes the correction and calibration process in more detail. The system level calibration
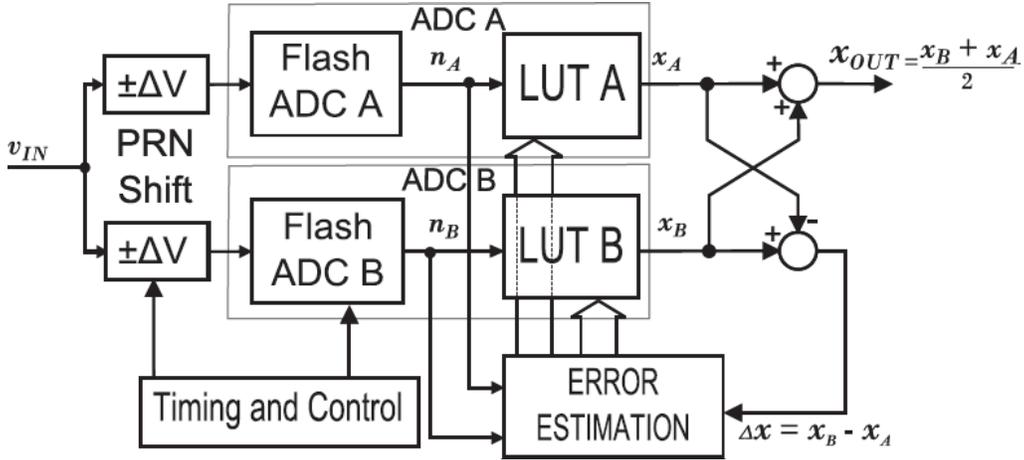
Figure 3.2: System block diagram

method that used in this work has been simulated in MATLAB by Anthony Crasso, M.S. student in the NECAMSID lab. Further details can be found in [84].

3.2   Digital Error Correction

To model the errors that need to be corrected and calibrated in this system, consider an example in which an input voltage is applied with a $-\Delta V$ shift in the A path and a $+\Delta V$ shift in B. Raw codes n_{iA} and n_{jB} from the A and B ADCs are mapped through the respective LUTs to produce corrected codes x_{iA} and x_{jB}:

$$n_{iA} \xrightarrow{\text{LUT "A"}} x_{iA} = x - \Delta C + \epsilon_{iA}$$

$$n_{jB} \xrightarrow{\text{LUT "B"}} x_{jB} = x + \Delta C + \epsilon_{jB} \tag{3.1}$$

In (3.1), we model each of the x_{iA} and x_{jB} outputs as being composed of the ideal output x corresponding to the original unshifted analog input, the $\pm\Delta C$ code shift, and errors ε_{iA} and ε_{jB} in the ith and jth locations of the A and B LUTs respectively. For the ADC output x_{OUT}, averaging the individual outputs in (3.1) gives

$$x_{OUT} = \frac{x_{iA} + x_{jB}}{2} = x + \frac{1}{2}(\varepsilon_{iA} + \varepsilon_{jB}) \tag{3.2}$$

so, as indicated earlier, the shift cancels and we are left with the ideal correct output x and an error component due to the errors in the LUTs. The calibration process to be described in the following section is an iterative procedure that drives the LUT errors ε_{iA} and ε_{jB} to zero, thereby ensuring accuracy of the digital output code x_{OUT}.

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3.3 Calibration

There are several possible methods for obtaining the LUT used for correction. One possibility is to use a foreground approach of applying a known signal, using a ramp or DAC, and determining a best fit LUT for the outputs observed. As quality of the calibration signal is increased, the accuracy of the LUT can be made as precise as necessary. Disadvantages of this approach include the need to generate the calibration signal, as well as taking the ADC offline whenever calibration is required.

A novel aspect of this work is the background approach in which the errors are estimated iteratively. The background calibration accommodates any variations in comparator thresholds that may occur over time or temperature. The algorithm estimates the LUT errors based on the information provided by the difference of the outputs. Taking the difference of the outputs in (3.1) gives

$$\Delta x = x_{jB} + x_{iA} = \varepsilon_{jB} - \varepsilon_{iA} + 2\Delta C \qquad (3.3)$$

From (3.3) we see that the (unknown) input signal is canceled from the calibration path, leaving only the known shift and the errors ε_{iA} and ε_{jB} we need to determine. To the extent that Δx differs from the target value of $\pm 2\Delta C$, we know there is a nonzero error in either or both of ε_{iA} and ε_{jB}. The purpose of the pseudo random analog shift is to provide additional information over multiple conversions that allows unambiguous determination of errors in the LUT. Without the shift, in the case of a DC input, there would be no way to assign the error from the observed Δx to ε_{iA} or ε_{jB}. We can keep track of all errors in the A and B LUTs with 127-element vectors ε_{iA} and ε_{jB}B; with this notation we can write (3) as

$$\Delta x = \overbrace{[\underbrace{0 \ldots 0 -1 \ldots 0}_{\text{``A'' LUT}} \colon \underbrace{0 \ldots 0 +1 \ldots 0}_{\text{``B'' LUT}}]}^{ASSIGNMENT\ \hat{W}} \overbrace{\begin{bmatrix} \varepsilon_{0A} \\ \vdots \\ \varepsilon_{iA} \\ - \\ \varepsilon_{0B} \\ \vdots \\ \varepsilon_{jB} \end{bmatrix}}^{\hat{e}} + 2\Delta C \qquad (3.4)$$

The assignment vector has a -1 entry corresponding to the ith location in the A LUT, and a +1 entry for the jth location in the B LUT. Over many conversions, we can accumulate a matrix of information relating the Δx values to codes in the

LUTs:

$$
\overbrace{\begin{bmatrix} \vdots \\ \Delta x \\ \vdots \end{bmatrix}}^{\hat{d}} = \overbrace{\begin{bmatrix} 0\,...\,-1\,...\,0\vdots 0\,...\,+1\,...\,0 \\ 0\,-10\,...\,0\vdots 0\,...\,0\,+1\,\,0 \\ \vdots \quad\quad\quad \vdots \\ 0\,...\,-1\,...\,0\vdots 0\,...\,+1\,...\,0 \end{bmatrix}}^{\hat{W}} \overbrace{\begin{bmatrix} \varepsilon_{0A} \\ \vdots \\ \varepsilon_{iA} \\ - \\ \varepsilon_{0B} \\ \vdots \\ \varepsilon_{jB} \end{bmatrix}}^{\hat{e}} + \overbrace{\begin{bmatrix} \vdots \\ 2\Delta C \\ \vdots \end{bmatrix}}^{\hat{s}} \qquad (3.5)
$$

Rather than solve the matrix equation in (3.5) exactly, the iterative technique in [73] is used.

3.4 LMS Procedure

The mathematical development proceeds as in [73]. Formally, beginning with $d = We + s$ in (3.5), we subtract s from each side and premultiply by the transpose of W to obtain

$$\hat{W}^T(\hat{d} - \hat{s}) = \hat{W}^T\hat{W}\hat{e} \qquad (3.6)$$

Since W is a very sparse matrix filled with only ± 1 for nonzero values, the product of $\hat{W}^T\hat{W}$ results in a diagonally dominant square matrix. If the matrix were purely diagonal, then its inverse would be easy to compute exactly as the inverse of the diagonal elements. Since, as in [73], we only need an approximate solution for the iterative least mean squares (LMS) procedure, we multiply by a factor μ to obtain estimates of the LUT errors:

$$\hat{e} = \mu\hat{W}^T(\hat{d} - \hat{s}) \qquad (3.7)$$

The LMS factor μ is chosen to be a power of 2 so the itration in [73] can be easily computed as a shift in the digital hardware. The choice of μ also affects the dynamics of the iteration convergence; for stable convergence μ should be chosen smaller than the inverse of the largest diagonal element of $\hat{W}^T\hat{W}$. The $\hat{W}^T(\hat{d} - \hat{s})$ data can be accumulated on a conversion-by-conversion basis and requires the same number of memory locations as the vector.

A block diagram of the calibration algorithm is shown in Fig 3.3. The calibration portion on the left side is performed after the system collects a set of data over a large number (of order 1000s) of conversion cycles.

3.5 Behavioral Results

The full split ADC system was simulated behaviorally using MATLAB by Anthony Crasso [84] for 45nm technology. The simulation has been repeated for 180nm

PARAMETER		VALUE
LMS Parameter	μ	2^{-21}
Analog shift value	ΔV	3.5 LSBs
Intial Error Estimate	ε	0
Threshold variation standard deviation	σ	5 LSBs
Total Number of Comparators		254
Effective Number of Bits (ENOB)		6.1
INL(after calibration)		1.52 LSB pk-pk
DNL(after calibration)		$+.85/-.90$ LSB

Table 3.1: System Simulation Parameters
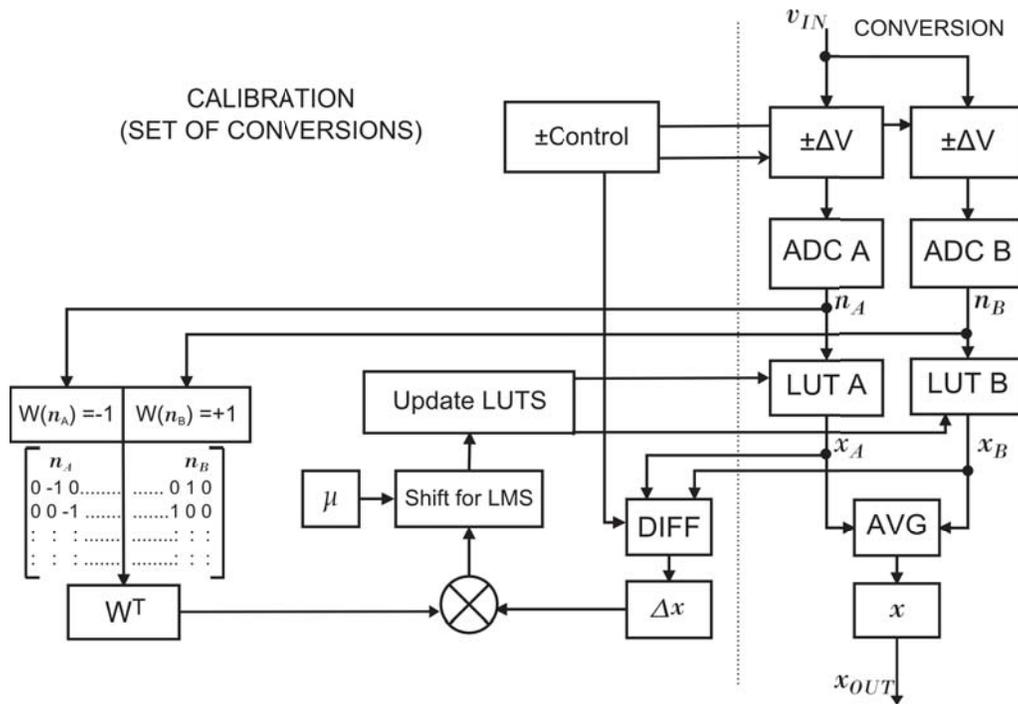
Figure 3.3: Calibration block diagram

technology for this work, with the system parameters shown in Table 3.1.

All results are reported at the 6b level. The comparator threshold variation value σ was estimated from circuit-level simulation and process specifications. Fig 3.4 show ADC differential nonlinearity (DNL) and integral nonlinearity (INL) of the system before and after calibration. DNL improves from $+1.53/-1.00$ to $+.85/-.90$ LSB; INL improves from 2.56 to 1.52 LSB pk-pk.

The adaptation transient of the ADC for different μ values is shown in Fig 3.6. So that the detailed performance of the calibration algorithm can be seen, corrected code outputs are reported in 12b precision rather than truncated to 6 bits.
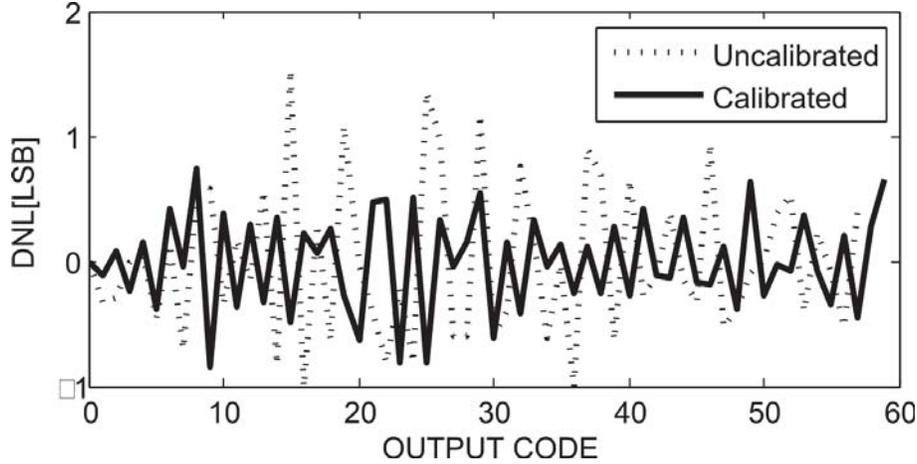
Figure 3.4: Calibrated and Uncalibrated DNL
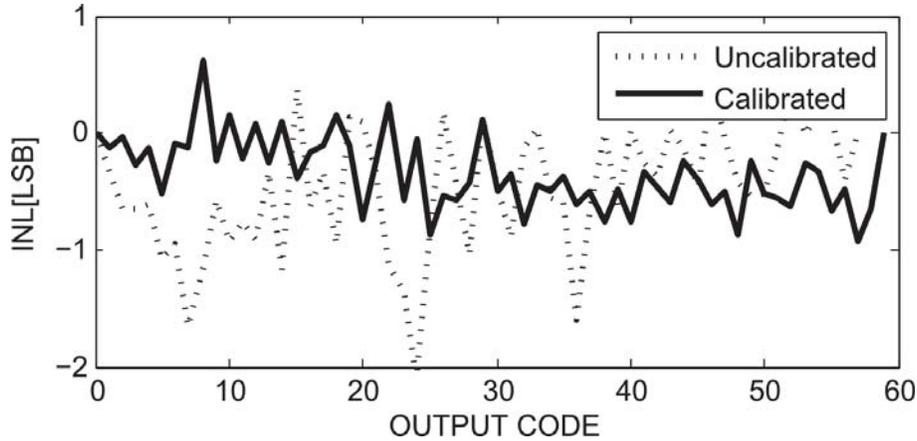
Figure 3.5: Calibrated and Uncalibrated INL

For the $\mu = 2^{-21}$ case, convergence to ENOB > 6 is seen within 2E+9 conversions. At 200MS/s, this corresponds to less than 2 seconds to converge to what would be quantization-limited accuracy. As is typical of LMS systems, faster convergence is seen for smaller μ, subject to stability and accuracy trade offs.

3.6   Summary

This chapter has presented all digital background calibration of a redundant flash ADC suitable for for aggressively scaled CMOS technologies. Implementation using the split-ADC calibration technique minimizes analog complexity and enables purely background calibration. All redundant comparators are used and correction is realized using a lookup table which is continuously updated in the background. Simulation results show the proposed algorithm has the ability to reach performance
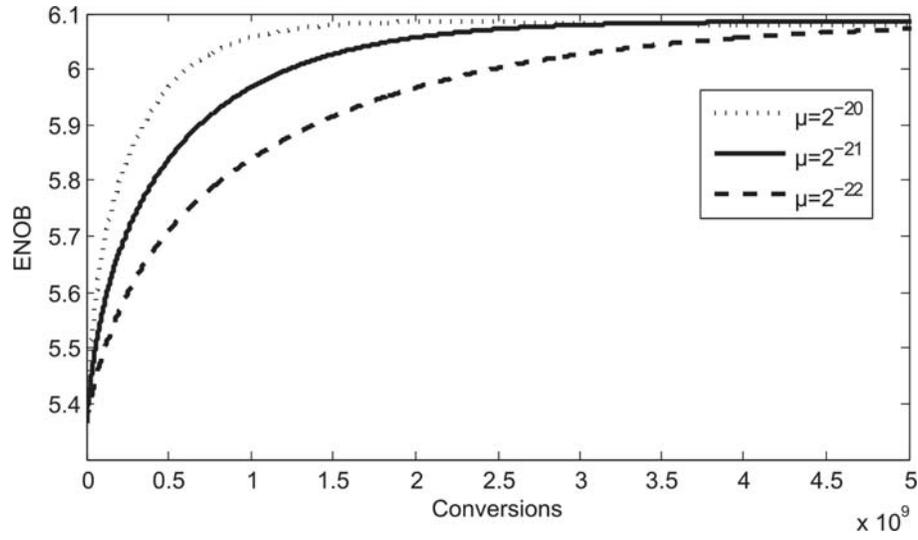
Figure 3.6: Calibration Convergence

comparable to previous work without requiring additional silicon area, a precise signal source, or offline calibration.

Chapter 4

FLASH ADC Chip Implementation

The 7-bit Split Redundant Flash ADC was implemented in 180nm IBM cmrf7sf bulk CMOS technology. In this chapter, the design of this 7-bit flash ADC is presented, which is targeted for applications such as wireless receivers and high density disk drives. This redundant flash ADC uses a Split-ADC calibration structure and lookup-table-based correction. ADC input capacitance is minimized through use of small, power efficient comparators which (in simulation) only consumed 17.4 μW power with 1.8V supply voltage at 200MHz clock; redundancy is used to tolerate the resulting large offset voltages. Correction of errors and estimation of calibration parameters are performed in the background in the digital domain as it reduces the test/trim time. This 5.8 ENOB flash ADC was designed for a sampling rate of 200MS/s.

4.1   System Overview

The block diagram of the proposed flash ADC is shown in Fig.4.1 again to illustrate the general building blocks that are used in to design the flash ADC in this work. As it is mentioned before each of the "A" and "B" ADCs is composed of 127 comparators, for a redundancy factor [7,83] of $R = 2$ compared with the $2^6 - 1$ comparators required for a 6b ADC with no redundancy. With the split ADC structure the overall redundancy factor is $R = 4$. To assist background calibration as described in 3.2, a small pseudo random voltage shift $\pm \Delta V$ is presented at each ADC input. The $\pm \Delta V$ shift uses a source follower structure biased by current sources, and for an ideal converter would cause a known shift in output code of $\pm \Delta C$. Each of the digital outputs n_A, n_B is developed with a Wallace tree decoder. This chapter explains the circuit level design of these building blocks.
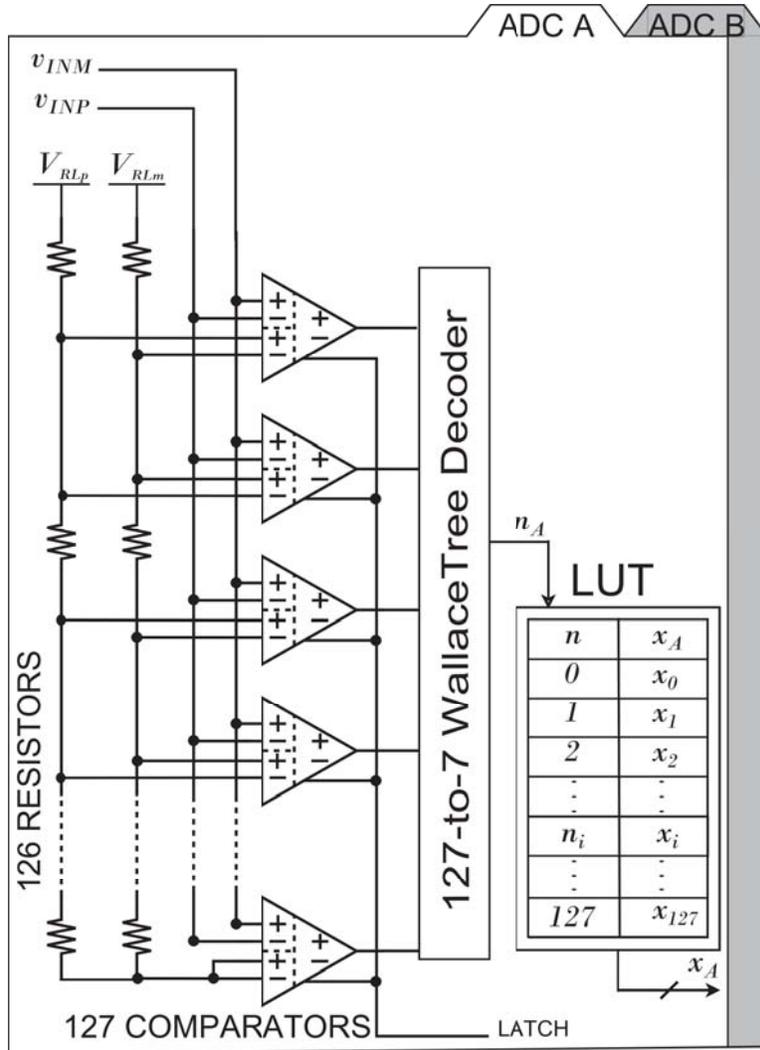
Figure 4.1: Block diagram of split redundant flash ADC

4.2 Analog Blocks

Analog blocks of the proposed flash ADC are 254 dynamic comparators and an analog shift which are designed to be low power. Reference voltages for comparators are provided through a resistive ladder.

4.2.1 Dynamic Comparator Design

Comparators are the core of all ADCs [85]. Therefore the properties of comparators like speed, offset and power consumption directly affect the ADC's performance, accuracy and total power consumption. In this work, to minimize power consumption, a dynamic comparator is chosen, with schematic as shown in Fig 4.2. Offset is not a critical parameter in our design, since the digital background calibration
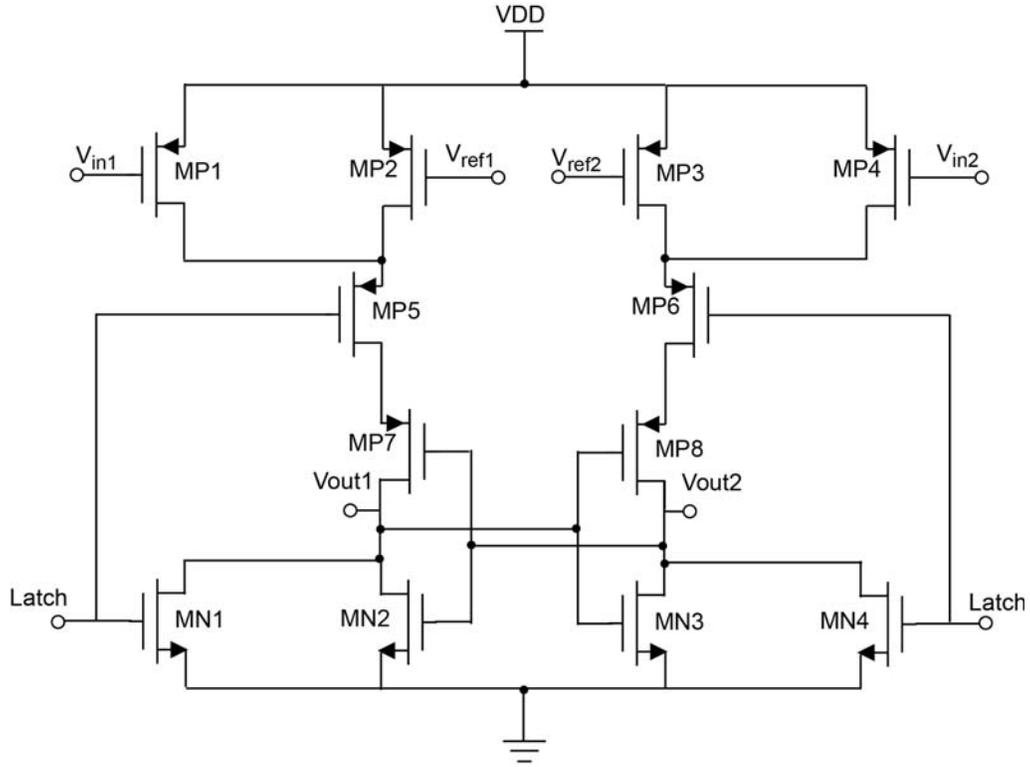
Figure 4.2: Block diagram of dynamic comparator

that is explained in 3 will improve the ADC accuracy; thus there is no need for a preamplification stage in front of the regenerative latch comparator and all the transistors are minimum sized to reduce input capacitance and minimize power consumption. The flow of current only happens during regeneration and reset which helps with minimizing the power consumption. However, the absence of preamplifier increases the sensitivity to dynamic latch noise behavior. In order to limit the error probability of ADC a minimum step size up to 6 times the RMS noise is suggested in literature [86]. In this dynamic comparator, a PMOS input differential pair is used, to cover the the analog input common mode range that is close to ground. The comparator uses the Lewis-Gray architecture [87]: when 'Latch' is high the comparator is reset; when 'Latch' is low regeneration around the MN1-MN4 loop is enabled. The conductivity imbalance from the MP1-MP4 input pair [63] forces the comparator output to go low or high. Cadence virtuoso simulation waveform of this dynamic comparator is shown in Fig 4.3.

Comparator Offset

The input offset voltage of the comparators accumulates into the ADC input voltage and thus directly influences the flash ADC linearity. If the comparator offset, V_{offset}, is the only source of ADC nonlinearity, it will be measured as INL while

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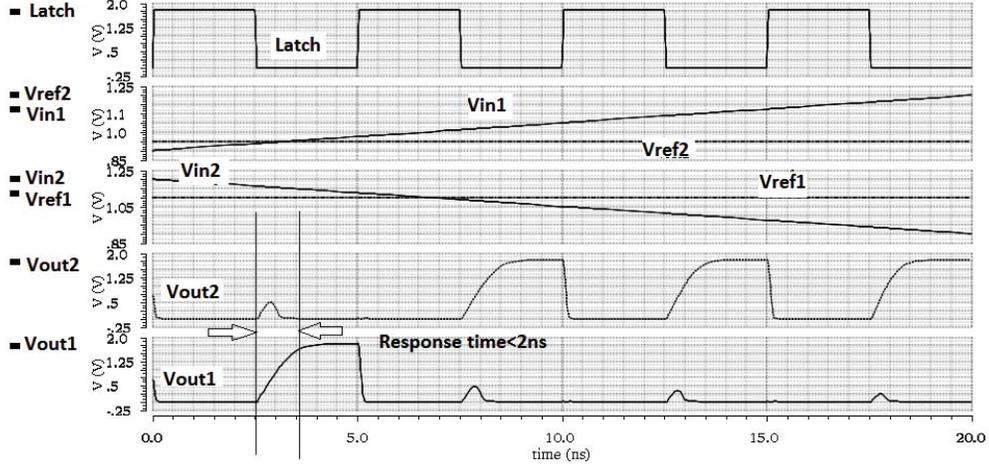
Figure 4.3: Dynamic comparator simulation results

DNL can be defined as the difference between the adjacent offset errors. Fig 4.4 illustrates the indication of comparator offset in flash ADC design [8]. The dynamic comparator that is used in this work consists of a differential pair at the input. The mismatch between the differential pair transistors biased in saturation is assumed to be normally distributed and defined as [8, 14]:

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{WL}} \tag{4.1}$$

$$\frac{\Delta\beta}{\beta} = \frac{A_\beta}{\sqrt{WL}} \tag{4.2}$$

where V_T is the threshold voltage, β is the current factor, W and L are the width and length of the transistor respectively. Distance on chip between devices in a differential pair has been ignored in Eq 4.1and Eq 4.2 [8]. The input offset for differential pair can be calculated as [8]:

$$\sigma(V_{gs}) = \sqrt{\frac{A_{VT}^2 . A_\beta^2 . \Delta V_{gs}^2}{4.WL}} \tag{4.3}$$

where ΔV_{gs} is the overdrive voltage of the differential pair transistors. We can extend the use of Eq 4.3 to estimate the input offset of the comparator. Based on Eq 4.3 the input offset of the comparator is inversely proportional to transistor area. Therefore in order to increase the resolution only one bit, the transistor area WL has to increase 4 times if sizing is the only parameter to control the offset in the design. It has been shown in literature in order to have high yield in flash ADC design, the standard deviation of comparator offset should satisfy the Eq 4.4 [8]:

$$\sigma_{offset} \leq \lambda \times LSB \tag{4.4}$$

40

Figure 4.4: Indication of comparator offset in flash ADC design [8]

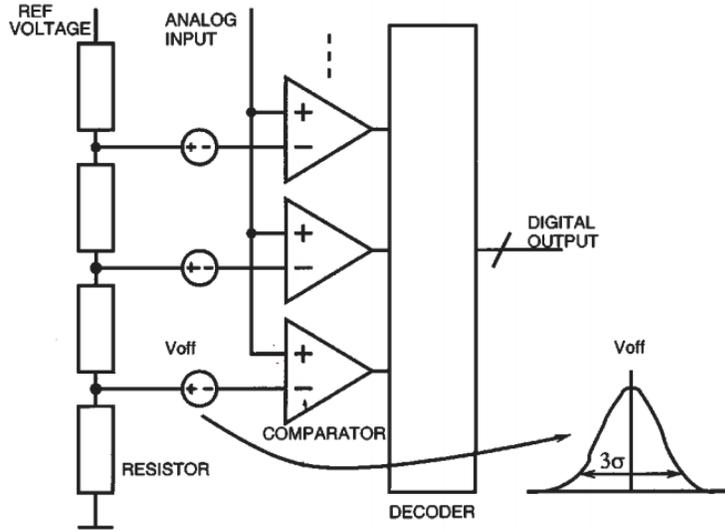where λ is a constant depending on the resolution and the desired yield percentage and LSB is the least significant bit of the ADC [8]. Fig 4.5 shows the MonteCarlo simulation of yield of ADC as a function of σ_{offset} of comparator. As given by this figure, in order to have a flash ADC with 99% yield σ_{offset} should be less than $0.2LSB$ [8] that requires a large area. As it is mentioned earlier, with digital background calibration in this work and using redundant comparators any amount of comparator offset is tolerable.

Dynamic Comparator Metastablity

Metastability is a problem that arises in latching comparators when the input voltage is very close to the comparator threshold voltage, making the comparator transition to a valid output state take more time than is available in the sampling interval [88]. In an ideal condition the comparator outputs generate a thermometer code. If the reference voltage is above the comparator input the digital output would be 0, otherwise the digital output would be 1. Metastability can produce glitches in digital output word and influences the ADC performance due to timing error and possibly makes "bubble" error in thermometer code. [2, 9]. Fig 4.6 illustrates effect of comparator metastability in flash ADCs. Metastability error is a function of comparator regenerative time constant and clock frequency, which means this type of error can increase in orders of magnitude with increasing of clock frequency and scaling down the supply voltages [9]. It has been shown in literature that metastability error rates of below 10^{-10} errors/cycle is required in flash ADC design for telecommunication applications [9]. For a differential latch comparator, the

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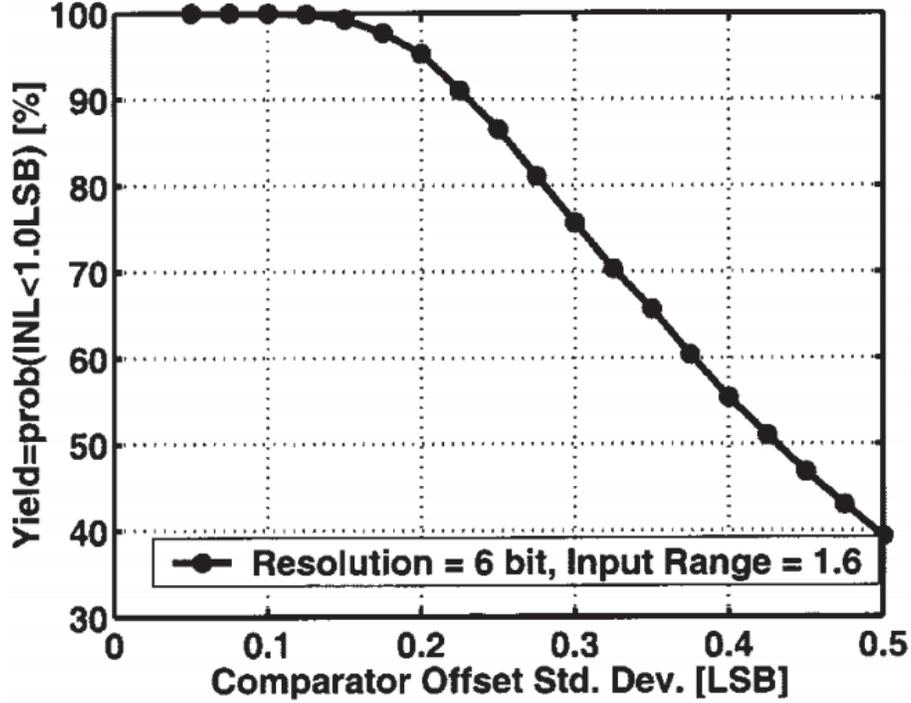
Figure 4.5: MonteCarlo simulation of yield of ADC vs. σ_{offset} of comparator [8]

regenerative time constatnt τ is:

$$\tau = \frac{C}{g_m} \tag{4.5}$$

where C is the total capacitance at a regenerative node, and g_m is the transconductance of a regenerative device in the latch biased when it is switching [9]. The two cross-coupled transconductors with load capacitances in a regenerative latch is shown in Fig 4.7. The probability of having metastability error for an n-bit flash ADC can be calculated as [2, 9]:

$$P_M = \frac{2(2^n - 1)V_o}{V_{in}.A_o} e^{\frac{t_L}{\tau}} \tag{4.6}$$

where V_o is the output voltage swing needed in thermometer code circuitry for having a valid logic level, V_{in} is the analog input rang, τ is the regenerative time constant, A_o is the gain of latch during the transparent state and t_L is the resolution time of the latch comparator [9]. Comparator resolution time is approximated to $\frac{1}{f_s}$, where f_s is the sampling frequency. From Eq 4.6we can conclude that metastability error increases exponentially with increasing sampling frequency. For input voltages V_{in} greater than 0.5LSB, comparator should provide the ADC with a certain digital

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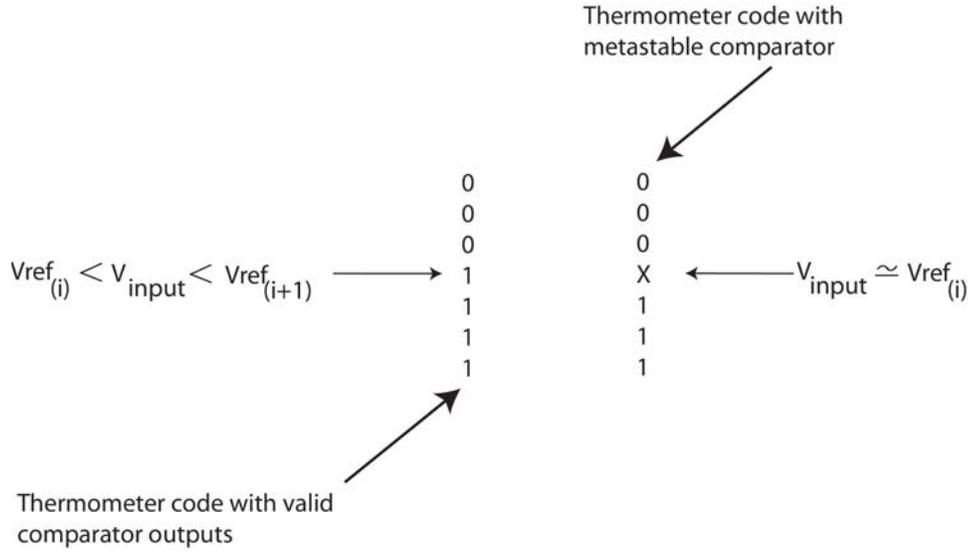
Figure 4.6: Flash ADC with unstable thermometer code as digital output [9]
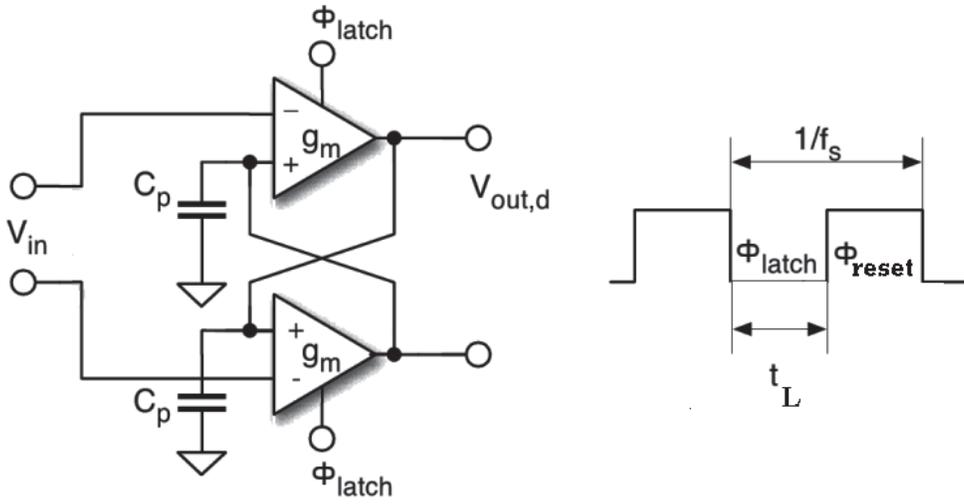
Figure 4.7: Regenerative latch structure [2]

output. Thus for $V_{in} = \frac{V_{FS}}{2^{n+1}}$ the metastability error P_M should be less than a desired $P_{M,max}$. From Eq 4.6 we have [2]:

$$f_s \times ln\Big[\frac{V_o.2^{n+1}}{P_{M,max}.V_{FS}.A_o}\Big] < \frac{1}{2\tau} \tag{4.7}$$

In order to reduce the possibility of metastability error, in designing a good comparator, regenerative time constant should be minimized by maximizing the g_m and minimizing the total capacitance at the regenerative point. Using the minimum size device will help with minimizing the total capacitance at the cost of increasing

the device mismatch.

Comparator Kickback Noise

Latch-based comparators have the disadvantage of creating kickback noise at the input [5, 89]. The clock signal which is shown as latch signal in Fig. 4.2 can be capacitively coupled into the input pair of class AB latched comparator and thus the common-mode kickback noise is very high. This is due to large voltage transition at regenerative node. During the reset phase the drain nodes of the MP1,MP4 are reset to ground and during the regeneration phase, if the V_out is switched from low to high, this large variation of regenerative node voltage induces the common-mode kickback noise. In order to reduce the kickback noise in dynamic comparator in this work, the neutralization technique in [90] is used. Transistors MP5 and MP6 in Fig. 4.2 isolates the input pair devices from the regenerative nodes and reduce the kickback noise.

4.2.2 Reference Ladder

Reference voltages for the differential dynamic comparator are provided through a resistive ladder since resistive ladders are an easy way of creating threshold levels. In this design resistive ladder is made of 50Ω resistors (total resistor of $6.35\text{k}\Omega$ for each ADC). Due to the problem of ladder feed through, the value of the resistors are chosen to be small although small resistance means higher power consumption of ladder. For better current handling, better linearity and higher unit square sheet resistance [91] silicided OP P+ poly resistors (opppcresx) are used for the ladder implementation. One advantage of having silicide on polysilicon is minimization of parasitic resistances [91].

Input feedthrough in the reference ladder is due to capacitive coupling from the input signal that is applied to the input of differential pair into the reference ladder's threshold levels.The worst case feedthrough is from the input pair to the midpoint of the ladder [92]. The total resistance of the ladder in order to avoid the degradation of the performance of flash ADC due to the feedthrough can be calculated as [92]:

$$\frac{V_{ref} \times (2^N - 1)}{V_{in}} = \frac{\pi}{4} f_{in} R_{total} C_{total} \tag{4.8}$$

where C_{total} is the total capacitance from the input signal to the resistive ladder and f_in is the input frequency [92]. Since the C_{total} is almost a fixed amount of the capacitance in dynamic comparator's design, using the small size of resistor can help with reducing the feedthrough. One can also add decoupling capacitor to reduce the feedthrough. It is important to know that the gate-source capacitance changes with input signal amplitude which causes unwanted harmonic distortion [92]. However, the differential architecture of the design can minimize this non-ideality.

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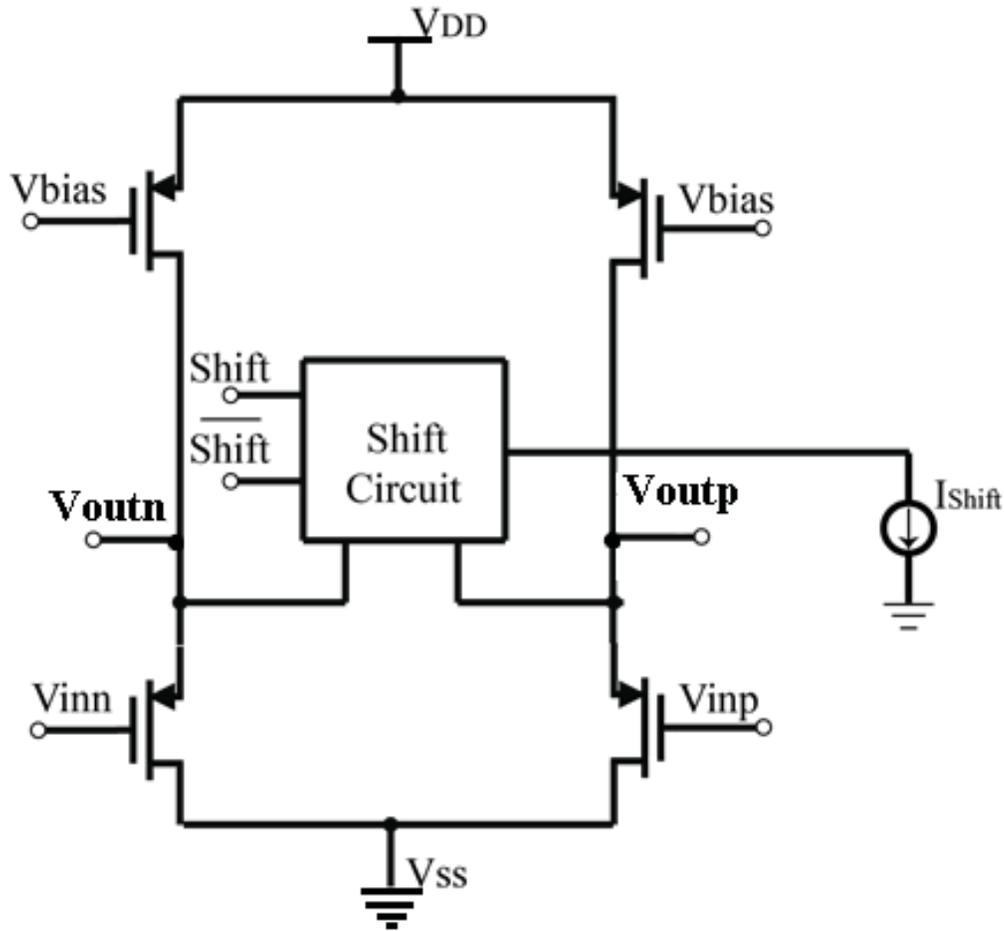
Figure 4.8: Analog Shift Circuit

4.2.3   Analog Shift Design

To assist background calibration as described in 3.2, a small pseudo random voltage shift $\pm\Delta V$ is presented at each ADC input. The $\pm\Delta V$ shift uses a source follower structure biased by current sources, and for an ideal converter would cause a known shift in output code of $\pm\Delta C$. The analog shift is implemented as shown in Fig 4.8. The ΔI_S current which is added to one of the branches of the source follower provides the appropriate voltage shift. The shift need not be instantaneous as long as it is symmetric; samples from the transition region when ΔV has not reached its full value are discarded from the calibration data. The size of the ΔV shift is subject to an optimization trade off: too large a shift consumes excessive signal range, while too small a shift does not provide sufficient information for calibration [18].

Since the input pair of differential latched comparator are PMOS devices, the PMOS type source follower is used for analog shift circuit. Source follower senses the input signal V_{in} at the gate and provides the load (comparator input pair) with

Figure 4.9: Source Follower Circuit

the output at the source. As input voltage increases, the V_{out} follows the V_{in} with a level shift which is equal to the gate-source voltage V_{gs} of the gain stage [93]. For simplicity in explaining the input-output characteristic of a source follower, a single ended structure with small signal model is shown in Fig. 4.9.

By using the small signal model in Fig. 4.9 the gain of this source follower can be calculated as:
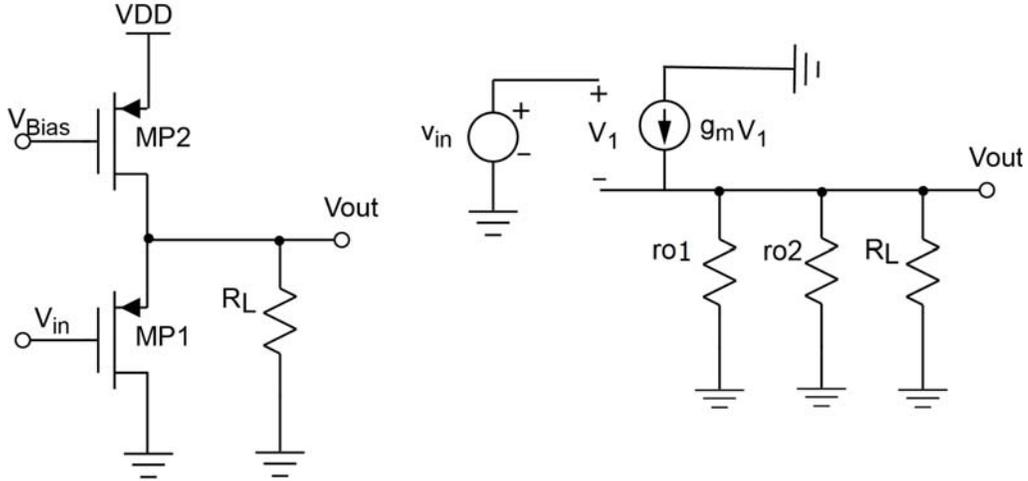
$$A_v = \frac{r_{o1} \parallel r_{o2} \parallel R_L}{r_{o1} \parallel r_{o2} \parallel R_L + \frac{1}{g_m}} \tag{4.9}$$

As shown in Eq 4.9, the gain of source follower is not exactly 1 as it desired. The source follower has a moderate output impedance r_o and suffers from nonlinearity and voltage headroom limitation [93]. The nonlinearity in source follower comes from nonlinear dependence of threshold voltage to source potential voltage [93] which is known as body effect. The advantage of using PMOS source follower is eliminating the body effect (of MP1) as the bulk is tied to source since NMOS devices share the same substrate. The lower mobility of PMOS devices leads to a higher output impedance. In order to improve the output impedance of source follower for better efficiency cascode transistors are used for the bias circuitry. Fig. 4.10 and 4.11 shows the source follower that is used as an analog shift in this design. Simulation result shows the source follower does not limit the bandwidth of the input signal for this flash ADC. Fig 4.12 shows the simulation result for analog shift design. The 3dB frequency is 713.9MHz which is adequate for a 200MS/s flash ADC. Fig 4.13 shows the DC simulation results for 6LSB shift.

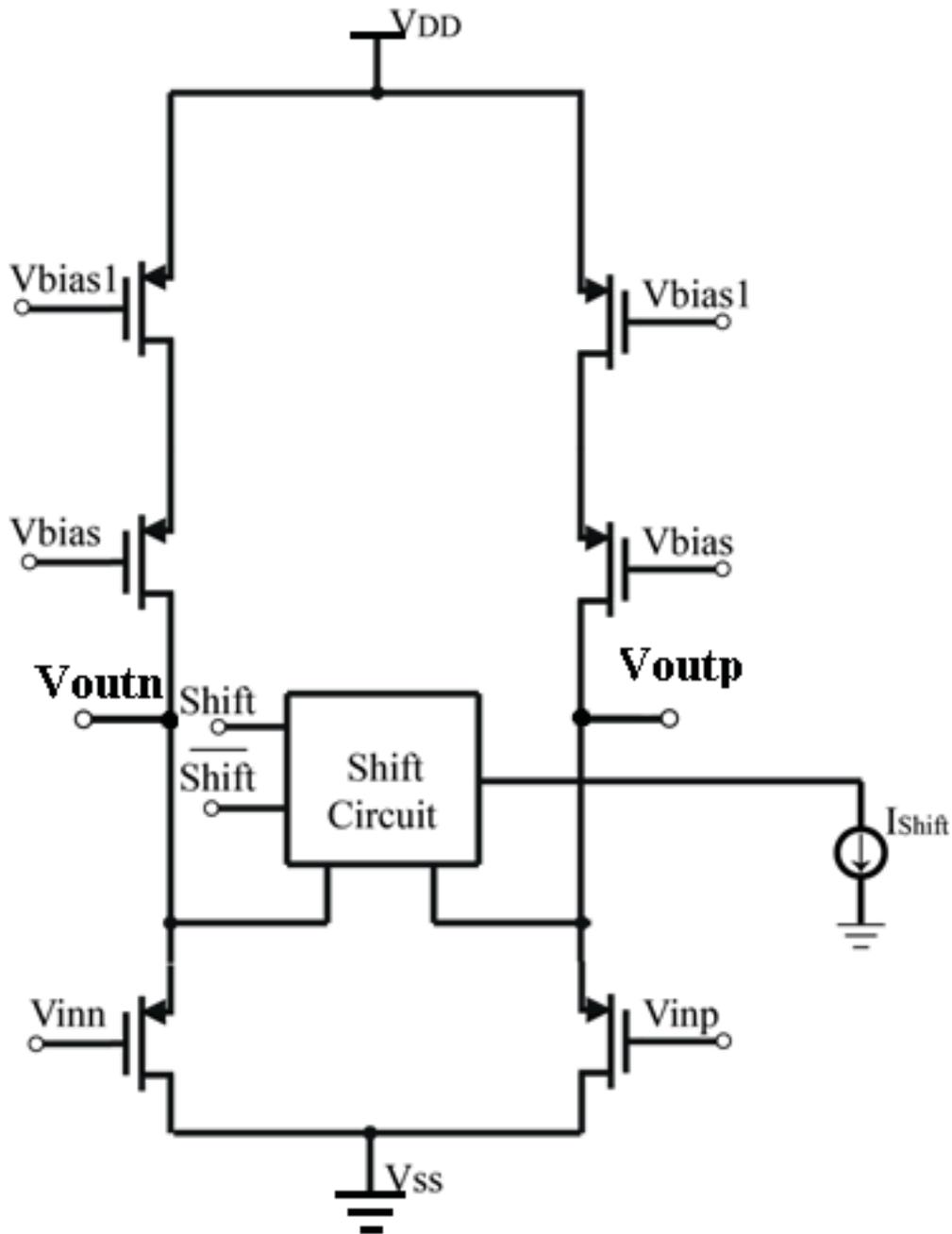Figure 4.10: Source Follower with cascode bias Circuit

4.3 Digital Blocks

Fig 4.14shows the block diagram of digital circuitry. Each flash ADC (A and B) has 127 comparators. The thermometer code generated by comparators are latched in 127 D-flip flops and then through a one's counter the number of high outputs (1.8V) are counted and finally a 7-bit D- flip flop stores the digital outputs of each ADC.
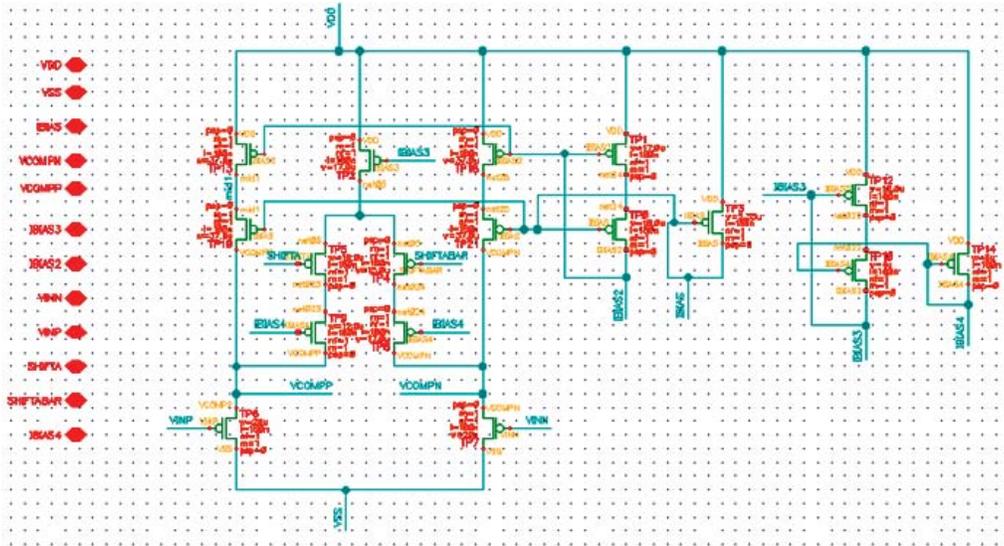
Figure 4.11: Analog shift schematic view

A tapered buffer is used to connect the digital output of each ADC to the pads on the chip.

4.3.1 Decoder Design

The digital circuitry of flash ADC can have a significant influence on the ADC performance. Comparator outputs generate a thermometer code. If the reference voltage is above the comparator input the digital output would be 0, otherwise the digital output would be 1. A thermometer to binary decoder reduces the number of thermometer outputs to n-bit binary output. The errors in thermometer code due to comparator offset, metastability or clock skew are known as "bubble" errors. Bubble erros appears as 0s in the lower string of 1s or 1s in a upper string of 0s. In this work, a ones-counter is used to decode the thermometer code. One's counter has the advantage of providing bubble error correction/supression [94]. Another advantage of using ones-counter is that, based on the speed of the ADC, a suitable ones-counter topology can be used while the power consumption is reduced [94]. Wallace tree topology has been a promising design for high speed applications [94]. The Fig 4.15 shows the block diagram of the Wallace tree decoder that is used in this work. In order to have a symmetric layout, 63 output codes are decoded to 6 bits and the output of the 127th comparator is added to this 7-bit output word using a full adder. To improve the speed of the design in decoding the 63 thermometer output, carry look ahead topology was used. The design of Wallace decoder was implemented with verilog HDL code. The functionality of the design was tested with MODELSIM SE and then the code was synthesized with synopsis using the IBM cmrf7f digital library. The whole layout was done in Encounter which is a
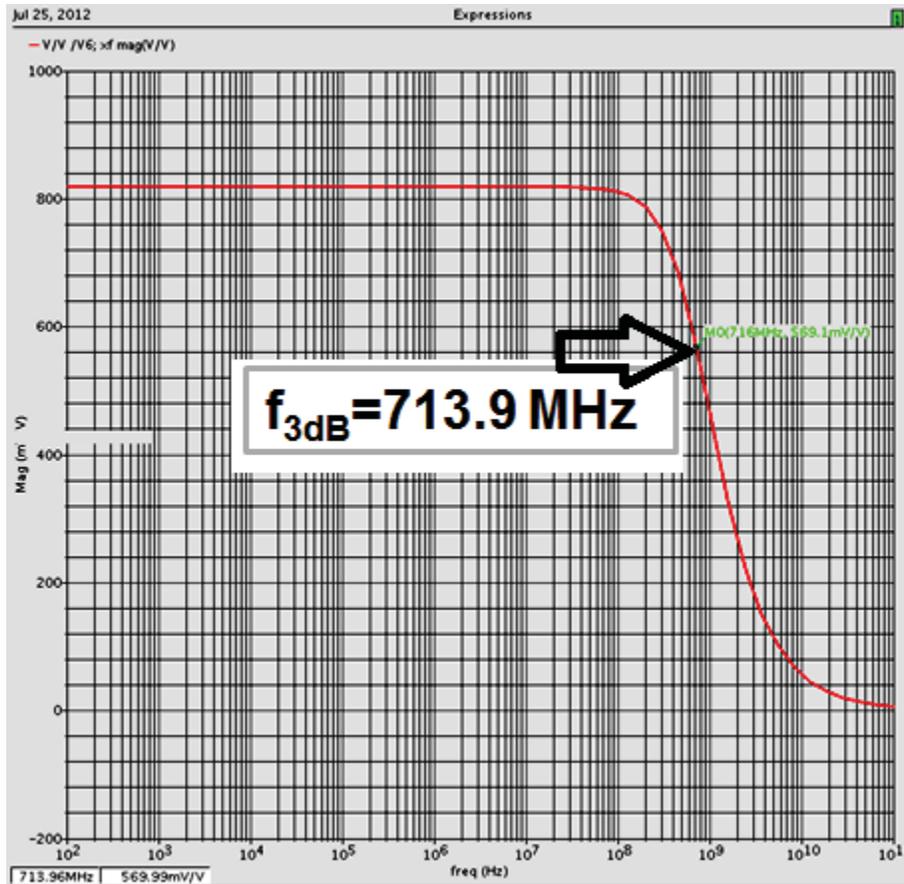
Figure 4.12: Analog shift: AC simulation result

toolbox from Cadence. The Wallace tree decoder and full adder are fast enough to prepare the digital output in 13ns. In other words ADC output is ready after a digital pipeline delay of 2.5 clock frequency. The verilog code related to this design is available in Appendix.

4.3.2 Output Buffer Design

Tapered buffers are used to connect ADC digital outputs to the pads without any limitation for capacitive load up to $10.2pF$. Simulation results show the output buffers do not limit digital output speed. Fig 4.16 shows the block digram of tapered buffer that is used in this work.

4.3.3 Summary

This chapter presented the details on designing a 7-bit flash ADC in circuit level. Analog and digital blocks of this flash ADC were discussed. Dynamic comparator design, metastability and kickback noise in comparators was explained. The PMOS
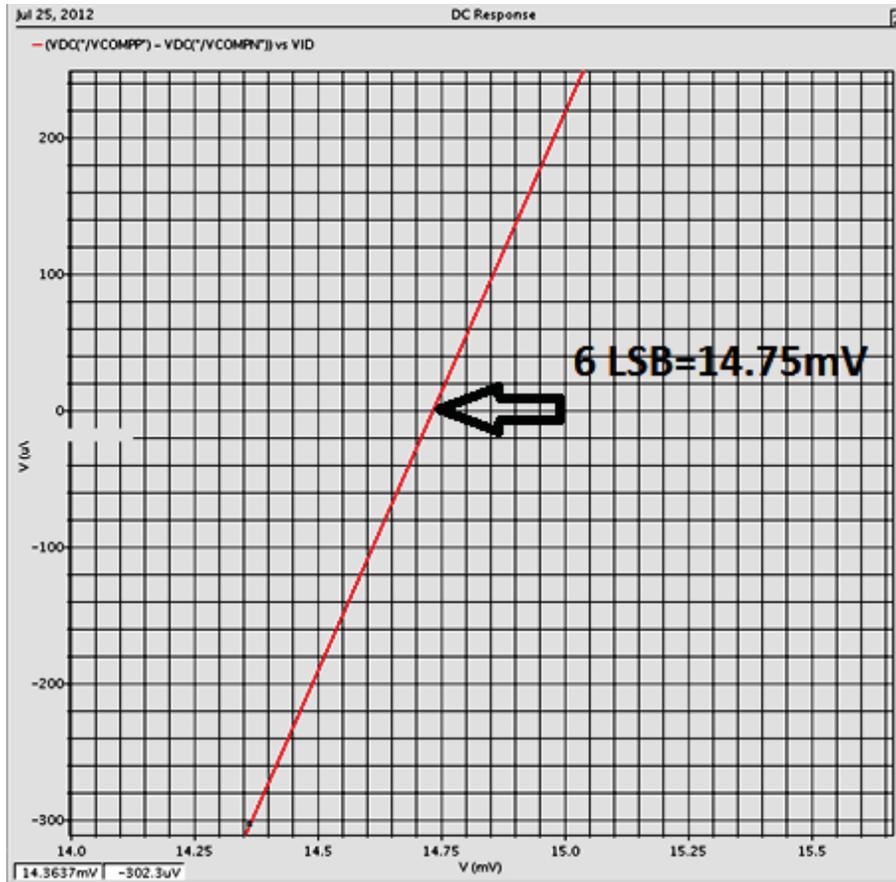
Figure 4.13: Analog shift simulation result: DC response
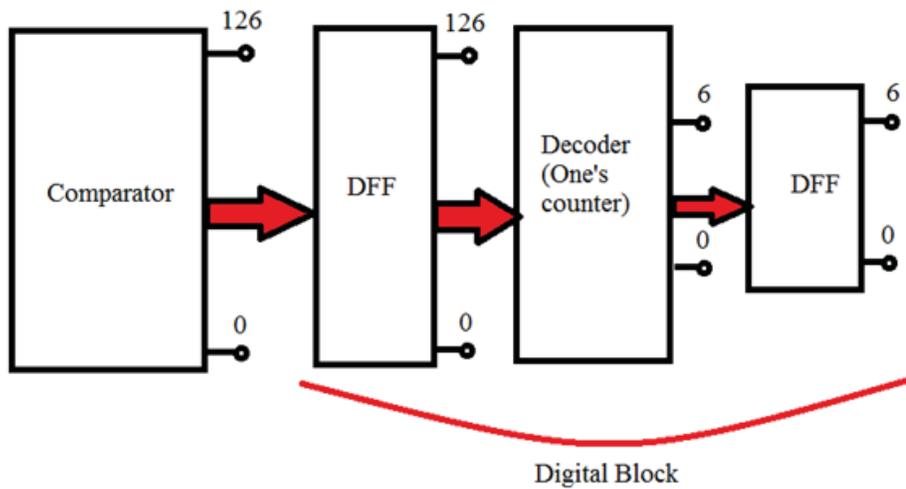
Figure 4.14: Digital block diagram of flash ADC
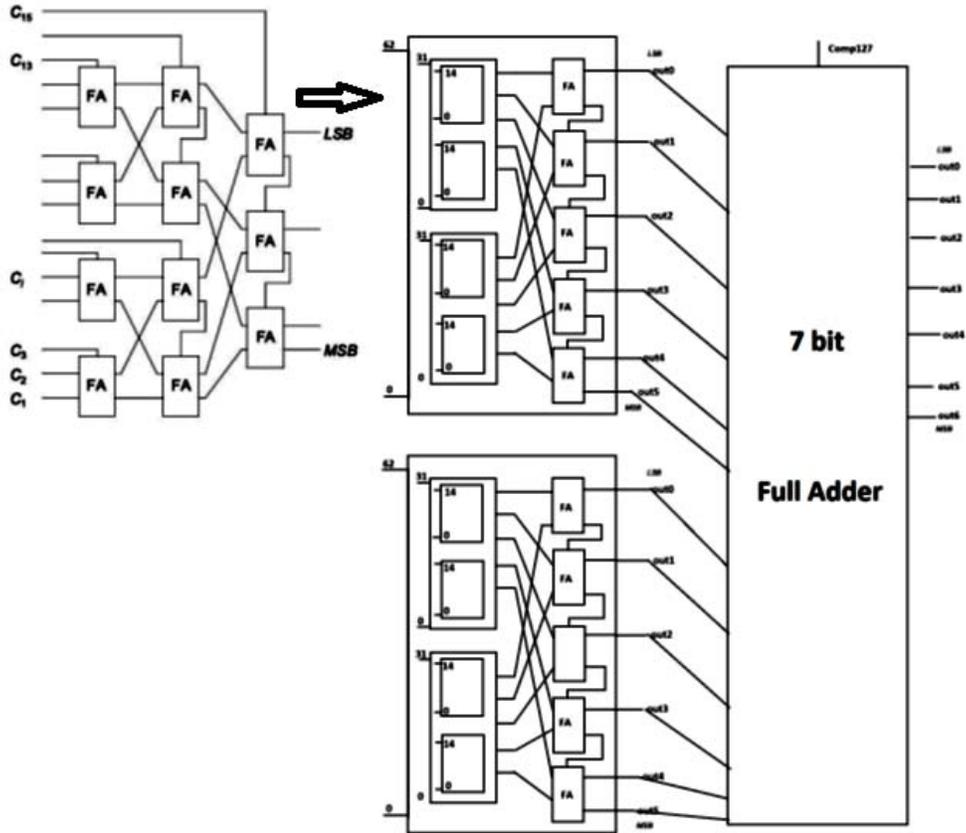
Figure 4.15: Wallace tree decoder for a 7-bit flash ADC
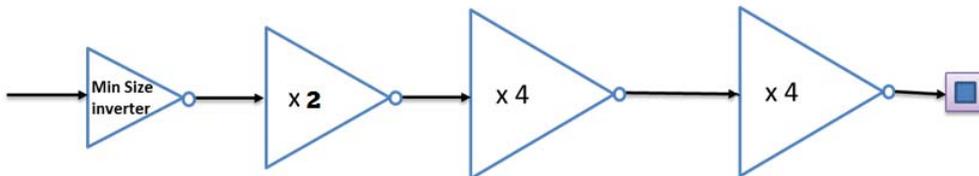
Figure 4.16: Block diagram of output buffers

type source follower as an analog shift structure was discussed. The Wallace tree decoder that is suitable for this flash ADC was explained.

Chapter 5

FLASH ADC Testing and Analysis

5.1 ADC Test Procedure

The split redundant flash ADC was fabricated in IBM cmrf7sf 180nm bulk CMOS technology through MOSIS. The bare dies are wire bonded through MOSIS into a lead-attach 68 pins ceramic QFN package. The die photo of the flash ADC test chip is shown in Fig 5.1.

Test chip was tested on a printed circuit board (PCB) which was designed for this ADC. The detailed PCB design is explained in section 5.1.1. The top level layout of this ADC is shown in Fig 5.2. Each ADC occupies active area of 315 μm $\times$304 μm which excludes the digital buffers.

5.1.1 PCB Design

A 4-layer printed circuit board as an interface between the dies and test equipment has been designed. Two inner layers are split VDD planes and ground planes. Linear regulators with low dropout voltage from Linear Technology [95] are used to create clean power supply and reference voltages. Each ADC has separate analog supplies (AVDDA,AGNDA,AVDDB,AGNDB) and voltage references. Digital output buffers also have their own supply rails (BufVDD,BufGND). Global VDD and GND are used for digital design on chip. Fig 5.3shows the block diagram of the voltage regulator. A 3-pin jumper is placed on the board that allows selection between the regulated voltage and direct voltage from power supply. A decoupling capacitor is also placed on the middle pin of the jumper which goes into the related pin on chip.

The reference voltages for the resistive ladder of each flash ADC are directly generated by a LDO LT3080 and a potentiometer (POT) is used to generated different ranges of voltages to the different ranges of input. A buffer from Analog Devices (AD8652) is used after the resistive divider following a low pass filter to suppress the noise of the reference voltages. Fig 5.4 shows the block diagram of the related circuit.
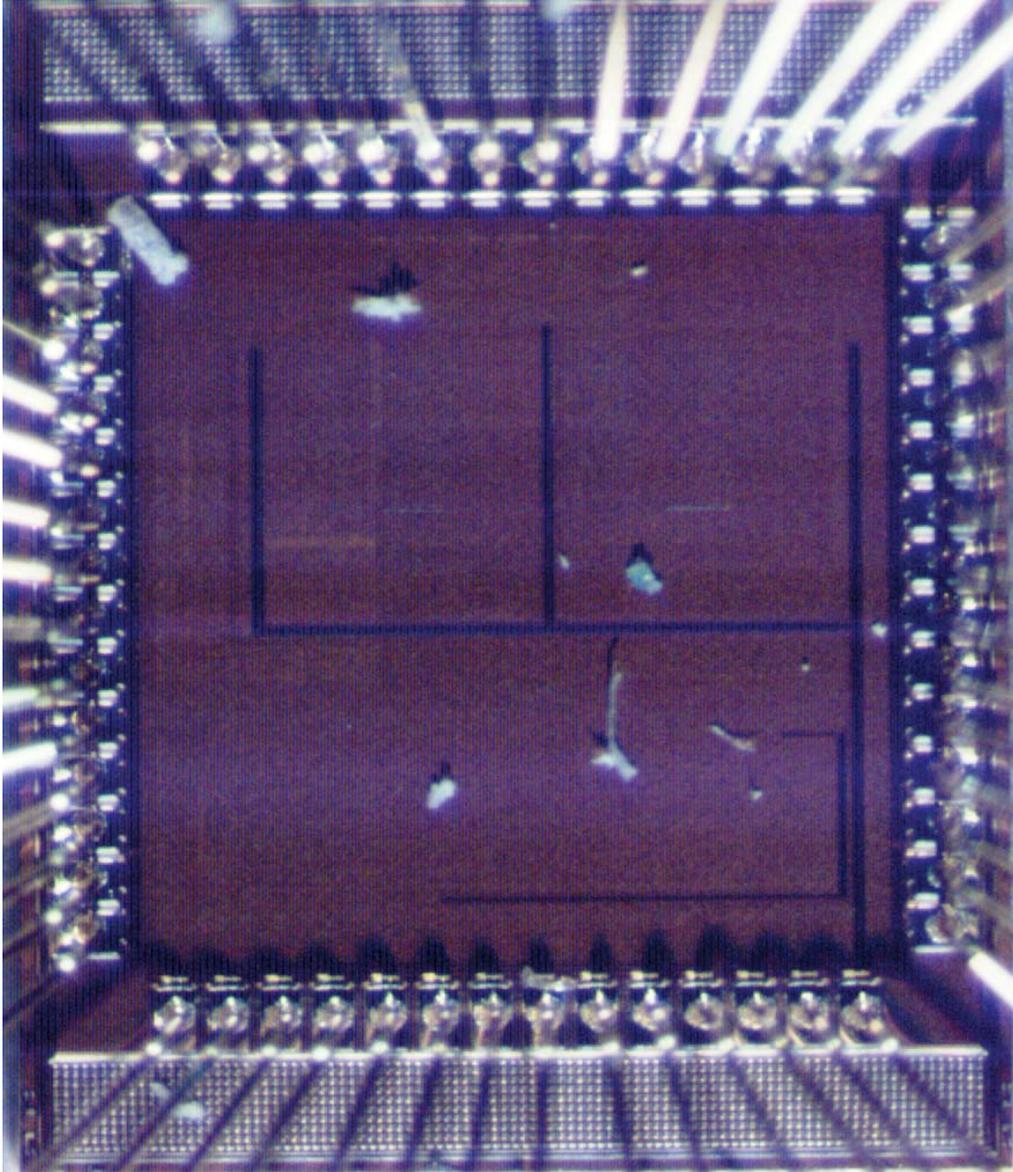
Figure 5.1: Flash ADC die photo

In order to provide a differential input for flash ADC a low distortion single-ended-to-differential converter with adjustable output common-mode voltage from Analog Devices (AD8138) is used. Fig 5.5 shows the bloack diagram of the related circuit. The AD8138 as an ADC driver has a -3dB bandwidth of 320 MHz and low harmonic distortion [96] which is suitable for this 200MS/s flash ADC. Single ended input is available through an SMA.

Bias current are provided with each ADC through resistive dividers with a potentiometer (POT). Latch signal for the dynamic comparators and clock signal for digital block are generated by a high performance triple inverter [97] from ON Semi-
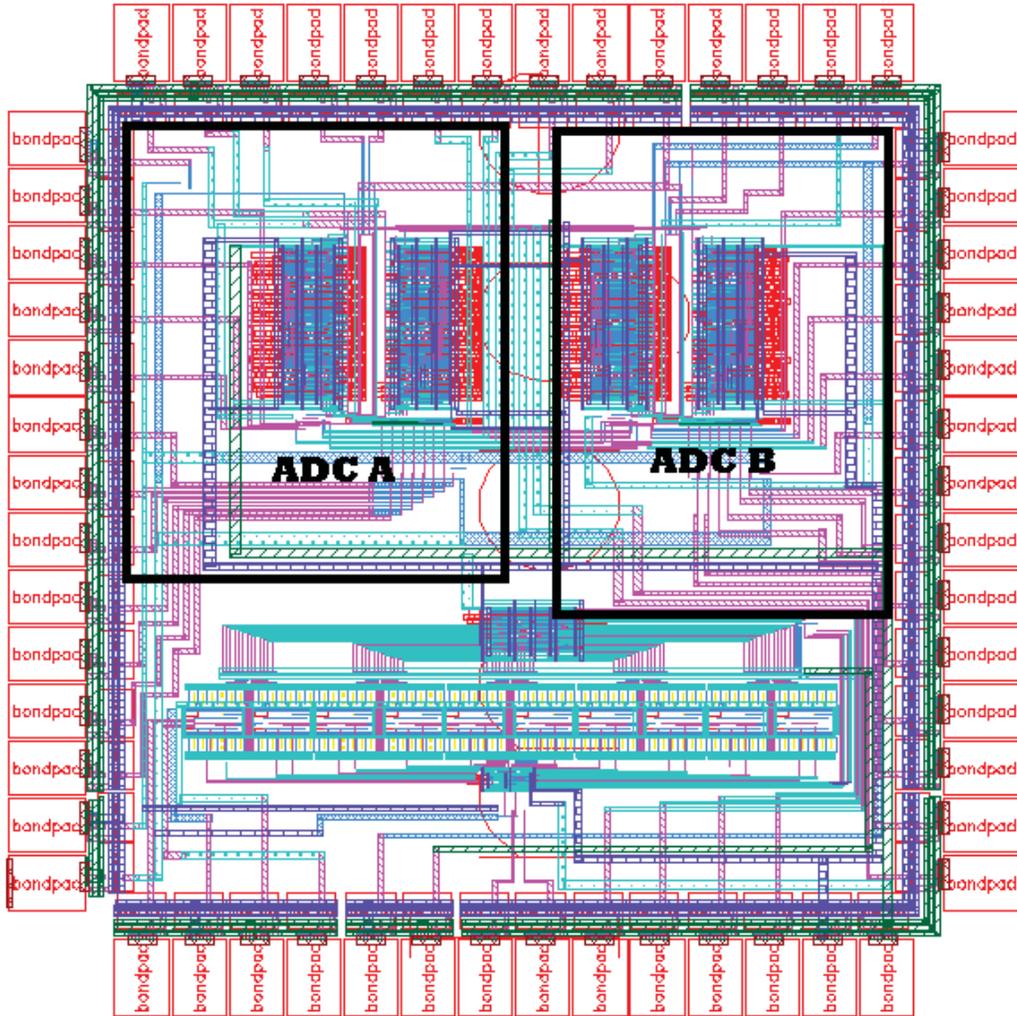
Figure 5.2: Flash ADCs Layout

conductor (NL37WZ04) which is operating from a 1.65 V to 5.5 V supply and has a propagation delay of 2ns. The differential input for pseudo random analog voltage shift are also provided with a low Distortion Differential ADC Driver (AD8138).

In order to avoid signal reflection, PCB traces should be terminated properly. Especially when driving an ADC, the clock distribution circuitry should be placed as close as possible to the ADC clock input. This can help with preventing the degradation in required slew rate and other losses such as undershoot and overshoot [98]. PCB trace dimension (length, width, and depth) affects the characteristic impedence (Z0) of the trace; therefore the output impedance of high speed signals must be matched to the characteristic impedance of the traces [98]. 50Ω resistors are placed on board for impedance matching of high speed signals such as ADC digital outputs and the clock signals.

Although each flash ADC has separate analog ground(AGND) and digital ground

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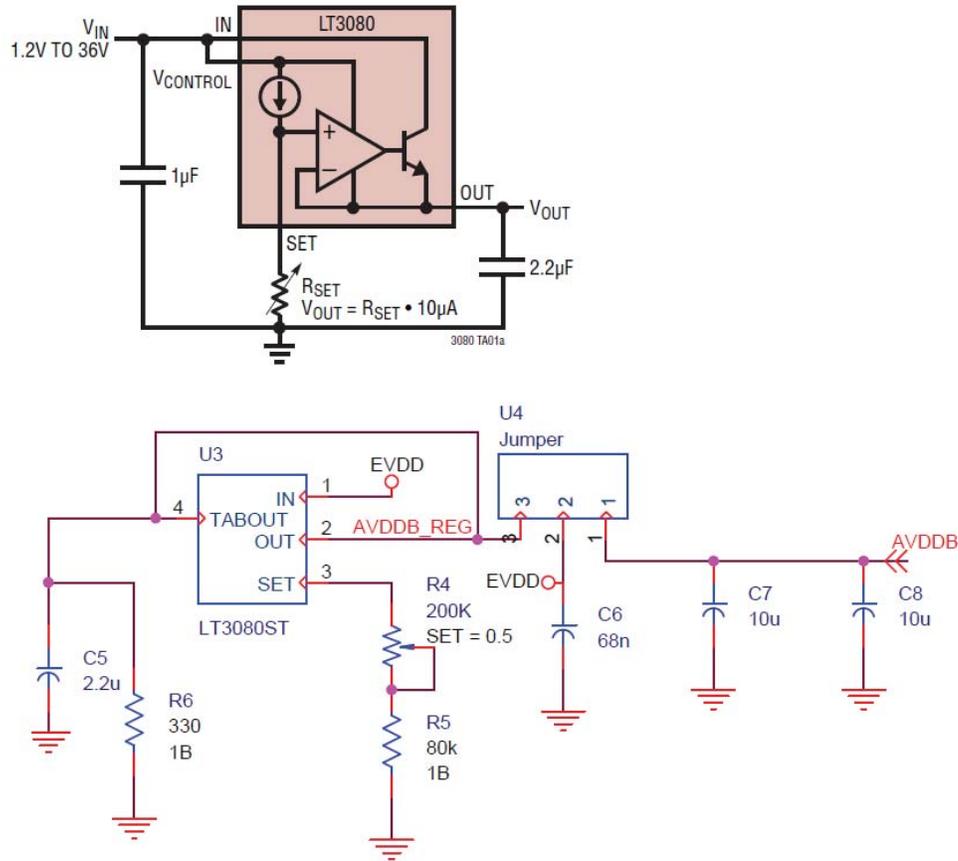
Figure 5.3: Linear regulators with low dropout voltage

(gnd!), for better noise performance, these ground pins are connected on the PCB board. Fig 5.6illustrates the concept of grounding for an ADC [99].

In order to decouple high frequency currents created by fast digital logic signals, a ground plane can be serve as a low impedance return path which can also help to minimize the EMI (Electromagnetic Interference) emissions [99]. The layout of PCB board was produced using Cadence PCB Editor 16.6. The layout and PCB board photo are shown in Fig 5.7 and 5.8.

5.2   Flash ADC Evaluation

While the flash ADC operates at 200MS/s, a slow ramp with 300mV amplitude is used to test the static performance and then a 50MHz full-scale sinewave is applied to measure the dynamic performance. Unfortunately the fabricated test chip failed to work properly and the reason for this failure will be discussed in 5.2.2. Post layout simlations with Casence Spectre shows the flash ADC digitizes the input
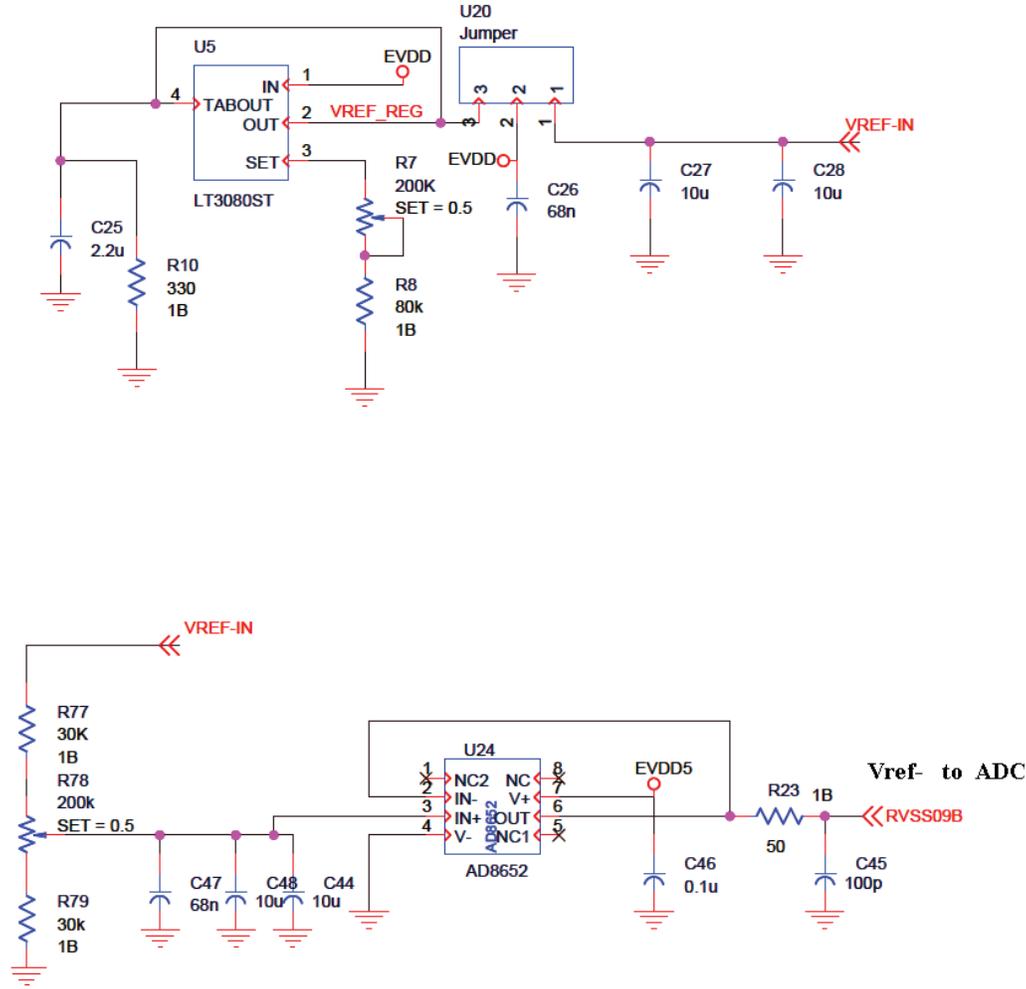
Figure 5.4: Generating reference voltages

signal properly, as described in the following section.

5.2.1 Simulation Results

Cadence Virtuoso AMS Designer, as a mixed-signal simulation solution integrated with the Cadence INCISIVE for digital design verification [100] is used for this flash ADC design and verification. Fig 5.9 shows the simulation results for one redundant flash ADC (out of two split flash ADCs) while the flash ADC works at 100MS/s for 10 consecutive conversions. A slow ramp is applied as an input. Due to space limitation assigned to cadence simulations and the fact that the simulations are time consuming (although APS feature for cadence simulation is used), the number of simulated conversions was not enough to verify the algorithm that introduced in chapter 3. Since the test chip failed to operate properly, the algorithm
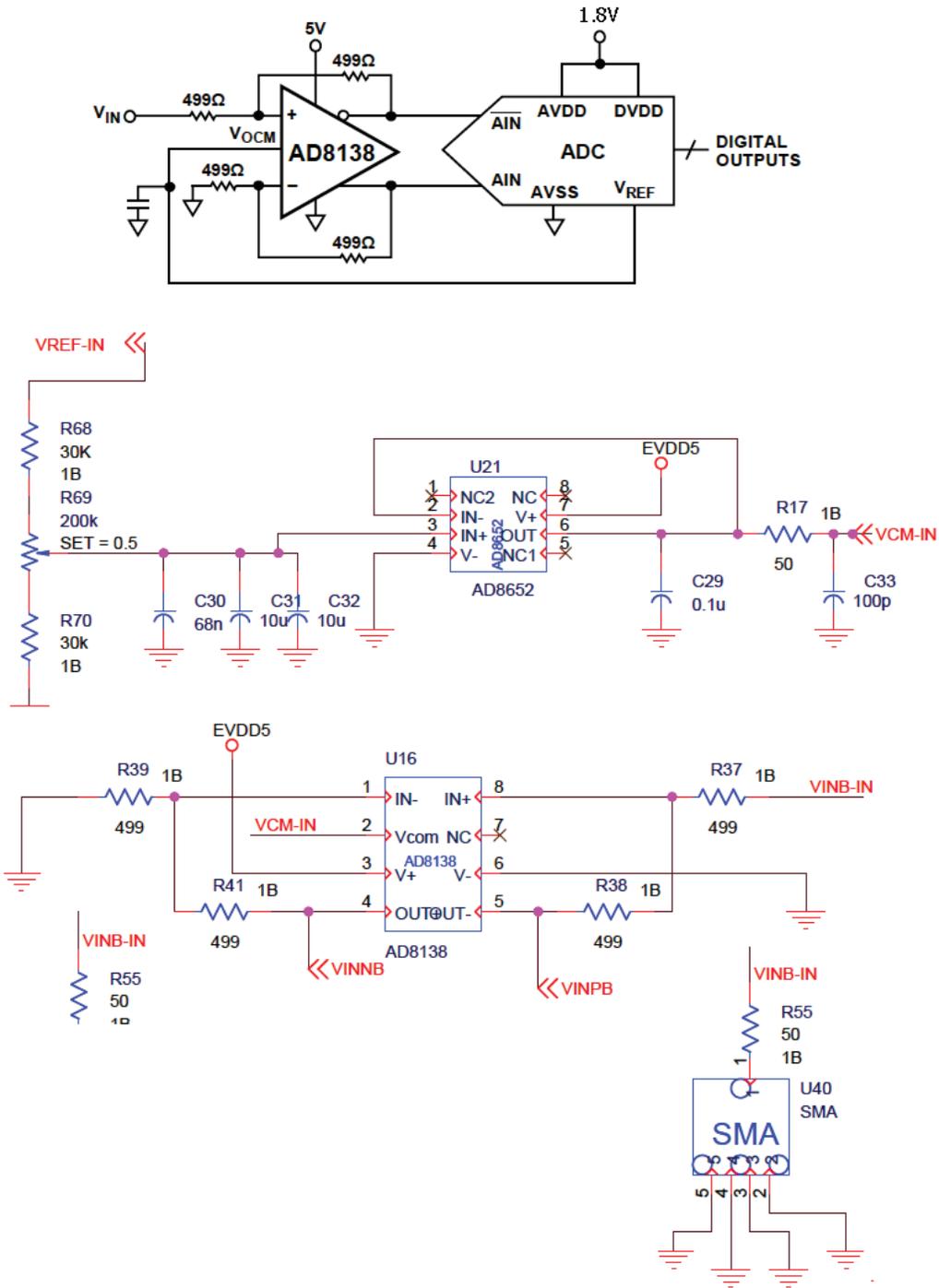
Figure 5.5: Generating differential input for each flash ADC

in chapter 3 was only tested with random input generated by MATLAB.
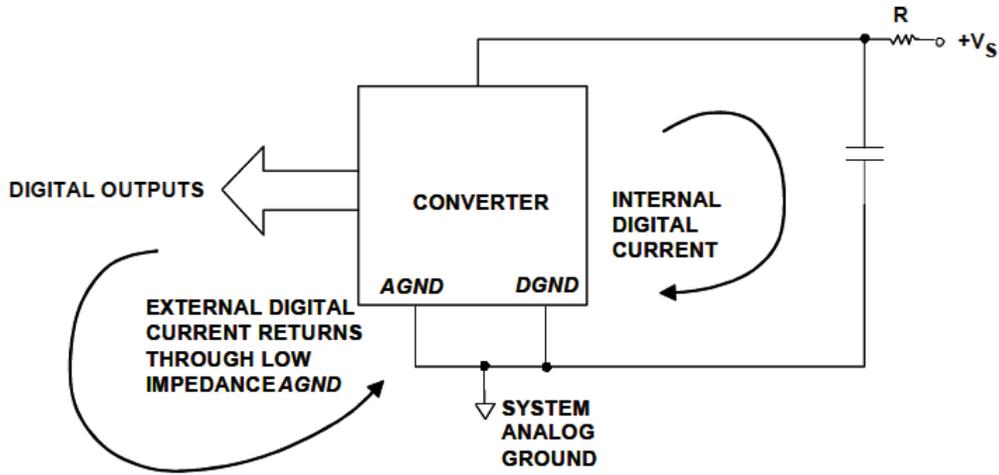
Figure 5.6: Connecting the Analog (AGND) and Digital Ground (DGND) Pins of ADC to System Analog Ground
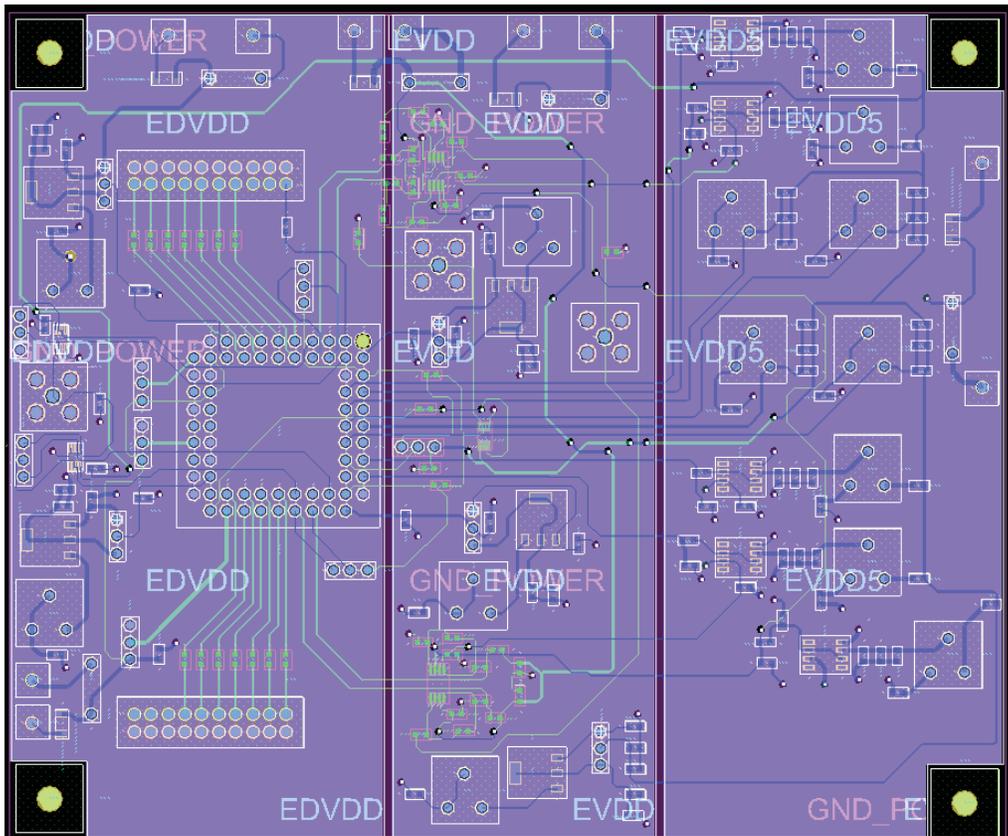
Figure 5.7: PCB layout for flash ADC evaluation

5.2.2 Measurement Results

This section presents failure analysis of swiftly identifying various failure conditions that occur in evaluating the test chip fabricated in IBM7RF 180nm Bulk

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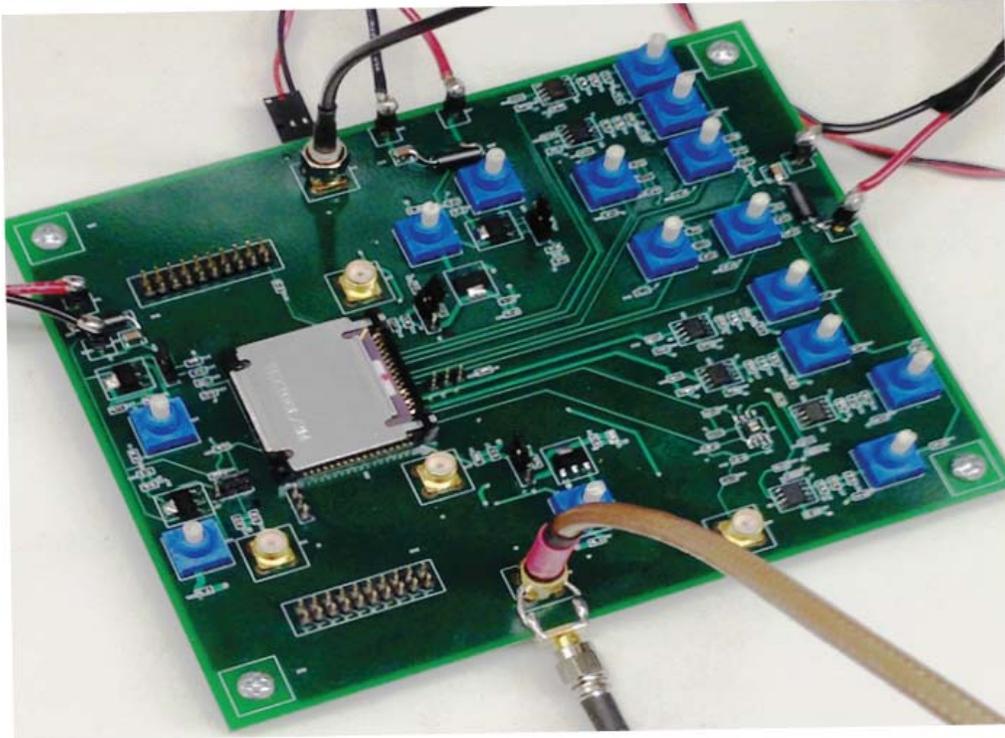
Figure 5.8: PCB board for flash ADC evaluation
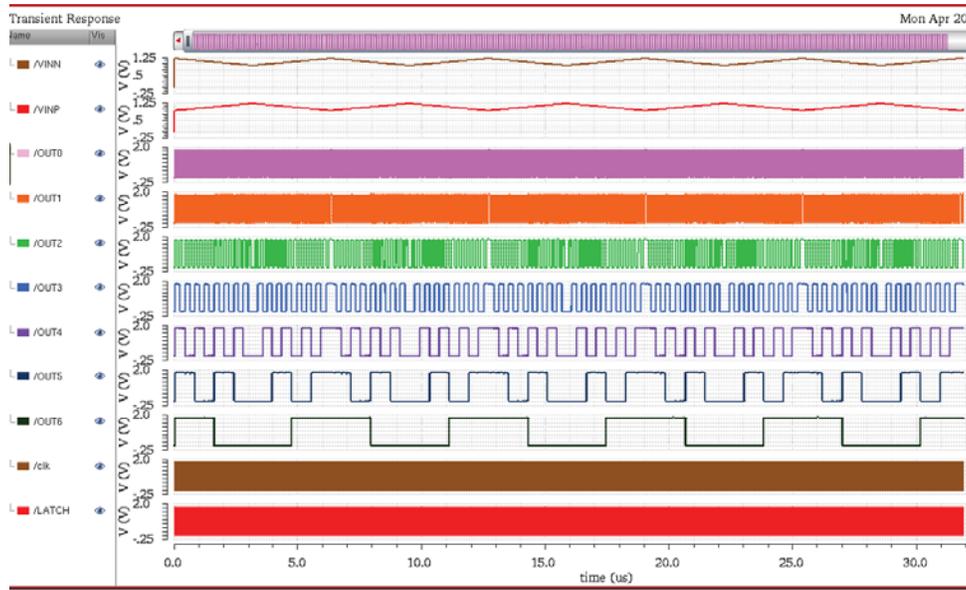
Figure 5.9: Simulation results for redundant flash ADC evaluation

CMOS with 6 layers of Metal (ie. M1, M2, M3, M4, MT, AM with DV (wirebound glass cut). This test chip has 56 bond pads inside a LCC68 Ceramic package (from

MOSIS) and lid attached with 2 corner dot of epoxy. The test chip consists of two ADCs as well as ten delay stages which are used for a DLL design that is not part of this work. The focus will be on causes and mechanisms that led to the failures of the ADCs. Isolation of test chip failure location began by investigating the electrical characteristics using an evaluation board which was designed specifically for this test chip. Then other investigations such as package inspections and bond wire and ESD inspections were performed. Finally test chip analysis from MOSIS was requested and careful layout check was done. Fig 5.10 summarizes the chip failure determination procedures.

- Evaluation of Electrical Characteristics: An oscilloscope is used for DC and AC characteristics evaluation. A voltage regulator (LT3080 from Linear Technology) is used to feed the ADC with clean supply voltages. When the DC input of 300mV is applied to the ADCs, the MUX and MUX' the two outputs of the DLL delay stages have a negative voltage of -400mV. NVDD (-5V) is only used as a supply for AD8138 which is a single ended-to- Differential converter. The assumption was failure due to ESD problem. To evaluate AC characteristic, a low frequency signal generated by function generator was applied to AD8138. ADC Input was a (10 kHz-100 kHz) sine wave with 300mVp-p amplitude and common mode of 0.35V. It was observed the input of ADC was reflected to the output of the ADC and by changing the frequency of the input, the frequency of the signal at the output was changed. The power supplies reached the current limit for the analog and digital supply during the DC and AC evaluation (400mA for digital supply and 327mA for Analog supply). In case the problem was caused by evaluation board, the second version of evaluation board with different routing was made. Different test chips were tested on the populated and non-populated evaluation boards in order to compare the current value of each case. In all different test cases the power supply reached the current limit. AVDDB which was the analog supply for the ADCB pulled a lot of current. Bonding diagram and chip layout was checked carefully. The chip footprint and the chip bond pads were compared. There was not any problem with these tests. High voltage and low voltage across the ESD of each section is connected to the related VDD and ground in that region. By disconnecting the bond wire of AVDDB, it was expected to see the large amount of current will disappear. But the power supply reached the current limit again. Then the inputs to the ADC were grounded and tested the ESD performance by sweeping the voltage from the low to high across the ESD diodes until the power supply reached the current limit. The test had four different cases. The test was performed on the cases with and without AVDDB connected to the voltage. Fig 5.11 shows when the voltage reaches 0.6V, when the diodes inside the ESD are ON, there is a big jump in the current!However cadence simulations for ESD test did not show any unexpected behavior in ESD performance. The next step was inspecting inside the package.

Test	Method	Result	Conclusion
DC characteristics	Apply DC Input to ADC	Negative output Values on DLL pins and large amount of current on power supply	Floating gates?/Short circuit somewhere in the chip/ESD Latch up?
AC characteristics	Apply low frequency sine wave/Ramp signal	Reflection of Input to the output! By changing the input frequency the output frequency changes	Antenna Violations Find the failure location that pulls lots of current
Match the bonding diagram and chip layout	Use Cadence Layout and Allegro PCB Layout to match the pins	Pins are matched	No pin position problem, check the bond wires
Bond Wire	Microscope	All the connections are fine	No wiring Problem
Power Supply check on the different populated/non populated Evaluation Boards to make sure the problem is with the chip not the PCB (Two different evaluation boards with different routing are made to evaluate the chip)	Isolating the power supplies from each other to find the source of high amount of current Disconnect bond wire related to the part that is assumed to be faulty	No changes in amount of current from power supply	ESD problem?
ESD characteristics	Apply zero Input	Current jump in order of mA	Latch up problem?
ESD/Bond pad short-cracking	Optical Microscope	No Problem	No fabrication problem
Request for Fab Analysis	DRC check by MOSIS	ESD Flags- Possible floating gates- Antenna Violations	Check the layout that was assumed to be DRC-LVS clean more carefully
Careful Layout checking	ERC check Add command to extarct6.rul ercCheckFloatingWell(directOnly) DRC check Floating.rul ESD.rul	Floating NWELL- PMOS problem Floating NWELL- PMOS problem	Use other method to find floating nets/wells Apply the rules to smaller area- find the Problem!

Figure 5.10: Procedure of Chip Failure Determination

- External Visual Inspection of the chip: In this step, floating bond pads or ESD defect were investigated. The test chip was observed with an optical microscope and SEM. External visual inspection of the chip shows the ESD and bond pads do not have any cracking or defect problem. There are no floating pads over interconnects. There is no bond pad-to-bond pad failure mechanism. The die photo for ESD defect investigation are shown in Fig 5.12 and 5.13.

- Fabrication Analysis: Prior to submission of flash ADC for fabrication, the design had a DRC and LVS clean report. Several ESD tests done in cadence and post layout simulation using Assura-QRC extracted layout did not show any problem in the performance of the ADCs. A request for test chip analysis was submitted to MOSIS. They provided their DRC report which showed some antenna violations and ESD warnings. Investigation on possible floating gates and the wells was perfomed. More DRC rules and ERC simulation was used for well checking. Working with IBM technology ERC-checks raises the flag to show contacts or diodes that create either a short or a forward biased
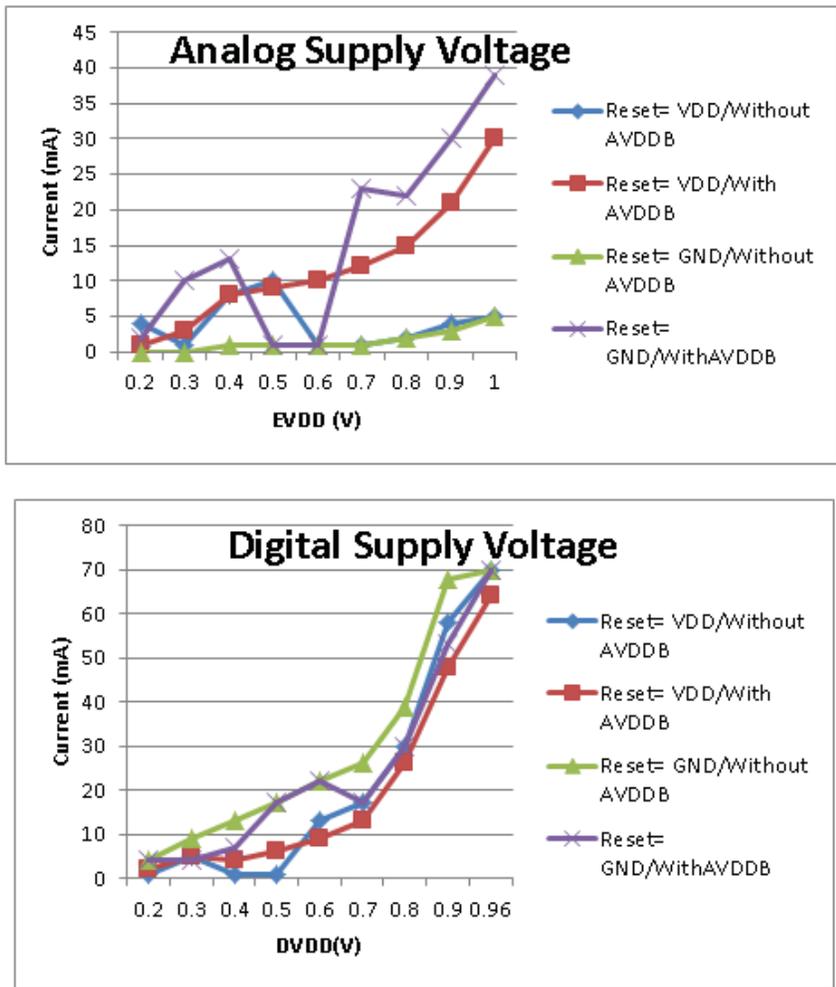
Figure 5.11: ESD test for flash ADC evaluation

condition that happens between power and ground nets. NW bias checking is also performed with ERC checking. In this technology substrate-derivation is associated with the "$NO - SUBC - IN - GRLOGIC$" switch. ERC checking is performed through LVS run. By adding this command: "ercCheckFloating-Well(directOnly)". ERC-checks shows the substrate of nfets is floating. Final ERC and DRC simulation for the main subcircuit in the design which is the comparator circuit shows floating WELL is happening for the PMOS input pairs inside the comparators. The PMOS-body of input pairs must connect to a voltage (BIAS1) different than supply VDD in order to use the body biasing technique to improve the comparator speed. In IBM cmrf technology there is no physical layer for PMOS body (inherited device) and subc represent the substrate for NMOS devices. The layout mistake on using the subc to connect the body of PMOS devices to BIAS1 created the floating substrate and was
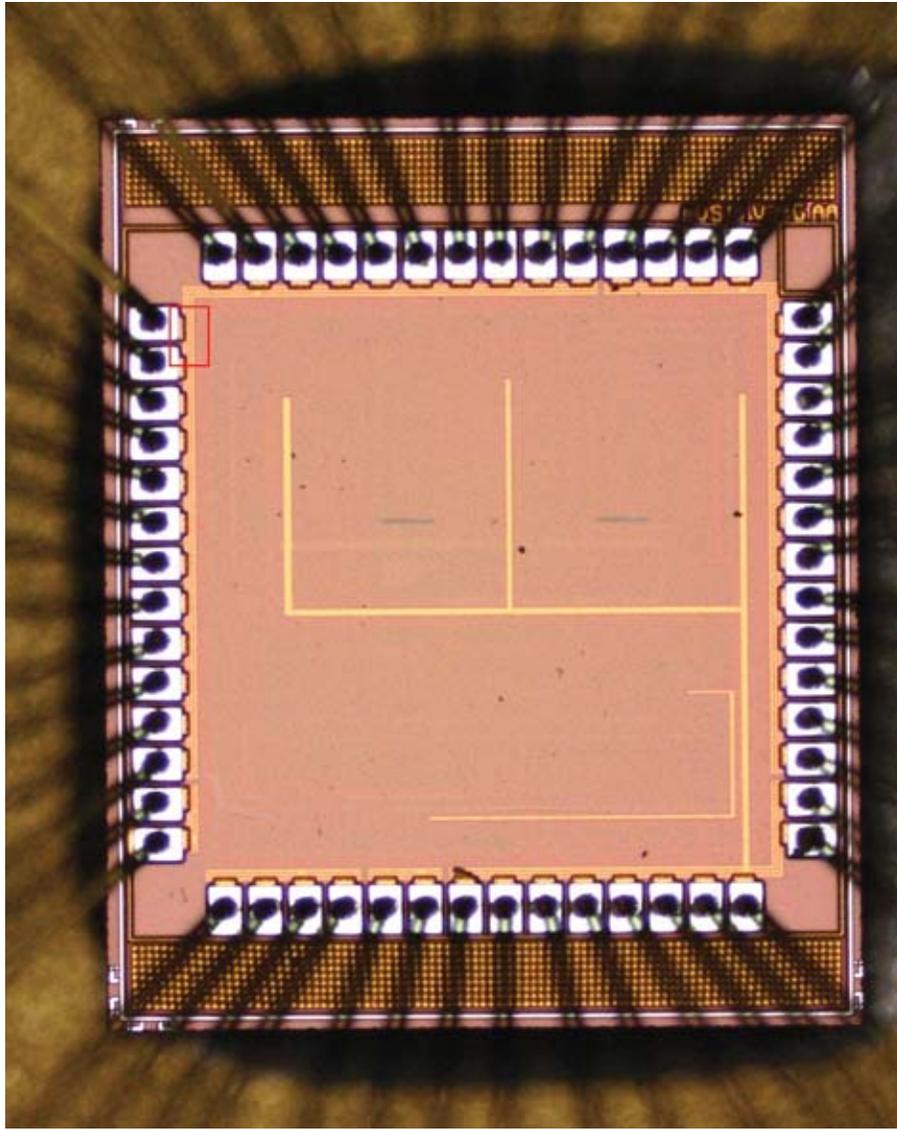
Figure 5.12: Test chip under optical microscope

the main reason of chip failure. Fig 5.14 ilustrates this connection mistake.

5.3 Performance Analysis

The 7-bit flash ADC was simulated in Cadence. Simulation results show the split Flash ADC consumes 4.45mW power for analog block and 1mW for digital block and has a FOM of 164 fJ/conversion step in simulation. Fig 5.15shows the histogram based differential nonlinearity (DNL) plot of one redundant flash ADC according to the simulation results. DNL results show the redundant flash ADC is monotonic and has no missing codes. The peak DNL is 0.32/-0.39.
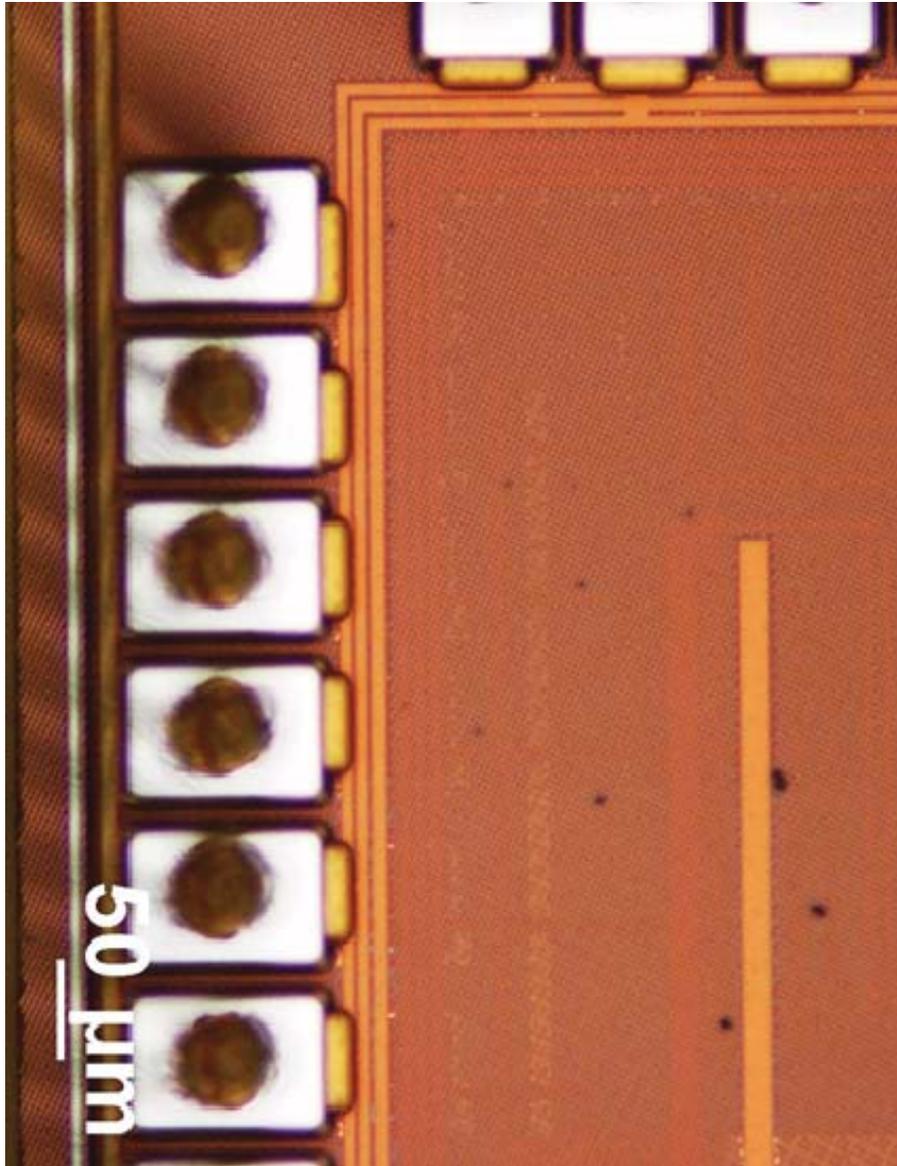
Figure 5.13: Closer view of ESD and bond pads

5.3.1 Summary

This chapter presented the detail on test and measurement of the fabricated 7-bit flash ADC. Design of a 4-layer evaluation board for this flash ADC was explained. Source of errors for chip failure were explored and cadence simulation result was provided. layout error to be corrected for future implementation was presented.
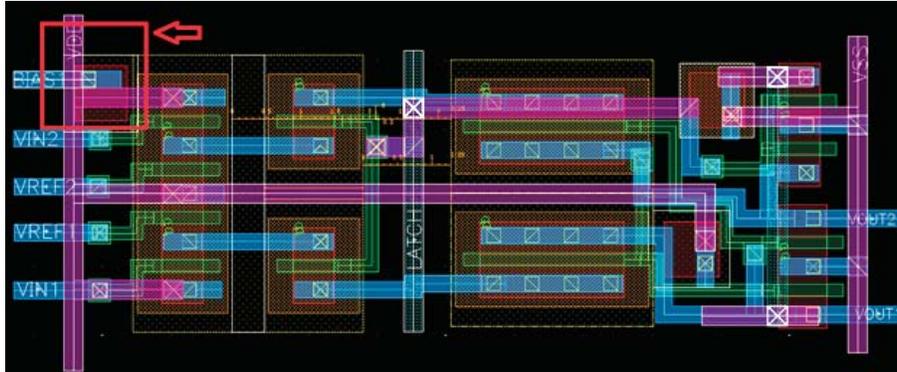
Figure 5.14: Layout mistake on PMOS substrate contact
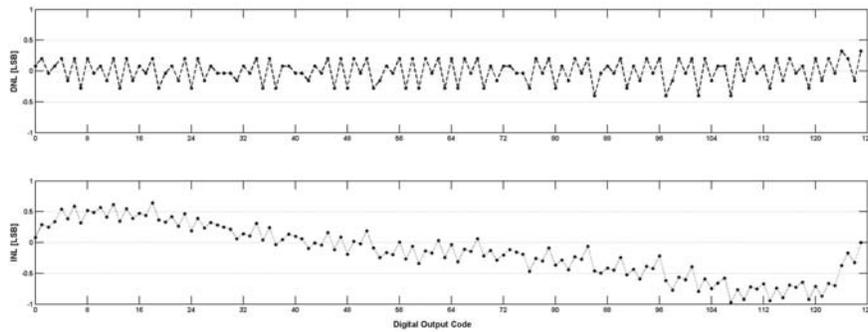
Figure 5.15: DNL result for redundant flash ADC

Chapter 6

SAR ADC Chip Implementation

6.1 SAR ADC Proposed Algorithm

This chapter presents a new switching algorithm which is proposed to reduce the power consumption of a successive approximation ADC (SAR ADC). Successive approximation ADCs are widely used as medium-to-high resolution and medium speed data converters. For high resolution SAR ADCs, fully differential techniques provide the best common mode noise rejection and lowest distortion [101]. For medium resolution ADCs in power-critical applications such as battery management, the lower power consumption of simpler single-ended architectures are attractive.

This chapter describes the design of a single-ended 7-bit SAR ADC that drives design tradeoffs toward minimum power consumption. Power reduction is achieved using a new method of switching the SA-ADC capacitive DAC, as well as improved efficiency in capacitor area.

6.2 SAR ADC Implementation

The conventional SAR ADC as it is explained in 2.4.3, consists of control logic, comparator, and capacitive DAC (CDAC). For medium resolution SAR ADCs in aggressively scaled CMOS technology, the contribution of control logic and CDAC switching must be considered to minimize overall ADC power consumption [13].

Several methods have been proposed to reduce CDAC power consumption. In [101], a switching method uses two CDAC arrays and a reference voltage of half amplitude $V_{REF}/2$. One capacitor array is used to sample the input and the switching is performed on the other array. This method imposes an area penalty for the second CDAC array, and is sensitive to the $V_{REF}/2$ biasing voltage. In [30], a capacitor splitting technique reduces the switching energy by 37%. In [102], a multi-step charging method in the charge redistribution DAC using a split capacitor array structure is proposed. This method introduces additional design complexity as well as making ADC linearity dependent on proper control of CDAC switching.

In [63], a switching method is described which is very power efficient. Eldo simulation results in the $0.35\mu m$ technology targeted for this work demonstrate power savings commensurate with those described in [63]. The work described in this chapter explores the opportunity for further improvement in power and area savings by eliminating the differential approach of [63] in favor of a single-ended architecture.

For the 7-bit resolution required in this work, a single ended SA-ADC with fewer numbers of devices than a differential topology is implemented as shown in Fig. 6.1. The building blocks of the proposed ADC are a comparator, control logic with decoder, CDAC, and switching network. As in [63], a binary weighted capacitor DAC provides adequate linearity.

The CDAC capacitor network serves both sample-and-hold and DAC functions. As shown in switching waveforms of Fig. 6.2, the signal and DAC voltage ranges are bounded by V_{in-min} and V_{in-max}.

The distinguishing feature of this architecture is the use of switches S1-S4 at the comparator inputs to allow a different target voltage for the DAC successive approximation process. The target is chosen depending on the value of the input and the MSB decision. Figure 6.2 shows the waveforms at the comparator inputs in the two cases. The ADC splits the searching algorithm into two regions as follows.

At the beginning of the conversion switch S1 and S3 are closed and the ADC input voltage V_{input} is compared directly with $V_{in-half}$, the midpoint of the signal range. After the MSB decision, switch S3 is opened and S4 is closed at the comparator - input for the remaining decisions. At the comparator + input one of two outcomes results depending on the MSB decision:

- MSB=1 (Figure 6.2a): If the output of the comparator shows $V_{input} > V_{in-half}$, the MSB is set high. Switch S1 remains closed and the successive approximation process converges toward $V_{in-half}$.

- MSB=0 (Figure 6.2b): If the output of the comparator shows $V_{input} < V_{in-half}$, the MSB is set low. Switch S1 is opened, switch S2 is closed, and the successive approximation process converges toward V_{in-min}.

The advantage of this technique is that the largest capacitance (and its associated switching) is removed from the DAC network, which reduces the area, power and capacitor switching.

While the function of the remaining cycles follows the conventional SA-ADC approach, the implementation of the design features techniques which provide further power savings. This ADC was designed for an application in which the signal range was limited to the range $300mV < V_{input} < 900mV$. Since this technology provides a 3.3V supply and the maximum voltage in DAC is 2V no bootstrapped switches are needed to turn on the NMOS switches.

A 3-to-8 decoder provides the switching for the remaining approximation cycles of the ADC. Only one capacitor switch is needed for each bit cycle which minimizes
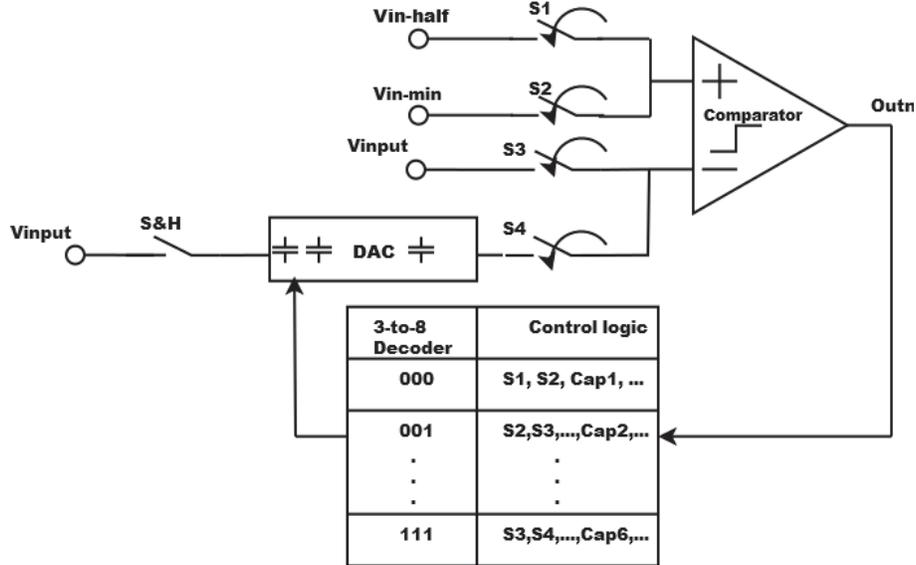
Figure 6.1: Proposed SA-ADC architecture

charge transfer and power consumption. Since the first MSB is determined without any capacitor switching, this can save a significant amount of power consumption.

6.3 ADC Building Blocks

6.3.1 Dynamic Comparator

To minimize power consumption, a dynamic comparator is chosen, with schematic as shown in Fig.6.3. A PMOS input differential pair is used, since the analog input common mode range in this specific application was close to ground. The comparator uses the Lewis-Gray [87] architecture: when 'Latch' is high the comparator is reset; when 'Latch' is low regeneration around the MN1-MN2 loop is enabled. The conductivity imbalance from the MP1-MP2 input pair [63] forces the comparator output to go low or high.

Additional offset cancellation techniques are applied to address mismatch in $MN1 - MN4$. To minimize the variation of effective voltage of the input pairs MP1-MP2, transistor Mc biased in saturation is added in the source path of switch $MP3$ [63]. $MP9$ and $MP10$ are added to improve the device matching. Cascode transistors $MN5$ and $MN6$ are added to increase the gain of the differential structure and thus decrease the input-referred comparator offset. Note that separate bias is used for NMOS cascode devices to minimize the influence on capacitance of regeneration nodes. $MP4$ and $MP5$ are added to improve the rise time.

Figure 6.4 shows results of a Monte-Carlo simulation of comparator offset for the comparator of Fig. 6.3. The standard deviation of $\sigma = 2.26mV$ gives an overall

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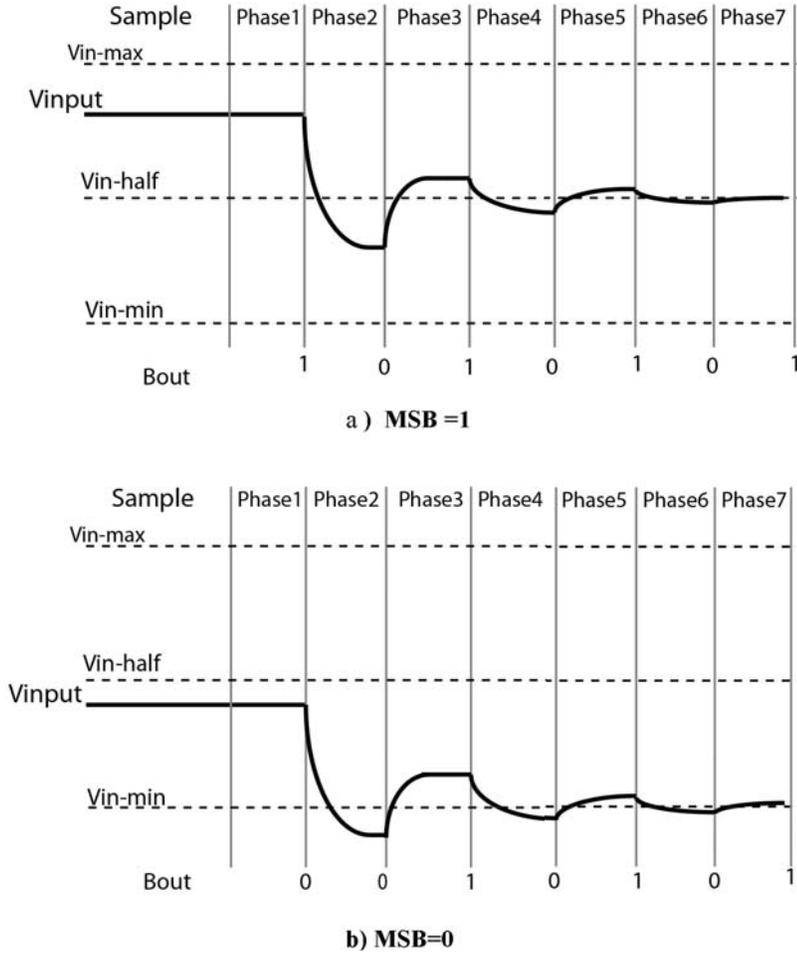
Figure 6.2: Waveforms of proposed switching procedure: (a) MSB=1 (b) MSB=0

ADC offset less than 1LSB, which is adequate for the targeted application.

6.3.2 DAC Capacitor Network

For the CDAC unit capacitor, a MOS capacitor in enhancement is used as it consumes less area than an equivalent value MIM capacitor and the error of charge injection from gate-source parasitic capacitance of NMOS switches in DAC logic is minimized. To achieve more linearity given the voltage swings in this specific application, P-type enhancement-mode MOS is chosen. The size of the unit capacitance is 66fF, with total layout area $6.1\mu m \times 6.1\mu m$ which satifies $\frac{kT}{C}$ limitations. As mentioned in Section 6.2, only one capacitor array is needed for the single ended SA-ADC approach, resulting in significant area saving. The 7-bit SA-ADC uses 63
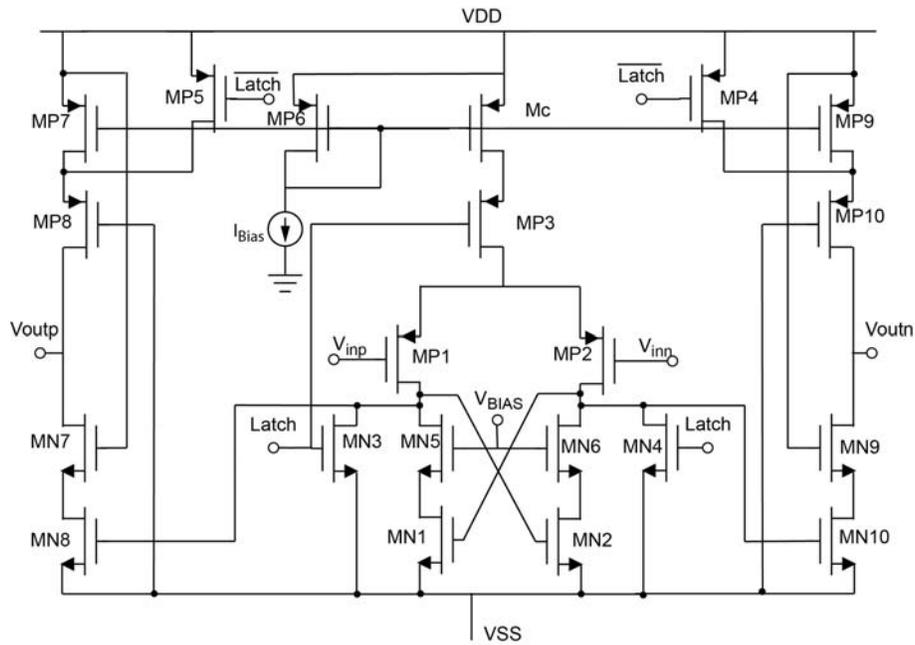
Figure 6.3: Dynamic Comparator
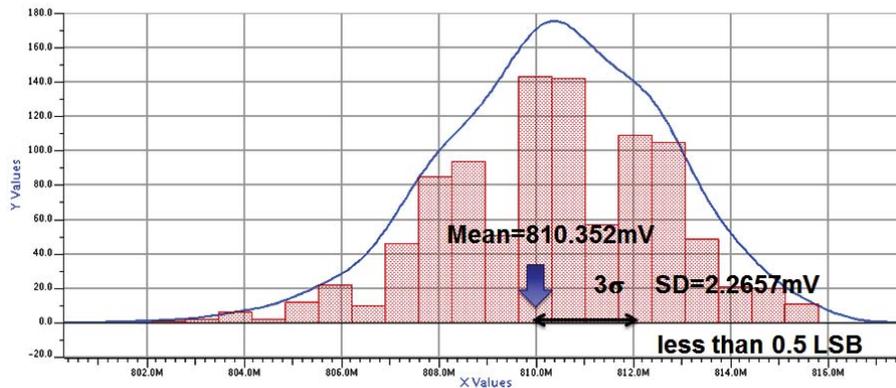
Figure 6.4: Monte-Carlo simulation of comparator offset. $\sigma = 2.26$mV

unit capacitors, giving a total capacitance ≈ 4pF. Monte-Carlo simulation of the capacitor network shows adequate matching for the linearity required of a 7-bit ADC. The charge and discharge path for the capacitors is through NMOS transistors. The gates of these NMOS transistors are controlled by the output of the switching logic network, as described in section 6.3.3 below. Careful layout techinques were observed to avoid parasitic influences on DAC performance [63].
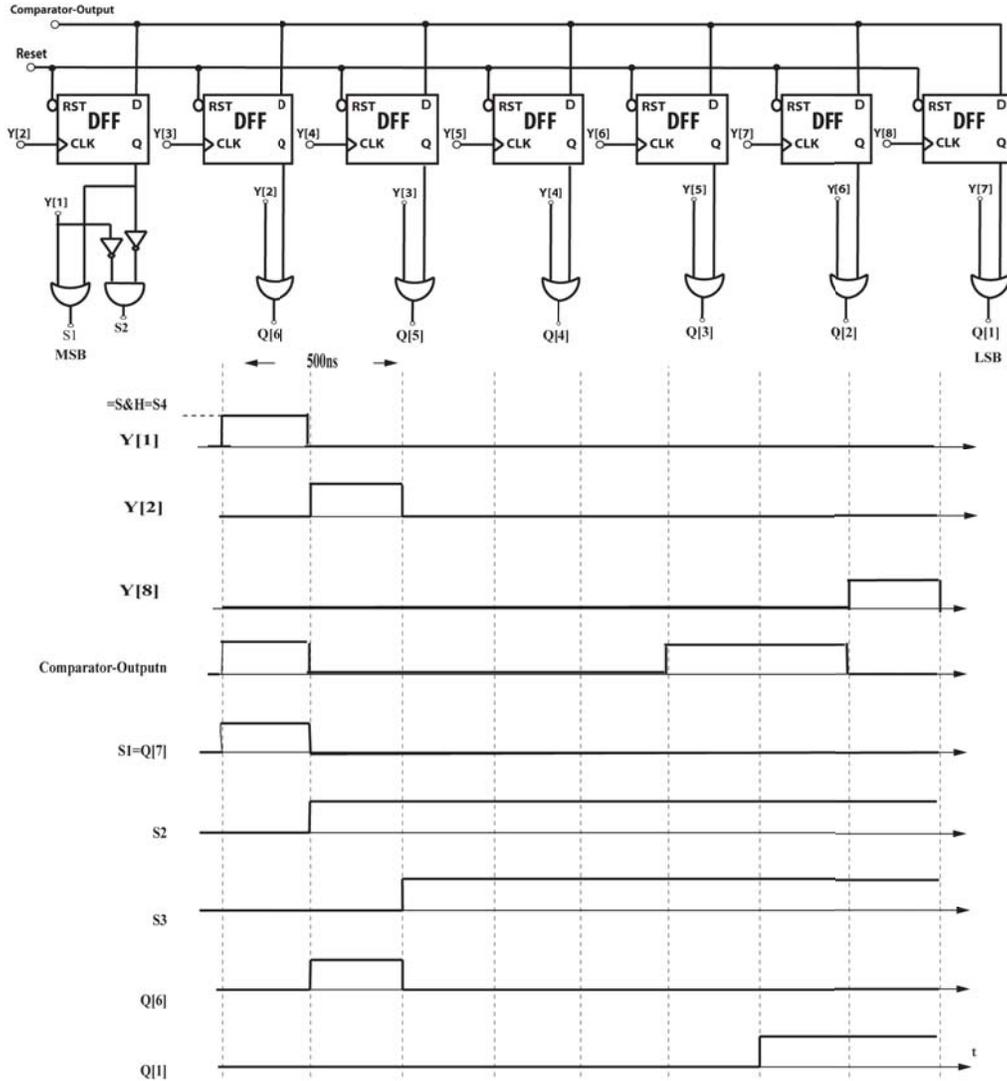
Figure 6.5: Control logic switches and timing

6.3.3 Switching Logic Network

Figure 6.5 shows the structure of the control logic circuitry and the timing diagram
of the decoder signals and switches. To minimize the power consumption the clock
signal for registers are all produced by a decoder. 7 registers are used to hold the bit
values. A 3-to-8 decoder generates 8 signals Y[1],...,Y[8]. Appropriate combinations
of these signals generate the control signals for the DAC and S1 and S2 switches.
Switch S1, S2 and S4 and the Sample and Hold signals are generated from Y[1] and
Y[8]. A one-shot reset is also generated at the beginning of the conversion from Y[1]
which is used to reset the registers when the conversion starts.

6.3.4   Sample and Hold

The input sampling signal is generated through the 3-to-8 decoder. To give enough time to ADC to sample the input, the sample control is the OR of first and last decoded signal (Y[1]+Y[8]). Sampling switches are CMOS transmission gates. The sampled input is held on capacitive DAC network. No additional sample and hold circuitry is needed.

6.3.5   Refference Volatges

Reference voltages for SAR ADC are generated by an on-chip band gap. A resistive divider provides the 300mV and the 600mV reference voltages for the comparator and the CDAC. Regerence voltages are followed by an analog buffer which features 4-bit trim with 4mV LSB for high and low trim after fabrication. This trim can affect the refference voltage up to -20mV/+20mV. Fig 6.6 shows the top level schematic of the SAR ADC. Datails on analog buffer with tuning feature is shown in Fig 6.7. R1-R8 have different values of . The comparator low voltage refference and the reference voltage for the DAC are both 300mV. In order to separate the noise path of these two refference voltages two separate analog buffers are used. The test chip can use an on-chip clock of 2MHz and an external clock which can be selected through a multiplexer as it is shown in Fig 6.6. Each clock path has its own buffer. Low voltage buffers of reference voltages also has separate supply rail (Bufrail) which is provided with the test chip externally.

6.3.6   Summary

This chapter presented the details on designing a 7-bit low power SAR ADC in circuit level. Analog and digital blocks of this SAR ADC were discussed. Dynamic comparator design, DAC capacitor network and switching logic network were explained.
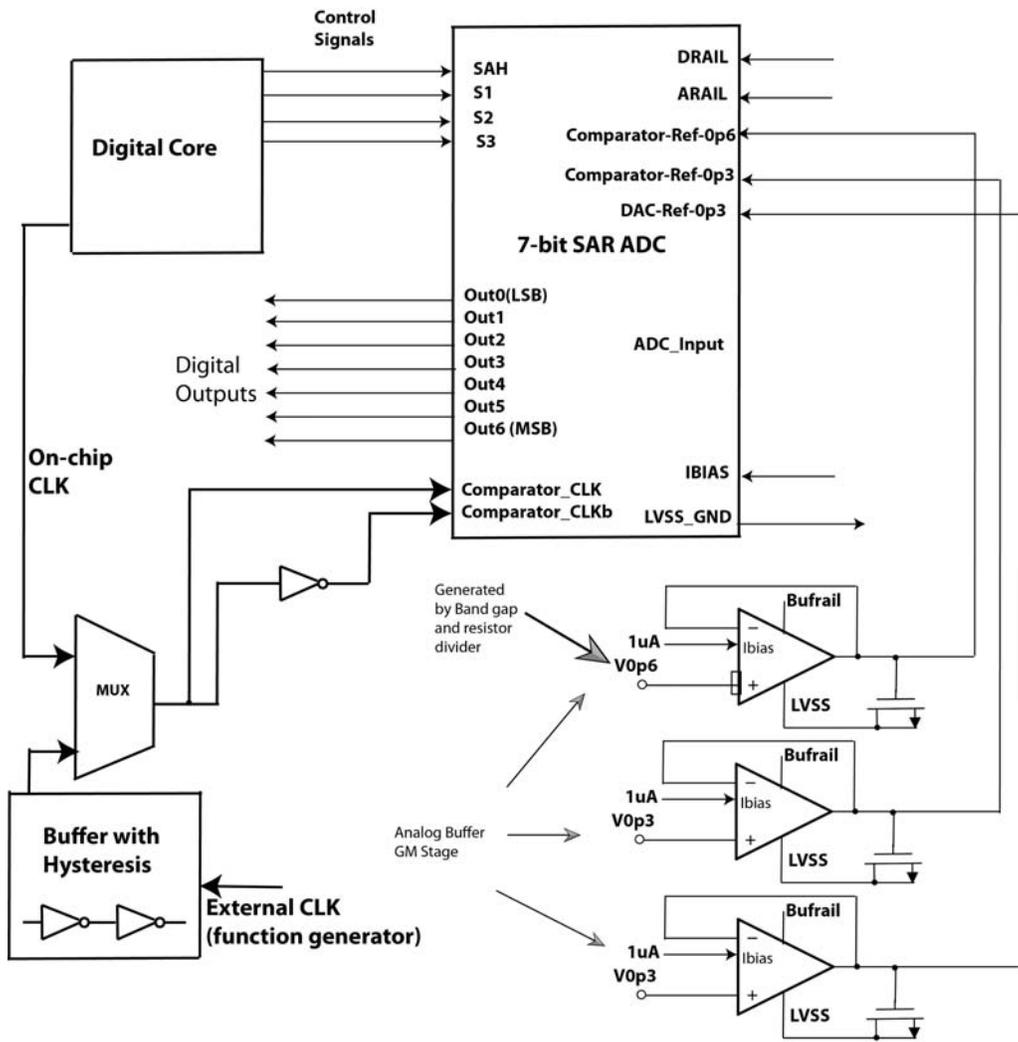
Figure 6.6: Top level schematic of SAR ADC design

VDD

MP3
1um/5um

MP4
1um/5um

Ibias
1uA

V_{inp}

2.5um/1.5um

MP1
2.5um/1.5um

MP2

V_{inn}

MN3
3um/3um

MN1

MN2

MN4
3um/3um

3um/3um

3um/3um

R2

R1

R1

R2

R4

R3

R3

R4

R6

R5

R5

R6

R8

R7

R7

R8

74VSS
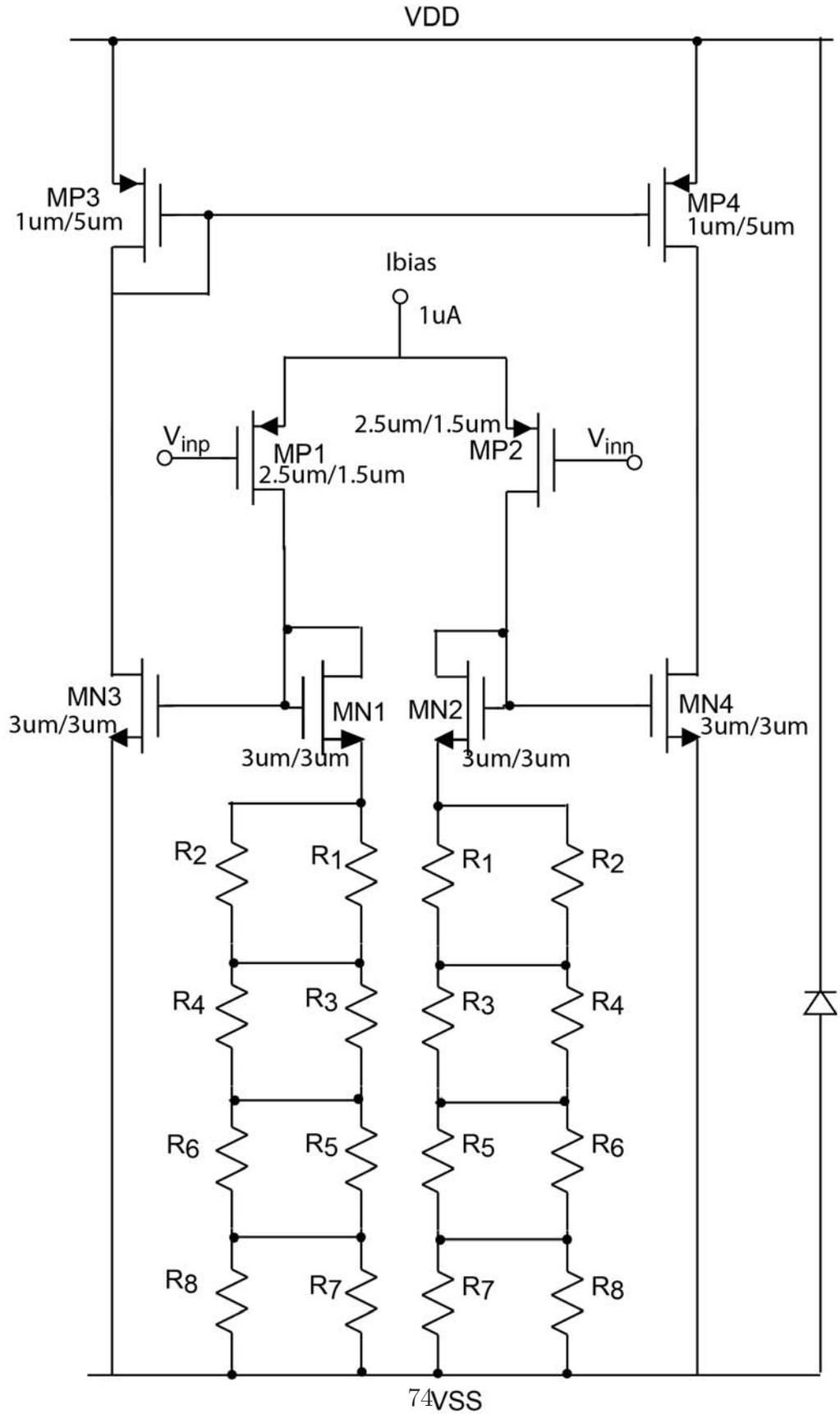
Figure 6.7: Analog buffer with tuning

Chapter 7

SAR ADC Testing and Analysis

A 7-bit 100kS/s SAR ADC has been designed using the proposed algorithm in 6.1, and simulated in $0.35\mu m$ CMOS-DMOS technology with Pyxis Mentor Graphic. Fig 7.1 shows the layout for this SAR ADC for analog blocks, including buffers, switches, DAC and comparator. Clock and logic block are not included in this figure. The analog part of the SAR ADC occupies 150μm$\times$ 105μm. The test chip has been fabricated as an internship project at ON Semicondctor. The bare dies are wire bonded in house at ON Semiconductor East Greenwich, RI into SOIC 28w package. The I/O pads for ADC digital output were small (76μm $\times$ 76μ m with minimum space 90 μm center-to-center of the pad. Therefore some of the digital outputs (SAH for monitoring, Out0(LSB), out2, out3, out5, out6 (MSB)) are measured by probe needles. 6 probe needles used simultaneously to measure these outputs. The output of the probe needles met the 50Ω matching resistors and the digital outputs were measured on the other side of the resitors using a rainbow digital cable and a header. Logic Analyzer inside a Lecroy Osciloscope was used for observing the analog and digital signals at the same time. Fig 7.2 shows the bonding diagram for this test chip.

An onchip 2-V supply has been used for the CDAC and switching logic network (DRAIL) while a separate on-chip 2V supply has been provided with the dynamic comparator (ARAIL). The 2V supply for both analog and digital blocks comes from a power block on-chip. The ADC input range in this case was 600mV (An input from 300mV to 900mV) but this is not a limitation; the architecture can be modified for other supply and input range combinations while preserving most of the power saving advantages.

Table 7.1 shows the ADC parameters and simulation results for this SAR ADC design.

PARAMETER	VALUE	UNITS
Resolution	7	bits
Sampling Rate	100	KS/s
Input Range	600	mV pk-pk
Supply Voltage		
DAC, Decoder, Logic	2.0	V
Comparator	2.0	V
Supply Current		
(excludes reference buffers)		
2.0V Supply	1.66	μA
2.0V Supply	0.69	μA
Power Consumption	4.7	μ W
Sampling Capacitance	4.0	pF

Table 7.1: System Simulation Results
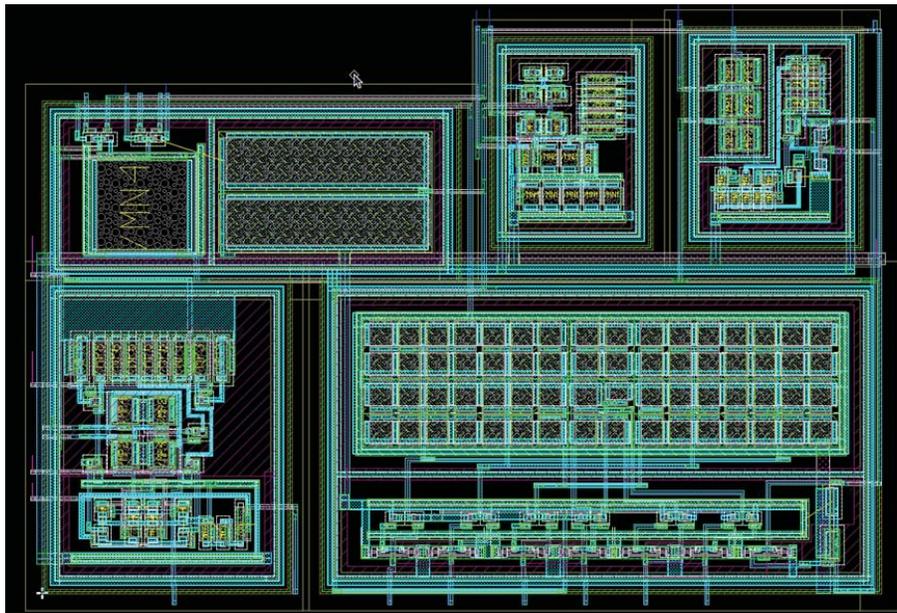
Figure 7.1: Analog portion of SAR ADC layout, including buffers, switches, DAC and comparator

7.1 PCB Design

Two layers printed circuit board with a ground plane on top, as an interface between the dies and test equipment has been designed. Linear regulator with low dropout voltage from linear technology [95] is used to create clean power supply for on-chip buffers (BufRAIL). A 3-pin jumper is placed on the board that allows
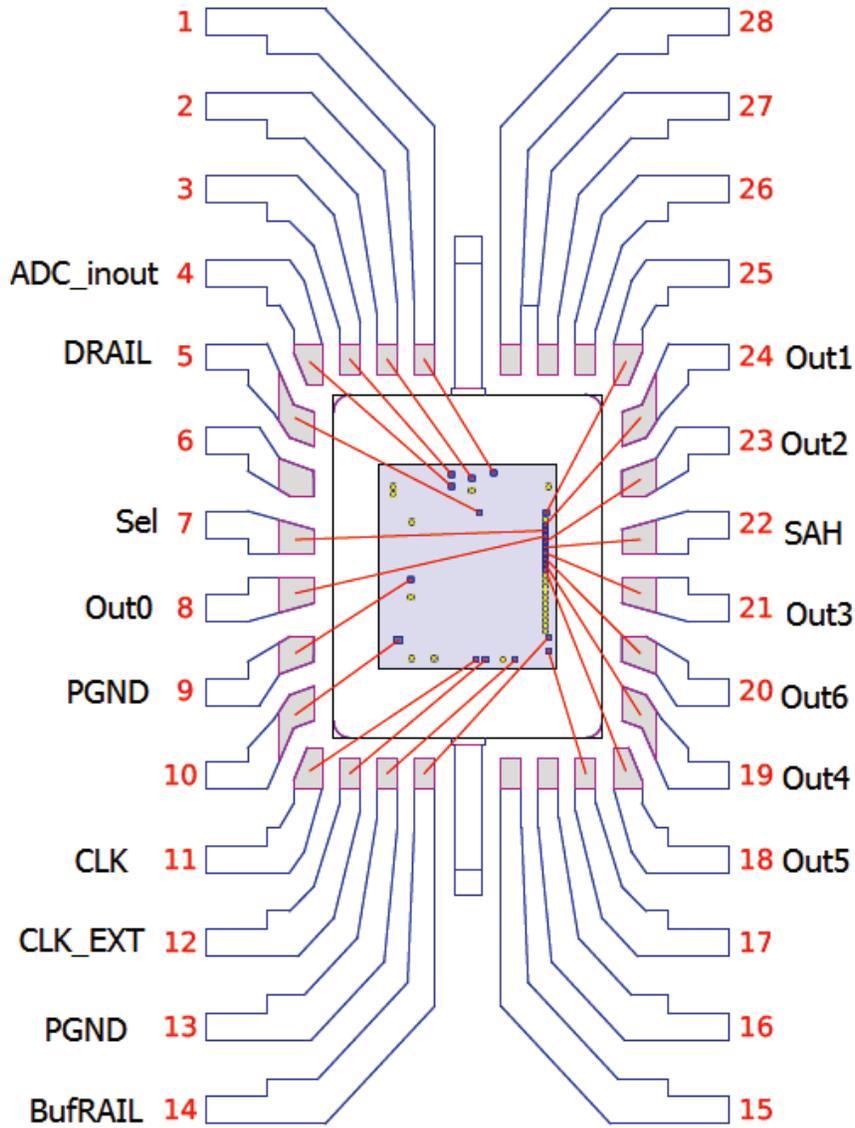
Figure 7.2: SAR ADC bonding diagram

selection between the regulated voltage and direct voltage from power supply. A decoupling capacitor is also placed on the middle pin of the jumper which goes into the related pin on chip. ADC input and external clock are provided through SMA connectors which have 50Ω matching resistors. Fig 7.3 shows the SAR ADC evaluation board and the Cadence schematic for this PCB design respectively.
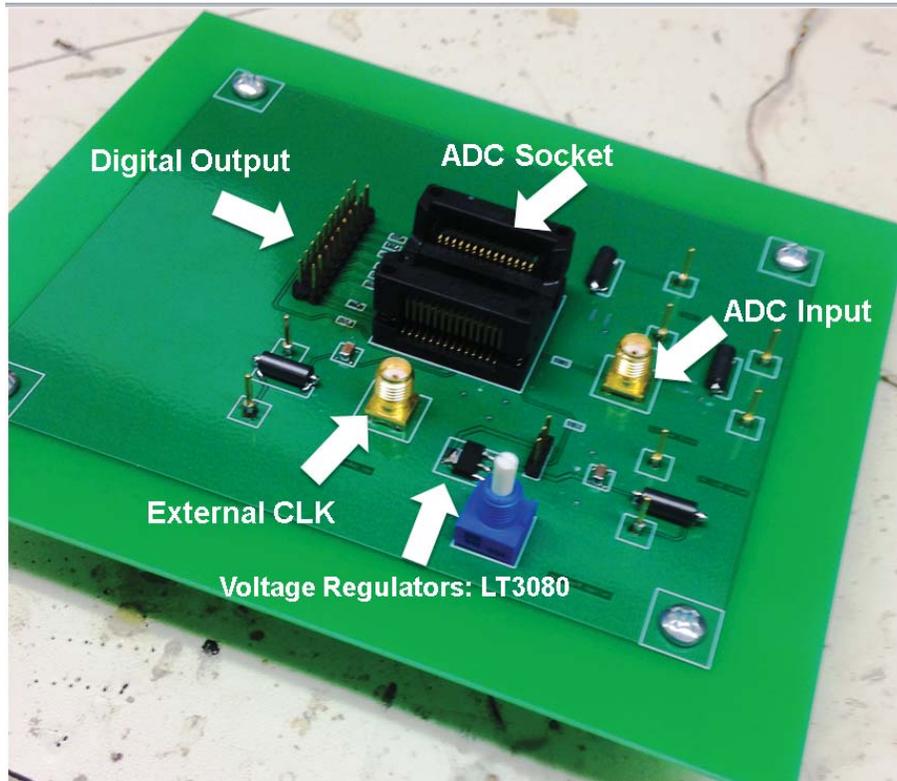
Figure 7.3: Measure DNL and INL for Die1

7.2 Static Performance

In order to measure the static performance of SAR ADC, a slow ramp (2048 μs ramp) was applied to SAR ADC and the linearity is tested 1000 times with 2 hits per code histogram. For this 7-bit 100kS/s SAR ADC, each conversion takes 8 clock cycles which is equal to 8μs. For 128 possible codes at least a 1024 μs ramp is needed. Two separate parts were tested with similar inputs. The results are shown in Fig 7.4 and 7.5. The peak DNL and INL are 0.88/-0.99 LSB and 2/-1.5 LSB for ADC1 and 0.9/-0.99 LSB and 1.6/-2 LSB for ADC2 respectively.

Static performance analysis of this SAR ADC shows the middle code 64 is the missing code. The refference voltages (300mV,600 mV) to ADC was measured through probing the test points on the chip and the tuning resistors in $GM - C$ buffers that is explianed in 6.3.5 were used to trim the reference voltages through a laser microscope. The average measured reference voltages after the tuning were 299V and 600.2V respictively. A clibration is needed to improve the linearity of this ADC. However since this SAR ADC is used in a feedback loop of a switching mode regulator, only one missing code will not cause any problem for this specific application.
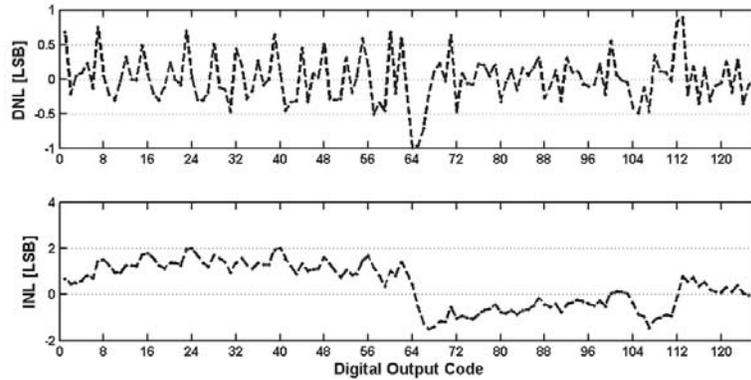
Figure 7.4: Measured DNL and INL with ramp input for Die1
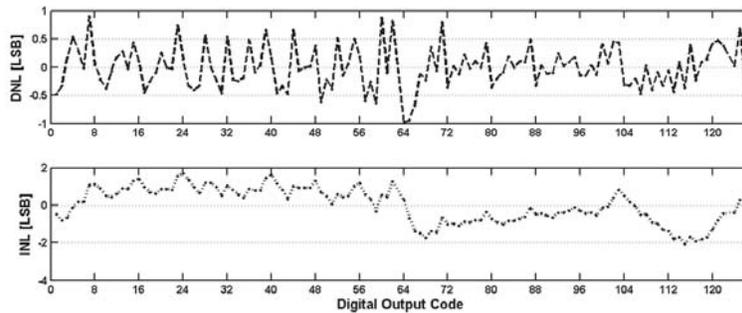
Figure 7.5: Measured DNL and INL with ramp input for Die2

7.3 Dynamic Performance

Fig 7.6 show the measured FFT spectrum with input frequency of close to 40kHz at a 2.0-V supply and a 100kS/sampling rate. The measured effective number of bits is 6.49 at low frequencies. The measured peak SNR due to quantization noise (SNQR) is 40.87dB. Since needle probes are source of collecting the noise, peak SNDR of 27.9dB was measured. A proper wire bonding of all digital outputs can improve the SNDR.

Total power consumption for this SAR ADC excluding the reference buffers is 4.7 μW, which is a 73% power reduction compared to an SAR ADC with conventional switching. Table 7.2summerizes the performance analysis for the SAR test chip. Walden FOM for this SAR ADC is 11.9 fJ/conversion-step.

7.4 summary

In this chapter the evaluation of SAR ADC and measurement results were presented. Measurement result shows the SAR ADC1 has a peak DNL of 0.88 /-0.99 and peak INL of 0.6/-1LSB. The SAR ADC2 has a peak DNL of 0.9 /-0.99 and peak
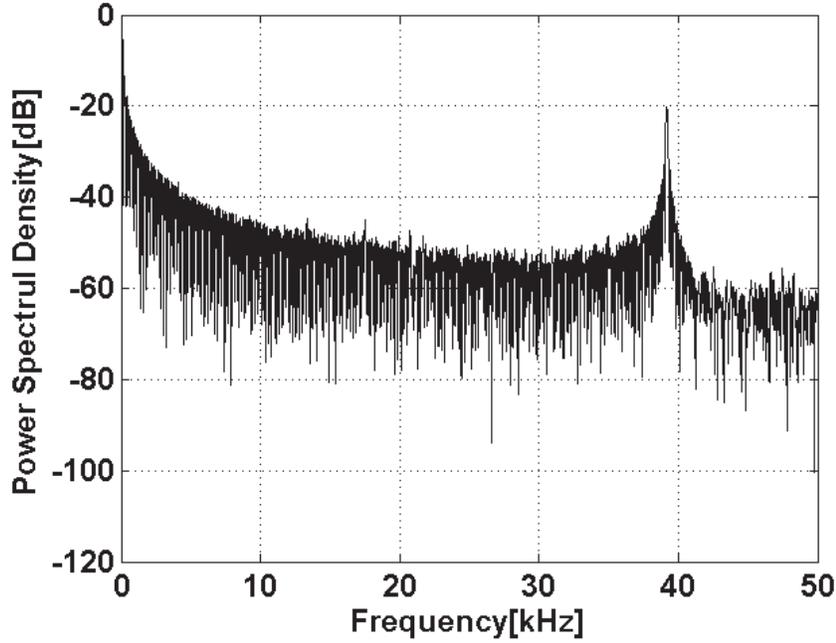
Figure 7.6: Measured 4096-point FFT spectrum at 100 kS/s.

Specification	[63]	[103]	[104]	This Work
Technology(mum)	0.13	0.13	0.18	0.35BCD
Supply Voltage(V)	1.2	1.2	1.0	2.0
Resolution(bit)	10	10	12	7
Sampling Rate (fs) kS/s	50000	1000	200(100)	100
Input frequency fin (KHz)	500	101	100(50)	1
ENOB (bits @ fin)	9.18	8.39	7.96(10.55)	6.49
FOM (fJ/conversion-step)	29	437	381(166)	11.9
Power Consumption (μW)	826	150	19(25)	5.61

Table 7.2: SAR ADC performance analysis

INL of 1.6/-2 LSB. The measured effective number of bits of 6.49 at low frequencies and the peak SNR due to quantization noise (SNQR) of 40.87dB was reported. The proposed algorithm has 73% power reduction compared to an SAR ADC with conventional switching. Although this SAR ADC suffers from a missing code in the middle, it will not make any issue for the application that this ADC is used.

Chapter 8

Conculsions

All digital background calibration of a 7-bit redundant flash ADC suitable for aggressively scaled CMOS technologies was presented and an ultra-low power single ended SAR ADC with a new conversion method was proposed in this dissertation.Chapter 2 provided a detailed background on flash ADC, SAR ADC and Split ADC architectures and previous calibration techniques.

Chapter 3 presented the details on digital background calibration of flash ADC and demonstrated the algorithm in behavioral simulation based on extracted IC layout in 180nm CMOS. The details on circuit level flash ADC deisgn were described in chapter 4 and simulation resluts, test and evaluation of flash ADC were demonstrated in chapter5.

The new DAC switching algorithm for SAR ADC was explained in chapter 6. The new architecture allows the ADC to perform the MSB decision without using the DAC resulting in significant power and area savings. The work presented in chapter 6 was implemented in an IC fabricated in 350nm CMOS DMOS technology sponsored by ON Semiconductor. Measurement results from tesing the SAR test chip were provided in chapter 7.

8.1   Future Work

All digital background calibration of split redundant flash ADC can be extended to use for an time interleaved flash ADC for a better speed and resolution. The algorithm can be applied to smaller technologies to achieve better performance.

The new DAC swithcing algorithm that is proposed for SAR ADC design can be more effective if the comparator offset is calibrated with auto zeroing techniques and a common centroid technique is used for capacitive DAC layout.

Appendix A

Glossary

A.1   Acronym

FS	Full Scale
HDL	Hardware Description Language
IC	Integrated Circuit
LMS	Least Mean Squares
LSB	Least Significant Bit
LUT	Lookup Table
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NMOS	N-Channel Metal Oxide Semiconductor
PMOS	P-Channel Metal Oxide Semiconductor
PRN	Pseudo Random Number
RMS	Root Mean Square
SAR	Successive Approximation Register
SNDR	Signal to Noise and Distortion Ratio

A.2 Flash ADC decoder design,verilog code

```verilog
module CLA_4bit(
    output [3:0] S,
    output Cout,//PG,GG,
    input [3:0] A,B,
    input Cin
    );
    wire [3:0] G,P,C;
    assign G = A & B; //Generate
    assign P = A ^ B; //Propagate
    assign C[0] = Cin;
    assign C[1] = G[0] | (P[0] & C[0]);
    assign C[2] = G[1] | (P[1] & G[0]) | (P[1] & P[0] & C[0]);
    assign C[3] = G[2] | (P[2] & G[1]) | (P[2] & P[1] & G[0]) |
        (P[2] & P[1] & P[0] & C[0]);
    assign Cout = G[3] | (P[3] & G[2]) | (P[3] & P[2] & G[1]) | (P[3]
    & P[2] & P[1] & G[0]) |(P[3] & P[2] & P[1] & P[0] & C[0]);
    assign S = P ^ C;
        // assign PG = P[3] & P[2] & P[1] & P[0];
    //assign GG = G[3] | (P[3] & G[2]) | (P[3] & P[2] & G[1]) | (P[3]
    & P[2] & P[1] & G[0]);
endmodule
```

```verilog
module CLA_5bit(
    output [4:0] S,
    output Cout,
    input [4:0] A,B,
    input Cin
    );
    wire [4:0] G,P,C;
    assign G = A & B; //Generate
    assign P = A ^ B; //Propagate
    assign C[0] = Cin;
    assign C[1] = G[0] | (P[0] & C[0]);
    assign C[2] = G[1] | (P[1] & G[0]) | (P[1] & P[0] & C[0]);
    assign C[3] = G[2] | (P[2] & G[1]) | (P[2] & P[1] & G[0]) | (P[2]
    & P[1] & P[0] & C[0]);
    assign C[4] = G[3] | (P[3] & G[2]) | (P[3] & P[2] & G[1]) | (P[3]
    & P[2] & P[1] & G[0]) | (P[3] & P[2] & P[1] & P[0] & C[0]);
    assign Cout = G[4] | (P[4] & G[3]) | (P[4] & P[3] & G[2]) | (P[4]
    & P[3] & P[2] & G[1]) |(P[4] & P[3] & P[2] & P[1] & G[0])| (P[4] &
    P[3] & P[2] & P[1]& P[0] & C[0]);
  assign S = P ^ C;
//assign PG = P[4] & P[3] & P[2] & P[1] & P[0];
//assign GG = G[4] | (P[4] & G[3]) | (P[4] & P[3] & G[2]) | (P[4] &
    P[3] & P[2] & G[1]) |(P[4] & P[3] & P[2] & P[1] & G[0]);
endmodule
```

```verilog
'timescale 1ns/1ps
module D_flipflop (d,clk,reset,q);
input d,reset,clk;
output q;
reg q;

always @(negedge clk) begin
   if (reset)
       q<=0;
else
q<=d;
end
endmodule
```

```verilog
'timescale 1ns/1ps
module D_flipflop6 (d,clk,reset,q);
input [5:0] d;
input clk,reset;
output [5:0] q;

//parameter delay1=0.1;

/////////1//////////////////

D_flipflop DUT2(d[5],clk,reset,q[5]);
D_flipflop DUT3(d[4],clk,reset,q[4]);
D_flipflop DUT4(d[3],clk,reset,q[3]);
D_flipflop DUT5(d[2],clk,reset,q[2]);
D_flipflop DUT6(d[1],clk,reset,q[1]);
D_flipflop DUT7(d[0],clk,reset,q[0]);


endmodule
```

```verilog
`timescale 1ns/100ps
module D_flipflop63 (d,clk,reset,q);
input [62:0] d;
input reset,clk;
output [62:0] q;
parameter delay1=1;



D_flipflop DUT62(d[62],clk,reset,q[62]);
D_flipflop DUT61(d[61],clk,reset,q[61]);
D_flipflop DUT60(d[60],clk,reset,q[60]);
D_flipflop DUT59(d[59],clk,reset,q[59]);
D_flipflop DUT58(d[58],clk,reset,q[58]);
D_flipflop DUT57(d[57],clk,reset,q[57]);


///////////////8//////////////////
D_flipflop DUT56(d[56],clk,reset,q[56]);
D_flipflop DUT55(d[55],clk,reset,q[55]);
D_flipflop DUT54(d[54],clk,reset,q[54]);
D_flipflop DUT53(d[53],clk,reset,q[53]);
D_flipflop DUT52(d[52],clk,reset,q[52]);
D_flipflop DUT51(d[51],clk,reset,q[51]);
D_flipflop DUT50(d[50],clk,reset,q[50]);
D_flipflop DUT49(d[49],clk,reset,q[49]);
D_flipflop DUT48(d[48],clk,reset,q[48]);
D_flipflop DUT47(d[47],clk,reset,q[47]);


///////////////9//////////////////
D_flipflop DUT46(d[46],clk,reset,q[46]);
D_flipflop DUT45(d[45],clk,reset,q[45]);
D_flipflop DUT44(d[44],clk,reset,q[44]);
D_flipflop DUT43(d[43],clk,reset,q[43]);
D_flipflop DUT42(d[42],clk,reset,q[42]);
D_flipflop DUT41(d[41],clk,reset,q[41]);
D_flipflop DUT40(d[40],clk,reset,q[40]);
D_flipflop DUT39(d[39],clk,reset,q[39]);
D_flipflop DUT38(d[38],clk,reset,q[38]);
D_flipflop DUT37(d[37],clk,reset,q[37]);


///////////////10//////////////////
D_flipflop DUT36(d[36],clk,reset,q[36]);
D_flipflop DUT35(d[35],clk,reset,q[35]);
D_flipflop DUT34(d[34],clk,reset,q[34]);
D_flipflop DUT33(d[33],clk,reset,q[33]);
D_flipflop DUT32(d[32],clk,reset,q[32]);
D_flipflop DUT31(d[31],clk,reset,q[31]);
D_flipflop DUT30(d[30],clk,reset,q[30]);
```

```verilog
52  D_flipflop DUT29(d[29],clk,reset,q[29]);
53  D_flipflop DUT28(d[28],clk,reset,q[28]);
54  D_flipflop DUT27(d[27],clk,reset,q[27]);
55
56
57  ///////////////11//////////////////
58  D_flipflop DUT26(d[26],clk,reset,q[26]);
59  D_flipflop DUT25(d[25],clk,reset,q[25]);
60  D_flipflop DUT24(d[24],clk,reset,q[24]);
61  D_flipflop DUT23(d[23],clk,reset,q[23]);
62  D_flipflop DUT22(d[22],clk,reset,q[22]);
63  D_flipflop DUT21(d[21],clk,reset,q[21]);
64  D_flipflop DUT20(d[20],clk,reset,q[20]);
65  D_flipflop DUT19(d[19],clk,reset,q[19]);
66  D_flipflop DUT18(d[18],clk,reset,q[18]);
67  D_flipflop DUT17(d[17],clk,reset,q[17]);
68
69
70  /////////////12//////////////////
71  D_flipflop DUT16(d[16],clk,reset,q[16]);
72  D_flipflop DUT15(d[15],clk,reset,q[15]);
73  D_flipflop DUT14(d[14],clk,reset,q[14]);
74  D_flipflop DUT13(d[13],clk,reset,q[13]);
75  D_flipflop DUT12(d[12],clk,reset,q[12]);
76  D_flipflop DUT11(d[11],clk,reset,q[11]);
77  D_flipflop DUT10(d[10],clk,reset,q[10]);
78  D_flipflop DUT9(d[9],clk,reset,q[9]);
79  D_flipflop DUT8(d[8],clk,reset,q[8]);
80  D_flipflop DUT7(d[7],clk,reset,q[7]);
81
82
83  /////////////13//////////////////
84
85  D_flipflop DUT6(d[6],clk,reset,q[6]);
86  D_flipflop DUT5(d[5],clk,reset,q[5]);
87  D_flipflop DUT4(d[4],clk,reset,q[4]);
88  D_flipflop DUT3(d[3],clk,reset,q[3]);
89  D_flipflop DUT2(d[2],clk,reset,q[2]);
90  D_flipflop DUT1(d[1],clk,reset,q[1]);
91  D_flipflop DUT0(d[0],clk,reset,q[0]);
92
93
94
95  /////////////////////////////////
96
97  endmodule
```

```verilog
`timescale 1ns/1ps
module DFF_encoder63(data,clk,reset,finalout);
input [62:0] data;
input clk,reset;
output [5:0] finalout;
wire [62:0]qout;
wire [5:0] wout;



D_flipflop63 DUT1(data,clk,reset,qout);

wallace_block3B DUT2(qout,wout);

D_flipflop6 DUT3(wout,clk,reset,finalout);


endmodule
```

```verilog
`timescale 1ns/1ps
module fulladder(a,b,c,sum,carry);
input a,b,c;
output sum,carry;
//wire sum,carry;

assign sum=a^b^c;       // sum bit
assign carry=((a&b) | (b&c) | (a&c));    //carry bit

endmodule
```

```verilog
`timescale 1ns/1ps
module wallace_block(d,out);
input [14:0] d;
output [3:0] out;
wire [1:0] w;
wire [7:0] z;
wire [7:0] s;
fulladder add1(z[0],z[4],d[14],out[0],w[0]);
fulladder add2(z[2],z[6],w[0],out[1],w[1]);
fulladder add3(z[3],z[7],w[1],out[2],out[3]);
/////////////////////////////////////////
//2nd block//
/////////////////////////////////////////
fulladder add4(s[0],s[2],d[13],z[0],z[1]);
fulladder add5(s[1],s[3],z[1],z[2],z[3]);
fulladder add6(s[4],s[6],d[6],z[4],z[5]);
fulladder add7(s[5],s[7],z[5],z[6],z[7]);
/////////////////////////////////////////
//3rd block//
/////////////////////////////////////////
fulladder add8(d[11],d[10],d[12],s[0],s[1]);
fulladder add9(d[8],d[7],d[9],s[2],s[3]);
fulladder add10(d[3],d[4],d[5],s[4],s[5]);
fulladder add11(d[1],d[0],d[2],s[6],s[7]);
endmodule
```

```verilog
`timescale 1ns/1ps
module wallace_block2B(d,out);
input [30:0] d;
output [4:0] out;
wire [3:0] t;
wire [3:0] y;
wallace_block b1(d[14:0],t[3:0]);
wallace_block b2(d[29:15],y[3:0]);
CLA_4bit u1(out[3:0],out[4],t,y,d[30]);
endmodule
```

```verilog
`timescale 1ns/1ps
module wallace_block3B(d,out);
input [62:0] d;
output [5:0] out;
wire [4:0] t;
wire [4:0] y;
wallace_block2B b1(d[30:0],t[4:0]);
wallace_block2B b2(d[61:31],y[4:0]);
//Carry_lookAheadadder_5bit u1(out[4:0],out[5],t,y,d[62]);
CLA_5bit u1(out[4:0],out[5],t,y,d[62]);
endmodule
```

A.3 Sampling jitter at different SNR and input frequency

```matlab
clc;
clear all;
SNR=[-66 -78 -90 -102];
dt=[1e6:5e5:1e8];
close ALL
axis([1e6 1e8 1e-14 1e-10])
hold on
for j=1:size(SNR,2);
    for i=1:size(dt,2)
        f(j,i)=10^(-SNR(j)/20)/(2*pi*dt(1,i));
    end
%   plot(dt,f(j,:))
end
```

A.4 Flash ADC, DNL/INL plot, MATLAB code

```matlab
clear;clc;
A=load('Flash_10_mat.csv');
B=size(A);
A_round=[A(:,1) fix(A(:,2)) fix(A(:,3)) fix(A(:,4)) fix(A(:,5))...
    fix(A(:,6)) fix(A(:,7))fix(A(:,8)) fix(A(:,9)) fix(A(:,10))...
    fix(A(:,11)) fix(A(:,12))];
A_round(:,13)=A_round(:,4)+2*A_round(:,5)+4*A_round(:,6)...
    +8*A_round(:,7)+16*A_round(:,8)+32*A_round(:,9)+64*A_round(:,10);
%plot(A_round(1:1500,1),A_round(1:1500,11))
j=0;
k=0;
n=2;
m=3;
for i=1:(size(A_round,1)-1)
    if and(A_round(i,11)>0,A_round(i+1,11)==0)
        j=j+1;
        if j==n
            k=k+1;
            C(k,:)=[i+1 A_round(i+1,13)];
        elseif j==(n+m)
            k=k+1;
            C(k,:)=[i+1 A_round(i+1,13)];
            m=m+3;
        end
    end
end
%
c_min=min(C(:,2));
c_max=max(C(:,2));
j=1;
for i=c_min:c_max
    if find(C(:,2)==i)
        d=size(find(C(:,2)==i),1);
        x1(j,:)=[i d];
        j=j+1;
    end
end
total_ave=sum(x1(:,2))/size(x1,1);
x3=[x1(:,1) x1(:,2)/total_ave];
dnl=x3(:,2)-1;
inl=cumsum(dnl);
createfigure(x1(:,1),dnl,inl)
```

A.5   SAR ADC, DNL/INL plot, MATLAB code

```matlab
clear ; clc ;
A=load ( ' clk −1MHz−ramp −511 die2 . csv ' ) ;
B=size (A,2) ;
A( : ,B+1)=A( : ,B−7)+A( : ,B−6)∗2+A( : ,B−5)∗4+A( : ,B−4) ∗ 8 . . .
+A( : ,B−3)∗16+A( : ,B−2)∗32+A( : ,B−1)∗64;
c_min=min(A( : ,1 0 ) ) ;
c_max=max(A( : ,1 0 ) ) ;
j =1;
for i=c_min : c_max
    if find (A( : ,B+1)==i )
        d=size ( find (A( : ,B+1)==i ) ,1) ;
        x1 ( j , : ) =[ i  d ] ;
        j=j +1;
    end
end
outlier =[0  63  123  127];
x2=x1 ;
k=0;
for i =1: size ( outlier ,2)
    x2 ( ( find ( x1 ( : ,1)==outlier (1 , i ) ) )−k , : ) =[];
    k=k+1;
end
total_ave=sum( x2 ( : ,2) ) / size ( x2 ,1) ;
x3 =[ x2 ( : ,1)  x2 ( : ,2) / total_ave ];
dnl=x3 ( : ,2) −1;
inl=cumsum( dnl ) ;
createfigure ( x2 ( : ,1) , dnl , inl )
```

A.6 SAR ADC, fft plot, SNR calculation MAT-LAB code

```
1  % ═══════════════════════════════════════════════════ %
2  %              Calculates SNR using N−point FFT              %
3  % ═══════════════════════════════════════════════════ %
4  clear ; clc ;
5  A=load ( ' clk1megsine1024 . csv ' ) ;
6  B=size (A, 2 ) ;
7  A( : ,B+1)=A( : ,B−7)+A( : ,B−6)∗2+A( : ,B−5)∗4+A( : ,B−4)∗8+A( : ,B−3)∗16 . . .
8  +A( : ,B−2)∗32+A( : ,B−1)∗64;
9  A( : , 1 1 )=(A( : , 1 0 ) /128)∗.6 −.3;
10 c_min=min (A( : , 1 1 ) ) ;
11 c_max=max(A( : , 1 1 ) ) ;
12 nump=size (A( : , 1 1 ) , 1 ) −111;                    % number of FFT points
13 %N =size (A( : , 1 1 ) , 1 ) −111;                    % number of FFT points
14 N=2^8;
15 fs   = 10e4 ;                      % sampling frequency
16 Ts   = 1/ fs ;
17 t    = 0: Ts : (N−1)∗Ts ;          % sampling time array
18 vout =[A( : , 1 )  A( : , 1 1 ) ] ;
19 vout ( 1:111 , : )=[] ;
20 % ─────── SNRcalculation ─────── %
21 vof    = abs ( ( fft ( vout ,N) ) ) /N;
22 vof    = vof /max( vof ) ;      % normalize the spectrum to full−scale
23 vof_db = db( vof ) ;
24 vofh   = vof (1:N/2) ;
25 [ vs , is ]= max( vofh ( 1:N/2) ) ;
26 Ps     = vs ^2;                    % fundamental signal power
27 Phar   = norm( vofh ( 2: is −1))^2 + norm( vofh ( is +1:N/2))^2; % total
            harmonic power
28 Pnoise = norm( vofh ( find (db( vofh ) <−55)))^2;   % −60 is  set based on the
            noise floor .
29 SQNR = 10∗log10 ( Ps /Pnoise )
30 SNDR = 10∗log10 ( Ps /Phar )
31 NPWR = 10∗log10 ( Phar ) ;
32 freq   = 0: fs /N: ( fs /2 − fs /N) ;
33 figure (2) , H = plot ( freq ∗1e−3, vof_db (1:N/2) , ' k−') ;
34 grid on ;
```

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