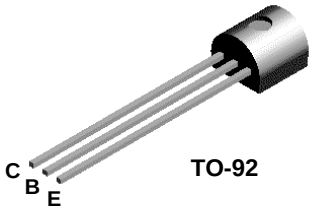
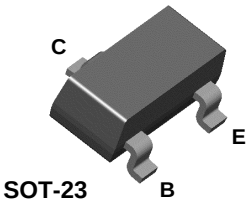
FAIRCHILD
SEMICONDUCTOR TM

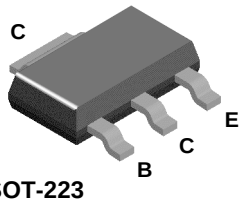
2N3904 MMBT3904 PZT3904



TO-92



SOT-23
Mark: 1A



SOT-223

NPN General Purpose Amplifier

This device is designed as a general purpose amplifier and switch. The useful dynamic range extends to 100 mA as a switch and to 100 MHz as an amplifier.

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	60	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

T_A = 25°C unless otherwise noted

Symbol	Characteristic	Max			Units
		2N3904	*MMBT3904	**PZT3904	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

**Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

NPN General Purpose Amplifier
(continued)

Electrical Characteristics
T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1.0 mA, I_B = 0	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	6.0		V
I_{BL}	Base Cutoff Current	V_{CE} = 30 V, V_{EB} = 3V		50	nA
I_{CEX}	Collector Cutoff Current	V_{CE} = 30 V, V_{EB} = 3V		50	nA
ON CHARACTERISTICS*					
h_{FE}	DC Current Gain	I_C = 0.1 mA, V_{CE} = 1.0 V I_C = 1.0 mA, V_{CE} = 1.0 V I_C = 10 mA, V_{CE} = 1.0 V I_C = 50 mA, V_{CE} = 1.0 V I_C = 100 mA, V_{CE} = 1.0 V	40 70 100 60 30	 300 	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA		0.2 0.3	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA	0.65	0.85 0.95	V V
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz	300		MHz
C_{obo}	Output Capacitance	V_{CB} = 5.0 V, I_E = 0, f = 1.0 MHz		4.0	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5 V, I_C = 0, f = 1.0 MHz		8.0	pF
NF	Noise Figure	I_C = 100 μA, V_{CE} = 5.0 V, R_S =1.0kΩ,f=10 Hz to 15.7kHz		5.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	V_{CC} = 3.0 V, V_{BE} = 0.5 V, I_C = 10 mA, I_{B1} = 1.0 mA		35	ns
t_r	Rise Time			35	ns
t_s	Storage Time	V_{CC} = 3.0 V, I_C = 10mA I_{B1} = I_{B2} = 1.0 mA		200	ns
t_f	Fall Time			50	ns

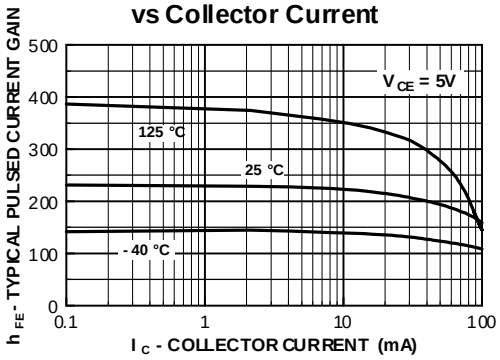
*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Spice Model

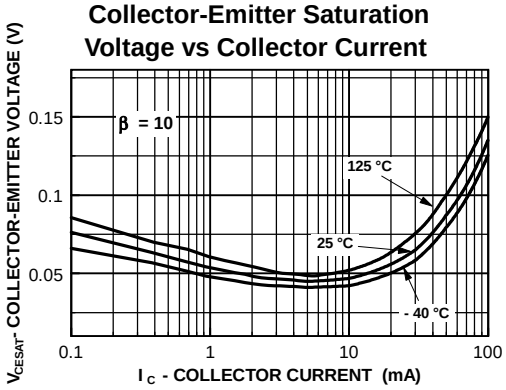
NPN (Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259 Ise=6.734 Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1 Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75 Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)

Typical Characteristics

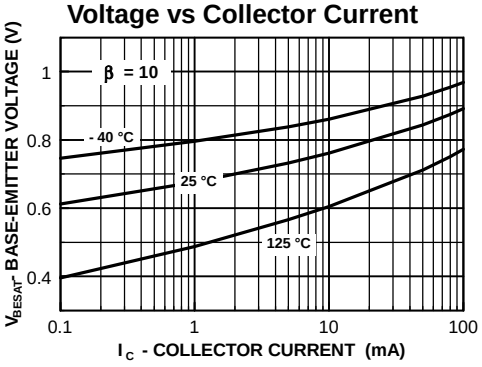
Typical Pulsed Current Gain vs Collector Current



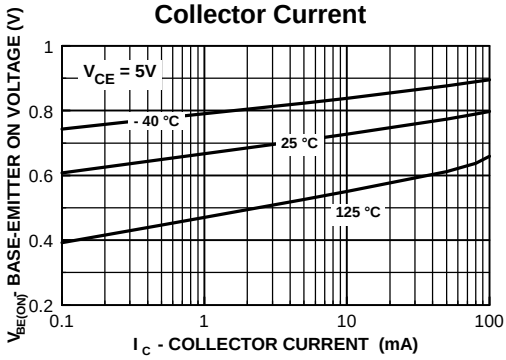
Collector-Emitter Saturation Voltage vs Collector Current



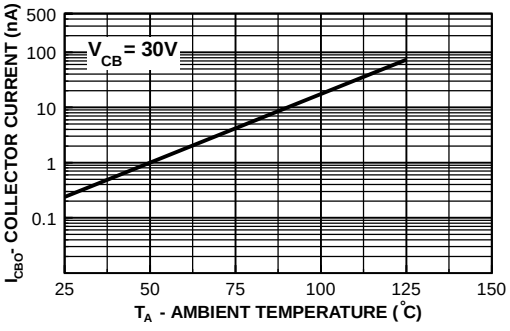
Base-Emitter Saturation Voltage vs Collector Current



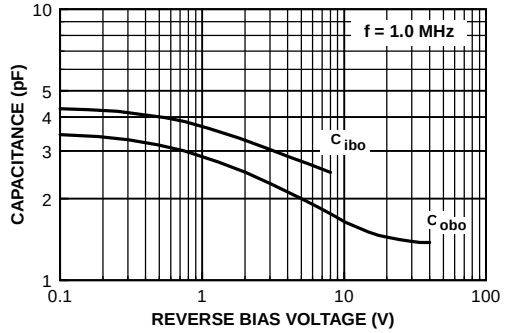
Base-Emitter ON Voltage vs Collector Current



Collector-Cutoff Current vs Ambient Temperature

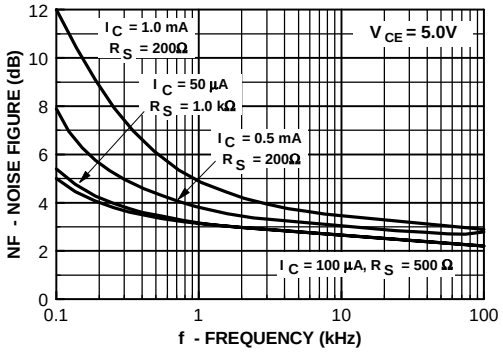


Capacitance vs Reverse Bias Voltage

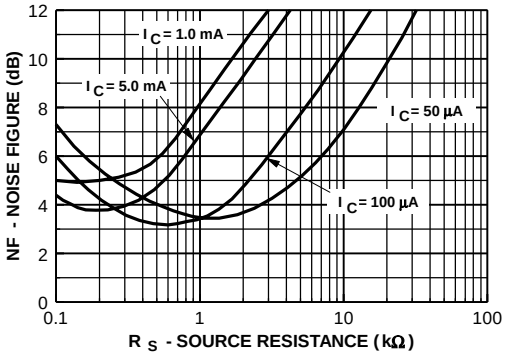


Typical Characteristics (continued)

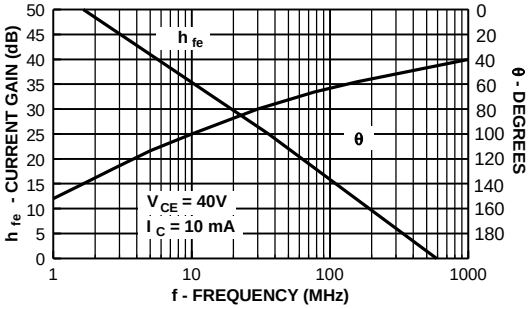
Noise Figure vs Frequency



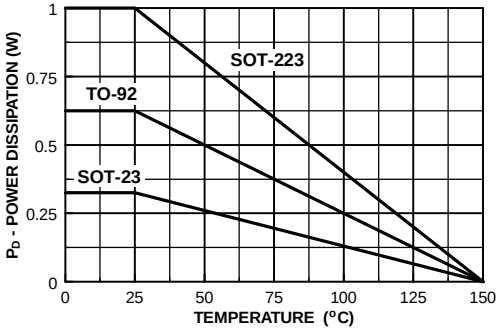
Noise Figure vs Source Resistance



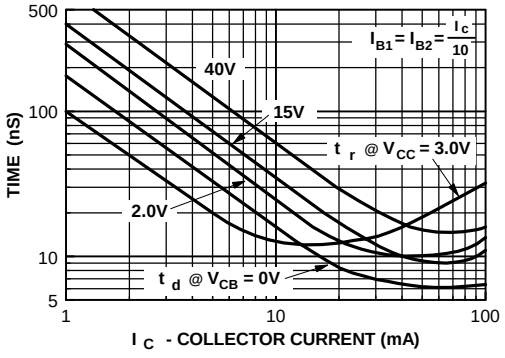
Current Gain and Phase Angle vs Frequency



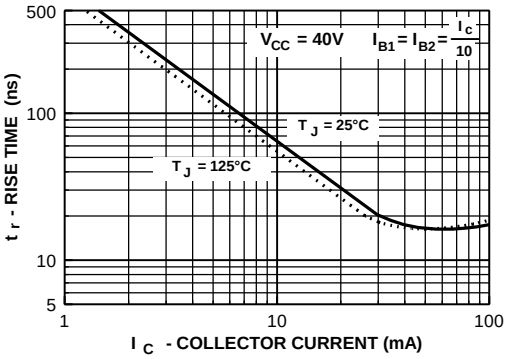
Power Dissipation vs Ambient Temperature



Turn-On Time vs Collector Current

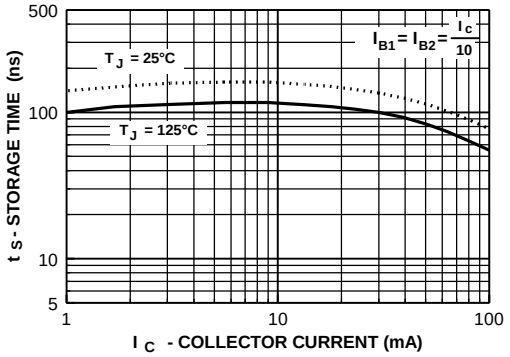


Rise Time vs Collector Current

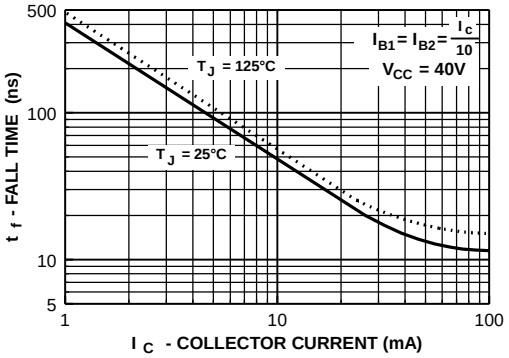


Typical Characteristics (continued)

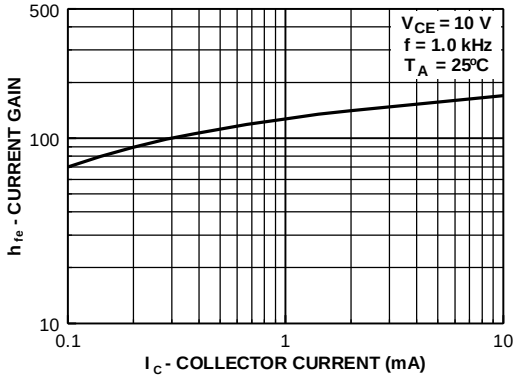
Storage Time vs Collector Current



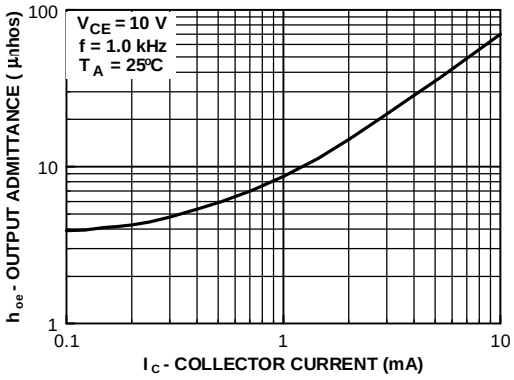
Fall Time vs Collector Current



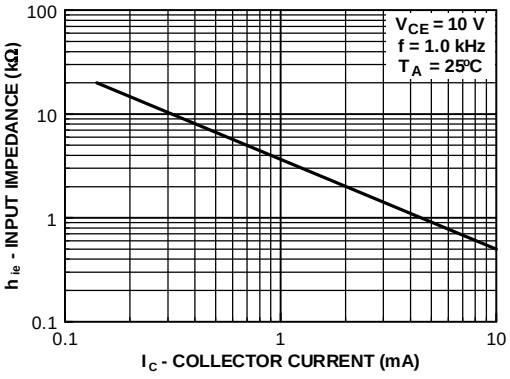
Current Gain



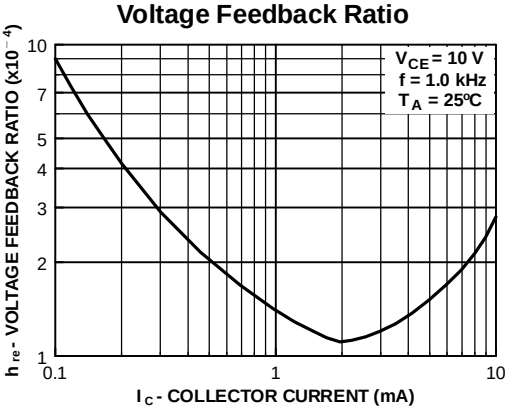
Output Admittance



Input Impedance



Voltage Feedback Ratio



Test Circuits

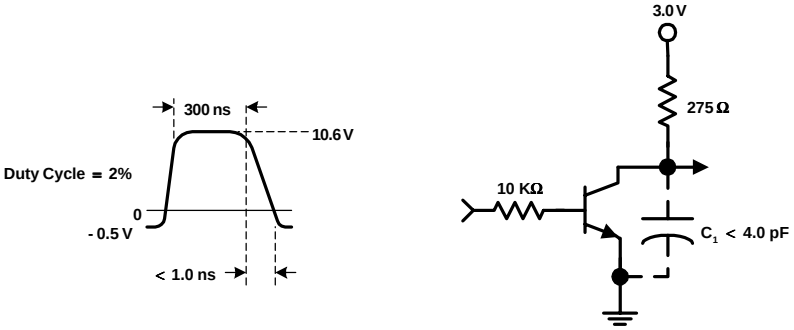


FIGURE 1: Delay and Rise Time Equivalent Test Circuit

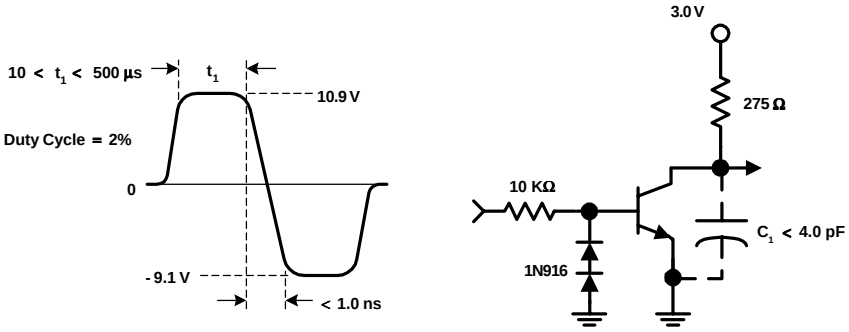


FIGURE 2: Storage and Fall Time Equivalent Test Circuit

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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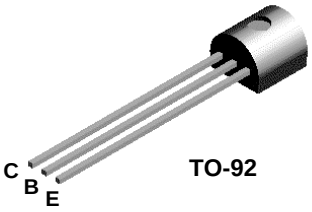
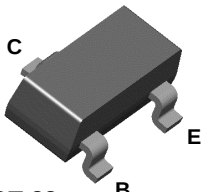
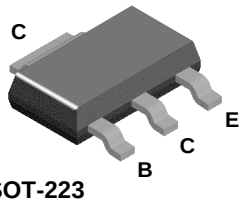
2N3906 MMBT3906 PZT3906



TO-92



SOT-23
Mark: 2A



SOT-223

PNP General Purpose Amplifier

This device is designed for general purpose amplifier and switching applications at collector currents of 10 μA to 100 mA.

Absolute Maximum Ratings* T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	40	V
V_{EBO}	Emitter-Base Voltage	5.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
3) All voltages (V) and currents (A) are negative polarity for PNP transistors.

Thermal Characteristics T_A = 25°C unless otherwise noted

Symbol	Characteristic	Max			Units
		2N3906	*MMBT3906	**PZT3906	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

**Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

PNP General Purpose Amplifier
(continued)

Electrical Characteristics
T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage*	I_C = 1.0 mA, I_B = 0	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 µA, I_E = 0	40		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 µA, I_C = 0	5.0		V
I_{BL}	Base Cutoff Current	V_{CE} = 30 V, V_{BE} = 3.0 V		50	nA
I_{CEX}	Collector Cutoff Current	V_{CE} = 30 V, V_{BE} = 3.0 V		50	nA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain *	I_C = 0.1 mA, V_{CE} = 1.0 V I_C = 1.0 mA, V_{CE} = 1.0 V I_C = 10 mA, V_{CE} = 1.0 V I_C = 50 mA, V_{CE} = 1.0 V I_C = 100 mA, V_{CE} = 1.0 V	60 80 100 60 30	300	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA		0.25 0.4	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA	0.65	0.85 0.95	V V
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz	250		MHz
C_{obo}	Output Capacitance	V_{CB} = 5.0 V, I_E = 0, f = 100 kHz		4.5	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5 V, I_C = 0, f = 100 kHz		10.0	pF
NF	Noise Figure	I_C = 100 µA, V_{CE} = 5.0 V, R_S =1.0kΩ,f=10 Hz to 15.7 kHz		4.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	V_{CC} = 3.0 V, V_{BE} = 0.5 V, I_C = 10 mA, I_{B1} = 1.0 mA		35	ns
t_r	Rise Time			35	ns
t_s	Storage Time	V_{CC} = 3.0 V, I_C = 10mA I_{B1} = I_{B2} = 1.0 mA		225	ns
t_f	Fall Time			75	ns

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

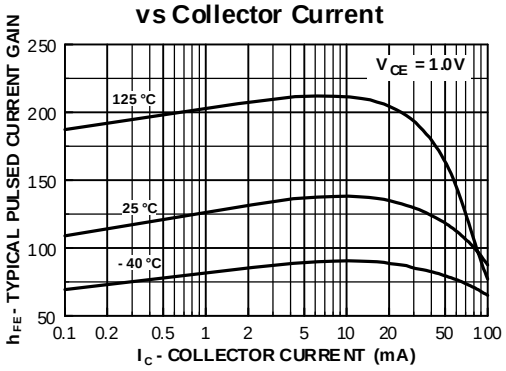
NOTE: All voltages (V) and currents (A) are negative polarity for PNP transistors.

Spice Model

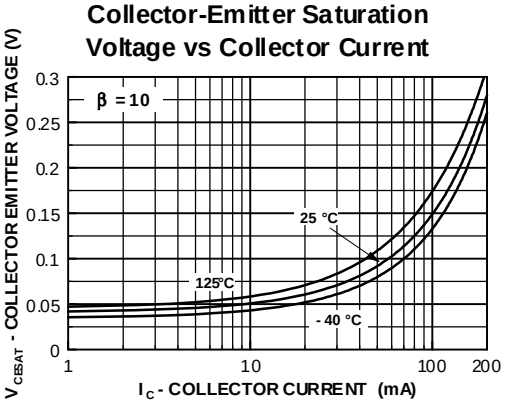
PNP (Is=1.41f Xti=3 Eg=1.11 Vaf=18.7 Bf=180.7 Ne=1.5 Ise=0 Ikf=80m Xtb=1.5 Br=4.977 Nc=2 Isc=0 Ikr=0 Rc=2.5 Cjc=9.728p Mjc=.5776 Vjc=.75 Fc=.5 Cje=8.063p Mje=.3677 Vje=.75 Tr=33.42n Tf=179.3p Itf=.4 Vtf=4 Xtf=6 Rb=10)

Typical Characteristics

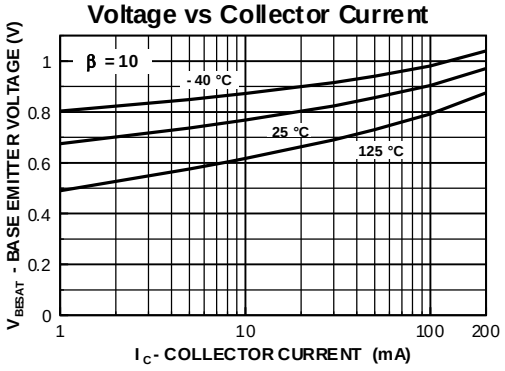
Typical Pulsed Current Gain vs Collector Current



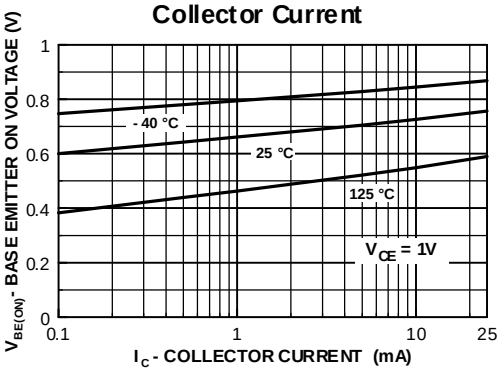
Collector-Emitter Saturation Voltage vs Collector Current



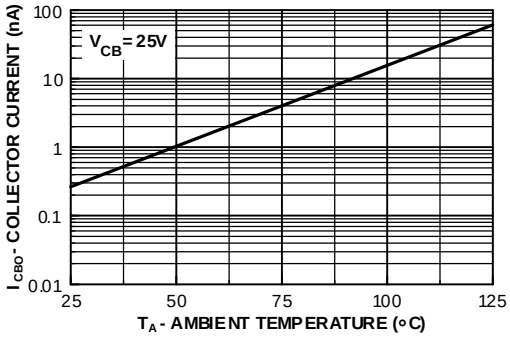
Base-Emitter Saturation Voltage vs Collector Current



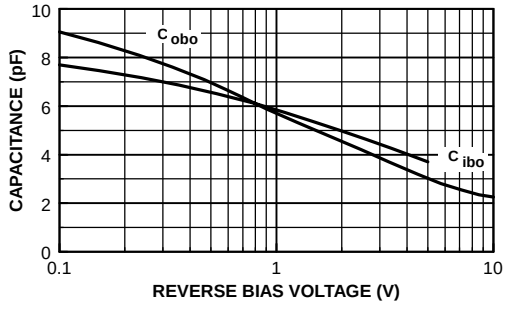
Base Emitter ON Voltage vs Collector Current



Collector-Cutoff Current vs Ambient Temperature

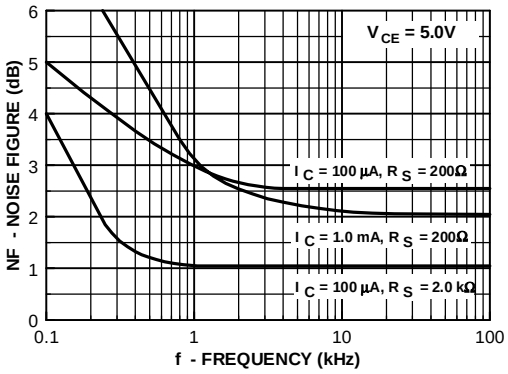


Common-Base Open Circuit Input and Output Capacitance vs Reverse Bias Voltage

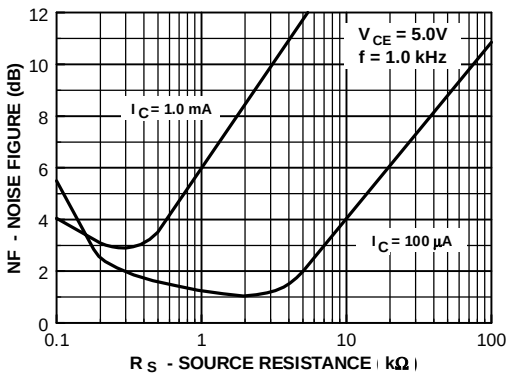


Typical Characteristics (continued)

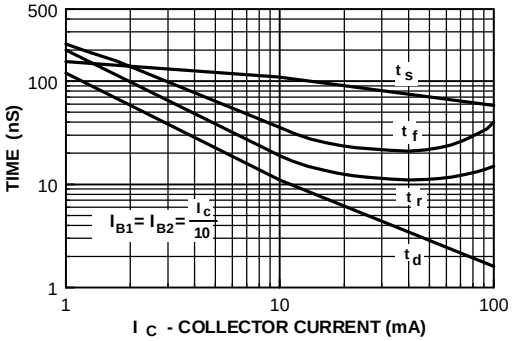
Noise Figure vs Frequency



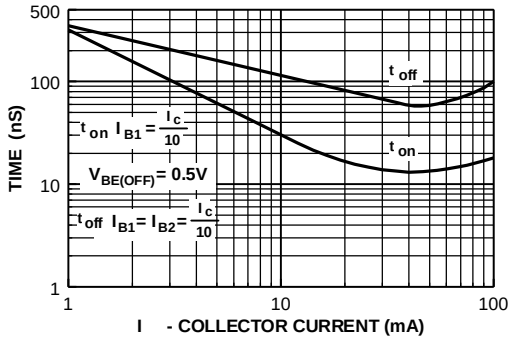
Noise Figure vs Source Resistance



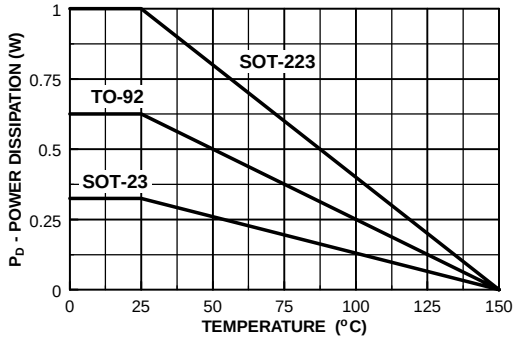
Switching Times vs Collector Current



Turn On and Turn Off Times vs Collector Current

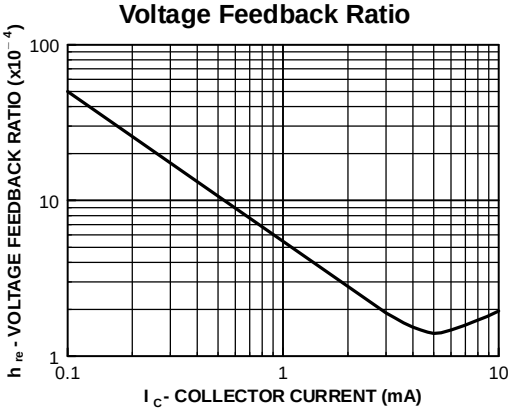


Power Dissipation vs Ambient Temperature

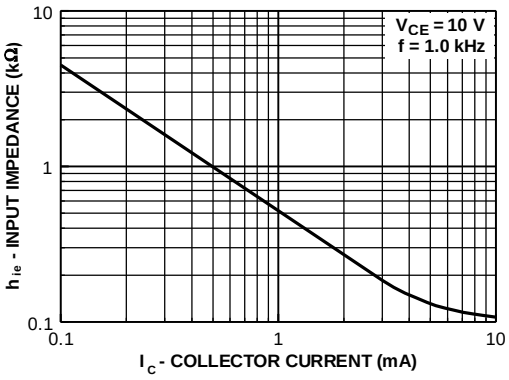


Typical Characteristics (continued)

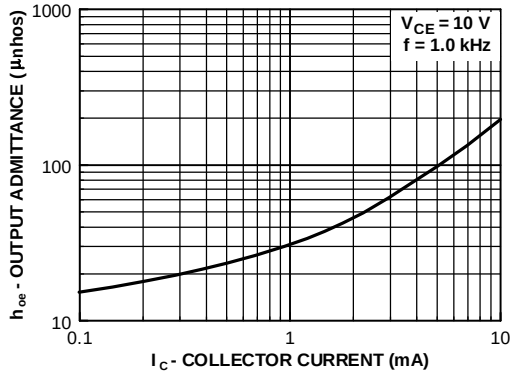
Voltage Feedback Ratio



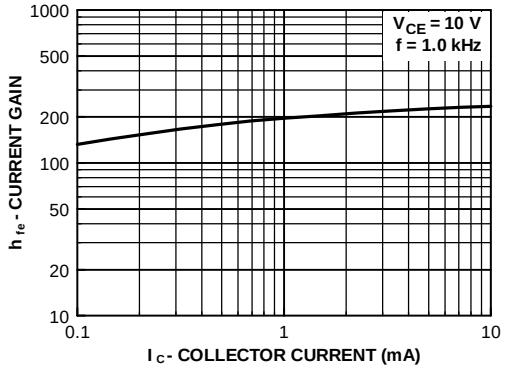
Input Impedance



Output Admittance



Current Gain



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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Part Number: 574502B00000G

Low cost labor saving slide on heat sink featuring spring action.
For use with TO-220 packages.

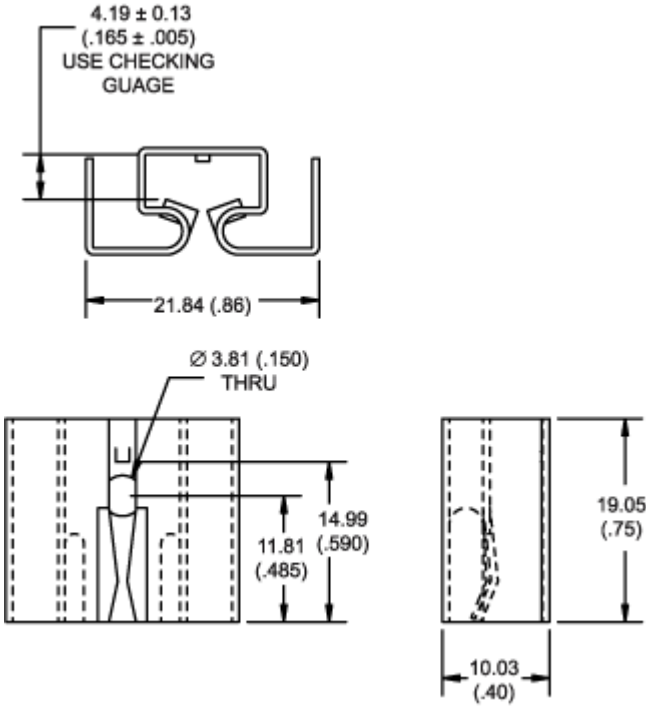
Order this part through
an Authorized Distributor
www.aavidthermalloy.com/sales
/disty.shtml

Product Information

This non-electronic component is functionally unaffected by the normal soldering or reflow processes used for semiconductor circuits. The heat resistance time or heat resistance temperature is not applicable for the component.

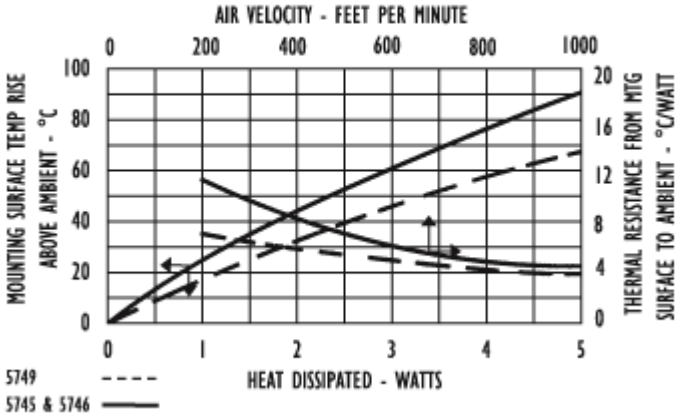
Part #	Finish	RoHS	PCN
574502B00000G	Black Anodize	RoHS ✓ Compliant	Product Change Notice

Mechanical Outline Drawing



Thermal Curve

Thermal	21.20



Resistance

Thermal resistance value is based on a 75°C rise in natural convection

Not Exactly what you need?

We offer several options for those applications which require a more unique solution. For slight modifications of this part or other attachment options, finishes, and interface materials, contact your sales associate. Challenge us with your thermal requirements - we can design custom solutions.

For technical help with our Standard Products,
please call (603) 224-9988, or contact your Aavid Sales Associate
Email: info@aavid.com

Visit us at www.aavidthermalloy.com •

HLMP-HG65, HLMP-HM65, HLMP-HB65

Precision Optical Performance Red Green and Blue
New 5mm Standard Oval LEDs

Data Sheet

Lead (Pb) Free
RoHS 6 fully
compliant

Description

These Precision Optical Performance Oval LEDs are specifically designed for full color/video and passenger information signs. The oval shaped radiation pattern and high luminous intensity ensure that these devices are excellent for wide field of view outdoor applications where a wide viewing angle and readability in sunlight are essential. The package epoxy contains both UV-A and UV-B inhibitors to reduce the effects of long term exposure to direct sunlight.

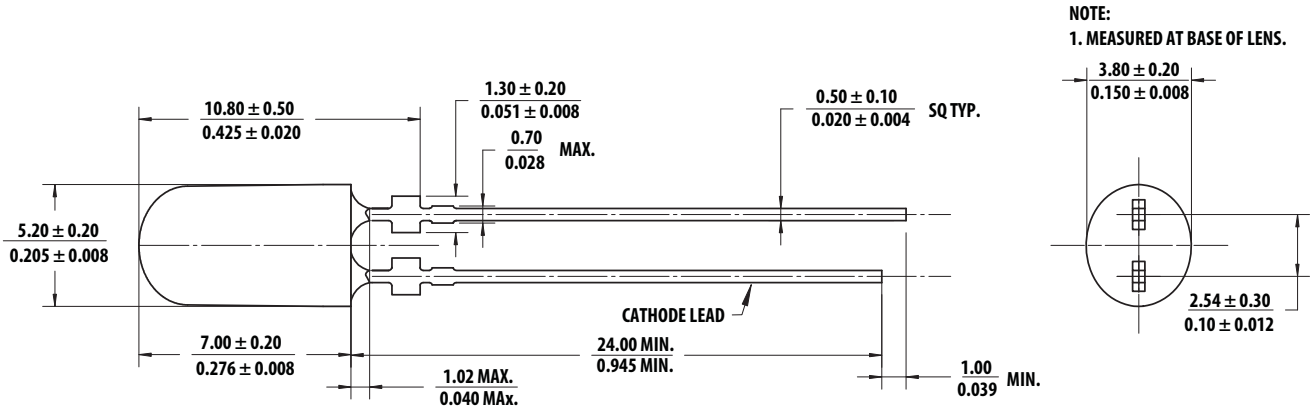
Applications

- Full color signs

Features

- Well defined spatial radiation pattern
- High brightness material
- Available in Red, Green and Blue color
  - Red AlInGaP 626 nm
  - Green InGaN 525nm
  - Blue InGaN 470nm
- Superior resistance to moisture
- Standoff Package
- Tinted and diffused
- Typical viewing angle 40° x 100°

Package Dimensions



Notes:
All dimensions in millimeters (inches).
Tolerance is ± 0.20mm unless other specified

***CAUTION**: INGaN devices are Class 1C HBM ESD sensitive per JEDEC Standard. Please observe appropriate precautions during handling and processing. Refer to Application Note AN – 1142 for additional details.*

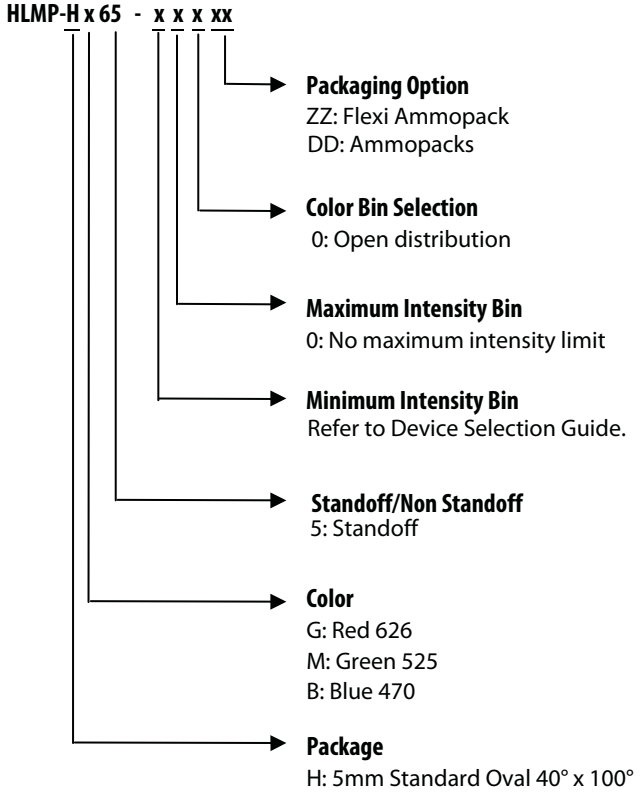
Device Selection Guide

Part Number	Color and Dominant Wavelength λd (nm) Typ	Luminous Intensity Iv (mcd) at 20 mA-Min [1]	Luminous Intensity Iv (mcd) at 20 mA-Max [1]
HLMP-HG65-VY0xx	Red 626	1150	2400
HLMP-HM65-Y30xx	Green 525	1990	5040
HLMP-HB65-QU0xx	Blue 470	460	1150

Tolerance for each intensity limit is ± 15%.

Notes:
1. The luminous intensity is measured on the mechanical axis of the lamp package and it is tested in pulsing condition.

Part Numbering System



Note:
Please refer to AB 5337 for complete information about part numbering system.

Absolute Maximum Ratings

$T_J = 25°C$

Parameter	Red	Green and Blue	Unit
DC Forward Current [1]	50	30	mA
Peak Forward Current	100 [2]	100 [3]	mA
Power Dissipation	120	116	mW
Reverse Voltage	5 (I_R = 100 µA)	5 (I_R = 10 µA)	V
LED Junction Temperature	130	110	°C
Operating Temperature Range	-40 to +100	-40 to +85	°C
Storage Temperature Range	-40 to +100	-40 to +100	°C

Notes:
1. Derate linearly as shown in Figure 4.
2. Duty Factor 30%, frequency 1KHz.
3. Duty Factor 10%, frequency 1KHz.

Electrical / Optical Characteristics

$T_J = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Forward Voltage	V_F				V	I_F = 20 mA
Red		1.8	2.1	2.4		
Green		2.8	3.2	3.8		
Blue		2.8	3.2	3.8		
Reverse Voltage	V_R				V	
Red		5				I_F = 100 µA
Green & blue		5				I_F = 10 µA
Dominant Wavelength [1]					nm	I_F = 20 mA
Red	λ_d	618	626	630		
Green		520	525	540		
Blue		460	470	480		
Peak Wavelength						
Red	λ_{PEAK}		634		nm	Peak of Wavelength of Spectral
Green			516			Distribution at I_F = 20 mA
Blue			464			
Thermal Resistance	$R\theta_{J-PIN}$		240		°C/W	LED Junction-to-Pin
Luminous Efficacy [2]						
Red	η_V		150		lm/W	Emitted Luminous Power/Emitted
Green			530			Radiant Power
Blue			65			

Notes:
1. The dominant wavelength is derived from the chromaticity Diagram and represents the color of the lamp
2. The radiant intensity, Ie in watts per steradian, may be found from the equation $I_e = I_V/\eta_V$ where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

AlInGaP Red

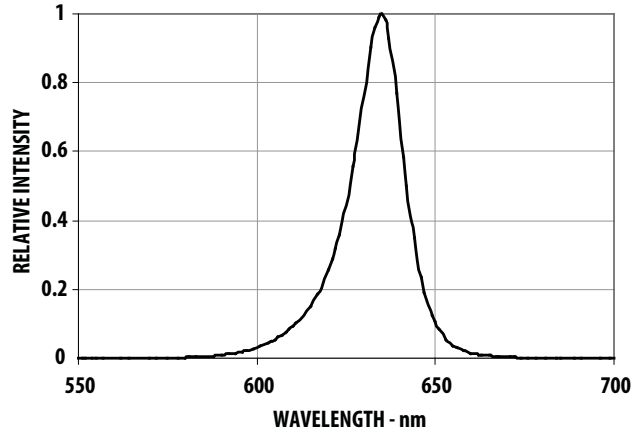


Figure 1. Relative Intensity vs Wavelength

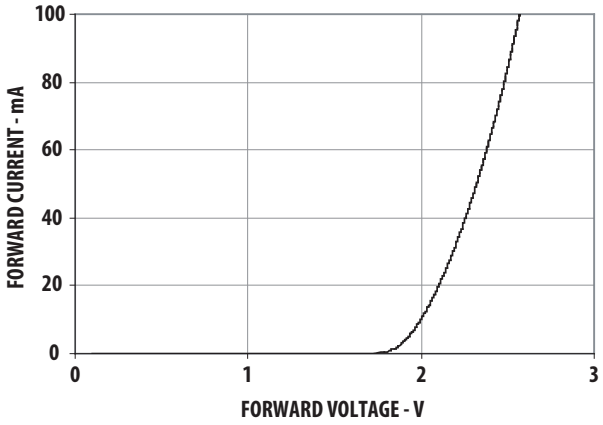


Figure 2. Forward Current vs Forward Voltage

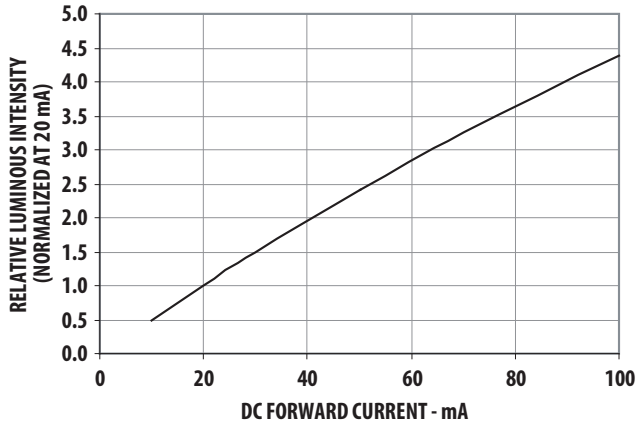


Figure 3. Relative Intensity vs Forward Current

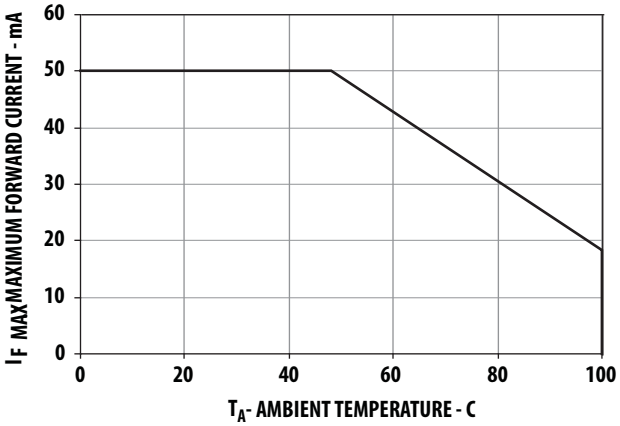


Figure 4. Maximum Forward Current vs Ambient Temperature

InGaN Blue and Green

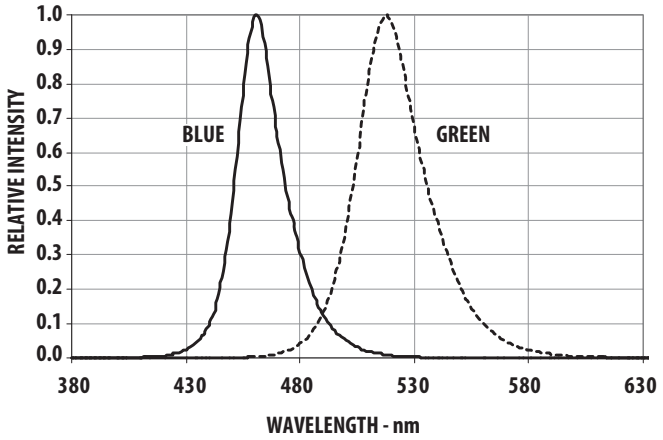


Figure 5. Relative Intensity vs Wavelength

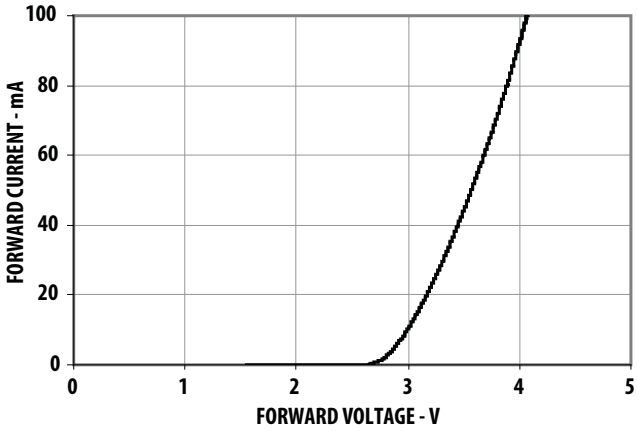


Figure 6. Forward Current vs Forward Voltage

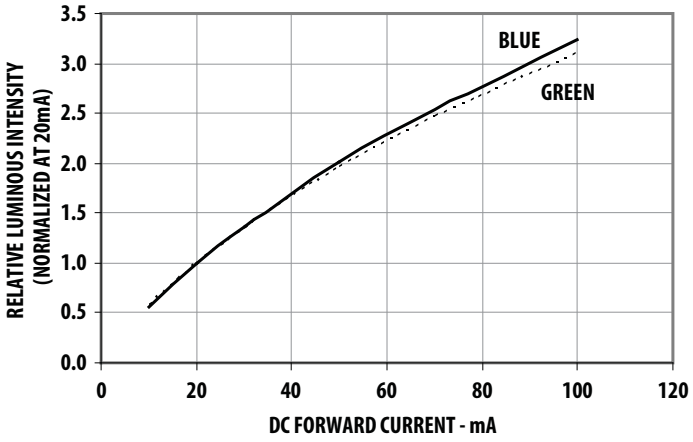


Figure 7. Relative Intensity vs Forward Current

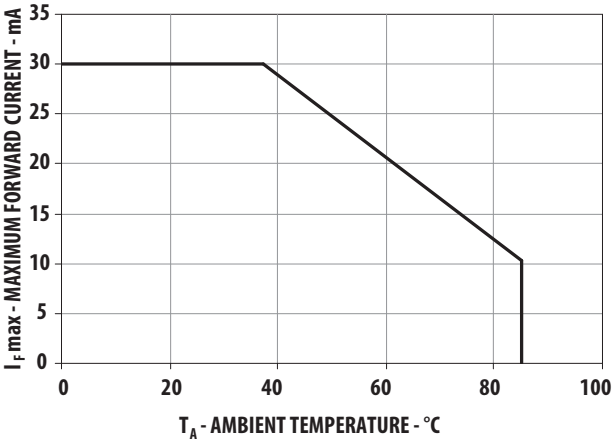


Figure 8. Maximum Forward Current vs Ambient Temperature

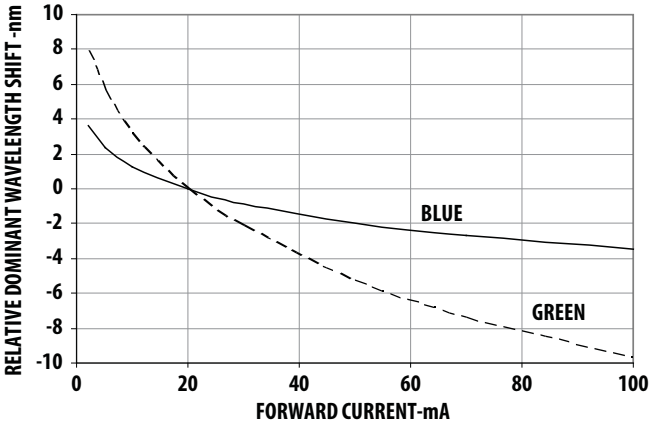


Figure 9. Relative dominant wavelength vs Forward Current

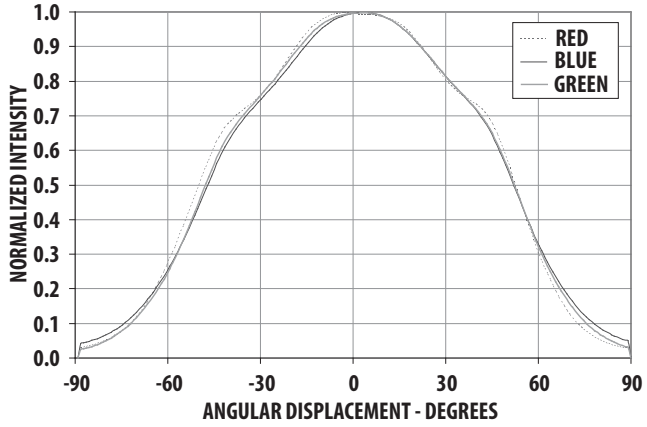


Figure 10. Radiation Pattern – Major Axis

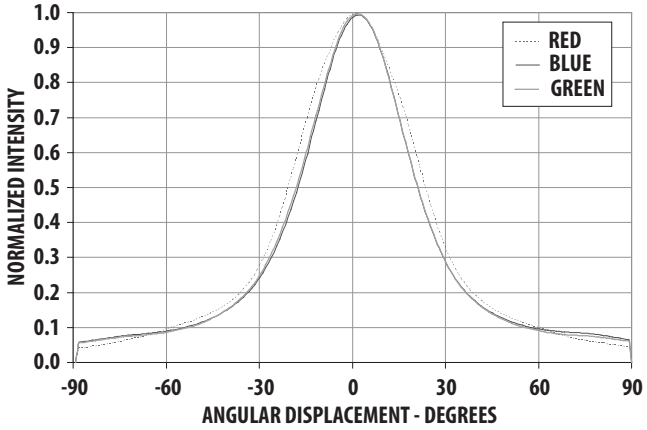


Figure 11. Radiation Pattern – Minor Axis

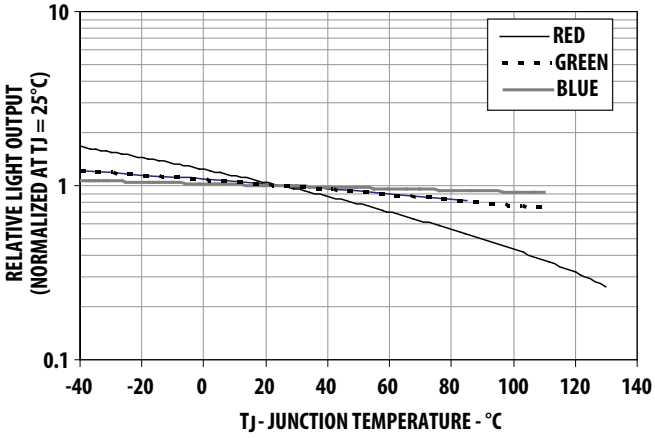


Figure12. Relative Light Output vs Junction Temperature

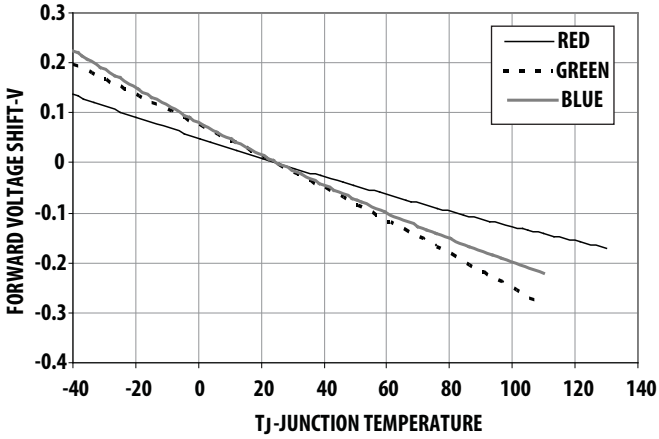


Figure 13. Relative Forward Voltage vs Junction Temperature

Intensity Bin Limit Table (1.2: 1 Iv Bin Ratio)

	Intensity (mcd) at 20 mA	
Bin	**Min**	**Max**
Q	460	550
R	550	660
S	660	800
T	800	960
U	960	1150
V	1150	1380
W	1380	1660
X	1660	1990
Y	1990	2400
Z	2400	2900
1	2900	3500
2	3500	4200
3	4200	5040

Tolerance for each bin limit is ± 15%

V_F Bin Table (V at 20mA)

Bin ID	Min	Max
VD	1.8	2.0
VA	2.0	2.2
VB	2.2	2.4

Notes:
1. Tolerance for each bin limit is ±0.05V
2. V_F binning only applicable to Red color.

Red Color Range

Min Dom	Max Dom	Xmin	Ymin	Xmax	Ymax
618	630	0.6872	0.3126	0.6890	0.2943
		0.6690	0.3149	0.7080	0.2920

Tolerance for each bin limit is ± 0.5nm

Green Color Bin Table

Bin	Min Dom	Max Dom	Xmin	Ymin	Xmax	Ymax
1	520.0	524.0	0.0743	0.8338	0.1856	0.6556
			0.1650	0.6586	0.1060	0.8292
2	524.0	528.0	0.1060	0.8292	0.2068	0.6463
			0.1856	0.6556	0.1387	0.8148
3	528.0	532.0	0.1387	0.8148	0.2273	0.6344
			0.2068	0.6463	0.1702	0.7965
4	532.0	536.0	0.1702	0.7965	0.2469	0.6213
			0.2273	0.6344	0.2003	0.7764
5	536.0	540.0	0.2003	0.7764	0.2659	0.6070
			0.2469	0.6213	0.2296	0.7543

Tolerance for each bin limit is ± 0.5nm.

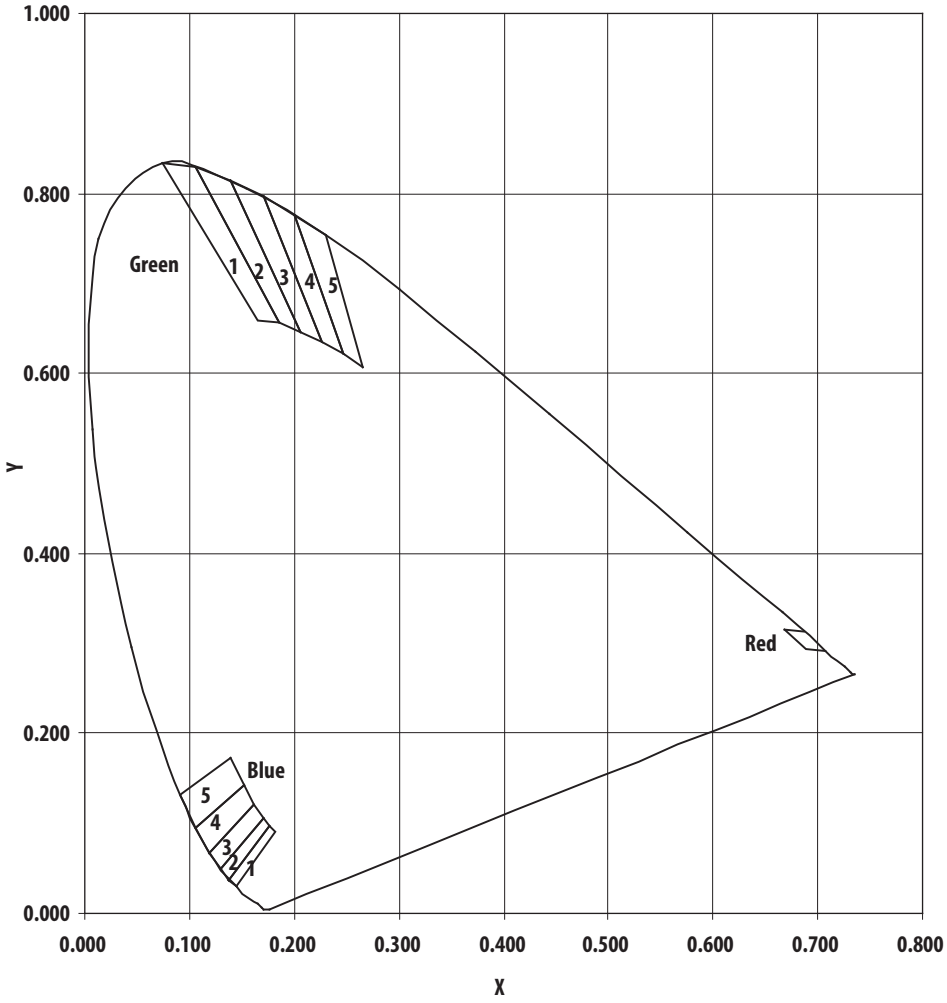
Blue Color Bin Table

Bin	Min Dom	Max Dom	Xmin	Ymin	Xmax	Ymax
1	460.0	464.0	0.1440	0.0297	0.1766	0.0966
			0.1818	0.0904	0.1374	0.0374
2	464.0	468.0	0.1374	0.0374	0.1699	0.1062
			0.1766	0.0966	0.1291	0.0495
3	468.0	472.0	0.1291	0.0495	0.1616	0.1209
			0.1699	0.1062	0.1187	0.0671
4	472.0	476.0	0.1187	0.0671	0.1517	0.1423
			0.1616	0.1209	0.1063	0.0945
5	476.0	480.0	0.1063	0.0945	0.1397	0.1728
			0.1517	0.1423	0.0913	0.1327

Tolerance for each bin limit is ± 0.5nm

Note:
1. All bin categories are established for classification of products. Products may not be available in all bin categories. Please contact your Avago representative for further information.

Avago Color Bin on CIE 1931 Chromaticity Diagram



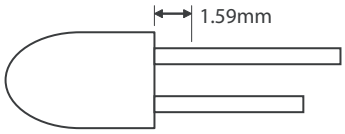
Precautions:

Lead Forming:

- The leads of an LED lamp may be preformed or cut to length prior to insertion and soldering on PC board.
- For better control, it is recommended to use proper tool to precisely form and cut the leads to applicable length rather than doing it manually.
- If manual lead cutting is necessary, cut the leads after the soldering process. The solder connection forms a mechanical ground which prevents mechanical stress due to lead cutting from traveling into LED package. This is highly recommended for hand solder operation, as the excess lead length also acts as small heat sink.

Soldering and Handling:

- Care must be taken during PCB assembly and soldering process to prevent damage to the LED component.
- LED component may be effectively hand soldered to PCB. However, it is only recommended under unavoidable circumstances such as rework. The closest manual soldering distance of the soldering heat source (soldering iron's tip) to the body is 1.59mm. Soldering the LED using soldering iron tip closer than 1.59mm might damage the LED.



- ESD precaution must be properly applied on the soldering station and personnel to prevent ESD damage to the LED component that is ESD sensitive. Do refer to Avago application note AN 1142 for details. The soldering iron used should have grounded tip to ensure electrostatic charge is properly grounded.
- Recommended soldering condition:

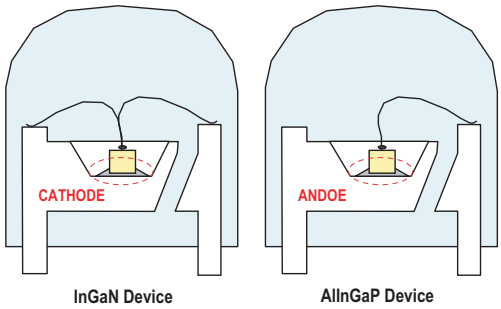
	Wave Soldering [1, 2]	Manual Solder Dipping
Pre-heat temperature	105 °C Max.	-
Preheat time	60 sec Max	-
Peak temperature	260 °C Max.	260 °C Max.
Dwell time	5 sec Max.	5 sec Max

Note:
1. Above conditions refers to measurement with thermocouple mounted at the bottom of PCB.
2. It is recommended to use only bottom preheaters in order to reduce thermal stress experienced by LED.

- Wave soldering parameters must be set and maintained according to the recommended temperature and dwell time. Customer is advised to perform daily check on the soldering profile to ensure that it is always conforming to recommended soldering conditions.

Note:
1. PCB with different size and design (component density) will have different heat mass (heat capacity). This might cause a change in temperature experienced by the board if same wave soldering setting is used. So, it is recommended to re-calibrate the soldering profile again before loading a new type of PCB.
2. Avago Technologies' AlInGaP high brightness LED are using high efficiency LED die with single wire bond as shown below. Customer is advised to take extra precaution during wave soldering to ensure that the maximum wave temperature does not exceed 260°C and the solder contact time does not exceeding 5sec. Over-stressing the LED during soldering process might cause premature failure to the LED due to delamination.

Avago Technologies LED configuration



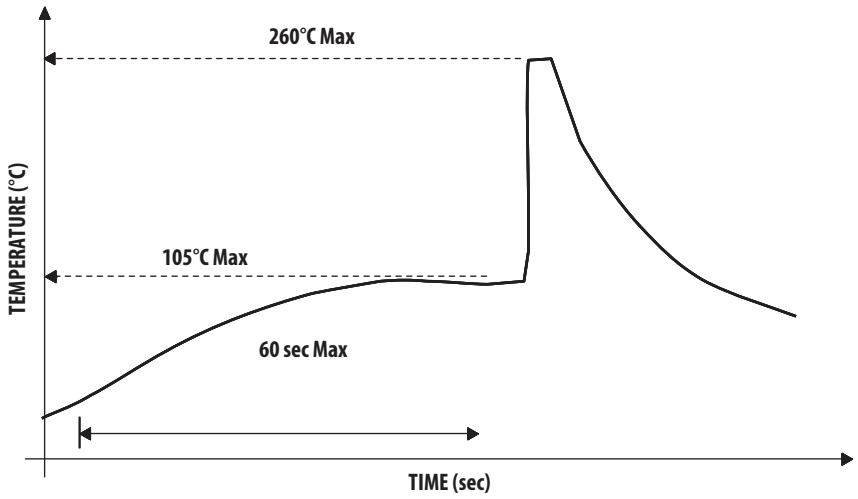
- Any alignment fixture that is being applied during wave soldering should be loosely fitted and should not apply weight or force on LED. Non metal material is recommended as it will absorb less heat during wave soldering process.
- At elevated temperature, LED is more susceptible to mechanical stress. Therefore, PCB must allowed to cool down to room temperature prior to handling, which includes removal of alignment fixture or pallet.
- If PCB board contains both through hole (TH) LED and other surface mount components, it is recommended that surface mount components be soldered on the top side of the PCB. If surface mount need to be on the bottom side, these components should be soldered using reflow soldering prior to insertion the TH LED.
- Recommended PC board plated through holes (PTH) size for LED component leads.

LED component lead size	Diagonal	Plated through hole diameter
0.45 x 0.45 mm (0.018x 0.018 inch)	0.636 mm (0.025 inch)	0.98 to 1.08 mm (0.039 to 0.043 inch)
0.50 x 0.50 mm (0.020x 0.020 inch)	0.707 mm (0.028 inch)	1.05 to 1.15 mm (0.041 to 0.045 inch)

- Over-sizing the PTH can lead to twisted LED after clinching. On the other hand under sizing the PTH can cause difficulty inserting the TH LED.

Refer to application note AN5334 for more information about soldering and handling of high brightness TH LED lamps.

Example of Wave Soldering Temperature Profile for TH LED



Recommended solder:
Sn63 (Leaded solder alloy)
SAC305 (Lead free solder alloy)

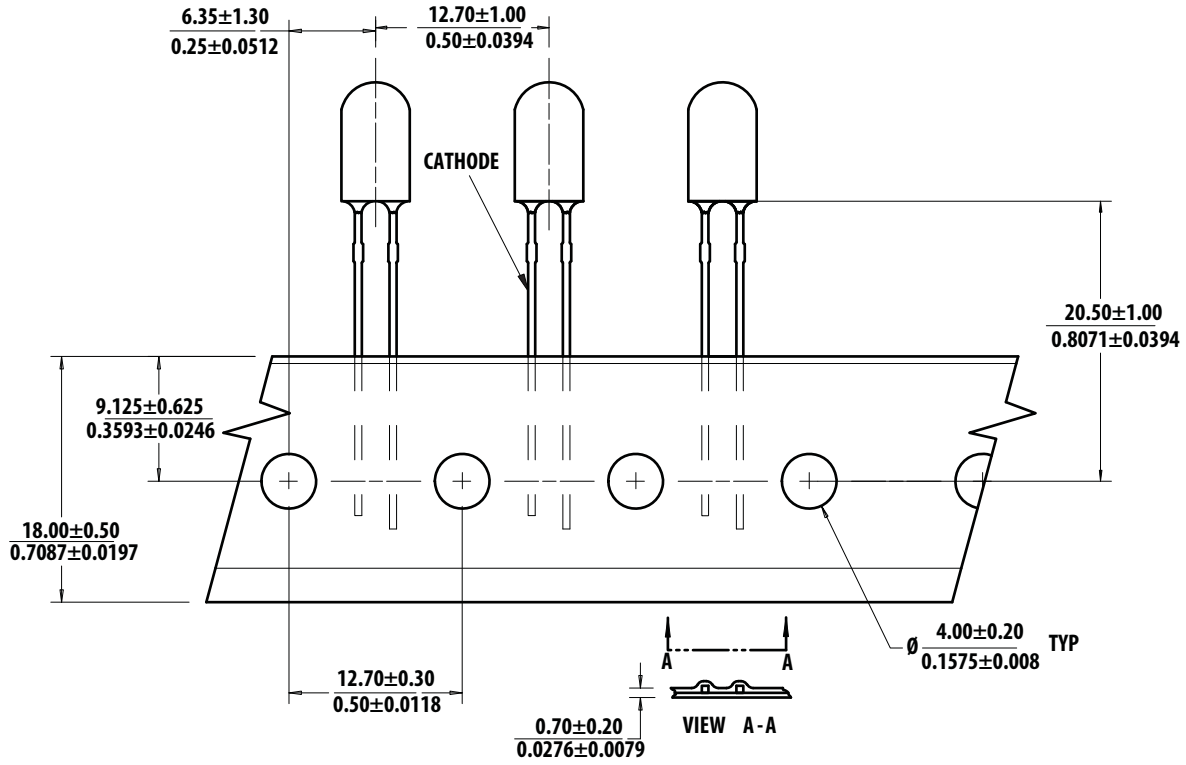
Flux: Rosin flux

Solder bath temperature: 255°C ± 5°C
(maximum peak temperature = 260°C)

Dwell time: 3.0 sec - 5.0 sec
(maximum = 5sec)

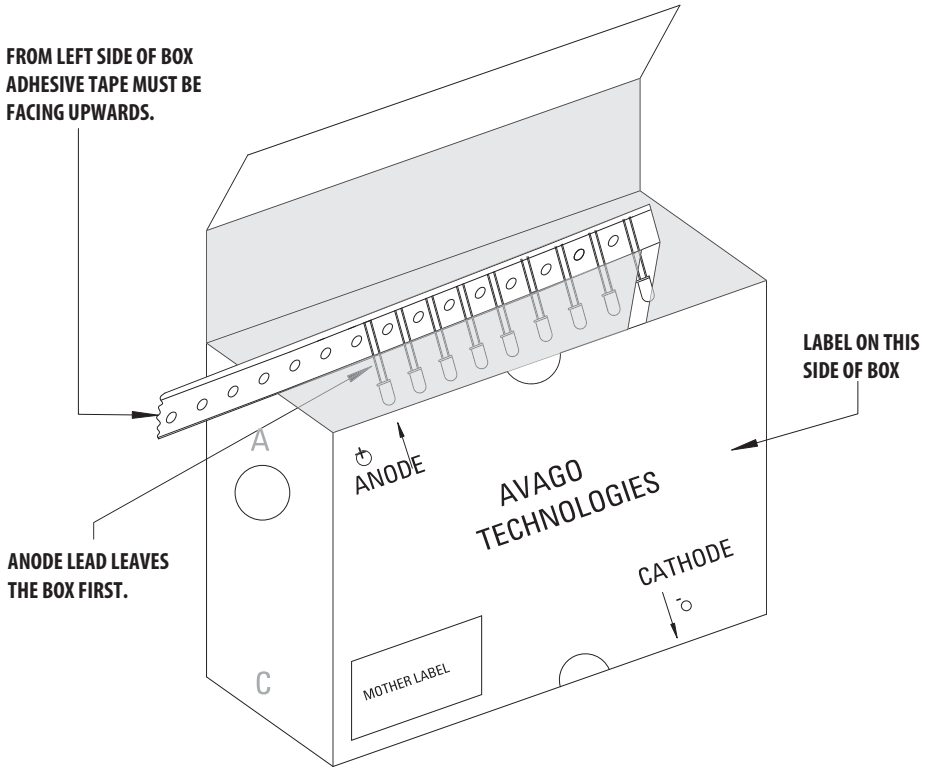
Note: Allow for board to be sufficiently cooled to room temperature before exerting mechanical force.

Ammo Packs Drawing



Note: All dimensions in millimeters (inches)

Packaging Box for Ammo Packs

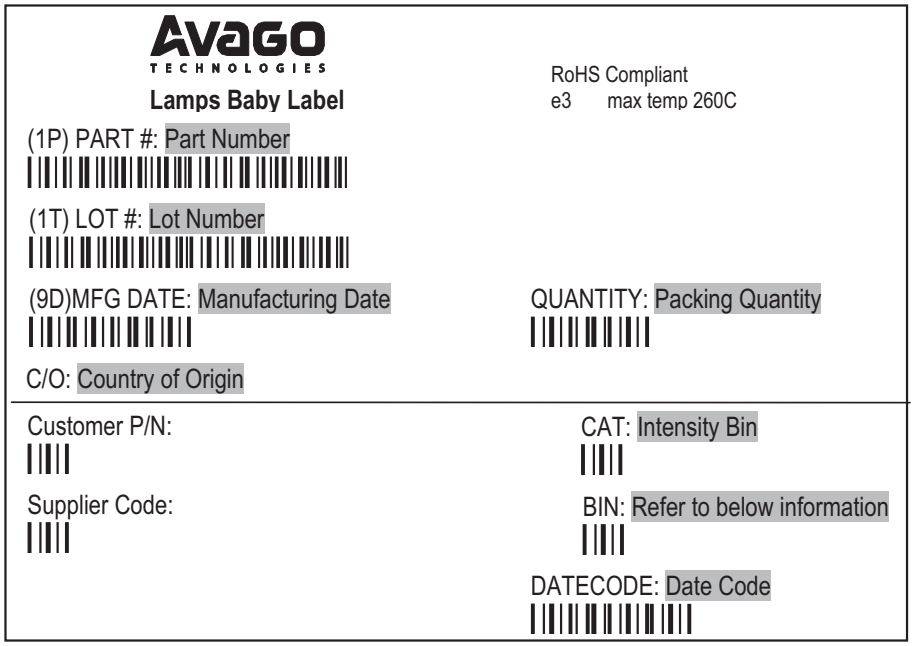


Note: For InGaN device, the ammo pack packaging box contain ESD logo

Packaging Label

(i) Avago Mother Label: (Available on packaging box of ammo pack and shipping box)

(ii) Avago Baby Label (Only available on bulk packaging)



Acronyms and Definition:

BIN:

(i) Color bin only or VF bin only

(Applicable for part number with color bins but without VF bin OR part number with VF bins and no color bin)

OR

(ii) Color bin incorporated with VF Bin

(Applicable for part number that have both color bin and VF bin)

Example:

(i) Color bin only or VF bin only

BIN: 2 (represent color bin 2 only)

BIN: VB (represent VF bin "VB" only)

(ii) Color bin incorporate with VF Bin

BIN: 2VB

VB: VF bin "VB"

2: Color bin 2 only

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AV02-1485EN - November 4, 2009

AVAGO TECHNOLOGIES

FAIRCHILD SEMICONDUCTOR®

March 2009

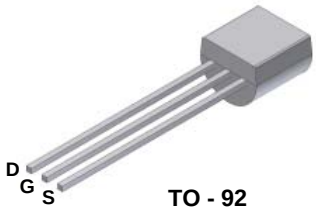
BS170 / MMBF170
N-Channel Enhancement Mode Field Effect Transistor

General Description

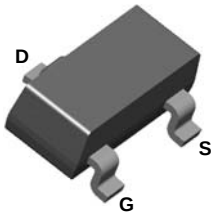
These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 500mA DC. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

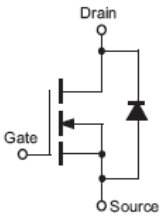
- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.



TO - 92



SOT - 23



Absolute Maximum Ratings T_a = 25°C unless otherwise noted

Symbol	Parameter	BS170	MMBF170	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1M\Omega$)	60		V
V_{GSS}	Gate-Source Voltage	± 20		V
I_D	Drain Current - Continuous	500	500	mA
	- Pulsed	1200	800	
T_J, T_{STG}	Operating and Storage Temperature Range	- 55 to 150		°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300		°C

Thermal Characteristics T_a = 25°C unless otherwise noted

Symbol	Parameter	BS170	MMBF170	Units
P_D	Maximum Power Dissipation Derate above 25°C	830 6.6	300 2.4	mW mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	150	417	°C/W

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Conditions	Type	Min.	Typ.	Max.	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 100 μA	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 25 V, V_{GS} = 0 V	All			0.5	μA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 15V, V_{DS} = 0 V	All			10	nA
On Characteristics (Notes 1)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	All	0.8	2.1	3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 200 mA	All		1.2	5	Ω
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 200 mA	BS170		320		mS
		$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA	MMBF170		320		
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	All		24	40	pF
C_{oss}	Output Capacitance		All		17	30	pF
C_{rss}	Reverse Transfer Capacitance		All		7	10	pF
Switching Characteristics (Notes 1)							
t_{on}	Turn-On Time	V_{DD} = 25 V, I_D = 200 mA, V_{GS} = 10 V, R_{GEN} = 25 Ω	BS170			10	ns
		V_{DD} = 25 V, I_D = 500 mA, V_{GS} = 10 V, R_{GEN} = 50 Ω	MMBF170			10	
t_{off}	Turn-Off Time	V_{DD} = 25 V, I_D = 200 mA, V_{GS} = 10 V, R_{GEN} = 25 Ω	BS170			10	ns
		V_{DD} = 25 V, I_D = 500 mA, V_{GS} = 10 V, R_{GEN} = 50 Ω	MMBF170			10	

Note:
1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

BS170 / MMBF170

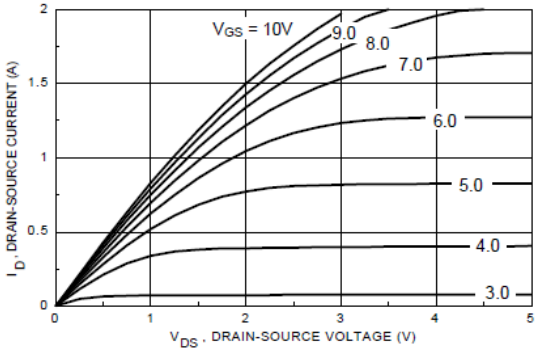


Figure 1. On-Region Characteristics.

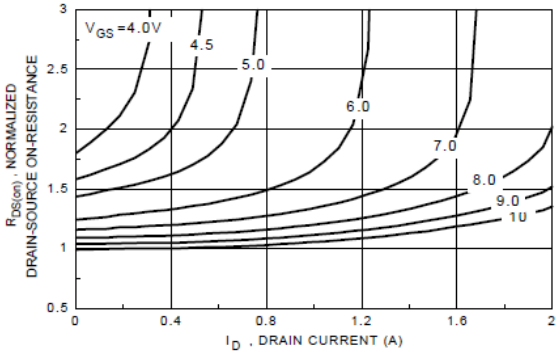


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

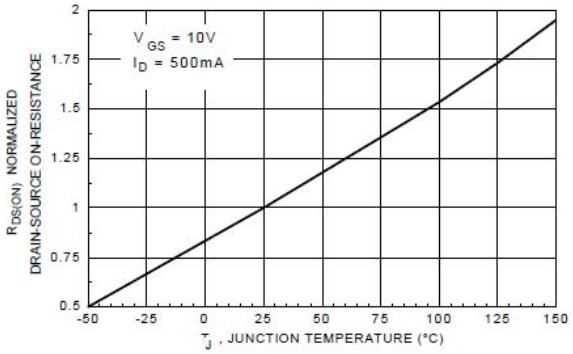


Figure 3. On-Resistance Variation with Temperature.

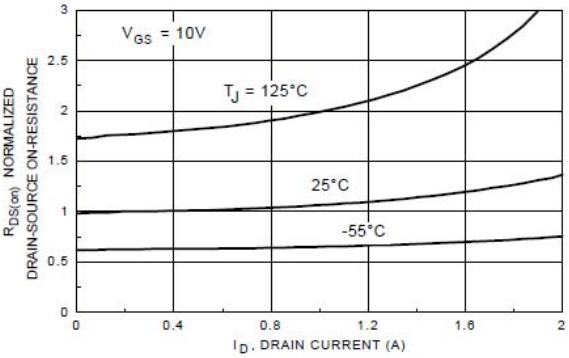


Figure 4. On-Resistance Variation with Drain Current and Temperature.

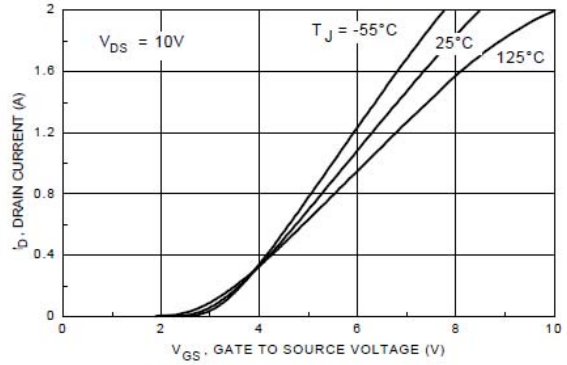


Figure 5. Transfer Characteristics.

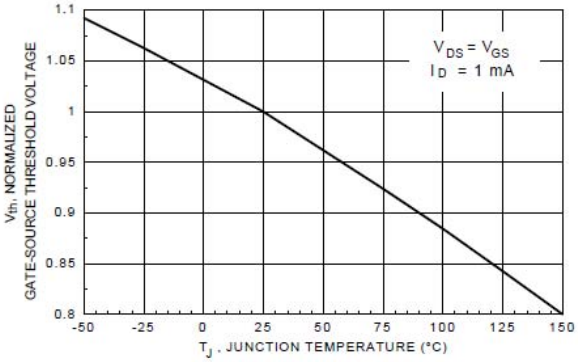


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

BS170 / MMBF170

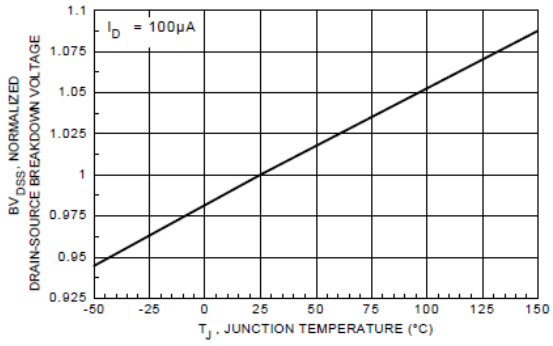


Figure 7. Breakdown Voltage Variation with Temperature.

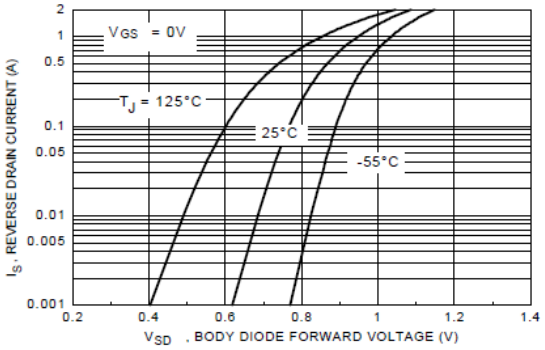


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

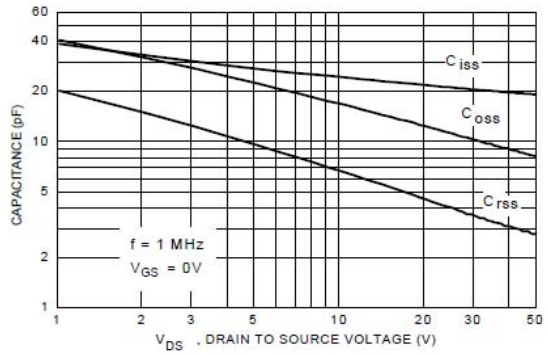


Figure 9. Capacitance Characteristics.

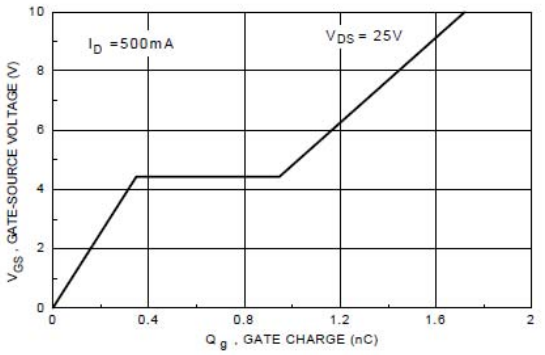


Figure 10. Gate Charge Characteristics.

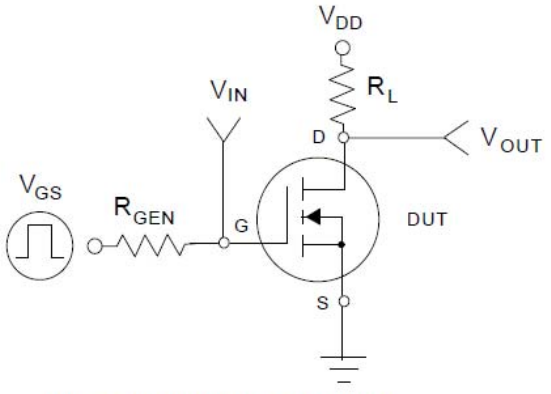


Figure 11. Switching Test Circuit.

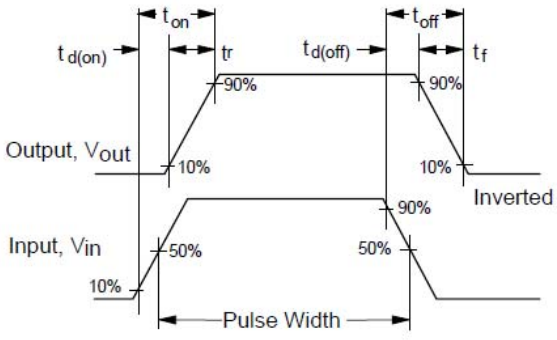


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

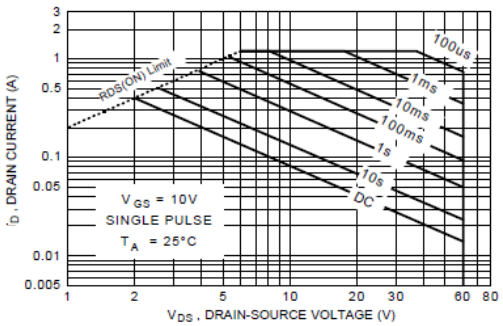


Figure 13. BS170 Maximum Safe Operating Area.

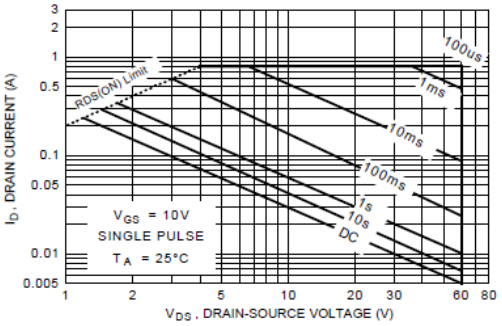


Figure 14. MMBF170 Maximum Safe Operating Area.

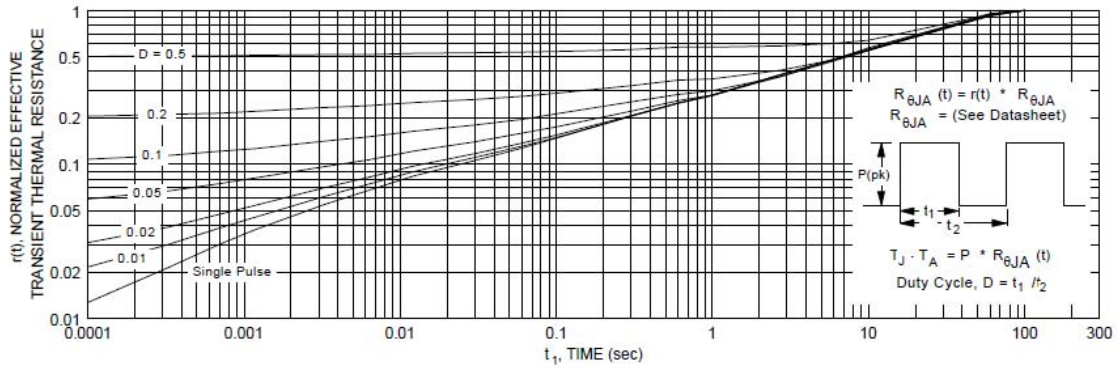


Figure 15. TO-92, BS170 Transient Thermal Response Curve.

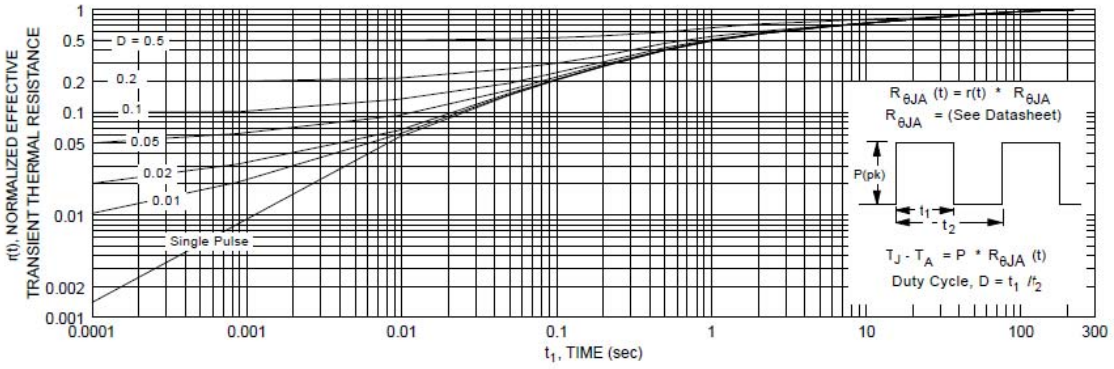
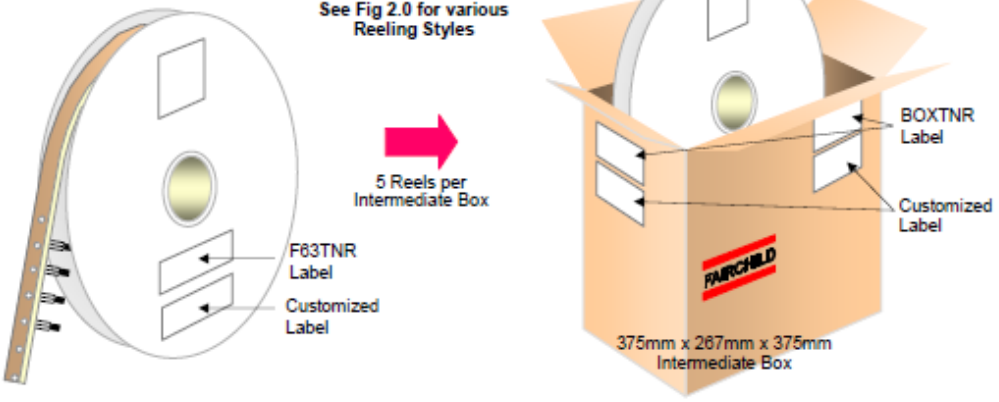


Figure 16. SOT-23, MMBF170 Transient Thermal Response Curve.

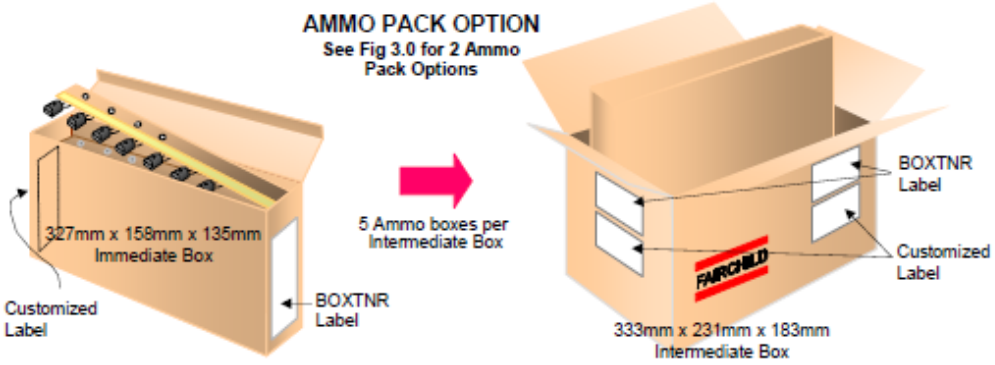
TO-92 Tape and Reel Data

TO-92 Packaging
Configuration: Figure 1.0

TAPE and REEL OPTION
See Fig 2.0 for various Reeling Styles



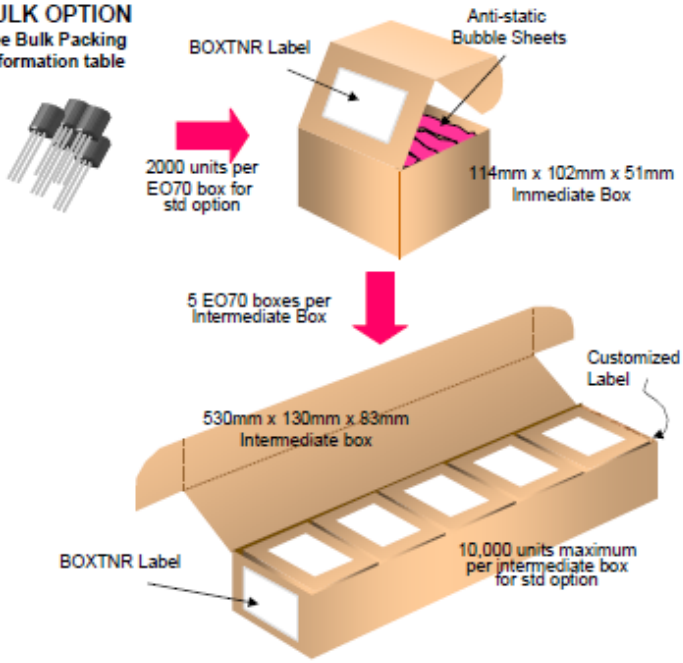
AMMO PACK OPTION
See Fig 3.0 for 2 Ammo Pack Options



BULK OPTION
See Bulk Packing Information table

BOXTNR Label sample

F63TNR Label sample



TO-92 Tape and Reel Data, continued

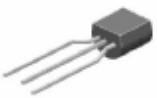
TO-92 Packing Information: Figure 2.0

TO-92 TNR/AMMO PACKING INFORMATION TABLE

Packing	Style	Quantity	EOL code
Reel	A	2,000	D26Z
	B	2,000	D11Z
	C	2,000	D28Z
	D	2,000	D10Z
	E	2,000	D27Z
	F	2,000	D81Z
	G	2,000	D29Z
	H	2,000	D89Z
Ammo	M	2,000	D74Z
	P	2,000	D75Z

Unit weight = 0.22 gm
Reel weight with components = 1.04 kg
Ammo weight with components = 1.02 kg
Max quantity per intermediate box = 10,000 units

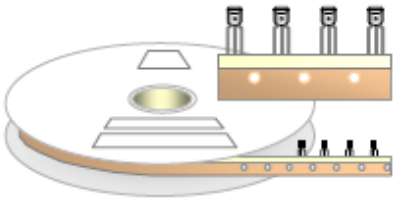
TO-92 BULK PACKING INFORMATION TABLE

EOL CODE / FLOW OPTION	DESCRIPTION	LEADCLIP DIMENSION	MINIMUM ORDER QTY	LEADFORM OULTINE
NO EOL CODE	STRAIGHT LEADS	NO LEAD CLIP	2.0K / BOX	
J18Z	TO-18 OPTION STD	NO LEAD CLIP	2.0K / BOX	
J35Z	TO-18 OPTION REVERSE	NO LEAD CLIP	2.0K / BOX	
J05Z	TO-5 OPTION STD	NO LEAD CLIP	1.5K / BOX	
J60Z	TO-5 OPTION REVERSE	NO LEAD CLIP	1.5K / BOX	
J61Z	IN LINE 0.200 SPACING	NO LEAD CLIP	1.5K / BOX	

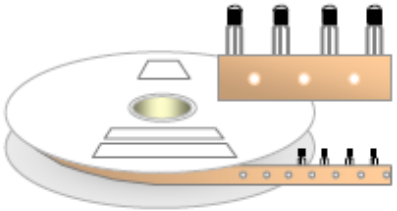
TO-92 Tape and Reel Data, continued

TO-92 Reeling Style
Configuration: Figure 3.0

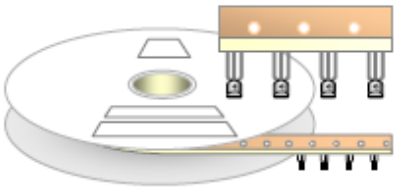
Machine Option "A" (H)



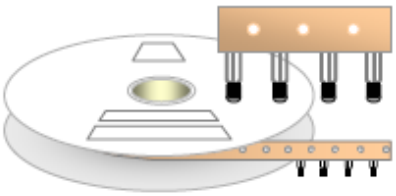
Style "A", D26Z



Style "B", D11Z

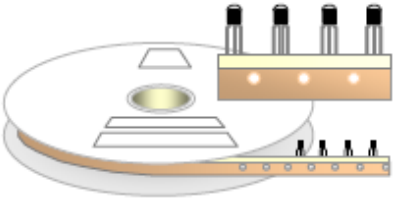


Style "C", D28Z

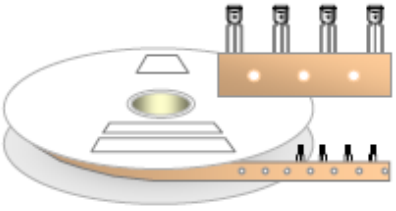


Style "D", D10Z

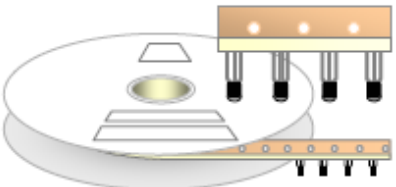
Machine Option "E" (J)



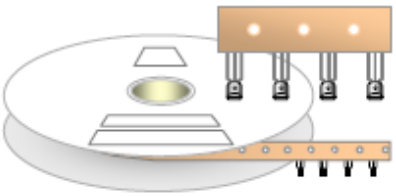
Style "E", D27Z



Style "F", D81Z

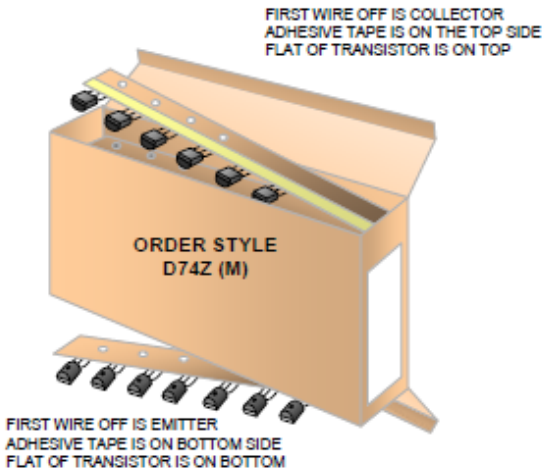


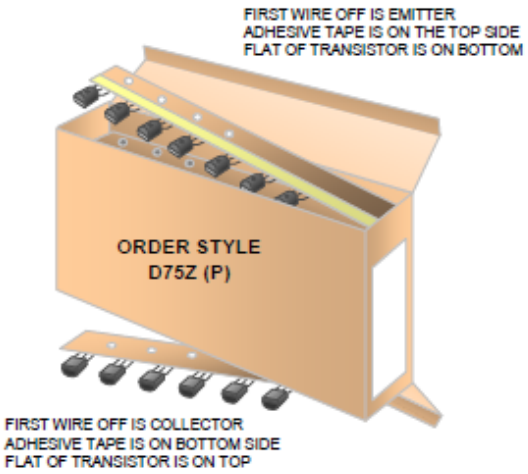
Style "G", D29Z



Style "H", D89Z

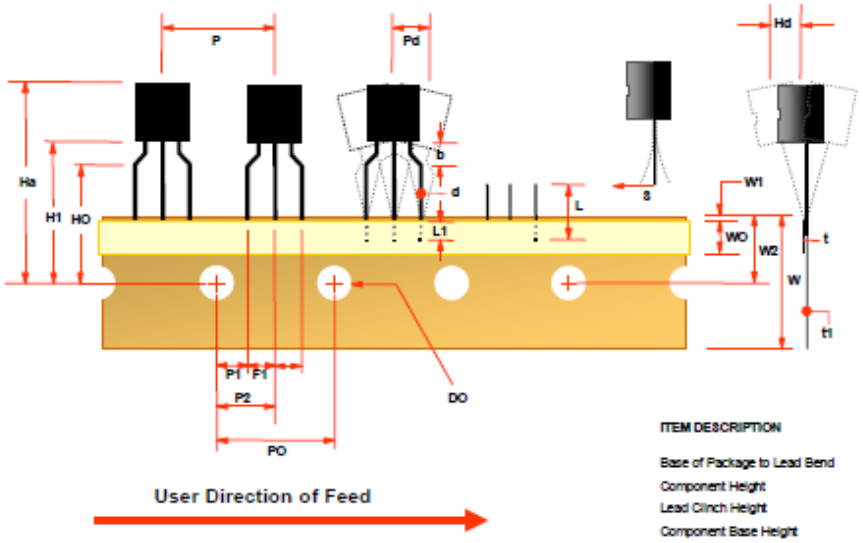
TO-92 Radial Ammo Packaging
Configuration: Figure 4.0





TO-92 Tape and Reel Data, continued

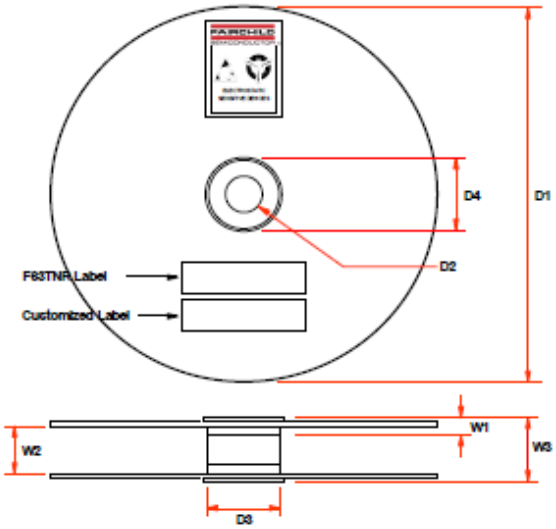
TO-92 Tape and Reel Taping
Dimension Configuration: Figure 5.0



ITEM DESCRIPTION	SYMBOL	DIMENSION
Base of Package to Lead Bend	b	0.098 (max)
Component Height	Ha	0.928 (+/- 0.025)
Lead Clinch Height	HO	0.630 (+/- 0.020)
Component Base Height	H1	0.748 (+/- 0.020)
Component Alignment (side/side)	Pd	0.040 (max)
Component Alignment (front/back)	Hd	0.031 (max)
Component Pitch	P	0.500 (+/- 0.020)
Feed Hole Pitch	PO	0.500 (+/- 0.008)
Hole Center to First Lead	P1	0.150 (+0.009, -0.010)
Hole Center to Component Center	P2	0.247 (+/- 0.007)
Lead Spread	F1/F2	0.104 (+/- 0 .010)
Lead Thickness	d	0.018 (+0.002, -0.003)
Cut Lead Length	L	0.429 (max)
Taped Lead Length	L1	0.209 (+0.051, -0.052)
Taped Lead Thickness	t	0.032 (+/- 0.006)
Carrier Tape Thickness	t1	0.021 (+/- 0.006)
Carrier Tape Width	W	0.708 (+0.020, -0.019)
Hold - down Tape Width	WO	0.236 (+/- 0.012)
Hold - down Tape position	W1	0.035 (max)
Feed Hole Position	W2	0.360 (+/- 0.025)
Sprocket Hole Diameter	DO	0.157 (+0.008, -0.007)
Lead Spring Out	S	0.004 (max)

Note : All dimensions are in inches.

TO-92 Reel
Configuration: Figure 6.0

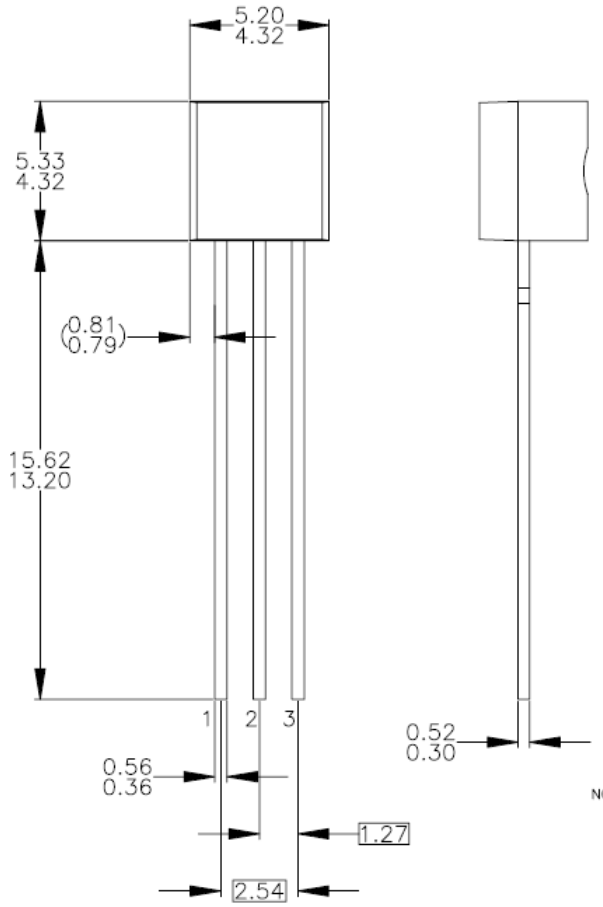


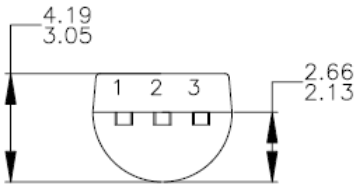
ITEM DESCRIPTION	SYMBOL	MINIMUM	MAXIMUM
Reel Diameter	D1	13.975	14.025
Arbor Hole Diameter (Standard)	D2	1.160	1.200
(Small Hole)	D2	0.650	0.700
Core Diameter	D3	3.100	3.300
Hub Recess Inner Diameter	D4	2.700	3.100
Hub Recess Depth	W1	0.370	0.570
Flange to Flange Inner Width	W2	1.630	1.690
Hub to Hub Center Width	W3		2.090

Note: All dimensions are inches

Mechanical Dimensions (TO - 92)

TO - 92





NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

P.N.	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

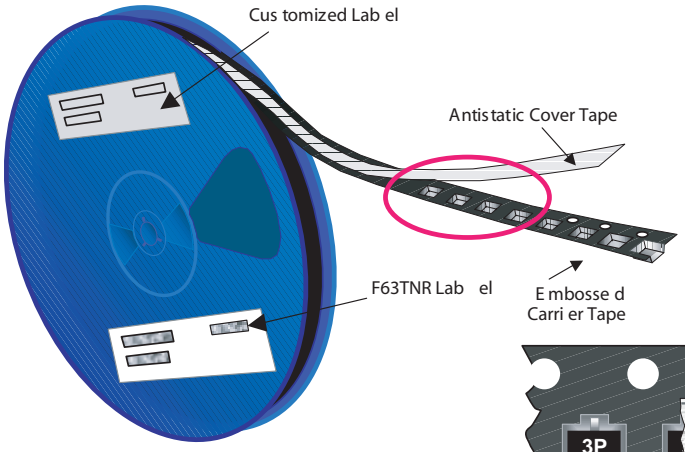
E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03DREV3.

Dimensions in Millimeters

SOT-23 Std Tape and Reel Data

FAIRCHILD SEMICONDUCTOR®

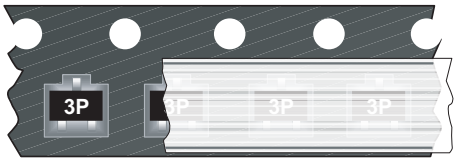
SOT23-3L Packaging Configuration: Figure 1.0



Packaging Description:

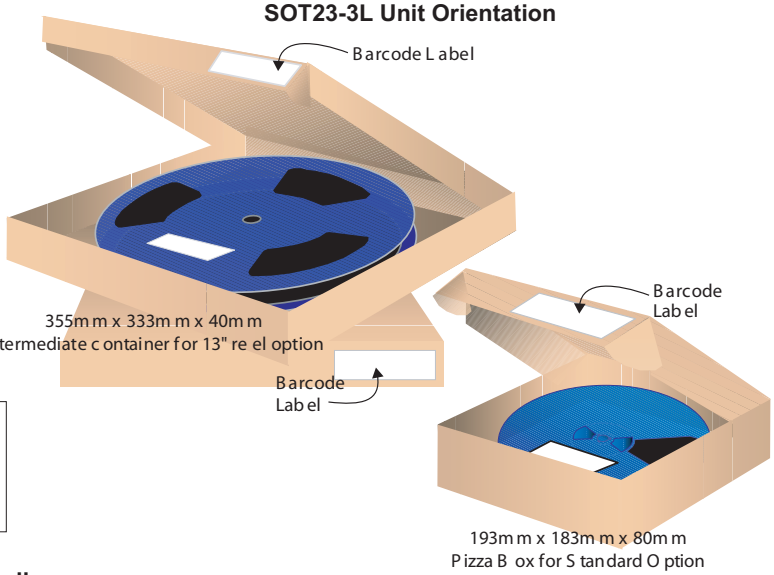
SOT23-3L parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 177mm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 10,000 units per 13" or 330cm diameter reel. This and some other options are described in the Packaging Information table.

These full reels are individually labeled and placed inside a standard immediate box made of recyclable corrugated brown paper with a Fairchild logo printing. One box contains five reels maximum. And these immediate boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

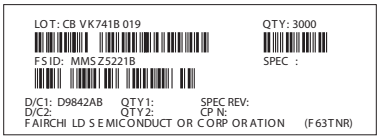


SOT23-3L Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	193x183x80	355x333x40
Max qty per Box	15,000	30,000
Weight per unit (gm)	0.0082	0.0082
Weight per Reel (kg)	0.1175	0.4006
Note/Comments		

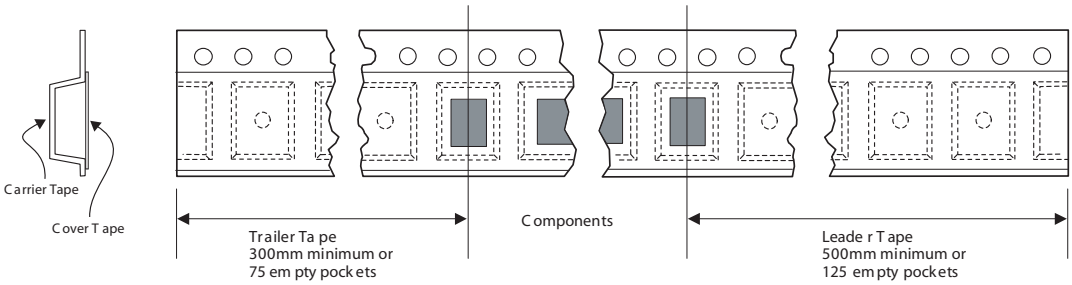
SOT23-3L Unit Orientation



Barcode Label sample

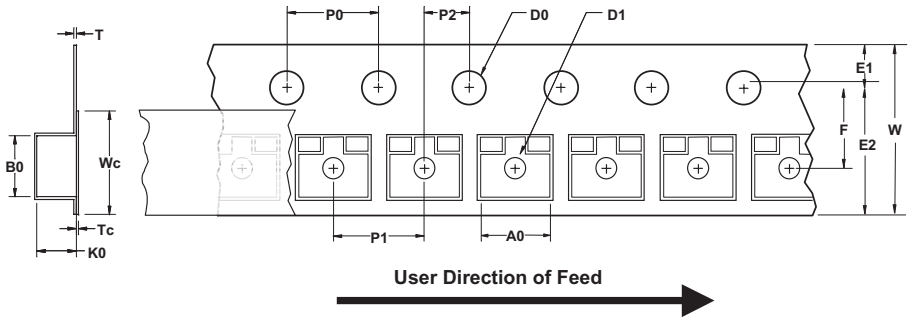


SOT23-3L Tape Leader and Trailer Configuration: Figure 2.0



SOT-23 Std Tape and Reel Data, continued

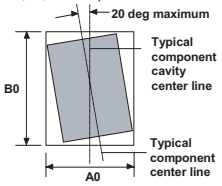
SOT23-3L Embossed Carrier Tape
Configuration: Figure 3.0



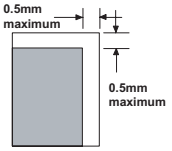
Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SOT-23 (8mm)	3.15 +/-0.10	2.77 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.30 +/-0.10	0.228 +/-0.013	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Sketch A (Side or Front Sectional View)
Component Rotation

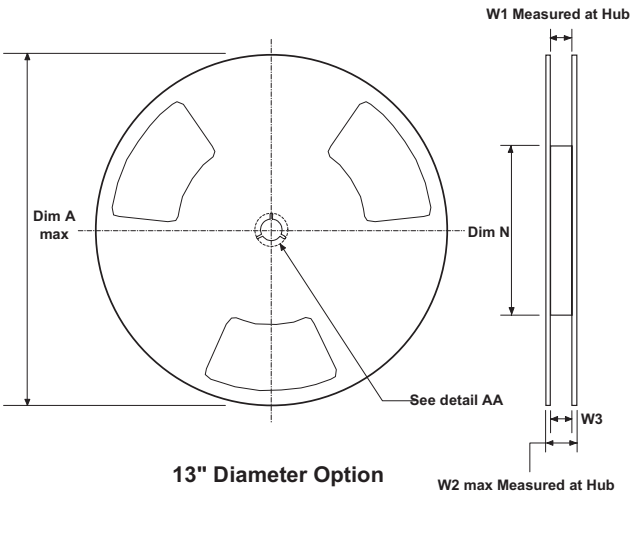


Sketch B (Top View)
Component Rotation

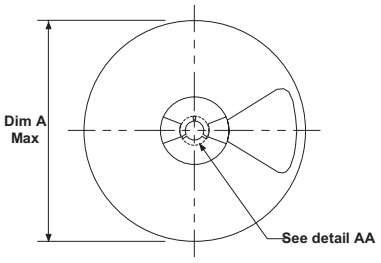


Sketch C (Top View)
Component lateral movement

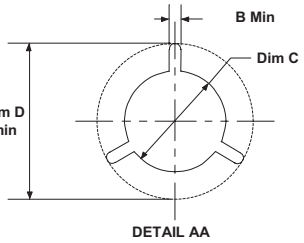
SOT23-3L Reel Configuration: Figure 4.0



13" Diameter Option



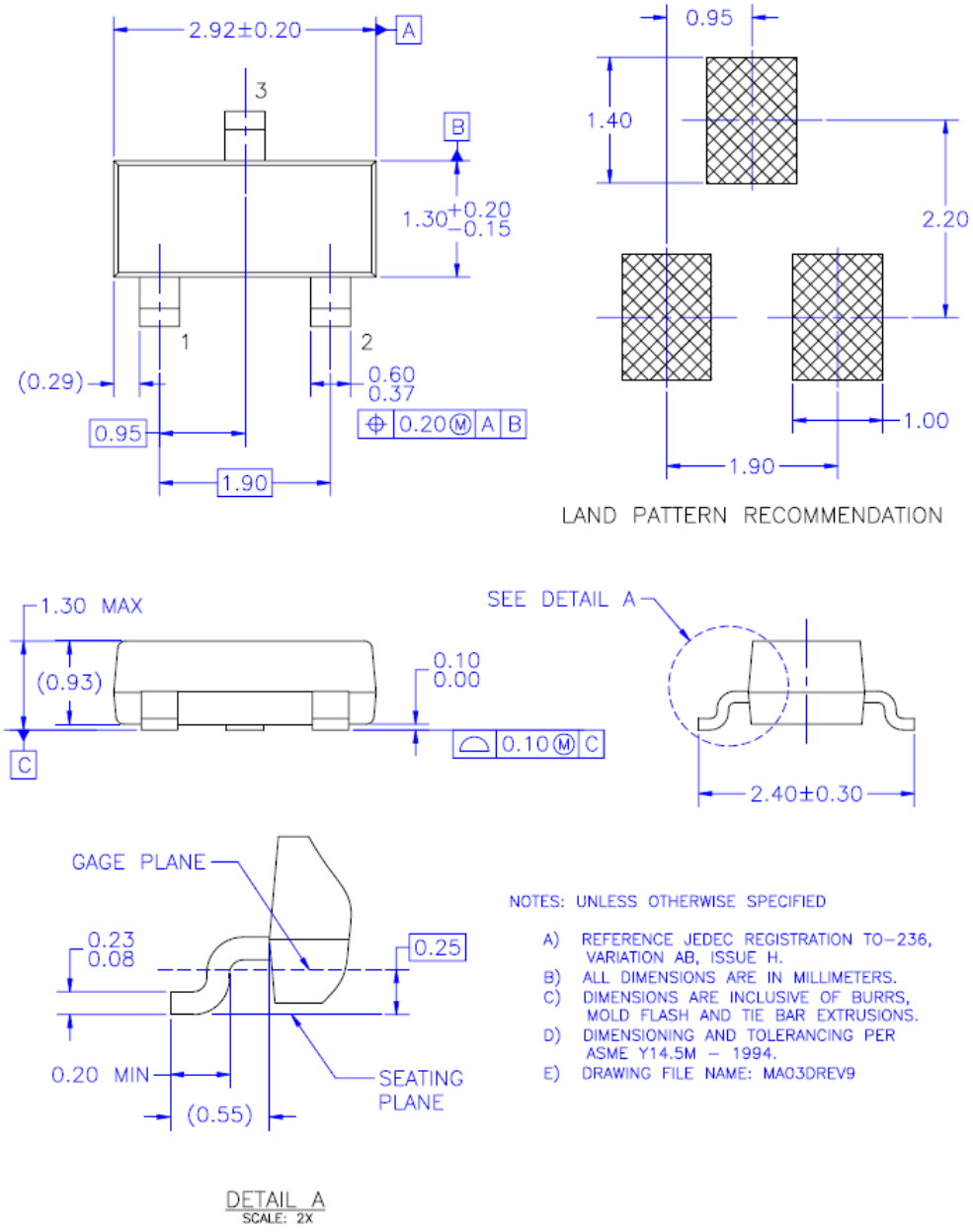
7" Diameter Option



Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10. 9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10. 9

Mechanical Dimensions (SOT - 23)

SOT - 23



Dimensions in Millimeters

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I40

Cree® Screen Master® 5-mm Oval LED
C5SMF-RJS/GJS/BJS
C5SME-RJS
Data Sheet

This oval LED is specifically designed for variable-message signs and passenger-information signs. The oval-shaped radiation pattern and high luminous intensity ensure that these devices are excellent for wide-field-of-view outdoor applications where a wide viewing angle and readability in sunlight are essential.

These lamps are made with an advanced optical-grade epoxy that offers superior high-temperature and moisture-resistance performance in outdoor signage applications. The encapsulation resin contains UV inhibitors to minimize the effects of long-term exposure to direct sunlight, resulting in stable light output over the life of the LED.

FEATURES

- Size (mm): 5
- Color and Typical Dominant Wavelength (nm):
  - » Red (621)
  - » Green (527)
  - » Blue (470)
- Luminous Intensity (mcd)
  - » C5SMF - Red (1100-4180)
    Green (2130-8200)
    Blue (550-2130)
- » C5SME - Red (770-2130)
- Lead-Free
- RoHS-Compliant

APPLICATIONS

- Electronic Signs & Signals (ESS)
- Full-Color Video Screen
- Motorway Signs
- Variable-Message Sign (VMS)
- Advertising Signs
- Petrol Signs

Absolute Maximum Ratings (T_A = 25°C)

Items	Symbol	Absolute Maximum Rating		Unit
		Red	Blue and Green	
Forward Current	I_F	50 Note1	35	mA
Peak Forward Current Note2	I_{FP}	200	100	mA
Reverse Voltage	V_R	5	5	V
Power Dissipation	P_D	130	140	mW
Operation Temperature	T_{opr}	-40 ~ +95		°C
Storage Temperature	T_{stg}	-40 ~ +100		°C
Lead Soldering Temperature	T_{sol}	Max. 260°C for 3 sec. max. (3 mm from the base of the epoxy bulb)		
Electrostatic Discharge Classification (MIL-STD-883E)	ESD	Class 2		

Note:

1. For long-term performance, the drive currents between 10 mA and 30 mA are recommended. Please contact a Cree sales representative for more information on recommended drive conditions.
2. Pulse width ≤0.1 msec, duty ≤1/10.

Typical Electrical & Optical Characteristics (T_A = 25°C)

Characteristics	Color	Symbol	Condition	Unit	Minimum	Typical	Maximum
Forward Voltage	Red	V_F	I_F = 20 mA	V		2.1	2.6
	Blue/Green	V_F	I_F = 20 mA	V		3.4	4.0
Reverse Current	Red	I_R	V_R = 5 V	μA			100
	Blue/Green	I_R	V_R = 5 V	μA			100
Dominant Wavelength	Red	λ_D	I_F = 20 mA	nm	619	621	624
	Green	λ_D	I_F = 20 mA	nm	520	527	535
	Blue	λ_D	I_F = 20 mA	nm	460	470	475
Luminous Intensity	C5SMF - Red	I_V	I_F = 20 mA	mcd	1100	2200	
	C5SME - Red	I_V	I_F = 20 mA	mcd	770	1100	
	Green	I_V	I_F = 20 mA	mcd	2130	4400	
	Blue	I_V	I_F = 20 mA	mcd	550	1100	

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.313.5778
www.cree.com/ledlamps

Intensity Bin Limit (I_F = 20 mA)

Red: C5SMF

Bin Code	Sub-bin	Min. (mcd)	Max. (mcd)
T0	T1	1100	1205
	T2	1205	1310
	T3	1310	1415
	T4	1415	1520
U0	U1	1520	1672
	U2	1672	1824
	U3	1824	1976
	U4	1976	2130
V0	V1	2130	2347
	V2	2347	2564
	V3	2564	2781
	V4	2781	3000
W0	W1	3000	3295
	W2	3295	3590
	W3	3590	3885
	W4	3885	4180

Green:C5SMF

Bin Code	Sub-bin	Min. (mcd)	Max. (mcd)
V0	V1	2130	2347
	V2	2347	2564
	V3	2564	2781
	V4	2781	3000
W0	W1	3000	3295
	W2	3295	3590
	W3	3590	3885
	W4	3885	4180
X0	X1	4180	4600
	X2	4600	5020
	X3	5020	5440
	X4	5440	5860
Y0	Y1	5860	6445
	Y2	6445	7030
	Y3	7030	7615
	Y4	7615	8200

Blue:C5SMF

Bin Code	Sub-bin	Min. (mcd)	Max. (mcd)
R0	R1	550	605
	R2	605	660
	R3	660	715
	R4	715	770
S0	S1	770	852
	S2	852	934
	S3	934	1017
	S4	1017	1100
T0	T1	1100	1205
	T2	1205	1310
	T3	1310	1415
	T4	1415	1520
U0	U1	1520	1672
	U2	1672	1824
	U3	1824	1976
	U4	1976	2130

Red: C5SME

Bin Code	Sub-bin	Min. (mcd)	Max. (mcd)
S0	S1	770	852
	S2	852	934
	S3	934	1017
	S4	1017	1100
T0	T1	1100	1205
	T2	1205	1310
	T3	1310	1415
	T4	1415	1520
U0	U1	1520	1672
	U2	1672	1824
	U3	1824	1976
	U4	1976	2130

Tolerance of measurement of luminous intensity is ±15%

Color Bin Limit (I_F = 20 mA)

Red

Bin Code	Min.(nm)	Max.(nm)
RB	619	624

Green

Bin Code	Min.(nm)	Max.(nm)
G7	520	525
G8	525	530
G9	530	535

Blue

Bin Code	Min.(nm)	Max.(nm)
B3	460	465
B4	465	470
B5	470	475

Tolerance of measurement of dominant wavelength is ±1 nm

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.313.5778
www.cree.com/ledlamps

Order Code Table*

C5SMF

Color	Kit Number	Luminous Intensity (mcd)		Dominant Wavelength				Package
		Min.	Max.	Color Bin	Min. (nm)	Color Bin	Max. (nm)	
Red	C5SMF-RJS-CT0W0BB1	1100	4180	RB	619	RB	624	Bulk
Red	C5SMF-RJS-CT14QBB1	Any 4 consecutive sub-bins: T1 (1100) - U2 (1824)		RB	619	RB	624	Bulk
Red	C5SMF-RJS-CT34QBB1	Any 4 consecutive sub-bins: T3 (1310) - U4 (2130)		RB	619	RB	624	Bulk
Red	C5SMF-RJS-CU14QBB1	Any 4 consecutive sub-bins: U1 (1520) - V2 (2564)		RB	619	RB	624	Bulk
Red	C5SMF-RJS-CU34QBB1	Any 4 consecutive sub-bins: U3 (1824) - V4 (3000)		RB	619	RB	624	Bulk
Red	C5SMF-RJS-CV14QBB1	Any 4 consecutive sub-bins: V1 (2130) - W2 (3590)		RB	619	RB	624	Bulk
Red	C5SMF-RJS-CT0W0BB2	1100	4180	RB	619	RB	624	Ammo
Red	C5SMF-RJS-CT14QBB2	Any 4 consecutive sub-bins: T1 (1100) - U2 (1824)		RB	619	RB	624	Ammo
Red	C5SMF-RJS-CT34QBB2	Any 4 consecutive sub-bins: T3 (1310) - U4 (2130)		RB	619	RB	624	Ammo
Red	C5SMF-RJS-CU14QBB2	Any 4 consecutive sub-bins: U1 (1520) - V2 (2564)		RB	619	RB	624	Ammo
Red	C5SMF-RJS-CU34QBB2	Any 4 consecutive sub-bins: U3 (1824) - V4 (3000)		RB	619	RB	624	Ammo
Red	C5SMF-RJS-CV14QBB2	Any 4 consecutive sub-bins: V1 (2130) - W2 (3590)		RB	619	RB	624	Ammo

Color	Kit Number	Luminous Intensity (mcd)		Dominant Wavelength				Package
		Min.	Max.	Color Bin	Min. (nm)	Color Bin	Max. (nm)	
Green	C5SMF-GJS-CV0Y0791	2130	8200	G7	520	G9	535	Bulk
Green	C5SMF-GJS-CV14Q7S1	Any 4 consecutive sub-bins: V1 (2130) - W2 (3590)		Any 1 color bin from G7 (520 nm) to G9 (535 nm)				Bulk
Green	C5SMF-GJS-CV14Q7T1	Any 4 consecutive sub-bins: V1 (2130) - W2 (3590)		Any 1 color bin from G7 (520 nm) to G8 (530 nm)				Bulk
Green	C5SMF-GJS-CW14Q7T1	Any 4 consecutive sub-bins: W1 (3000) - X2 (5020)		Any 1 color bin from G7 (520 nm) to G8 (530 nm)				Bulk
Green	C5SMF-GJS-CW34Q7T1	Any 4 consecutive sub-bins: W3 (3590) - X4 (5860)		Any 1 color bin from G7 (520 nm) to G8 (530 nm)				Bulk
Green	C5SMF-GJS-CX14Q7T1	Any 4 consecutive sub-bins: X1 (4180) - Y2 (7030)		Any 1 color bin from G7 (520 nm) to G8 (530 nm)				Bulk
Green	C5SMF-GJS-CV0Y0792	2130	8200	G7	520	G9	535	Ammo
Green	C5SMF-GJS-CV14Q7S2	Any 4 consecutive sub-bins: V1 (2130) - W2 (3590)		Any 1 color bin from G7 (520 nm) to G9 (535 nm)				Ammo
Green	C5SMF-GJS-CV14Q7T2	Any 4 consecutive sub-bins: V1 (2130) - W2 (3590)		Any 1 color bin from G7 (520 nm) to G8 (530 nm)				Ammo
Green	C5SMF-GJS-CW14Q7T2	Any 4 consecutive sub-bins: W1 (3000) - X2 (5020)		Any 1 color bin from G7 (520 nm) to G8 (530 nm)				Ammo
Green	C5SMF-GJS-CW34Q7T2	Any 4 consecutive sub-bins: W3 (3590) - X4 (5860)		Any 1 color bin from G7 (520 nm) to G8 (530 nm)				Ammo
Green	C5SMF-GJS-CX14Q7T2	Any 4 consecutive sub-bins: X1 (4180) - Y2 (7030)		Any 1 color bin from G7 (520 nm) to G8 (530 nm)				Ammo

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Order Code Table*

C5SMF

Color	Kit Number	Luminous Intensity (mcd)		Dominant Wavelength				Pack-age
		Min.	Max.	Color Bin	Min.(nm)	Color Bin	Max. (nm)	
Blue	C5SMF-BJS-CR0U0351	550	2130	B3	460	B5	475	Bulk
Blue	C5SMF-BJS-CR0U0451	550	2130	B4	465	B5	475	Bulk
Blue	C5SMF-BJS-CR14Q3T1	Any 4 consecutive sub-bins: R1 (550) - S2 (934)		Any 1 color bin from B3 (460 nm) to B4 (470 nm)				Bulk
Blue	C5SMF-BJS-CR14Q4T1	Any 4 consecutive sub-bins: R1 (550) - S2 (934)		Any 1 color bin from B4 (465 nm) to B5 (475 nm)				Bulk
Blue	C5SMF-BJS-CR24Q4T1	Any 4 consecutive sub-bins: R2 (605) - S3 (1017)		Any 1 color bin from B4 (465 nm) to B5 (475 nm)				Bulk
Blue	C5SMF-BJS-CS24Q3T1	Any 4 consecutive sub-bins: S2 (852) - T3 (1415)		Any 1 color bin from B3 (460 nm) to B4 (470 nm)				Bulk
Blue	C5SMF-BJS-CS24Q4T1	Any 4 consecutive sub-bins: S2 (852) - T3 (1415)		Any 1 color bin from B4 (465 nm) to B5 (475 nm)				Bulk
Blue	C5SMF-BJS-CT14Q3T1	Any 4 consecutive sub-bins: T1 (1100) - U2 (1824)		Any 1 color bin from B3 (460 nm) to B4 (470 nm)				Bulk
Blue	C5SMF-BJS-CT14Q4T1	Any 4 consecutive sub-bins: T1 (1100) - U2 (1824)		Any 1 color bin from B4 (465 nm) to B5 (475 nm)				Bulk
Blue	C5SMF-BJS-CR0U0352	550	2130	B3	460	B5	475	Ammo
Blue	C5SMF-BJS-CR0U0452	550	2130	B4	465	B5	475	Ammo
Blue	C5SMF-BJS-CR14Q3T2	Any 4 consecutive sub-bins: R1 (550) - S2 (934)		Any 1 color bin from B3 (460 nm) to B4 (470 nm)				Ammo
Blue	C5SMF-BJS-CR14Q4T2	Any 4 consecutive sub-bins: R1 (550) - S2 (934)		Any 1 color bin from B4 (465 nm) to B5 (475 nm)				Ammo
Blue	C5SMF-BJS-CR24Q4T2	Any 4 consecutive sub-bins: R2 (605) - S3 (1017)		Any 1 color bin from B4 (465 nm) to B5 (475 nm)				Ammo
Blue	C5SMF-BJS-CS24Q3T2	Any 4 consecutive sub-bins: S2 (852) - T3 (1415)		Any 1 color bin from B3 (460 nm) to B4 (470 nm)				Ammo
Blue	C5SMF-BJS-CS24Q4T2	Any 4 consecutive sub-bins: S2 (852) - T3 (1415)		Any 1 color bin from B4 (465 nm) to B5 (475 nm)				Ammo
Blue	C5SMF-BJS-CT14Q3T2	Any 4 consecutive sub-bins: T1 (1100) - U2 (1824)		Any 1 color bin from B3 (460 nm) to B4 (470 nm)				Ammo
Blue	C5SMF-BJS-CT14Q4T2	Any 4 consecutive sub-bins: T1 (1100) - U2 (1824)		Any 1 color bin from B4 (465 nm) to B5 (475 nm)				Ammo

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Order Code Table*

C5SME

Color	Kit Number	Luminous Intensity (mcd)		Dominant Wavelength				Pack-age
		Min.	Max.	Color Bin	Min.(nm)	Color Bin	Max.(nm)	
Red	C5SME-RJS-CS0U0BB1	770	2130	RB	619	RB	624	Bulk
Red	C5SME-RJS-CS14QBB1	Any 4 consecutive sub-bins: S1 (770) - T2 (1310)		RB	619	RB	624	Bulk
Red	C5SME-RJS-CS34QBB1	Any 4 consecutive sub-bins: S3 (934) - T4 (1520)		RB	619	RB	624	Bulk
Red	C5SME-RJS-CT14QBB1	Any 4 consecutive sub-bins: T1 (1100) - U2 (1824)		RB	619	RB	624	Bulk
Red	C5SME-RJS-CS0U0BB2	770	2130	RB	619	RB	624	Ammo
Red	C5SME-RJS-CS14QBB2	Any 4 consecutive sub-bins: S1 (770) - T2 (1310)		RB	619	RB	624	Ammo
Red	C5SME-RJS-CS34QBB2	Any 4 consecutive sub-bins: S3 (934) - T4 (1520)		RB	619	RB	624	Ammo
Red	C5SME-RJS-CT14QBB2	Any 4 consecutive sub-bins: T1 (1100) - U2 (1824)		RB	619	RB	624	Ammo

Notes:

1. The above kit numbers represent order codes that include multiple intensity-bin and color-bin codes. Only one intensity-sub-bin code and one color-bin code will be shipped on each reel. Selected single intensity-bin, single color-bin codes will be orderable in certain quantities. For example, any four consecutive sub-bins from V1 to W2 mean only one intensity bin with four sub-bins of the following brightness ranges (V1-V4, V2-W1, V3-W2) will be shipped by Cree. For example, any one-color bin from G7 to G9 means only one color bin (G7 or G8 or G9) will be shipped by Cree.
2. Please refer to the "Cree LED Lamp Reliability Test Standards" document for reliability test conditions.
3. Please refer to the "Cree LED Lamp Soldering & Handling" document for information about how to use this LED product safely.

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Graphs

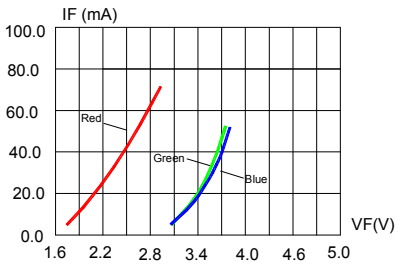

FIG.1 FORWARD CURRENT VS. FORWARD VOLTAGE.

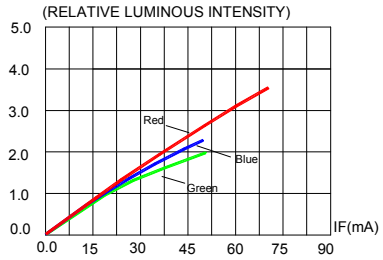

FIG.2 RELATIVE LUMINOUS INTENSITY VS. FORWARD CURRENT

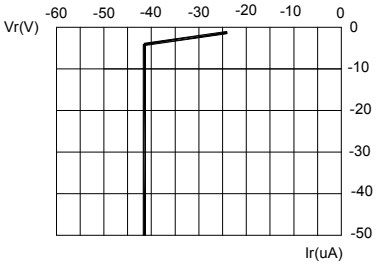

FIG.3a RED REVERSE CURRENT VS. REVERSE VOLTAGE.

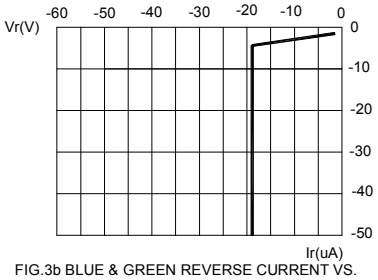

FIG.3b BLUE & GREEN REVERSE CURRENT VS. REVERSE VOLTAGE.

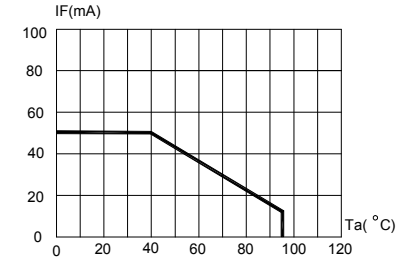

FIG.4a RED MAXIMUM FORWARD DC CURRENT VS AMBIENT TEMPERATURE (Tjmax=105°C)

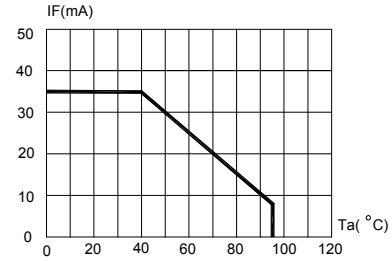

FIG.4b BLUE & GREEN MAXIMUM FORWARD DC CURRENT VS AMBIENT TEMPERATURE (Tjmax=105°C)

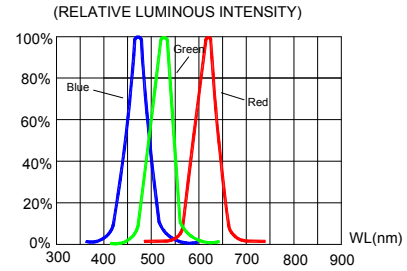

FIG.5 RELATIVE LUMINOUS INTENSITY VS. WAVELENGTH.

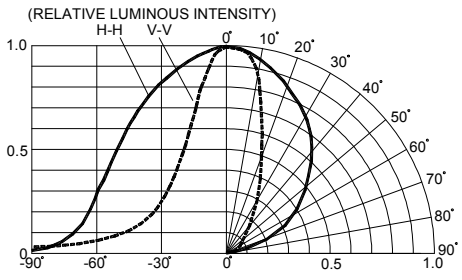

FIG.6 RED & BLUE&GREEN FAR FIELD PATTERN

The above data are collected from statistical figures that do not necessarily correspond to the actual parameters of each single LED. Hence, these data will be changed without further notice.

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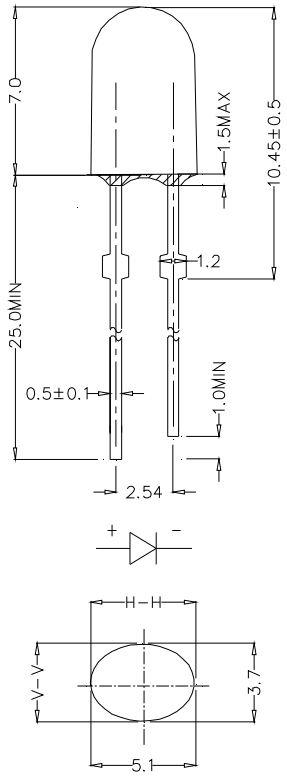
Mechanical Dimensions

All dimensions are in mm. Tolerance is ±0.25 mm unless otherwise noted.

An epoxy meniscus may extend about 1.5 mm down the leads.

Burr around bottom of epoxy may be 0.5 mm max.



Notes

RoHS Compliance

The levels of environmentally sensitive, persistent biologically toxic (PBT), persistent organic pollutants (POP), or otherwise restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS), as amended through April 21, 2006.

Vision Advisory Claim

Users should be cautioned not to stare at the light of this LED product. The bright light can damage the eye.

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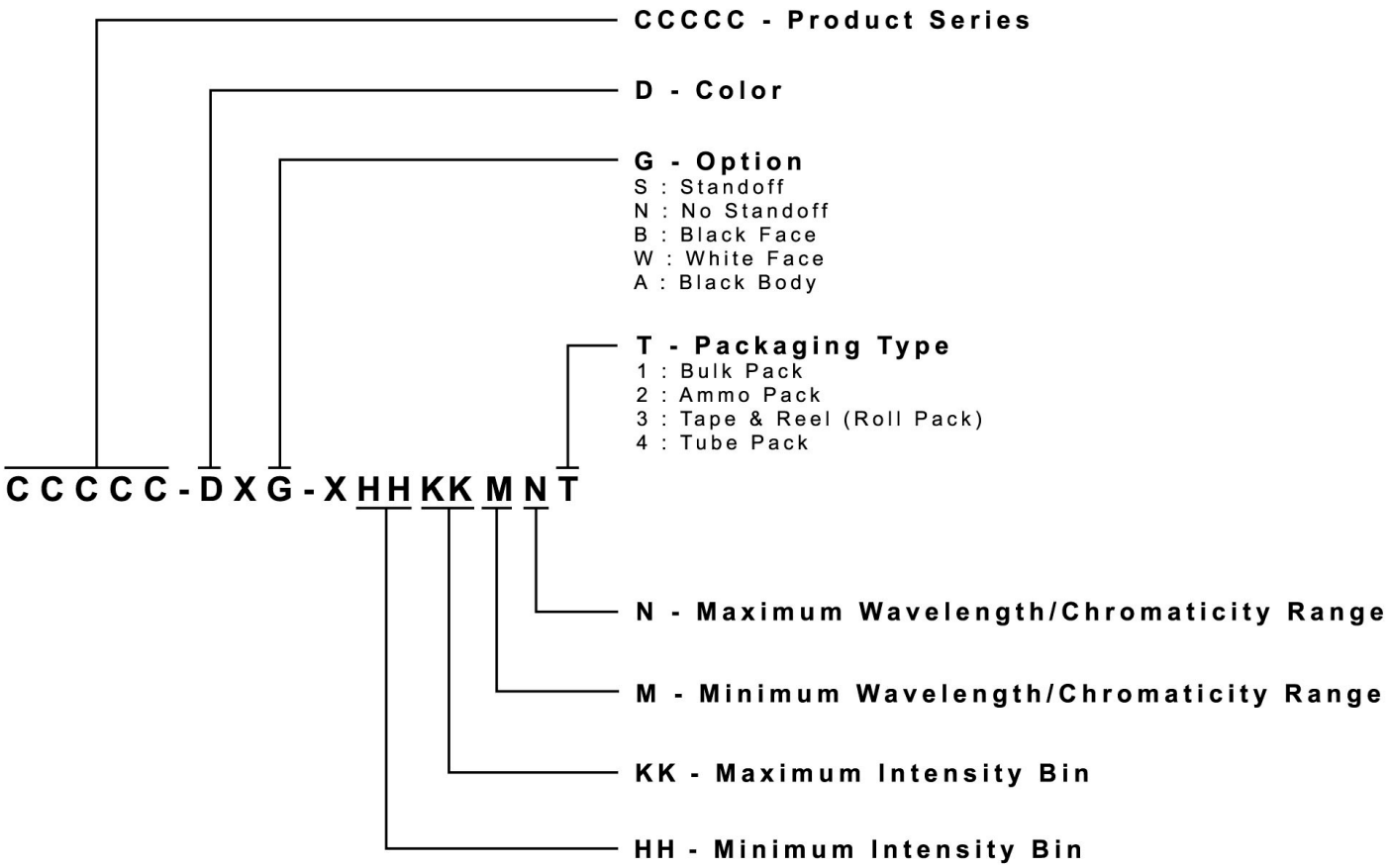
Kit Number System

Cree LED lamps are tested and sorted into performance bins. A bin is specified by ranges of color, forward voltage, and brightness. Sorted LEDs are packaged for shipping in various convenient options. Please refer to the "Cree LED Lamp Packaging Standard" document for more information about shipping and packaging options.

Cree LEDs are sold by order codes in combinations of bins called kits. Order codes are configured in the following manner:



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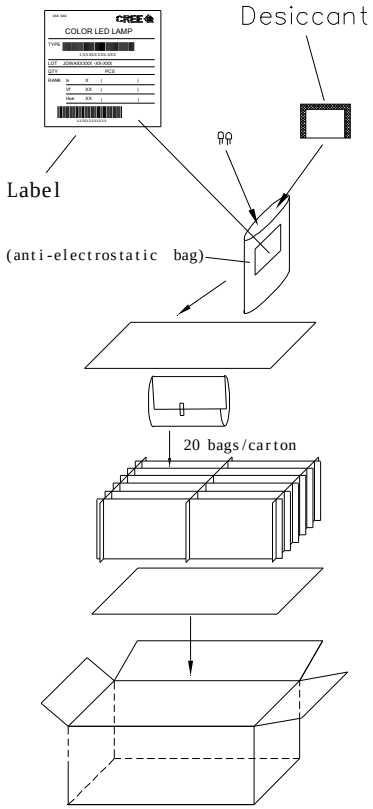
Package

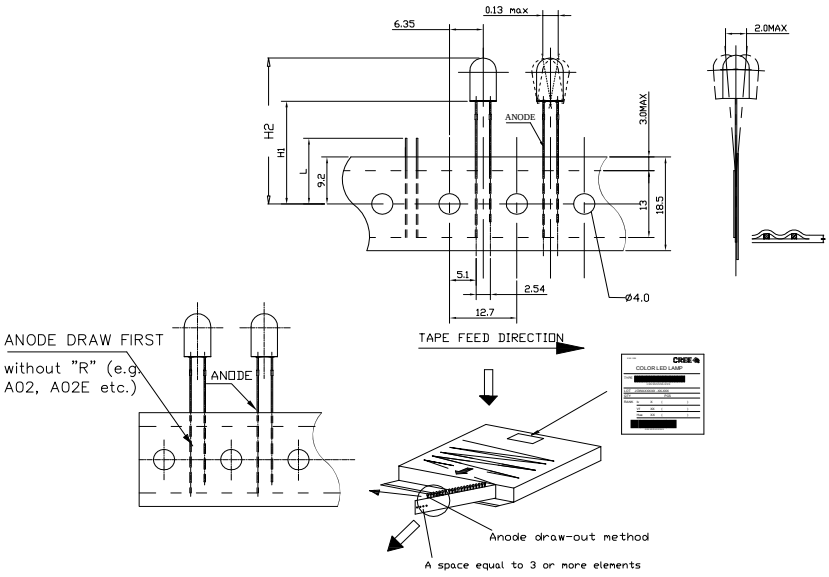
Features:

- The LEDs are packed in cardboard boxes after packaging in normal or anti-electrostatic bags.
- Cardboard boxes will be used to protect the LEDs from mechanical shock during transportation.
- The boxes are not water-resistant, and they must be kept away from water and moisture.
- There are two types of packaging: bulk pack and ammo pack.
- Max 500 pcs per bulk and max 2500 pcs per ammo.

Bulk Pack Packaging Type:



Ammo Pack Packaging Type:



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Fax: +1.919.313.5778
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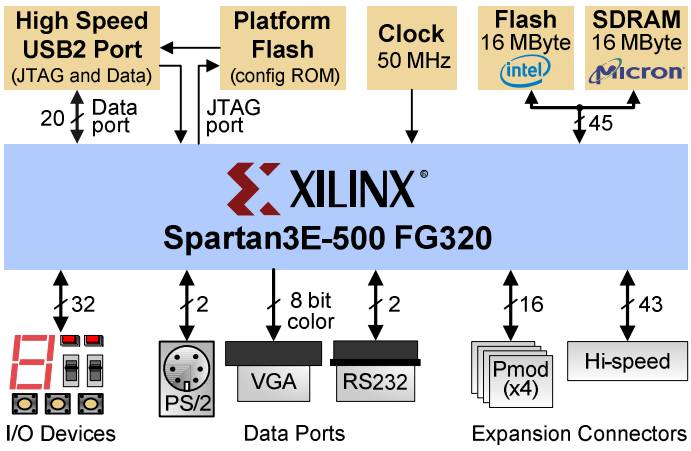
Digilent Nexys2 Board Reference Manual

Revision: June 21, 2008

www.digilentinc.com
215 E Main Suite D | Pullman, WA 99163
(509) 334 6306 Voice and Fax

Overview

The Nexys2 circuit board is a complete, ready-to-use circuit development platform based on a Xilinx Spartan 3E FPGA. Its on-board high-speed USB2 port, 16Mbytes of RAM and ROM, and several I/O devices and ports make it an ideal platform for digital systems of all kinds, including embedded processor systems based on Xilinx's MicroBlaze. The USB2 port provides board power and a programming interface, so the Nexys2 board can be used with a notebook computer to create a truly portable design station.



The Nexys2 brings leading technologies to a platform that anyone can use to gain digital design experience. It can host countless FPGA-based digital systems, and designs can easily grow beyond the board using any or all of the five expansion connectors. Four 12-pin Peripheral Module (Pmod) connectors can accommodate up to eight low-cost Pmods to add features like motor control, A/D and D/A conversion, audio circuits, and a host of sensor and actuator interfaces. All user-accessible signals on the Nexys2 board are ESD and short-circuit protected, ensuring a long operating life in any environment.

The Nexys2 board is fully compatible with all versions of the Xilinx ISE tools, including the free WebPack. Now anyone can build real digital systems for less than the price of a textbook.

- *500K-gate Xilinx Spartan 3E FPGA*
- *USB2-based FPGA configuration and high-speed data transfers (using the free Adept Suite Software)*
- *USB-powered (batteries and/or wall-plug can also be used)*
- *16MB of Micron PSDRAM &16MB of Intel StrataFlash ROM*
- *Xilinx Platform Flash for nonvolatile FPGA configurations*
- *Efficient switch-mode power supplies (good for battery powered applications)*
- *50MHz oscillator plus socket for second oscillator*
- *60 FPGA I/O's routed to expansion connectors (one high-speed Hirose FX2 connector and four 6-pin headers)*
- *8 LEDs, 4-digit 7-seg display, 4 buttons, 8 slide switches*
- *Ships in a plastic carry case with USB cable*

Figure 1: Nexys2 block diagram and features

Power Supplies

The Nexys2 board input power input bus can be driven from a USB cable, from a 5VDC-15VDC, center positive, 2.1mm wall-plug supply, or from a battery pack. A shorting block loaded on the "power select" jumper selects the power source. The USB circuitry is always powered from the USB cable – if no USB cable is attached, the USB circuitry is left unpowered.

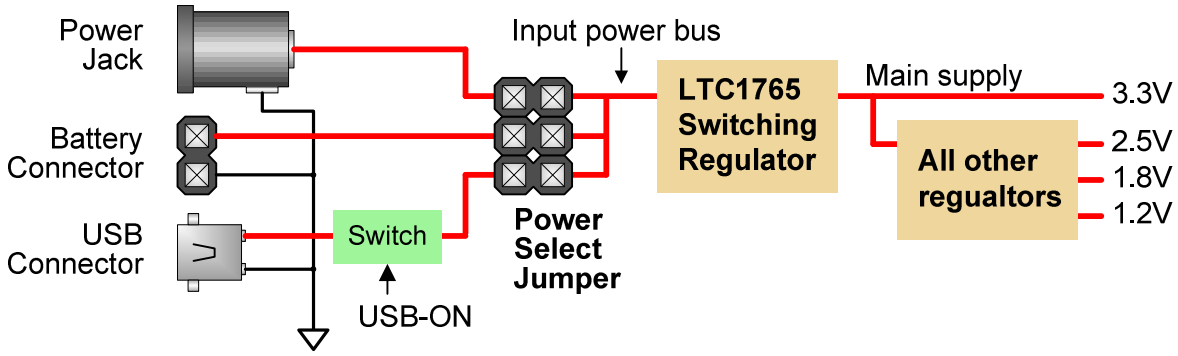


Figure 2: Nexys2 power supply block diagram

The input power bus drives a 3.3V voltage regulator that supplies all required board current. Some devices require 2.5V, 1.8V, and 1.2V supplies in addition to the main 3.3V supply, and these additional supplies are created by regulators that take their input from the main 3.3V supply. The primary supplies are generated by highly efficient switching regulators from Linear Technology. These regulators not only use USB power efficiently, they also allow the Nexys2 to run from battery packs for extended periods.

Total board current depends on the FPGA configuration, clock frequency, and external connections. In test circuits with roughly 20K gates routed, a 50MHz clock source, and all LEDs illuminated, about 200mA of current is drawn from the 1.2V supply, 50mA from the 2.5V supply, and 100mA from the 3.3V supply. Required current will increase if larger circuits are configured in the FPGA, and if peripheral boards are attached. The table above summarizes the power supply parameters.

The Nexys2 board can also receive power from (or deliver power to) a peripheral board connected to a Pmod connector or to the large 100-pin expansion connector. Jumpers near the Pmod connectors and large expansion connector (JP1 – JP5) can connect the Nexys2's input power bus to the connector's power pins. The Pmod jumpers can be used to route either the input power bus or regulated 3.3V to the Pmod power pins, while the expansion connector jumper can only make or break a connection with the input power bus.

USB power is supplied to the USB circuitry directly, but to the rest of the board through an electronic switch (Q1 in the Nexys2 schematic). The on-board USB controller turns on switch Q1 only after informing the host PC that

Table 1: Nexys2 Power Supplies

Supply	Device	Amps (max/typ)
3.3V main	IC6: LTC1765	3A/100mA
2.5V FPGA	IC7: LTC3417	1.4A/50mA
1.2V FPGA	IC7: LTC3417	1.4A/200mA
1.8V SRAM	IC8: LTC1844	150mA/90mA
3.3V USB	IC5: LTC1844	150mA/60mA

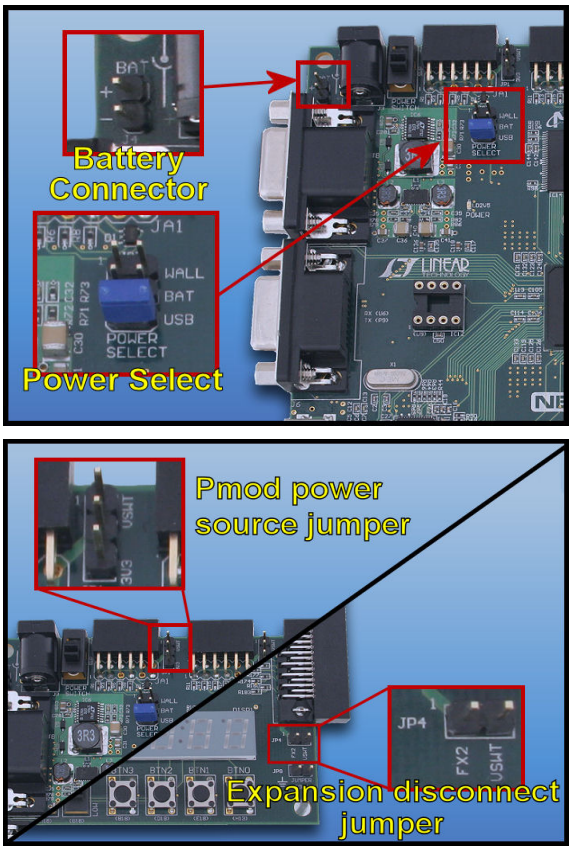


Figure 3: Nexys2 power supply jumpers

more than 100mA will be drawn through the USB cable (as required by the USB specification). A USB host can supply only 500mA of current at 5VDC. When using USB power, care must be taken to ensure the Nexys2 board and any attached peripheral boards do not draw more than 500mA, or damage to the host may result. The Nexys2 board typically consumes about 300mA of USB current, leaving about 200mA for peripheral boards. If peripheral boards require more current than the USB cable can supply, an external power supply should be used.

The Nexys2 board uses a six layer PCB, with the inner layers dedicated to VCC and GND planes. The FPGA and the other ICs on the board all have a large complement of bypass capacitors placed as close as possible to each VCC pin. The power supply routing and bypass capacitors result in a very clean, stable, and low-noise power supply.

FPGA and Platform Flash Configuration

The FPGA on the Nexys2 board must be configured (or programmed) by the user before it can perform any functions. During configuration, a "bit" file is transferred into memory cells within the FPGA to define the logical functions and circuit interconnects. The free ISE/WebPack CAD software from Xilinx can be used to create bit files from VHDL, Verilog, or schematic-based source files.

The FPGA can be programmed in two ways: directly from a PC using the on-board USB port, and from an on-board Platform Flash ROM (the Flash ROM is also user-programmable via the USB port). A jumper on the Nexys2 board determines which source (PC or ROM) the FPGA will use to load its configuration. The FPGA will automatically load a configuration from the Platform Flash ROM at power-on if the configuration Mode jumper is set to "Master serial". If the Mode jumper is set to "JTAG", the FPGA will await programming from the PC (via the USB cable).

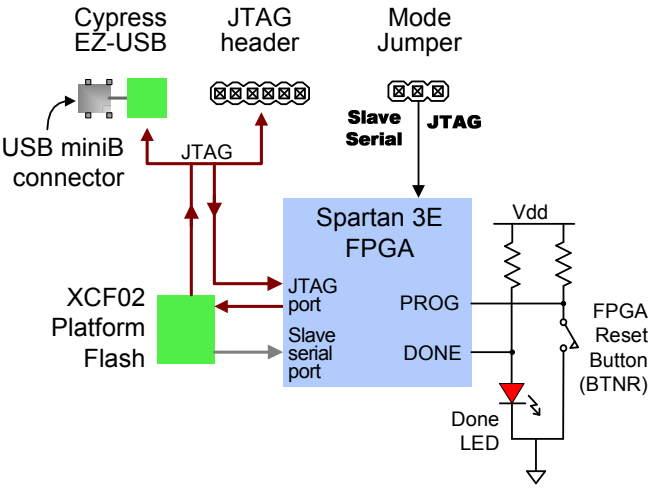


Figure 4: Nexys2 programming circuits

Digilent's freely available PC-based Adept software can be used to configure the FPGA and Platform Flash with any suitable file stored on the computer. Adept uses the USB cable to transfer a selected bit file from the PC to the FPGA or Platform Flash ROM. After the FPGA is configured, it will remain so until it is reset by a power-cycle event or by the FPGA reset button (BTNR) being pressed. The Platform Flash ROM will retain a bit file until it is reprogrammed, regardless of power-cycle events.

To program the Nexys2 board using Adept, attach the USB cable to the board (if USB power will not be used, attach a suitable power supply to the power jack or battery connector on the board, and set the power switch to "wall" or "bat"). Start the Adept software, and wait for the FPGA and the Platform Flash ROM to be recognized. Use the browse function to associate the desired .bit file with the FPGA, and/or the desired .mcs file with the Platform Flash ROM. Right-click on the device to be programmed, and select the "program" function. The configuration file will be sent to the FPGA or Platform Flash, and the software will indicate whether programming was successful. The configuration

"done" LED will illuminate after the FPGA has been successfully configured. For further information on using Adept, please see the Adept documentation available at the Digilent website.

The Nexys2 board can also be programmed using Xilinx's iMPACT software by connecting a suitable programming cable to the JTAG header. Digilent's JTAG3 cable or any other Xilinx cable may be used.

A demonstration configuration is loaded into the Platform Flash on the Nexys2 board during manufacturing. That configuration, also available on the Digilent webpage, can be used to check all of the devices and circuits on the Nexys2 board.

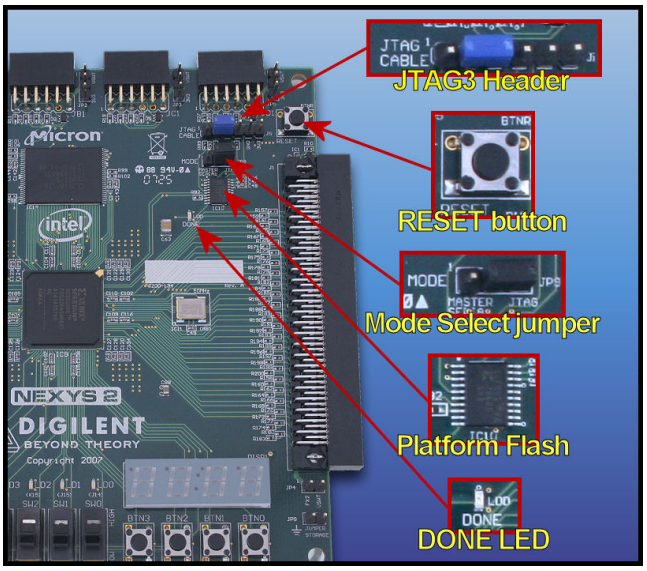


Figure 5: Nexys2 board programming circuits

Clocks

The Nexys2 board includes a 50MHz oscillator and a socket for a second oscillator. Clock signals from the oscillators connect to global clock input pins on the FPGA so they can drive the clock synthesizer blocks available in FPGA. The clock synthesizers (called DLLs, or delay locked loops) provide clock management capabilities that include doubling or quadrupling the input frequency, dividing the input frequency by any integer multiple, and defining precise phase and delay relationships between various clock signals.

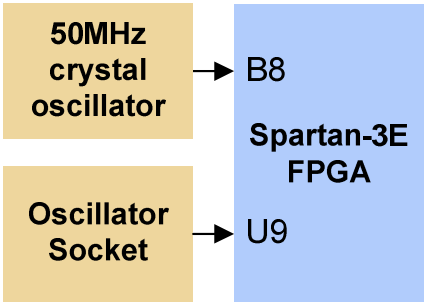


Figure 6: Nexys2 clocks

User I/O

The Nexys2 board includes several input devices, output devices, and data ports, allowing many designs to be implemented without the need for any other components.

Figure 7: Nexys2 board I/O devices

Inputs: Slide Switches and Pushbuttons

Four pushbuttons and eight slide switches are provided for circuit inputs. Pushbutton inputs are normally low, and they are driven high only when the pushbutton is pressed. Slide switches generate constant high or low inputs depending on their position. Pushbutton and slide switch inputs use a

series resistor for protection against short circuits (a short circuit would occur if an FPGA pin assigned to a pushbutton or slide switch was inadvertently defined as an output).

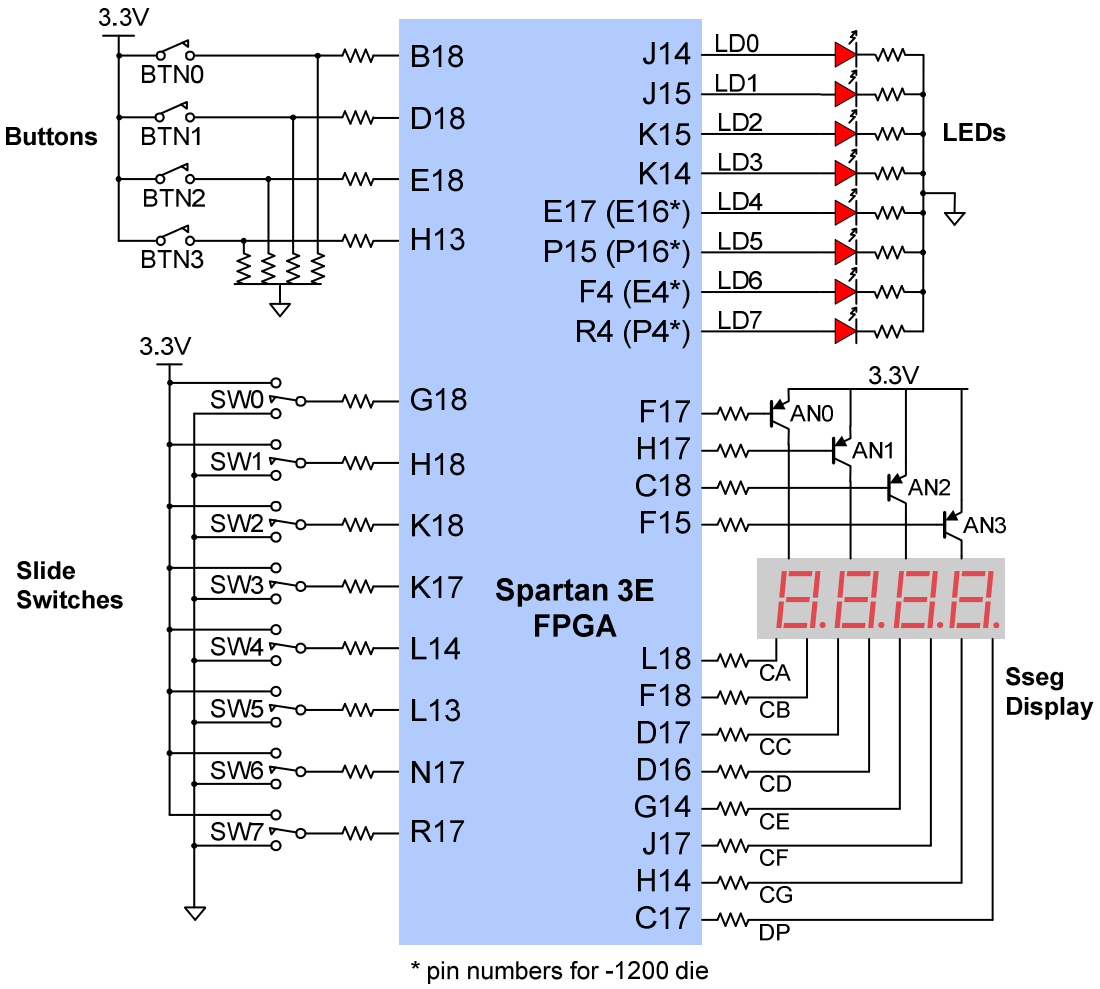


Figure 8: Nexys2 I/O devices and circuits

Outputs: LEDs

Eight LEDs are provided for circuit outputs. LED anodes are driven from the FPGA via 390-ohm resistors, so a logic '1' output will illuminate them with 3-4ma of drive current. A ninth LED is provided as a power-on LED, and a tenth LED indicates FPGA programming status. Note that LEDs 4-7 have different pin assignments due to pinout differences between the -500 and the -1200 die.

Outputs: Seven-Segment Display

The Nexys2 board contains a four-digit common anode seven-segment LED display. Each of the four digits is composed of seven segments arranged in a "figure 8" pattern, with an LED embedded in each segment. Segment LEDs can be individually illuminated, so any one of 128 patterns can be displayed on a digit by illuminating certain LED segments and leaving the others dark. Of these 128 possible patterns, the ten corresponding to the decimal digits are the most useful.

The anodes of the seven LEDs forming each digit are tied together into one “common anode” circuit node, but the LED cathodes remain separate. The common anode signals are available as four “digit enable” input signals to the 4-digit display. The cathodes of similar segments on all four displays are connected into seven circuit nodes labeled CA through CG (so, for example, the four “D” cathodes from the four digits are grouped together into a single circuit node called “CD”). These seven cathode signals are available as inputs to the 4-digit display. This signal connection scheme creates a multiplexed display, where the cathode signals are common to all digits but they can only illuminate the segments of the digit whose corresponding anode signal is asserted.

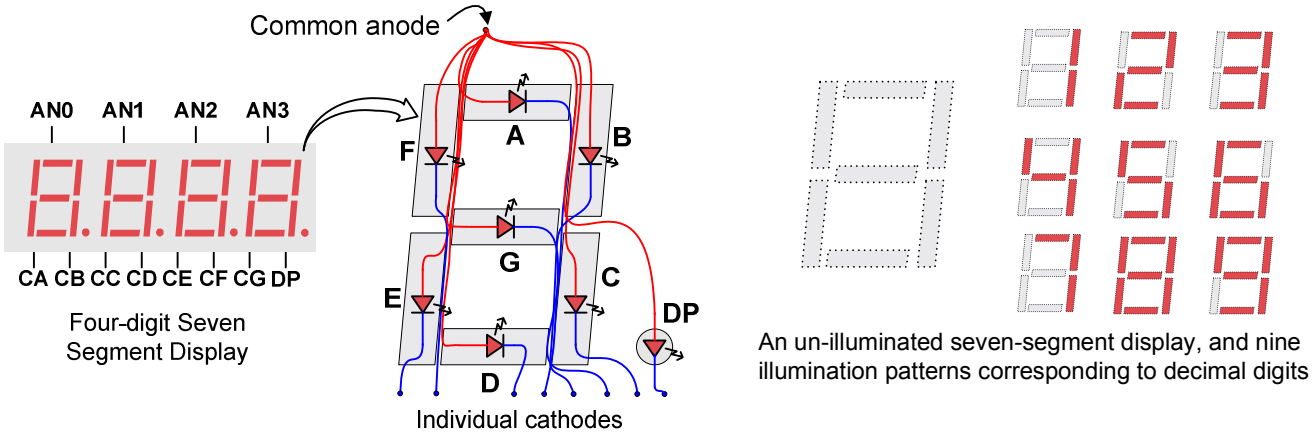


Figure 9: Nexys2 seven-segment displays

A scanning display controller circuit can be used to show a four-digit number on this display. This circuit drives the anode signals and corresponding cathode patterns of each digit in a repeating, continuous succession, at an update rate that is faster than the human eye can detect. Each digit is illuminated just one-quarter of the time, but because the eye cannot perceive the darkening of a digit before it is illuminated again, the digit appears continuously illuminated. If the update or “refresh” rate is slowed to around 45 hertz, most people will begin to see the display flicker.

In order for each of the four digits to appear bright and continuously illuminated, all four digits should be driven once every 1 to 16ms, for a refresh frequency of 1KHz to 60Hz. For example, in a 60Hz refresh scheme, the entire display would be refreshed once every 16ms, and each digit would be illuminated for ¼ of the refresh cycle, or 4ms. The controller must drive the cathodes with the correct pattern when the corresponding anode signal is driven. To illustrate the process, if AN0 is asserted while CB and CC are asserted, then a “1” will be displayed in digit position 1. Then, if AN1 is asserted while CA, CB and CC are asserted, then a “7” will be displayed in digit position 2. If AN0 and CB, CC are driven for 4ms, and then A1 and CA, CB, CC are driven for 4ms in an endless succession, the display will show “17” in the first two digits. An example timing diagram for a four-digit controller is provided.

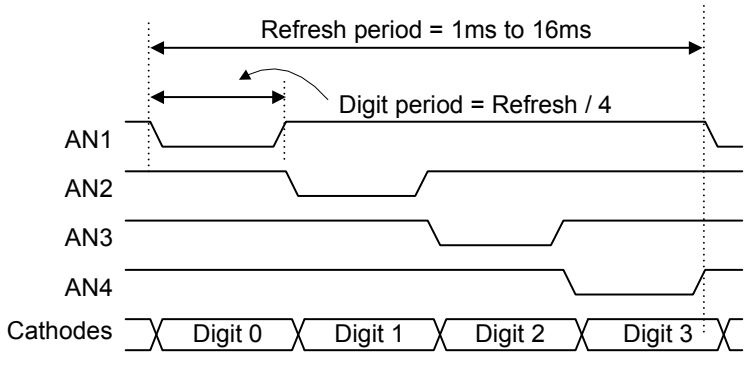


Figure 10: Seven-segment display timing diagram

USB Port

The Nexys2 includes a high-speed USB2 port based on a Cypress CY7C68013A USB controller. The USB port can be used to program the on-board Xilinx devices, to perform user-data transfers at up to 38Mbytes/sec, and to provide power to the board. Programming is accomplished with Digilent's free Adept Suite Software. User data transfers can also be accomplished using the Adept software, or custom user software can be written using Digilent's public API's to access the Nexys2 USB connection. Information on using Adept and/or the public API's to transfer data can be found on the Digilent website.

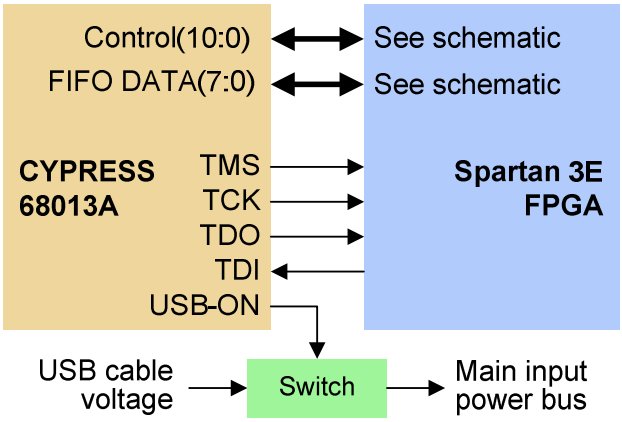


Figure 11: Nexys2 USB circuit

The USB port can also provide power to the Nexys2 board if the power select jumper is set to "USB". The USB specification requires that attached devices draw no more than 100mA until they have requested more current, after which up to 500mA may be drawn. When first attached to a USB host, the Nexys2 board requests 500mA, and then activates a transistor switch to connect the USB cable voltage to the main input power bus. The Nexys2 board typically draws around 300mA from the USB cable, and care should be taken (especially when using peripheral boards) to ensure that no more than 500mA is drawn.

PS/2 Port

The 6-pin mini-DIN connector can accommodate a PS/2 mouse or keyboard. Most PS/2 devices can operate from a 3.3V supply, but older devices may require a 5VDC supply. A three-pin jumper on the Nexys2 board immediately adjacent to the PS/2 connector selects whether regulated 3.3V or the main input power bus voltage (VU) is supplied to the PS/2 connector. To send 5V to the PS/2 connector, set the PS2 power jumper to Vswt (the main input power bus), and ensure the board is powered from USB or a 5VDC wall-plug supply. To send 3.3V to the connector, set the jumper to 3.3V.

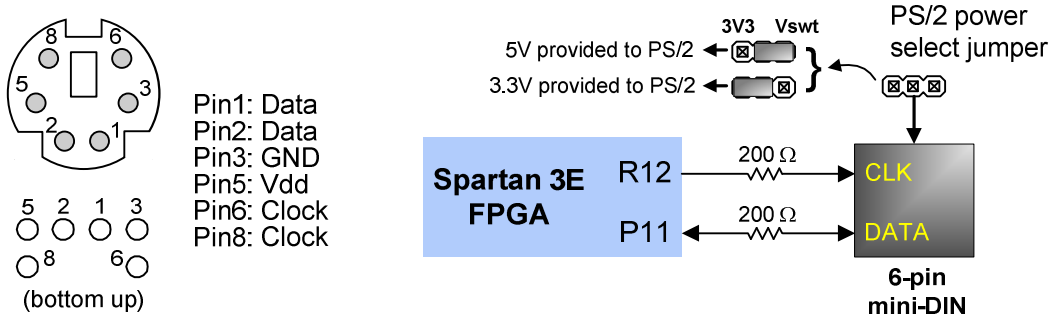
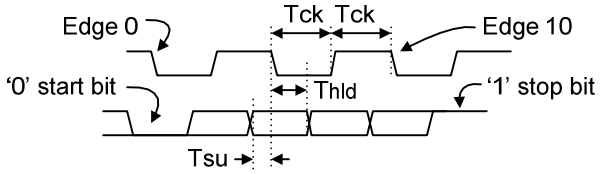


Figure 12: Nexys2 PS/2 circuits

Both the mouse and keyboard use a two-wire serial bus (clock and data) to communicate with a host device. Both use 11-bit words that include a start, stop and odd parity bit, but the data packets are organized differently, and the keyboard interface allows bi-directional data transfers (so the host

device can illuminate state LEDs on the keyboard). Bus timings are shown in the figure. The clock and data signals are only driven when data transfers occur, and otherwise they are held in the "idle" state at logic '1'. The timings define signal requirements for mouse-to-host communications and bi-directional keyboard communications. A PS/2 interface circuit can be implemented in the FPGA to create a keyboard or mouse interface.



Symbol	Parameter	Min	Max
T_{CK}	Clock time	30us	50us
T_{SU}	Data-to-clock setup time	5us	25us
T_{HLD}	Clock-to-data hold time	5us	25us

Figure 13: PS/2 signal timings

Keyboard

The keyboard uses open-collector drivers so the keyboard or an attached host device can drive the two-wire bus (if the host device will not send data to the keyboard, then the host can use input-only ports).

PS2-style keyboards use scan codes to communicate key press data. Each key is assigned a code that is sent whenever the key is pressed; if the key is held down, the scan code will be sent repeatedly about once every 100ms. When a key is released, a "F0" key-up code is sent, followed by the scan code of the released key. If a key can be "shifted" to produce a new character (like a capital letter), then a shift character is sent in addition to the scan code, and the host must determine which ASCII character to use. Some keys, called extended keys, send an "E0" ahead of the scan code (and they may send more than one scan code). When an extended key is released, an "E0 F0" key-up code is sent, followed by the scan code. Scan codes for most keys are shown in the figure. A host device can also send data to the keyboard. Below is a short list of some common commands a host might send.

ED Set Num Lock, Caps Lock, and Scroll Lock LEDs. Keyboard returns "FA" after receiving "ED", then host sends a byte to set LED status: Bit 0 sets Scroll Lock; bit 1 sets Num Lock; and Bit 2 sets Caps lock. Bits 3 to 7 are ignored.
EE Echo (test). Keyboard returns "EE" after receiving "EE".
F3 Set scan code repeat rate. Keyboard returns "F3" on receiving "FA", then host sends second byte to set the repeat rate.
FE Resend. "FE" directs keyboard to re-send most recent scan code.
FF Reset. Resets the keyboard.

The keyboard can send data to the host only when both the data and clock lines are high (or idle). Since the host is the "bus master", the keyboard must check to see whether the host is sending data before driving the bus. To facilitate this, the clock line is used as a "clear to send" signal. If the host pulls the clock line low, the keyboard must not send any data until the clock is released. The keyboard sends data to the host in 11-bit words that contain a '0' start bit, followed by 8-bits of scan code (LSB first), followed by an odd parity bit and terminated with a '1' stop bit. The keyboard generates 11 clock transitions (at around 20 - 30KHz) when the data is sent, and data is valid on the falling edge of the clock.

Scan codes for most PS/2 keys are shown in the figure below.

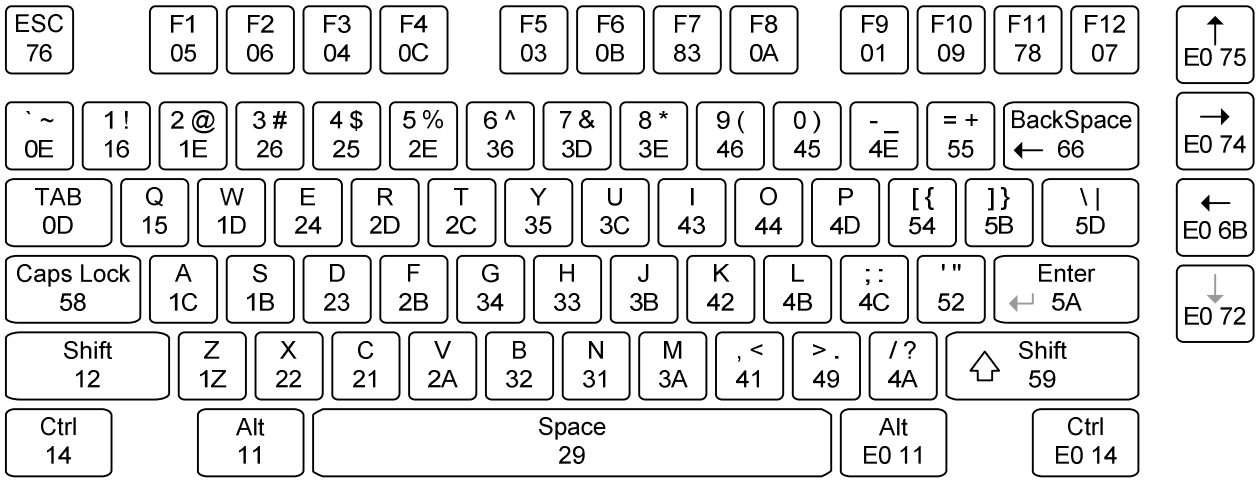


Figure 14: PS/2 keyboard scan codes

Mouse

The mouse outputs a clock and data signal when it is moved; otherwise, these signals remain at logic '1'. Each time the mouse is moved, three 11-bit words are sent from the mouse to the host device. Each of the 11-bit words contains a '0' start bit, followed by 8 bits of data (LSB first), followed by an odd parity bit, and terminated with a '1' stop bit. Thus, each data transmission contains 33 bits, where bits 0, 11, and 22 are '0' start bits, and bits 11, 21, and 33 are '1' stop bits. The three 8-bit data fields contain movement data as shown in the figure above. Data is valid at the falling edge of the clock, and the clock period is 20 to 30KHz.

The mouse assumes a relative coordinate system wherein moving the mouse to the right generates a positive number in the X field, and moving to the left generates a negative number. Likewise, moving the mouse up generates a positive number in the Y field, and moving down represents a negative number (the XS and YS bits in the status byte are the sign bits – a '1' indicates a negative number). The magnitude of the X and Y numbers represent the rate of mouse movement – the larger the number, the faster the mouse is moving (the XV and YV bits in the status byte are movement overflow indicators – a '1' means overflow has occurred). If the mouse moves continuously, the 33-bit transmissions are repeated every 50ms or so. The L and R fields in the status byte indicate Left and Right button presses (a '1' indicates the button is being pressed).

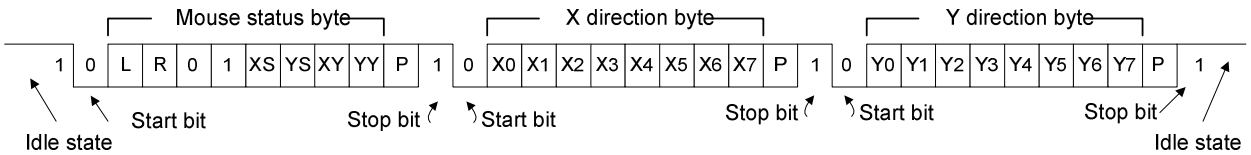


Figure 15: Mouse data format

VGA Port

The Nexys2 board uses 10 FPGA signals to create a VGA port with 8-bit color and the two standard sync signals (HS – Horizontal Sync, and VS – Vertical Sync). The color signals use resistor-divider circuits that work in conjunction with the 75-ohm termination resistance of the VGA display to create eight signal levels on the red and green VGA signals, and four on blue (the human eye is less sensitive to blue levels). This circuit, shown in figure 13, produces video color signals that proceed in equal increments between 0V (fully off) and 0.7V (fully on). Using this circuit, 256 different colors can be displayed, one for each unique 8-bit pattern. A video controller circuit must be created in the FPGA to drive the sync and color signals with the correct timing in order to produce a working display system.

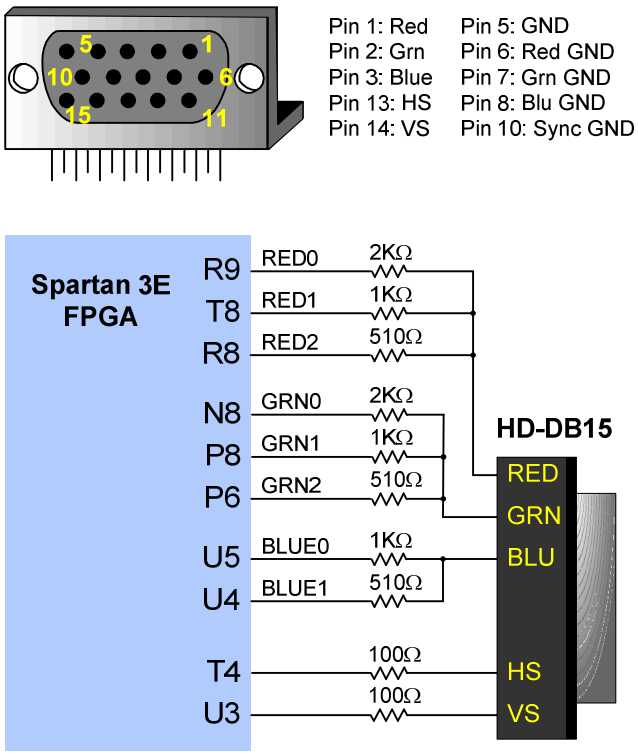


Figure 16: VGA pin definitions and Nexys2 circuit

VGA System Timing

VGA signal timings are specified, published, copyrighted and sold by the VESA organization (www.vesa.org). The following VGA system timing information is provided as an example of how a VGA monitor might be driven in 640 by 480 mode. For more precise information, or for information on other VGA frequencies, refer to documentation available at the VESA website.

CRT-based VGA displays use amplitude-modulated moving electron beams (or cathode rays) to display information on a phosphor-coated screen. LCD displays use an array of switches that can impose a voltage across a small amount of liquid crystal, thereby changing light permittivity through the crystal on a pixel-by-pixel basis. Although the following description is limited to CRT displays, LCD displays have evolved to use the same signal timings as CRT displays (so the "signals" discussion below pertains to both CRTs and LCDs). Color CRT displays use three electron beams (one for red, one for blue, and one for green) to energize the phosphor that coats the inner side of the display end of a cathode ray tube (see illustration). Electron beams emanate from "electron guns" which are finely-pointed heated cathodes placed in close proximity to a positively charged annular plate called a "grid". The electrostatic force imposed by the grid pulls rays of energized electrons

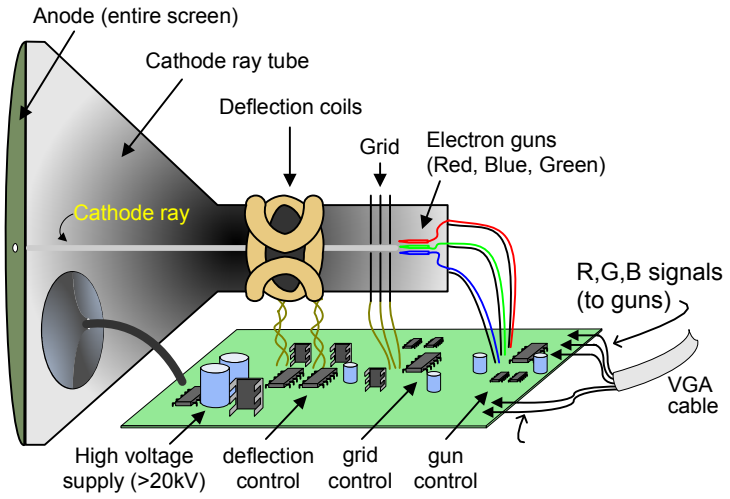


Figure 17: CRT deflection system

from the cathodes, and those rays are fed by the current that flows into the cathodes. These particle rays are initially accelerated towards the grid, but they soon fall under the influence of the much larger electrostatic force that results from the entire phosphor-coated display surface of the CRT being charged to 20kV (or more). The rays are focused to a fine beam as they pass through the center of the grids, and then they accelerate to impact on the phosphor-coated display surface. The phosphor surface glows brightly at the impact point, and it continues to glow for several hundred microseconds after the beam is removed. The larger the current fed into the cathode, the brighter the phosphor will glow.

Between the grid and the display surface, the beam passes through the neck of the CRT where two coils of wire produce orthogonal electromagnetic fields. Because cathode rays are composed of charged particles (electrons), they can be deflected by these magnetic fields. Current waveforms are passed through the coils to produce magnetic fields that interact with the cathode rays and cause them to transverse the display surface in a “raster” pattern, horizontally from left to right and vertically from top to bottom. As the cathode ray moves over the surface of the display, the current sent to the electron guns can be increased or decreased to change the brightness of the display at the cathode ray impact point.

Information is only displayed when the beam is moving in the “forward” direction (left to right and top to bottom), and not during the time the beam is reset back to the left or top edge of the display. Much of the potential display time is therefore lost in “blanking” periods when the beam is reset and stabilized to begin a new horizontal or vertical display pass. The size of the beams, the frequency at which the beam can be traced across the display, and the frequency at which the electron beam can be modulated determine the display resolution. Modern VGA displays can accommodate different resolutions, and a VGA controller circuit dictates the resolution by producing timing signals to control the raster patterns. The controller must produce synchronizing pulses at 3.3V (or 5V) to set the frequency at which current flows through the deflection coils, and it must ensure that video data is applied to the electron guns at the correct time. Raster video displays define a number of “rows” that corresponds to the number of horizontal passes the cathode makes over the display area, and a number of “columns” that corresponds to an area on each row that is assigned to one “picture element” or pixel. Typical displays use from 240 to 1200 rows and from 320 to 1600 columns. The overall size of a display and the number of rows and columns determines the size of each pixel.

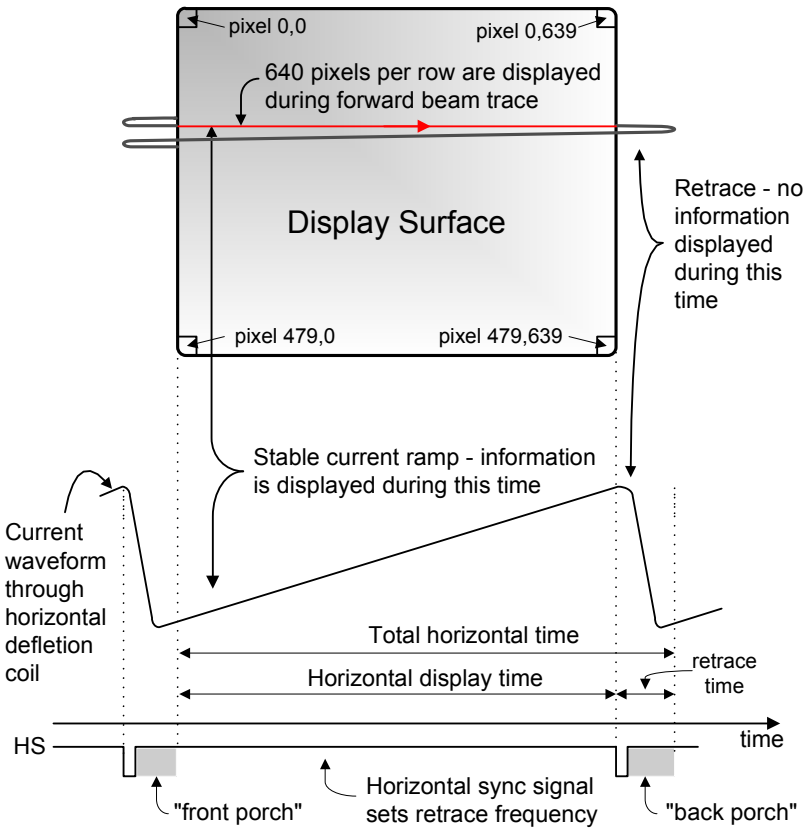
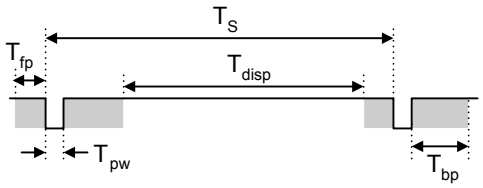


Figure 18: VGA system signals

Video data typically comes from a video refresh memory, with one or

more bytes assigned to each pixel location (the Nexys2 uses three bits per pixel). The controller must index into video memory as the beams move across the display, and retrieve and apply video data to the display at precisely the time the electron beam is moving across a given pixel.

A VGA controller circuit must generate the HS and VS timings signals and coordinate the delivery of video data based on the pixel clock. The pixel clock defines the time available to display one pixel of information. The VS signal defines the "refresh" frequency of the display, or the frequency at which all information on the display is redrawn. The minimum refresh frequency is a function of the display's phosphor and electron beam intensity, with practical refresh frequencies falling in the 50Hz to 120Hz range. The number of lines to be displayed at a given refresh frequency defines the horizontal "retrace" frequency. For a 640-pixel by 480-row display using a 25MHz pixel clock and 60 +/-1Hz refresh, the signal timings shown in the table at right can be derived. Timings for sync pulse width and front and back porch intervals (porch intervals are the pre- and post-sync pulse times during which information cannot be displayed) are based on observations taken from actual VGA displays.



Symbol	Parameter	Vertical Sync			Horiz. Sync	
		Time	Clocks	Lines	Time	Clks
T_S	Sync pulse	16.7ms	416,800	521	32 us	800
T_{disp}	Display time	15.36ms	384,000	480	25.6 us	640
T_{pw}	Pulse width	64 us	1,600	2	3.84 us	96
T_{fp}	Front porch	320 us	8,000	10	640 ns	16
T_{bp}	Back porch	928 us	23,200	29	1.92 us	48

Figure 19: VGA system timings for 640x480 display

A VGA controller circuit decodes the output of a horizontal-sync counter driven by the pixel clock to generate HS signal timings. This counter can be used to locate any pixel location on a given row. Likewise, the output of a vertical-sync counter that increments with each HS pulse can be used to generate VS signal timings, and this counter can be used to locate any given row. These two continually running counters can be used to form an address into video RAM. No time relationship between the onset of the HS pulse and the onset of the VS pulse is specified, so the designer can arrange the counters to easily form video RAM addresses, or to minimize decoding logic for sync pulse generation.

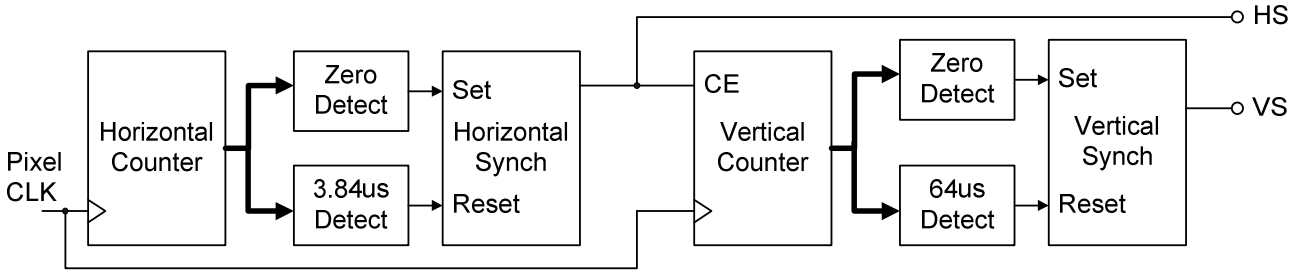


Figure 20: Schematic for a VGA controller circuit

Serial Port

The Nexys2 contains a two-wire serial port based on an ST Microelectronics ST3232 voltage converter. The ST3232 converts the signal levels used by RS-232 communications (-12 to -3 for a logic '1' and 12V to 3V for a logic '0') to the 3.3V signals used by the FPGA. Since only two signals are connected (RXD and TXD), an FPGA-based serial port controller can only use software hand-shaking protocols (XON/XOFF). The Nexys2 serial port is useful for many applications, and in particular for debugging and working with Xilinx's MicroBlaze embedded processor.

The two devices connected to either end of a serial cable are known as the Data Terminal Equipment (DTE) and the Data Communications Equipment (DCE). The DCE was originally conceived to be a modem, but now many devices connect to a computer as a DCE. A DTE "source" device uses a male DB-9 connector, and a DCE "peripheral" device uses a female DB-9 connector. Two DTE devices can be connected via a serial cable only if lines two and three (RXD and TXD) are crossed, producing what is known as a null modem cable. A DTE and DCE device can be connected with a straight-through cable. The Nexys2 is configured as a DCE device, with the assumption it will most typically be connected to a DTE device like a computer.

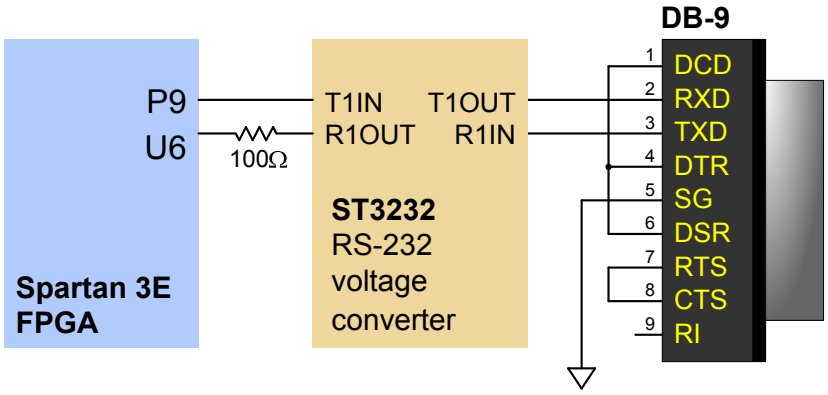


Figure 21: Nexys2 serial port circuit

Memory

The Nexys2 board has external RAM and ROM devices. The external RAM is a 128Mbit Micron M45W8MW16 Cellular RAM pseudo-static DRAM device organized as 8Mbytes x 16bits. It can operate as a typical asynchronous SRAM with read and write cycle times of 70ns, or as a synchronous memory with an 80MHz bus. When operated as an asynchronous SRAM, the Cellular RAM automatically refreshes its internal DRAM arrays, allowing for a simplified memory controller design (similar to any SRAM) in the FPGA. When operated in synchronous mode, continuous transfers of up to 80MHz are possible.

The external ROM is a 128Mbit Intel TE28F128J3D75-110 StrataFlash device organized as 8Mbytes x 16bits. Internally, it contains 128 blocks that can be individually erased, and it supports 110ns read cycle times, with 25ns page-mode reads within blocks. It has an internal 32-byte write buffer that can be written with 70ns cycle times, and the 32-byte buffer can be transferred to the Flash array in 218us (typical).

Both devices share a common 16-bit data bus and 24-bit address bus. The Cellular RAM is byte addressable using the upper-byte and lower-byte signals (MT-UB and MT-LB), but the StrataFlash is configured for 16 byte operations only (it is not byte addressable). The output enable (OE) and write enable (WE) signals are shared by both devices, but each device has individual chip enable (CE) signals. Additionally, the Cellular RAM has clock (MT-CLK), wait (MT-WAIT), address valid (MT-ADV) and control register enable (MT_CRE) signals available to the FPGA for use with synchronous transfers, and the StrataFlash has Reset (RP#) and status (STS) signals routed to the FPGA.

VDHL source code is available in a reference design posted on the Digilent website to illustrate the use of these devices. A base system builder file is also available for using these devices with Xilinx's EDK tool and MicroBlaze processor core, both available from Xilinx. Complete information is available for both devices from the manufacturer websites.

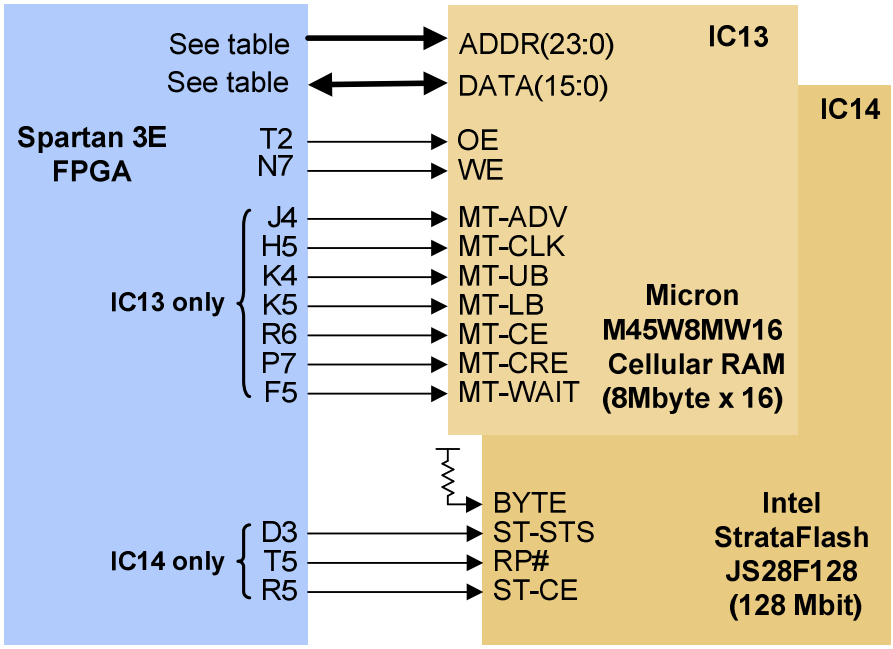


Figure 22: Nexys2 memory circuits

Table 2: Memory Address and Data Bus Pin Assignments				
Address signals			Data signals	
ADDR0: NA	ADDR8: H6	ADDR16: M5	DATA0: L1	DATA8: L3
ADDR1: J1	ADDR9: F1	ADDR17: E2	DATA1: L4	DATA9: L5
ADDR2: J2	ADDR10: G3	ADDR18: C2	DATA2: L6	DATA10: M3
ADDR3: H4	ADDR11: G6	ADDR19: C1	DATA3: M4	DATA11: M6
ADDR4: H1	ADDR12: G5	ADDR20: D2	DATA4: N5	DATA12: L2
ADDR5: H2	ADDR13: G4	ADDR21: K3	DATA5: P1	DATA13: N4
ADDR6: J5	ADDR14: F2	ADDR22: D1	DATA6: P2	DATA14: R3
ADDR7: H3	ADDR15: E1	ADDR23: K6	DATA7: R2	DATA15: T1

Peripheral Connectors

The Nexys2 board provides four two-row 6-pin Pmod connectors that together can accommodate up to 8 Pmods. The four 12-pin connectors each have 8 data signals, two GND pins, and two Vdd pins. All data signals include short circuit protection resistors and ESD protection Diodes. A jumper block adjacent to each Pmod connector can connect the Pmod's Vdd signal to the Nexys2 board's 3.3V supply or to the input power bus (VU). If the jumper is set to VU and USB power is driving the main power bus, care should be taken to ensure no more than 200mA is consumed by the Pmod. Further, if the jumper is set to VU, a voltage source connected to the Pmod can drive the main power bus of the Nexys2 board, so care should be taken to avoid connecting conflicting power supplies.

The Pmod connectors are labeled JA (nearest the power jack), JB, JC, and JD (nearest the expansion connector). Pinouts for the Pmod connectors are provided in the table below.

More than 30 low-cost are available for attachment to these connectors. Pmods can either be attached directly, or by using a small cable. Available Pmods include A/D and D/A converters, motor drivers, speaker amplifiers, distance measuring devices, etc. Please see www.digilentinc.com for more information.

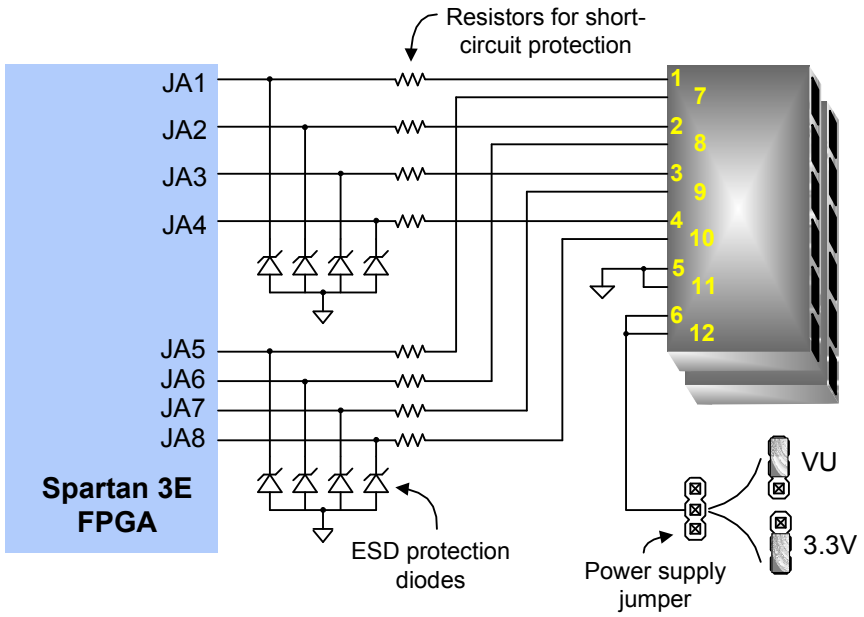


Figure 23: Nexys2 Pmod connector circuits

Table 3: Nexys2 Pmod Connector Pin Assignments							
Pmod JA		**Pmod JB**		**Pmod JC**		**Pmod JD**	
JA1: L15	JA7: K13	JB1: M13	JB7: P17	JC1: G15	JC7: H15	JD1: J13	JD7: K14[1]
JA2: K12	JA8: L16	JB2: R18	JB8: R16	JC2: J16	JC8: F14	JD2: M18	JD8: K15[2]
JA3: L17	JA9: M14	JB3: R15	JB9: T18	JC3: G13	JC9: G16	JD3: N18	JD9: J15[3]
JA4: M15	JA10: M16	JB4: T17	JB10: U18	JC4: H16	JC10: J12	JD4:; P18	JD10: J14[4]

Notes: [1] shared with LD3 [2] shared with LD3 [3] shared with LD3 [4] shared with LD3

Expansion connector

The Nexys2 board includes a Hirose FX-2 high-density 100 pin connector that is suitable for driving peripheral boards with signal rates in excess of 100 MHz. Many connector signals are routed to the FPGA as differential pairs, and 47 connector pins are tied to ground, resulting in a very low-noise connection system. The self-aligning Hirose FX-2 connector can be used for board-to-board connections or board-to-cable connections using the mating Hirose FX2-100S-1.27 available from many catalog distributors and directly from Digilent.

All signals routed from the FPGA to the FX-2 connector include 75-ohm series resistors. The table on the right shows all signal connections between the FX-2 connector and the FPGA. Signals without corresponding entries in the FPGA column are not directly connected to the FPGA.

Table 4: Hirose FX2 Connector Pin Assignments

J1A	Name	FPGA	J1B	Name	FPGA
1	VCC3V3		1	SHIELD	
2	VCC3V3		2	GND	
3	TMS	D15	3	TDO-ROM	
4	JTSEL		4	TCK	A17
5	TDO-FX2		5	GND	
6	FX2-IO1	B4	6	GND	
7	FX2-IO2	A4	7	GND	
8	FX2-IO3	C3	8	GND	
9	FX2-IO4	C4	9	GND	
10	FX2-IO5	B6	10	GND	
11	FX2-IO6	D5	11	GND	
12	FX2-IO7	C5	12	GND	
13	FX2-IO8	F7	13	GND	
14	FX2-IO9	E7	14	GND	
15	FX2-IO10	A6	15	GND	
16	FX2-IO11	C7	16	GND	
17	FX2-IO12	F8	17	GND	
18	FX2-IO13	D7	18	GND	
19	FX2-IO14	E8	19	GND	
20	FX2-IO15	E9	20	GND	
21	FX2-IO16	C9	21	GND	
22	FX2-IO17	A8	22	GND	
23	FX2-IO18	G9	23	GND	
24	FX2-IO19	F9	24	GND	
25	FX2-IO20	D10	25	GND	
26	FX2-IO21	A10	26	GND	
27	FX2-IO22	B10	27	GND	
28	FX2-IO23	A11	28	GND	
29	FX2-IO24	D11	29	GND	
30	FX2-IO25	E10	30	GND	
31	FX2-IO26	B11	31	GND	
32	FX2-IO27	C11	32	GND	
33	FX2-IO28	E11	33	GND	
34	FX2-IO29	F11	34	GND	
35	FX2-IO30	E12	35	GND	
36	FX2-IO31	F12	36	GND	
37	FX2-IO32	A13	37	GND	
38	FX2-IO33	B13	38	GND	
39	FX2-IO34	E13	39	GND	
40	FX2-IO35	A14	40	GND	
41	FX2-IO36	C14	41	GND	
42	FX2-IO37	D14	42	GND	
43	FX2-IO38	B14	43	GND	
44	FX2-IO39	A16	44	GND	
45	FX2-IO40	B16	45	GND	
46	GND		46	FX2-CLKIN	B9
47	FX2-CLKOUT	D9	47	GND	
48	GND		48	FX2-CLKIO	M9
49	VCCFX2		49	VCCFX2	
50	VCCFX2		50	SHIELD	

Built in Self Test

A demonstration configuration is loaded into the Platform Flash ROM on the Nexys2 board during manufacturing. This demo, also available on the resource CD and on the Digilent website, can serve as a board verification test since it interacts with all devices and ports on the board. To configure the FPGA from a bit file stored in Platform Flash, set the Mode Jumper to Slave Serial and cycle power or press the FPGA reset button.

The self-test checks the on-board memories, and then connects the switches to the LEDs, the buttons and PS/2 keyboard (if attached) to the seven-segment display, and a VGA monitor (if attached) will show a color pattern. If the on-board memories pass test, “PASS” will be displayed on the seven-segment display (otherwise, “FAIL”). After the memory test, the buttons and switches will drive the LEDs and seven-segment display, so that all user I/O devices can be manually checked.

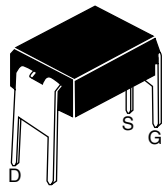
If the self test is not resident in the Platform Flash ROM, it can be programmed into the FPGA or reloaded into the ROM using the Adept programming software.

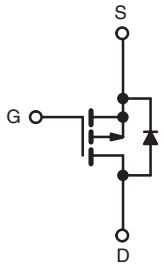
All Nexys2 boards are 100% tested during the manufacturing process. If any device on the Nexys2 board fails test or is not responding properly, it is likely that damage occurred during transport or during use. Typical damage includes stressed solder joints, or contaminants in switches and buttons resulting in intermittent failures. Stressed solder joints can be repaired by reheating and reflowing solder, and contaminants can be cleaned with off-the-shelf electronics cleaning products. If a board fails test within the warranty period, it will be replaced at no cost. If a board fails test outside of the warranty period and cannot be easily repaired, Digilent can repair the board or offer a discounted replacement. Contact Digilent for more details.

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	- 200	
$R_{DS(on)}$ (Ω)	V_{GS} = - 10 V	3.0
Q_g (Max.) (nC)	8.9	
Q_{gs} (nC)	2.1	
Q_{gd} (nC)	3.9	
Configuration	Single	

HVMDIP





P-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- P-Channel
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC

Available
RoHS* COMPLIANT

DESCRIPTION

The Power MOSFETs technology is the key to Vishay advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design archieve very low on-state resistance combined with high transconductance and extreme device ruggedness.
The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRFD9210PbF
	SiHFD9210-E3
SnPb	IRFD9210
	SiHFD9210

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

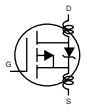
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 200	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	T_C = 25 °C	I_D	- 0.40	A
		T_C = 100 °C		- 0.25	
Pulsed Drain Current[a]			I_{DM}	- 3.2	
Linear Derating Factor				0.0083	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	210	mJ
Repetitive Avalanche Current[a]			I_{AR}	- 0.40	A
Repetitive Avalanche Energy[a]			E_{AR}	0.10	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	1.0	W
Peak Diode Recovery dV/dt[c]			dV/dt	- 5.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = - 50 V, starting T_J = 25 °C, L = 123 mH, R_g = 25 Ω, I_{AS} = - 1.6 A (see fig. 12).
c. I_{SD} ≤ - 2.3 A, dI/dt ≤ 70 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = - 1 mA	-	- 0.23	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 200 V, V_{GS} = 0 V	-	-	- 100	µA
		V_{DS} = - 160 V, V_{GS} = 0 V, T_J = 125 °C	-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 0.24 A[b]	-	-	3.0	Ω
Forward Transconductance	g_{fs}	V_{DS} = - 50 V, I_D = - 0.24 A	0.27	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1.0 MHz, see fig. 5	-	170	-	pF
Output Capacitance	C_{oss}		-	54	-	
Reverse Transfer Capacitance	C_{rss}		-	16	-	
Total Gate Charge	Q_g	V_{GS} = - 10 V, I_D = - 1.3 A, V_{DS} = - 160 V, see fig. 6 and 13[b]	-	-	8.9	nC
Gate-Source Charge	Q_{gs}		-	-	2.1	
Gate-Drain Charge	Q_{gd}		-	-	3.9	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 100 V, I_D = - 2.3 A, R_g = 24 Ω, R_D = 41 Ω, see fig. 10[b]	-	8.0	-	ns
Rise Time	t_r		-	12	-	
Turn-Off Delay Time	$t_{d(off)}$		-	11	-	
Fall Time	t_f		-	13	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.0	-	nH
Internal Source Inductance	L_S		-	6.0	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	- 0.40	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	- 3.2	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = - 0.40 A, V_{GS} = 0 V[b]	-	-	- 5.8	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = - 2.3 A, dI/dt = 100 A/µs[b]	-	110	220	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.56	1.1	µC

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

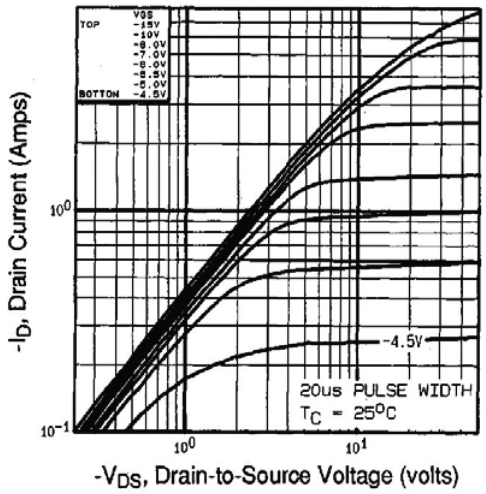


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

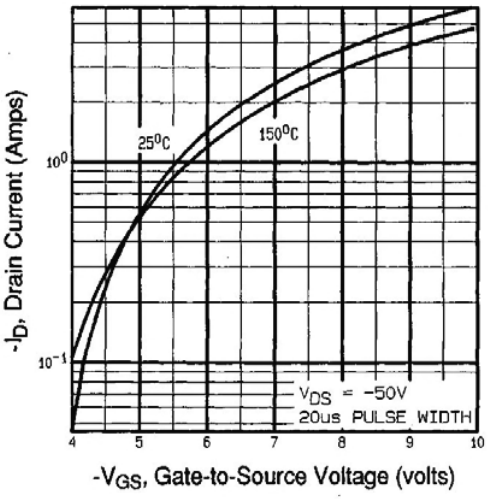


Fig. 3 - Typical Transfer Characteristics

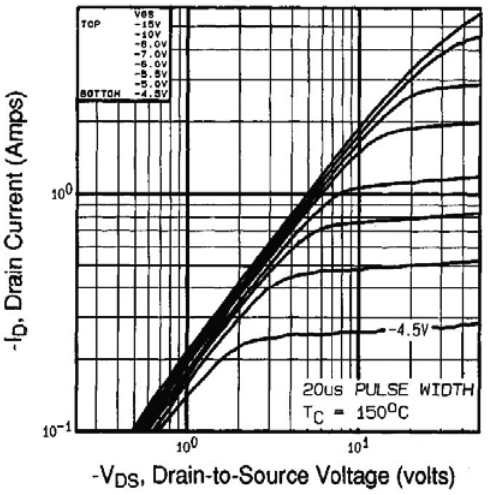


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

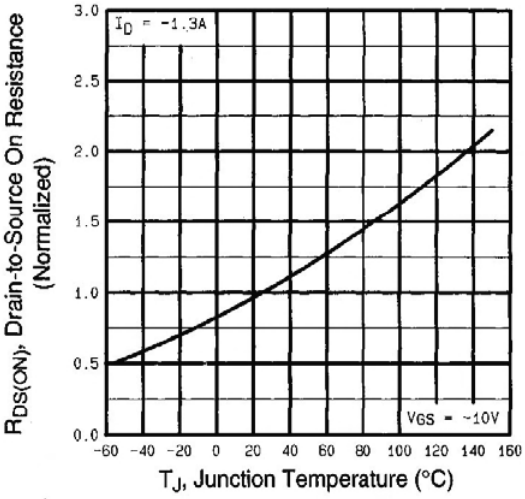


Fig. 4 - Normalized On-Resistance vs. Temperature

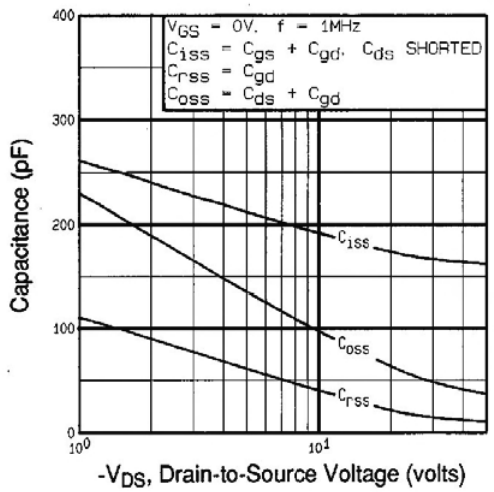


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

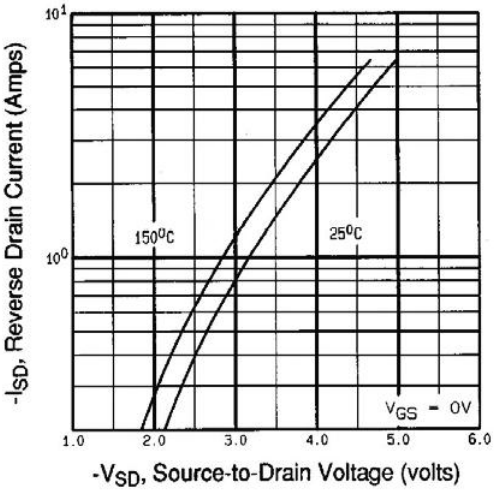


Fig. 7 - Typical Source-Drain Diode Forward Voltage

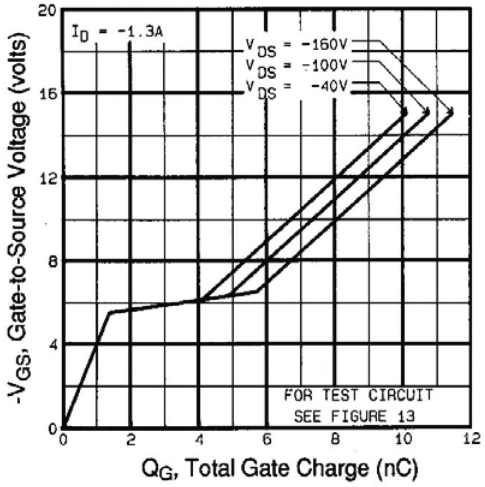


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

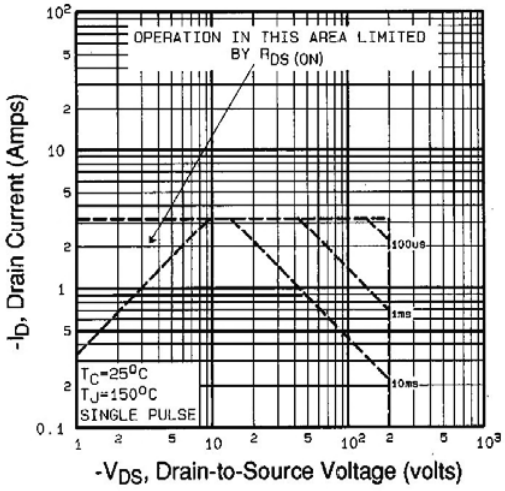


Fig. 8 - Maximum Safe Operating Area

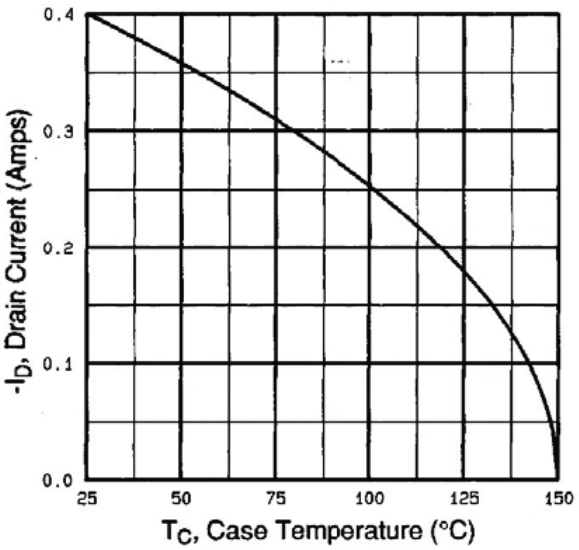


Fig. 9 - Maximum Drain Current vs. Case Temperature

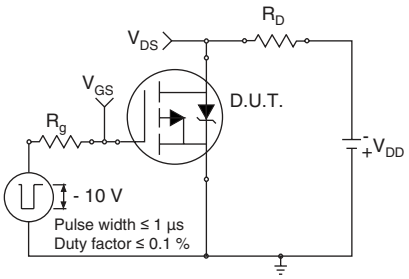


Fig. 10a - Switching Time Test Circuit

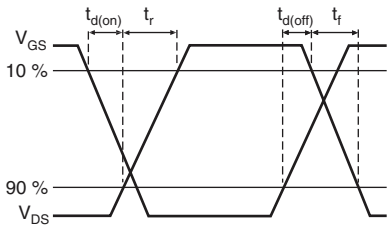


Fig. 10b - Switching Time Waveforms

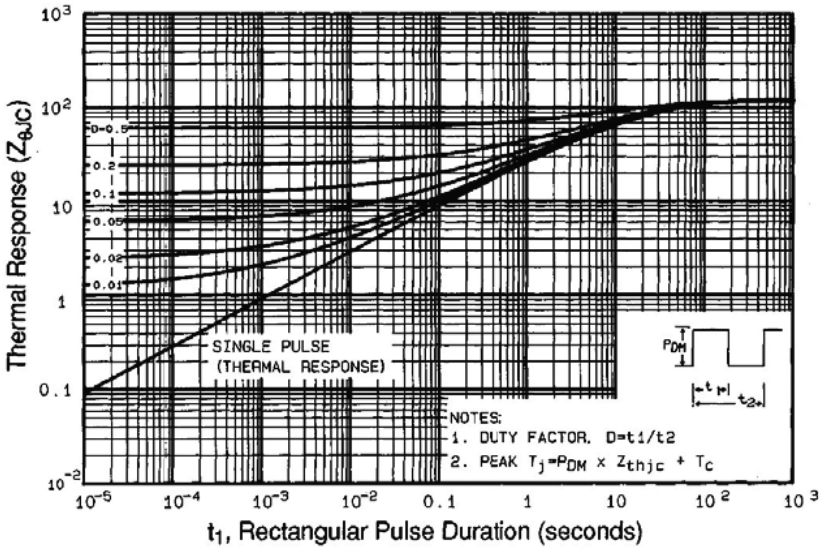


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

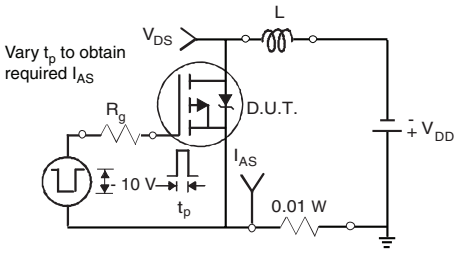


Fig. 12a - Unclamped Inductive Test Circuit

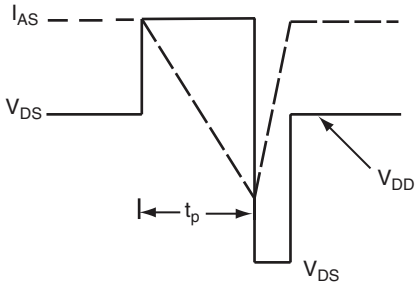


Fig. 12b - Unclamped Inductive Waveforms

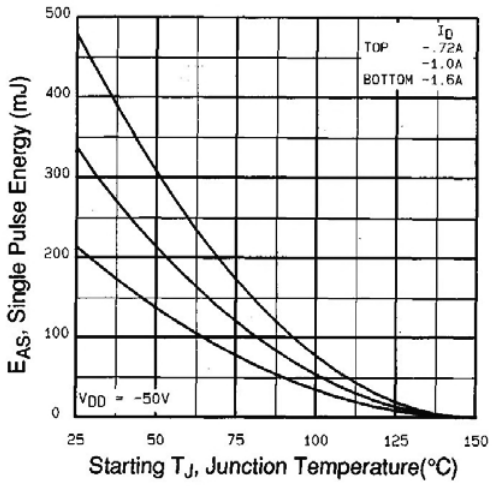


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

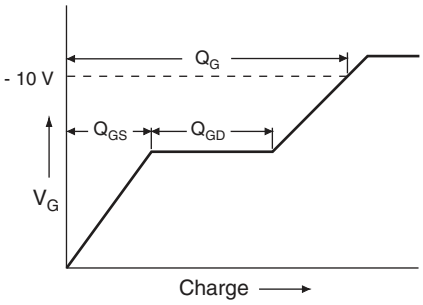


Fig. 13a - Basic Gate Charge Waveform

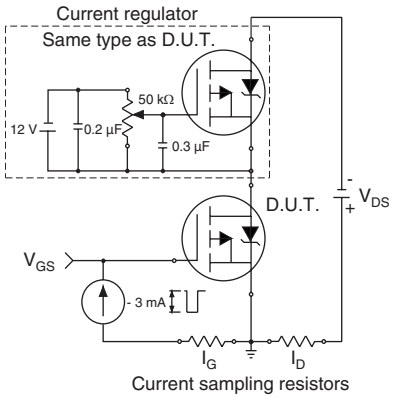
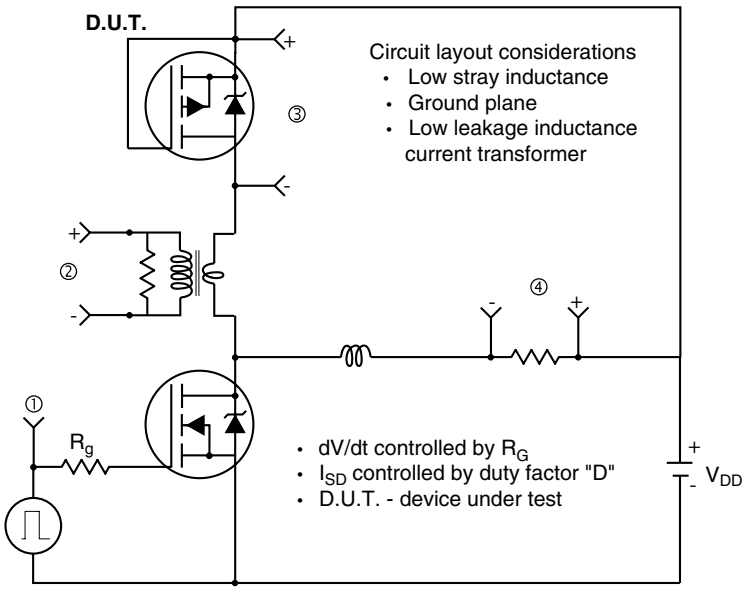
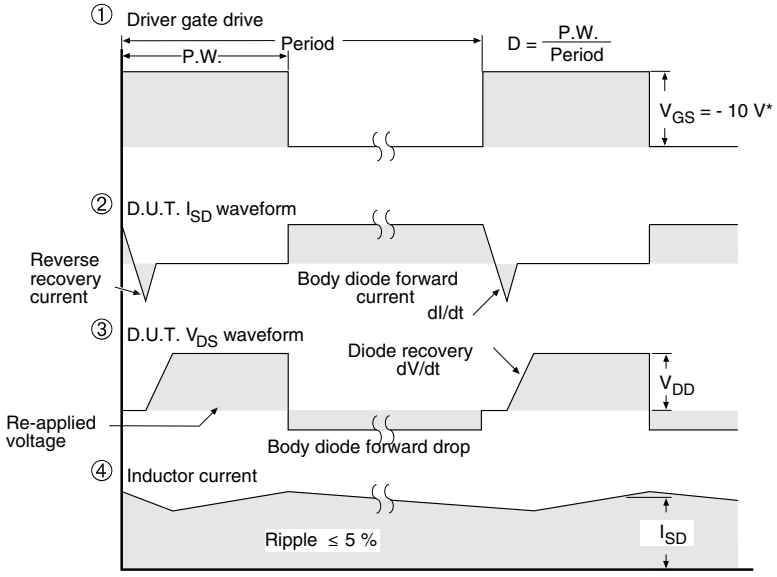


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 14 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91140.

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National Semiconductor

July 2006

LM340/LM78XX Series 3-Terminal Positive Regulators

General Description

The LM140/LM340A/LM340/LM78XXC monolithic 3-terminal positive voltage regulators employ internal current-limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1.0A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

Considerable effort was expended to make the entire series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

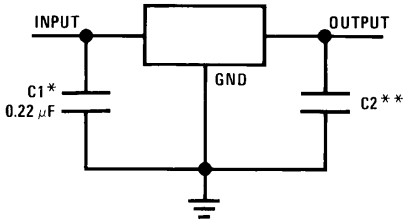
The 5V, 12V, and 15V regulator options are available in the steel TO-3 power package. The LM340A/LM340/LM78XXC series is available in the TO-220 plastic power package, and the LM340-5.0 is available in the SOT-223 package, as well as the LM340-5.0 and LM340-12 in the surface-mount TO-263 package.

Features

- Complete specifications at 1A load
- Output voltage tolerances of ±2% at T_j = 25˚C and ±4% over the temperature range (LM340A)
- Line regulation of 0.01% of V_{OUT}/V of ΔV_{IN} at 1A load (LM340A)
- Load regulation of 0.3% of V_{OUT}/A (LM340A)
- Internal thermal overload protection
- Internal short-circuit current limit
- Output transistor safe area protection
- P^+ Product Enhancement tested

Typical Applications

Fixed Output Regulator

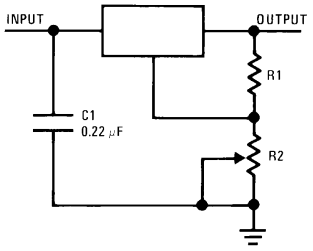


00778101

*Required if the regulator is located far from the power supply filter.

**Although no output capacitor is needed for stability, it does help transient response. (If needed, use 0.1 µF, ceramic disc).

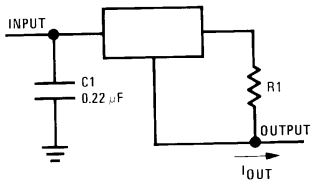
Adjustable Output Regulator



00778102

V_{OUT} = 5V + (5V/R1 + I_Q) R2 5V/R1 > 3 I_Q,
load regulation (L_r) ≈ [(R1 + R2)/R1] (L_r of LM340-5).

Current Regulator

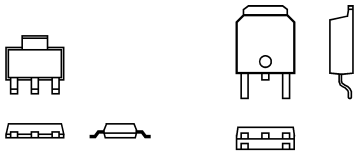


00778103

$$I_{OUT} = \frac{V2\text{-}3}{R1} + I_Q$$

ΔI_Q = 1.3 mA over line and load changes.

Comparison between SOT-223 and D-Pak (TO-252) Packages



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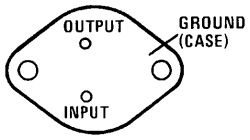
Scale 1:1

Ordering Information

Package	Temperature Range	Part Number	Packaging Marking	Transport Media	NSC Drawing
3-Lead TO-3	-55˚C to +125˚C	LM140K-5.0	LM140K 5.0P+	50 Per Tray	K02A
		LM140K-12	LM140K 12P+	50 Per Tray	
		LM140K-15	LM140K 15P+	50 Per Tray	
	0˚C to +125˚C	LM340K-5.0	LM340K 5.0 7805P+	50 Per Tray	
		LM340K-12	LM340K 12 7812P+	50 Per Tray	
		LM340K-15	LM340K 15 7815P+	50 Per Tray	
3-lead TO-220	0˚C to +125˚C	LM340AT-5.0	LM340AT 5.0 P+	45 Units/Rail	T03B
		LM340T-5.0	LM340T5 7805 P+	45 Units/Rail	
		LM340T-12	LM340T12 7812 P+	45 Units/Rail	
		LM340T-15	LM340T15 7815 P+	45 Units/Rail	
		LM7808CT	LM7808CT	45 Units/Rail	
3-Lead TO-263	0˚C to +125˚C	LM340S-5.0	LM340S-5.0 P+	45 Units/Rail	TS3B
		LM340SX-5.0		500 Units Tape and Reel	
		LM340S-12	LM340S-12 P+	45 Units/Rail	
		LM340SX-12		500 Units Tape and Reel	
		LM340AS-5.0	LM340AS-5.0 P+	45 Units/Rail	
		LM340ASX-5.0		500 Units Tape and Reel	
4-Lead SOT-223	0˚C to +125˚C	LM340MP-5.0	N00A	1k Units Tape and Reel	MP04A
		LM340MPX-5.0		2k Units Tape and Reel	
Unpackaged Die	–55˚C to 125˚C	LM140KG-5 MD8		Waffle Pack or Gel Pack	DL069089
		LM140KG-12 MD8		Waffle Pack or Gel Pack	DL059093
		LM140KG-15 MD8		Waffle Pack or Gel Pack	DL059093
	0˚C to +125˚C	LM340-5.0 MDA		Waffle Pack or Gel Pack	DI074056
		LM7808C MDC		Waffle Pack or Gel Pack	DI074056

Connection Diagrams

TO-3 Metal Can Package (K)



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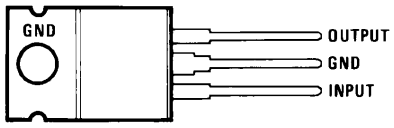
Bottom View
See Package Number K02A

TO-220 Power Package (T)



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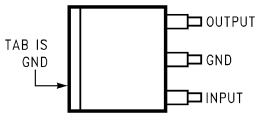
Top View
See Package Number T03B

TO-263 Surface-Mount Package (S)



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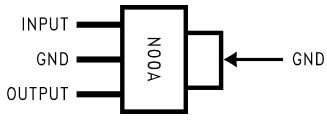
Top View
See Package Number TS3B

3-Lead SOT-223



00778143

Top View
See Package Number MP04A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 5)

DC Input Voltage	35V
Internal Power Dissipation (Note 2)	Internally Limited
Maximum Junction Temperature	150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 10 sec.)	
TO-3 Package (K)	300˚C
TO-220 Package (T), TO-263 Package (S)	230˚C
ESD Susceptibility (Note 3)	2 kV

Operating Conditions (Note 1)

Temperature Range (T_A) (Note 2)	
LM140	−55˚C to +125˚C
LM340A, LM340	0˚C to +125˚C
LM7808C	0˚C to +125˚C

LM340A Electrical Characteristics

I_{OUT} = 1A, 0˚C ≤ T_J ≤ + 125˚C (LM340A) unless otherwise specified (Note 4)

Symbol	Output Voltage		5V			12V			15V			Units
	Input Voltage (unless otherwise noted)		10V			19V			23V			
	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	T_J = 25˚C	4.9	5	5.1	11.75	12	12.25	14.7	15	15.3	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A	4.8		5.2	11.5		12.5	14.4		15.6	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
ΔV_O	Line Regulation	I_O = 500 mA			10			18			22	mV
		ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
		T_J = 25˚C		3	10		4	18		4	22	mV
		ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
		T_J = 25˚C			4			9			10	mV
		Over Temperature			12			30			30	mV
		ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
ΔV_O	Load Regulation	T_J = 25˚C, 5 mA ≤ I_O ≤ 1.5A		10	25		12	32		12	35	mV
		T_J = 25˚C, 250 mA ≤ I_O ≤ 750 mA			15			19			21	mV
		Over Temperature, 5 mA ≤ I_O ≤ 1A			25			60			75	mV
I_Q	Quiescent Current	T_J = 25˚C			6			6			6	mA
		Over Temperature			6.5			6.5			6.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A		0.5			0.5			0.5		mA
		T_J = 25˚C, I_O = 1A			0.8			0.8			0.8	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
		I_O = 500 mA			0.8			0.8			0.8	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(8 ≤ V_{IN} ≤ 25)			(15 ≤ V_{IN} ≤ 30)			(17.9 ≤ V_{IN} ≤ 30)			V
V_N	Output Noise Voltage	T_A = 25˚C, 10 Hz ≤ f ≤ 100 kHz		40			75			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	T_J = 25˚C, f = 120 Hz, I_O = 1A	68	80		61	72		60	70		dB
		or f = 120 Hz, I_O = 500 mA, Over Temperature,	68			61			60			dB
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	T_J = 25˚C, I_O = 1A		2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz		8			18			19		mΩ
	Short-Circuit Current	T_J = 25˚C		2.1			1.5			1.2		A

LM340A Electrical Characteristics (Continued)

I_{OUT} = 1A, 0˚C ≤ T_J ≤ + 125˚C (LM340A) unless otherwise specified (Note 4)

Symbol	Output Voltage		5V			12V			15V			Units
	Input Voltage (unless otherwise noted)		10V			19V			23V			
	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Peak Output Current	T_J = 25˚C		2.4			2.4			2.4		A
	Average TC of V_O	Min, T_J = 0˚C, I_O = 5 mA		−0.6			−1.5			−1.8		mV/˚C
V_{IN}	Input Voltage Required to Maintain Line Regulation	T_J = 25˚C	7.5			14.5			17.5			V

LM140 Electrical Characteristics (Note 4)

−55˚C ≤ T_J ≤ +150˚C unless otherwise specified

Symbol	Output Voltage			5V			12V			15V			Units
	Input Voltage (unless otherwise noted)			10V			19V			23V			
	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	T_J = 25˚C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A V_{MIN} ≤ V_{IN} ≤ V_{MAX}		4.75 (8 ≤ V_{IN} ≤ 20)		5.25	11.4 (15.5 ≤ V_{IN} ≤ 27)		12.6	14.25 (18.5 ≤ V_{IN} ≤ 30)		15.75	V V
ΔV_O	Line Regulation	I_O = 500 mA	T_J = 25˚C ΔV_{IN}		3 (7 ≤ V_{IN} ≤ 25)	50		4 (14.5 ≤ V_{IN} ≤ 30)	120		4 (17.5 ≤ V_{IN} ≤ 30)	150	mV V
			−55˚C ≤ T_J ≤ +150˚C ΔV_{IN}			50 (8 ≤ V_{IN} ≤ 20)			120 (15 ≤ V_{IN} ≤ 27)			150 (18.5 ≤ V_{IN} ≤ 30)	mV V
		I_O ≤ 1A	T_J = 25˚C ΔV_{IN}			50 (7.5 ≤ V_{IN} ≤ 20)			120 (14.6 ≤ V_{IN} ≤ 27)			150 (17.7 ≤ V_{IN} ≤ 30)	mV V
			−55˚C ≤ T_J ≤ +150˚C ΔV_{IN}			25 (8 ≤ V_{IN} ≤ 12)			60 (16 ≤ V_{IN} ≤ 22)			75 (20 ≤ V_{IN} ≤ 26)	mV V
ΔV_O	Load Regulation	T_J = 25˚C	5 mA ≤ I_O ≤ 1.5A 250 mA ≤ I_P ≤ 750 mA		10	50 25		12	120 60		12	150 75	mV mV
		−55˚C ≤ T_J ≤ +150˚C, 5 mA ≤ I_O ≤ 1A				50			120			150	mV
I_Q	Quiescent Current	I_O ≤ 1A	T_J = 25˚C			6			6			6	mA
			−55˚C ≤ T_J ≤ +150˚C			7			7			7	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A			0.5			0.5			0.5		mA
		T_J = 25˚C, I_O ≤ 1A V_{MIN} ≤ V_{IN} ≤ V_{MAX}				0.8 (8 ≤ V_{IN} ≤ 20)			0.8 (15 ≤ V_{IN} ≤ 27)			0.8 (18.5 ≤ V_{IN} ≤ 30)	mA V
		I_O = 500 mA, −55˚C ≤ T_J ≤ +150˚C V_{MIN} ≤ V_{IN} ≤ V_{MAX}				0.8 (8 ≤ V_{IN} ≤ 25)			0.8 (15 ≤ V_{IN} ≤ 30)			0.8 (18.5 ≤ V_{IN} ≤ 30)	mA V
V_N	Output Noise Voltage	T_A = 25˚C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		μV

LM140 Electrical Characteristics (Note 4) (Continued)

$-55^{\circ}C \le T_J \le +150^{\circ}C$ unless otherwise specified

Symbol	Output Voltage			5V			12V			15V			Units
	Input Voltage (unless otherwise noted)			10V			19V			23V			
	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection		$I_O \le 1A$, $T_J = 25^{\circ}C$ or	68	80		61	72		60	70		dB
		f = 120 Hz	$I_O \le 500$ mA, $-55^{\circ}C \le T_J \le +150^{\circ}C$	68			61			60			dB
		$V_{MIN} \le V_{IN} \le V_{MAX}$		$(8 \le V_{IN} \le 18)$			$(15 \le V_{IN} \le 25)$			$(18.5 \le V_{IN} \le 28.5)$			V
R_O	Dropout Voltage	$T_J = 25^{\circ}C$, $I_O = 1A$			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ
	Short-Circuit Current	$T_J = 25^{\circ}C$			2.1			1.5			1.2		A
	Peak Output Current	$T_J = 25^{\circ}C$			2.4			2.4			2.4		A
	Average TC of V_{OUT}	$0^{\circ}C \le T_J \le +150^{\circ}C$, $I_O = 5$ mA			−0.6			−1.5			−1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	$T_J = 25^{\circ}C$, $I_O \le 1A$		7.5			14.6			17.7			V

LM340 Electrical Characteristics (Note 4)

$0^{\circ}C \le T_J \le +125^{\circ}C$ unless otherwise specified

Symbol	Output Voltage			5V			12V			15V			Units
	Input Voltage (unless otherwise noted)			10V			19V			23V			
	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	$T_J = 25^{\circ}C$, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		$P_D \le 15W$, 5 mA ≤ I_O ≤ 1A		4.75		5.25	11.4		12.6	14.25		15.75	V
		$V_{MIN} \le V_{IN} \le V_{MAX}$		$(7.5 \le V_{IN} \le 20)$			$(14.5 \le V_{IN} \le 27)$			$(17.5 \le V_{IN} \le 30)$			V
ΔV_O	Line Regulation	I_O = 500 mA	$T_J = 25^{\circ}C$		3	50		4	120		4	150	mV
			ΔV_{IN}	$(7 \le V_{IN} \le 25)$			$(14.5 \le V_{IN} \le 30)$			$(17.5 \le V_{IN} \le 30)$			V
			$0^{\circ}C \le T_J \le +125^{\circ}C$			50			120			150	mV
			ΔV_{IN}	$(8 \le V_{IN} \le 20)$			$(15 \le V_{IN} \le 27)$			$(18.5 \le V_{IN} \le 30)$			V
		$I_O \le 1A$	$T_J = 25^{\circ}C$			50			120			150	mV
			ΔV_{IN}	$(7.5 \le V_{IN} \le 20)$			$(14.6 \le V_{IN} \le 27)$			$(17.7 \le V_{IN} \le 30)$			V
			$0^{\circ}C \le T_J \le +125^{\circ}C$			25			60			75	mV
			ΔV_{IN}	$(8 \le V_{IN} \le 12)$			$(16 \le V_{IN} \le 22)$			$(20 \le V_{IN} \le 26)$			V
ΔV_O	Load Regulation	$T_J = 25^{\circ}C$	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
			250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, $0^{\circ}C \le T_J \le +125^{\circ}C$				50			120			150	mV
I_Q	Quiescent Current	$I_O \le 1A$	$T_J = 25^{\circ}C$			8			8			8	mA
			$0^{\circ}C \le T_J \le +125^{\circ}C$			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A			0.5			0.5			0.5		mA
		$T_J = 25^{\circ}C$, $I_O \le 1A$				1.0			1.0			1.0	mA

LM340 Electrical Characteristics (Note 4) (Continued)

$0^\circ C \le T_J \le +125^\circ C$ unless otherwise specified

Symbol	Output Voltage / Input Voltage (unless otherwise noted) / Parameter	Conditions		5V / 10V Min	5V / 10V Typ	5V / 10V Max	12V / 19V Min	12V / 19V Typ	12V / 19V Max	15V / 23V Min	15V / 23V Typ	15V / 23V Max	Units
		$V_{MIN} \le V_{IN} \le V_{MAX}$		$(7.5 \le V_{IN} \le 20)$			$(14.8 \le V_{IN} \le 27)$			$(17.9 \le V_{IN} \le 30)$			V
		$I_O \le 500$ mA, $0^\circ C \le T_J \le +125^\circ C$				1.0			1.0			1.0	mA
		$V_{MIN} \le V_{IN} \le V_{MAX}$		$(7 \le V_{IN} \le 25)$			$(14.5 \le V_{IN} \le 30)$			$(17.5 \le V_{IN} \le 30)$			V
V_N	Output Noise Voltage	$T_A = 25^\circ C$, 10 Hz ≤ f ≤ 100 kHz			40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection		$I_O \le 1A$, $T_J = 25^\circ C$	62	80		55	72		54	70		dB
		f = 120 Hz	or $I_O \le 500$ mA, $0^\circ C \le T_J \le +125^\circ C$	62			55			54			dB
		$V_{MIN} \le V_{IN} \le V_{MAX}$		$(8 \le V_{IN} \le 18)$			$(15 \le V_{IN} \le 25)$			$(18.5 \le V_{IN} \le 28.5)$			V
R_O	Dropout Voltage	$T_J = 25^\circ C$, $I_O = 1A$			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ
	Short-Circuit Current	$T_J = 25^\circ C$			2.1			1.5			1.2		A
	Peak Output Current	$T_J = 25^\circ C$			2.4			2.4			2.4		A
	Average TC of V_{OUT}	$0^\circ C \le T_J \le +125^\circ C$, $I_O = 5$ mA			–0.6			–1.5			–1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	$T_J = 25^\circ C$, $I_O \le 1A$		7.5			14.6			17.7			V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be guaranteed. For guaranteed specifications and test conditions see the Electrical Characteristics.

Note 2: The maximum allowable power dissipation at any ambient temperature is a function of the maximum junction temperature for operation (T_{JMAX} = 125°C or 150°C), the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A). $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above T_{JMAX} and the electrical specifications do not apply. If the die temperature rises above 150°C, the device will go into thermal shutdown. For the TO-3 package (K, KC), the junction-to-ambient thermal resistance (θ_{JA}) is 39°C/W. When using a heatsink, θ_{JA} is the sum of the 4°C/W junction-to-case thermal resistance (θ_{JC}) of the TO-3 package and the case-to-ambient thermal resistance of the heatsink. For the TO-220 package (T), θ_{JA} is 54°C/W and θ_{JC} is 4°C/W. If SOT-223 is used, the junction-to-ambient thermal resistance is 174°C/W and can be reduced by a heatsink (see Applications Hints on heatsinking).

If the TO-263 package is used, the thermal resistance can be reduced by increasing the PC board copper area thermally connected to the package: Using 0.5 square inches of copper area, θ_{JA} is 50°C/W; with 1 square inch of copper area, $\theta_{JA}$is 37°C/W; and with 1.6 or more inches of copper area, θ_{JA} is 32°C/W.

Note 3: ESD rating is based on the human body model, 100 pF discharged through 1.5 kΩ.

Note 4: All characteristics are measured with a 0.22 μF capacitor from input to ground and a 0.1 μF capacitor from output to ground. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Note 5: Military datasheets are available upon request. At the time of printing, the military datasheet specifications for the LM140K-5.0/883, LM140K-12/883, and LM140K-15/883 complied with the min and max limits for the respective versions of the LM140. The LM140H and LM140K may also be procured as JAN devices on slash sheet JM38510/107.

LM7808C
Electrical Characteristics

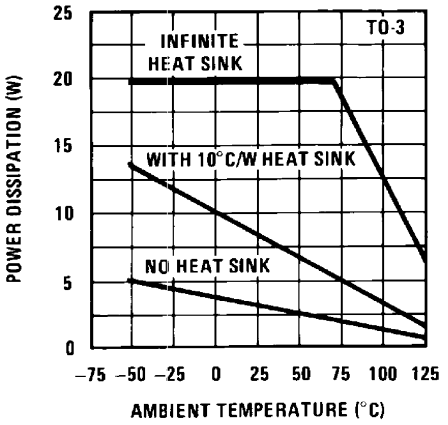
$0^{\circ}C \le T_J \le +150^{\circ}C$, $V_I = 14V$, $I_O = 500$ mA, $C_I = 0.33$ µF, $C_O = 0.1$ µF, unless otherwise specified

Symbol	Parameter		Conditions (Note 6)		LM7808C			Units
					Min	Typ	Max	
V_O	Output Voltage		$T_J = 25^{\circ}C$		7.7	8.0	8.3	V
ΔV_O	Line Regulation		$T_J = 25^{\circ}C$	$10.5V \le V_I \le 25V$		6.0	160	mV
				$11.0V \le V_I \le 17V$		2.0	80	
ΔV_O	Load Regulation		$T_J = 25^{\circ}C$	$5.0\ mA \le I_O \le 1.5A$		12	160	mV
				$250\ mA \le I_O \le 750\ mA$		4.0	80	
V_O	Output Voltage		$11.5V \le V_I \le 23V$, $5.0\ mA \le I_O \le 1.0A$, $P \le 15W$		7.6		8.4	V
I_Q	Quiescent Current		$T_J = 25^{\circ}C$			4.3	8.0	mA
ΔI_Q	Quiescent	With Line	$11.5V \le V_I \le 25V$				1.0	mA
	Current Change	With Load	$5.0\ mA \le I_O \le 1.0A$				0.5	
V_N	Noise		$T_A = 25^{\circ}C$, $10\ Hz \le f \le 100\ kHz$			52		µV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 120 Hz, $I_O = 350$ mA, $T_J = 25^{\circ}C$		56	72		dB
V_{DO}	Dropout Voltage		$I_O = 1.0A$, $T_J = 25^{\circ}C$			2.0		V
R_O	Output Resistance		f = 1.0 kHz			16		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25^{\circ}C$, $V_I = 35V$			0.45		A
I_{PK}	Peak Output Current		$T_J = 25^{\circ}C$			2.2		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			0.8		mV/°C

Note 6: All characteristics are measured with a 0.22 µF capacitor from input to ground and a 0.1 µF capacitor from output to ground. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

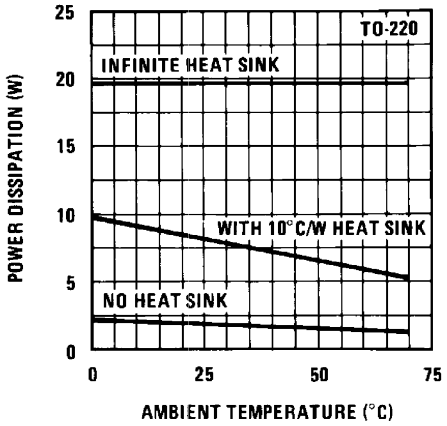
Typical Performance Characteristics

Maximum Average Power Dissipation



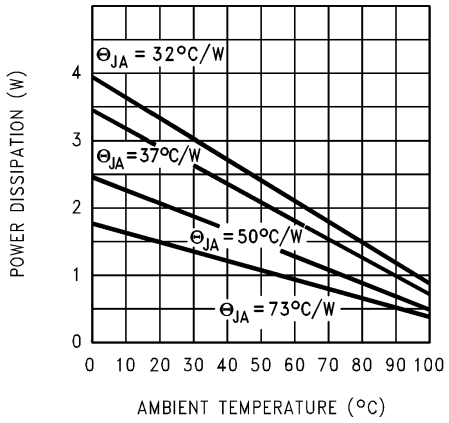
00778122

Maximum Average Power Dissipation



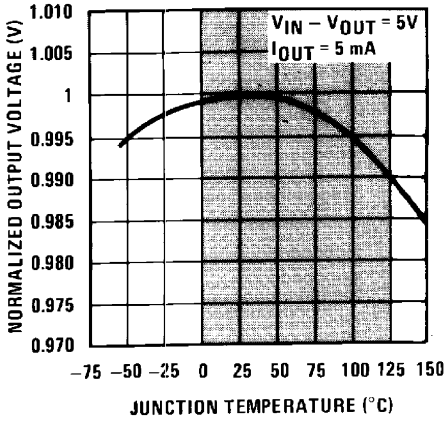
00778123

Maximum Power Dissipation (TO-263)
(See Note 2)



00778124

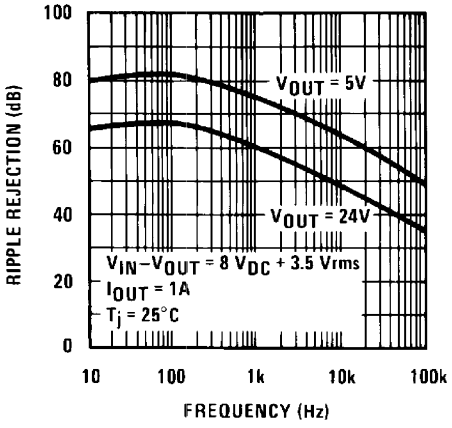
Output Voltage (Normalized to 1V at T_J = 25°C)



00778125

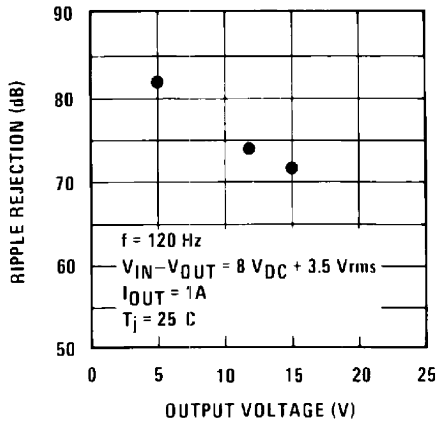
Note: Shaded area refers to LM340A/LM340, LM7805C, LM7812C and LM7815C.

Ripple Rejection



00778126

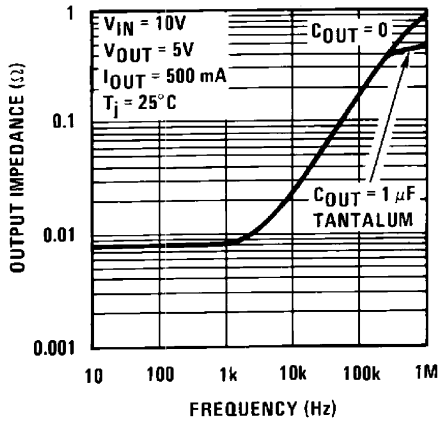
Ripple Rejection



00778127

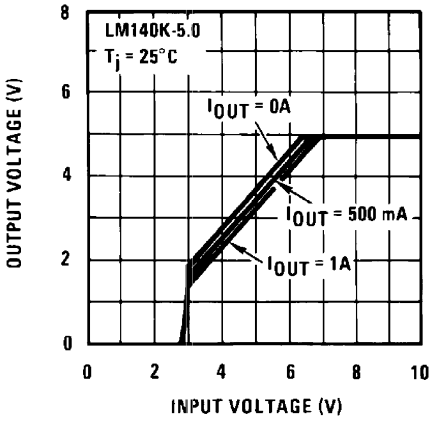
Typical Performance Characteristics (Continued)

Output Impedance



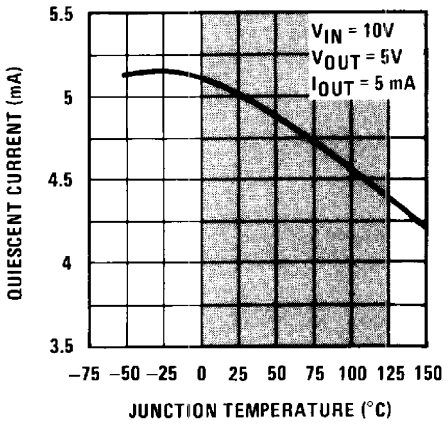
00778128

Dropout Characteristics



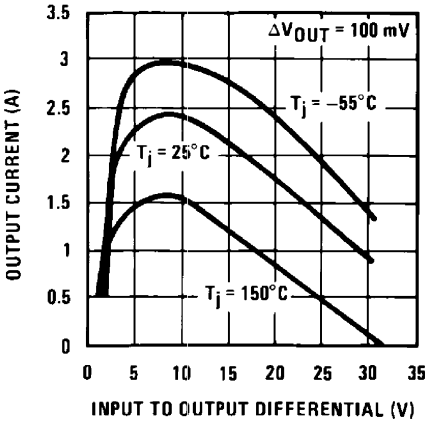
00778129

Quiescent Current



00778130

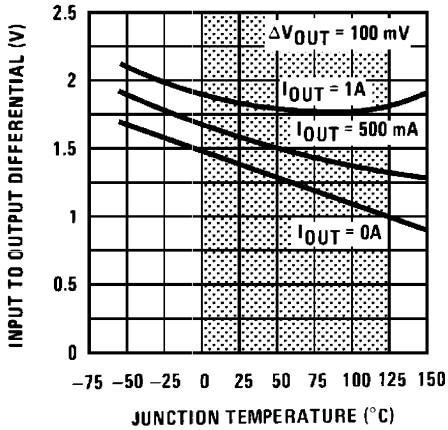
Peak Output Current



00778131

Note: Shaded area refers to LM340A/LM340, LM7805C, LM7812C and LM7815C.

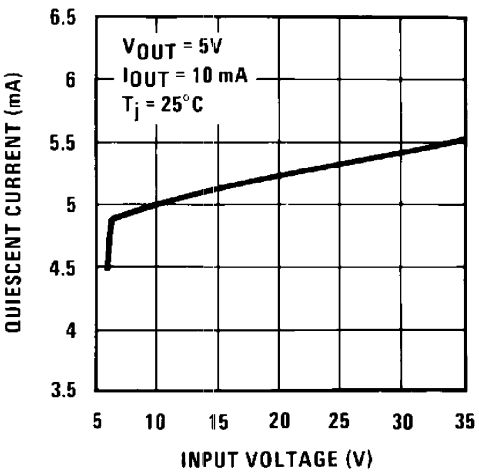
Dropout Voltage



00778132

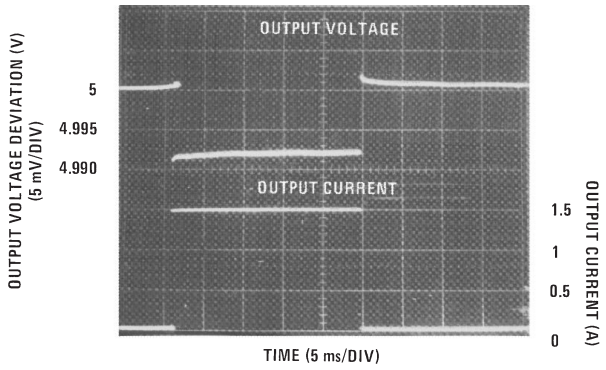
Note: Shaded area refers to LM340A/LM340, LM7805C, LM7812C and LM7815C.

Quiescent Current



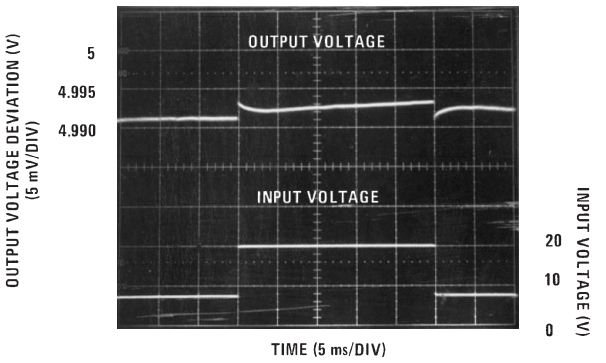
00778133

Line Regulation
140AK-5.0, I_{OUT} = 1A, T_A = 25˚C



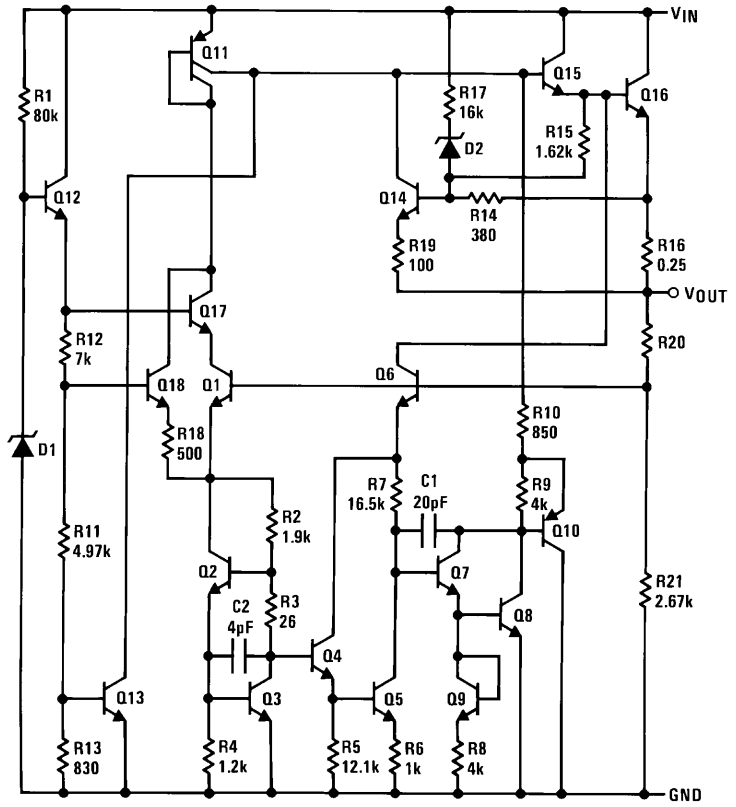
00778105

Line Regulation
140AK-5.0, V_{IN} = 10V, T_A = 25˚C



00778106

Equivalent Schematic



00778107

Application Hints

The LM340/LM78XX series is designed with thermal protection, output short-circuit protection and output transistor safe area protection. However, as with *any* IC regulator, it becomes necessary to take precautions to assure that the regulator is not inadvertently damaged. The following describes possible misapplications and methods to prevent damage to the regulator.

SHORTING THE REGULATOR INPUT

When using large capacitors at the output of these regulators, a protection diode connected input to output (*Figure 1*) may be required if the input is shorted to ground. Without the protection diode, an input short will cause the input to rapidly approach ground potential, while the output remains near the initial V_{OUT}because of the stored charge in the large output capacitor. The capacitor will then discharge through a large internal input to output diode and parasitic transistors. If the energy released by the capacitor is large enough, this diode, low current metal and the regulator will be destroyed. The fast diode in *Figure 1* will shunt most of the capacitors discharge current around the regulator. Generally no protection diode is required for values of output capacitance ≤ 10 µF.

RAISING THE OUTPUT VOLTAGE ABOVE THE INPUT VOLTAGE

Since the output of the device does not sink current, forcing the output high can cause damage to internal low current paths in a manner similar to that just described in the “Shorting the Regulator Input” section.

REGULATOR FLOATING GROUND (*Figure 2*)

When the ground pin alone becomes disconnected, the output approaches the unregulated input, causing possible damage to other circuits connected to V_{OUT}. If ground is reconnected with power “ON”, damage may also occur to the regulator. This fault is most likely to occur when plugging in regulators or modules with on card regulators into powered up sockets. Power should be turned off first, thermal limit ceases operating, or ground should be connected first if power must be left on.

TRANSIENT VOLTAGES

If transients exceed the maximum rated input voltage of the device, or reach more than 0.8V below ground and have sufficient energy, they will damage the regulator. The solution is to use a large input capacitor, a series input breakdown diode, a choke, a transient suppressor or a combination of these.

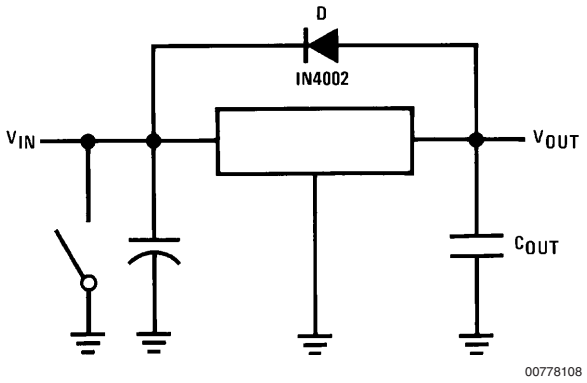


FIGURE 1. Input Short

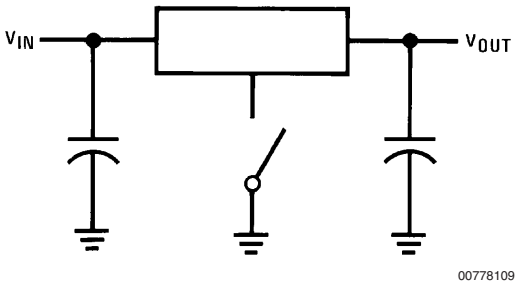


FIGURE 2. Regulator Floating Ground

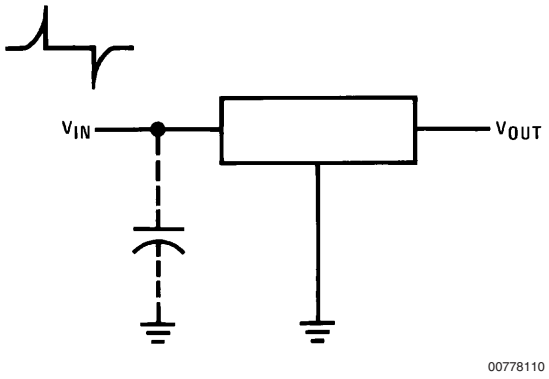


FIGURE 3. Transients

When a value for $\theta_{(H-A)}$ is found using the equation shown, a heatsink must be selected that has *a value that is less than or equal to this number.*

$\theta_{(H-A)}$ is specified numerically by the heatsink manufacturer in this catalog, or shown in a curve that plots temperature rise vs power dissipation for the heatsink.

Application Hints (Continued)

HEATSINKING TO-263 AND SOT-223 PACKAGE PARTS

Both the TO-263 ("S") and SOT-223 ("MP") packages use a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the plane.

shows for the TO-263 the measured values of $\theta_{(J-A)}$ for different copper area sizes using a typical PCB with 1 ounce copper *and no solder mask over the copper area used for heatsinking*.

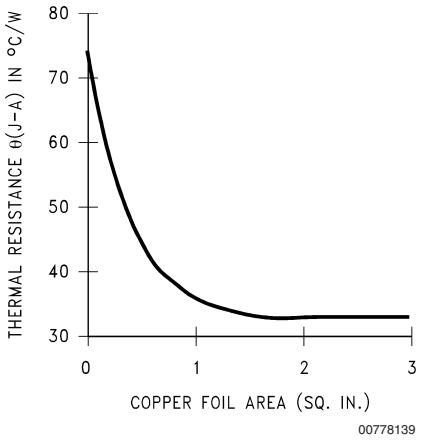


FIGURE 4. $\theta_{(J-A)}$ vs Copper (1 ounce) Area for the TO-263 Package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. It should also be observed that the minimum value of $\theta_{(J-A)}$ for the TO-263 package mounted to a PCB is 32˚C/W.

As a design aid, *Figure 5* shows the maximum allowable power dissipation compared to ambient temperature for the TO-263 device (assuming $\theta_{(J-A)}$ is 35˚C/W and the maximum junction temperature is 125˚C).

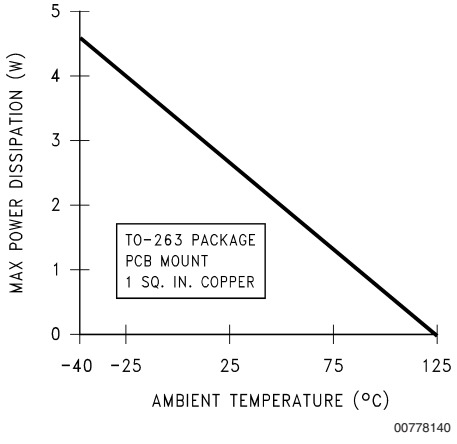


FIGURE 5. Maximum Power Dissipation vs T_{AMB} for the TO-263 Package

Figures 6, 7 show the information for the SOT-223 package. *Figure 6* assumes a $\theta_{(J-A)}$ of 74˚C/W for 1 ounce copper and 51˚C/W for 2 ounce copper and a maximum junction temperature of 125˚C.

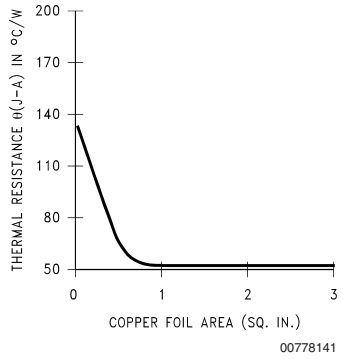


FIGURE 6. $\theta_{(J-A)}$ vs Copper (2 ounce) Area for the SOT-223 Package

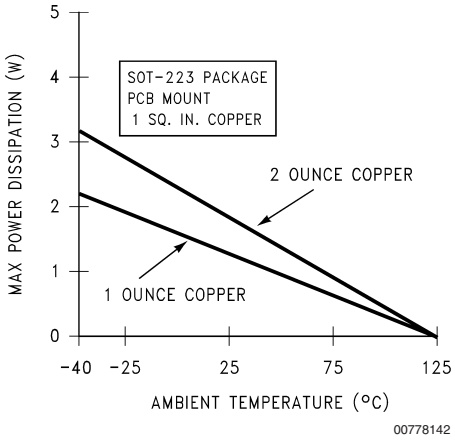
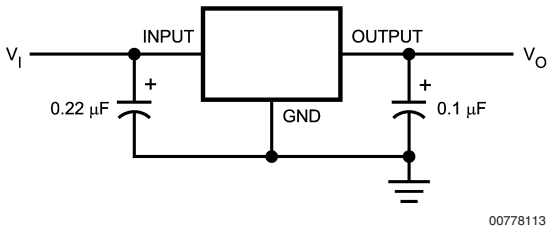


FIGURE 7. Maximum Power Dissipation vs T_{AMB} for the SOT-223 Package

Please see AN-1028 for power enhancement techniques to be used with the SOT-223 package.

Typical Applications

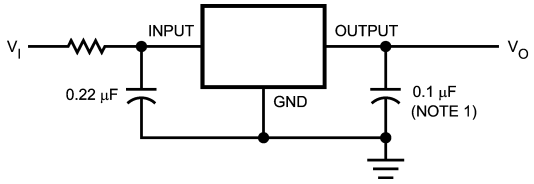
Fixed Output Regulator



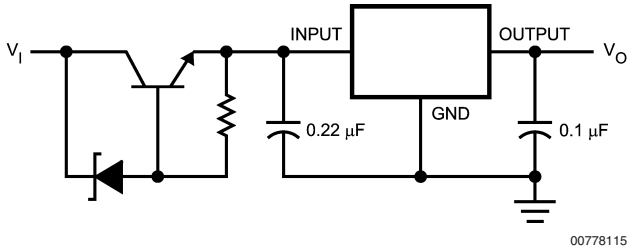
00778113

Note: Bypass capacitors are recommended for optimum stability and transient response, and should be located as close as possible to the regulator.

High Input Voltage Circuits

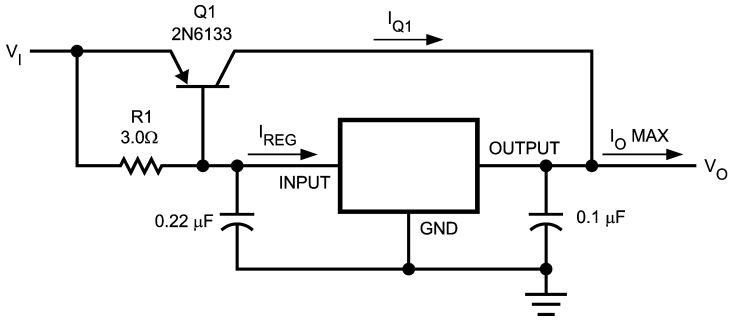


00778114



00778115

High Current Voltage Regulator



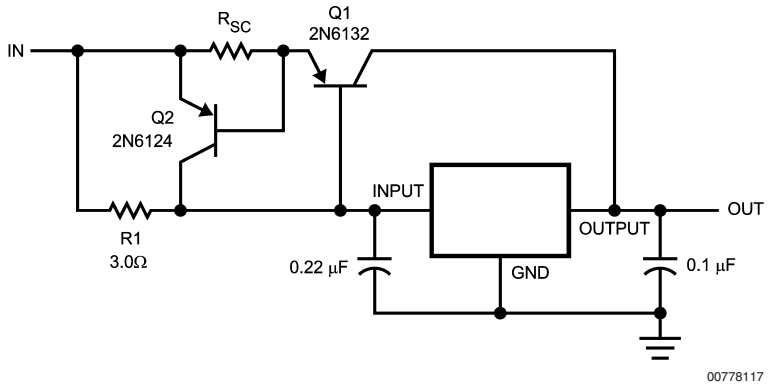
00778116

$$\beta(Q1) \geq \frac{I_{O\ Max}}{I_{REG\ Max}}$$

$$R1 = \frac{0.9}{I_{REG}} = \frac{\beta(Q1)\ V_{BE(Q1)}}{I_{REG\ Max}\ (\beta + 1) - I_{O\ Max}}$$

Typical Applications (Continued)

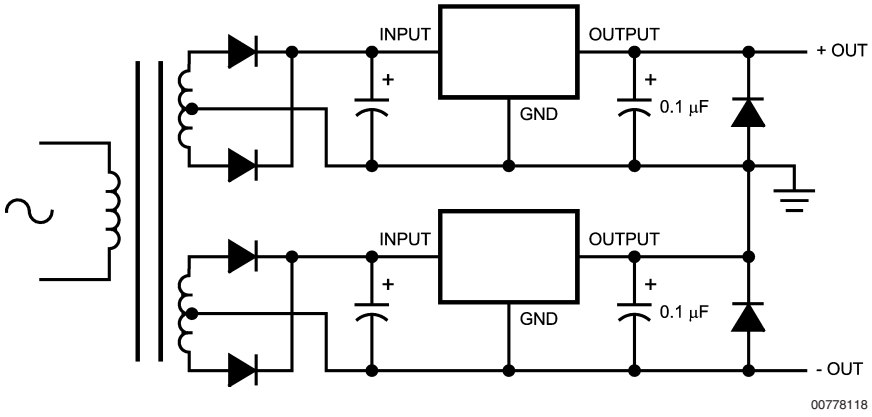
High Output Current, Short Circuit Protected



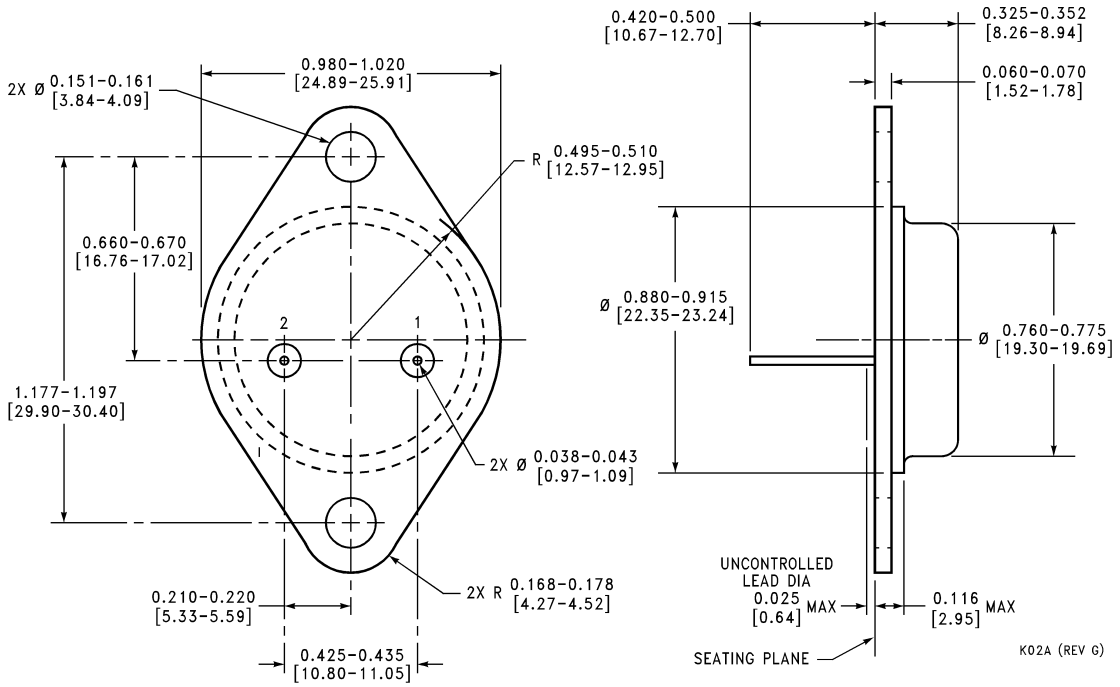
$$R_{SC} = \frac{0.8}{I_{SC}}$$

$$R1 = \frac{\beta V_{BE(Q1)}}{I_{REG\ Max}(\beta + 1) - I_{O\ Max}}$$

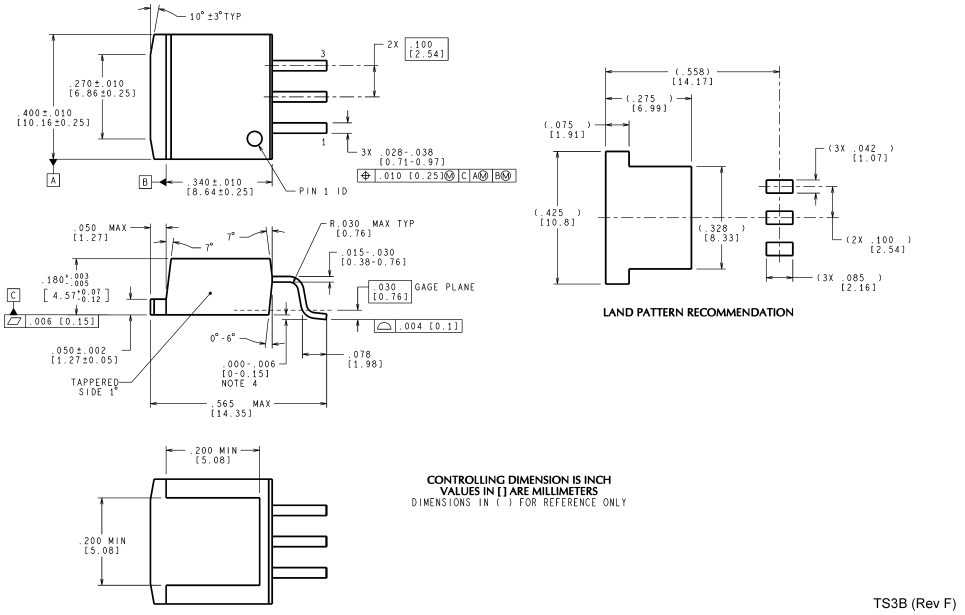
Positive and Negative Regulator



Physical Dimensions inches (millimeters) unless otherwise noted

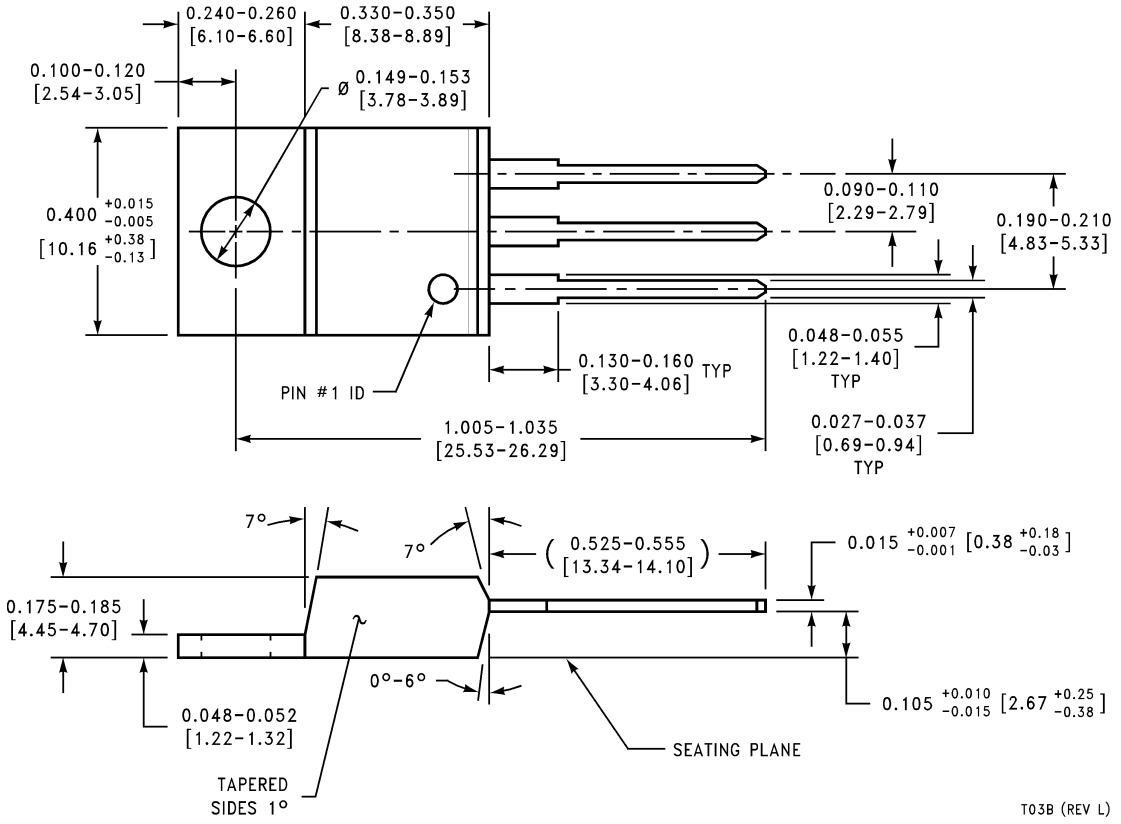


TO-3 Metal Can Package (K)
NS Package Number K02A

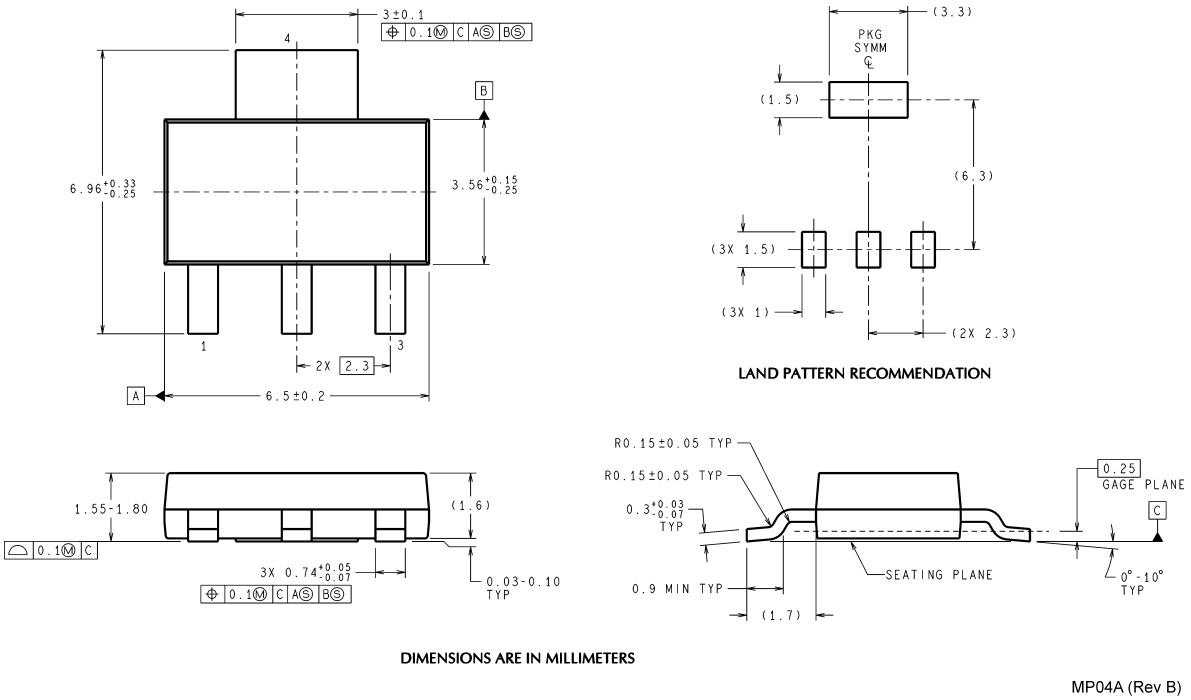


TO-263 Surface-Mount Package (S)
NS Package Number TS3B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



TO-220 Power Package (T)
NS Package Number T03B



3-Lead SOT-223 Package
NS Package Number MP04A

Notes

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Asia Pacific Customer
Support Center
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Tel: 81-3-5639-7560

National Semiconductor

August 2000

LM741
Operational Amplifier

General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

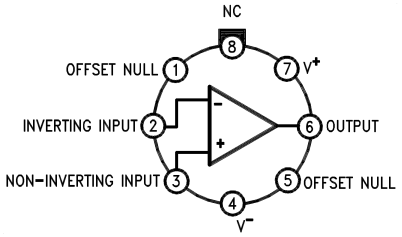
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0˚C to +70˚C temperature range, instead of −55˚C to +125˚C.

Features

Connection Diagrams

Metal Can Package

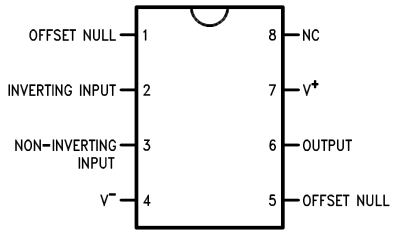


00934102

Note 1: LM741H is available per JM38510/10101

Order Number LM741H, LM741H/883 (Note 1)**, LM741AH/883 or LM741CH**
See NS Package Number H08C

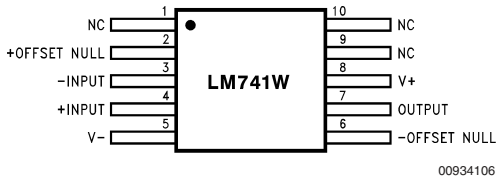
Dual-In-Line or S.O. Package



00934103

Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak

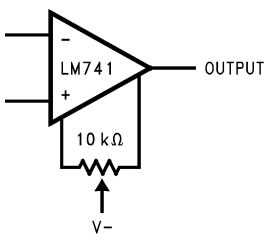


00934106

Order Number LM741W/883
See NS Package Number W10A

Typical Application

Offset Nulling Circuit



00934107

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	−55˚C to +125˚C	−55˚C to +125˚C	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C	−65˚C to +150˚C	−65˚C to +150˚C
Junction Temperature	150˚C	150˚C	100˚C
Soldering Information			
N-Package (10 seconds)	260˚C	260˚C	260˚C
J- or H-Package (10 seconds)	300˚C	300˚C	300˚C
M-Package			
Vapor Phase (60 seconds)	215˚C	215˚C	215˚C
Infrared (15 seconds)	215˚C	215˚C	215˚C
See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.			
ESD Tolerance (Note 8)	400V	400V	400V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25˚C$										
	$R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							µV/˚C
Input Offset Voltage Adjustment Range	$T_A = 25˚C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25˚C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/˚C
Input Bias Current	$T_A = 25˚C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25˚C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25˚C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V

Electrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$T_A = 25^\circ C$, $R_L \geq 2\ k\Omega$										
	$V_S = \pm 20V$, $V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
	$R_L \geq 2\ k\Omega$,										
	$V_S = \pm 20V$, $V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V$, $V_O = \pm 2V$	10									V/mV
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	±16									V
	$R_L \geq 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		V
Output Short Circuit	$T_A = 25^\circ C$	10	25	35		25			25		mA
Current	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\Omega$, $V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
Ratio	$V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25^\circ C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 6)	$T_A = 25^\circ C$	0.437	1.5								MHz
Slew Rate	$T_A = 25^\circ C$, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	$T_A = 25^\circ C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25^\circ C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100˚C/W	100˚C/W	170˚C/W	195˚C/W
θ_{jC} (Junction to Case)	N/A	N/A	25˚C/W	N/A

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

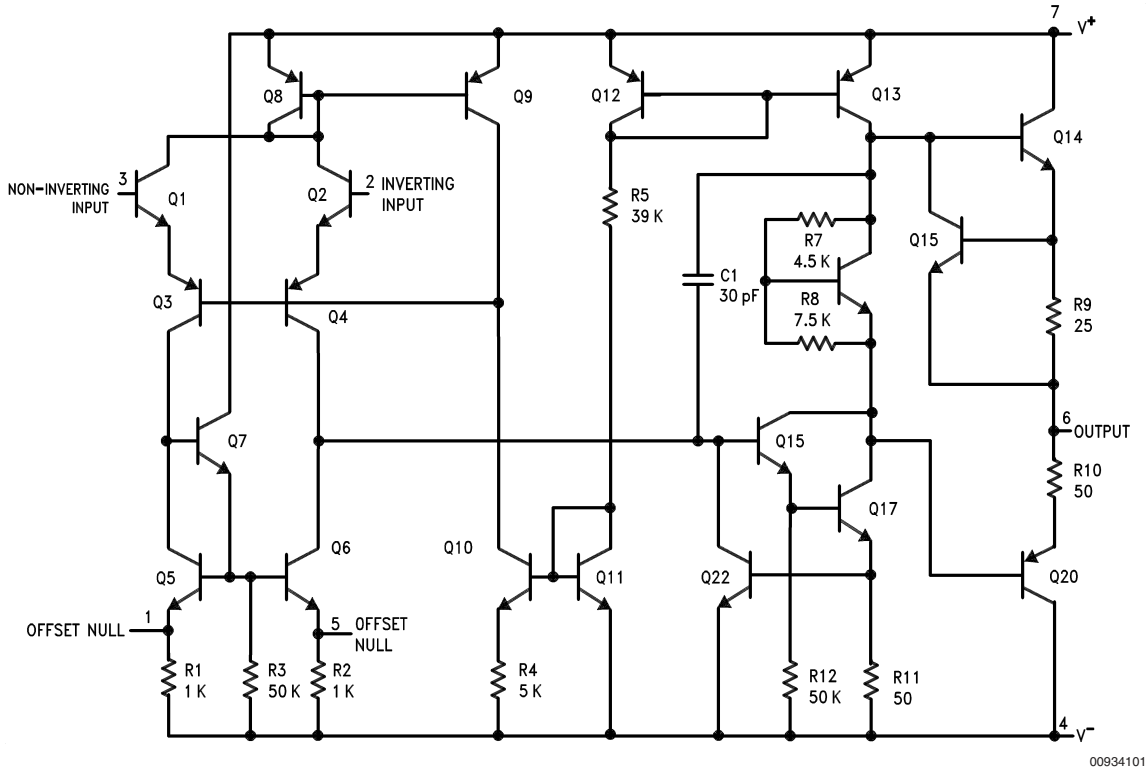
Note 5: Unless otherwise specified, these specifications apply for V_S = ±15V, −55˚C ≤ T_A ≤ +125˚C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0˚C ≤ T_A ≤ +70˚C.

Note 6: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 7: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

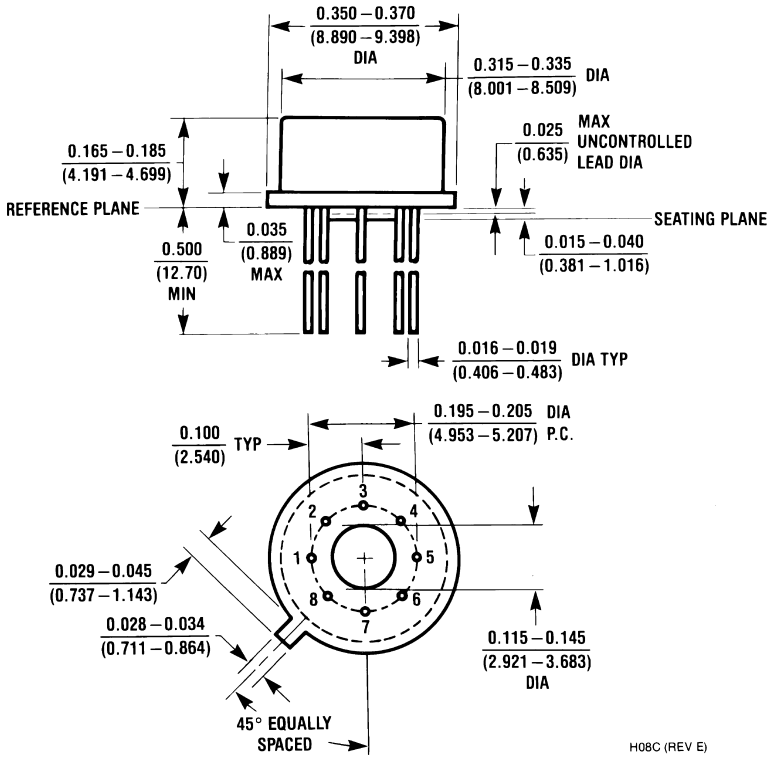
Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Schematic Diagram



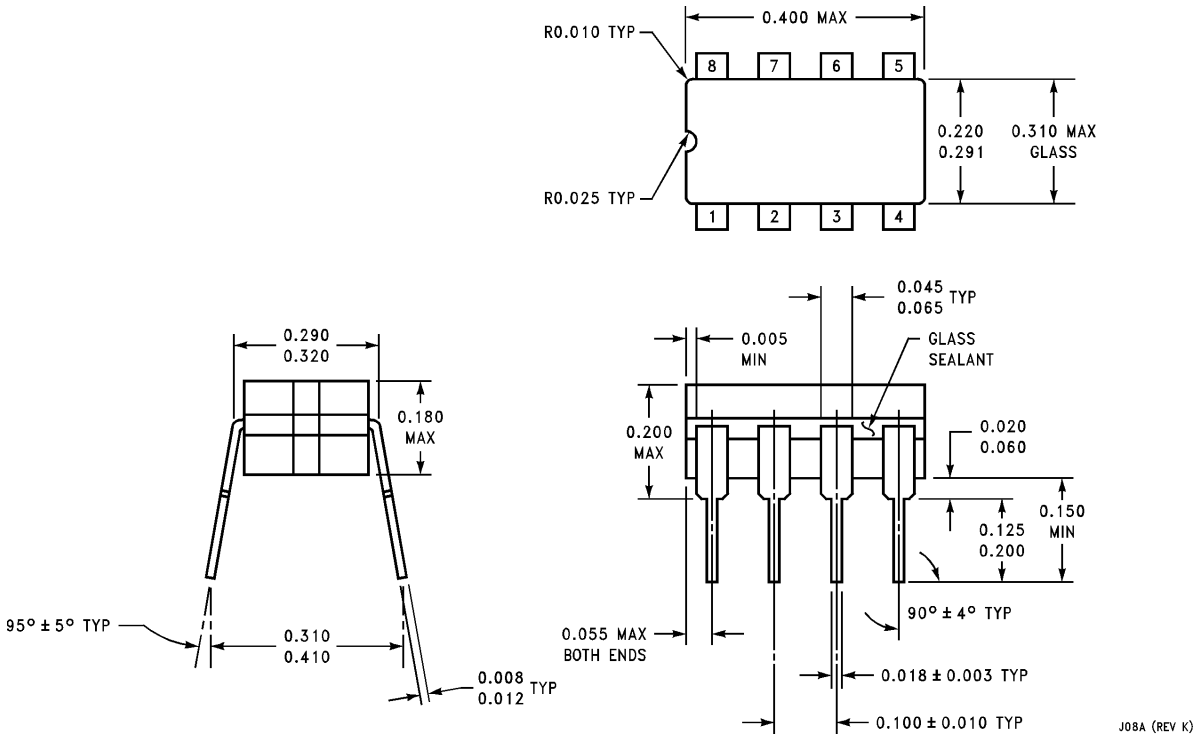
Physical Dimensions inches (millimeters)

unless otherwise noted

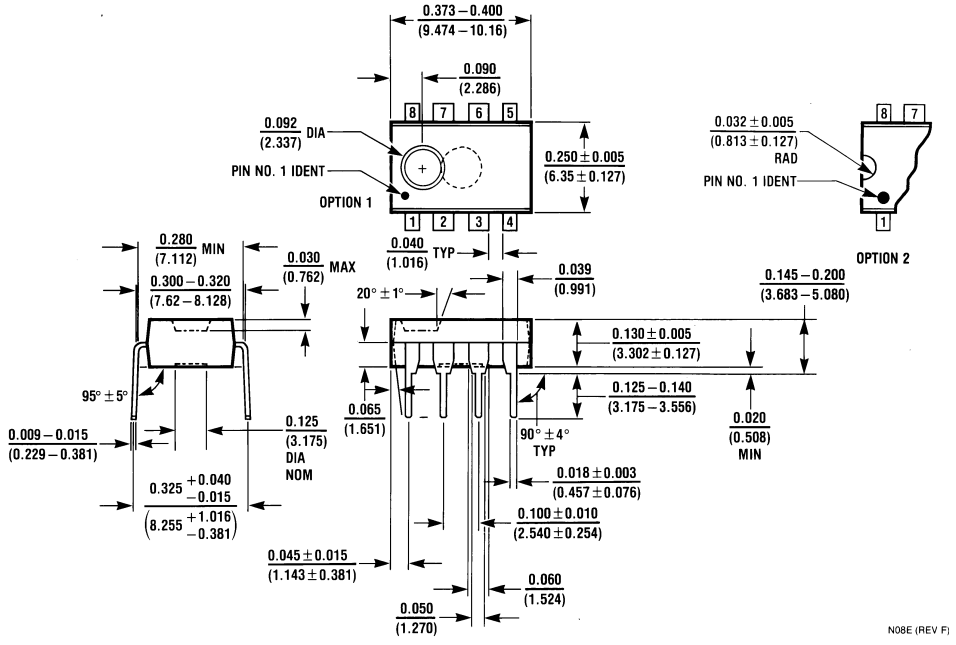


Metal Can Package (H)
Order Number LM741H, LM741H/883, LM741AH/883, LM741AH-MIL or LM741CH
NS Package Number H08C

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

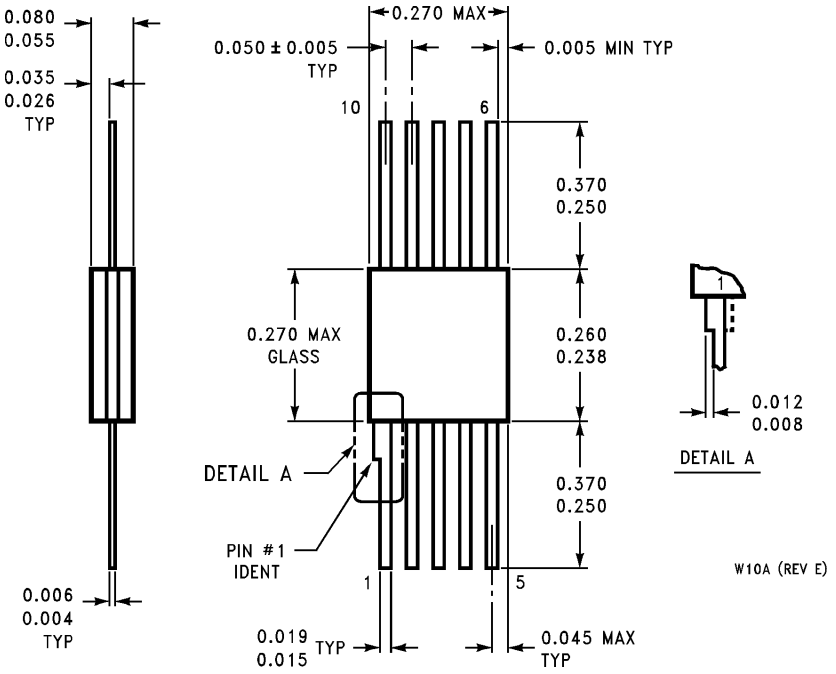


Ceramic Dual-In-Line Package (J)
Order Number LM741J/883
NS Package Number J08A



Dual-In-Line Package (N)
Order Number LM741CN
NS Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



10-Lead Ceramic Flatpak (W)
Order Number LM741W/883, LM741WG-MPR or LM741WG/883
NS Package Number W10A

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MC34151, MC33151

High Speed Dual MOSFET Drivers

The MC34151/MC33151 are dual inverting high speed drivers specifically designed for applications that require low current digital circuitry to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS and LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent erratic system operation at low supply voltages.

Typical applications include switching power supplies, dc to dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

These devices are available in dual−in−line and surface mount packages.

Features

- Pb−Free Packages are Available
- Two Independent Channels with 1.5 A Totem Pole Output
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs
- Pin Out Equivalent to DS0026 and MMH0026

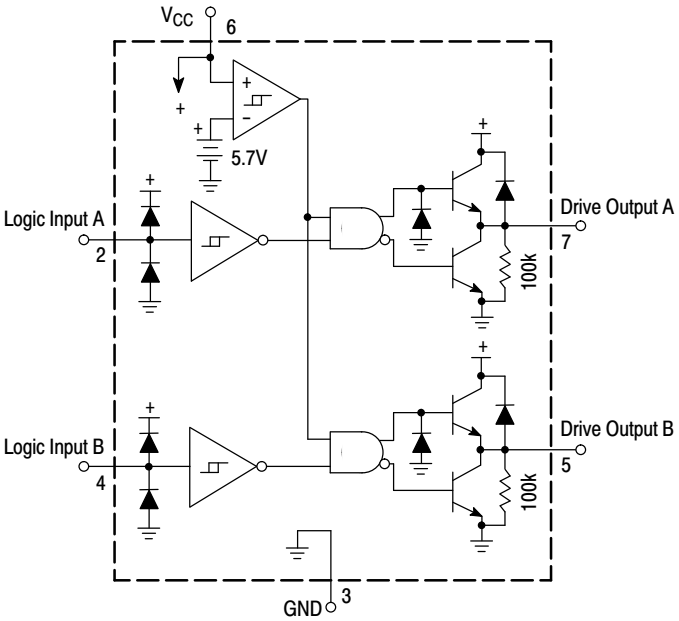

Figure 1. Representative Block Diagram

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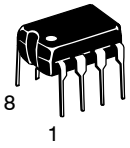
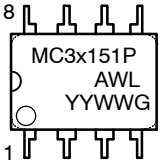
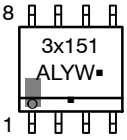
MARKING DIAGRAMS



PDIP−8
P SUFFIX
CASE 626



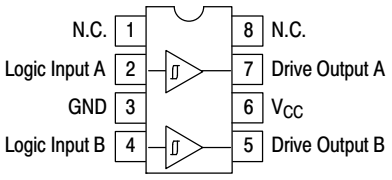
SOIC−8
D SUFFIX
CASE 751



x	= 3 or 4
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Logic Inputs (Note 1)	V_{in}	−0.3 to V_{CC}	V
Drive Outputs (Note 2) Totem Pole Sink or Source Current Diode Clamp Current (Drive Output to V_{CC})	 I_O $I_{O(clamp)}$	 1.5 1.0	A
Power Dissipation and Thermal Characteristics D Suffix SOIC−8 Package Case 751 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction−to−Air P Suffix 8−Pin Package Case 626 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 0.56 180 1.0 100	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34151 MC33151 MC33151V	T_A	 0 to +70 −40 to +85 −40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Electrostatic Discharge Sensitivity (ESD) Human Body Model (HBM) Machine Model (MM)	ESD	 2000 200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC}, whichever is less.
2. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the only operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage – Output Transition High to Low State	V_{IH}	–	1.75	2.6	V
Output Transition Low to High State	V_{IL}	0.8	1.58	–	
Input Current – High State (V_{IH} = 2.6 V)	I_{IH}	–	200	500	μA
– Low State (V_{IL} = 0.8 V)	I_{IL}	–	20	100	
DRIVE OUTPUT					
Output Voltage – Low State (I_{Sink} = 10 mA)	V_{OL}	–	0.8	1.2	V
(I_{Sink} = 50 mA)		–	1.1	1.5	
(I_{Sink} = 400 mA)		–	1.7	2.5	
– High State (I_{Source} = 10 mA)	V_{OH}	10.5	11.2	–	
(I_{Source} = 50 mA)		10.4	11.1	–	
(I_{Source} = 400 mA)		9.5	10.9	–	
Output Pulldown Resistor	R_{PD}	–	100	–	kΩ
SWITCHING CHARACTERISTICS (T_A = 25°C)					
Propagation Delay (10% Input to 10% Output, C_L = 1.0 nF)					ns
Logic Input to Drive Output Rise	$t_{PLH(in/out)}$	–	35	100	
Logic Input to Drive Output Fall	$t_{PHL(in/out)}$	–	36	100	
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF	t_r	–	14	30	ns
C_L = 2.5 nF		–	31	–	
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF	t_f	–	16	30	ns
C_L = 2.5 nF		–	32	–	
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Standby (Logic Inputs Grounded)		–	6.0	10	
Operating (C_L = 1.0 nF Drive Outputs 1 and 2, f = 100 kHz)		–	10.5	15	
Operating Voltage	V_{CC}	6.5	–	18	V

1. For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC}, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. T_{low} = 0°C for MC34151 T_{high} = +70°C for MC34151
   −40°C for MC33151 +85°C for MC33151

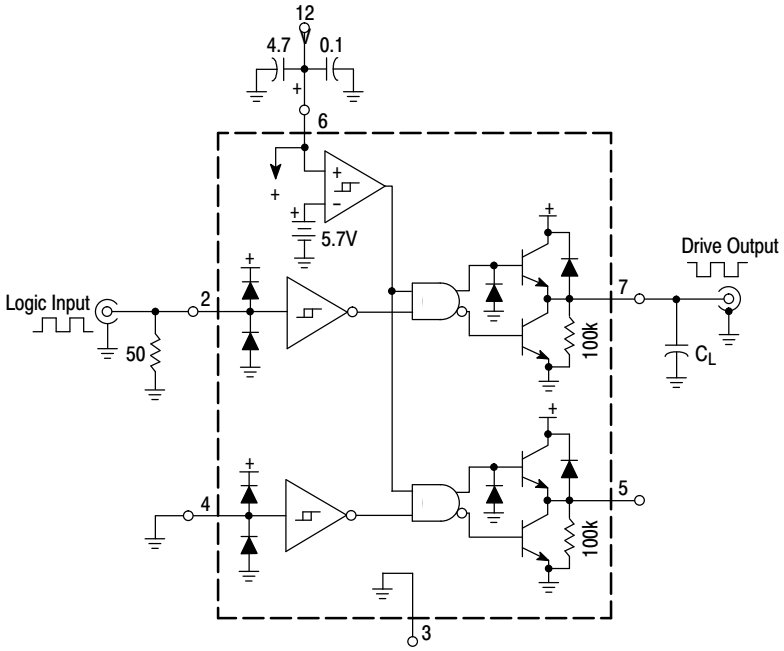


Figure 2. Switching Characteristics Test Circuit

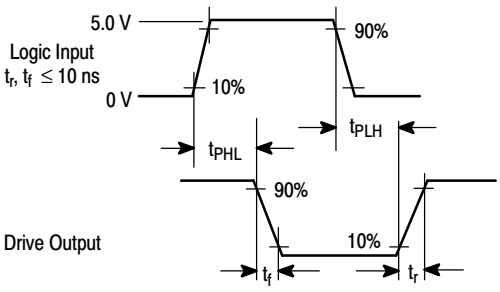


Figure 3. Switching Waveform Definitions

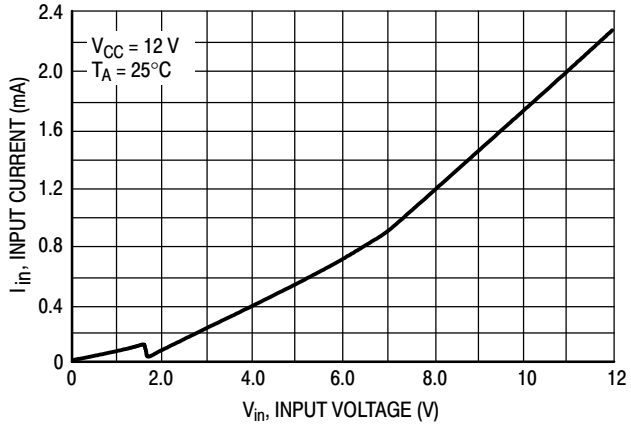


Figure 4. Logic Input Current versus Input Voltage

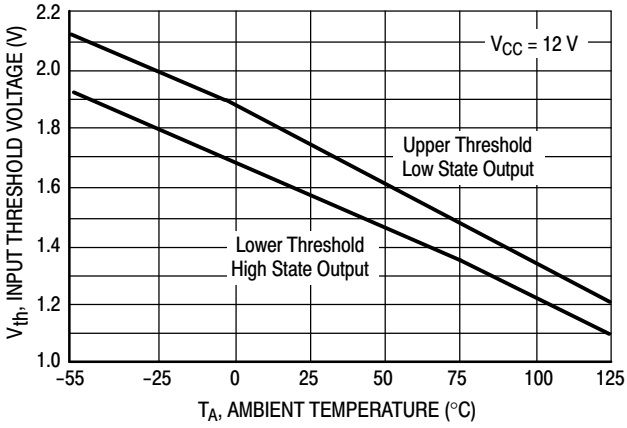


Figure 5. Logic Input Threshold Voltage versus Temperature

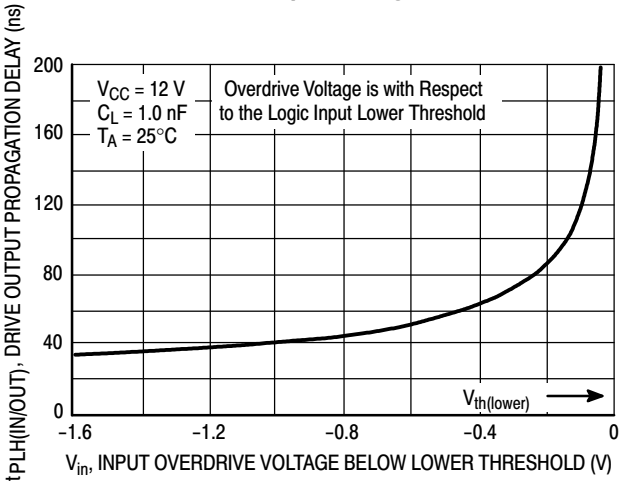


Figure 6. Drive Output Low−to−High Propagation Delay versus Logic Overdrive Voltage

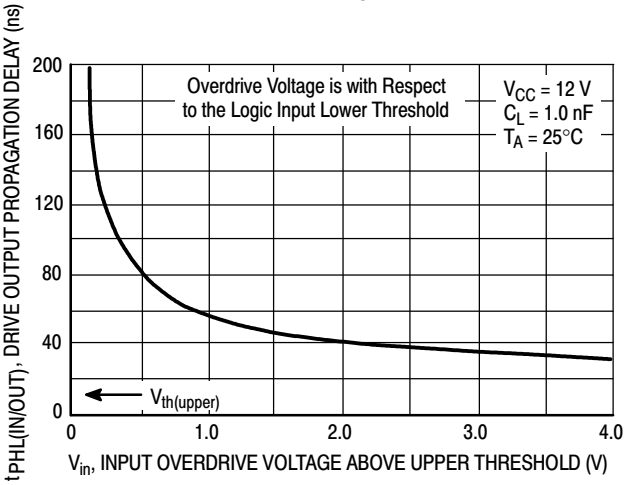


Figure 7. Drive Output High−to−Low Propagation Delay versus Logic Input Overdrive Voltage

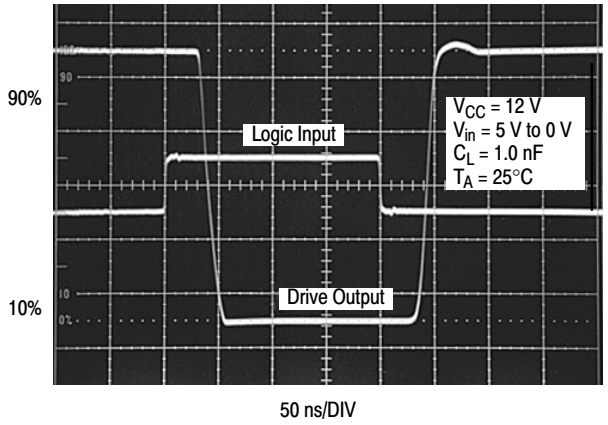


Figure 8. Propagation Delay

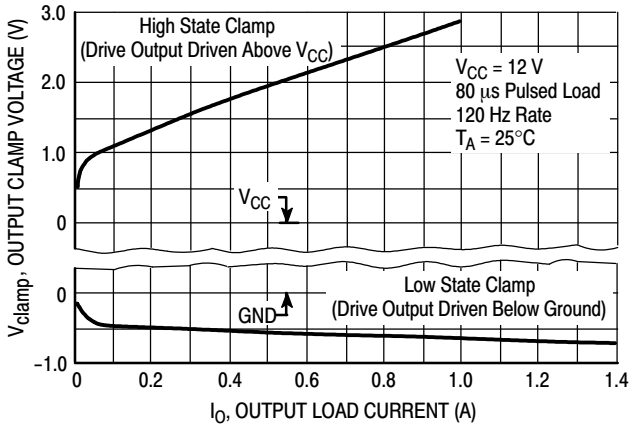


Figure 9. Drive Output Clamp Voltage versus Clamp Current

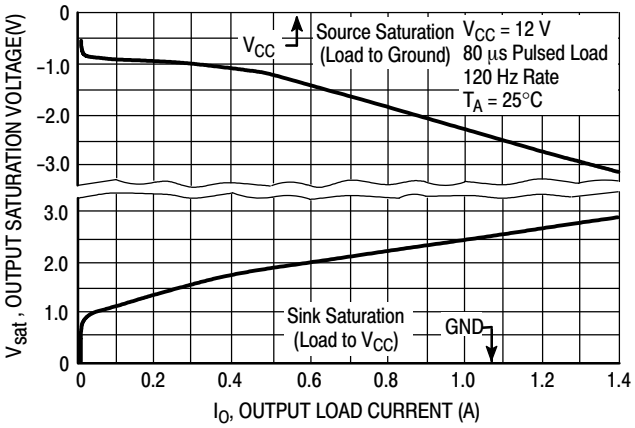


Figure 10. Drive Output Saturation Voltage versus Load Current

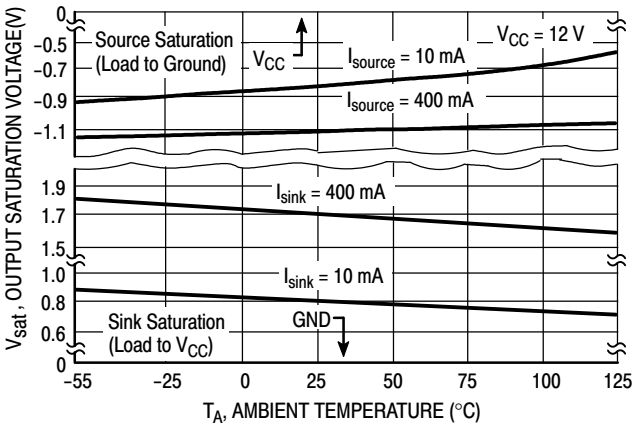


Figure 11. Drive Output Saturation Voltage versus Temperature

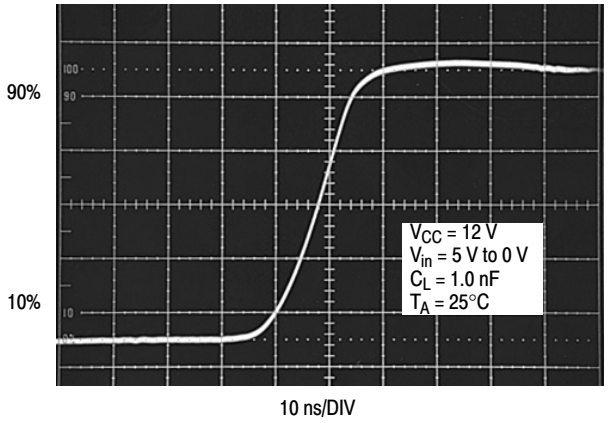


Figure 12. Drive Output Rise Time

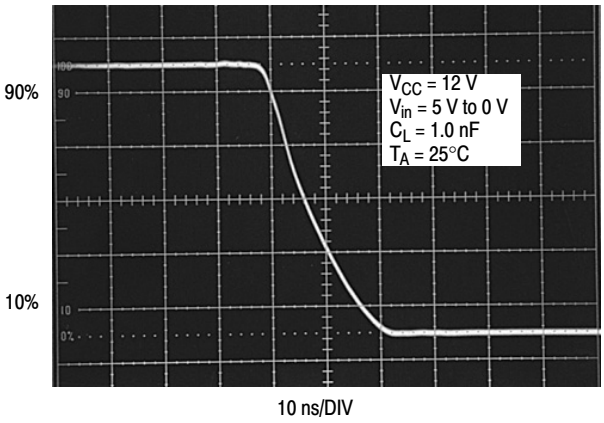


Figure 13. Drive Output Fall Time

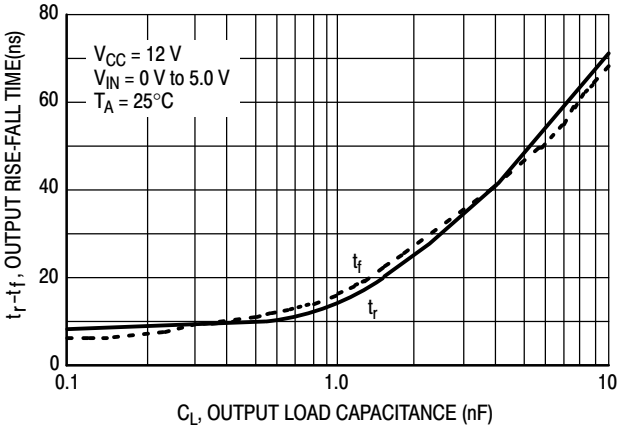


Figure 14. Drive Output Rise and Fall Time versus Load Capacitance

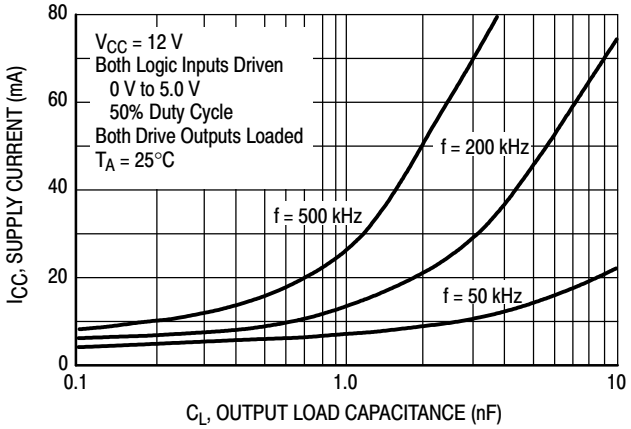


Figure 15. Supply Current versus Drive Output Load Capacitance

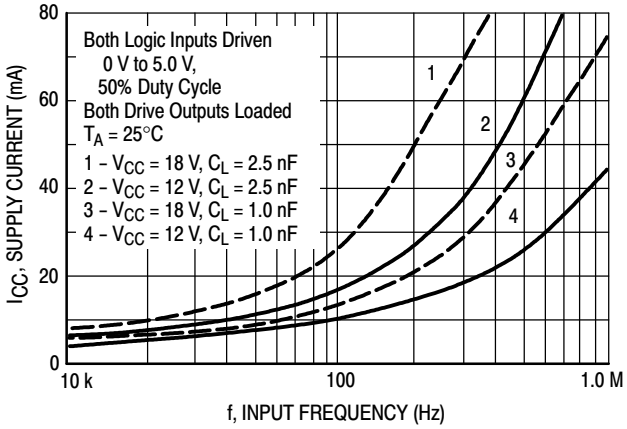


Figure 16. Supply Current versus Input Frequency

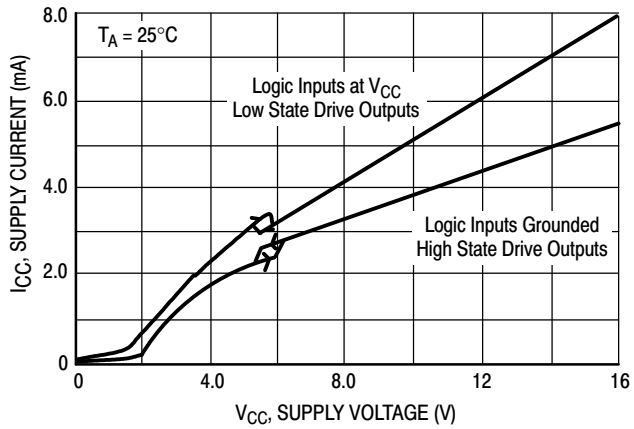


Figure 17. Supply Current versus Supply Voltage

APPLICATIONS INFORMATION

Description

The MC34151 is a dual inverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to V_{CC} making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to V_{CC}. This allows the output of one channel to directly drive the input of a second channel for master−slave operation. Each input has a 30 kΩ pulldown resistor so that an unconnected open input will cause the associated Drive Output to be in a known high state.

Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical ‘on’ resistance of 2.4 Ω at 1.0 A. The low ‘on’ resistance allows high output currents to be attained at a lower V_{CC} than with comparative CMOS drivers. Each output has a 100 kΩ pulldown resistor to keep the MOSFET gate low when V_{CC} is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to V_{CC} or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above V_{CC} during the turn−on transition, and below ground during the turn−off transition. With CMOS drivers, this mode of operation can cause a destructive output latchup condition. The MC34151 is immune to output latchup. The Drive Outputs contain an internal diode to V_{CC} for clamping positive voltage transients. When operating with V_{CC} at 18 V, proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pullup transistor. Since full supply voltage is applied across

the NPN pullup during the negative output transient, power dissipation at high frequencies can become excessive. Figures 20, 21, and 22 show a method of using external Schottky diode clamps to reduce driver power dissipation.

Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as V_{CC} rises from 1.4 V to the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V, yielding about 500 mV of hysteresis.

Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D (R_{\theta JA})$$

where:
T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
$R_{\theta JA}$ = Thermal Resistance Junction to Ambient

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$P_D = P_Q + P_C + P_T$$

where:
P_Q = Quiescent Power Dissipation
P_C = Capacitive Load Power Dissipation
P_T = Transition Power Dissipation

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 17. The device's quiescent power dissipation is:

$$P_Q = V_{CC} \left(I_{CCL} (1-D) + I_{CCH} (D) \right)$$

where:
I_{CCL} = Supply Current with Low State Drive Outputs
I_{CCH} = Supply Current with High State Drive Outputs
D = Output Duty Cycle

The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$$P_C = V_{CC} (V_{OH} - V_{OL}) C_L f$$

where:
V_{OH} = High State Drive Output Voltage
V_{OL} = Low State Drive Output Voltage
C_L = Load Capacitance
f = frequency

When driving a MOSFET, the calculation of capacitive load power P_C is somewhat complicated by the changing gate to source capacitance C_{GS} as the device switches. To aid in this calculation, power MOSFET manufacturers provide gate charge information on their data sheets. Figure 18 shows a curve of gate voltage versus gate charge for the ON Semiconductor MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on', the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge Q_g of 110 nC is required when operating the MOSFET with a drain to source voltage V_{DS} of 400 V.

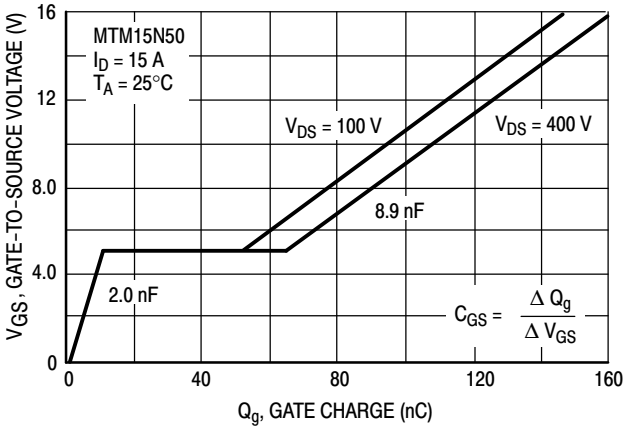


Figure 18. Gate−To−Source Voltage versus Gate Charge

The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$P_{C(MOSFET)} = V_C Q_g f$$

The flat region from 10 nC to 55 nC is caused by the drain−to−gate Miller capacitance, occurring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34151 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34151 at a higher V_{CC}, additional charge can be provided to bring the gate above 10 V. This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$P_T = V_{CC} (1.08 V_{CC} C_L f - 8 \text{ y } 10^{-4})$$

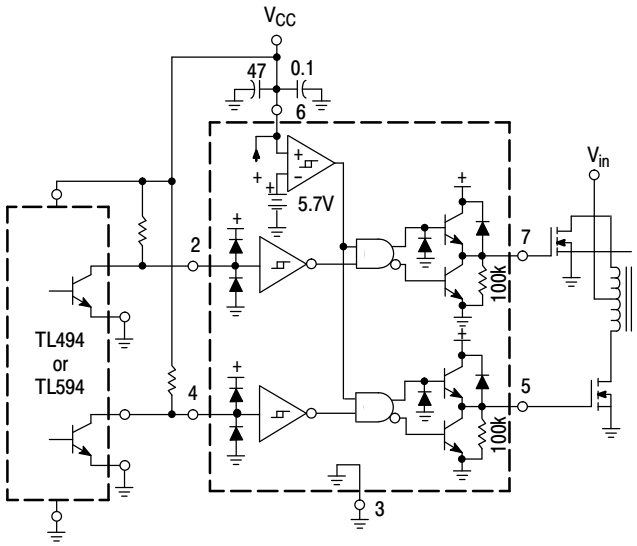
P_T must be greater than zero.

Switching time characterization of the MC34151 is performed with fixed capacitive loads. Figure 14 shows that for small capacitance loads, the switching speed is limited by transistor turn−on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

LAYOUT CONSIDERATIONS

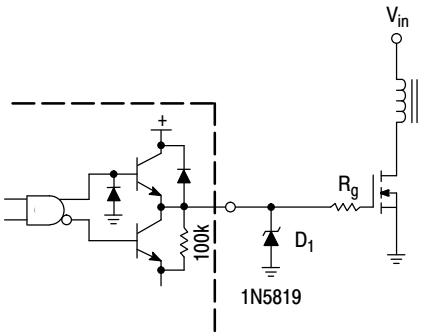
High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire–wrap or plug–in prototype boards.** When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the V_{CC} pin and ground as the layout will permit. Suggested capacitors are a low inductance 0.1 μF ceramic in parallel with a 4.7 μF tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

Proper printed circuit board layout is extremely critical and cannot be over emphasized.



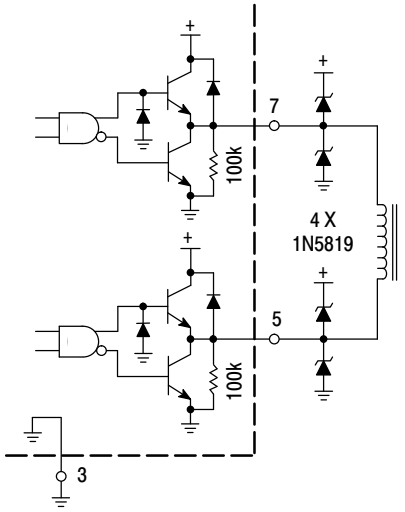
The MC34151 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

Figure 19. Enhanced System Performance with Common Switching Regulators



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 20. MOSFET Parasitic Oscillations



Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above V_{CC} and below ground.

Figure 21. Direct Transformer Drive

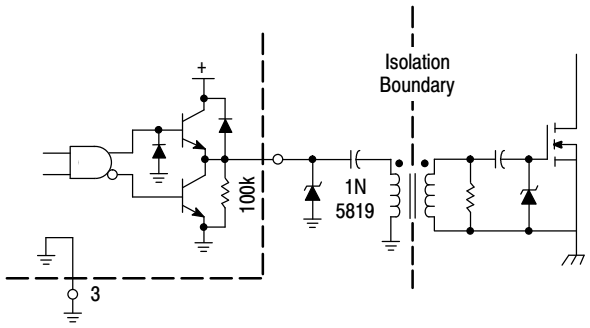
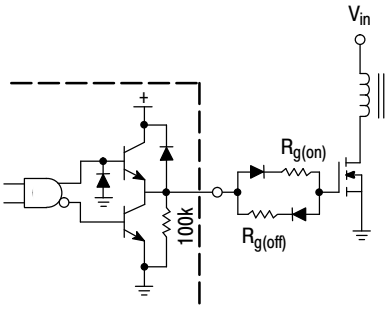
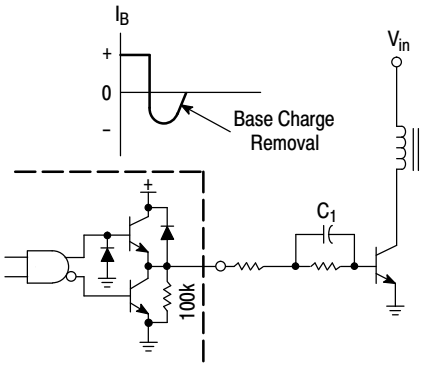


Figure 22. Isolated MOSFET Drive



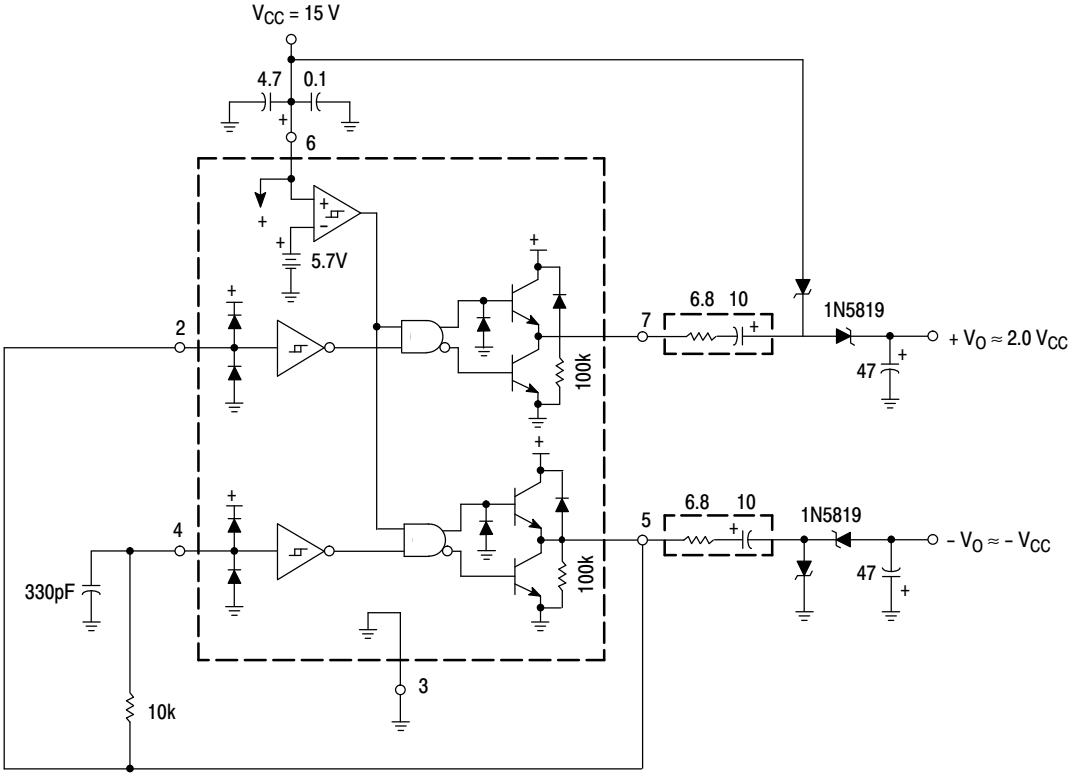
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn−on and turn−off times.

Figure 23. Controlled MOSFET Drive



The totem−pole outputs can furnish negative base current for enhanced transistor turn−off, with the addition of capacitor C_1.

Figure 24. Bipolar Transistor Drive



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Figure 25. Dual Charge Pump Converter

Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	27.7	−13.3
1.0	27.4	−12.9
10	26.4	−11.9
20	25.5	−11.2
30	24.6	−10.5
50	22.6	−9.4

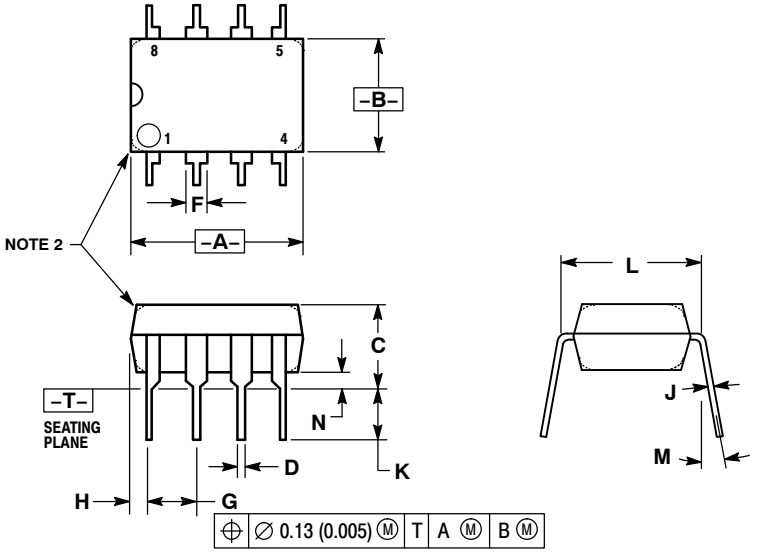
ORDERING INFORMATION

Device	Package	Shipping†
MC34151D	SOIC−8	98 Units / Rail
MC34151DG	SOIC−8 (Pb−Free)	98 Units / Rail
MC34151DR2	SOIC−8	2500 Tape & Reel
MC34151DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel
MC34151P	PDIP−8	50 Units / Rail
MC34151PG	PDIP−8 (Pb−Free)	50 Units / Rail
MC33151D	SOIC−8	98 Units / Rail
MC33151DG	SOIC−8 (Pb−Free)	98 Units / Rail
MC33151DR2	SOIC−8	2500 Tape & Reel
MC33151DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel
MC33151P	PDIP−8	50 Units / Rail
MC33151PG	PDIP−8 (Pb−Free)	50 Units / Rail
MC33151VD	SOIC−8	98 Units / Rail
MC33151VDR2	SOIC−8	2500 Tape & Reel
MC33151VDR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

PDIP−8
P SUFFIX
CASE 626−05
ISSUE L

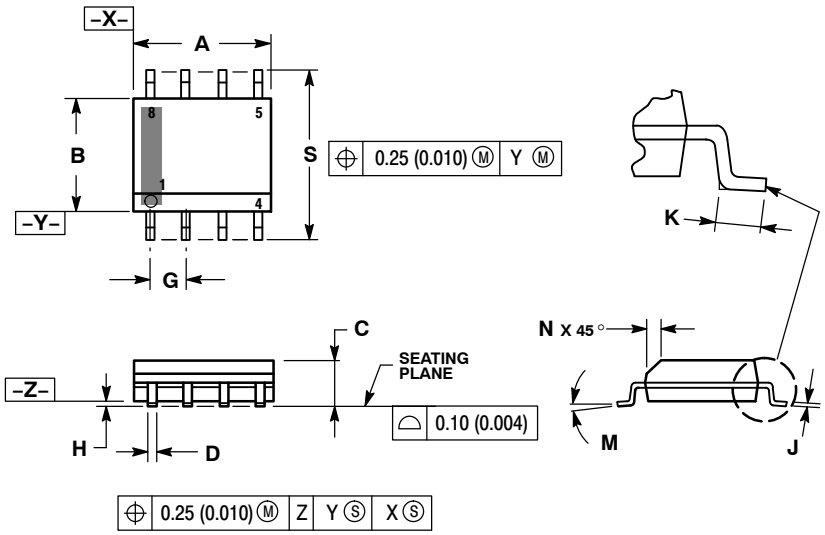


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

PACKAGE DIMENSIONS

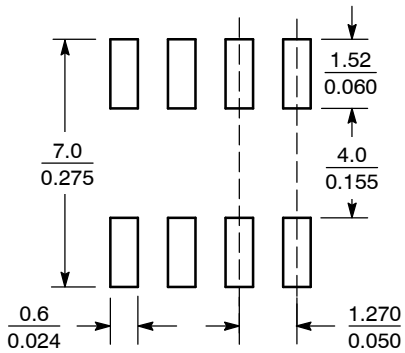
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AJ



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

SPECIFICATIONS FOR NICHIA **BLUE** LED

MODEL : **NSPB546DS**

NICHIA CORPORATION

1.SPECIFICATIONS

(1) Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Absolute Maximum Rating	Unit
Forward Current	I_F	35	mA
Pulse Forward Current	I_{FP}	110	mA
Reverse Voltage	V_R	5	V
Power Dissipation	P_D	123	mW
Operating Temperature	T_{opr}	-30 ~ + 85	°C
Storage Temperature	T_{stg}	-40 ~ +100	°C
Soldering Temperature	T_{sld}	265°C for 10sec.	

I_{FP} Conditions : Pulse Width ≤ 10msec. and Duty ≤ 1/10

(2) Initial Electrical/Optical Characteristics (Ta=25°C)

Item		Symbol	Condition	Typ.	Max.	Unit
Forward Voltage		V_F	I_F=20[mA]	(3.2)	3.5	V
Reverse Current		I_R	V_R= 5[V]	-	50	μA
Luminous Intensity		Iv	I_F=20[mA]	(970)(new)*1	-	mcd
Luminous Intensity		Iv	I_F=20[mA]	(1200)(old)*2	-	mcd
Chromaticity Coordinate*	x	-	I_F=20[mA]	0.133	-	-
	y	-	I_F=20[mA]	0.075	-	-

＊ Please refer to CIE 1931 chromaticity diagram.

＊1 Changed previously listed luminous intensity values (see ＊2) to luminous intensity values traceable to the current national standards on and after August 1, 2008.
(In accordance with CIE 127:2007)

(3) Ranking (Ta=25°C)

Item		Symbol	Condition	Min.	Max.	Unit
Luminous Intensity (new)*1	Rank V	Iv	I_F=20[mA]	980	1390	mcd
	Rank U	Iv	I_F=20[mA]	690	980	mcd
	Rank T	Iv	I_F=20[mA]	480	690	mcd

(Ta=25°C)

Item		Symbol	Condition	Min.	Max.	Unit
Luminous Intensity (old)*2	Rank V	Iv	I_F=20[mA]	1210	1720	mcd
	Rank U	Iv	I_F=20[mA]	860	1210	mcd
	Rank T	Iv	I_F=20[mA]	600	860	mcd

＊ Luminous Intensity Measurement allowance is ± 10%.

Color Rank (IF=20mA,Ta=25°C)

	Rank W			
x	0.11	0.11	0.15	0.15
y	0.04	0.10	0.10	0.04

∗ Color Coordinates Measurement allowance is ± 0.01.

∗ Basically, a shipment shall consist of the LEDs of a combination of the above ranks.
The percentage of each rank in the shipment shall be determined by Nichia.

2.INITIAL OPTICAL/ELECTRICAL CHARACTERISTICS

Please refer to "CHARACTERISTICS" on the following pages.

3.OUTLINE DIMENSIONS AND MATERIALS

Please refer to "OUTLINE DIMENSIONS" on the following page.

Material as follows ;

Resin	:	Epoxy Resin
Lens Color	:	Blue (Diffusion type)
Leadframe	:	Ag plating Copper Alloy

4.PACKAGING

· The LEDs are packed in cardboard boxes after packaging in anti-electrostatic bags.
Please refer to "PACKING" on the following pages.
The label on the minimum packing unit shows ; Part Number, Lot Number, Ranking, Quantity
· In order to protect the LEDs from mechanical shock, we pack them in cardboard boxes for transportation.
· The LEDs may be damaged if the boxes are dropped or receive a strong impact against them, so precautions must be taken to prevent any damage.
· The boxes are not water resistant and therefore must be kept away from water and moisture.
· When the LEDs are transported, we recommend that you use the same packing method as Nichia.

5.LOT NUMBER

The first six digits number shows **lot number**.
The lot number is composed of the following characters;

○□××××-△■

○ - Year (7 for 2007, 8 for 2008)
□ - Month (1 for Jan., 9 for Sep., A for Oct., B for Nov.)
×××× - Nichia's Product Number
△ - Ranking by Color Coordinates
■ - Ranking by Luminous Intensity

6.RELIABILITY

(1) TEST ITEMS AND RESULTS

Test Item	Standard Test Method	Test Conditions	Note	Number of Damaged
Resistance to Soldering Heat	JEITA ED-4701 300 302	Tsld=260 ± 5°C, 10sec. 3mm from the base of the epoxy bulb	1 time	0/50
Solderability	JEITA ED-4701 300 303	Tsld=235 ± 5°C, 5sec. (using flux)	1 time over 95%	0/50
Thermal Shock	JEITA ED-4701 300 307	0°C ~ 100°C 15sec. 15sec.	100 cycles	0/50
Temperature Cycle	JEITA ED-4701 100 105	-40°C ~ 25°C ~ 100°C ~ 25°C 30min. 5min. 30min. 5min.	100 cycles	0/50
Moisture Resistance Cyclic	JEITA ED-4701 200 203	25°C ~ 65°C ~ -10°C 90%RH 24hrs./1cycle	10 cycles	0/50
Terminal Strength (bending test)	JEITA ED-4701 400 401	Load 5N (0.5kgf) 0° ~ 90° ~ 0° bend 2 times	No noticeable damage	0/50
Terminal Strength (pull test)	JEITA ED-4701 400 401	Load 10N (1kgf) 10 ± 1 sec.	No noticeable damage	0/50
High Temperature Storage	JEITA ED-4701 200 201	Ta=100°C	1000hrs.	0/50
Temperature Humidity Storage	JEITA ED-4701 100 103	Ta=60°C, RH=90%	1000hrs.	0/50
Low Temperature Storage	JEITA ED-4701 200 202	Ta=-40°C	1000hrs.	0/50
Steady State Operating Life		Ta=25°C, I_F=35mA	1000hrs.	0/50
Steady State Operating Life of High Humidity Heat		60°C, RH=90%, I_F=20mA	500hrs.	0/50
Steady State Operating Life of Low Temperature		Ta=-30°C, I_F=20mA	1000hrs.	0/50

(2) CRITERIA FOR JUDGING DAMAGE

Item	Symbol	Test Conditions	Criteria for Judgement	
			Min.	Max.
Forward Voltage	V_F	I_F=20mA	-	U.S.L.*)× 1.1
Reverse Current	I_R	V_R=5V	-	U.S.L.*)× 2.0
Luminous Intensity	I_V	I_F=20mA	L.S.L.**)× 0.7	-

*) U.S.L. : Upper Standard Level **) L.S.L. : Lower Standard Level

7.CAUTIONS

(1) Lead Forming

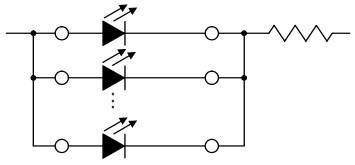
· When forming leads, the leads should be bent at a point at least 3mm from the base of the epoxy bulb. Do not use the base of the leadframe as a fulcrum during lead forming.
· Lead forming should be done before soldering.
· Do not apply any bending stress to the base of the lead. The stress to the base may damage the LED's characteristics or it may break the LEDs.
· When mounting the LEDs onto a printed circuit board, the holes on the circuit board should be exactly aligned with the leads of the LEDs. If the LEDs are mounted with stress at the leads, it causes deterioration of the epoxy resin and this will degrade the LEDs.

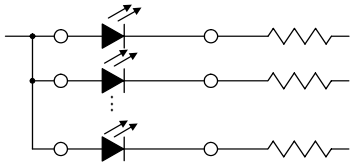
(2) Storage

· The LEDs should be stored at 30°C or less and 70%RH or less after being shipped from Nichia and the storage life limits are 3 months. If the LEDs are stored for 3 months or more, they can be stored for a year in a sealed container with a nitrogen atmosphere and moisture absorbent material.
· Nichia LED leadframes are silver plated copper alloy. The silver surface may be affected by environments which contain corrosive substances. Please avoid conditions which may cause the LED to corrode, tarnish or discolor. This corrosion or discoloration may cause difficulty during soldering operations. It is recommended that the LEDs be used as soon as possible.
· Please avoid rapid transitions in ambient temperature, especially, in high humidity environments where condensation can occur.

(3) Recommended circuit

· In designing a circuit, the current through each LED must not exceed the absolute maximum rating specified for each LED. It is recommended to use Circuit B which regulates the current flowing through each LED. In the meanwhile, when driving LEDs with a constant voltage in Circuit A, the current through the LEDs may vary due to the variation in forward voltage (V_F) of the LEDs. In the worst case, some LED may be subjected to stresses in excess of the absolute maximum rating.

(A) 

(B) 

· This product should be operated in forward bias. A driving circuit must be designed so that the product is not subjected to either forward or reverse voltage while it is off. In particular, if a reverse voltage is continuously applied to the product, such operation can cause migration resulting in LED damage.

(4) Static Electricity

· Static electricity or surge voltage damages the LEDs.
It is recommended that a wrist band or an anti-electrostatic glove be used when handling the LEDs.
· All devices, equipment and machinery must be properly grounded. It is recommended that precautions be taken against surge voltage to the equipment that mounts the LEDs.
· When inspecting the final products in which LEDs were assembled, it is recommended to check whether the assembled LEDs are damaged by static electricity or not. It is easy to find static-damaged LEDs by a light-on test or a VF test at a lower current (below 1mA is recommended).
· Damaged LEDs will show some unusual characteristics such as the leak current remarkably increases, the forward voltage becomes lower, or the LEDs do not light at the low current.
Criteria : (V_F > 2.0V at I_F=0.5mA)

(5) Soldering Conditions

· Nichia LED leadframes are silver plated copper alloy. This substance has a low thermal coefficient (easily conducts heat). Careful attention should be paid during soldering.
· Solder the LED no closer than 3mm from the base of the epoxy bulb. Soldering beyond the base of the tie bar is recommended.
· Recommended soldering conditions

Dip Soldering		Hand Soldering	
Pre-Heat	120°C Max.	Temperature	350°C Max.
Pre-Heat Time	60 seconds Max.	Soldering Time	3 seconds Max.
Solder Bath Temperature	260°C Max.	Position	No closer than 3 mm from the base of the epoxy bulb.
Dipping Time	10 seconds Max.		
Dipping Position	No lower than 3 mm from the base of the epoxy bulb.		

· Although the recommended soldering conditions are specified in the above table, dip or hand soldering at the lowest possible temperature is desirable for the LEDs.
· A rapid-rate process is not recommended for cooling the LEDs down from the peak temperature.
· Dip soldering should not be done more than one time.
· Hand soldering should not be done more than one time.
· Do not apply any stress to the lead particularly when heated.
· The LEDs must not be repositioned after soldering.
· After soldering the LEDs, the epoxy bulb should be protected from mechanical shock or vibration until the LEDs return to room temperature.
· Direct soldering onto a PC board should be avoided. Mechanical stress to the resin may be caused from warping of the PC board or from the clinching and cutting of the leadframes. When it is absolutely necessary, the LEDs may be mounted in this fashion but the User will assume responsibility for any problems. Direct soldering should only be done after testing has confirmed that no damage, such as wire bond failure or resin deterioration, will occur. Nichia's LEDs should not be soldered directly to double sided PC boards because the heat will deteriorate the epoxy resin.
· When it is necessary to clamp the LEDs to prevent soldering failure, it is important to minimize the mechanical stress on the LEDs.
· Cut the LED leadframes at room temperature. Cutting the leadframes at high temperatures may cause failure of the LEDs.

(6) Heat Generation

· Thermal design of the end product is of paramount importance. Please consider the heat generation of the LED when making the system design. The coefficient of temperature increase per input electric power is affected by the thermal resistance of the circuit board and density of LED placement on the board, as well as other components. It is necessary to avoid intense heat generation and operate within the maximum ratings given in this specification.
· The operating current should be decided after considering the ambient maximum temperature of LEDs.

(7) Cleaning

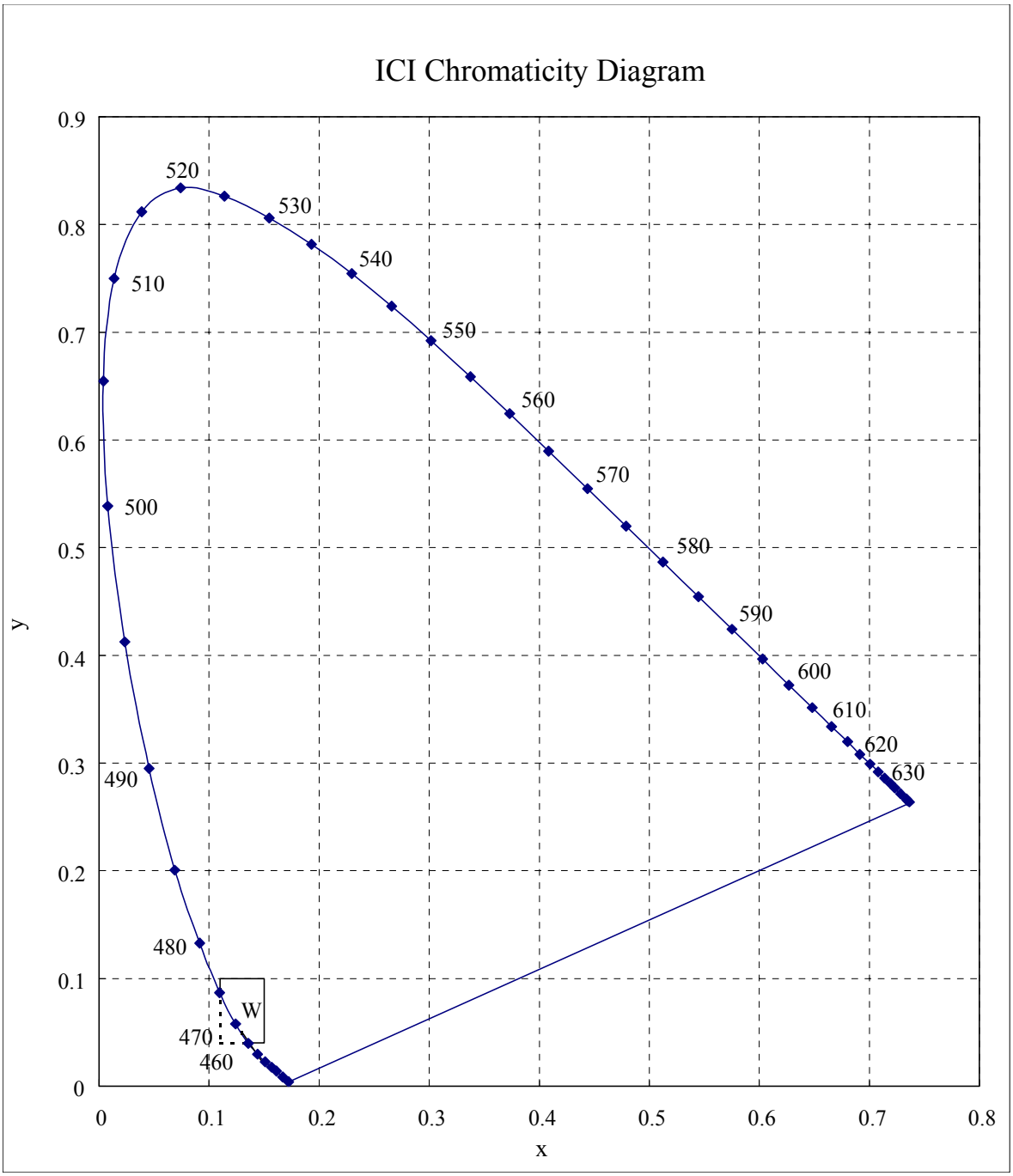
· It is recommended that isopropyl alcohol be used as a solvent for cleaning the LEDs. When using other solvents, it should be confirmed beforehand whether the solvents will dissolve the resin or not. Freon solvents should not be used to clean the LEDs because of worldwide regulations.
· Do not clean the LEDs by the ultrasonic. When it is absolutely necessary, the influence of ultrasonic cleaning on the LEDs depends on factors such as ultrasonic power and the assembled condition. Before cleaning, a pre-test should be done to confirm whether any damage to the LEDs will occur.

(8) Safety Guideline for Human Eyes

· The International Electrical Commission (IEC) published in 2006 IEC 62471:*2006 Photobiological safety of lamps and lamp systems* which includes LEDs within its scope. Meanwhile LEDs were removed from the scope of the IEC 60825-1:2007 laser safety standard, the 2001 edition of which included LED sources within its scope. However, keep in mind that some countries and regions have adopted standards based on the IEC laser safety standard IEC 60825-1:2001 which includes LEDs within its scope.
Following IEC 62471:2006, most of Nichia LEDs can be classified as belonging to either Exempt Group or Risk Group 1. Optical characteristics of a LED such as output power, spectrum and light distribution are factors that affect the risk group determination of the LED. Especially a high-power LED, that emits light containing blue wavelengths, may be in Risk Group 2.
Great care should be taken when viewing directly the LED driven at high current or the LED with optical instruments, which may greatly increase the hazard to your eyes.

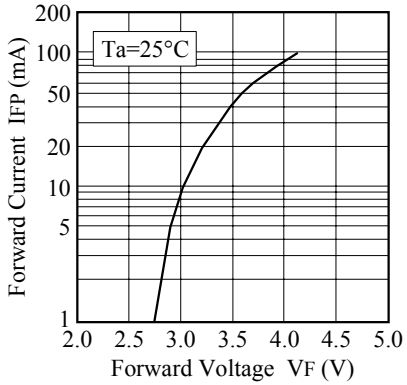
(9) Others

· NSPB546DS complies with RoHS Directive.
· Care must be taken to ensure that the reverse voltage will not exceed the absolute maximum rating when using the LEDs with matrix drive.
· Flashing lights have been known to cause discomfort in people; you can prevent this by taking precautions during use. Also, people should be cautious when using equipment that has had LEDs incorporated into it.
· The LEDs described in this brochure are intended to be used for ordinary electronic equipment (such as office equipment, communications equipment, measurement instruments and household appliances). Consult Nichia's sales staff in advance for information on the applications in which exceptional quality and reliability are required, particularly when the failure or malfunction of the LEDs may directly jeopardize life or health (such as for airplanes, aerospace, submersible repeaters, nuclear reactor control systems, automobiles, traffic control equipment, life support systems and safety devices).
· User shall not reverse engineer by disassembling or analysis of the LEDs without having prior written consent from Nichia. When defective LEDs are found, the User shall inform Nichia directly before disassembling or analysis.
· The formal specifications must be exchanged and signed by both parties before large volume purchase begins.
· The appearance and specifications of the product may be modified for improvement without notice.

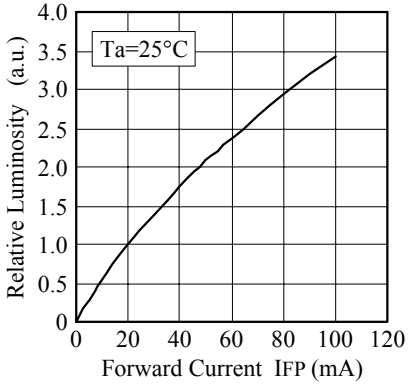


∗ Color Coordinates Measurement allowance is ± 0.01.

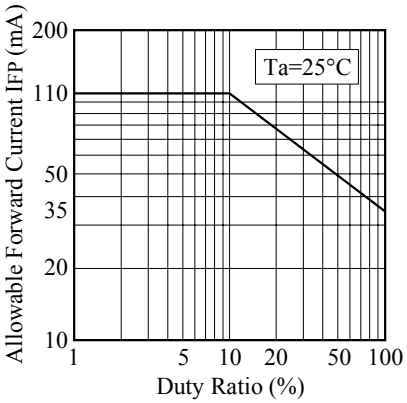
■ Forward Voltage vs. Forward Current



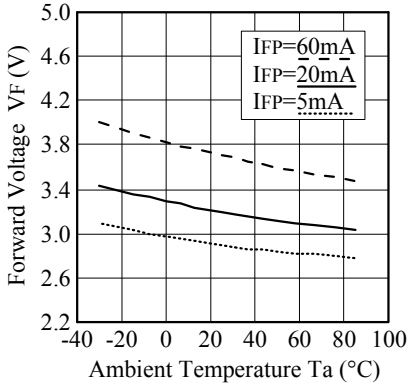
■ Forward Current vs. Relative Luminosity



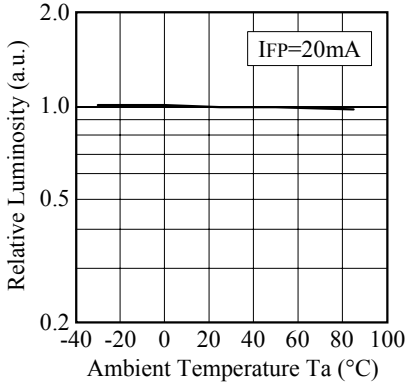
■ Duty Ratio vs. Allowable Forward Current



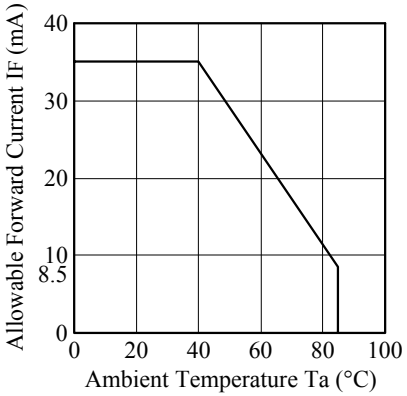
■ Ambient Temperature vs. Forward Voltage



■ Ambient Temperature vs. Relative Luminosity



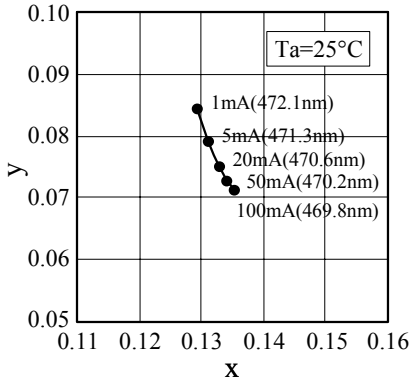
■ Ambient Temperature vs. Allowable Forward Current



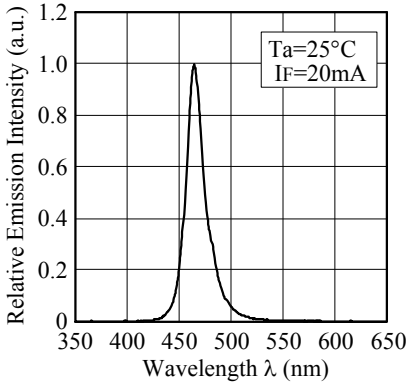
NICHIA CORPORATION	Model	NSPBxxxx
	Title	CHARACTERISTICS
	No.	060721654451

Nichia STS-DA1-0206
<Cat.No.080512>

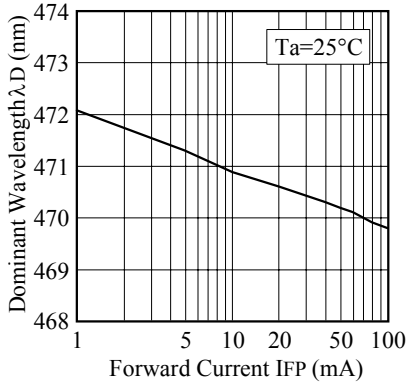
■ Forward Current vs. Chromaticity Coordinate (λ_D)



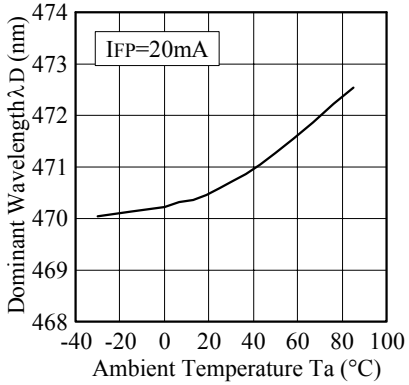
■ Spectrum



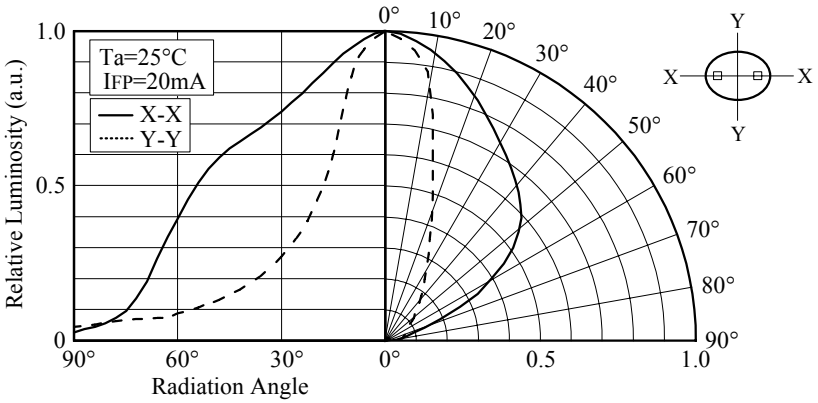
■ Forward Current vs. Dominant Wavelength



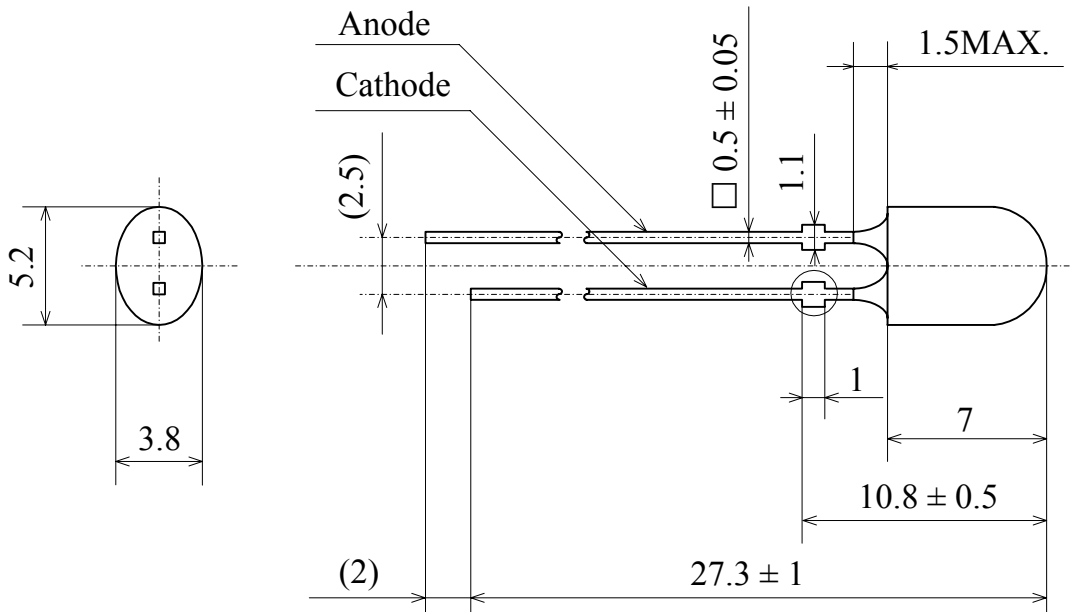
■ Ambient Temperature vs. Dominant Wavelength

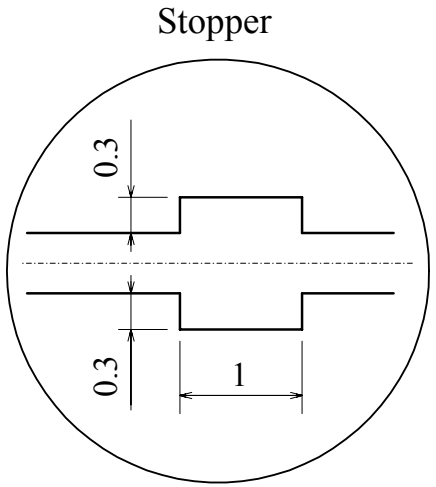


■ Directivity



NICHIA CORPORATION	Model	NSPB546DS
	Title	CHARACTERISTICS
	No.	060721654461



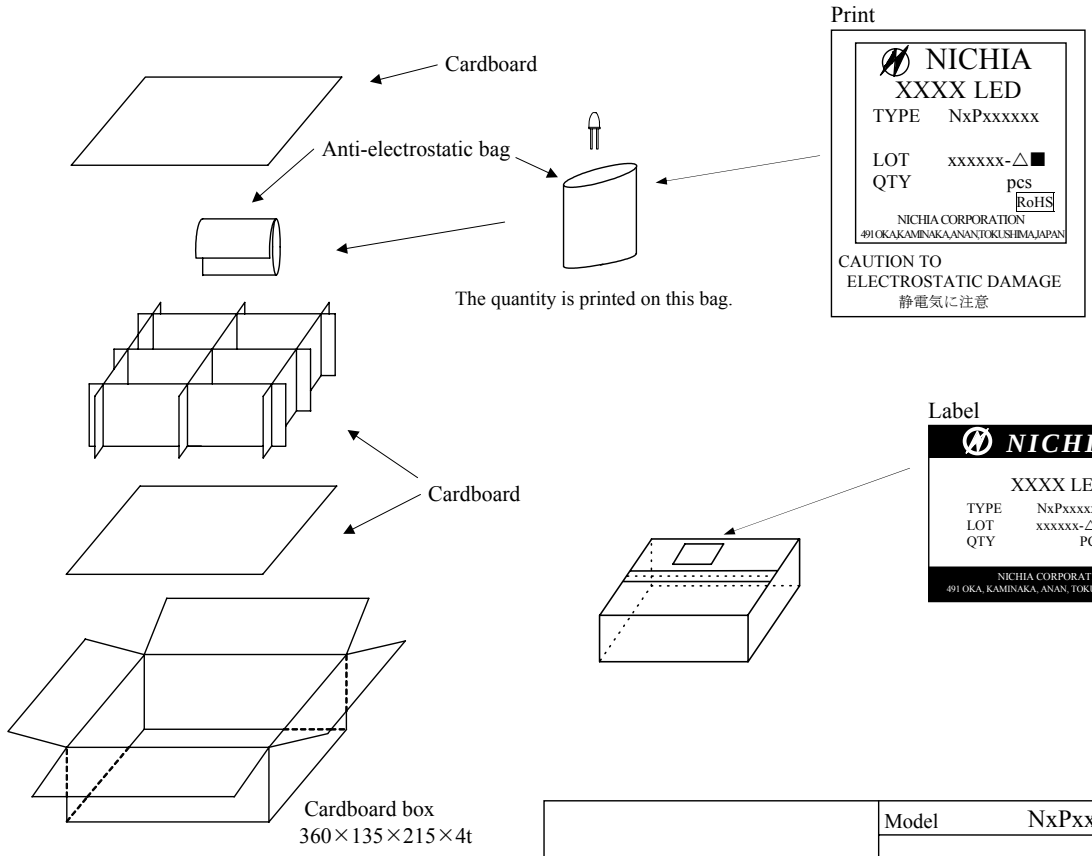


ITEM	MATERIALS
RESIN	Epoxy Resin
LENS COLOR	Blue (Diffusion type)
LEAD FRAME	Ag Plating Copper Alloy

Remark:

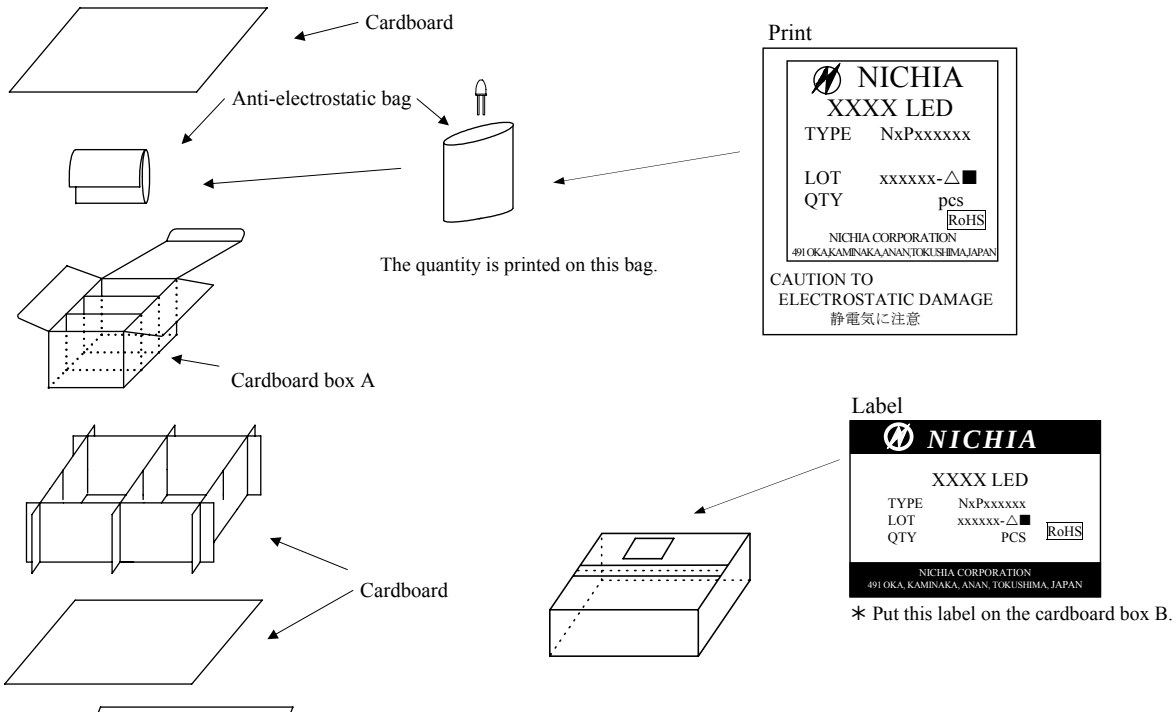
Please note that the bare copper alloy showing at the cut end of the lead frame may be corroded under certain conditions. LEDs have some sharp edges and points, particularly lead frames. Please handle with care so as to avoid injuries.

NICHIA CORPORATION	Model	NSPB546DS	Unit mm
	Title	OUTLINE DIMENSIONS	3/1 Scale
	No.	080508815881	Allow ±0.2



∗ One box contains 8 bags at maximum.

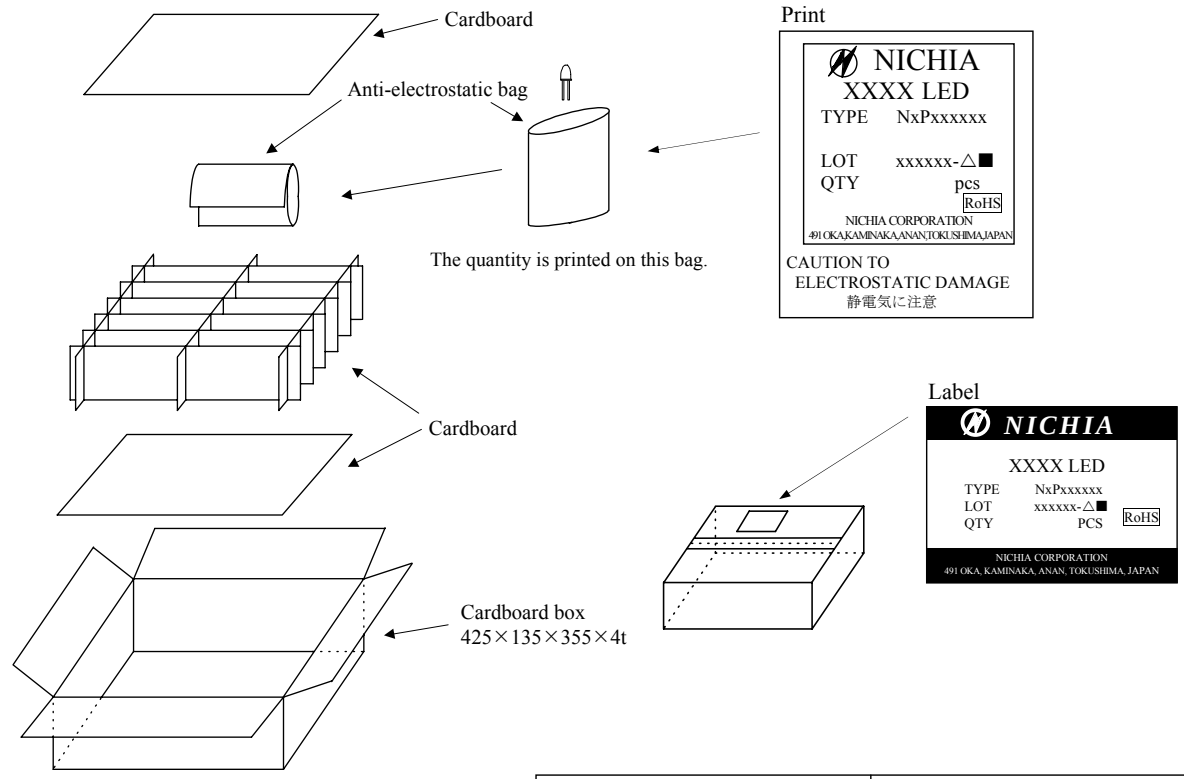
NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659112



∗ Put this label on the cardboard box B.

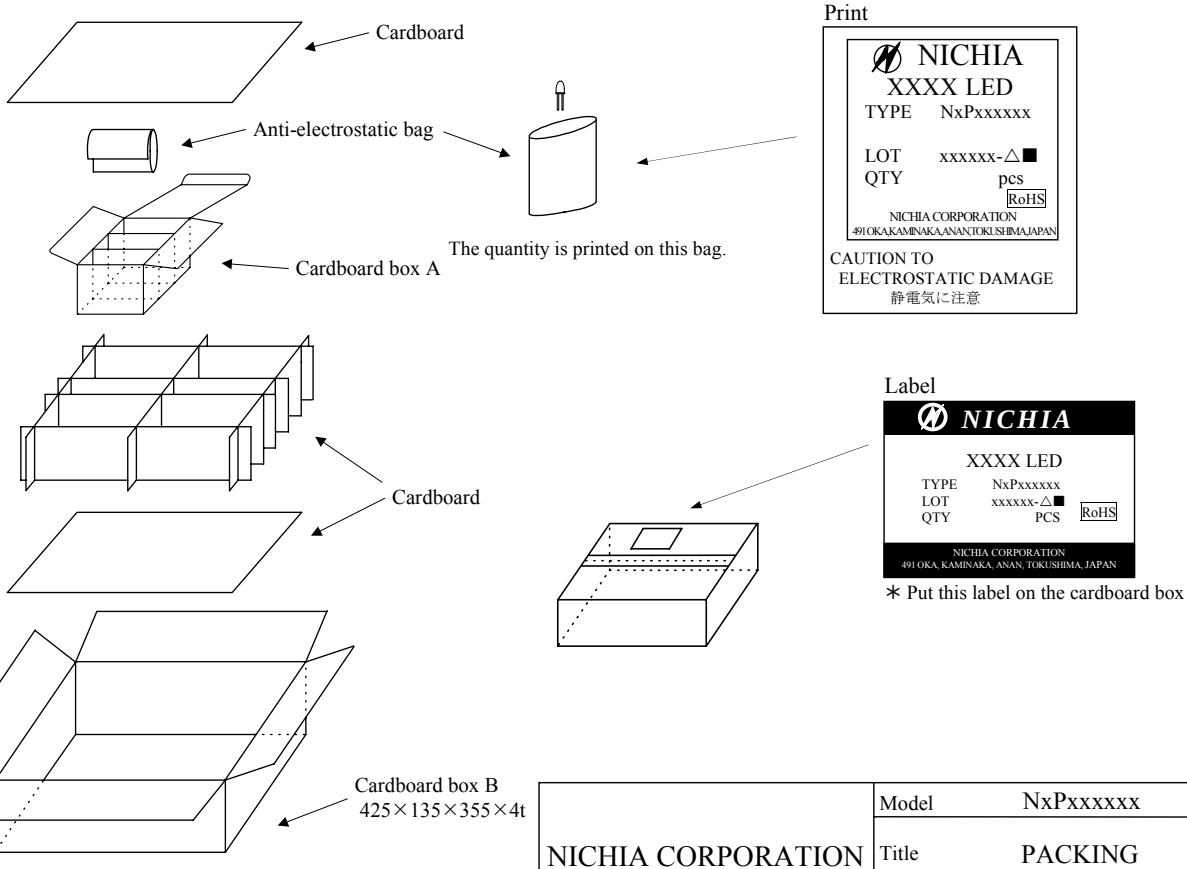
∗ The cardboard box B contains
2 cardboard box A at maximum.

NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659122



∗ One box contains 20 bags at maximum.

NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659132



∗ Put this label on the cardboard box B.

∗ The cardboard box B contains 4 cardboard box A at maximum.

NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659142

SPECIFICATIONS FOR NICHIA **GREEN** LED

MODEL : **NSPG546GS**

NICHIA CORPORATION

1.SPECIFICATIONS

(1) Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Absolute Maximum Rating	Unit
Forward Current	I_F	35	mA
Pulse Forward Current	I_{FP}	110	mA
Reverse Voltage	V_R	5	V
Power Dissipation	P_D	123	mW
Operating Temperature	T_{opr}	-30 ~ + 85	°C
Storage Temperature	T_{stg}	-40 ~ +100	°C
Soldering Temperature	T_{sld}	265°C for 10sec.	

I_{FP} Conditions : Pulse Width ≤ 10msec. and Duty ≤ 1/10

(2) Initial Electrical/Optical Characteristics (Ta=25°C)

Item		Symbol	Condition	Typ.	Max.	Unit
Forward Voltage		V_F	I_F=20[mA]	(3.2)	3.5	V
Reverse Current		I_R	V_R= 5[V]	-	50	μA
Luminous Intensity		Iv	I_F=20[mA]	(3635)(new)*1	-	mcd
Luminous Intensity		Iv	I_F=20[mA]	(4400)(old)*2	-	mcd
Chromaticity Coordinate*	x	-	I_F=20[mA]	0.189	-	-
	y	-	I_F=20[mA]	0.718	-	-

＊ Please refer to CIE 1931 chromaticity diagram.

＊1 Changed previously listed luminous intensity values (see ＊2) to luminous intensity values traceable to the current national standards on and after August 1, 2008.
(In accordance with CIE 127:2007)

(3) Ranking (Ta=25°C)

Item		Symbol	Condition	Min.	Max.	Unit
Luminous Intensity (new)*1	Rank V	Iv	I_F=20[mA]	3420	4760	mcd
	Rank U	Iv	I_F=20[mA]	2380	3420	mcd
	Rank T	Iv	I_F=20[mA]	1710	2380	mcd

(Ta=25°C)

Item		Symbol	Condition	Min.	Max.	Unit
Luminous Intensity (old)*2	Rank V	Iv	I_F=20[mA]	4140	5760	mcd
	Rank U	Iv	I_F=20[mA]	2880	4140	mcd
	Rank T	Iv	I_F=20[mA]	2070	2880	mcd

＊ Luminous Intensity Measurement allowance is ± 10%.

Color Ranks (I_F=20mA,Ta=25°C)

	Rank G0e					
x	0.156	0.127	0.159	0.203	0.222	0.184
y	0.676	0.733	0.750	0.750	0.688	0.690

	Rank Hc				
x	0.222	0.203	0.249	0.266	0.274
y	0.688	0.750	0.738	0.724	0.677

∗ Color Coordinates Measurement allowance is ± 0.01.

∗ Basically, a shipment shall consist of the LEDs of a combination of the above ranks.
The percentage of each rank in the shipment shall be determined by Nichia.

2.INITIAL OPTICAL/ELECTRICAL CHARACTERISTICS

Please refer to “CHARACTERISTICS” on the following pages.

3.OUTLINE DIMENSIONS AND MATERIALS

Please refer to “OUTLINE DIMENSIONS” on the following page.

Material as follows ; Resin : Epoxy Resin
Lens Color : Green (Diffusion type)
Leadframe : Ag plating Copper Alloy

4.PACKAGING

· The LEDs are packed in cardboard boxes after packaging in anti-electrostatic bags.
Please refer to “PACKING” on the following pages.
The label on the minimum packing unit shows ; Part Number, Lot Number, Ranking, Quantity
· In order to protect the LEDs from mechanical shock, we pack them in cardboard boxes for transportation.
· The LEDs may be damaged if the boxes are dropped or receive a strong impact against them, so precautions must be taken to prevent any damage.
· The boxes are not water resistant and therefore must be kept away from water and moisture.
· When the LEDs are transported, we recommend that you use the same packing method as Nichia.

5.LOT NUMBER

The first six digits number shows **lot number**.
The lot number is composed of the following characters;

○□××××-△■

○ - Year (7 for 2007, 8 for 2008)
□ - Month (1 for Jan., 9 for Sep., A for Oct., B for Nov.)
×××× - Nichia's Product Number
△ - Ranking by Color Coordinates
■ - Ranking by Luminous Intensity

6.RELIABILITY

(1) TEST ITEMS AND RESULTS

Test Item	Standard Test Method	Test Conditions	Note	Number of Damaged
Resistance to Soldering Heat	JEITA ED-4701 300 302	Tsld=260 ± 5°C, 10sec. 3mm from the base of the epoxy bulb	1 time	0/50
Solderability	JEITA ED-4701 300 303	Tsld=235 ± 5°C, 5sec. (using flux)	1 time over 95%	0/50
Temperature Cycle	JEITA ED-4701 100 105	-40°C ~ 25°C ~ 100°C ~ 25°C 30min. 5min. 30min. 5min.	100 cycles	0/50
Moisture Resistance Cyclic	JEITA ED-4701 200 203	25°C ~ 65°C ~ -10°C 90%RH 24hrs./1cycle	10 cycles	0/50
Terminal Strength (bending test)	JEITA ED-4701 400 401	Load 5N (0.5kgf) 0° ~ 90° ~ 0° bend 2 times	No noticeable damage	0/50
Terminal Strength (pull test)	JEITA ED-4701 400 401	Load 10N (1kgf) 10 ± 1 sec.	No noticeable damage	0/50
High Temperature Storage	JEITA ED-4701 200 201	Ta=100°C	1000hrs.	0/50
Temperature Humidity Storage	JEITA ED-4701 100 103	Ta=60°C, RH=90%	1000hrs.	0/50
Low Temperature Storage	JEITA ED-4701 200 202	Ta=-40°C	1000hrs.	0/50
Steady State Operating Life		Ta=25°C, I_F=35mA	1000hrs.	0/50
Steady State Operating Life of High Humidity Heat		60°C, RH=90%, I_F=20mA	500hrs.	0/50
Steady State Operating Life of Low Temperature		Ta=-30°C, I_F=20mA	1000hrs.	0/50

(2) CRITERIA FOR JUDGING DAMAGE

Item	Symbol	Test Conditions	Criteria for Judgement	
			Min.	Max.
Forward Voltage	V_F	I_F=20mA	-	U.S.L.*)× 1.1
Reverse Current	I_R	V_R=5V	-	U.S.L.*)× 2.0
Luminous Intensity	I_V	I_F=20mA	L.S.L.**)× 0.7	-

*) U.S.L. : Upper Standard Level **) L.S.L. : Lower Standard Level

7.CAUTIONS

(1) Lead Forming

· When forming leads, the leads should be bent at a point at least 3mm from the base of the epoxy bulb. Do not use the base of the leadframe as a fulcrum during lead forming.
· Lead forming should be done before soldering.
· Do not apply any bending stress to the base of the lead. The stress to the base may damage the LED's characteristics or it may break the LEDs.
· When mounting the LEDs onto a printed circuit board, the holes on the circuit board should be exactly aligned with the leads of the LEDs. If the LEDs are mounted with stress at the leads, it causes deterioration of the epoxy resin and this will degrade the LEDs.

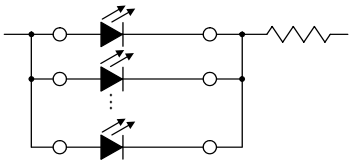
(2) Storage

· The LEDs should be stored at 30°C or less and 70%RH or less after being shipped from Nichia and the storage life limits are 3 months. If the LEDs are stored for 3 months or more, they can be stored for a year in a sealed container with a nitrogen atmosphere and moisture absorbent material.
· Nichia LED leadframes are silver plated copper alloy. The silver surface may be affected by environments which contain corrosive substances. Please avoid conditions which may cause the LED to corrode, tarnish or discolor. This corrosion or discoloration may cause difficulty during soldering operations. It is recommended that the LEDs be used as soon as possible.
· Please avoid rapid transitions in ambient temperature, especially, in high humidity environments where condensation can occur.

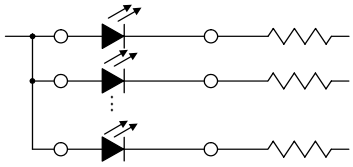
(3) Recommended circuit

· In designing a circuit, the current through each LED must not exceed the absolute maximum rating specified for each LED. It is recommended to use Circuit B which regulates the current flowing through each LED. In the meanwhile, when driving LEDs with a constant voltage in Circuit A, the current through the LEDs may vary due to the variation in forward voltage (V_F) of the LEDs. In the worst case, some LED may be subjected to stresses in excess of the absolute maximum rating.

(A)



(B)



· This product should be operated in forward bias. A driving circuit must be designed so that the product is not subjected to either forward or reverse voltage while it is off. In particular, if a reverse voltage is continuously applied to the product, such operation can cause migration resulting in LED damage.

(4) Static Electricity

· Static electricity or surge voltage damages the LEDs.
It is recommended that a wrist band or an anti-electrostatic glove be used when handling the LEDs.
· All devices, equipment and machinery must be properly grounded. It is recommended that precautions be taken against surge voltage to the equipment that mounts the LEDs.
· When inspecting the final products in which LEDs were assembled, it is recommended to check whether the assembled LEDs are damaged by static electricity or not. It is easy to find static-damaged LEDs by a light-on test or a VF test at a lower current (below 1mA is recommended).
· Damaged LEDs will show some unusual characteristics such as the leak current remarkably increases, the forward voltage becomes lower, or the LEDs do not light at the low current.
Criteria : (V_F > 2.0V at I_F=0.5mA)

(5) Soldering Conditions

· Nichia LED leadframes are silver plated copper alloy. This substance has a low thermal coefficient (easily conducts heat). Careful attention should be paid during soldering.
· Solder the LED no closer than 3mm from the base of the epoxy bulb. Soldering beyond the base of the tie bar is recommended.
· Recommended soldering conditions

Dip Soldering		Hand Soldering	
Pre-Heat	120°C Max.	Temperature	350°C Max.
Pre-Heat Time	60 seconds Max.	Soldering Time	3 seconds Max.
Solder Bath Temperature	260°C Max.	Position	No closer than 3 mm from the base of the epoxy bulb.
Dipping Time	10 seconds Max.		
Dipping Position	No lower than 3 mm from the base of the epoxy bulb.		

· Although the recommended soldering conditions are specified in the above table, dip or hand soldering at the lowest possible temperature is desirable for the LEDs.
· A rapid-rate process is not recommended for cooling the LEDs down from the peak temperature.
· Dip soldering should not be done more than one time.
· Hand soldering should not be done more than one time.
· Do not apply any stress to the lead particularly when heated.
· The LEDs must not be repositioned after soldering.
· After soldering the LEDs, the epoxy bulb should be protected from mechanical shock or vibration until the LEDs return to room temperature.
· Direct soldering onto a PC board should be avoided. Mechanical stress to the resin may be caused from warping of the PC board or from the clinching and cutting of the leadframes. When it is absolutely necessary, the LEDs may be mounted in this fashion but the User will assume responsibility for any problems. Direct soldering should only be done after testing has confirmed that no damage, such as wire bond failure or resin deterioration, will occur. Nichia's LEDs should not be soldered directly to double sided PC boards because the heat will deteriorate the epoxy resin.
· When it is necessary to clamp the LEDs to prevent soldering failure, it is important to minimize the mechanical stress on the LEDs.
· Cut the LED leadframes at room temperature. Cutting the leadframes at high temperatures may cause failure of the LEDs.

(6) Heat Generation

· Thermal design of the end product is of paramount importance. Please consider the heat generation of the LED when making the system design. The coefficient of temperature increase per input electric power is affected by the thermal resistance of the circuit board and density of LED placement on the board, as well as other components. It is necessary to avoid intense heat generation and operate within the maximum ratings given in this specification.
· The operating current should be decided after considering the ambient maximum temperature of LEDs.

(7) Cleaning

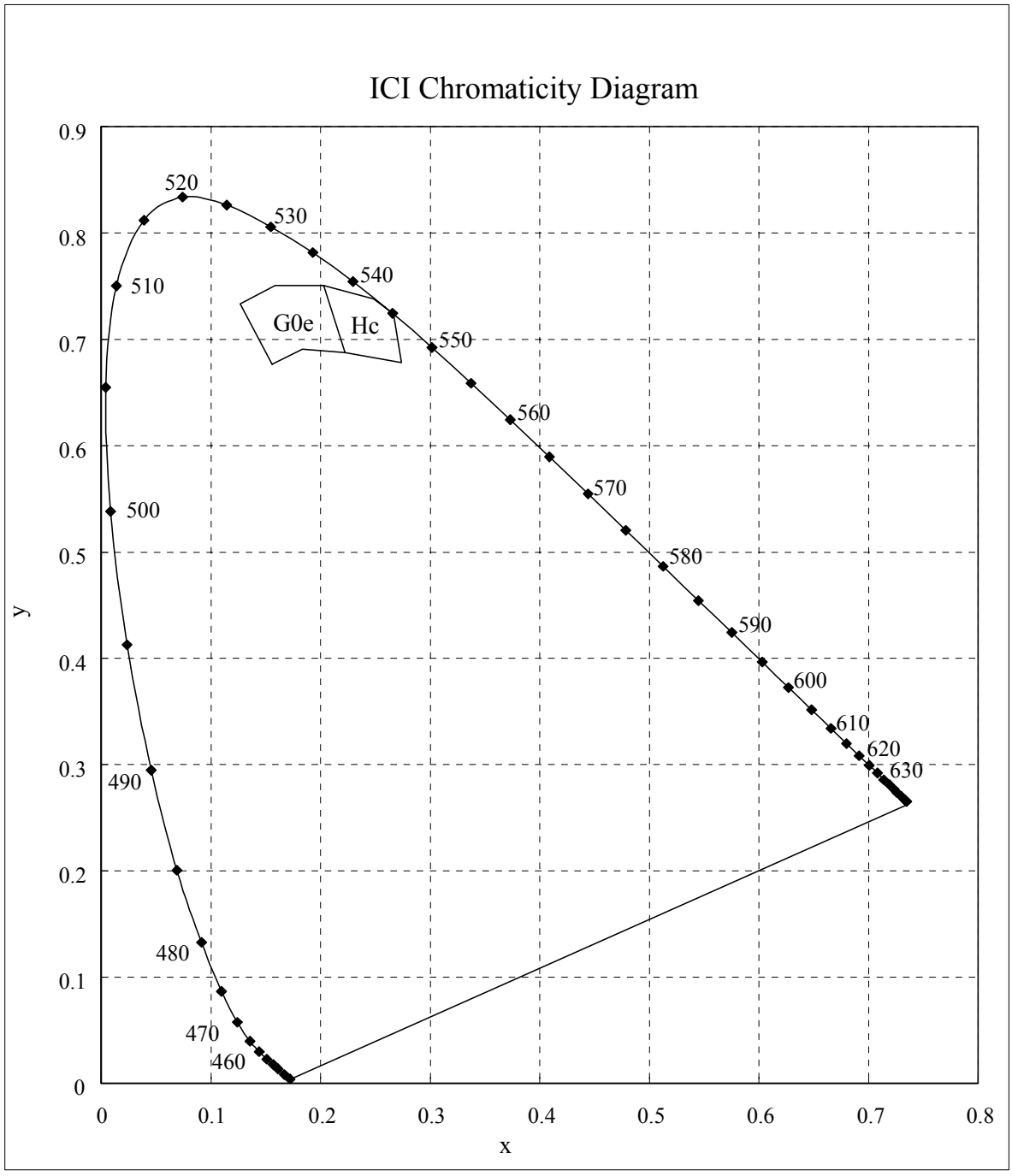
· It is recommended that isopropyl alcohol be used as a solvent for cleaning the LEDs. When using other solvents, it should be confirmed beforehand whether the solvents will dissolve the resin or not. Freon solvents should not be used to clean the LEDs because of worldwide regulations.
· Do not clean the LEDs by the ultrasonic. When it is absolutely necessary, the influence of ultrasonic cleaning on the LEDs depends on factors such as ultrasonic power and the assembled condition. Before cleaning, a pre-test should be done to confirm whether any damage to the LEDs will occur.

(8) Safety Guideline for Human Eyes

· The International Electrical Commission (IEC) published in 2006 IEC 62471:*2006 Photobiological safety of lamps and lamp systems* which includes LEDs within its scope. Meanwhile LEDs were removed from the scope of the IEC 60825-1:2007 laser safety standard, the 2001 edition of which included LED sources within its scope. However, keep in mind that some countries and regions have adopted standards based on the IEC laser safety standard IEC 60825-1:2001 which includes LEDs within its scope.
Following IEC 62471:2006, most of Nichia LEDs can be classified as belonging to either Exempt Group or Risk Group 1. Optical characteristics of a LED such as output power, spectrum and light distribution are factors that affect the risk group determination of the LED. Especially a high-power LED, that emits light containing blue wavelengths, may be in Risk Group 2.
Great care should be taken when viewing directly the LED driven at high current or the LED with optical instruments, which may greatly increase the hazard to your eyes.

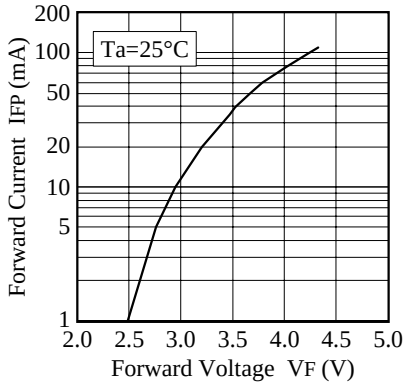
(9) Others

· NSPG546GS complies with RoHS Directive.
· Care must be taken to ensure that the reverse voltage will not exceed the absolute maximum rating when using the LEDs with matrix drive.
· Flashing lights have been known to cause discomfort in people; you can prevent this by taking precautions during use. Also, people should be cautious when using equipment that has had LEDs incorporated into it.
· The LEDs described in this brochure are intended to be used for ordinary electronic equipment (such as office equipment, communications equipment, measurement instruments and household appliances). Consult Nichia's sales staff in advance for information on the applications in which exceptional quality and reliability are required, particularly when the failure or malfunction of the LEDs may directly jeopardize life or health (such as for airplanes, aerospace, submersible repeaters, nuclear reactor control systems, automobiles, traffic control equipment, life support systems and safety devices).
· User shall not reverse engineer by disassembling or analysis of the LEDs without having prior written consent from Nichia. When defective LEDs are found, the User shall inform Nichia directly before disassembling or analysis.
· The formal specifications must be exchanged and signed by both parties before large volume purchase begins.
· The appearance and specifications of the product may be modified for improvement without notice.

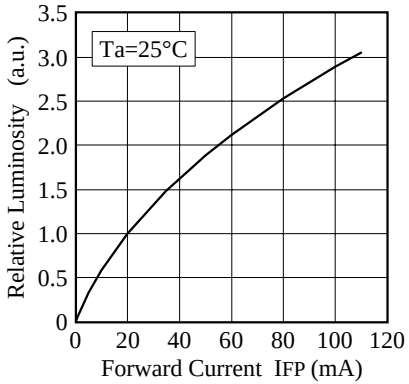


∗ Color Coordinates Measurement allowance is ± 0.01.

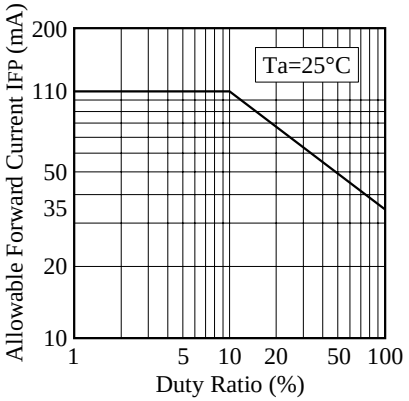
■ Forward Voltage vs. Forward Current



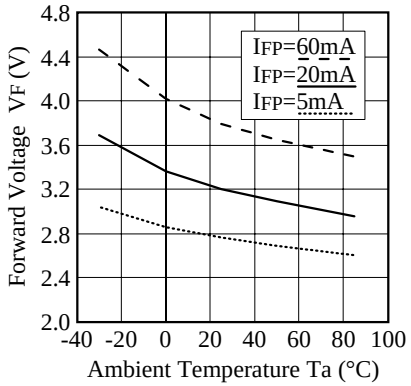
■ Forward Current vs. Relative Luminosity



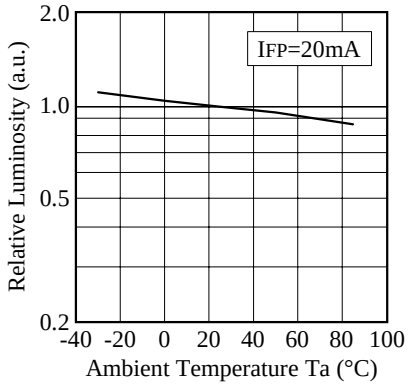
■ Duty Ratio vs. Allowable Forward Current



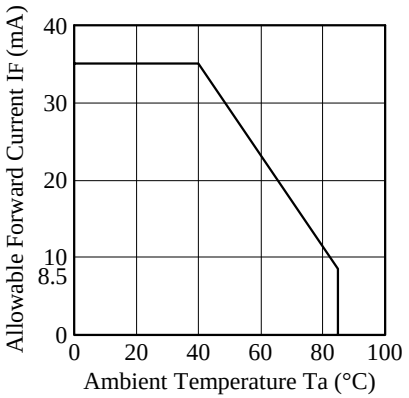
■ Ambient Temperature vs. Forward Voltage



■ Ambient Temperature vs. Relative Luminosity



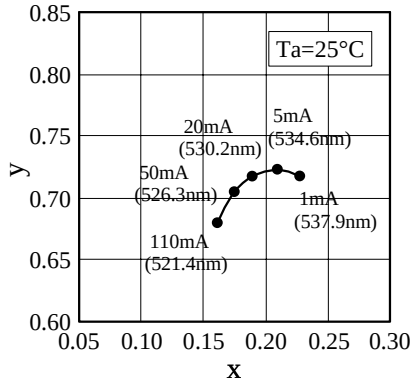
■ Ambient Temperature vs. Allowable Forward Current



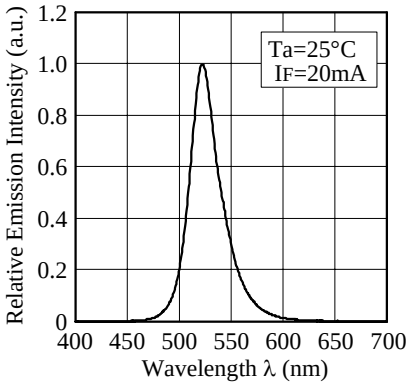
NICHIA CORPORATION	Model	NSPGxxxx
	Title	CHARACTERISTICS
	No.	070524761922

Nichia STS-DA1-0254
<Cat.No.080606>

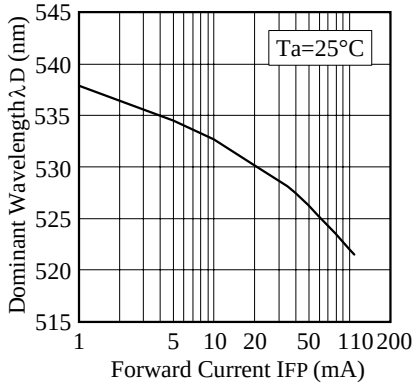
■ Forward Current vs. Chromaticity Coordinate (λ_D)



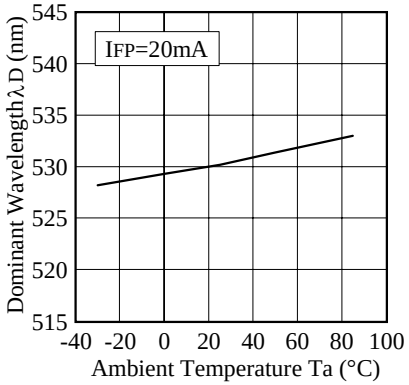
■ Spectrum



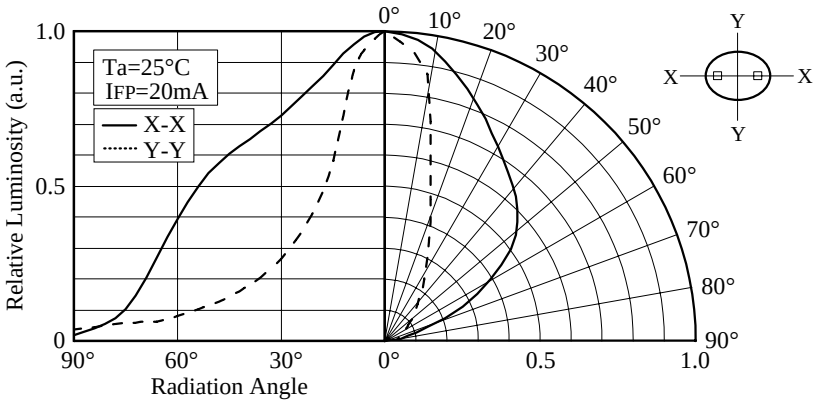
■ Forward Current vs. Dominant Wavelength



■ Ambient Temperature vs. Dominant Wavelength

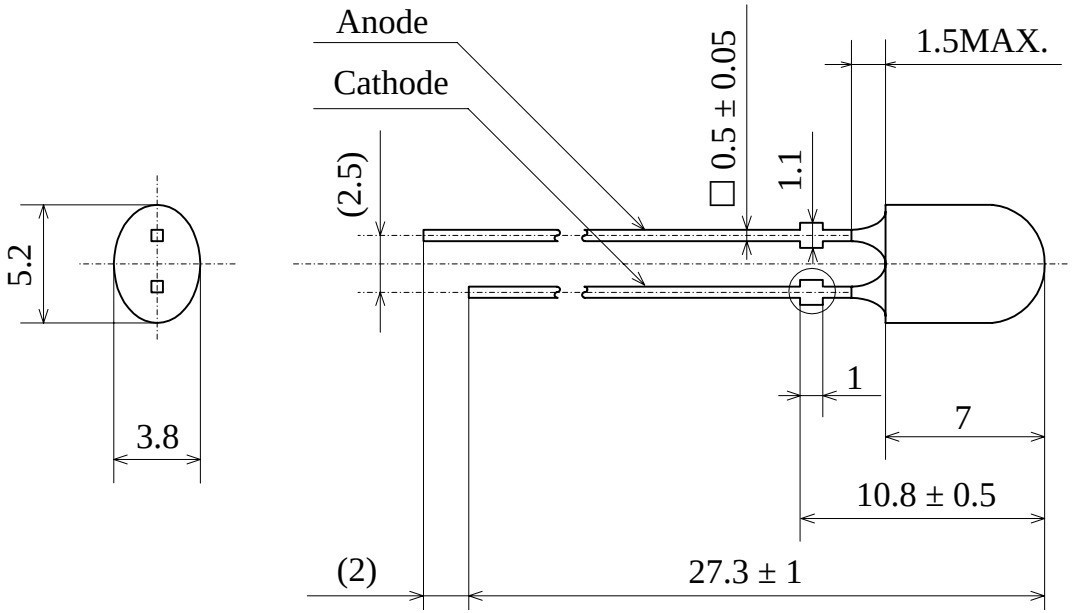


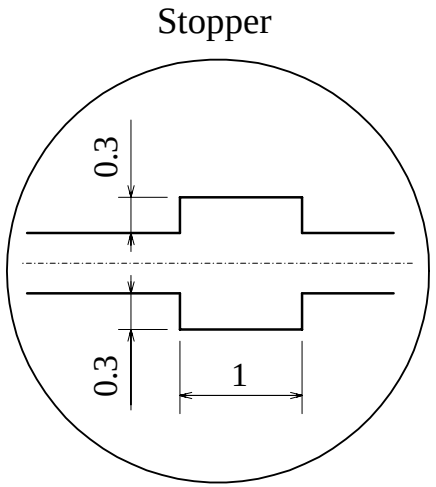
■ Directivity



NICHIA CORPORATION	Model	NSPG546GS
	Title	CHARACTERISTICS
	No.	070625767551

Nichia STS-DA1-0254
<Cat.No.080606>



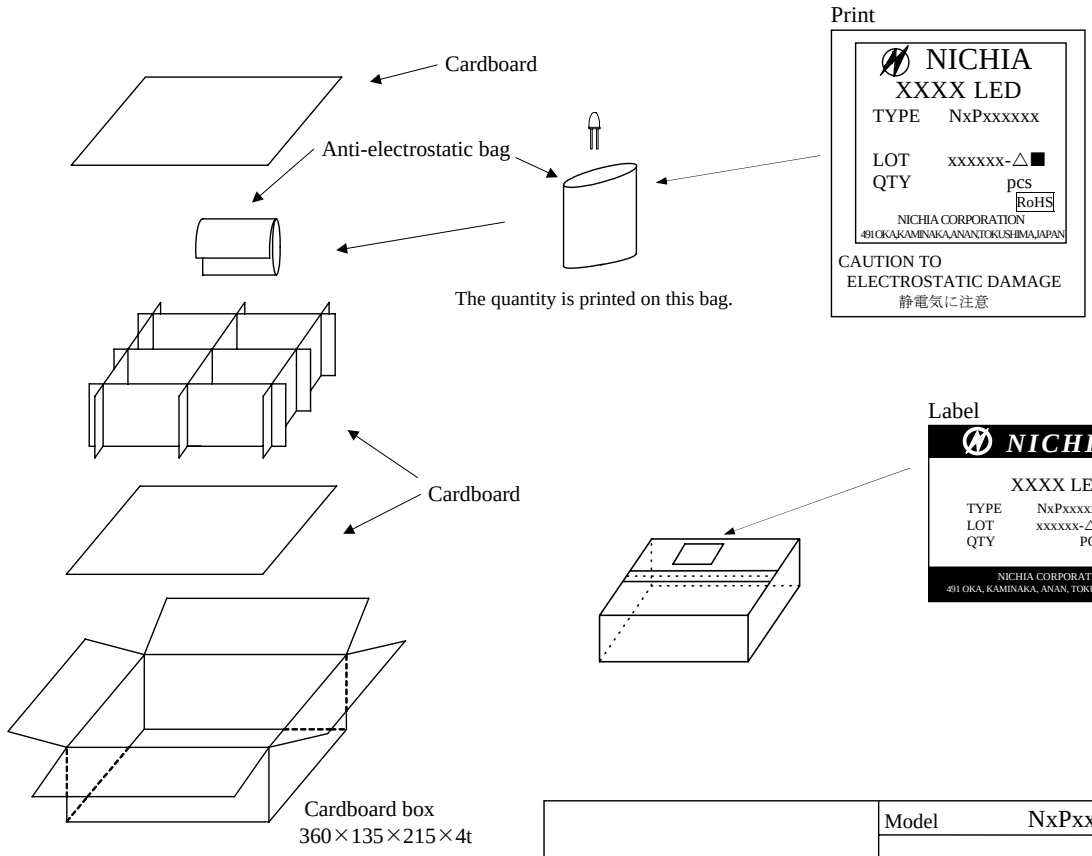


ITEM	MATERIALS
RESIN	Epoxy Resin
LENS COLOR	Green (Diffusion type)
LEAD FRAME	Ag Plating Copper Alloy

Remark:

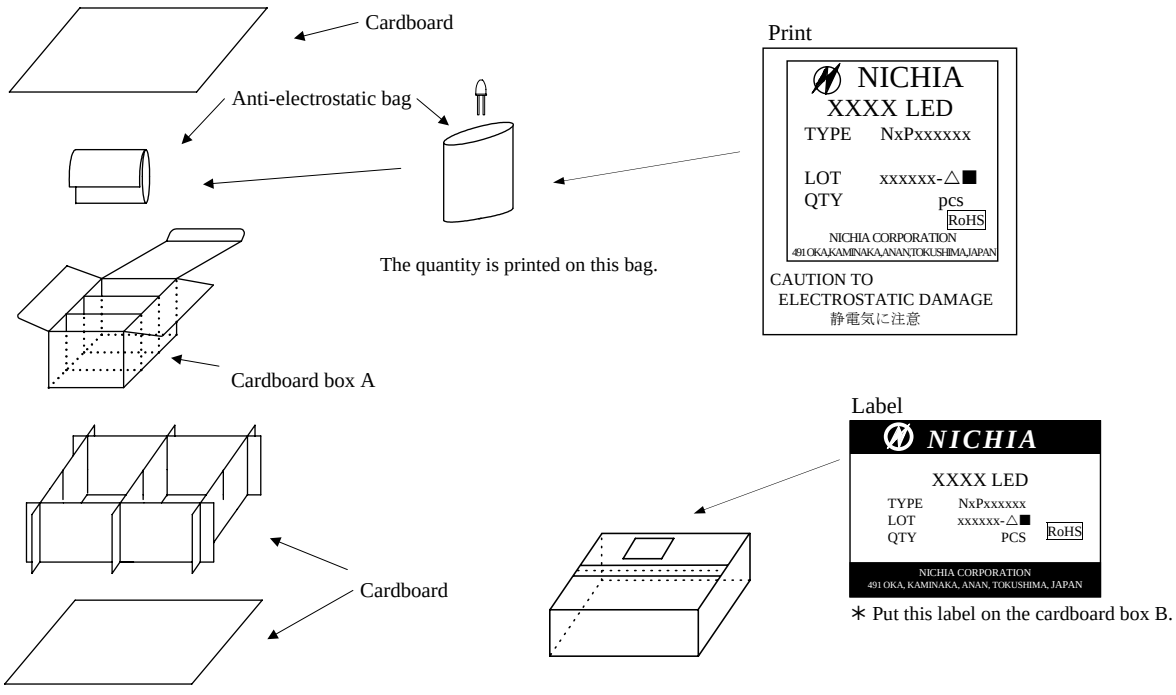
Please note that the bare copper alloy showing at the cut end of the lead frame may be corroded under certain conditions. LEDs have some sharp edges and points, particularly lead frames. Please handle with care so as to avoid injuries.

NICHIA CORPORATION	Model NSPG546GS	Unit mm
	Title OUTLINE DIMENSIONS	3/1 Scale
	No. 080521817101	Allow ±0.2



∗ One box contains 8 bags at maximum.

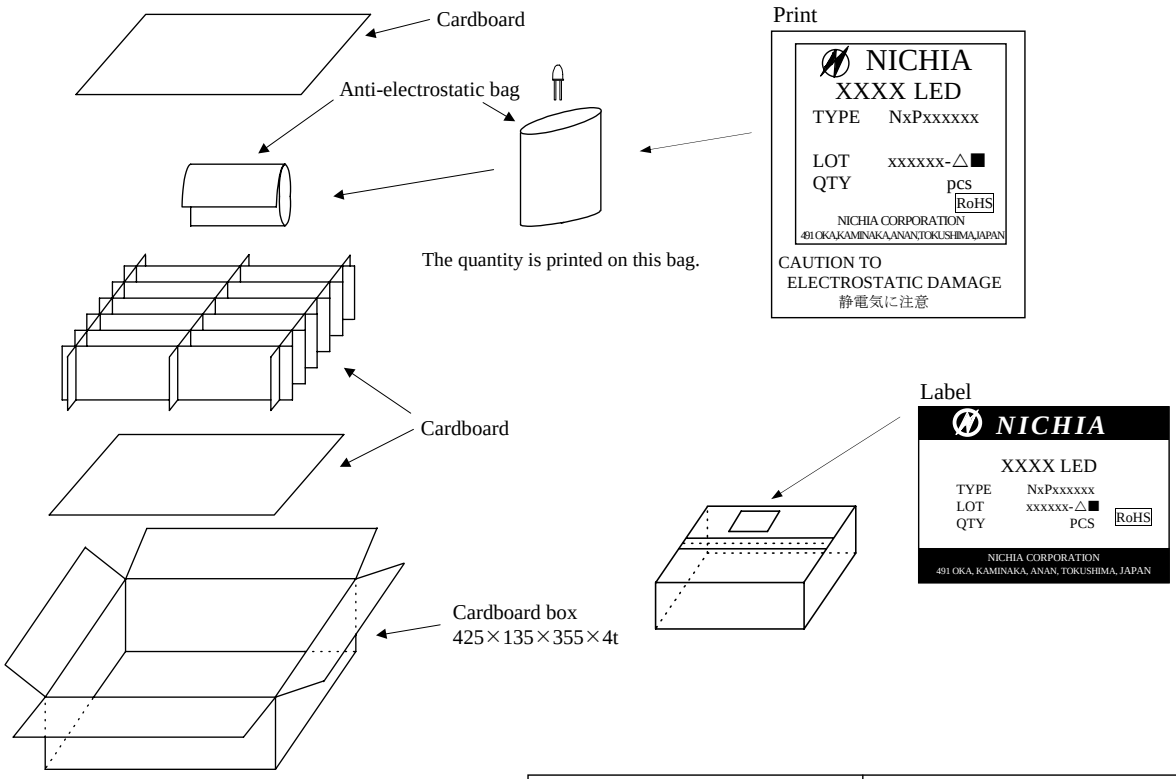
NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659112



∗ Put this label on the cardboard box B.

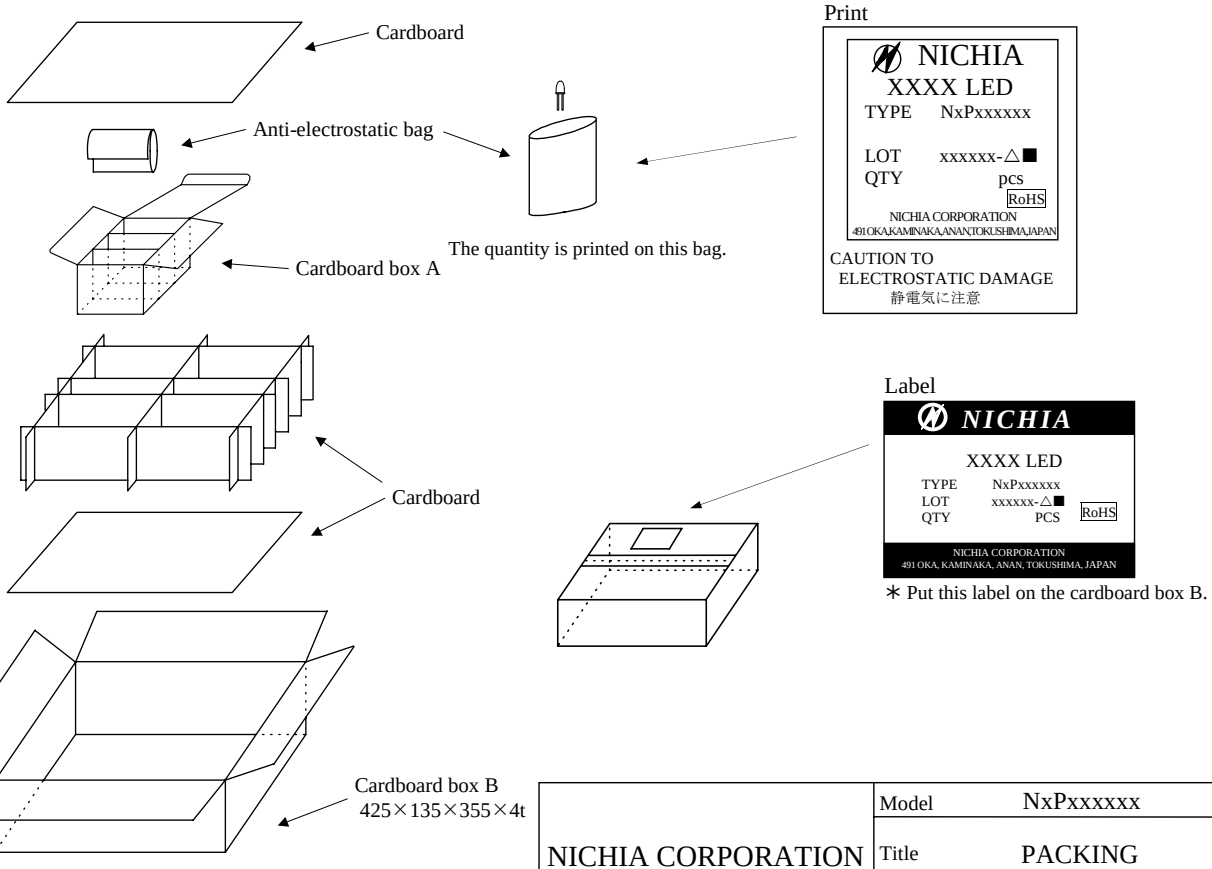
∗ The cardboard box B contains 2 cardboard box A at maximum.

NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659122



∗ One box contains 20 bags at maximum.

NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659132



∗ Put this label on the cardboard box B.

∗ The cardboard box B contains 4 cardboard box A at maximum.

NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659142

SPECIFICATIONS FOR NICHIA **RED** LED

MODEL : **NSPR546HS**

NICHIA CORPORATION

1.SPECIFICATIONS

(1) Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Absolute Maximum Rating	Unit
Forward Current	I_F	50	mA
Pulse Forward Current	I_{FP}	200	mA
Reverse Voltage	V_R	5	V
Power Dissipation	P_D	125	mW
Operating Temperature	T_{opr}	-30 ~ + 85	°C
Storage Temperature	T_{stg}	-40 ~ +100	°C
Soldering Temperature	T_{sld}	265°C for 10sec.	

I_{FP} Conditions : Pulse Width ≤ 10msec. and Duty ≤ 1/10

(2) Initial Electrical/Optical Characteristics (Ta=25°C)

Item		Symbol	Condition	Typ.	Max.	Unit
Forward Voltage		V_F	I_F=20[mA]	(2.1)	2.5	V
Reverse Current		I_R	V_R= 5[V]	-	50	μA
Luminous Intensity		Iv	I_F=20[mA]	(1180)(new)*1	-	mcd
Luminous Intensity		Iv	I_F=20[mA]	(1200)(old)*2	-	mcd
Chromaticity Coordinate*	x	-	I_F=20[mA]	0.700	-	-
	y	-	I_F=20[mA]	0.299	-	-

＊ Please refer to CIE 1931 chromaticity diagram.

＊1 Changed previously listed luminous intensity values (see ＊2) to luminous intensity values traceable to the current national standards on and after August 1, 2008.
(In accordance with CIE 127:2007)

(3) Ranking (Ta=25°C)

Item		Symbol	Condition	Min.	Max.	Unit
Luminous Intensity (new)*1	Rank V	Iv	I_F=20[mA]	1410	2000	mcd
	Rank U	Iv	I_F=20[mA]	1000	1410	mcd
	Rank T	Iv	I_F=20[mA]	710	1000	mcd

(Ta=25°C)

Item		Symbol	Condition	Min.	Max.	Unit
Luminous Intensity (old)*2	Rank V	Iv	I_F=20[mA]	1440	2040	mcd
	Rank U	Iv	I_F=20[mA]	1020	1440	mcd
	Rank T	Iv	I_F=20[mA]	720	1020	mcd

＊ Luminous Intensity Measurement allowance is ± 10%.

Color Rank (IF=20mA,Ta=25°C)

	Rank R			
x	0.67	0.67	0.73	0.73
y	0.27	0.33	0.33	0.27

∗ Color Coordinates Measurement allowance is ± 0.01.

∗ Basically, a shipment shall consist of the LEDs of a combination of the above ranks.
The percentage of each rank in the shipment shall be determined by Nichia.

2.INITIAL OPTICAL/ELECTRICAL CHARACTERISTICS

Please refer to "CHARACTERISTICS" on the following pages.

3.OUTLINE DIMENSIONS AND MATERIALS

Please refer to "OUTLINE DIMENSIONS" on the following page.

Material as follows ;

Resin	:	Epoxy Resin
Lens Color	:	Red (Diffusion type)
Leadframe	:	Ag plating Copper Alloy

4.PACKAGING

· The LEDs are packed in cardboard boxes after packaging in anti-electrostatic bags.
Please refer to "PACKING" on the following pages.
The label on the minimum packing unit shows ; Part Number, Lot Number, Ranking, Quantity
· In order to protect the LEDs from mechanical shock, we pack them in cardboard boxes for transportation.
· The LEDs may be damaged if the boxes are dropped or receive a strong impact against them, so precautions must be taken to prevent any damage.
· The boxes are not water resistant and therefore must be kept away from water and moisture.
· When the LEDs are transported, we recommend that you use the same packing method as Nichia.

5.LOT NUMBER

The first six digits number shows **lot number**.
The lot number is composed of the following characters;

○□××××-△■

○ - Year (7 for 2007, 8 for 2008)
□ - Month (1 for Jan., 9 for Sep., A for Oct., B for Nov.)
×××× - Nichia's Product Number
△ - Ranking by Color Coordinates
■ - Ranking by Luminous Intensity

6.RELIABILITY

(1) TEST ITEMS AND RESULTS

Test Item	Standard Test Method	Test Conditions	Note	Number of Damaged
Resistance to Soldering Heat	JEITA ED-4701 300 302	Tsld=260 ± 5°C, 10sec. 3mm from the base of the epoxy bulb	1 time	0/50
Solderability	JEITA ED-4701 300 303	Tsld=235 ± 5°C, 5sec. (using flux)	1 time over 95%	0/50
Thermal Shock	JEITA ED-4701 300 307	0°C ~ 100°C 15sec. 15sec.	100 cycles	0/50
Temperature Cycle	JEITA ED-4701 100 105	-40°C ~ 25°C ~ 100°C ~ 25°C 30min. 5min. 30min. 5min.	100 cycles	0/50
Moisture Resistance Cyclic	JEITA ED-4701 200 203	25°C ~ 65°C ~ -10°C 90%RH 24hrs./1cycle	10 cycles	0/50
Terminal Strength (bending test)	JEITA ED-4701 400 401	Load 5N (0.5kgf) 0° ~ 90° ~ 0° bend 2 times	No noticeable damage	0/50
Terminal Strength (pull test)	JEITA ED-4701 400 401	Load 10N (1kgf) 10 ± 1 sec.	No noticeable damage	0/50
High Temperature Storage	JEITA ED-4701 200 201	Ta=100°C	1000hrs.	0/50
Temperature Humidity Storage	JEITA ED-4701 100 103	Ta=60°C, RH=90%	1000hrs.	0/50
Low Temperature Storage	JEITA ED-4701 200 202	Ta=-40°C	1000hrs.	0/50
Steady State Operating Life		Ta=25°C, I_F=50mA	1000hrs.	0/50
Steady State Operating Life of High Humidity Heat		60°C, RH=90%, I_F=20mA	500hrs.	0/50
Steady State Operating Life of Low Temperature		Ta=-30°C, I_F=20mA	1000hrs.	0/50

(2) CRITERIA FOR JUDGING DAMAGE

Item	Symbol	Test Conditions	Criteria for Judgement	
			Min.	Max.
Forward Voltage	V_F	I_F=20mA	-	U.S.L.*)× 1.1
Reverse Current	I_R	V_R=5V	-	U.S.L.*)× 2.0
Luminous Intensity	I_V	I_F=20mA	L.S.L.**)× 0.7	-

*) U.S.L. : Upper Standard Level **) L.S.L. : Lower Standard Level

7.CAUTIONS

(1) Lead Forming

· When forming leads, the leads should be bent at a point at least 3mm from the base of the epoxy bulb. Do not use the base of the leadframe as a fulcrum during lead forming.
· Lead forming should be done before soldering.
· Do not apply any bending stress to the base of the lead. The stress to the base may damage the LED's characteristics or it may break the LEDs.
· When mounting the LEDs onto a printed circuit board, the holes on the circuit board should be exactly aligned with the leads of the LEDs. If the LEDs are mounted with stress at the leads, it causes deterioration of the epoxy resin and this will degrade the LEDs.

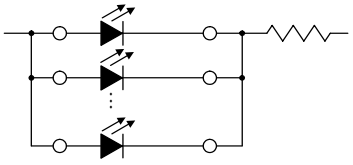
(2) Storage

· The LEDs should be stored at 30°C or less and 70%RH or less after being shipped from Nichia and the storage life limits are 3 months. If the LEDs are stored for 3 months or more, they can be stored for a year in a sealed container with a nitrogen atmosphere and moisture absorbent material.
· Nichia LED leadframes are silver plated copper alloy. The silver surface may be affected by environments which contain corrosive substances. Please avoid conditions which may cause the LED to corrode, tarnish or discolor. This corrosion or discoloration may cause difficulty during soldering operations. It is recommended that the LEDs be used as soon as possible.
· Please avoid rapid transitions in ambient temperature, especially, in high humidity environments where condensation can occur.

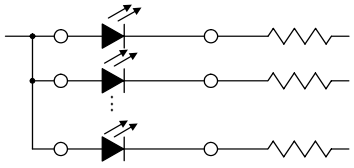
(3) Recommended circuit

· In designing a circuit, the current through each LED must not exceed the absolute maximum rating specified for each LED. It is recommended to use Circuit B which regulates the current flowing through each LED. In the meanwhile, when driving LEDs with a constant voltage in Circuit A, the current through the LEDs may vary due to the variation in forward voltage (V_F) of the LEDs. In the worst case, some LED may be subjected to stresses in excess of the absolute maximum rating.

(A)



(B)



· This product should be operated in forward bias. A driving circuit must be designed so that the product is not subjected to either forward or reverse voltage while it is off. In particular, if a reverse voltage is continuously applied to the product, such operation can cause migration resulting in LED damage.

(4) Soldering Conditions

· Nichia LED leadframes are silver plated copper alloy. This substance has a low thermal coefficient (easily conducts heat). Careful attention should be paid during soldering.

· Solder the LED no closer than 3mm from the base of the epoxy bulb. Soldering beyond the base of the tie bar is recommended.

· Recommended soldering conditions

Dip Soldering		Hand Soldering	
Pre-Heat	120°C Max.	Temperature	350°C Max.
Pre-Heat Time	60 seconds Max.	Soldering Time	3 seconds Max.
Solder Bath Temperature	260°C Max.	Position	No closer than 3 mm from the base of the epoxy bulb.
Dipping Time	10 seconds Max.		
Dipping Position	No lower than 3 mm from the base of the epoxy bulb.		

· Although the recommended soldering conditions are specified in the above table, dip or hand soldering at the lowest possible temperature is desirable for the LEDs.

· A rapid-rate process is not recommended for cooling the LEDs down from the peak temperature.

· Dip soldering should not be done more than one time.

· Hand soldering should not be done more than one time.

· Do not apply any stress to the lead particularly when heated.

· The LEDs must not be repositioned after soldering.

· After soldering the LEDs, the epoxy bulb should be protected from mechanical shock or vibration until the LEDs return to room temperature.

· Direct soldering onto a PC board should be avoided. Mechanical stress to the resin may be caused from warping of the PC board or from the clinching and cutting of the leadframes. When it is absolutely necessary, the LEDs may be mounted in this fashion but the User will assume responsibility for any problems. Direct soldering should only be done after testing has confirmed that no damage, such as wire bond failure or resin deterioration, will occur. Nichia's LEDs should not be soldered directly to double sided PC boards because the heat will deteriorate the epoxy resin.

· When it is necessary to clamp the LEDs to prevent soldering failure, it is important to minimize the mechanical stress on the LEDs.

· Cut the LED leadframes at room temperature. Cutting the leadframes at high temperatures may cause failure of the LEDs.

(5) Heat Generation

· Thermal design of the end product is of paramount importance. Please consider the heat generation of the LED when making the system design. The coefficient of temperature increase per input electric power is affected by the thermal resistance of the circuit board and density of LED placement on the board, as well as other components. It is necessary to avoid intense heat generation and operate within the maximum ratings given in this specification.

· The operating current should be decided after considering the ambient maximum temperature of LEDs.

(6) Cleaning

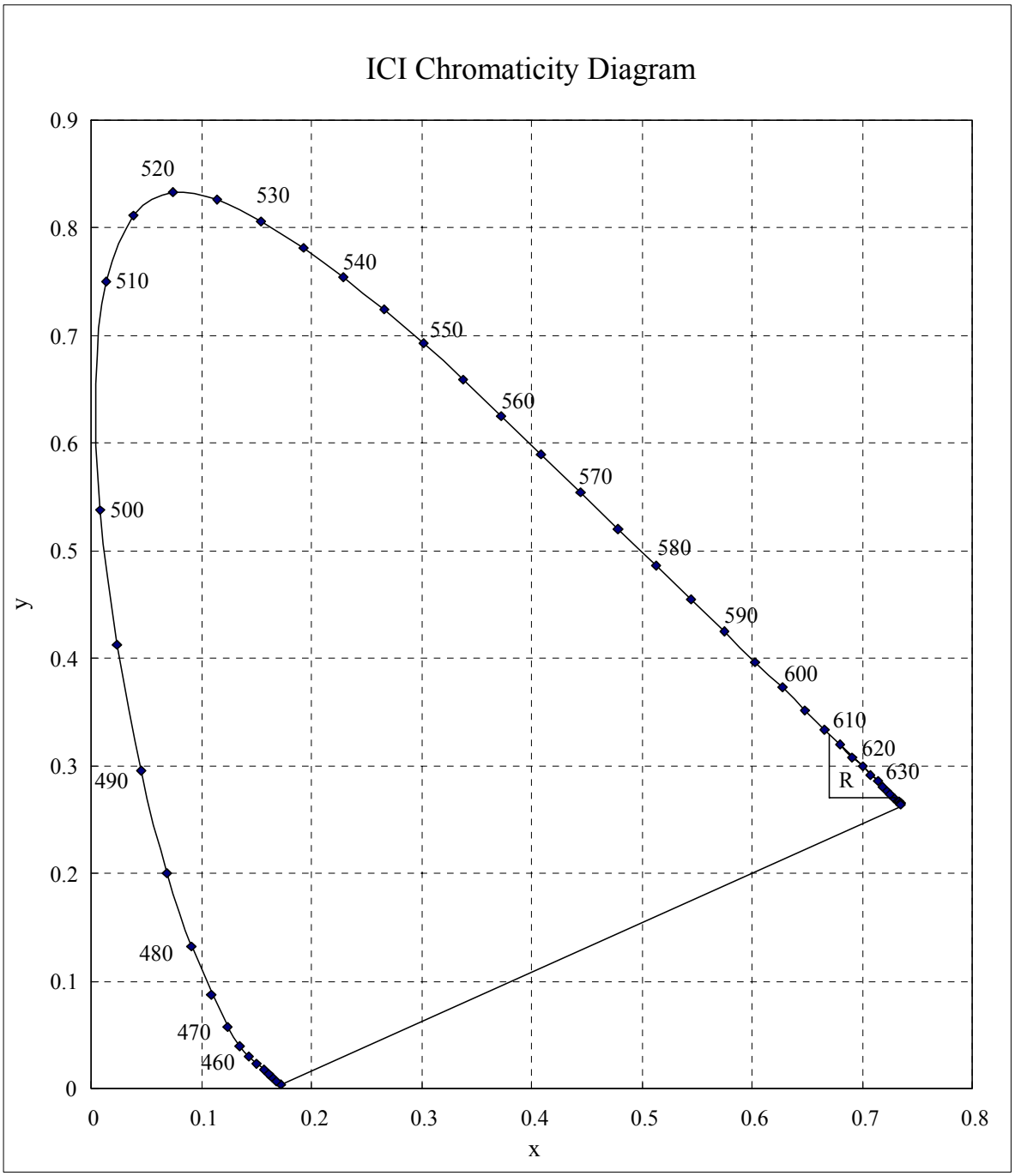
· It is recommended that isopropyl alcohol be used as a solvent for cleaning the LEDs. When using other solvents, it should be confirmed beforehand whether the solvents will dissolve the resin or not. Freon solvents should not be used to clean the LEDs because of worldwide regulations.
· Do not clean the LEDs by the ultrasonic. When it is absolutely necessary, the influence of ultrasonic cleaning on the LEDs depends on factors such as ultrasonic power and the assembled condition. Before cleaning, a pre-test should be done to confirm whether any damage to the LEDs will occur.

(7) Safety Guideline for Human Eyes

· The International Electrical Commission (IEC) published in 2006 IEC 62471:*2006 Photobiological safety of lamps and lamp systems* which includes LEDs within its scope. Meanwhile LEDs were removed from the scope of the IEC 60825-1:2007 laser safety standard, the 2001 edition of which included LED sources within its scope. However, keep in mind that some countries and regions have adopted standards based on the IEC laser safety standard IEC 60825-1:2001 which includes LEDs within its scope.
Following IEC 62471:2006, most of Nichia LEDs can be classified as belonging to either Exempt Group or Risk Group 1. Optical characteristics of a LED such as output power, spectrum and light distribution are factors that affect the risk group determination of the LED. Especially a high-power LED, that emits light containing blue wavelengths, may be in Risk Group 2.
Great care should be taken when viewing directly the LED driven at high current or the LED with optical instruments, which may greatly increase the hazard to your eyes.

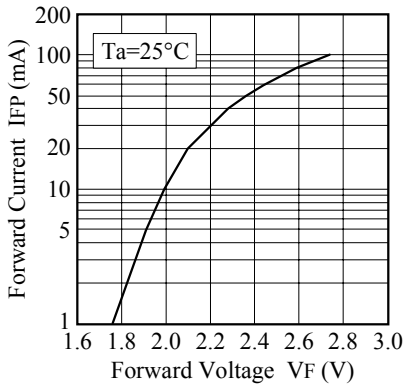
(8) Others

· NSPR546HS complies with RoHS Directive.
· Care must be taken to ensure that the reverse voltage will not exceed the absolute maximum rating when using the LEDs with matrix drive.
· Flashing lights have been known to cause discomfort in people; you can prevent this by taking precautions during use. Also, people should be cautious when using equipment that has had LEDs incorporated into it.
· The LEDs described in this brochure are intended to be used for ordinary electronic equipment (such as office equipment, communications equipment, measurement instruments and household appliances). Consult Nichia's sales staff in advance for information on the applications in which exceptional quality and reliability are required, particularly when the failure or malfunction of the LEDs may directly jeopardize life or health (such as for airplanes, aerospace, submersible repeaters, nuclear reactor control systems, automobiles, traffic control equipment, life support systems and safety devices).
· User shall not reverse engineer by disassembling or analysis of the LEDs without having prior written consent from Nichia. When defective LEDs are found, the User shall inform Nichia directly before disassembling or analysis.
· The formal specifications must be exchanged and signed by both parties before large volume purchase begins.
· The appearance and specifications of the product may be modified for improvement without notice.

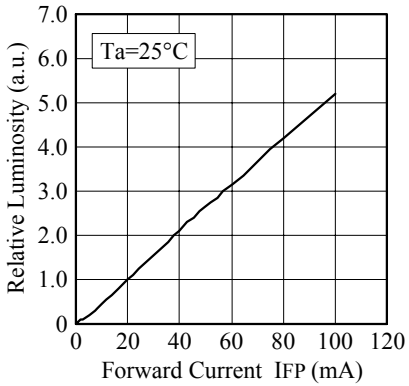


∗ Color Coordinates Measurement allowance is ± 0.01.

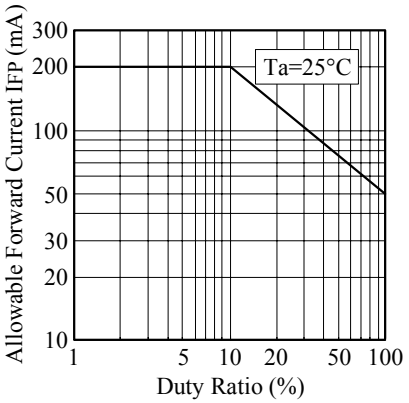
■ Forward Voltage vs. Forward Current



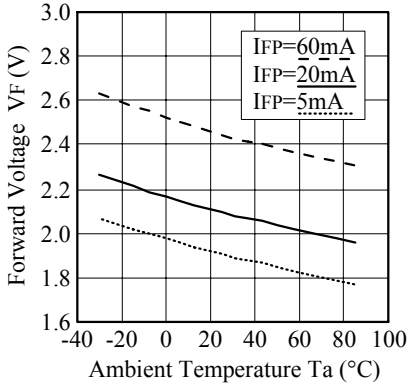
■ Forward Current vs. Relative Luminosity



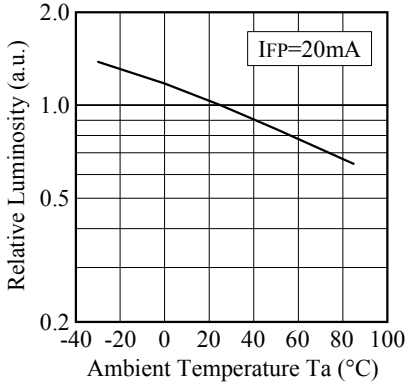
■ Duty Ratio vs. Allowable Forward Current



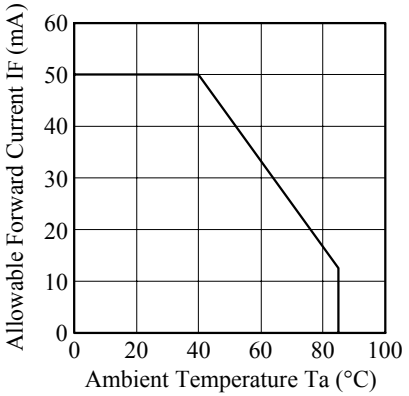
■ Ambient Temperature vs. Forward Voltage



■ Ambient Temperature vs. Relative Luminosity



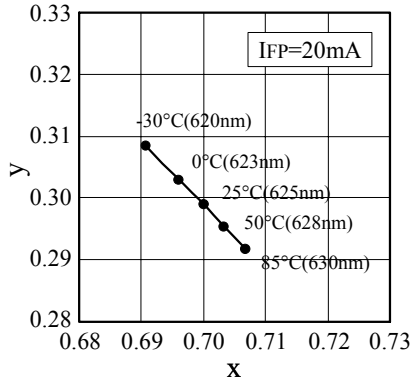
■ Ambient Temperature vs. Allowable Forward Current



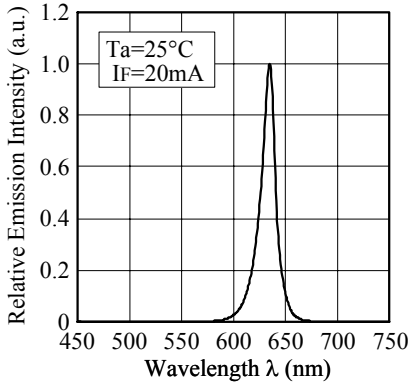
NICHIA CORPORATION	Model	NSPR546HS
	Title	CHARACTERISTICS
	No.	061122658331

Nichia STS-DA1-0218
<Cat.No.080512>

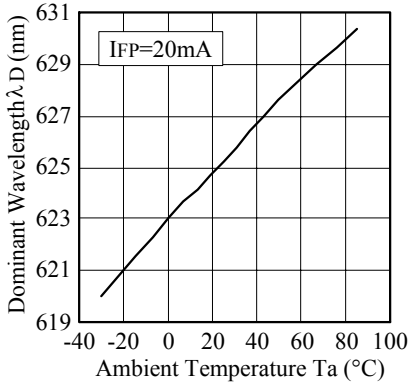
■ Ambient Temperature vs. Chromaticity Coordinate (λ_D)



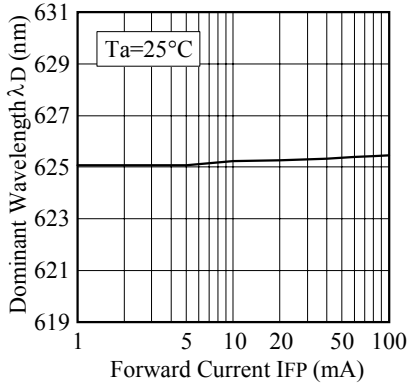
■ Spectrum



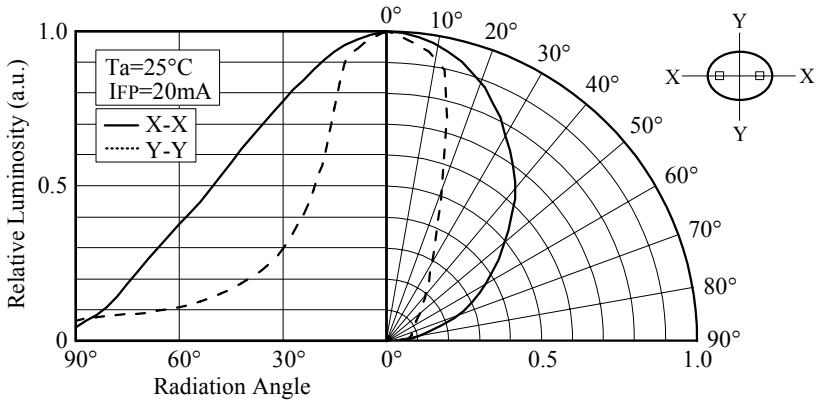
■ Ambient Temperature vs. Dominant Wavelength



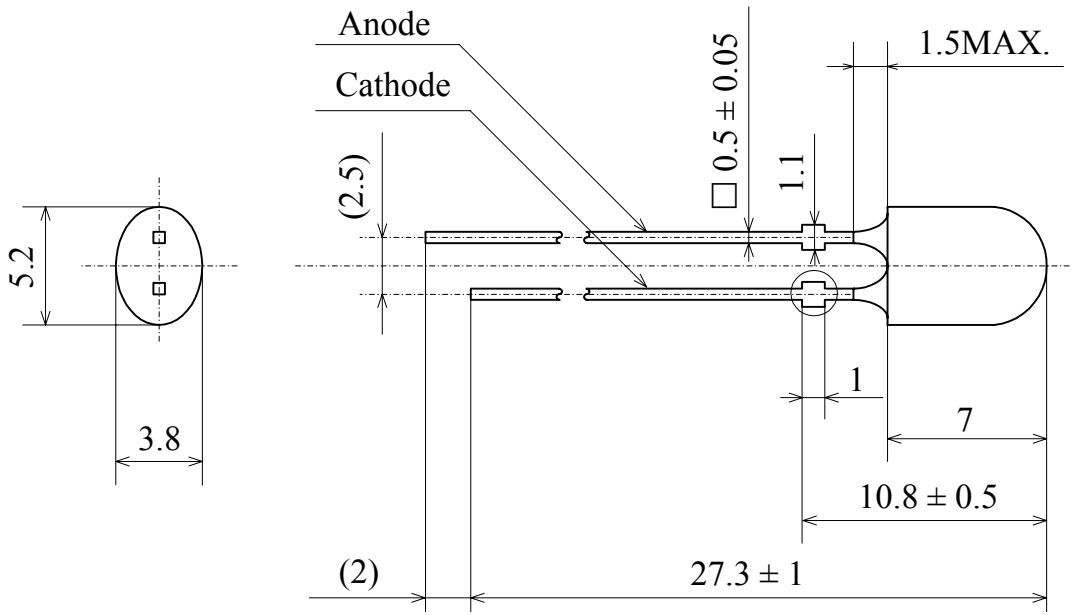
■ Forward Current vs. Dominant Wavelength

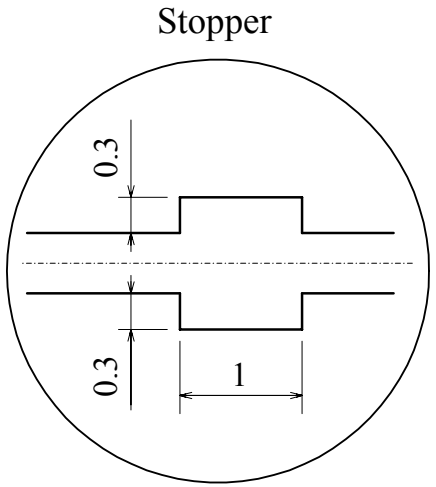


■ Directivity



NICHIA CORPORATION	Model	NSPR546HS
	Title	CHARACTERISTICS
	No.	061122658341



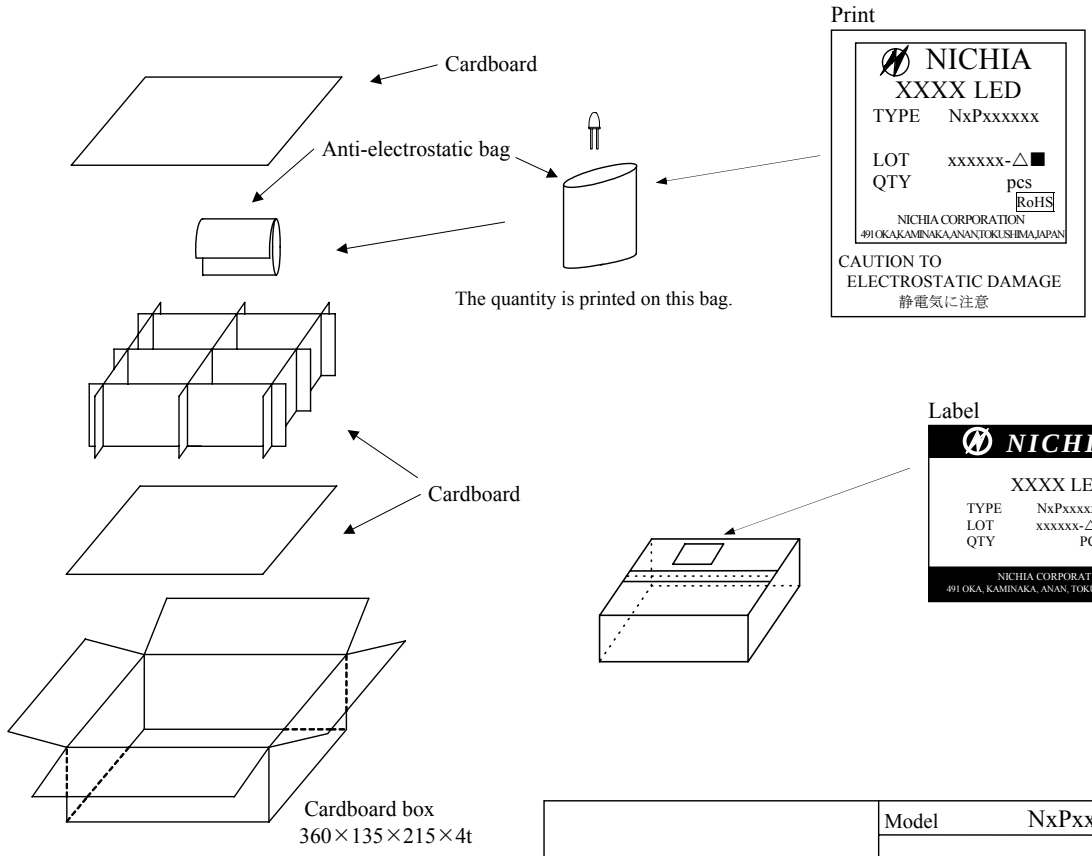


ITEM	MATERIALS
RESIN	Epoxy Resin
LENS COLOR	Red (Diffusion type)
LEAD FRAME	Ag Plating Copper Alloy

Remark:

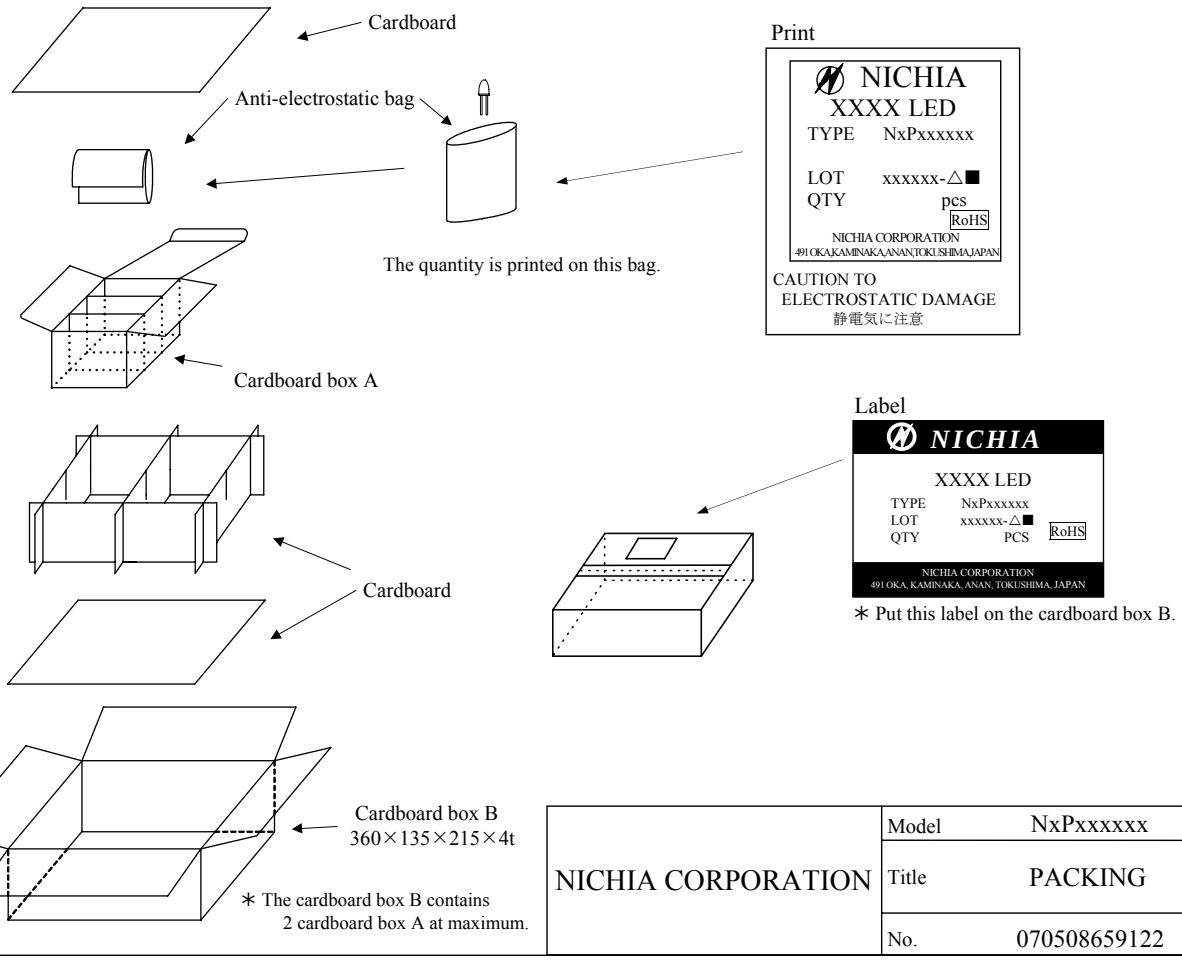
Please note that the bare copper alloy showing at the cut end of the lead frame may be corroded under certain conditions. LEDs have some sharp edges and points, particularly lead frames. Please handle with care so as to avoid injuries.

NICHIA CORPORATION	Model	NSPR546HS	Unit mm
	Title	OUTLINE DIMENSIONS	3/1 Scale
	No.	080508815971	Allow ±0.2



∗ One box contains 8 bags at maximum.

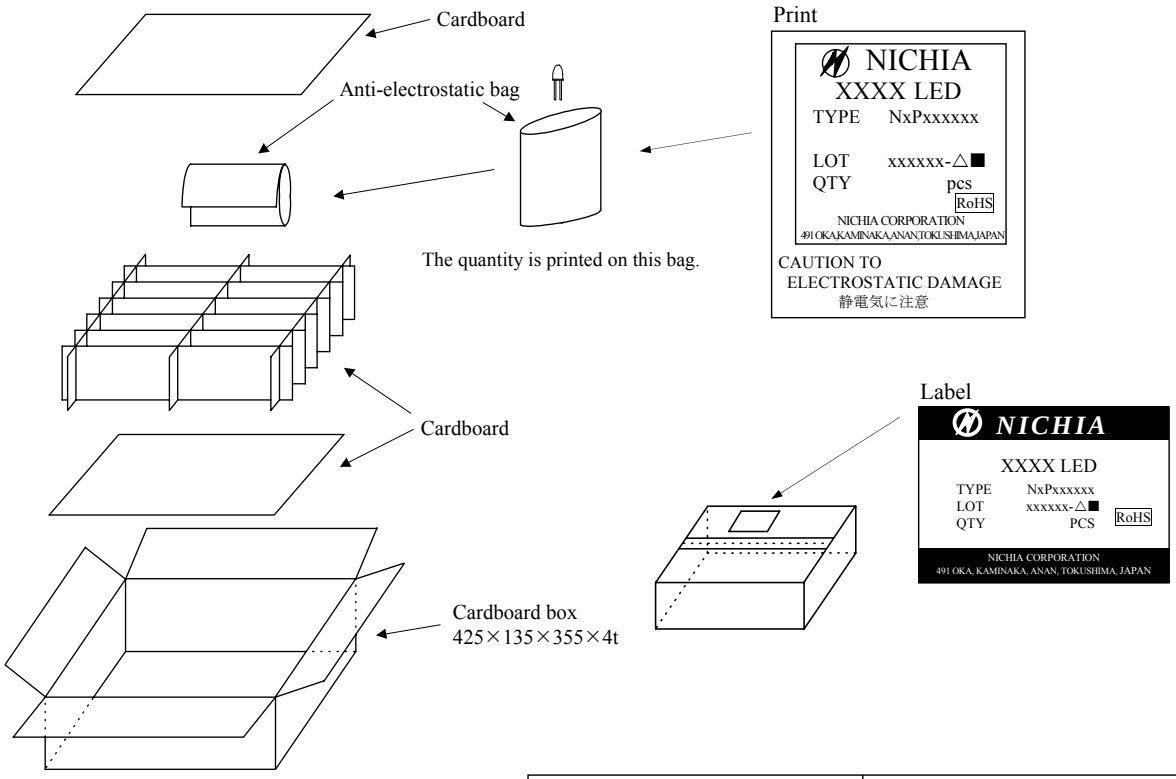
NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659112



∗ Put this label on the cardboard box B.

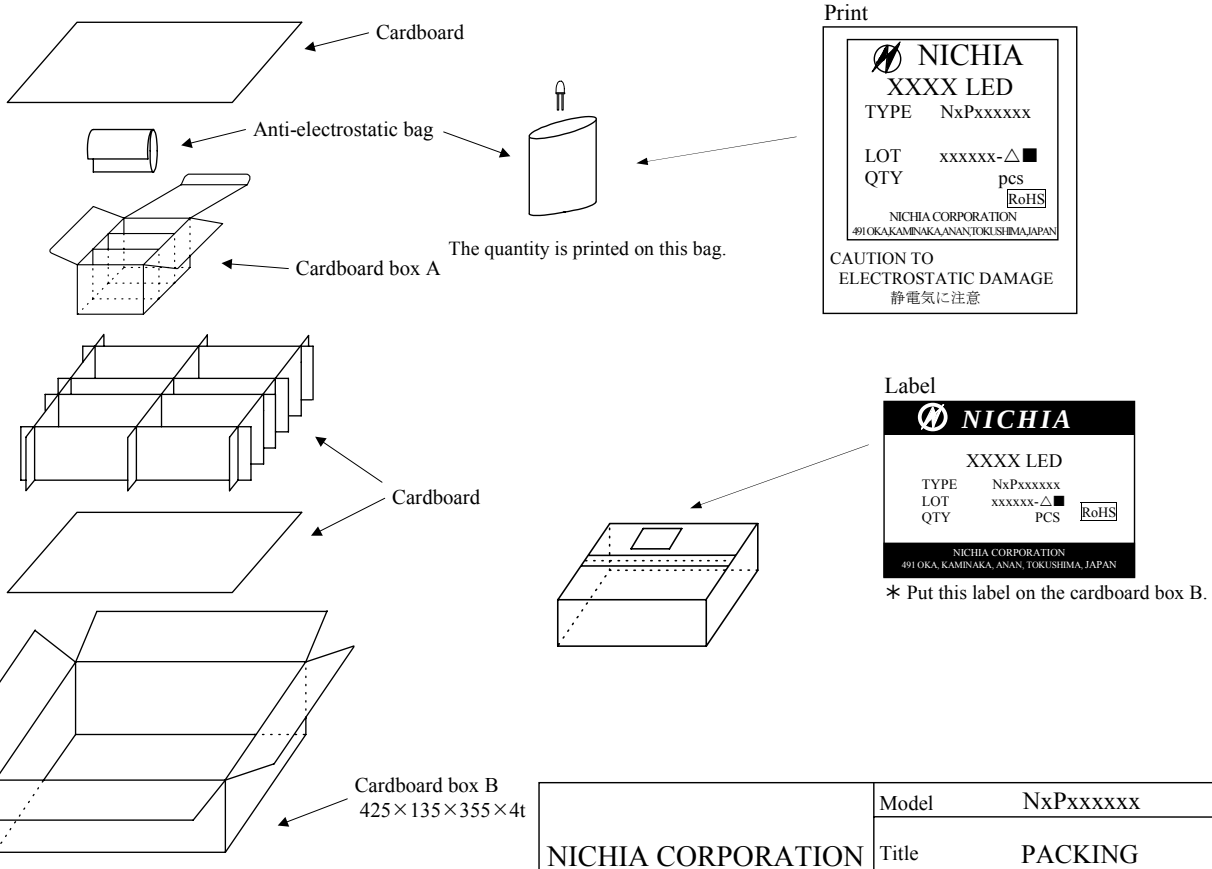
∗ The cardboard box B contains
2 cardboard box A at maximum.

NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659122



∗ One box contains 20 bags at maximum.

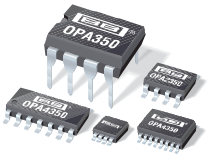
NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659132



∗ Put this label on the cardboard box B.

∗ The cardboard box B contains 4 cardboard box A at maximum.

NICHIA CORPORATION	Model	NxPxxxxxx
	Title	PACKING
	No.	070508659142



SBOS099C − SEPTEMBER 2000 − REVISED JANUARY 2005

High-Speed, Single-Supply, Rail-to-Rail OPERATIONAL AMPLIFIERS

*Micro*Amplifier™ Series

FEATURES

- RAIL-TO-RAIL INPUT
- RAIL-TO-RAIL OUTPUT (within 10mV)
- WIDE BANDWIDTH: 38MHz
- HIGH SLEW RATE: 22V/μs
- LOW NOISE: 5nV/√Hz
- LOW THD+NOISE: 0.0006%
- UNITY-GAIN STABLE
- *Micro*SIZE PACKAGES
- SINGLE, DUAL, AND QUAD

APPLICATIONS

- CELL PHONE PA CONTROL LOOPS
- DRIVING A/D CONVERTERS
- VIDEO PROCESSING
- DATA ACQUISITION
- PROCESS CONTROL
- AUDIO PROCESSING
- COMMUNICATIONS
- ACTIVE FILTERS
- TEST EQUIPMENT

DESCRIPTION

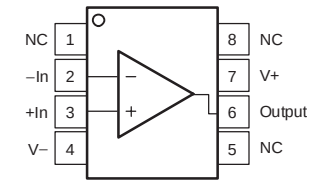
The OPA350 series rail-to-rail CMOS operational amplifiers are optimized for low voltage, single-supply operation. Rail-to-rail input/output, low noise (5nV/√Hz), and high speed operation (38MHz, 22V/μs) make them ideal for driving sampling Analog-to-Digital (A/D) converters. They are also well suited for cell phone PA control loops and video processing (75Ω drive capability) as well as audio and general purpose applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

The OPA350 series operates on a single supply as low as 2.5V with an input common-mode voltage range that extends 300mV below ground and 300mV above the positive supply. Output voltage swing is to within 10mV of the supply rails with a 10kΩ load. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

The single (OPA350) and dual (OPA2350) come in the miniature MSOP-8 surface mount, SO-8 surface mount, and DIP-8 packages. The quad (OPA4350) packages are the space-saving SSOP-16 surface mount and SO-14 surface mount. All are specified from −40°C to +85°C and operate from −55°C to +150°C.

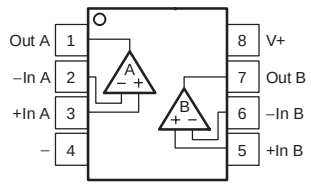
SPICE model available at www.ti.com

OPA350



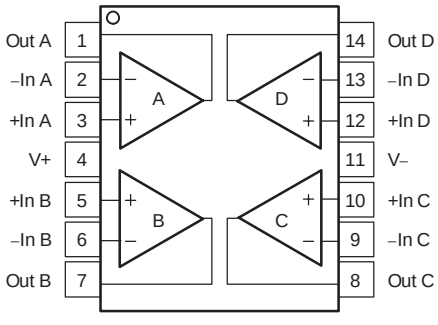
DIP−8, SO−8, MSOP−8

OPA2350



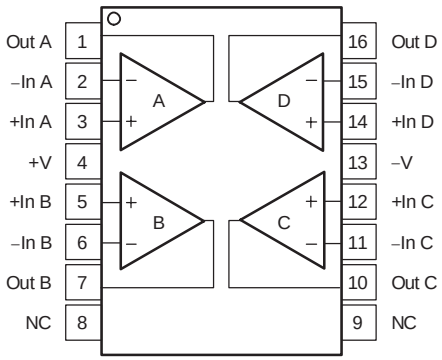
DIP−8, SO−8, MSOP−8

OPA4350



SO−14

OPA4350



SSOP−16

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	7.0V
Signal Input Terminals(2), Voltage	(V−) − 0.3V to (V+) + 0.3V
Current	10mA
Open Short-Circuit Current(3)	Continuous
Operating Temperature Range	−55°C to +150°C
Storage Temperature Range	−55°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
SINGLE						
OPA350EA	MSOP-8	DGK	−40°C to +85°C	C50	OPA350EA/250	Tape and Reel, 250
					OPA350EA/2K5	Tape and Reel, 2500
OPA350UA	SO-8	D	−40°C to +85°C	OPA350UA	OPA350UA	Rails
					OPA350UA/2K5	Tape and Reel, 2500
OPA350PA	DIP-8	P	−40°C to +85°C	OPA350PA	OPA350PA	Rails
DUAL						
OPA2350EA	MSOP-8	DGK	−40°C to +85°C	D50	OPA2350EA/250	Tape and Reel, 250
					OPA2350EA/2K5	Tape and Reel, 2500
OPA2350UA	SO-8	D	−40°C to +85°C	OPA2350UA	OPA2350UA	Rails
					OPA2350UA/2K5	Tape and Reel, 2500
OPA2350PA	DIP-8	P	−40°C to +85°C	OPA2350PA	OPA2350PA	Rails
QUAD						
OPA4350EA	SSOP-16	DBQ	−40°C to +85°C	OPA4350EA	OPA4350EA/250	Tape and Reel, 250
					OPA4350EA/2K5	Tape and Reel, 2500
OPA4350UA	SO-14	D	−40°C to +85°C	OPA4350UA	OPA4350UA	Rails
					OPA4350UA/2K5	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTRICAL CHARACTERISTICS: V_S = 2.7V to 5.5V

Boldface limits apply over the temperature range, **T_A = −40°C to +85°C**. V_S = 5V.

All specifications at T_A = +25°C, R_L = 1kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA350, OPA2350, OPA4350 MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 5V		±150	±500	µV
T_A = −40°C to +85°C					**±1**	mV
vs Temperature		**T_A = −40°C to +85°C**		**±4**		µV/°C
vs Power-Supply Rejection Ratio	PSRR	V_S = 2.7V to 5.5V, V_{CM} = 0V		40	150	µV/V
T_A = −40°C to +85°C		**V_S = 2.7V to 5.5V, V_{CM} = 0V**			**175**	µV/V
Channel Separation (dual, quad)		dc		0.15		µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.5	±10	pA
vs Temperature				See Typical Characteristics		
Input Offset Current	I_{OS}			±0.5	±10	pA
NOISE						
Input Voltage Noise, f = 100Hz to 400kHz				4		µVrms
Input Voltage Noise Density, f = 10kHz	e_n			7		nV/√Hz
Input Current Noise Density, f = 100kHz				5		nV/√Hz
Current Noise Density, f = 10kHz	i_n			4		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	**T_A = −40°C to +85°C**	**−0.1**		**(V+) + 0.1**	V
Common-Mode Rejection Ratio	CMRR	V_S = 2.7V, −0.1V < V_{CM} < 2.8V	66	84		dB
		V_S = 5.5V, −0.1V < V_{CM} < 5.6V	74	90		dB
T_A = −40°C to +85°C		**V_S = 5.5V, −0.1V < V_{CM} < 5.6V**	**74**			dB
INPUT IMPEDANCE						
Differential				10^{13} ‖ 2.5		Ω ‖ pF
Common-Mode				10^{13} ‖ 6.5		Ω ‖ pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 10kΩ, 50mV < V_O < (V+) −50mV	100	122		dB
T_A = −40°C to +85°C		**R_L = 10kΩ, 50mV < V_O < (V+) −50mV**	**100**			dB
		R_L = 1kΩ, 200mV < V_O < (V+) −200mV	100	120		dB
T_A = −40°C to +85°C		**R_L = 1kΩ, 200mV < V_O < (V+) −200mV**	**100**			dB
FREQUENCY RESPONSE		C_L = 100pF				
Gain-Bandwidth Product	GBW	G = 1		38		MHz
Slew Rate	SR	G = 1		22		V/µs
Settling Time: 0.1%		G = ±1, 2V Step		0.22		µs
0.01%		G = ±1, 2V Step		0.5		µs
Overload Recovery Time		V_{IN} • G = V_S		0.1		µs
Total Harmonic Distortion + Noise	THD+N	R_L = 600Ω, V_O = 2.5V_{PP}(2), G = 1, f = 1kHz		0.0006		%
Differential Gain Error		G = 2, R_L = 600Ω, V_O = 1.4V(3)		0.17		%
Differential Phase Error		G = 2, R_L = 600Ω, V_O = 1.4V(3)		0.17		deg

(1) V_S = +5V.
(2) V_{OUT} = 0.25V to 2.75V.
(3) NTSC signal generator used. See Figure 6 for test circuit.
(4) Output voltage swings are measured between the output and power supply rails.
(5) See typical characteristic curve, *Output Voltage Swing vs Output Current*.

ELECTRICAL CHARACTERISTICS: V_S = 2.7V to 5.5V (continued)

Boldface limits apply over the temperature range, **T_A = −40°C to +85°C**. V_S = 5V.

All specifications at T_A = +25°C, R_L = 1kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

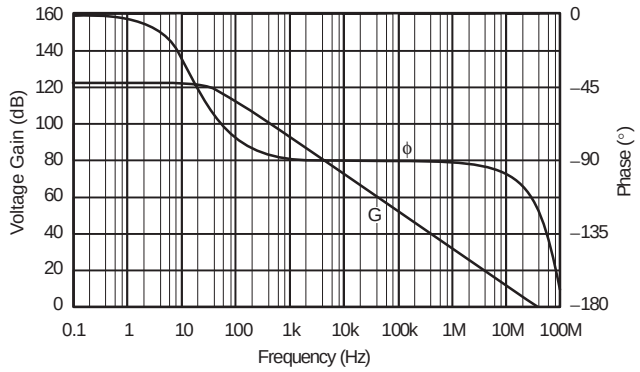
PARAMETER		TEST CONDITIONS	OPA350, OPA2350, OPA4350 MIN	TYP(1)	MAX	UNIT
OUTPUT						
Voltage Output Swing from Rail(4)	V_{OUT}	R_L = 10kΩ, A_{OL} ≥ 100dB		10	50	mV
T_A = −40°C to +85°C		**R_L = 10kΩ, A_{OL} ≥ 100dB**			**50**	mV
		R_L = 1kΩ, A_{OL} ≥ 100dB		25	200	mV
T_A = −40°C to +85°C		**R_L = 1kΩ, A_{OL} ≥ 100dB**			**200**	mV
Output Current	I_{OUT}			±40(5)		mA
Short-Circuit Current	I_{SC}			±80		mA
Capacitive Load Drive	C_{LOAD}			See Typical Characteristics		
POWER SUPPLY						
Operating Voltage Range	V_S	**T_A = −40°C to +85°C**	**2.7**		**5.5**	V
Minimum Operating Voltage				2.5		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		5.2	7.5	mA
T_A = −40°C to +85°C		I_O = 0			**8.5**	mA
TEMPERATURE RANGE						
Specified Range			−40		+85	°C
Operating Range			−55		+150	°C
Storage Range			−55		+150	°C
Thermal Resistance	θ_{JA}					
MSOP-8 Surface Mount				150		°C/W
SO-8 Surface Mount				150		°C/W
DIP-8				100		°C/W
SO-14 Surface Mount				100		°C/W
SSOP-16 Surface Mount				100		°C/W

(1) V_S = +5V.
(2) V_{OUT} = 0.25V to 2.75V.
(3) NTSC signal generator used. See Figure 6 for test circuit.
(4) Output voltage swings are measured between the output and power supply rails.
(5) See typical characteristic curve, *Output Voltage Swing vs Output Current*.

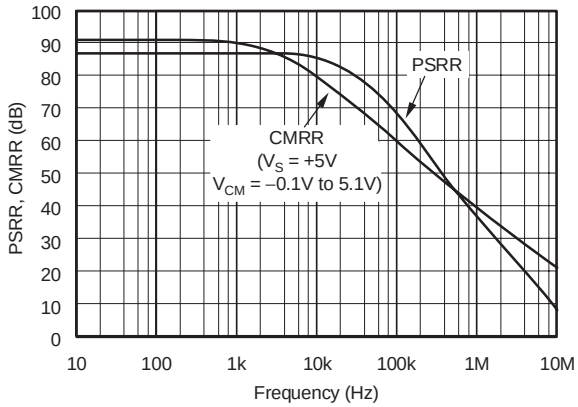
TYPICAL CHARACTERISTICS

All specifications at T_A = +25°C, V_S = +5V, and R_L = 1kΩ connected to V_S/2, unless otherwise noted.

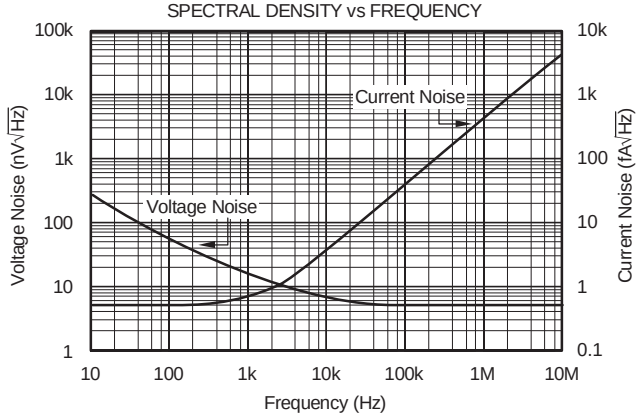
OPEN-LOOP GAIN/PHASE vs FREQUENCY



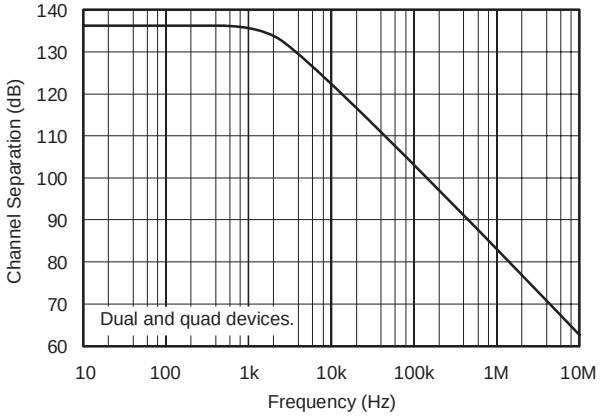
POWER SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY



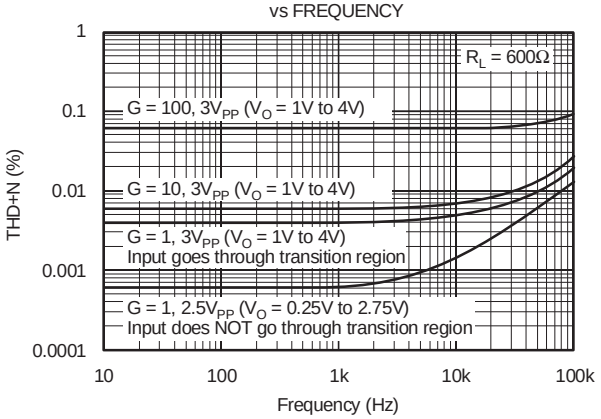
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



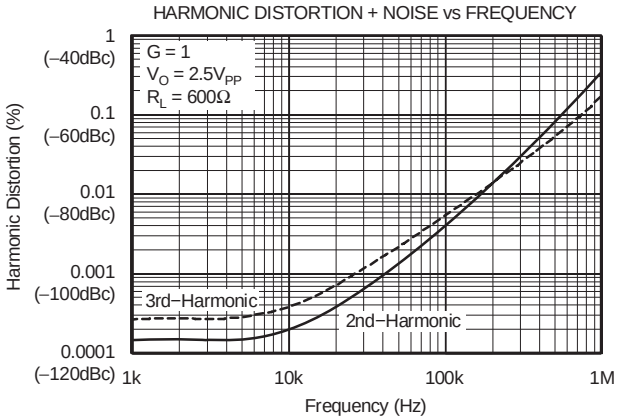
CHANNEL SEPARATION vs FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



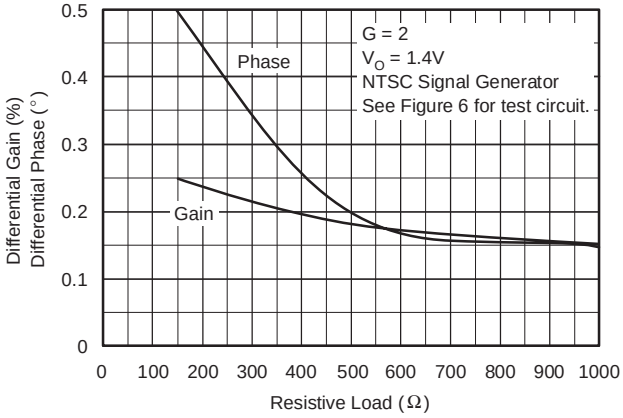
HARMONIC DISTORTION + NOISE vs FREQUENCY



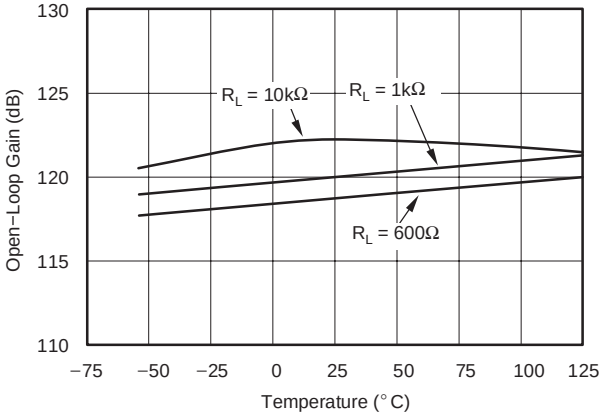
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_S = +5V, and R_L = 1kΩ connected to V_S/2, unless otherwise noted.

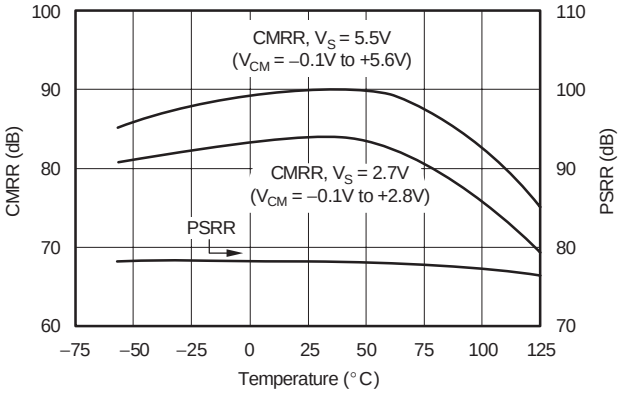
DIFFERENTIAL GAIN/PHASE vs RESISTIVE LOAD



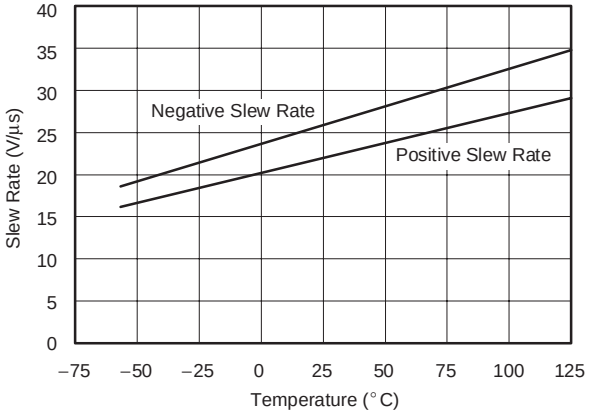
OPEN−LOOP GAIN vs TEMPERATURE



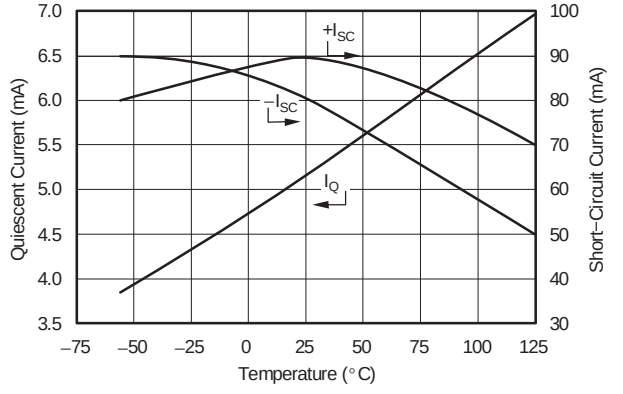
COMMON−MODE AND POWER−SUPPLY REJECTION RATIO vs TEMPERATURE



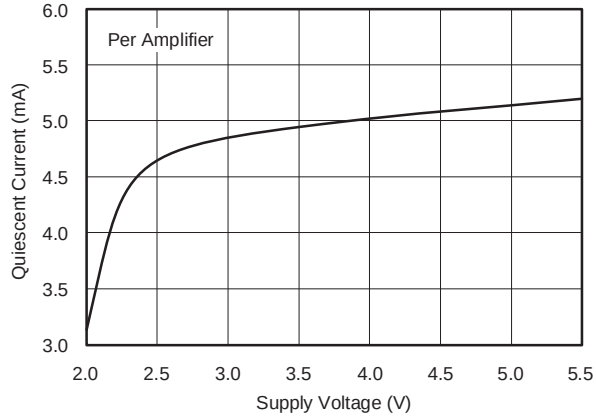
SLEW RATE vs TEMPERATURE



QUIESCENT CURRENT AND SHORT−CIRCUIT CURRENT vs TEMPERATURE



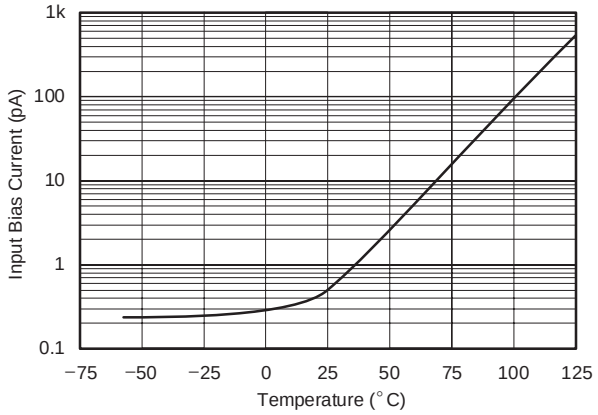
QUIESCENT CURRENT vs SUPPLY VOLTAGE



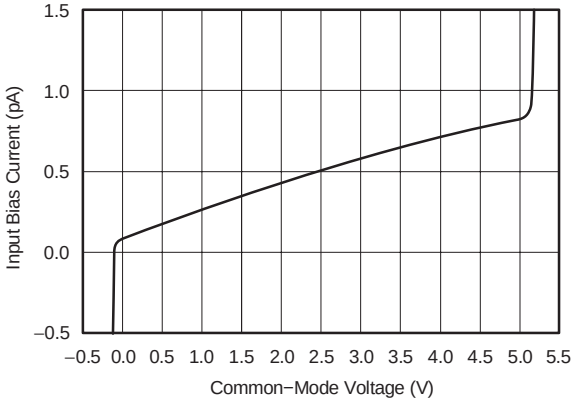
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_S = +5V, and R_L = 1kΩ connected to V_S/2, unless otherwise noted.

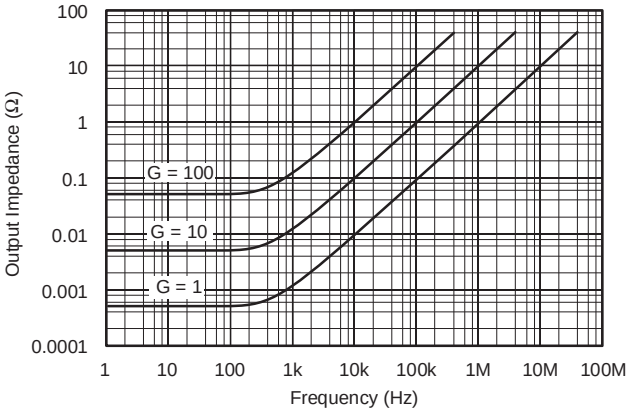
INPUT BIAS CURRENT vs TEMPERATURE



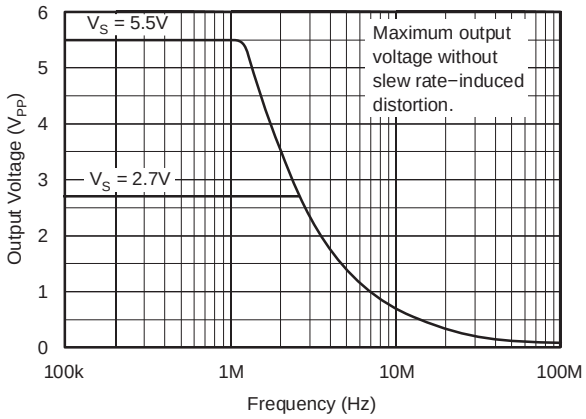
INPUT BIAS CURRENT
vs INPUT COMMON−MODE VOLTAGE



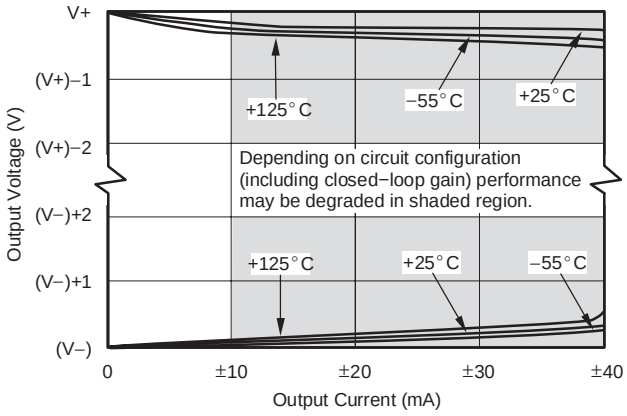
CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY



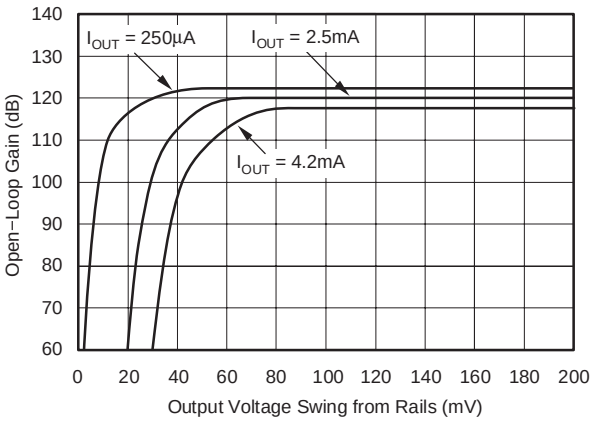
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



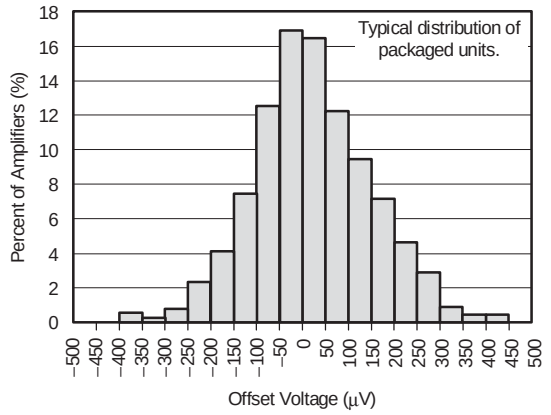
OPEN−LOOP GAIN vs OUTPUT VOLTAGE SWING



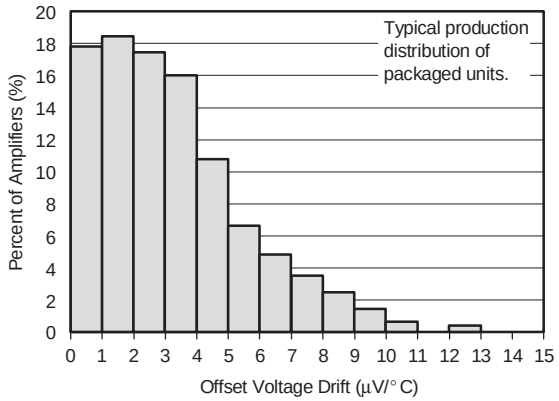
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_S = +5V, and R_L = 1kΩ connected to V_S/2, unless otherwise noted.

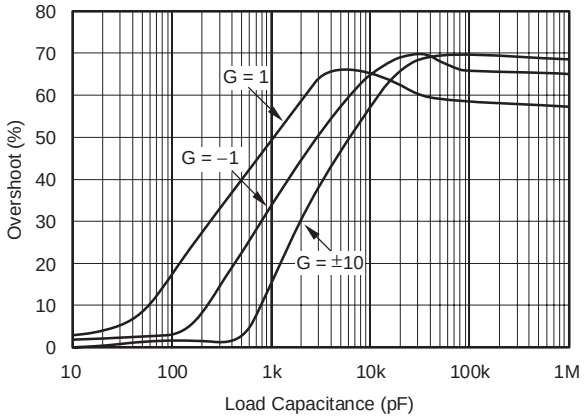
OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



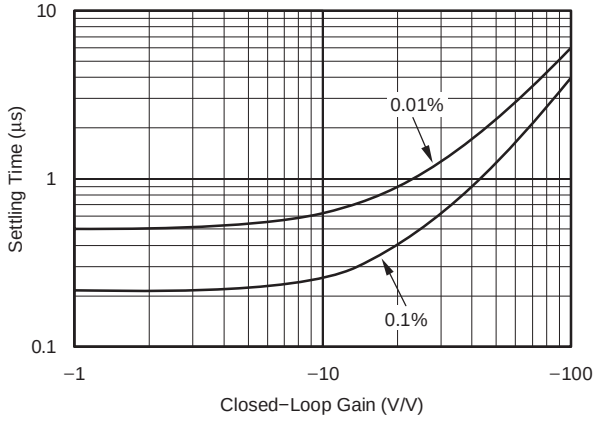
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



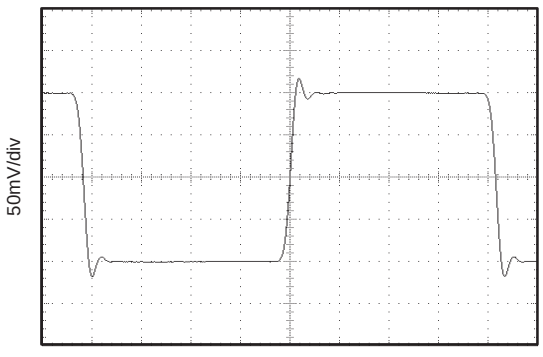
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



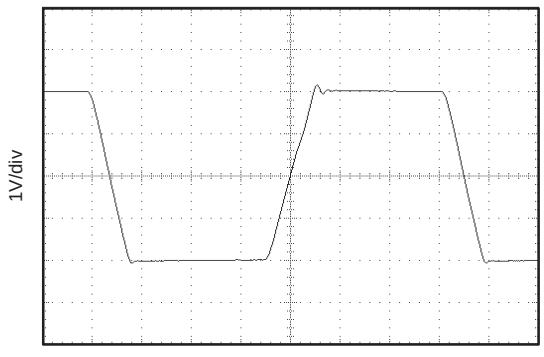
SETTLING TIME vs CLOSED−LOOP GAIN



SMALL−SIGNAL STEP RESPONSE
C_L = 100pF



LARGE−SIGNAL STEP RESPONSE
C_L = 100pF



APPLICATIONS INFORMATION

OPA350 series op amps are fabricated on a state-of-the-art 0.6 micron CMOS process. They are unity-gain stable and suitable for a wide range of general-purpose applications. Rail-to-rail input/output make them ideal for driving sampling A/D converters. They are also well-suited for controlling the output power in cell phones. These applications often require high speed and low noise. In addition, the OPA350 series offers a low-cost solution for general-purpose and consumer video applications (75Ω drive capability).

Excellent ac performance makes the OPA350 series well-suited for audio applications. Their bandwidth, slew rate, low noise (5nV/√Hz), low THD (0.0006%), and small package options are ideal for these applications. The class AB output stage is capable of driving 600Ω loads connected to any point between V+ and ground.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low voltage supply applications. Figure 1 shows the input and output waveforms for the OPA350 in unity-gain configuration. Operation is from a single +5V supply with a 1kΩ load connected to $V_S/2$. The input is a $5V_{PP}$ sinusoid. Output voltage swing is approximately $4.95V_{PP}$.

Power supply pins should be bypassed with 0.01µF ceramic capacitors.

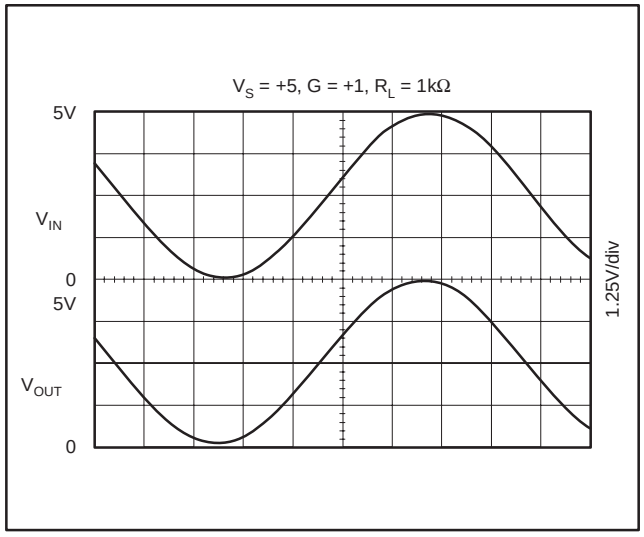


Figure 1. Rail-to-Rail Input and Output

OPERATING VOLTAGE

OPA350 series op amps are fully specified from +2.7V to +5.5V. However, supply voltage may range from +2.5V to +5.5V. Parameters are tested over the specified supply range—a unique feature of the OPA350 series. In addition, many specifications apply from −40°C to +85°C. Most behavior remains virtually unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage or temperature are shown in the typical characteristics.

RAIL-TO-RAIL INPUT

The tested input common-mode voltage range of the OPA350 series extends 100mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 2. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.8V to 100mV above the positive supply, while the P-channel pair is on for inputs from 100mV below the negative supply to approximately (V+) – 1.8V. There is a small transition region, typically (V+) – 2V to (V+) – 1.6V, in which both pairs are on. This 400mV transition region can vary ±400mV with process variation. Thus, the transition region (both input stages on) can range from (V+) – 2.4V to (V+) – 2.0V on the low end, up to (V+) – 1.6V to (V+) – 1.2V on the high end.

OPA350 series op amps are laser-trimmed to reduce offset voltage difference between the N-channel and P-channel input stages, resulting in improved common-mode rejection and a smooth transition between the N-channel pair and the P-channel pair. However, within the 400mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage. Normally, input bias current is approximately 500fA. However, large inputs (greater than 300mV beyond the supply rails) can turn on the OPA350's input protection diodes, causing excessive current to flow in or out of the input pins. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the current on the input pins is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 3. Many input signals are inherently current-limited to less than 10mA; therefore, a limiting resistor is not required.

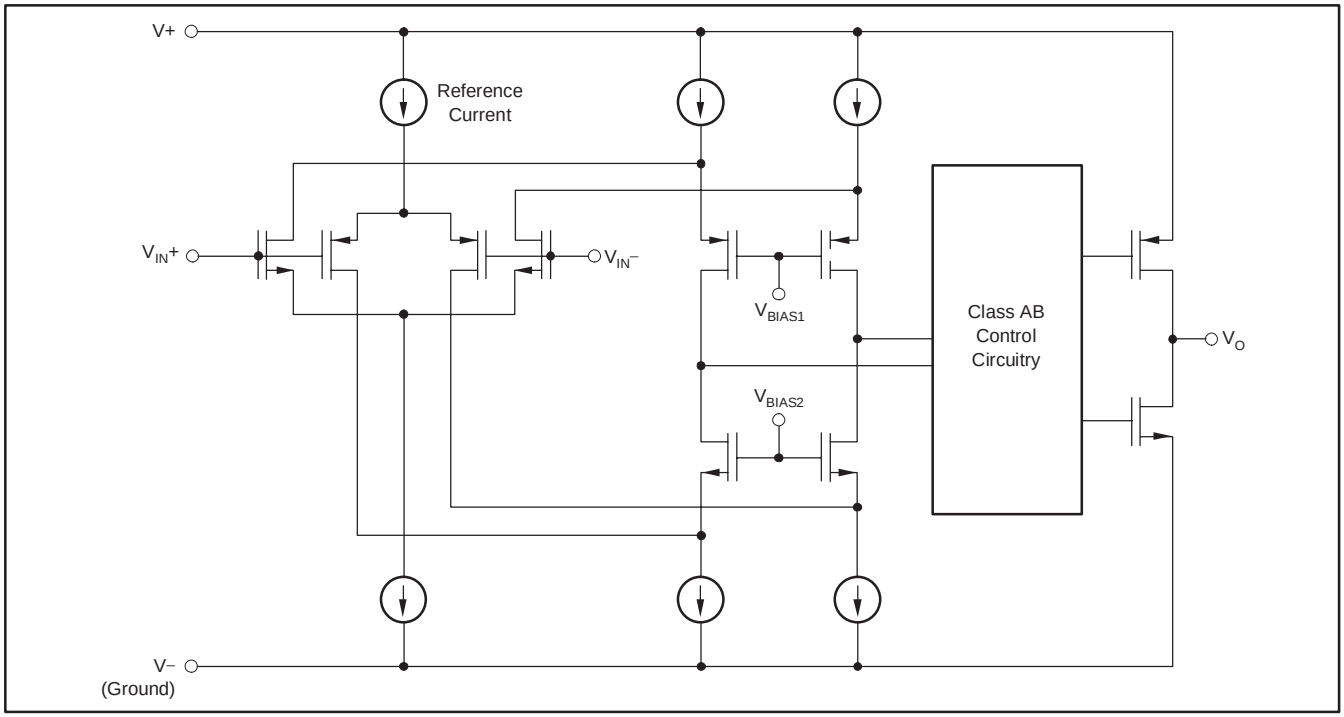


Figure 2. Simplified Schematic

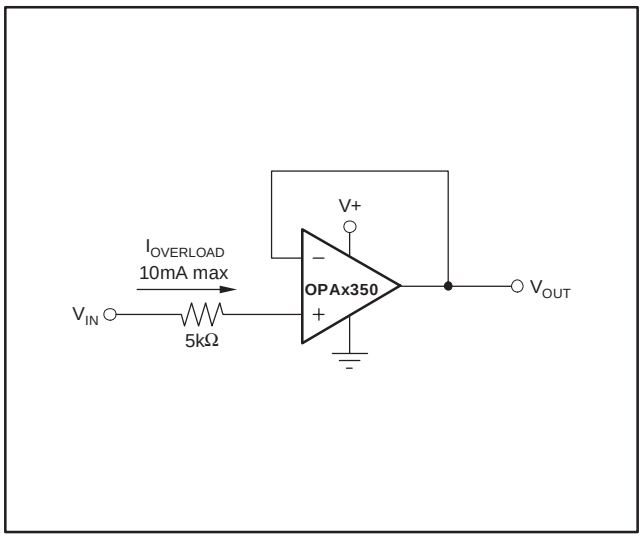


Figure 3. Input Current Protection for Voltages Exceeding the Supply Voltage

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (>10kΩ), the output voltage swing is typically ten millivolts from the supply rails. With heavier resistive loads (600Ω to 10kΩ), the output can swing to within a few tens of millivolts from the supply rails and maintain high open-loop gain. See the typical characteristics *Output Voltage Swing vs Output Current* and *Open-Loop Gain vs Output Voltage*.

CAPACITIVE LOAD AND STABILITY

OPA350 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is the most susceptible to the effects of capacitive load. The capacitive load reacts with the op amp's output impedance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin.

In unity gain, OPA350 series op amps perform well with very large capacitive loads. Increasing gain enhances the amplifier's ability to drive more capacitance. The typical characteristic *Small-Signal Overshoot vs Capacitive Load* shows performance with a 1kΩ resistive load. Increasing load resistance improves capacitive load drive capability.

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 4. This capacitor compensates for the zero created by the feedback network impedance and the OPA350's input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.

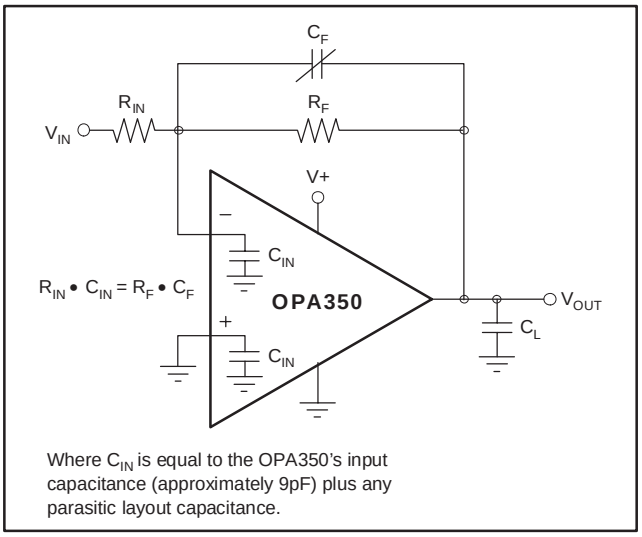


Figure 4. Feedback Capacitor Improves Dynamic Performance

It is suggested that a variable capacitor be used for the feedback capacitor since input capacitance may vary between op amps and layout capacitance is difficult to determine. For the circuit shown in Figure 4, the value of the variable feedback capacitor should be chosen so that the input resistance times the input capacitance of the OPA350 (typically 9pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$$R_{IN} \cdot C_{IN} = R_F \cdot C_F$$

where C_{IN} is equal to the OPA350's input capacitance (sum of differential and common-mode) plus the layout capacitance. The capacitor can be varied until optimum performance is obtained.

DRIVING A/D CONVERTERS

OPA350 series op amps are optimized for driving medium speed (up to 500kHz) sampling A/D converters. However, they also offer excellent performance for higher speed converters. The OPA350 series provides an effective means of buffering the A/D's input capacitance and resulting charge injection while providing signal gain.

Figure 5 shows the OPA350 driving an ADS7861. The ADS7861 is a dual, 500kHz, 12-bit sampling converter in the tiny SSOP-24 package. When used with the miniature package options of the OPA350 series, the combination is ideal for space-limited applications. For further information, consult the ADS7861 data sheet (SBAS110A).

OUTPUT IMPEDANCE

The low frequency open-loop output impedance of the OPA350's common-source output stage is approximately 1kΩ. When the op amp is connected with feedback, this value is reduced significantly by the loop gain of the op amp. For example, with 122dB of open-loop gain, the output impedance is reduced in unity-gain to less than 0.001Ω. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount which results in a ten-fold increase in effective output impedance (see the typical characteristic, *Output Impedance vs Frequency*).

At higher frequencies, the output impedance will rise as the open-loop gain of the op amp drops. However, at these frequencies the output also becomes capacitive due to parasitic capacitance. This prevents the output impedance from becoming too high, which can cause stability problems when driving capacitive loads. As mentioned previously, the OPA350 has excellent capacitive load drive capability for an op amp with its bandwidth.

VIDEO LINE DRIVER

Figure 6 shows a circuit for a single supply, G = 2 composite video line driver. The synchronized outputs of a composite video line driver extend below ground. As shown, the input to the op amp should be ac-coupled and shifted positively to provide adequate signal swing to account for these negative signals in a single-supply configuration.

The input is terminated with a 75Ω resistor and ac-coupled with a 47μF capacitor to a voltage divider that provides the dc bias point to the input. In Figure 6, this point is approximately (V−) + 1.7V. Setting the optimal bias point requires some understanding of the nature of composite video signals. For best performance, one should be careful to avoid the distortion caused by the transition region of the OPA350's complementary input stage. Refer to the discussion of rail-to-rail input.

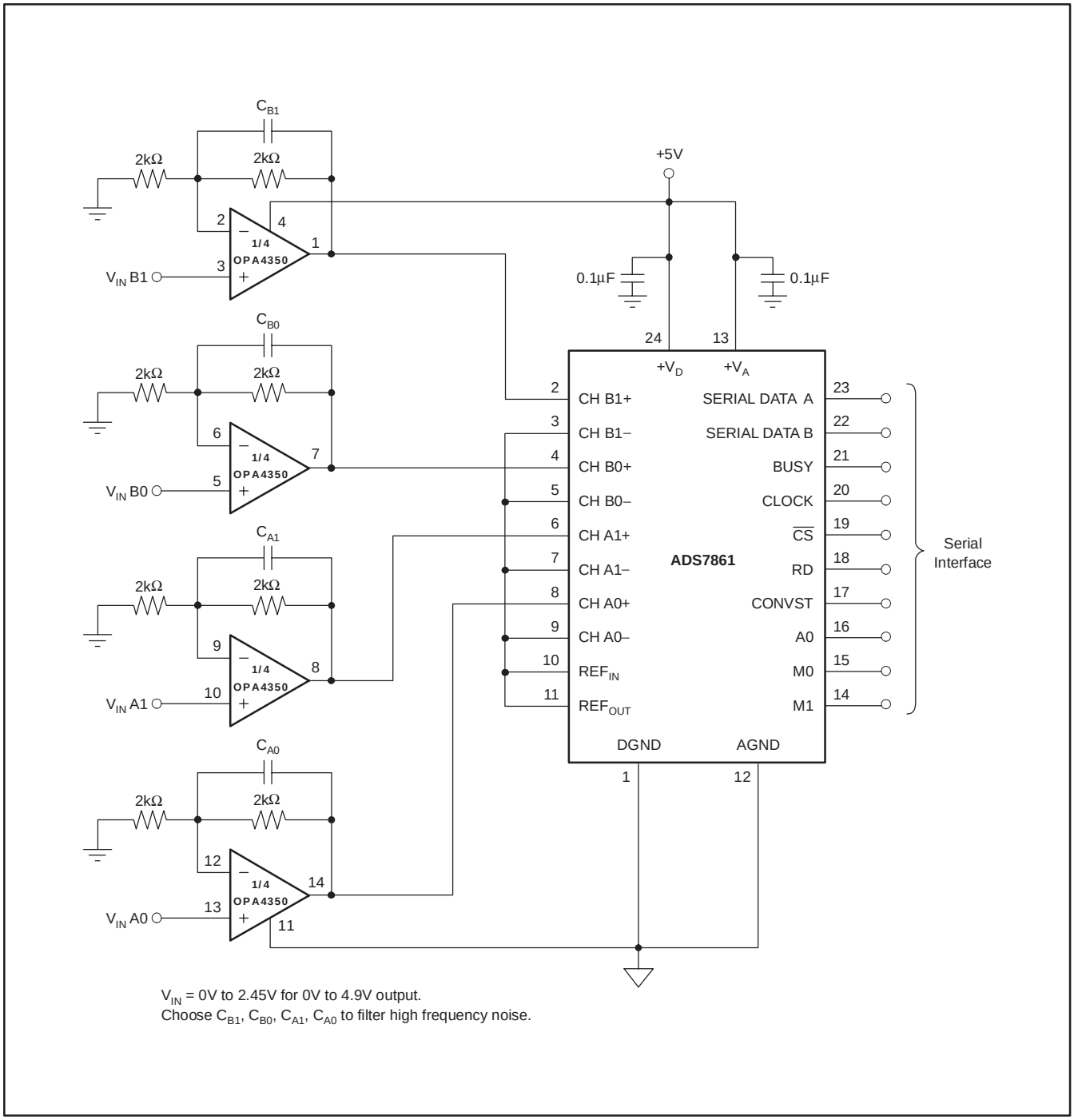


Figure 5. OPA4350 Driving Sampling A/D Converter

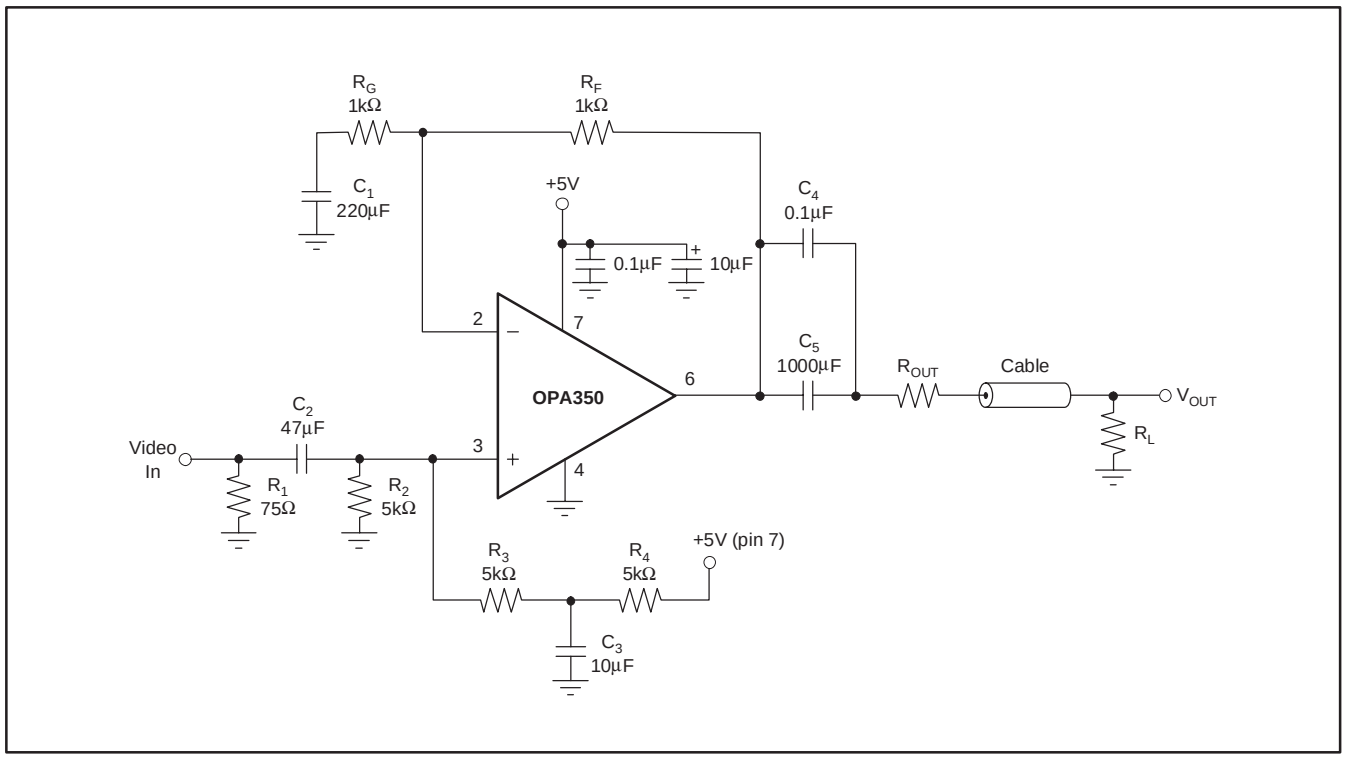


Figure 6. Single-Supply Video Line Driver

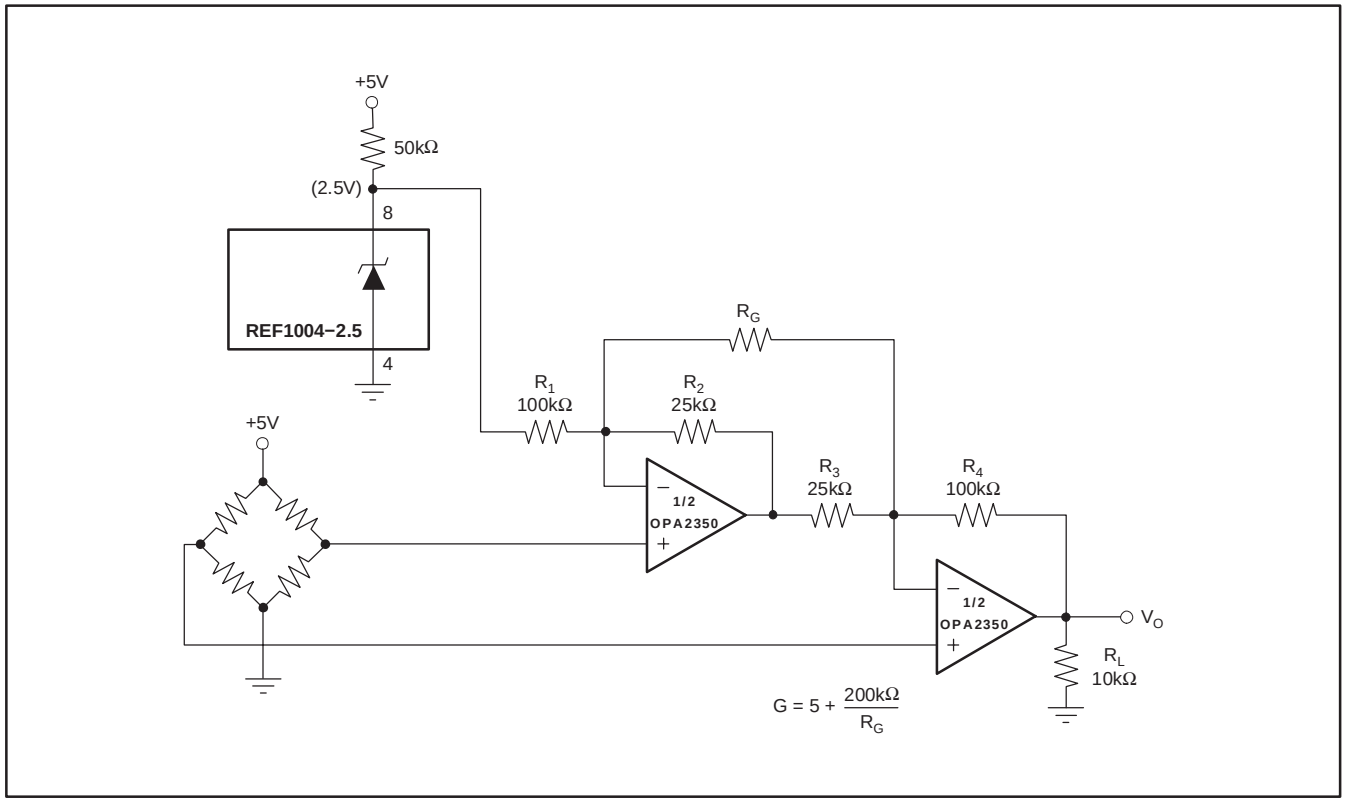


Figure 7. Two Op-Amp Instrumentation Amplifier With Improved High Frequency Common-Mode Rejection

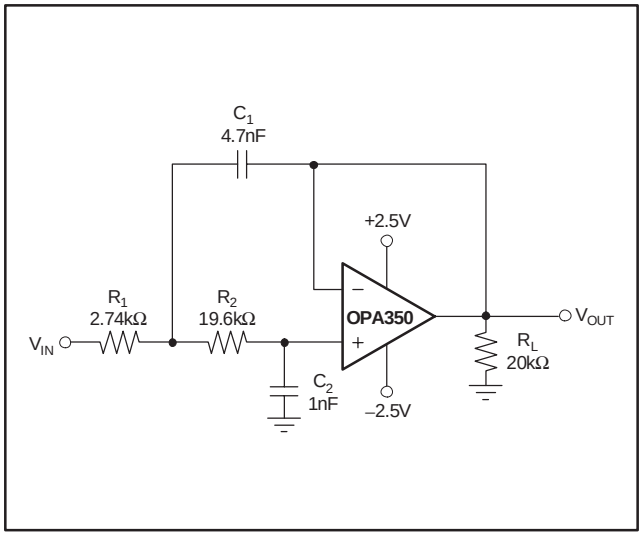


Figure 8. 10kHz Low-Pass Filter

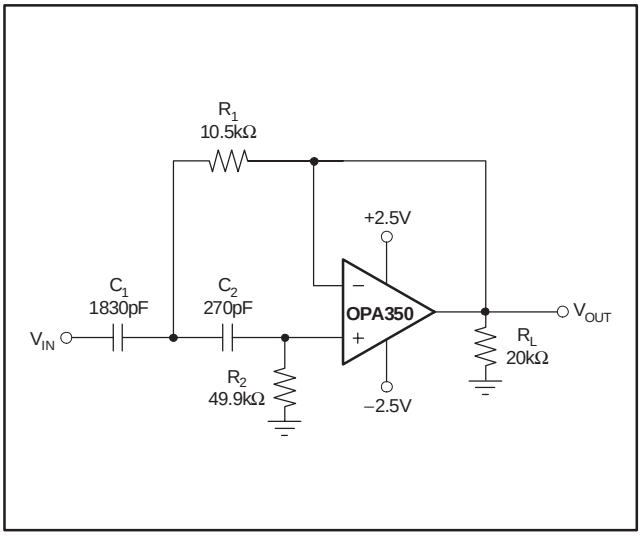


Figure 9. 10kHz High-Pass Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA2350EA/250	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2350EA/250G4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2350EA/2K5	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2350EA/2K5G4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2350PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2350PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2350UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2350UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2350UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2350UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA350EA/250	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA350EA/250G4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA350EA/2K5	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA350EA/2K5G4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA350PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA350PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA350UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA350UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA350UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA350UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA4350EA/250	ACTIVE	SSOP/ QSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA4350EA/250G4	ACTIVE	SSOP/ QSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA4350EA/2K5	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA4350EA/2K5G4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA4350UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA4350UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA4350UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA4350UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

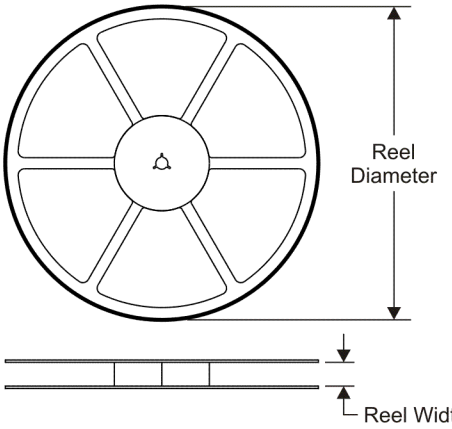
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

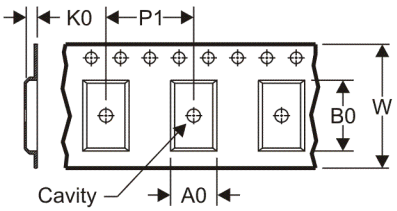
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

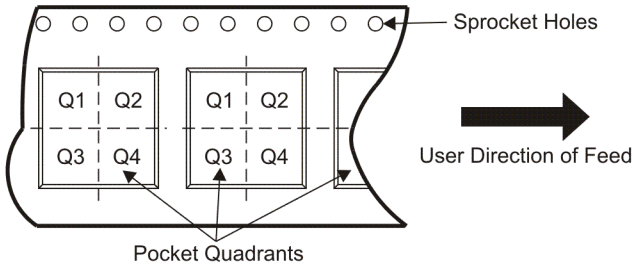


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

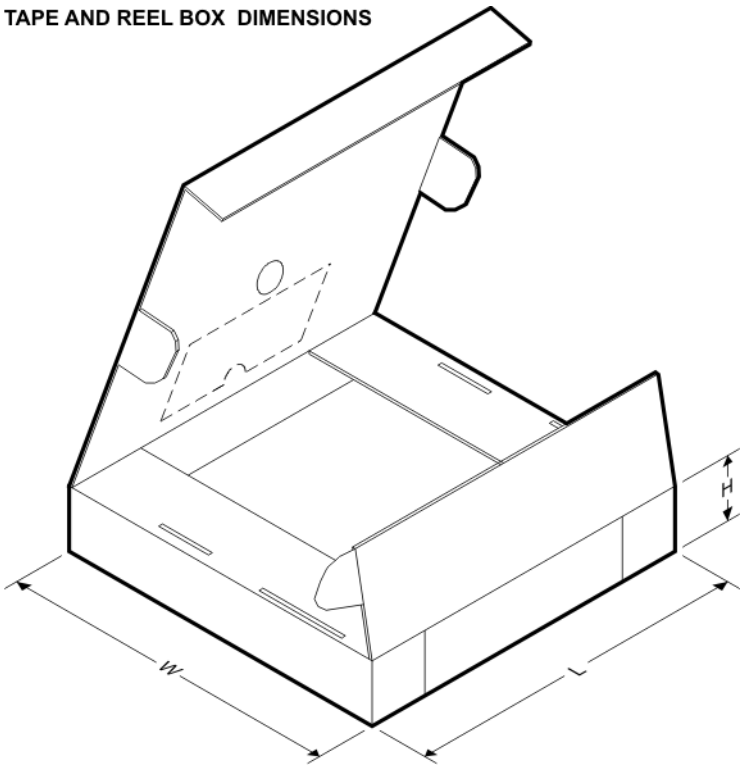
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2350EA/250	MSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2350EA/2K5	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2350UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA350EA/250	MSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA350EA/2K5	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA350UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4350EA/250	SSOP/ QSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4350EA/2K5	SSOP/ QSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4350UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

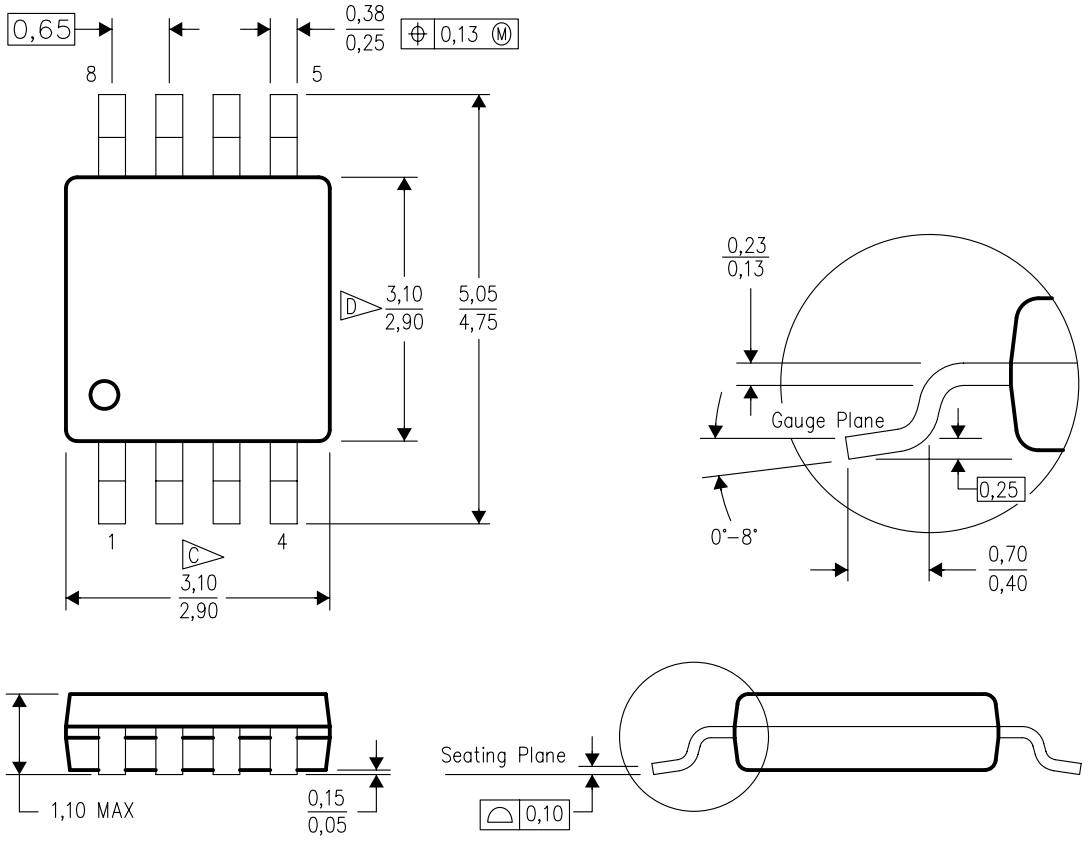
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2350EA/250	MSOP	DGK	8	250	190.5	212.7	31.8
OPA2350EA/2K5	MSOP	DGK	8	2500	346.0	346.0	29.0
OPA2350UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA350EA/250	MSOP	DGK	8	250	190.5	212.7	31.8
OPA350EA/2K5	MSOP	DGK	8	2500	346.0	346.0	29.0
OPA350UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA4350EA/250	SSOP/QSOP	DBQ	16	250	190.5	212.7	31.8
OPA4350EA/2K5	SSOP/QSOP	DBQ	16	2500	346.0	346.0	29.0
OPA4350UA/2K5	SOIC	D	14	2500	346.0	346.0	33.0

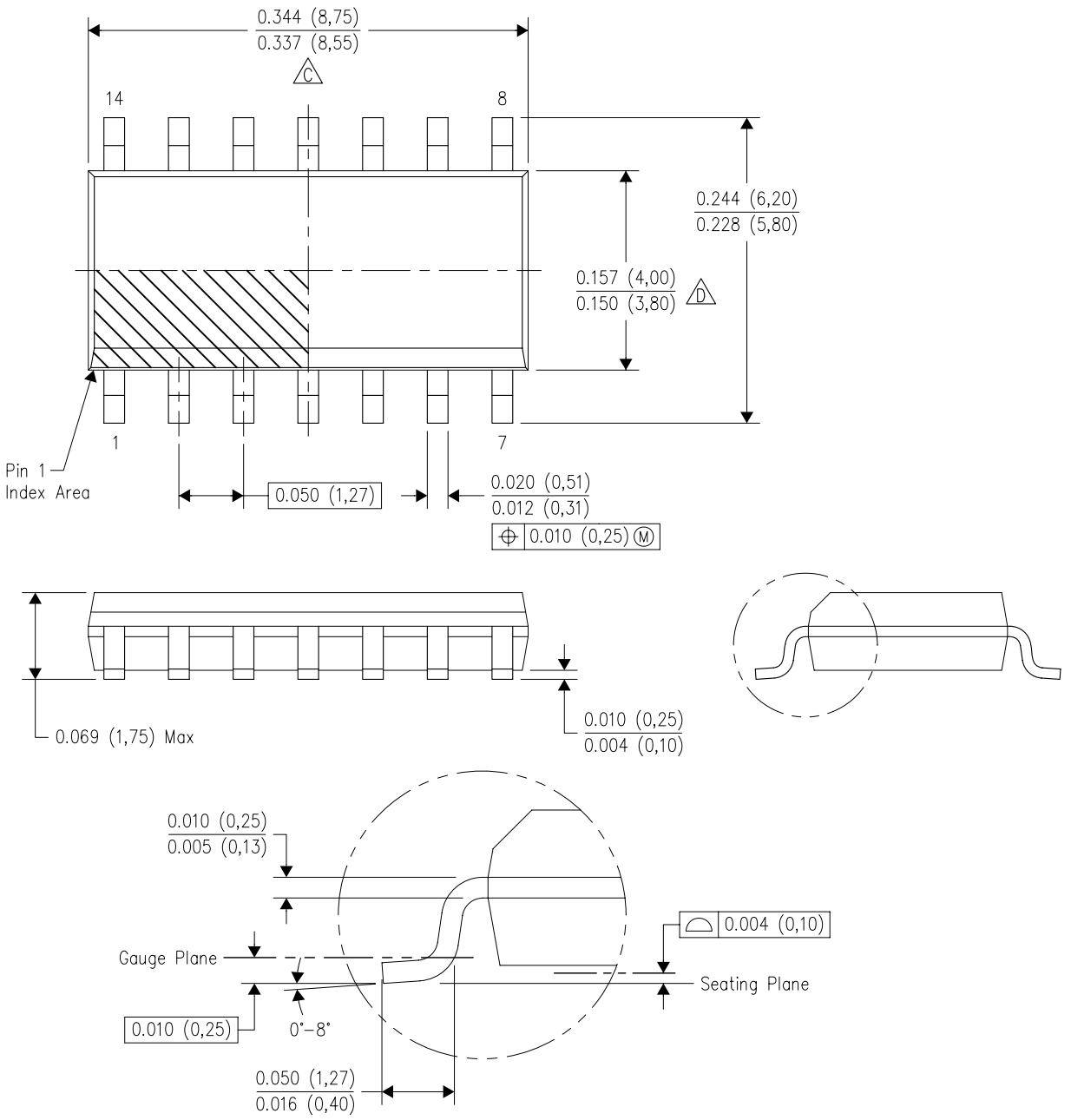
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

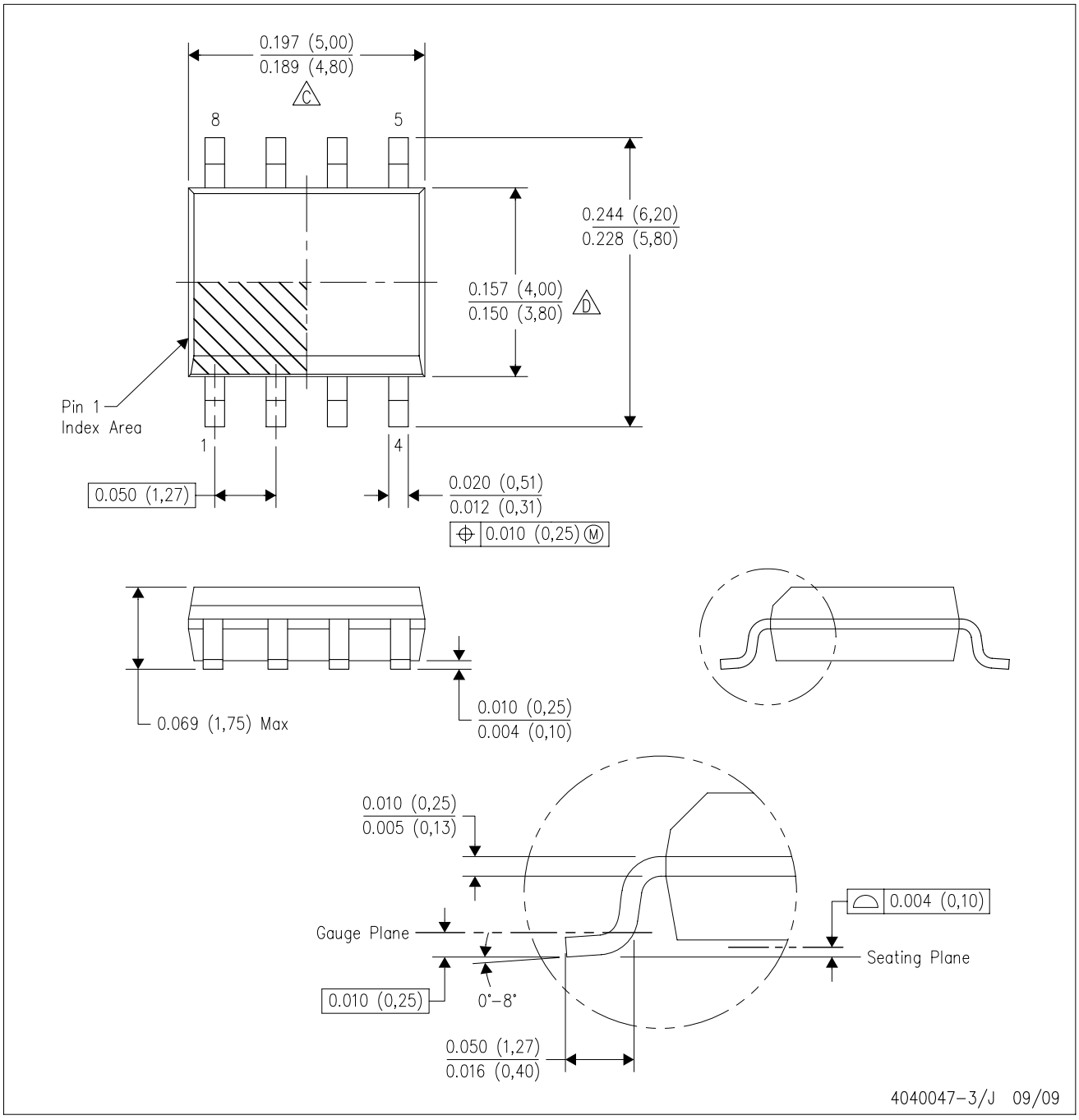
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

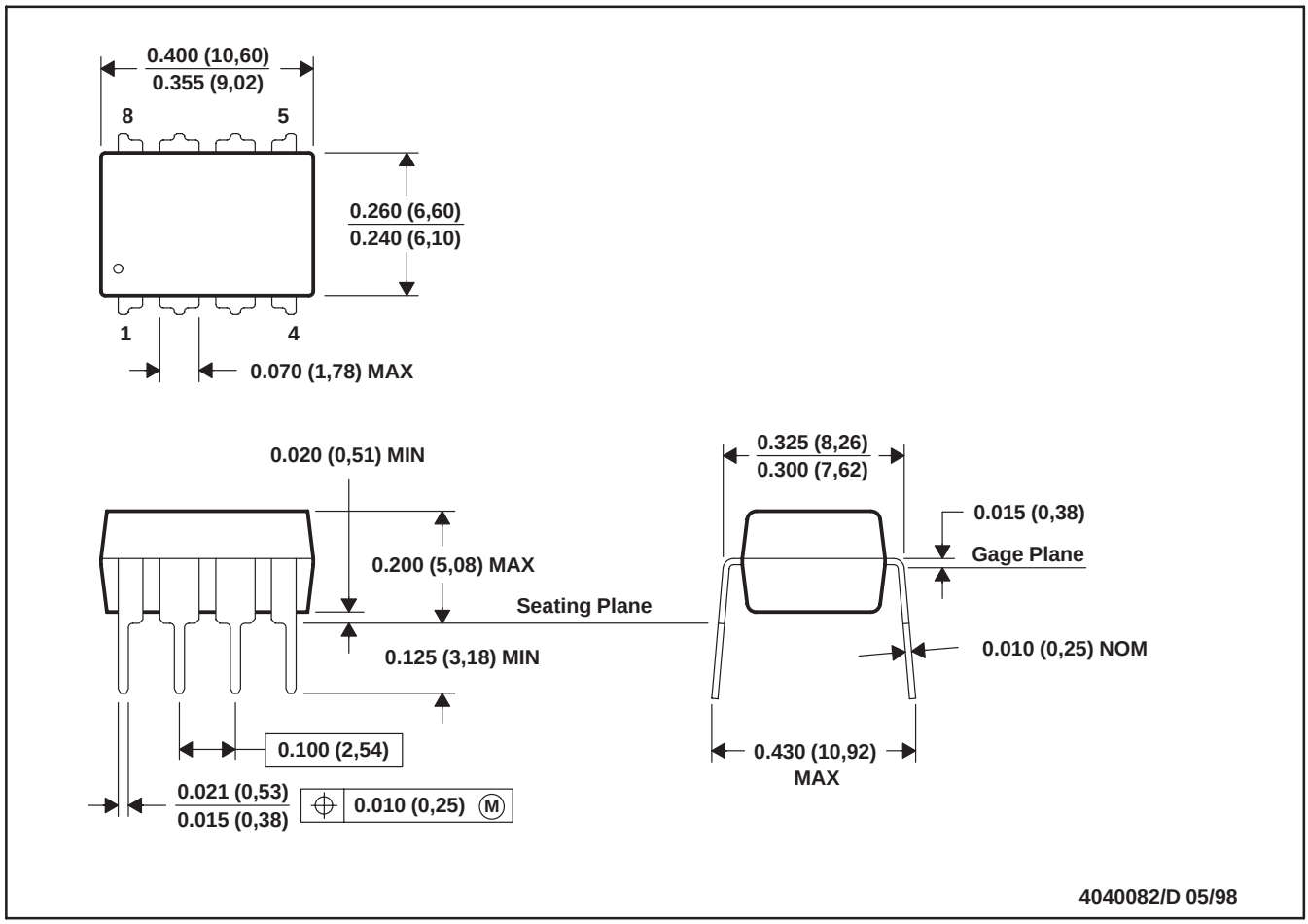
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

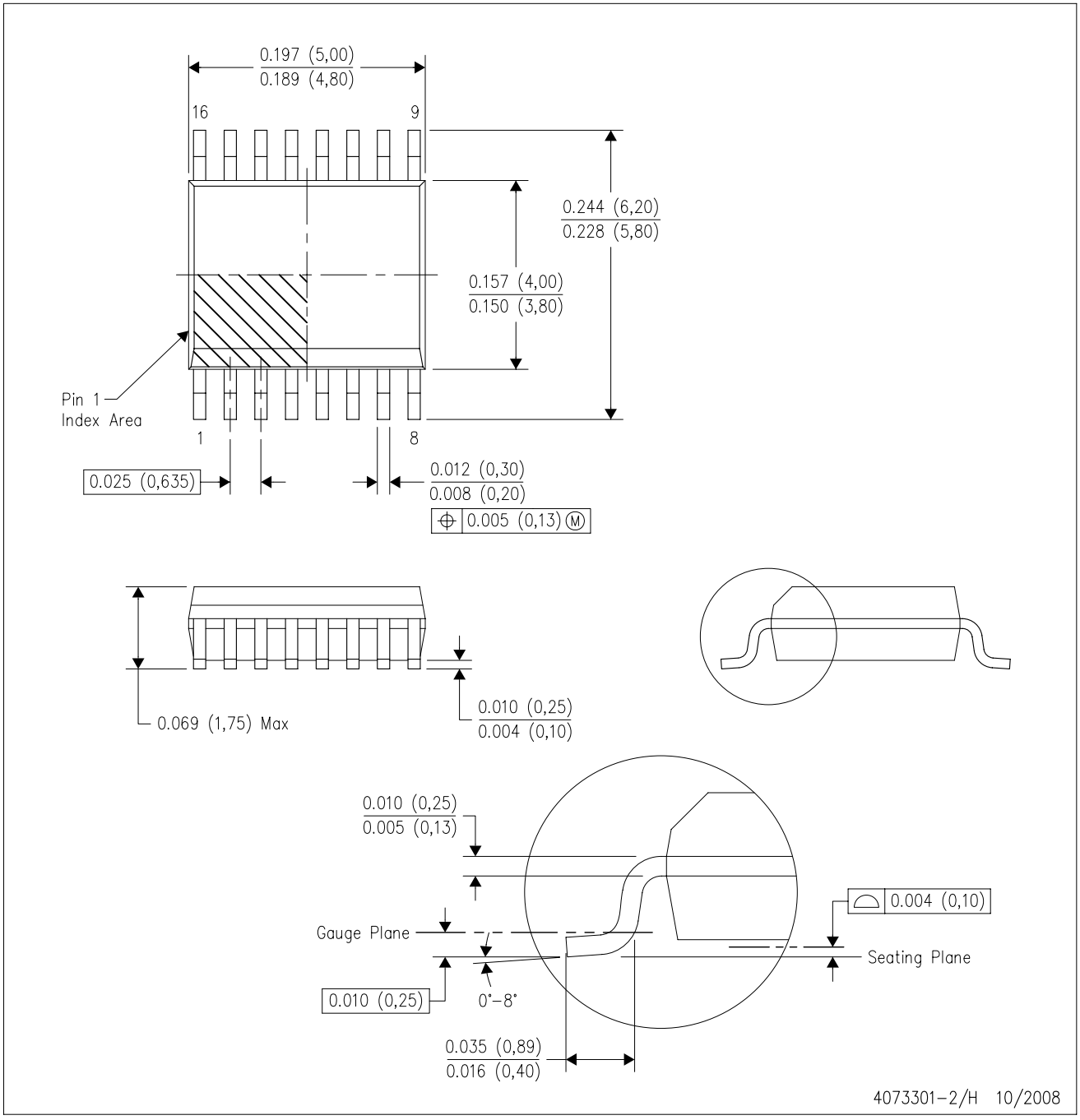
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

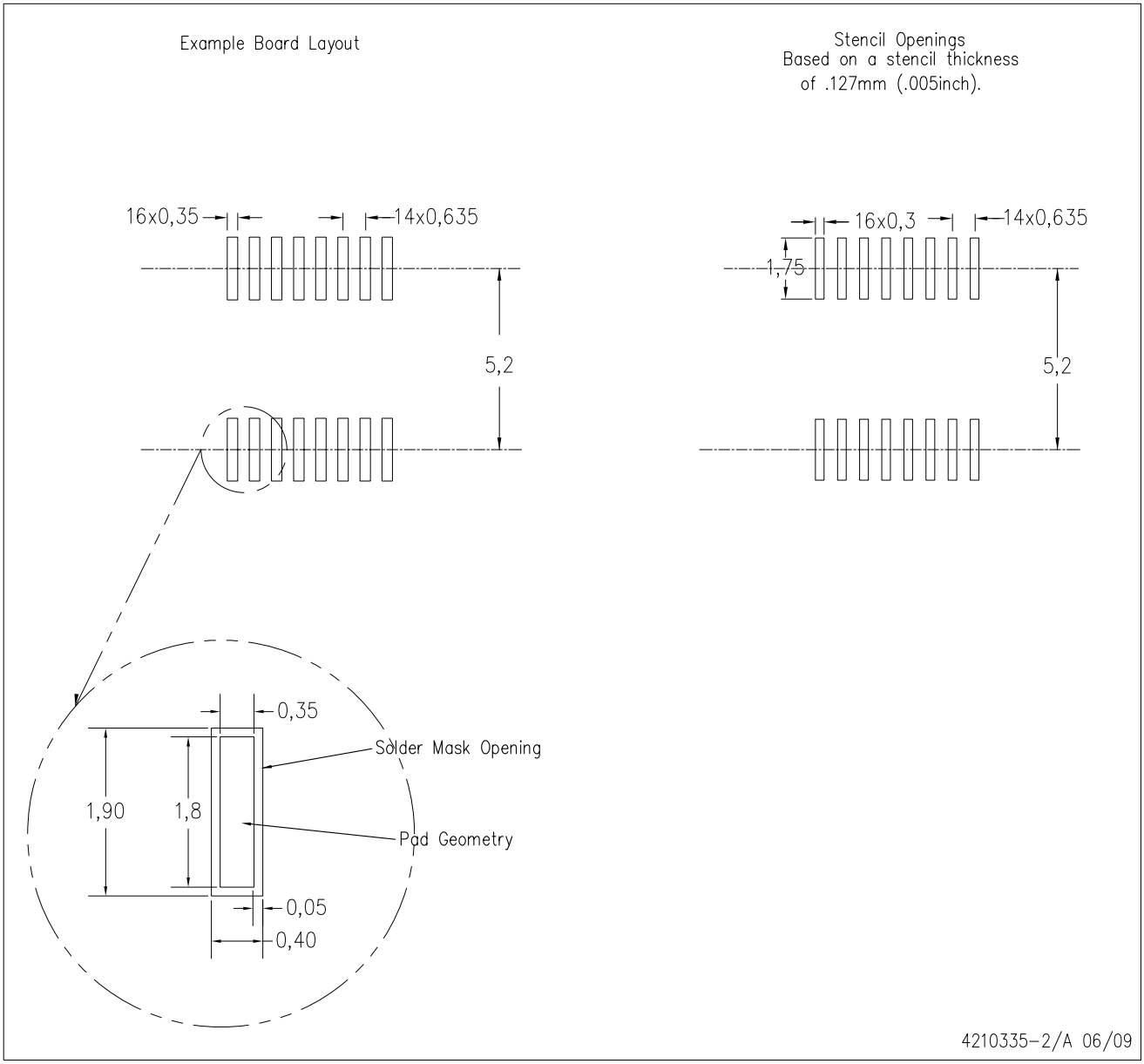
For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

DBQ (R–PDSO–G16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

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Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

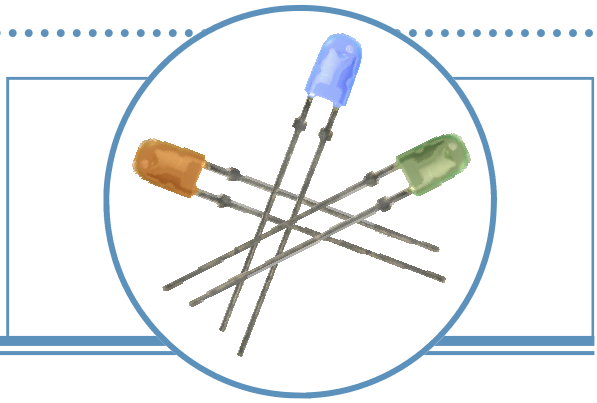
Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Oval Blue LED Lamp (4mm)

TT electronics
OPTEK Technology

OVLJBGD8

- High luminous intensity
- Defined spatial radiation
- Multiple viewing angles
- UV-resistant epoxy
- Precision optical performance

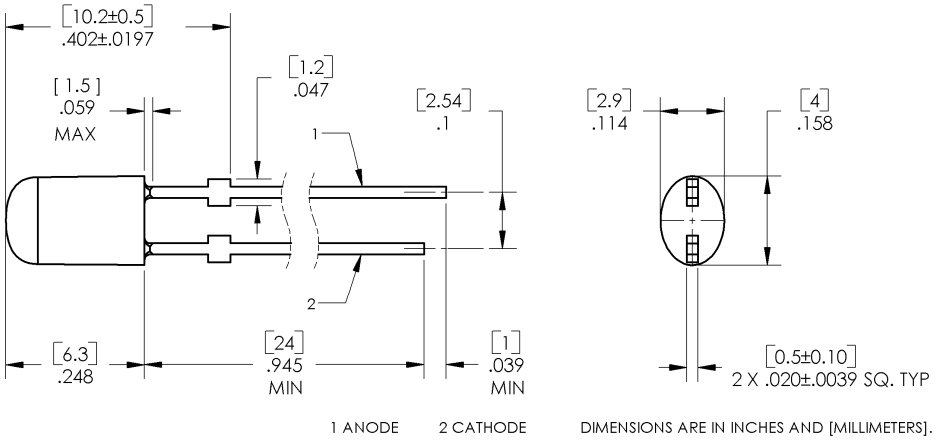


The OVLJBGD8 is designed for superior performance in outdoor environments. Its radiation pattern matches red (OVLJRGD8) and green (OVLJGGD8) devices in identical packages to create LED pixels for full-color video screens.

Applications

- Variable Message Signs
- Indoor/Outdoor Advertising Signage
- Traffic and Highway Signs
- Full-Color Video Signs

Part Number	Material	Emitted Color	Intensity Typ. mcd	Lens Color
OVLJBGD8	InGaN	Blue	300	Blue Diffused



1 ANODE 2 CATHODE

DIMENSIONS ARE IN INCHES AND [MILLIMETERS].

RoHS

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ELECTROSTATIC
SENSITIVE DEVICES

Data is subject to change without prior notice.

Oval Blue LED Lamp (4mm)
OVLJBGD8

TT electronics
OPTEK Technology

Absolute Maximum Ratings
T_A = 25° C unless otherwise noted

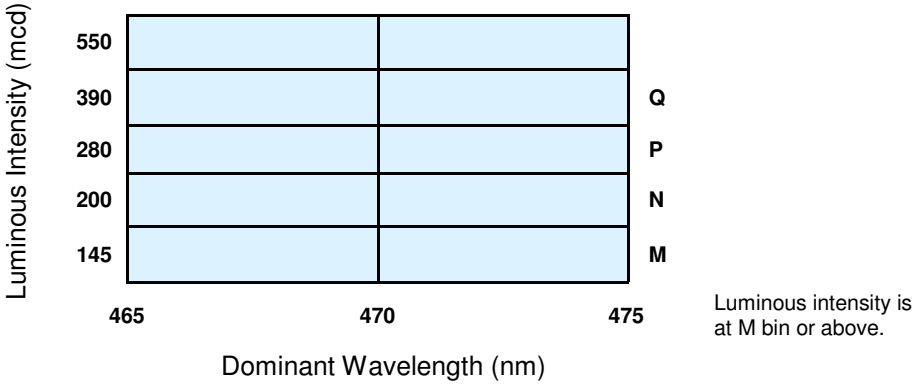
Storage Temperature Range	-40 ~ +100 ℃
Operating Temperature Range	-40 ~ +95 ℃
Reverse Voltage	5 V
Continuous Forward Current	25 mA
Peak Forward Current (10% Duty Cycle, 1KHz)	100 mA
Power Dissipation	105 mW
Lead Soldering Temperature (3mm from the base of the epoxy bulb)[1]	260℃

Note:
1. Solder time less than 3 seconds at temperature extreme.

Electrical Characteristics
T_A = 25° C unless otherwise noted

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_v	Luminous Intensity	145	300	----	mcd	I_F = 20mA
V_F	Forward Voltage	----	3.6	4.2	V	I_F = 20mA
I_R	Reverse Current	----	----	100	μA	V_R = 5V
λ_D	Dominant Wavelength	465	470	475	nm	I_F = 20mA
2Θ½H-H	50% Power Angle	----	100	----	deg	I_F = 20mA
2Θ½V-V		----	50	----	deg	I_F = 20mA

Standard Bins (I_F = 20mA)
Lamps are sorted to luminous intensity (I_V) and dominant wavelength (λ_D) bins shown.
Orders for OVLJBGD8 may be filled with any or all bins contained as below.

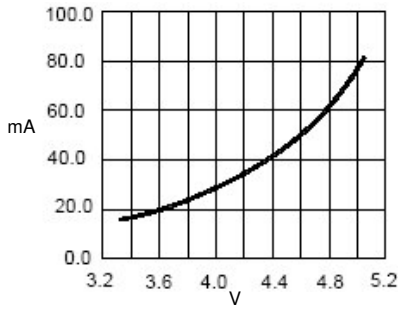


Luminous intensity is at M bin or above.

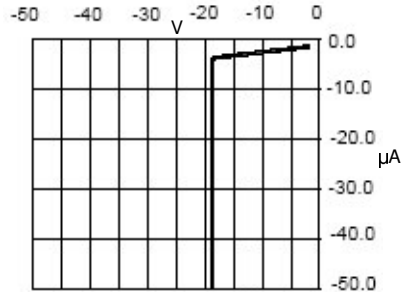
Important Notes:
1. All ranks will be included per delivery, rank ratio will be based on the chip distribution.
2. To designate luminous intensity ranks, please contact OPTEK.
3. Pb content <1000PPM.

OPTEK Technology Inc. — 1645 Wallace Drive, Carrollton, Texas 75006
Phone: (972) 323-2200 or (800) 341-4747 FAX: (972) 323-2396 visibleLED@optekinc.com www.optekinc.com

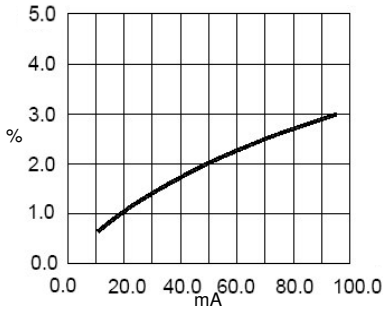
Typical Electro-Optical Characteristics Curves



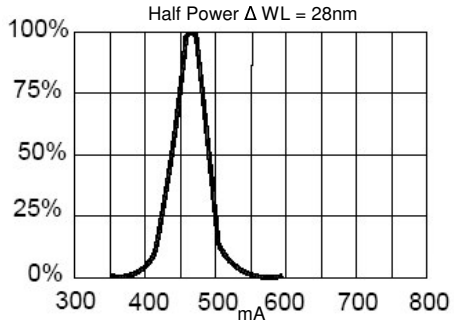
Forward Current vs. Forward Voltage



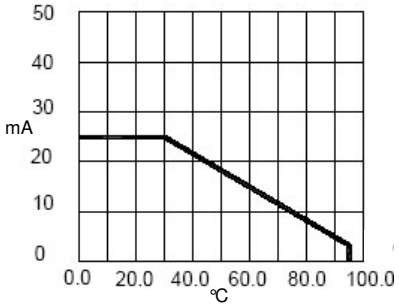
Reverse Current vs. Reverse Voltage



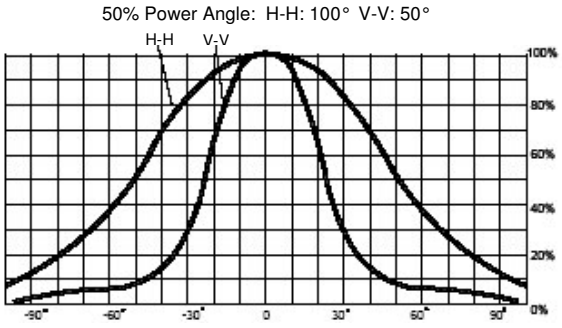
Relative Luminous Intensity vs. Forward Current



Relative Luminous Intensity vs. Wavelength



Maximum Forward DC Current vs. Ambient Temperature



Far Field Pattern

Issue	Change Description	Approval	Date
1.0	Initial Release	J. Haynie	5/26/05

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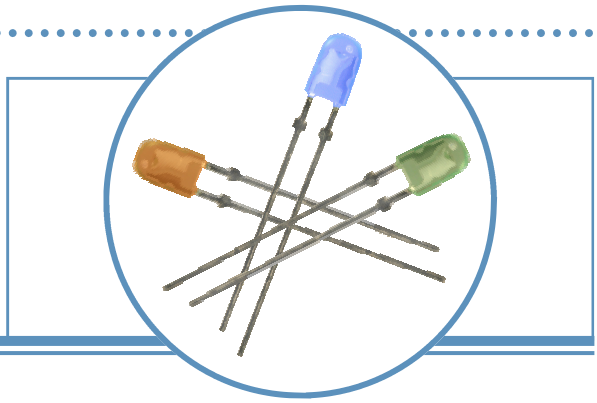
Oval Green LED Lamp (4mm)

TT electronics
OPTEK Technology

OVLJGGD8

- High luminous intensity
- Defined spatial radiation
- Multiple viewing angles
- UV-resistant epoxy
- Precision optical performance

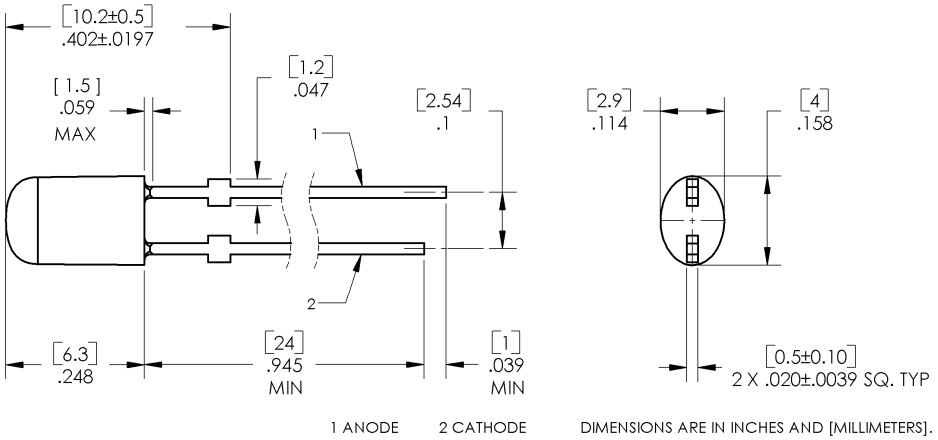


The OVLJGGD8 is designed for superior performance in outdoor environments. Its radiation pattern matches red (OVLJRGD8) and blue (OVLJBGD8) devices in identical packages to create LED pixels for full-color video screens.

Applications

- Variable Message Signs
- Indoor/Outdoor Advertising Signage
- Traffic and Highway Signs
- Full-Color Video Signs

Part Number	Material	Emitted Color	Intensity Typ. mcd	Lens Color
OVLJGGD8	InGaN	Green	1200	Green Diffused



RoHS

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ELECTROSTATIC
SENSITIVE DEVICES

Data is subject to change without prior notice.

Absolute Maximum Ratings

T_A = 25° C unless otherwise noted

Storage Temperature Range	-40 ~ +100 ℃
Operating Temperature Range	-40 ~ +95 ℃
Reverse Voltage	5 V
Continuous Forward Current	25 mA
Peak Forward Current (10% Duty Cycle, 1KHz)	100 mA
Power Dissipation	105 mW
Lead Soldering Temperature (3mm from the base of the epoxy bulb)[1]	260℃

Note:
1. Solder time less than 3 seconds at temperature extreme.

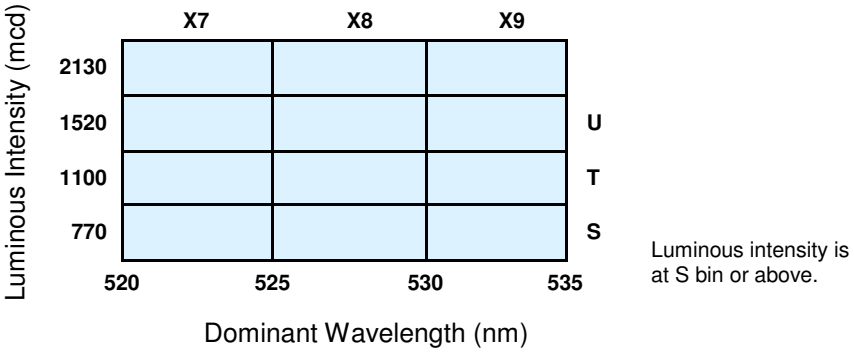
Electrical Characteristics

T_A = 25° C unless otherwise noted

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_v	Luminous Intensity	770	1200	----	mcd	I_F = 20mA
V_F	Forward Voltage	----	3.6	4.2	V	I_F = 20mA
I_R	Reverse Current	----	----	100	μA	V_R = 5V
λ_D	Dominant Wavelength	520	525	535	nm	I_F = 20mA
2Θ½H-H	50% Power Angle	----	100	----	deg	I_F = 20mA
2Θ½V-V		----	50	----	deg	I_F = 20mA

Standard Bins (I_F = 20mA)

Lamps are sorted to luminous intensity (I_V) and dominant wavelength (λ_D) bins shown.
Orders for OVLJGGD8 may be filled with any or all bins contained as below.



Luminous intensity is at S bin or above.

Important Notes:
1. All ranks will be included per delivery, rank ratio will be based on the chip distribution.
2. To designate luminous intensity ranks, please contact OPTEK.
3. Pb content <1000PPM.

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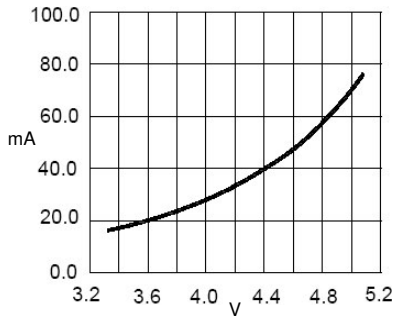
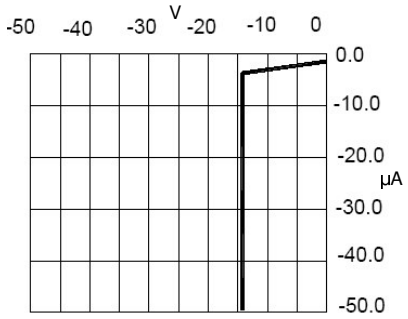
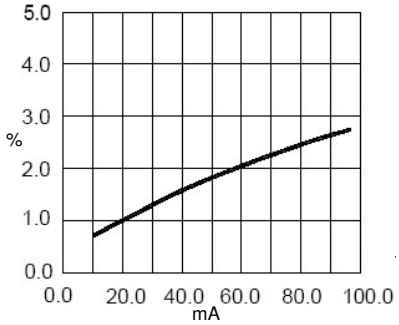
Typical Electro-Optical Characteristics Curves



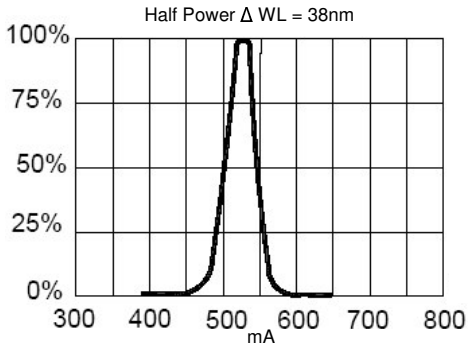
Forward Current vs. Forward Voltage



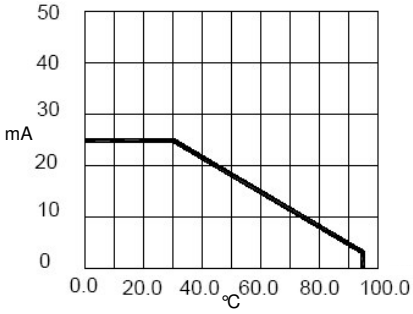
Reverse Current vs. Reverse Voltage



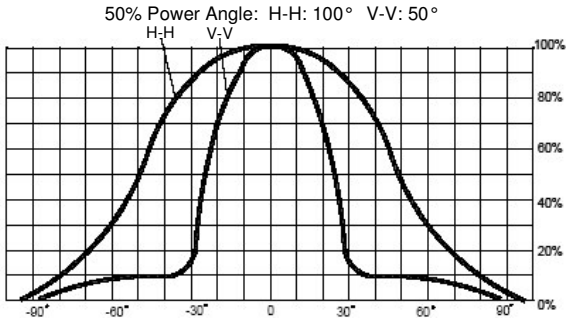
Relative Luminous Intensity vs. Forward Current



Relative Luminous Intensity vs. Wavelength



Maximum Forward DC Current vs. Ambient Temperature



Far Field Pattern

Issue	Change Description	Approval	Date
1.0	Initial Release	J. Haynie	5/26/05

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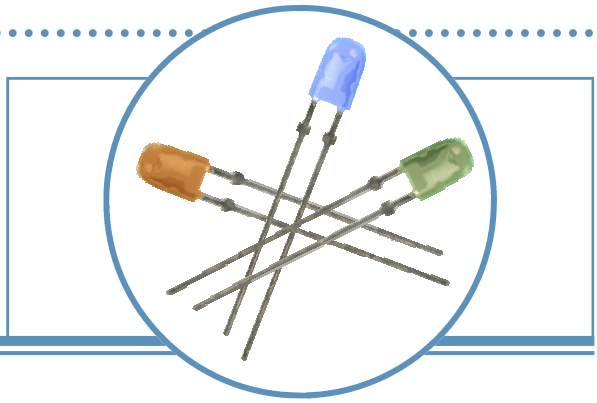
Oval Red LED Lamp (4mm)

TT electronics
OPTEK Technology

OVLJRGD8

- High luminous intensity
- Defined spatial radiation
- Multiple viewing angles
- UV-resistant epoxy
- Precision optical performance

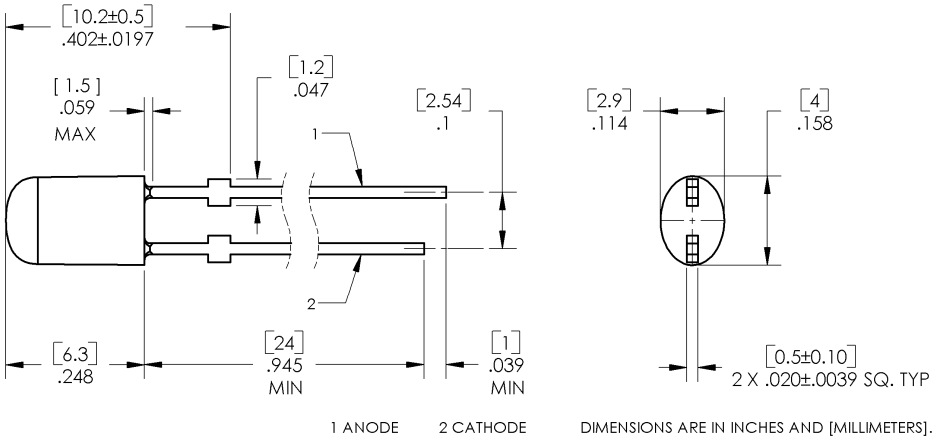


The OVLJRGD8 is designed for superior performance in outdoor environments. Its radiation pattern matches green (OVLJGGD8) and blue (OVLJBGD8) devices in identical packages to create LED pixels for full-color video screens.

Applications

- Variable Message Signs
- Indoor/Outdoor Advertising Signage
- Traffic and Highway Signs
- Full-Color Video Signs

Part Number	Material	Emitted Color	Intensity Typ. mcd	Lens Color
OVLJRGD8	AlInGaP	Red	400	Red Diffused



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SENSITIVE DEVICES

Data is subject to change without prior notice.

Oval Red LED Lamp (4mm)
OVLJRGD8

Absolute Maximum Ratings
T_A = 25° C unless otherwise noted

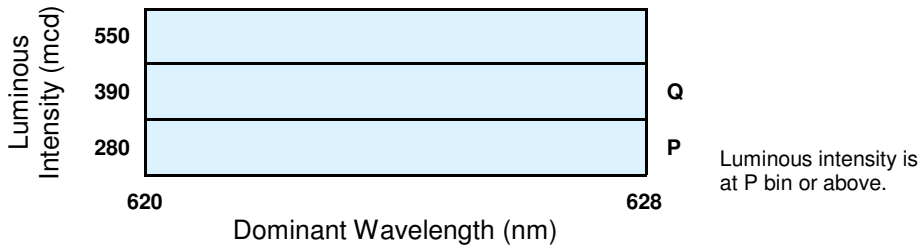
Storage Temperature Range	-40 ~ +100 ℃
Operating Temperature Range	-40 ~ +95 ℃
Reverse Voltage	5 V
Continuous Forward Current[1]	50 mA
Peak Forward Current (10% Duty Cycle, 1KHz)	200 mA
Power Dissipation	125 mW
Lead Soldering Temperature (3mm from the base of the epoxy bulb)[2]	260℃

Notes:
1. For long term performance the drive currents between 10mA and 30mA are recommended. Please contact an Optek sales representative for more information on recommended drive conditions.
2. Solder time less than 3 seconds at temperature extreme.

Electrical Characteristics
T_A = 25° C unless otherwise noted

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_v	Luminous Intensity	280	400	----	mcd	I_F = 20mA
V_F	Forward Voltage	----	2.0	2.5	V	I_F = 20mA
I_R	Reverse Current	----	----	100	µA	V_R = 5V
λ_D	Dominant Wavelength	620	624	628	nm	I_F = 20mA
2Θ½H-H	50% Power Angle	----	100	----	deg	I_F = 20mA
2Θ½V-V		----	50	----	deg	I_F = 20mA

Standard Bins (I_F = 20mA)
Lamps are sorted to luminous intensity (I_V) and dominant wavelength (λ_D) bins shown.
Orders for OVLJRGD8 may be filled with any or all bins contained as below.



Important Notes:
1. All ranks will be included per delivery, rank ratio will be based on the chip distribution.
2. To designate luminous intensity ranks, please contact OPTEK.
3. Pb content <1000PPM.

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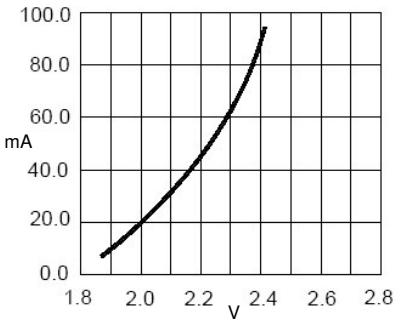
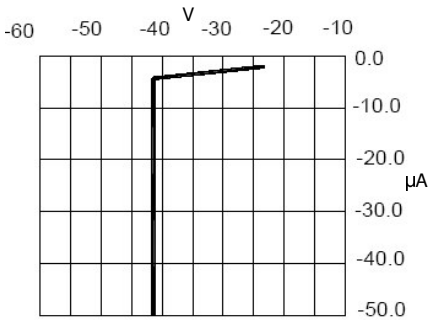
Phone: (972) 323-2200 or (800) 341-4747 FAX: (972) 323-2396 visibleLED@optekinc.com www.optekinc.com

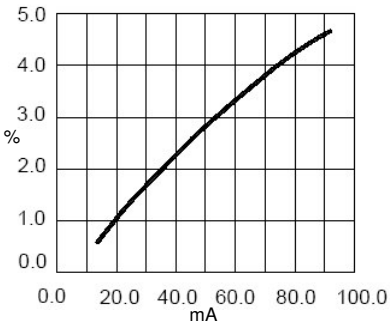
Typical Electro-Optical Characteristics Curves



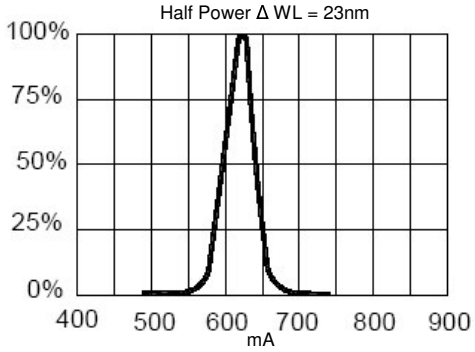
Forward Current vs. Forward Voltage



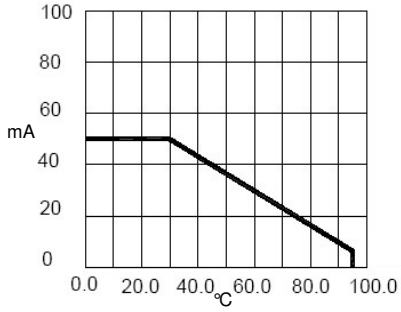
Reverse Current vs. Reverse Voltage



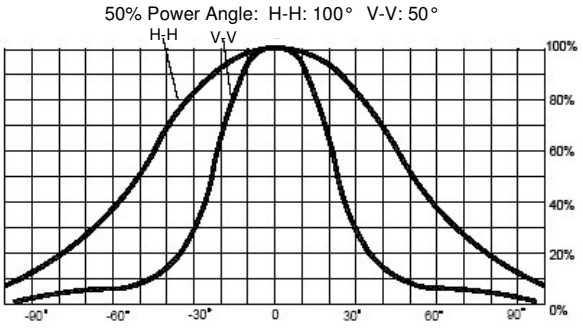
Relative Luminous Intensity vs. Forward Current



Relative Luminous Intensity vs. Wavelength



Maximum Forward DC Current vs. Ambient Temperature



Far Field Pattern

Issue	Change Description	Approval	Date
1.0	Initial Release	J. Haynie	5/26/05

OPTEK Technology Inc. — 1645 Wallace Drive, Carrollton, Texas 75006
Phone: (972) 323-2200 or (800) 341-4747 FAX: (972) 323-2396 visibleLED@optekinc.com www.optekinc.com

Digilent PmodDA1™ Digital To Analog Module Converter Board Reference Manual

Revision: 04/12/05

www.digilentinc.com

215 E Main Suite D | Pullman, WA 99163
(509) 334 6306 Voice and Fax

Overview

The Digilent PmodAD1 Digital to Analog Module Converter module (the DA1™) converts signals from digital to analog at up to one MSa per second. The DA1 uses a 6-pin header connector and at less than one square inch is small enough to be located where the reconstructed signal is needed.

Features include:

- two AD7303 8-bit D/A converter chips that convert up to one MSa per second
- a 6-pin header and 6-pin connector
- four D/A conversion channels
- very low power consumption
- small form factor (0.80” x 0.80”).

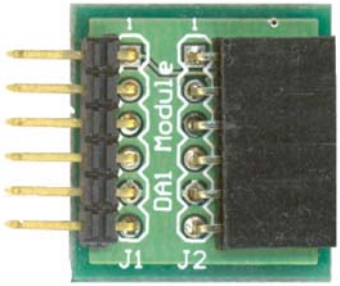
Functional Description

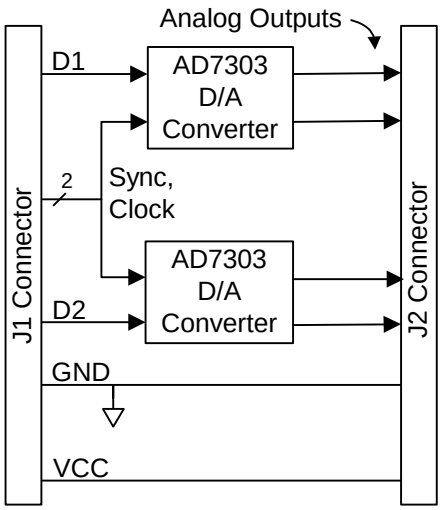
The DA1 can produce an analog output ranging from 0-3.3 volts. It has four simultaneous D/A conversion channels, each with an 8-bit converter that can process separate digital signals.

The DA1 is equipped with two AD7303 digital to analog converters. Each converter has two channels through which digital signals can be converted to analog signals.

Outputs are produced by sending commands via the SPI/MICROWIRE™ serial bus to the D/A converters. The two converters are connected in parallel so that commands are sent to both converters simultaneously.

The DA1 is designed to work with Digilent system boards. Some system boards, like the Digilent Pegasus board, have a 6-pin header that can be connected to the DA1’s 6-pin header using a 6-pin cable.





DA1 Circuit Diagram

Other Digilent boards may need a Digilent Modular Interface Board (MIB) and a 6-pin cable to connect to the DA1. The MIB plugs into the system board and the cable connects the MIB to the DA1.

The DA1 can be powered by voltage from either a Digilent system board or an outside device. Damage can result if power is supplied from both sources or if the outside device supplies more than 3V. For more information, see www.digilentinc.com.

For information on the AD7303, see the Analog Devices data sheet at www.analog.com.

PmodDA1™ Reference Component

Revision: December 1, 2008

This document was produced by Digilent Romania. For questions, contact support@digilent.ro.

Overview

The PmodDA1 Reference Component synchronizes data communications between a Digilent FPGA development board and the PmodDA1 board.

The PmodDA1 Reference Component inputs a digital signal and shifts out the data serially to the PmodDA1. It takes in an 8-bit vector and shifts out a 16-bit frame containing the 8-bit data vector along with the control signals. It also supplies the appropriate timing sequence to clock the PmodDA1.

Functional Description

Component Architecture

The VHDL component is an entity named DA1RefComp that has five inputs and five outputs. The input ports are a 50MHz clock (labeled CLK) that is divided down and used to clock the processes in the component, and an asynchronous reset signal (labeled RST) that resets the processes that occur inside the component. The data inputs for the two AD7303 chips are two 8-bit vectors (DATA1 and DATA2) that are shifted out serially to the PmodDA1 data pins. The START input signal is used to tell the component when to start a conversion.

The output ports are the divided clock signal CLK_OUT (12MHz), and two serial outputs (D1 and D2) that provide the shifted data to the PmodDA1. An nSYNC output is used to latch the data inside the PmodDA1 after the data has been shifted out. An output labeled DONE tells the user when the conversion is done. A block diagram of the component is shown in Figure 1.

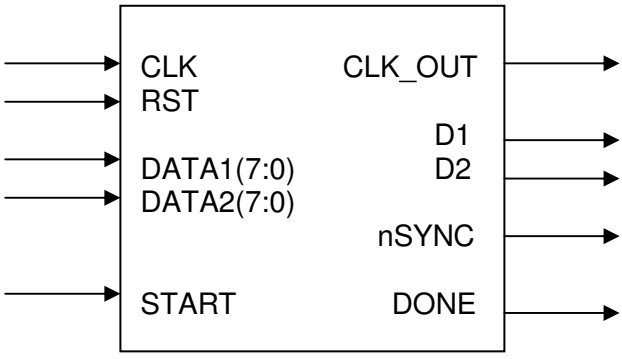


Figure 1 ***PmodDA1 Reference Component***

Timing

The timing diagram in figure 2 is used to determine the correct timing sequence for the finite state machine that clocks the PmodDA1. It is the timing sequence that is used to send 16 bits of data to AD7303 chips inside the PmodDA1. The two data signals are sent to the first channels of the two AD7303 chips. The signal nSYNC must be at a low or zero state while the data is transferred in on the rising edge of the clock signal. Immediately following the data transfer, the signal nSYNC must be driven high to latch the data into the AD7303 chip.

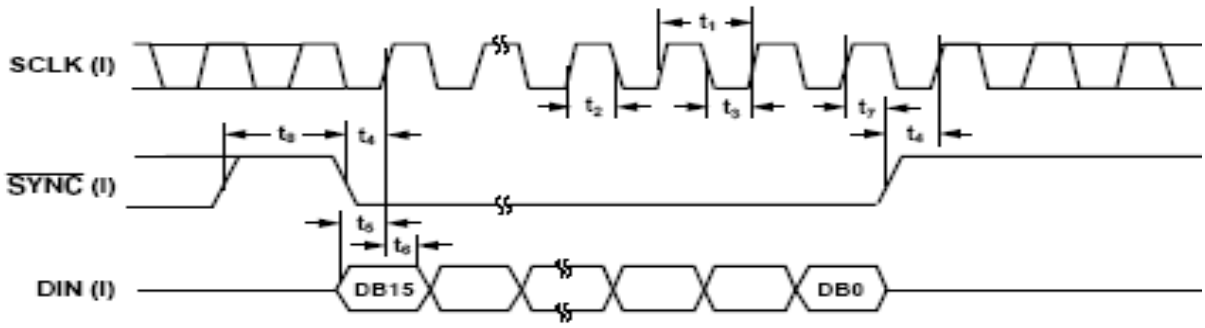


Figure 2 ***Timing Diagram of the AD7303 Chip on the PmodDA1***

The logic that created the timing sequence to take in the DATA1 and DATA2 input and shift out the data bits serially on outputs D1 and D2, as well as drive the nSYNC and DONE output signals, was designed by creating the finite state machine shown in Figure 3.

State Machine

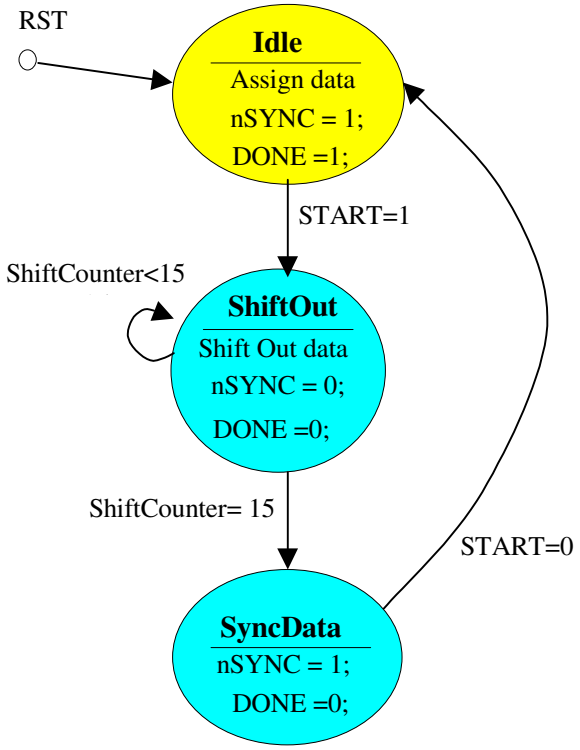


Figure 3 ***FSM of the PmodDA1 Reference Component***

There are three states: Idle, ShiftOut, and SyncData. During the Idle state, the 8-bit data vector is updated along with the 8-bit control register. The DONE output signal needs to be high in order to allow a conversion. When the START input signal activates during the Idle state, the state machine goes into the ShiftOut state.

In the ShiftOut state, the data bits are shifted out from MSB to LSB using a counter that counts 16 clock periods. It is this counter that ensures that all the data will be shifted out before moving on to the SyncData state.

When the counter reaches the value 15, the state machine goes into the SyncData state. In this state, the signal nSYNC is driven high to latch the data into the AD7303 chips on the PmodDA1.

If the START input signal is low, the machine goes back to the Idle state, ready to accept another conversion.

No mater what the current state is, the RST input signal resets the state machine and puts it in the Idle state.

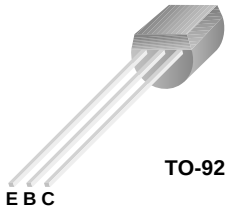
FAIRCHILD SEMICONDUCTOR®

February 2009

PN2222A/MMBT2222A/PZT2222A
NPN General Purpose Amplifier

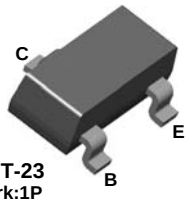
- This device is for use as a medium power amplifier and switch requiring collector currents up to 500mA.
- Sourced from process 19.

PN2222A



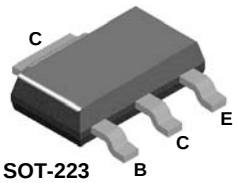
TO-92

MMBT2222A



SOT-23
Mark:1P

PZT2222A



SOT-223

Absolute Maximum Ratings * T_a = 25×C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	75	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current	1.0	A
T_{STG}	Operating and Storage Junction Temperature Range	- 55 ~ 150	°C

* This ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:

1) These rating are based on a maximum junction temperature of 150 degrees C.

2) These are steady limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics T_a = 25°C unless otherwise noted

Symbol	Parameter	Max.			Units
		PN2222A	*MMBT2222A	**PZT2222A	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

* Device mounted on FR-4 PCB 1.6” × 1.6” × 0.06”.

** Device mounted on FR-4 PCB 36mm × 18mm × 1.5mm; mounting pad for the collector lead min. $6cm^2$.

Electrical Characteristics T_a = 25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
Off Characteristics					
$BV_{(BR)CEO}$	Collector-Emitter Breakdown Voltage *	I_C = 10mA, I_B = 0	40		V
$BV_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10μA, I_E = 0	75		V
$BV_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10μA, I_C = 0	6.0		V
I_{CEX}	Collector Cutoff Current	V_{CE} = 60V, $V_{EB(off)}$ = 3.0V		10	nA
I_{CBO}	Collector Cutoff Current	V_{CB} = 60V, I_E = 0 V_{CB} = 60V, I_E = 0, T_a = 125°C		0.01 10	μA μA
I_{EBO}	Emitter Cutoff Current	V_{EB} = 3.0V, I_C = 0		10	nA
I_{BL}	Base Cutoff Current	V_{CE} = 60V, $V_{EB(off)}$ = 3.0V		20	nA
On Characteristics					
h_{FE}	DC Current Gain	I_C = 0.1mA, V_{CE} = 10V I_C = 1.0mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V, T_a = -55°C I_C = 150mA, V_{CE} = 10V * I_C = 150mA, V_{CE} = 10V * I_C = 500mA, V_{CE} = 10V *	35 50 75 35 100 50 40	300	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage *	I_C = 150mA, V_{CE} = 10V I_C = 500mA, V_{CE} = 10V		0.3 1.0	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage *	I_C = 150mA, V_{CE} = 10V I_C = 500mA, V_{CE} = 10V	0.6	1.2 2.0	V V
Small Signal Characteristics					
f_T	Current Gain Bandwidth Product	I_C = 20mA, V_{CE} = 20V, f = 100MHz	300		MHz
C_{obo}	Output Capacitance	V_{CB} = 10V, I_E = 0, f = 1MHz		8.0	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5V, I_C = 0, f = 1MHz		25	pF
$rb'C_c$	Collector Base Time Constant	I_C = 20mA, V_{CB} = 20V, f = 31.8MHz		150	pS
NF	Noise Figure	I_C = 100μA, V_{CE} = 10V, R_S = 1.0KΩ, f = 1.0KHz		4.0	dB
$Re(h_{ie})$	Real Part of Common-Emitter High Frequency Input Impedance	I_C = 20mA, V_{CE} = 20V, f = 300MHz		60	Ω
Switching Characteristics					
t_d	Delay Time	V_{CC} = 30V, $V_{EB(off)}$ = 0.5V, I_C = 150mA, I_{B1} = 15mA		10	ns
t_r	Rise Time			25	ns
t_s	Storage Time	V_{CC} = 30V, I_C = 150mA, I_{B1} = I_{B2} = 15mA		225	ns
t_f	Fall Time			60	ns

* Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%

Typical Characteristics

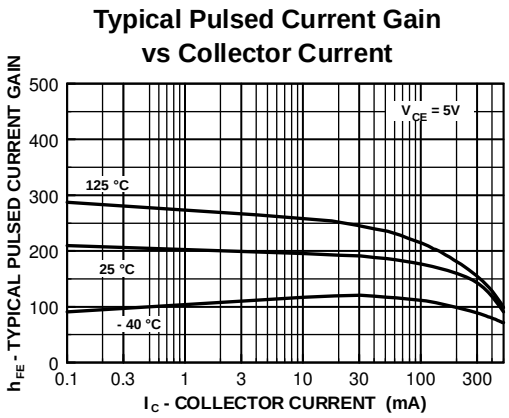


Figure 1. Typical Pulsed Current Gain vs Collector Current

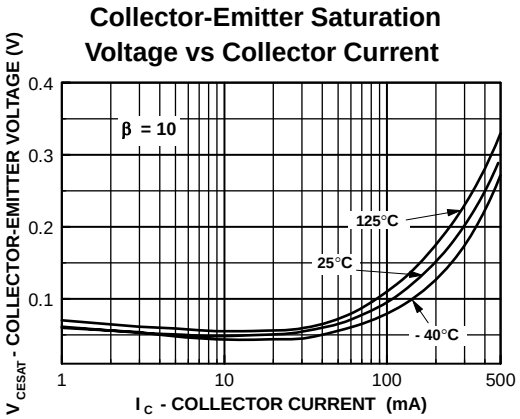


Figure 2. Collector-Emitter Saturation Voltage vs Collector Current

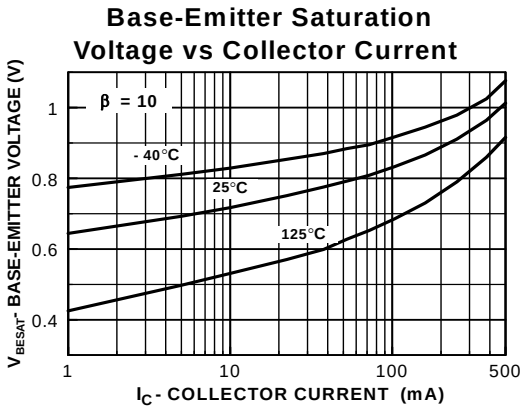


Figure 3. Base-Emitter Saturation Voltage vs Collector Current

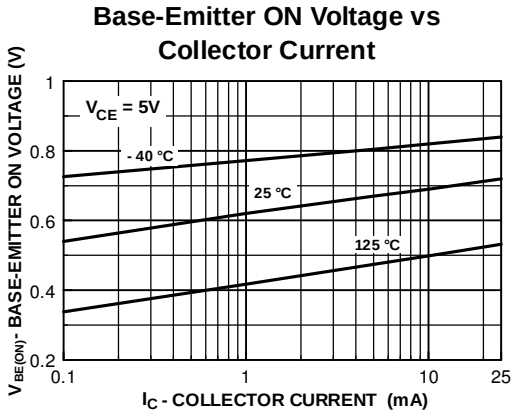


Figure 4. Base-Emitter On Voltage vs Collector Current

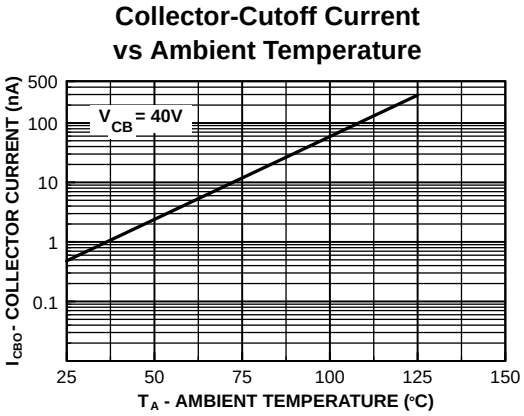


Figure 5. Collector Cutoff Current vs Ambient Temperature

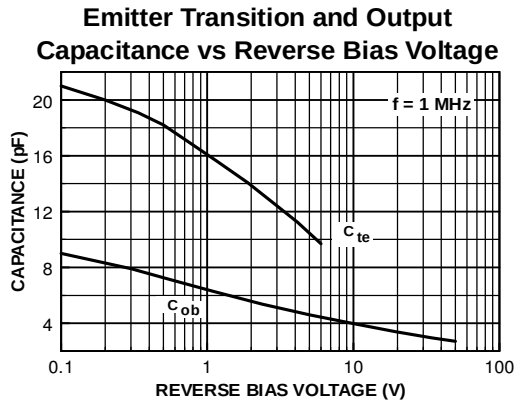


Figure 6. Emitter Transition and Output Capacitance vs Reverse Bias Voltage

Typical Characteristics

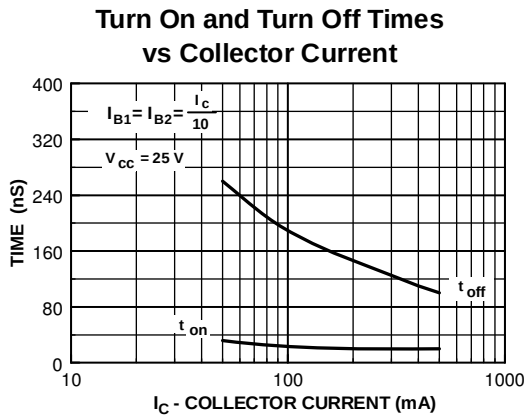


Figure 1. Turn On and Turn Off Times vs Collector Current

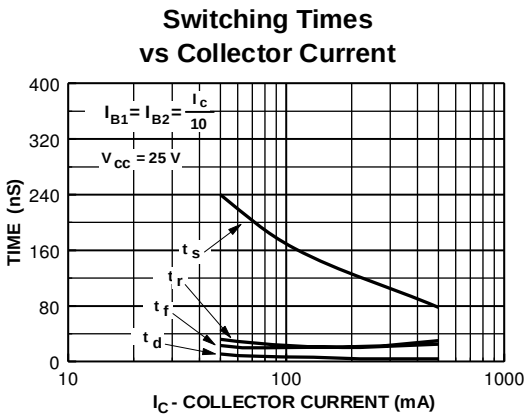


Figure 2. Switching Times vs Collector Current

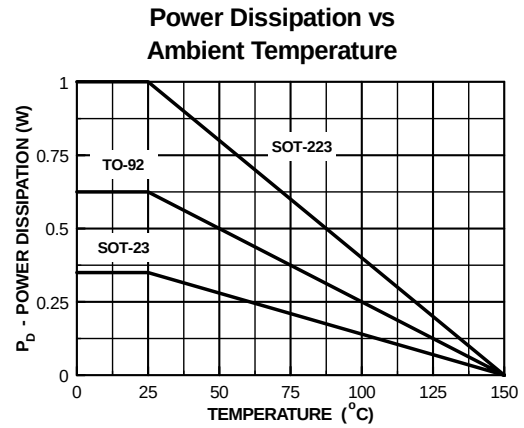


Figure 3. Power Dissipation vs Ambient Temperature

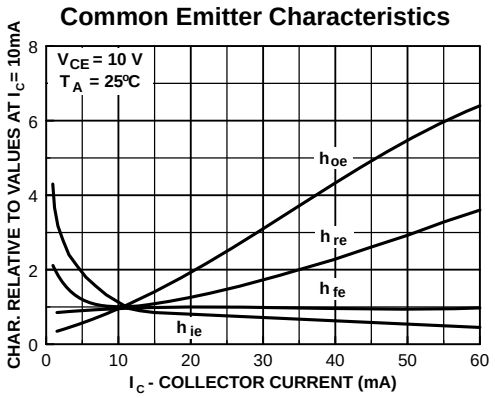


Figure 4. Common Emitter Characteristics

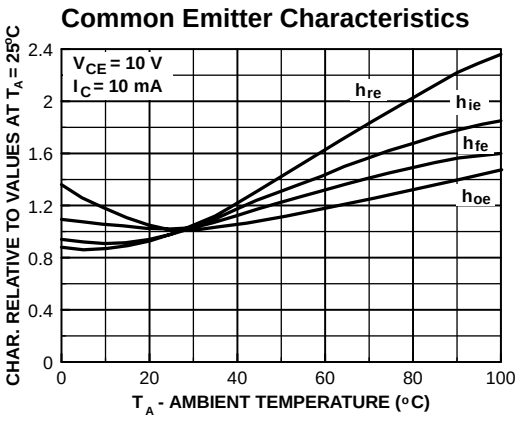


Figure 5. Common Emitter Characteristics

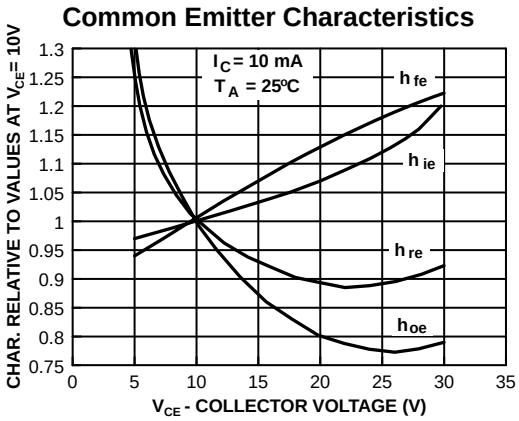


Figure 6. Common Emitter Characteristics

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CROSSVOLT™	*i-Lo*™	PowerTrench®	the power franchise
CTL™	IntelliMAX™	Programmable Active Droop™	
Current Transfer Logic™	ISOPLANAR™	QFET®	TinyBoost™
EcoSPARK®	MegaBuck™	QS™	TinyBuck™
	MICROCOUPLER™	QT Optoelectronics™	TinyLogic®
Fairchild®	MicroFET™	Quiet Series™	TINYOPTO™
Fairchild Semiconductor®	MicroPak™	RapidConfigure™	TinyPower™
FACT Quiet Series™	MillerDrive™	SMART START™	TinyPWM™
FACT®	Motion-SPM™	SPM®	TinyWire™
FAST®	OPTOLOGIC®	STEALTH™	µSerDes™
FastvCore™	OPTOPLANAR®	SuperFET™	UHC®
FPS™	®	SuperSOT™-3	UniFET™
FRFET®	PDP-SPM™	SuperSOT™-6	VCX™
Global Power Resource℠	Power220®		

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I31

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **High Input Impedance . . . JFET-Input Stage**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

description/ordering information

The TL08x JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The Q-suffix devices are characterized for operation from −40°C to 125°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

ORDERING INFORMATION

T_J	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	15 mV	PDIP (P)	Tube of 50	TL081CP	TL081CP
			Tube of 50	TL082CP	TL082CP
		PDIP (N)	Tube of 25	TL084CN	TL084CN
		SOIC (D)	Tube of 75	TL081CD	TL081C
			Reel of 2500	TL081CDR	
			Tube of 75	TL082CD	TL082C
			Reel of 2500	TL082CDR	
			Tube of 50	TL084CD	TL084C
			Reel of 2500	TL084CDR	
		SOP (PS)	Reel of 2000	TL081CPSR	T081
			Reel of 2000	TL082CPSR	T082
		SOP (NS)	Reel of 2000	TL084CNSR	TL084
		TSSOP (PW)	Tube of 150	TL082CPW	T082
			Reel of 2000	TL082CPWR	
			Tube of 90	TL084CPW	T084
			Reel of 2000	TL084CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

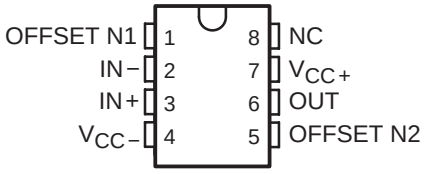
description/ordering information (continued)

ORDERING INFORMATION

T_J	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	6 mV	PDIP (P)	Tube of 50	TL081ACP	TL081ACP
			Tube of 50	TL082ACP	TL082ACP
		PDIP (N)	Tube of 25	TL084ACN	TL084ACN
		SOIC (D)	Tube of 75	TL081ACD	081AC
			Reel of 2500	TL081ACDR	
			Tube of 75	TL082ACD	082AC
			Reel of 2500	TL082ACDR	
			Tube of 50	TL084ACD	TL084AC
			Reel of 2500	TL084ACDR	
		SOP (PS)	Reel of 2000	TL082ACPSR	T082A
		SOP (NS)	Reel of 2000	TL084ACNSR	TL084A
	3 mV	PDIP (P)	Tube of 50	TL081BCP	TL081BCP
			Tube of 50	TL082BCP	TL082BCP
		PDIP (N)	Tube of 25	TL084BCN	TL084BCN
		SOIC (D)	Tube of 75	TL081BCD	081BC
			Reel of 2500	TL081BCDR	
			Tube of 75	TL082BCD	082BC
			Reel of 2500	TL082BCDR	
			Tube of 50	TL084BCD	TL084BC
			Reel of 2500	TL084BCDR	
−40°C to 85°C	6 mV	PDIP (P)	Tube of 50	TL081IP	TL081IP
			Tube of 50	TL082IP	TL082IP
		PDIP (N)	Tube of 25	TL084IN	TL081IN
		SOIC (D)	Tube of 75	TL081ID	TL081I
			Reel of 2500	TL081IDR	
			Tube of 75	TL082ID	TL082I
			Reel of 2500	TL082IDR	
			Tube of 50	TL084ID	TL084I
			Reel of 2500	TL084IDR	
		TSSOP (PW)	Reel of 2000	TL082IPWR	Z082
−40°C to 125°C	9 mV	SOIC (D)	Tube of 50	TL084QD	TL084QD
			Reel of 2500	TL084QDR	
−55°C to 125°C	9 mV	CDIP (J)	Tube of 25	TL084MJ	TL084MJ
		LCCC (FK)	Reel of 55	TL084FK	TL084FK
	6 mV	CDIP (JG)	Tube of 50	TL082MJG	TL082MJG
		LCCC (FK)	Tube of 55	TL082MFK	TL082MFK

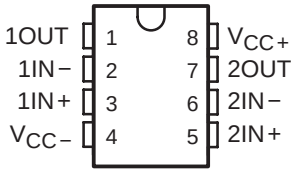
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

TL081, TL081A, TL081B
D, P, OR PS PACKAGE
(TOP VIEW)

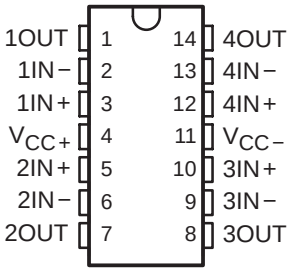


NC − No internal connection

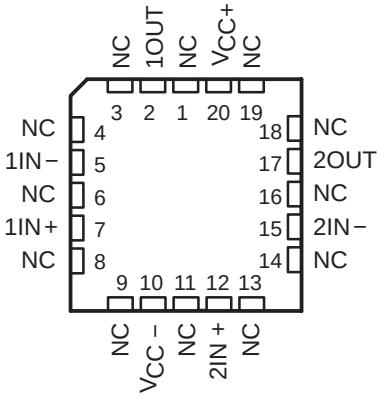
TL082, TL082A, TL082B
D, JG, P, PS, OR PW PACKAGE
(TOP VIEW)



TL084, TL084A, TL084B
D, J, N, NS, OR PW PACKAGE
(TOP VIEW)

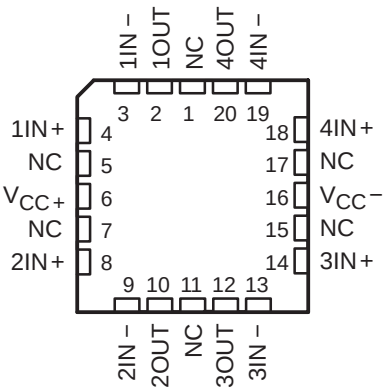


TL082M . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

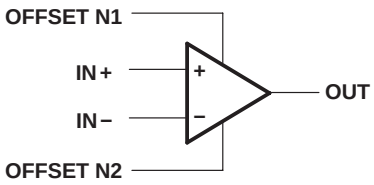
TL084M . . . FK PACKAGE
(TOP VIEW)



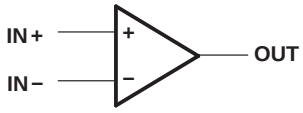
NC − No internal connection

symbols

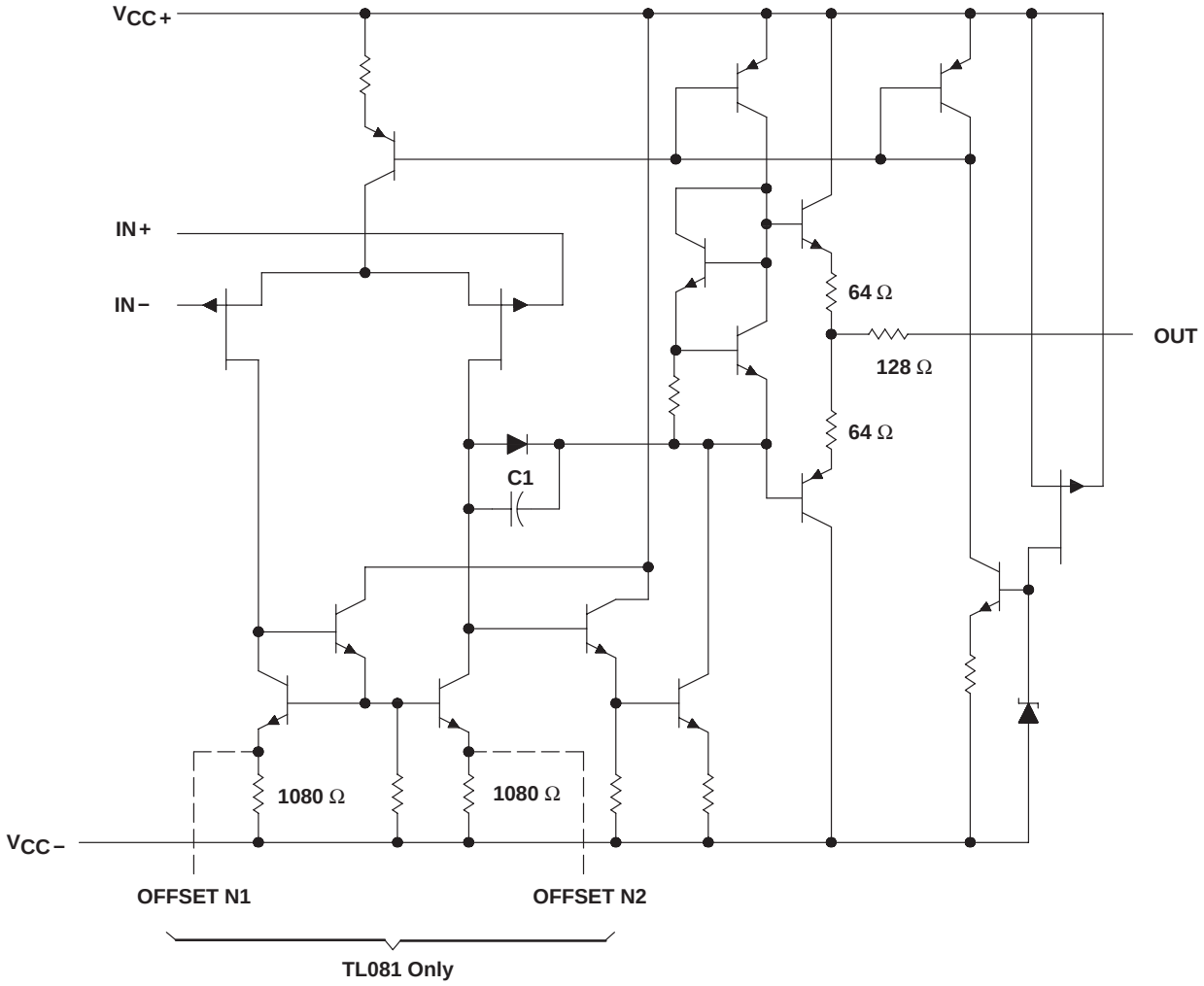
TL081



TL082 (EACH AMPLIFIER)
TL084 (EACH AMPLIFIER)



schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		TL08_C TL08_AC TL08_BC	TL08_I	TL084Q	TL08_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	−18	−18	V
Differential input voltage, V_{ID} (see Note 2)		±30	±30	±30	±30	V
Input voltage, V_I (see Notes 1 and 3)		±15	±15	±15	±15	V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	Unlimited	
Continuous total power dissipation		See Dissipation Rating Table				
Operating free-air temperature range, T_A		0 to 70	− 40 to 85	− 40 to 125	− 55 to 125	°C
Package thermal impedance, θ_{JA} (see Notes 5 and 6)	D package (8-pin)	97	97			°C/W
	D package (14-pin)	86	86			
	N package (14-pin)	76	76			
	NS package (14-pin)	80				
	P package (8-pin)	85	85			
	PS package (8-pin)	95	95			
	PW package (8-pin)	149				
	PW package (14-pin)	113	113			
Operating virtual junction temperature		150	150	150	150	°C
Case temperature for 60 seconds, T_C	FK package				260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or JG package				300	°C
Storage temperature range, T_{stg}		− 65 to 150	− 65 to 150	− 65 to 150	− 65 to 150	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TL081C, TL082C, TL084C			TL081AC, TL082AC, TL084AC			TLO81BC, TL082BC, TL084BC			TL081I, TL082I, TL084I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	R_S = 50 Ω	25°C		3	15		3	6		2	3		3	6	mV
				Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0	R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current‡	V_O = 0		25°C		5	200		5	100		5	100		5	100	pA
				Full range			2			2			2			10	nA
I_{IB}	Input bias current‡	V_O = 0		25°C		30	400		30	200		30	200		30	200	pA
				Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range			25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ		Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ			±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
		V_O = ±10 V,	R_L ≥ 2 kΩ	Full range	15			25			25			25			
B_1	Unity-gain bandwidth			25°C		3			3			3			3		MHz
r_i	Input resistance			25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0,	R_S = 50 Ω	25°C	70	86		75	86		75	86		75	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ± 9 V, V_O = 0,	R_S = 50 Ω	25°C	70	86		80	86		80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	V_O = 0,	No load	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and –40°C to 85°C for TL08_I.

‡ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TL081M, TL082M			TL084Q, TL084M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0 R_S = 50 Ω	Full range		18			18		μV/°C
I_{IO}	Input offset current‡	V_O = 0	25°C		5	100		5	100	pA
			125°C			20			20	nA
I_{IB}	Input bias current‡	V_O = 0	25°C		30	200		30	200	pA
			125°C			50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		25	200		V/mV
		V_O = ±10 V, R_L ≥ 2 kΩ	Full range	15			15			
B_1	Unity-gain bandwidth		25°C		3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

† All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 17. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V,	R_L = 2 kΩ,	C_L = 100 pF,	See Figure 1	8*	13		V/μs
		V_I = 10 V, T_A = − 55°C to 125°C,	R_L = 2 kΩ, See Figure 1	C_L = 100 pF,		5*			
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,	C_L = 100 pF,	See Figure 1		0.05		μs
	Overshoot factor						20		%
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz				18		nV/√Hz
			f = 10 Hz to 10 kHz				4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz				0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, f = 1 kHz	A_{VD} = 1,	R_S ≤ 1 kΩ,	R_L ≥ 2 kΩ,		0.003		%

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V,	R_L = 2 kΩ,	C_L = 100 pF,	See Figure 1	8	13		V/μs
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,	C_L = 100 pF,	See Figure 1		0.05		μs
	Overshoot factor						20		%
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz				18		nV/√Hz
			f = 10 Hz to 10 kHz				4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz				0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, f = 1 kHz	A_{VD} = 1,	R_S ≤ 1 kΩ,	R_L ≥ 2 kΩ,		0.003		%

PARAMETER MEASUREMENT INFORMATION

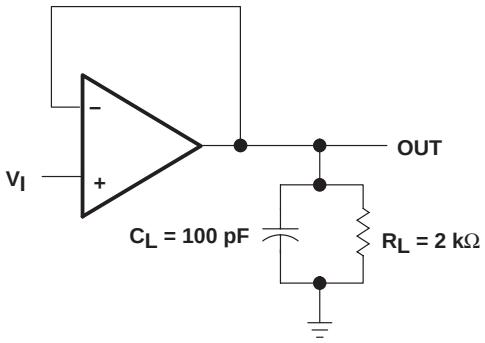


Figure 1

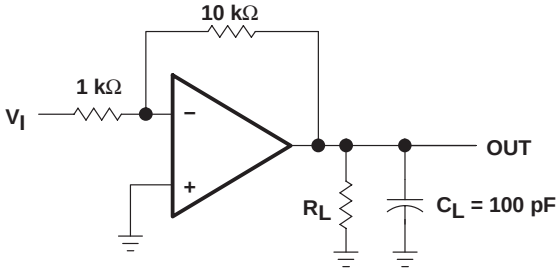


Figure 2

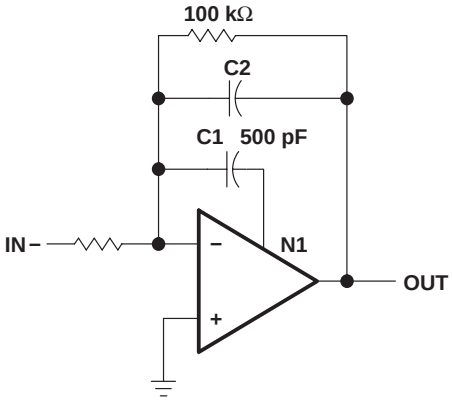


Figure 3

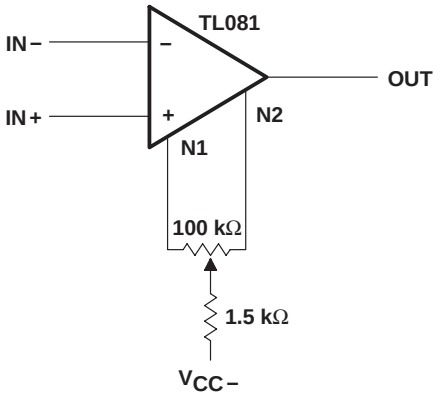


Figure 4

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OM}	Maximum peak output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Differential voltage amplification	vs Frequency with feed-forward compensation	13
P_D	Total power dissipation	vs Free-air temperature	14
I_{CC}	Supply current	vs Free-air temperature vs Supply voltage	15 16
I_{IB}	Input bias current	vs Free-air temperature	17
	Large-signal pulse response	vs Time	18
V_O	Output voltage	vs Elapsed time	19
CMRR	Common-mode rejection ratio	vs Free-air temperature	20
V_n	Equivalent input noise voltage	vs Frequency	21
THD	Total harmonic distortion	vs Frequency	22

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

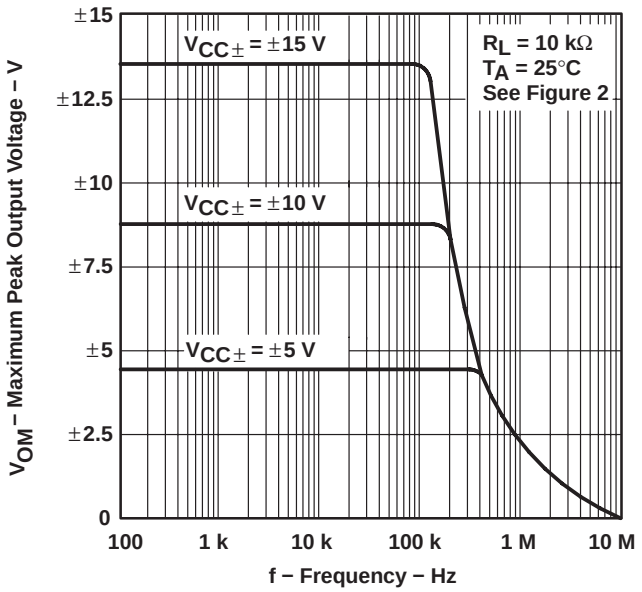


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

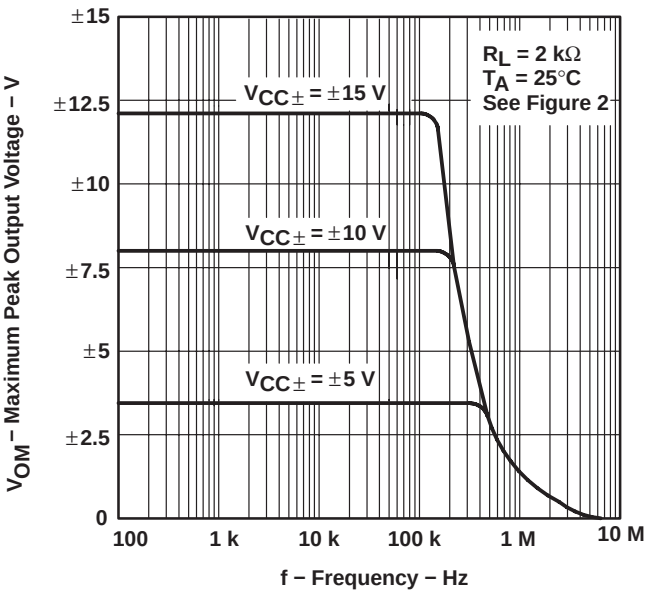


Figure 6

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

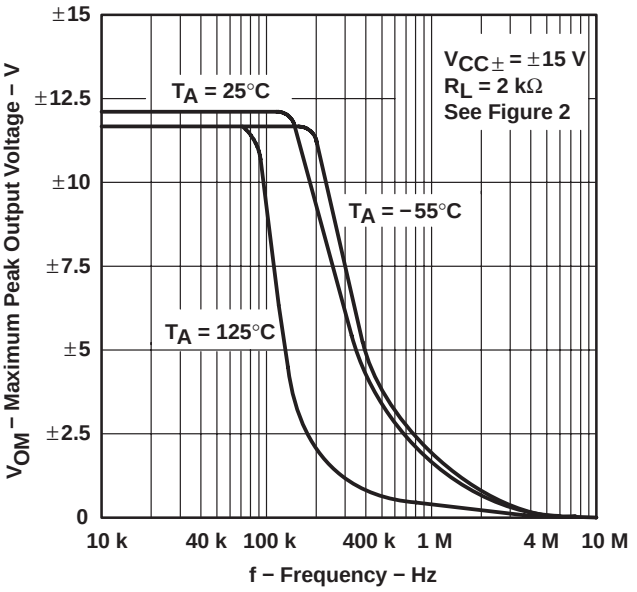


Figure 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

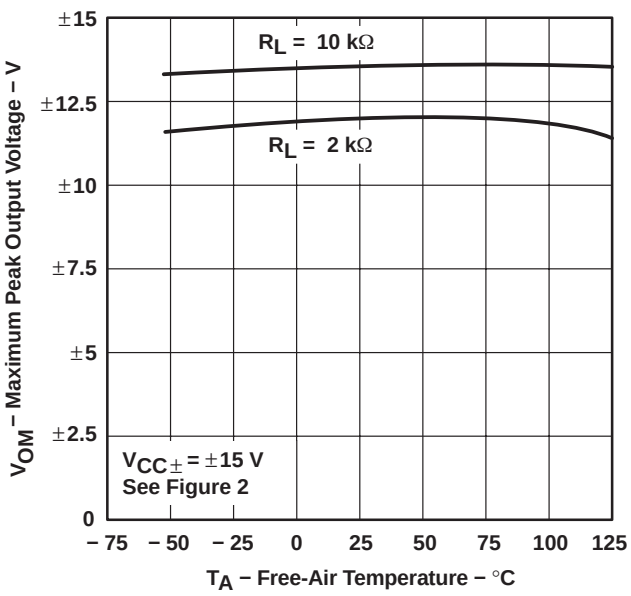


Figure 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

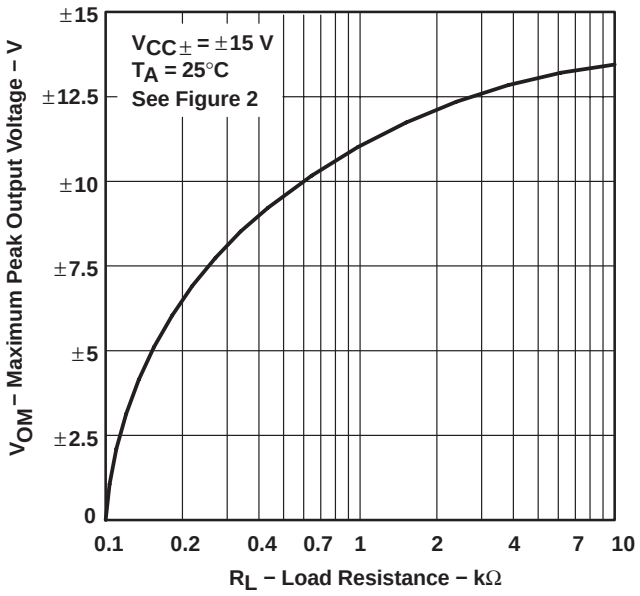


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

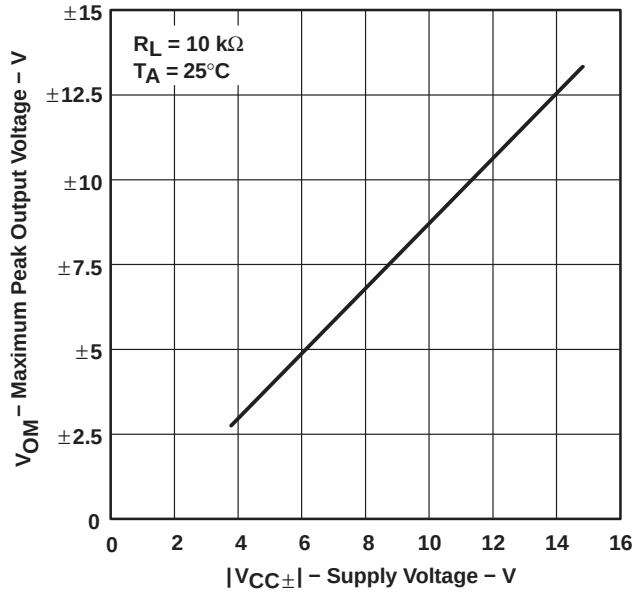


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

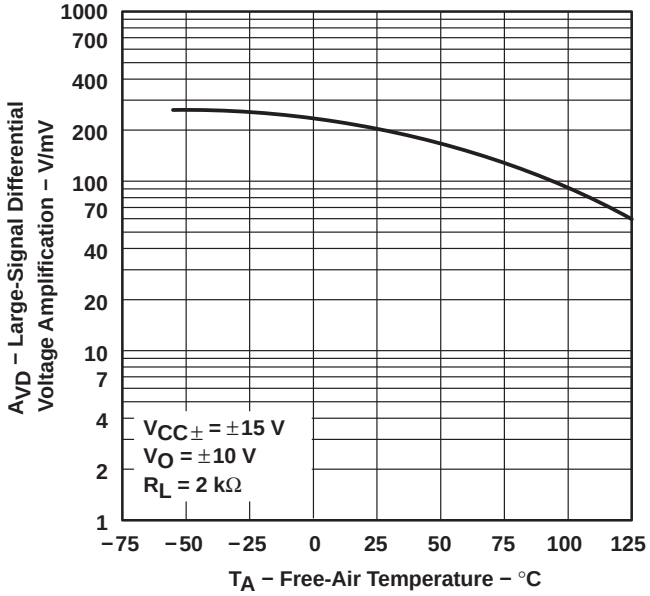


Figure 11

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

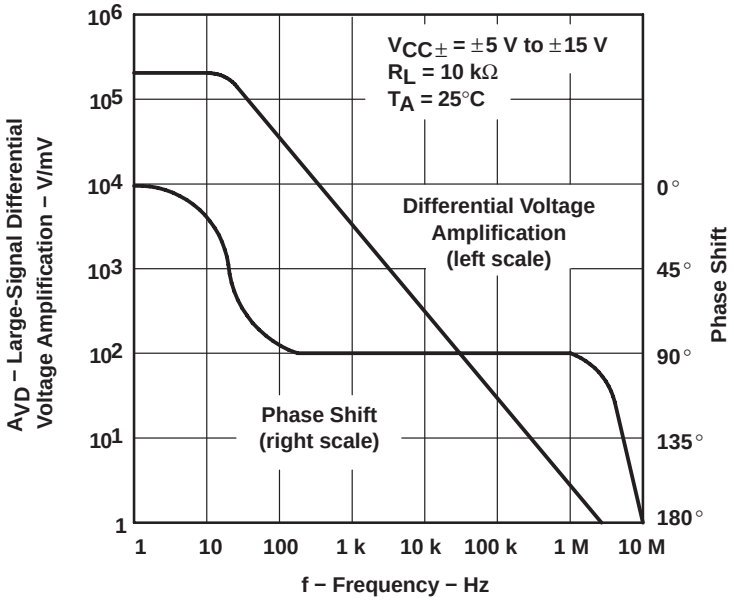


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY WITH FEED-FORWARD COMPENSATION

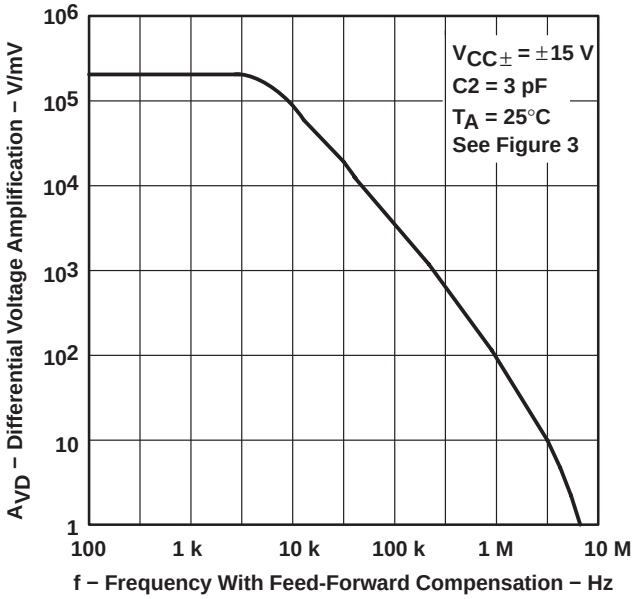


Figure 13

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

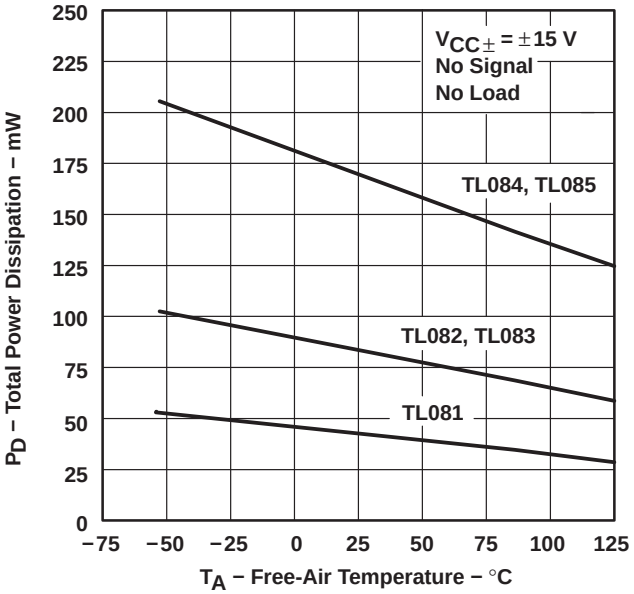


Figure 14

SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

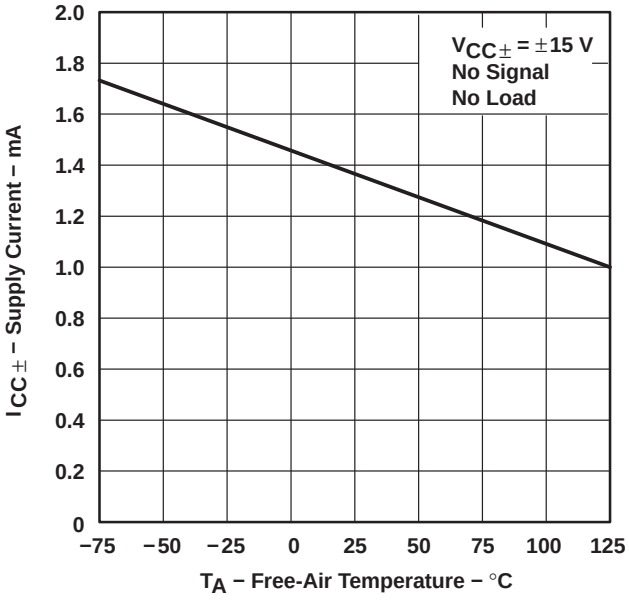


Figure 15

SUPPLY CURRENT vs SUPPLY VOLTAGE

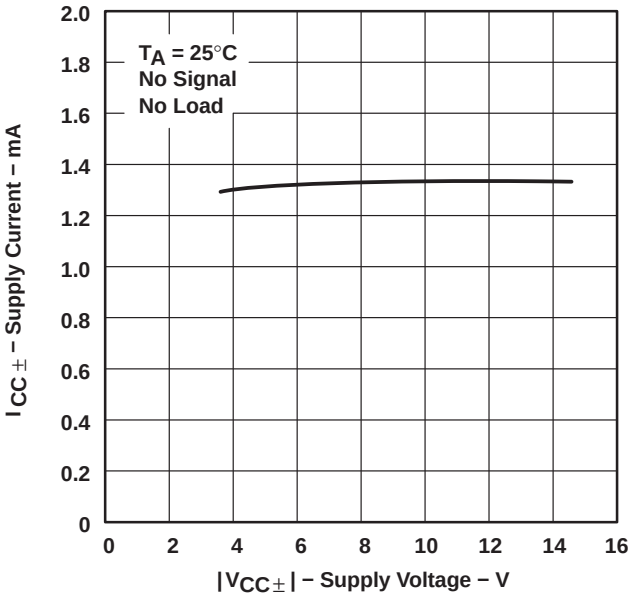


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

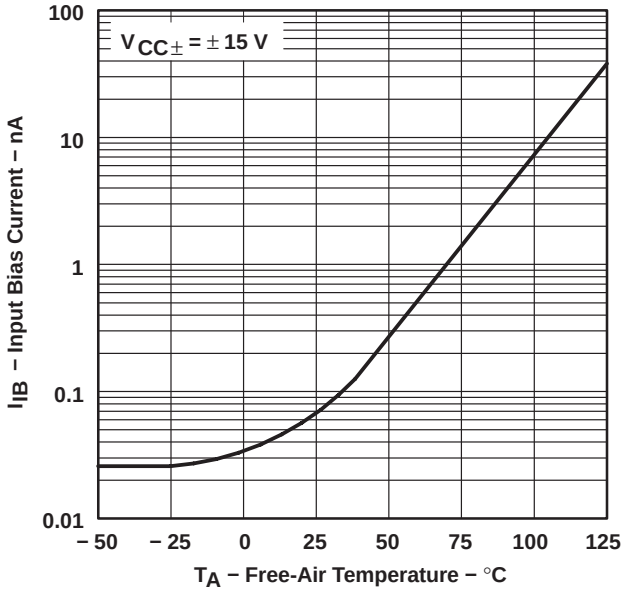


Figure 17

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

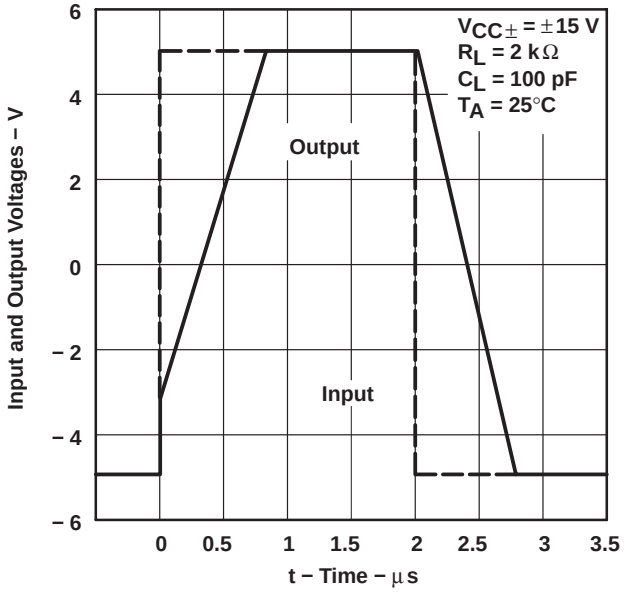


Figure 18

OUTPUT VOLTAGE vs ELAPSED TIME

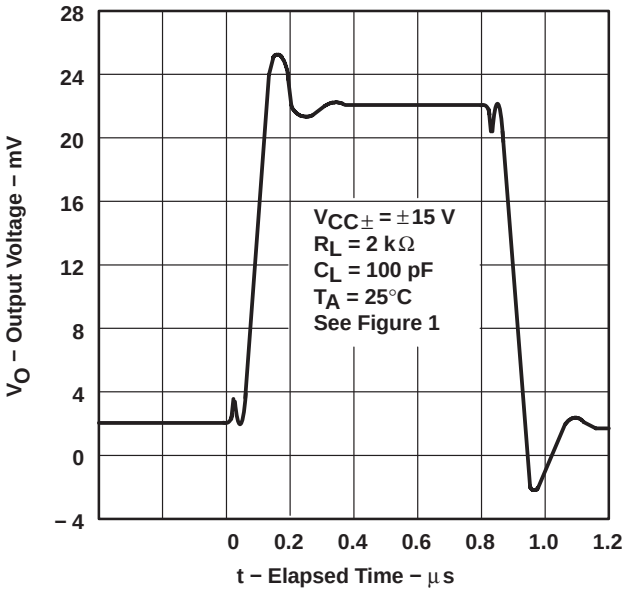


Figure 19

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

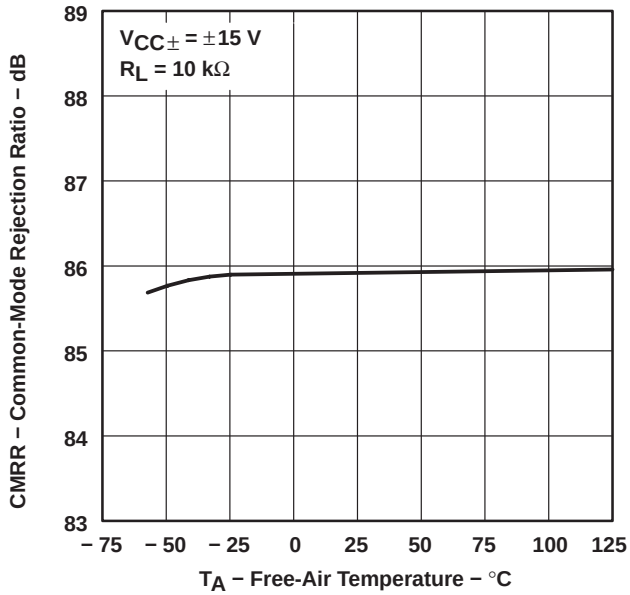


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

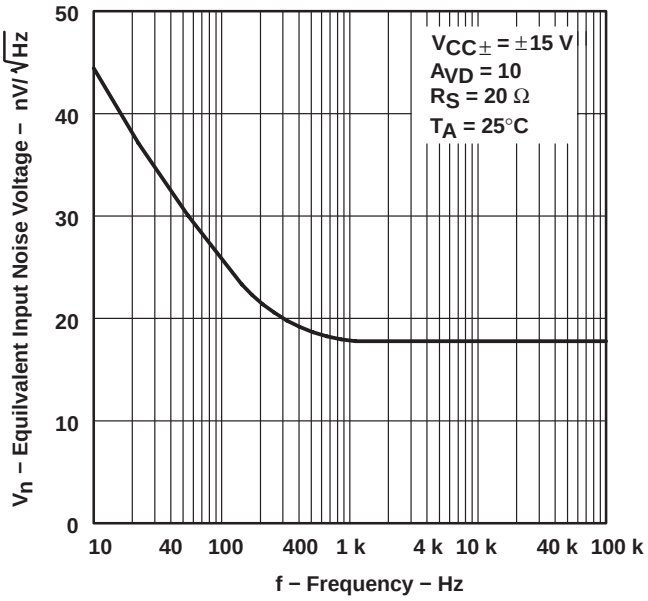


Figure 21

TOTAL HARMONIC DISTORTION vs FREQUENCY

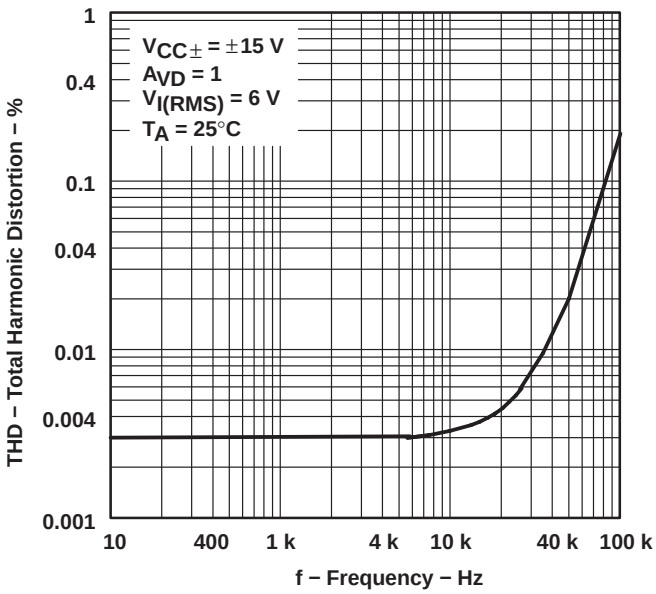


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

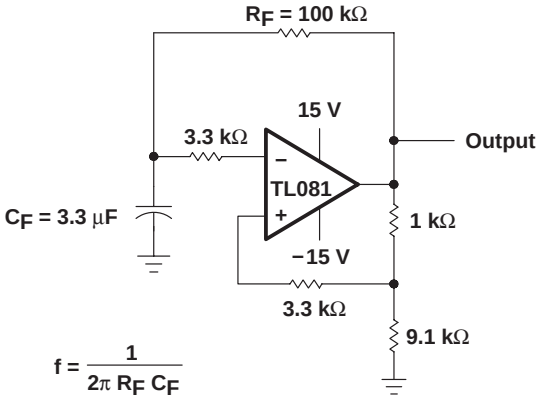


Figure 23

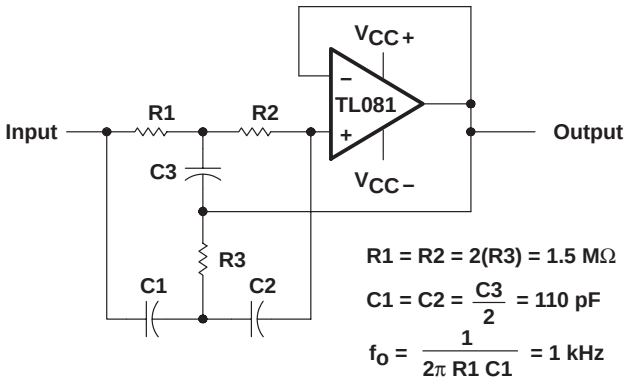


Figure 24

APPLICATION INFORMATION

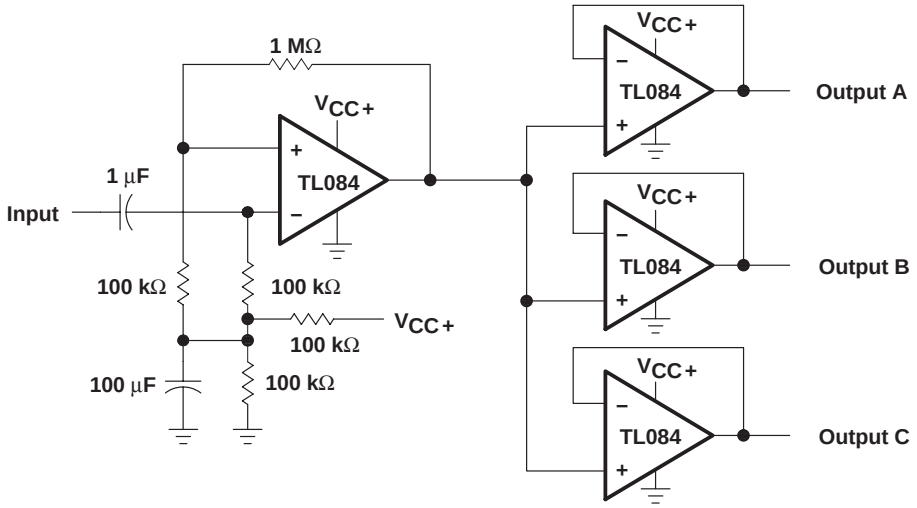
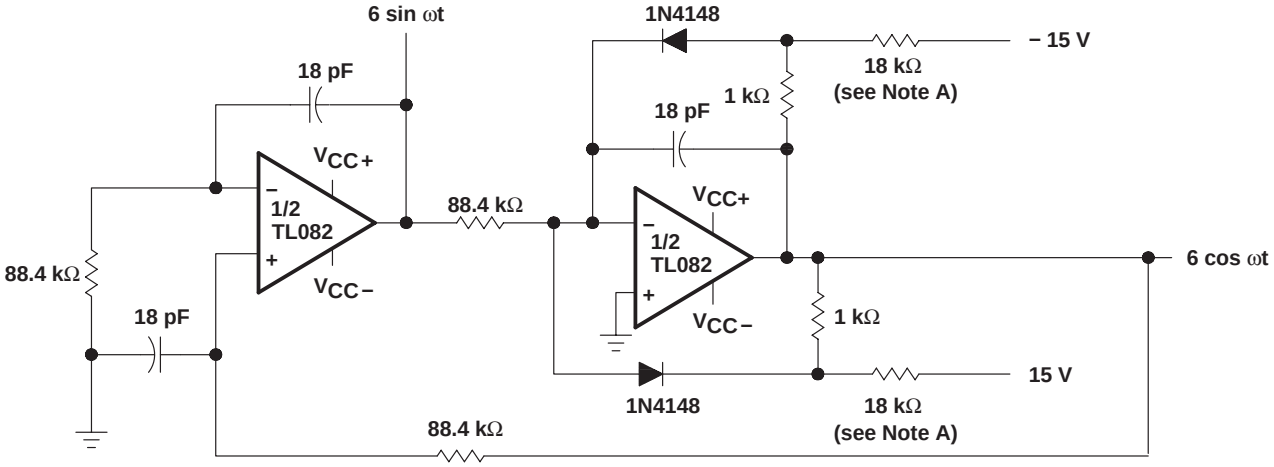


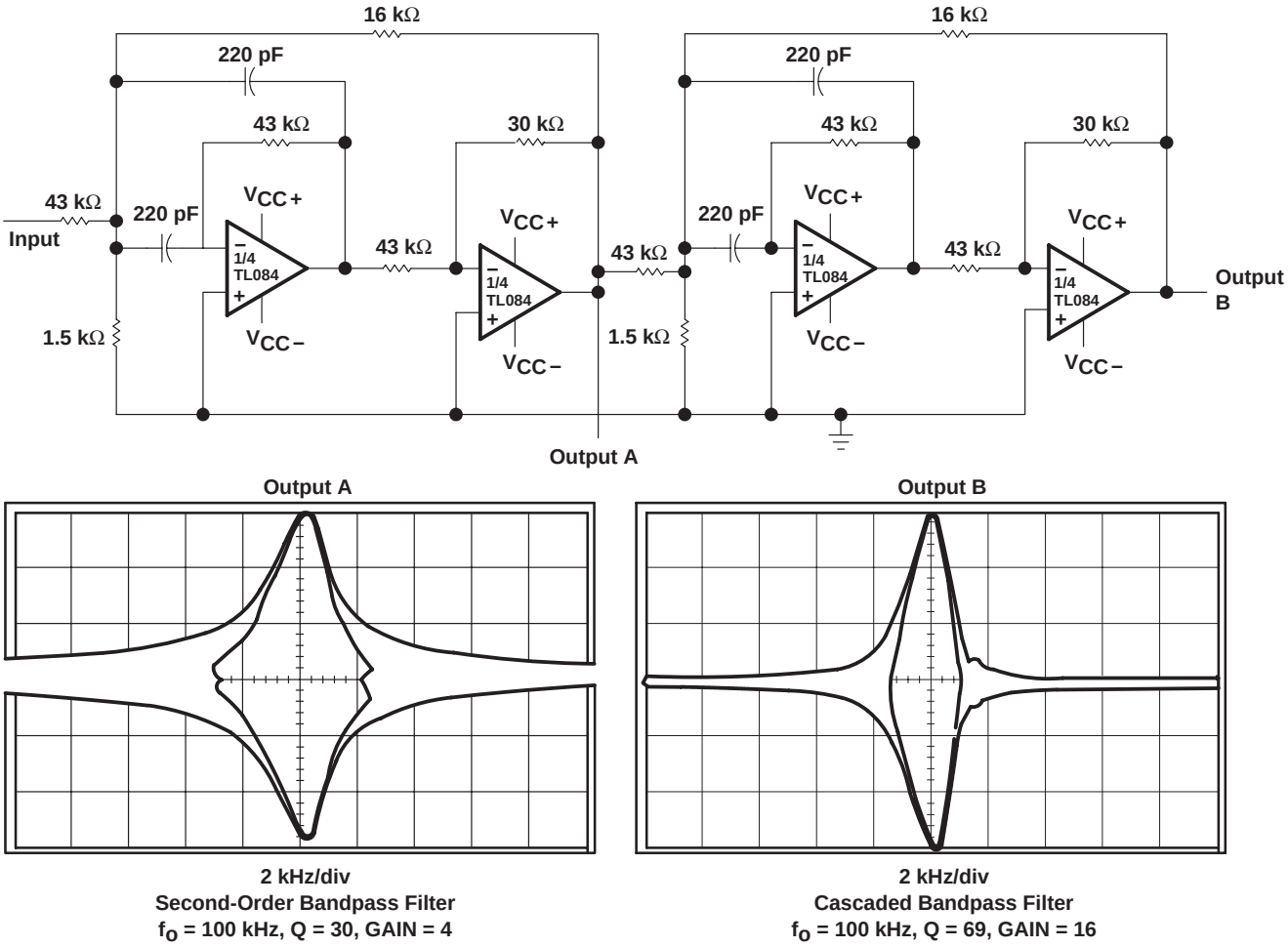
Figure 25. Audio-Distribution Amplifier



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-KHz Quadrature Oscillator

APPLICATION INFORMATION



Output A

2 kHz/div
Second-Order Bandpass Filter
f_O = 100 kHz, Q = 30, GAIN = 4

Output B

2 kHz/div
Cascaded Bandpass Filter
f_O = 100 kHz, Q = 69, GAIN = 16

Figure 27. Positive-Feedback Bandpass Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9851501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9851501QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
5962-9851503Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9851503QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
TL081ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081ACJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL081ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL081ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL081BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL081BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL081CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL081CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL081CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL081CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TL081ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL081IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL081IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL081MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
TL081MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL081MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL082ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL082ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL082ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082ACPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082ACPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
TL082BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL082BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL082CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL082CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL082CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL082CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TL082CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL082ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082IJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL082IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL082IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL082IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082MFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
TL082MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TL082MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
TL082MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
TL084ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084ACDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL084ACNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL084ACNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084ACNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084ACNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL084BCDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084BCDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084BCDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084BCDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL084BCNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL084CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL084CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL084CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL084CNSLE	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI
TL084CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
TL084CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL084IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084IJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL084IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL084INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL084MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TL084MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TL084MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
TL084MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
TL084QD	ACTIVE	SOIC	D	14	50	TBD	CU NIPDAU	Level-1-220C-UNLIM
TL084QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084QDR	ACTIVE	SOIC	D	14	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
TL084QDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL082, TL082M, TL084, TL084M :

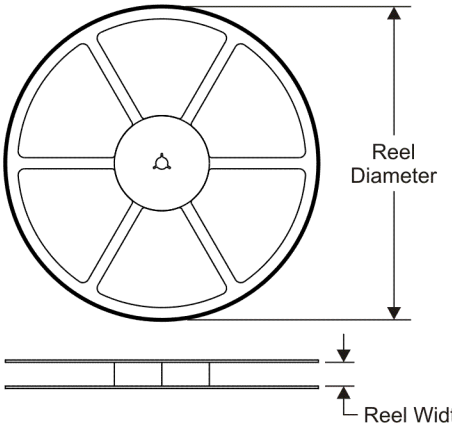
- Automotive: TL082-Q1

NOTE: Qualified Version Definitions:

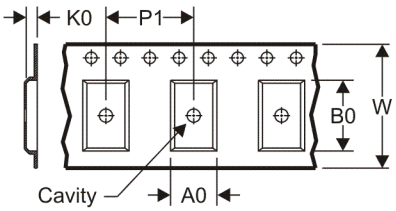
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

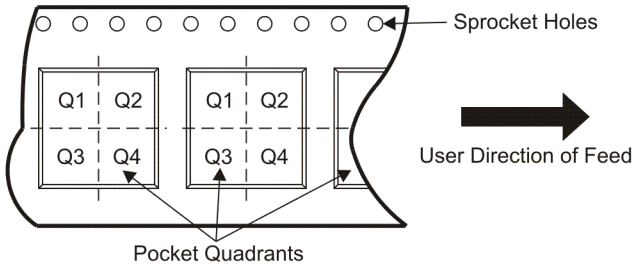


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

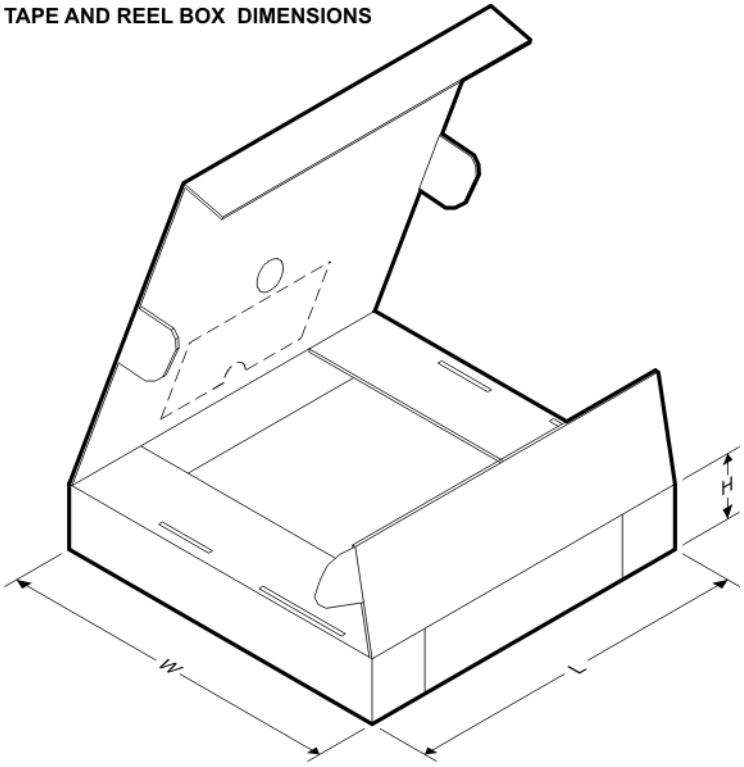


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL081ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL081IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL082BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL082CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL084ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL084BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

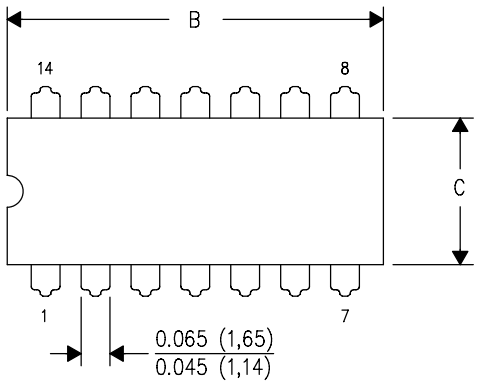
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL081ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CPSR	SO	PS	8	2000	346.0	346.0	33.0
TL081IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACDR	SOIC	D	8	2500	346.0	346.0	29.0
TL082ACPSR	SO	PS	8	2000	346.0	346.0	33.0
TL082BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082CDR	SOIC	D	8	2500	346.0	346.0	29.0
TL082CDR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082CPSR	SO	PS	8	2000	346.0	346.0	33.0
TL082CPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TL082IDR	SOIC	D	8	2500	346.0	346.0	29.0
TL082IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082IPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TL084ACDR	SOIC	D	14	2500	346.0	346.0	33.0
TL084ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084ACNSR	SO	NS	14	2000	346.0	346.0	33.0
TL084BCDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CNSR	SO	NS	14	2000	346.0	346.0	33.0
TL084CPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
TL084IDR	SOIC	D	14	2500	333.2	345.9	28.6

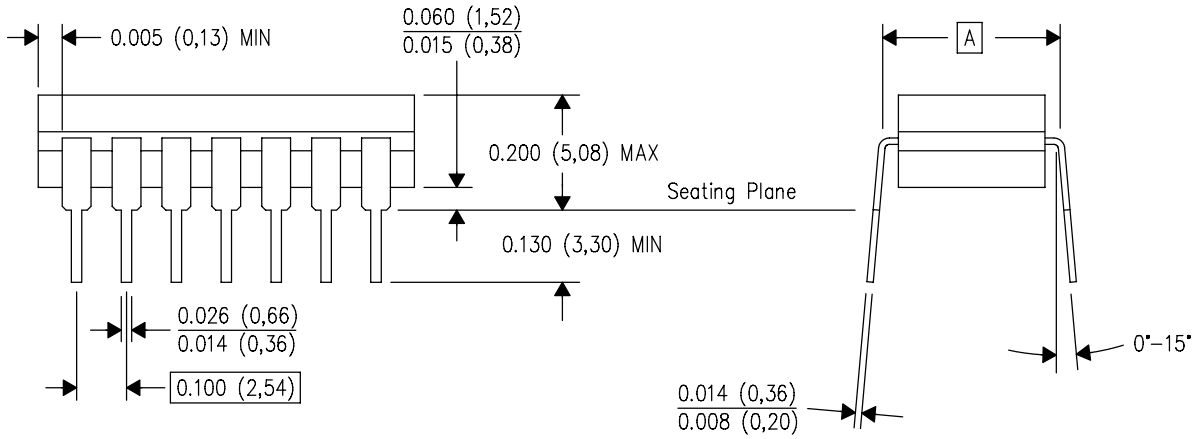
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



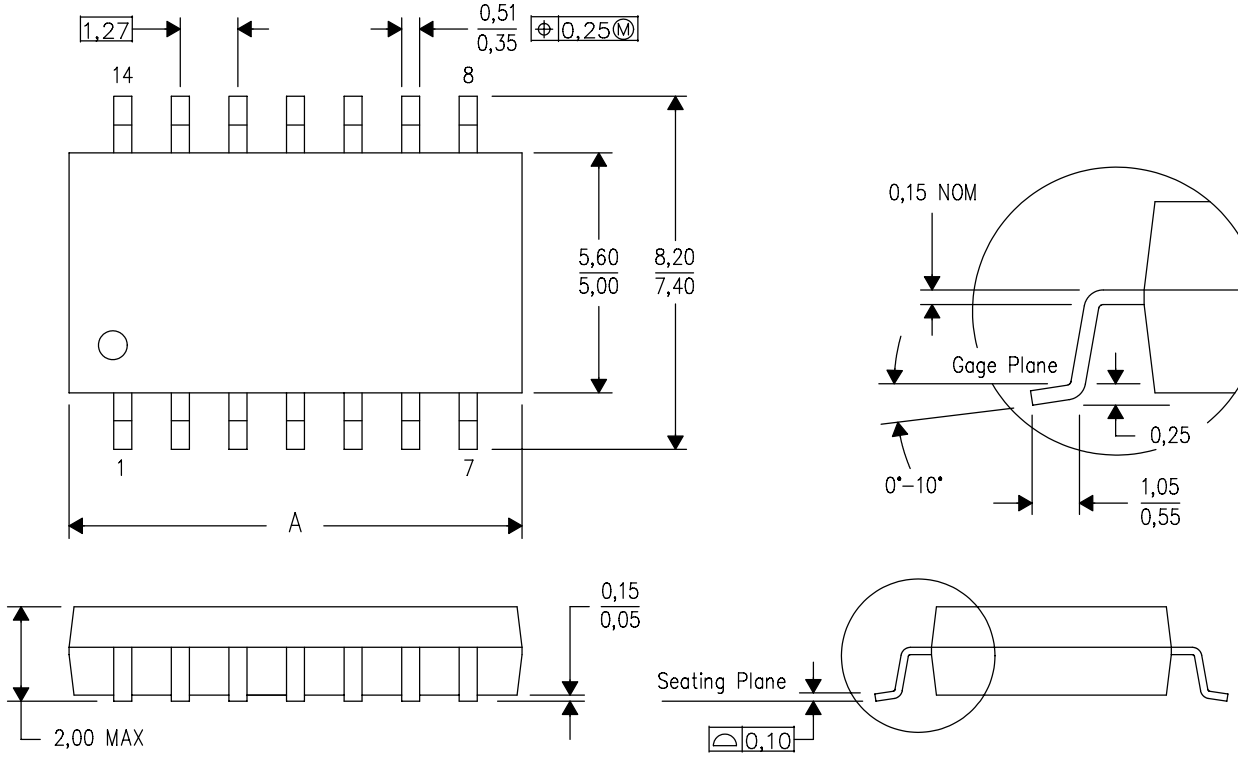
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



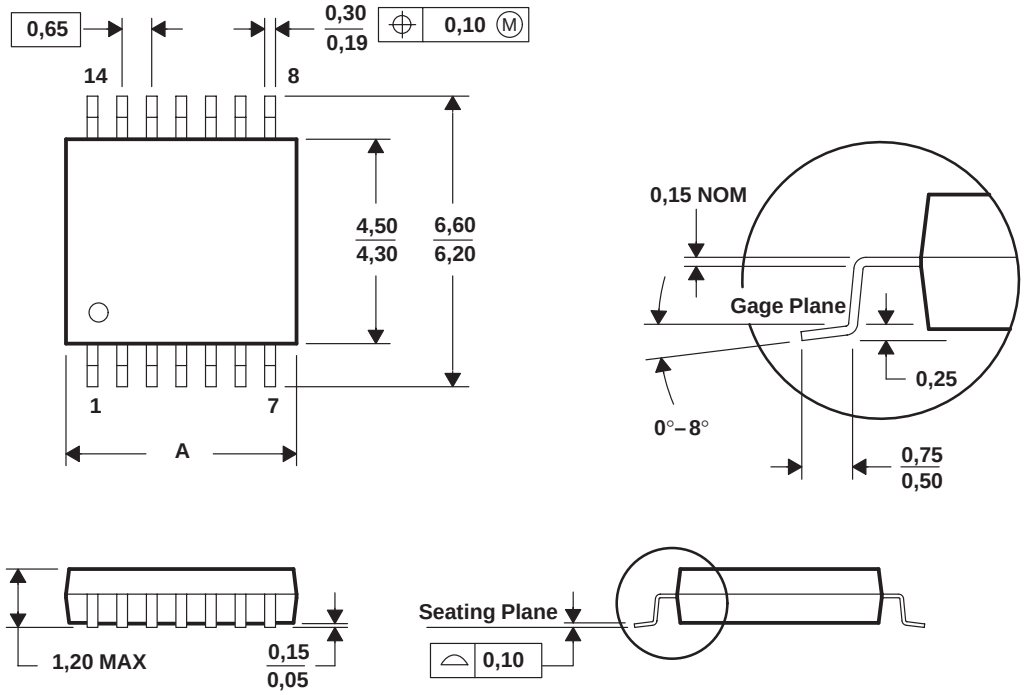
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



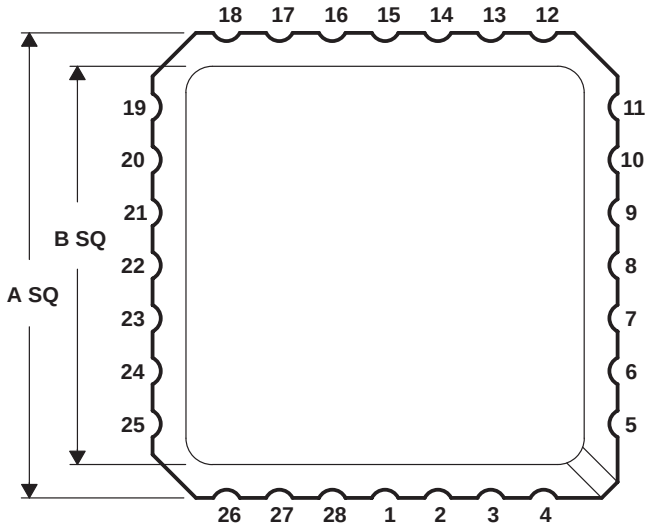
DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

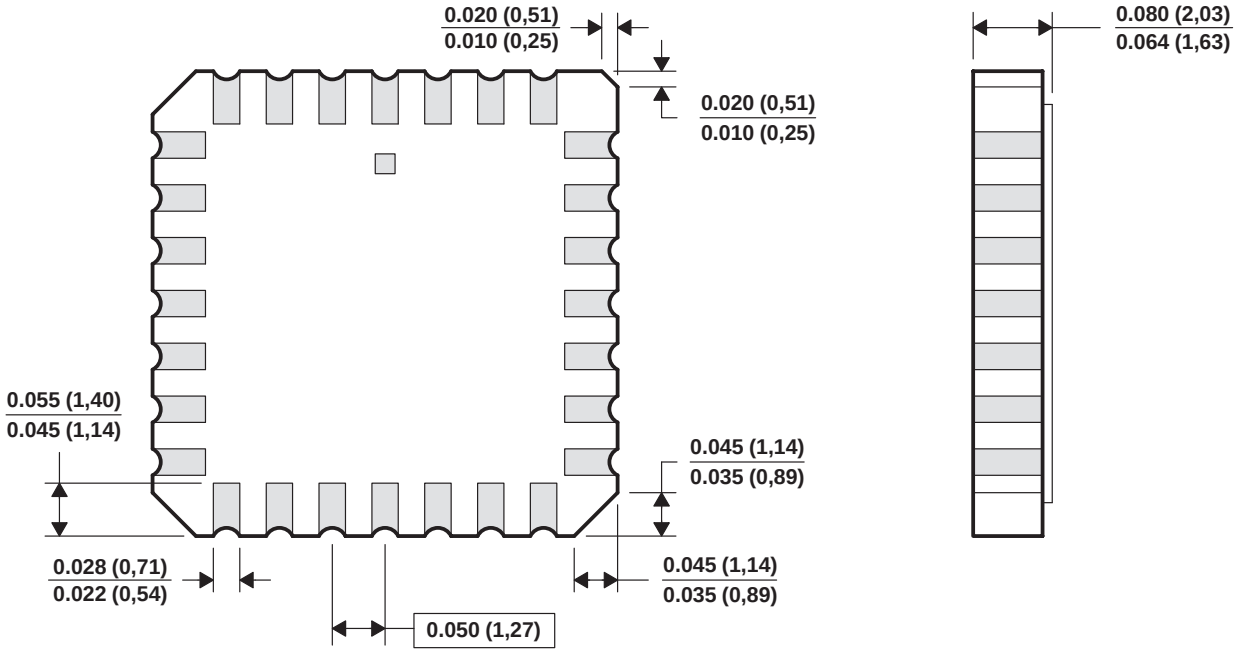
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

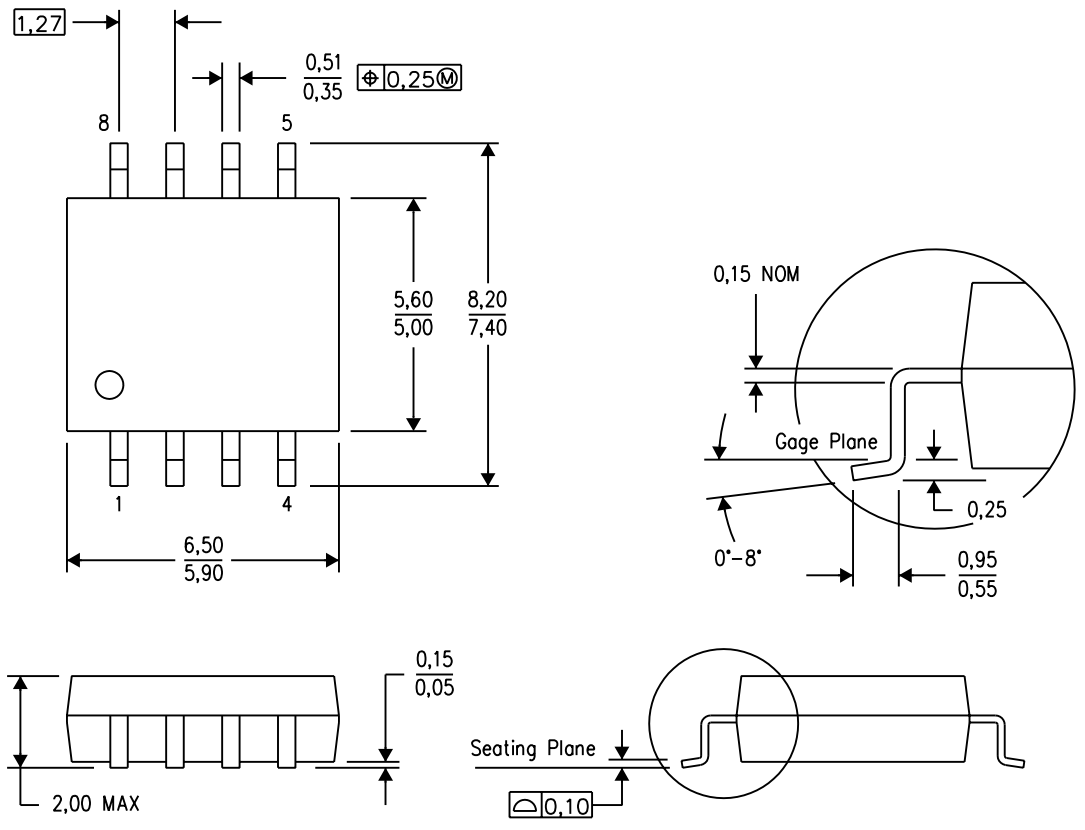


4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MECHANICAL DATA

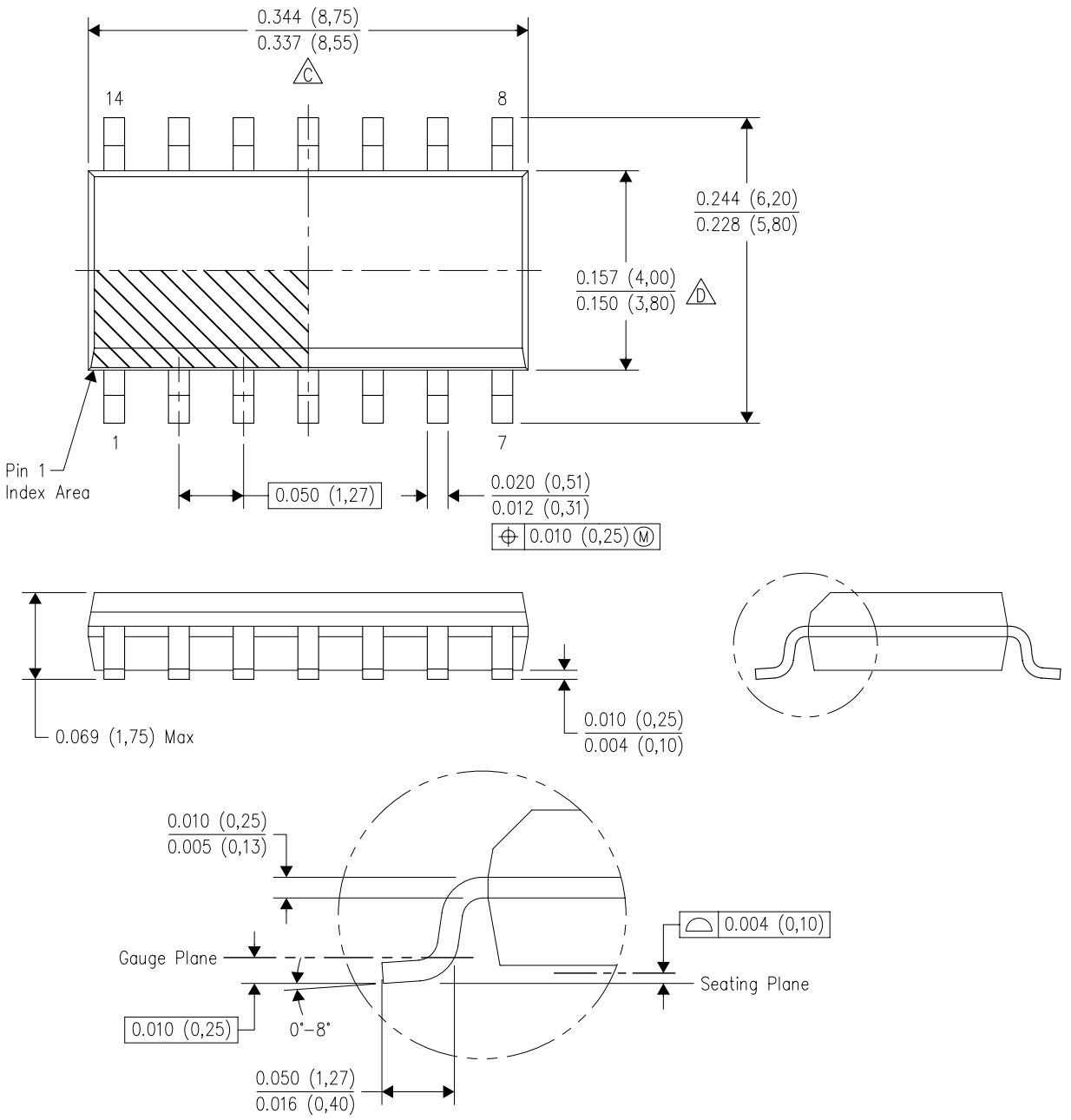
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

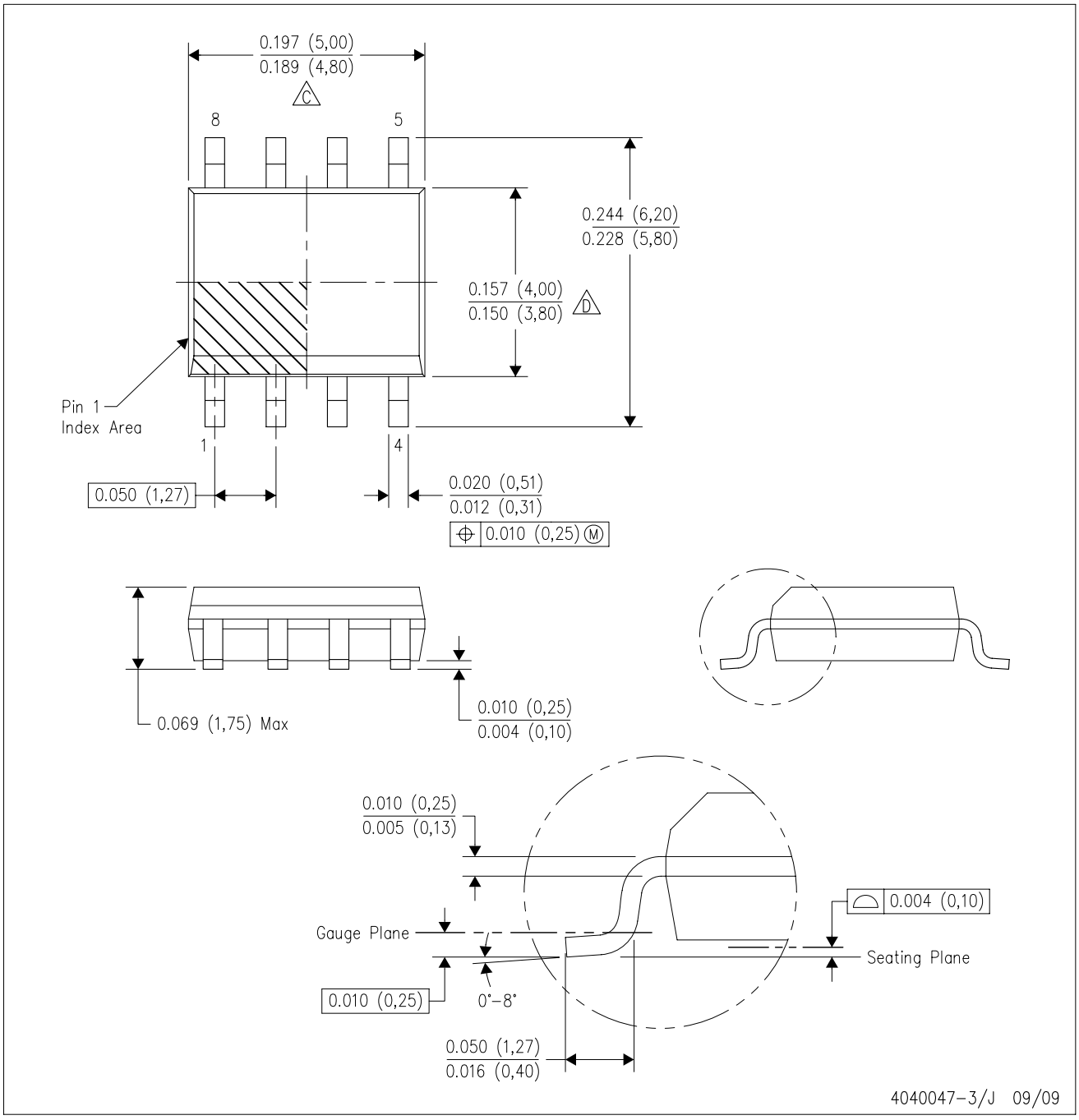
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

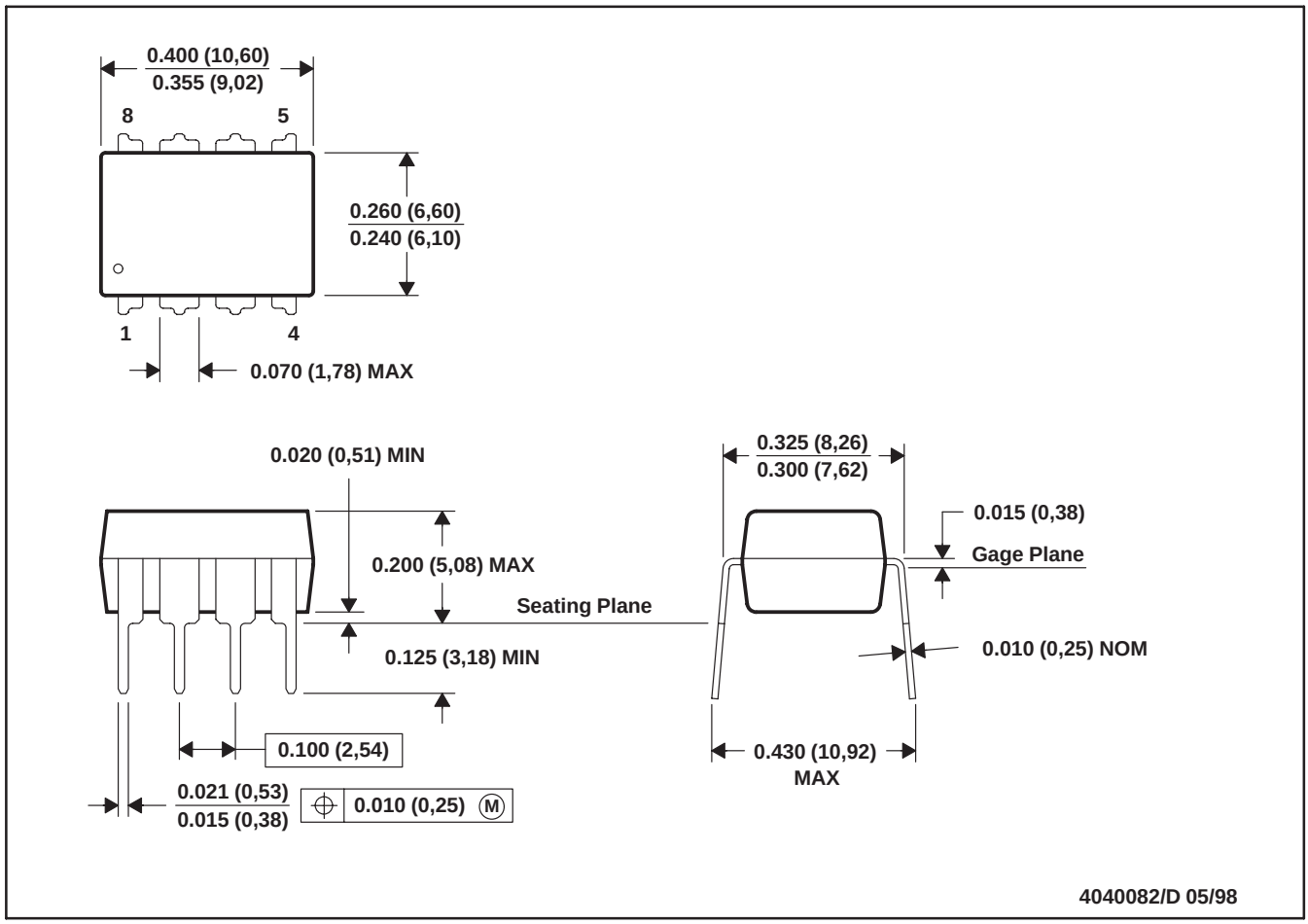
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**

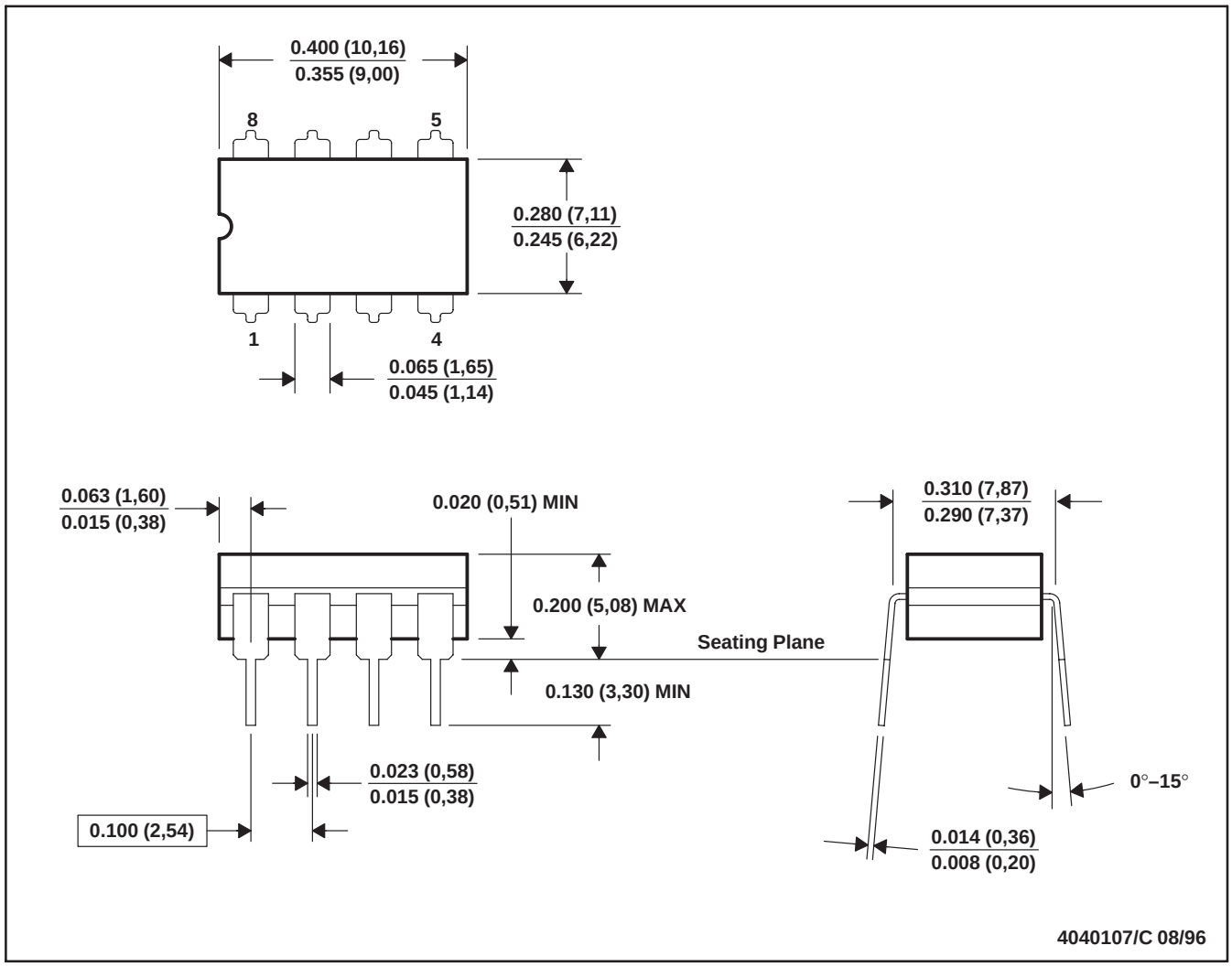


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**

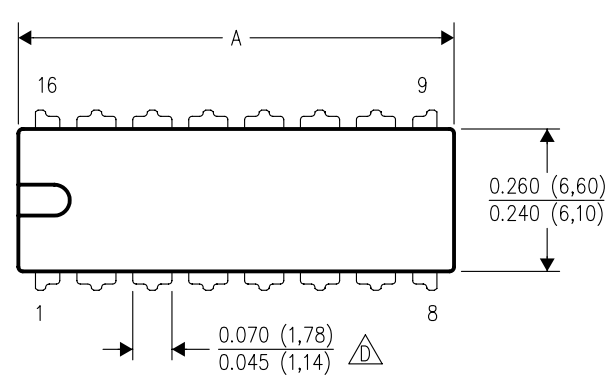


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

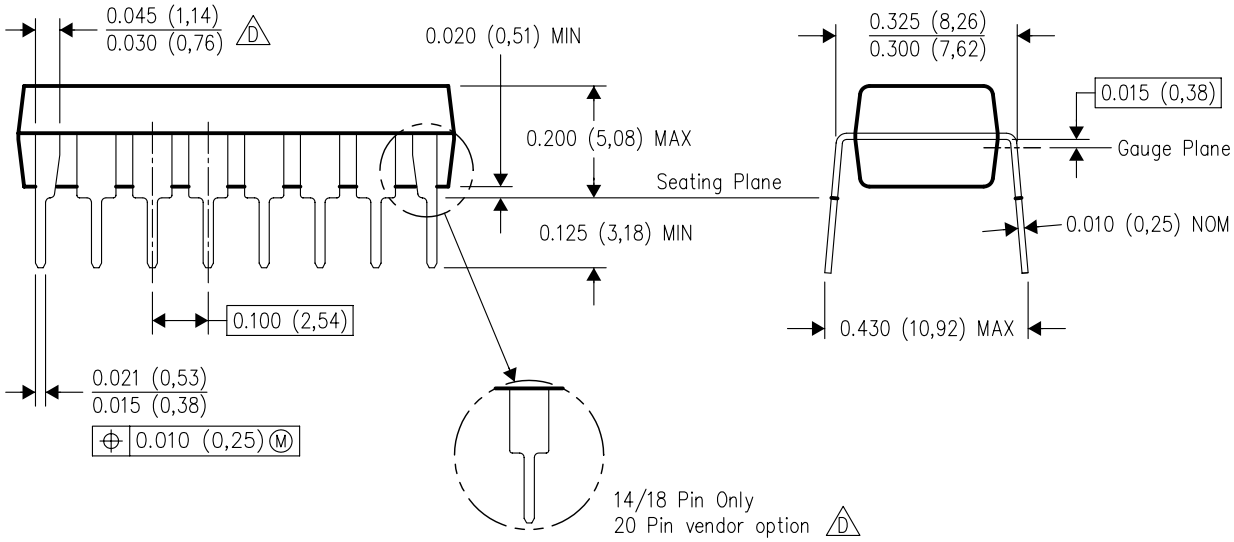
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

USB650 Red Tide Spectrometer for Education

World's Most Amazing Low-Cost Spectrometer

The Red Tide Spectrometer is a low-cost, small- footprint lab spectrometer that's ideal as a general-purpose instrument for your budget-conscious classroom or teaching lab. The Red Tide has a wavelength range of 350-1000 nm, and utilizes a detector with 650 active pixels; that's 650 data points in one full spectrum, or one data point per nanometer. Configured with a 25 µm entrance slit, the Red Tide offers ~2.0 nm optical resolution (FWHM).

Contact an Ocean Optics Applications Scientistist

Convenient Wavelength Calibration! Click here for Details

See additional Educational Spectrometers at Vernier Software & Technology

Flexible Platform, Convenient Interface

The Red Tide is a preconfigured, off-the-shelf spectrometer where all of the optical bench options, such as grating and entrance slit size, are already selected. The Red Tide can be used with various Ocean Optics spectrometer accessories, light sources and sampling optics, to create application-specific systems for various absorbance, reflection and emission applications. With its small footprint (89.1 mm x 63.3 mm), convenient USB interface, and integration times as fast as 3 milliseconds, the Red Tide is a great tool for basic lab measurements.

Spectrometer Alone or with Sampling System

The USB-650 Red Tide comes without a light source or sample system, allowing you the freedom to choose the accessories that best fit your application.

The USB-650-VIS-NIR (at right) comes with a direct-attach light source and sample holder. The light source includes an LED-boosted tungsten source and a sample holder for 1-cm cuvettes that connects to the front of the spectrometer. In this configuration, the system has a wavelength range of 370-980 nm.

The USB-650-UV-VIS includes a deuterium tungsten halogen light source and a 1-cm cuvette holder. In this configuration, the system has a wavelength range of 200-850 nm.

Note: The Red Tide USB650 is not recommended for absolute irradiance measurements. For absolute irradiance, we recommend the USB2000+ miniature spectrometer.

Operable with PCs or Dataloggers

The Red Tide interfaces to PCs via its USB port, which streamlines start-up and supports hot swapping of the spectrometer. What's more, the Red Tide interfaces to PASCO's Xplorer GLX (in blue), a unique combination of datalogger and lab analysis tool that eliminates the need for a PC. The Xplorer GLX is available from Ocean Optics or PASCO. Visit PASCO for details.

The Red Tide also works with Vernier's Logger Pro Software. Visit Vernier for details.

Cross-platform Spectrometer Software

Red Tide operates via SpectraSuite Spectroscopy Operating Software, the first spectroscopy software to run in Macintosh, Linux and Windows. The Chemistry module for SpectraSuite includes features specifically designed for educational use, such as a Beer's Law calculator for absorbance experiments. The Red Tide also works with our educational distributors' software.

Specifications

Physical	
Dimensions (in mm):	89.1 x 63.3 x 34.4
Weight:	190 g
Detector	
Type:	Linear silicon CCD array
Pixels:	650 enabled pixels
Pixel size:	14 µm x 200 µm
Pixel well depth:	~62,500
Sensitivity:	75 photons/count @ 400 nm
Optical Bench	
Design:	f/4, asymmetrical crossed Czerny-Turner
Focal length:	42 mm input; 68 mm output
Entrance aperture:	25 µm wide slit
Fiber optic connector:	SMA 905
Spectroscopic	
Wavelength range: USB-650 USB-650-VIS-NIR USB-650-UV-VIS	350-1000 nm
Optical resolution:n::	~2.0 nm FWHM
Signal-to-noise ratio:	250:1 (at full signal)
A/D resolution:	12 bit
Dark noise:	3.2 RMS counts
Dynamic range:	2 x 10^8; 1300:1 for a single acquisition
Integration time:	3 ms to 65 s (15 s typical max)
Stray light:	<0.05% @ 600 nm; <0.10% @ 435 nm
Corrected linearity:	>99.8%
Computer	
Operating systems:	Windows 98/Me/2000/XP, Mac OS X and Linux w/USB port
Operating software (required):	SpectraSuite Spectroscopy Software

Pricing

Item	Description	Price
USB-650	Red Tide Spectrometer for Education	$1154
USB-650-VIS-NIR	Red Tide Spectrometer for Education with USB-ISS-VIS Integrated Sampling System (Tungsten Light Source and Cuvette Holder Combo)	$1732
USB-650-UV-VIS	Red Tide Spectrometer for Education with USB-ISS-UV-VIS Integrated Sampling System (Deuterium Tungsten Halogen Light Source and Cuvette Holder Combo)	$2887
PS-2636	PASCO's Xplorer GLX Handheld Datalogger & License Key	Call for Price
USB-ISS-VIS	Integrated Sampling System for Cuvettes (Tungsten Light Source and Cuvette Holder Combo)	$577
SPECTRASUITE	Cross-platform Spectroscopy Operating Software	$199
SPECTRASUITE-E	Site license for SpectraSuite allows up to 40 copies for educational institutions only	$2499

+1 727.733.2447 • +1 Fax 727.733.3962 • Info@OceanOptics.com