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OPTIMIZATION OF SURFACE MOUNT TECHNOLOGY SPECIALIZING IN HEAT DISSIPATION IN BGA CSPs

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MQP Proposal Summary
Optimization of Surface Mount Technology

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The purpose of this Major Qualifying Project (MQP) is to research the design and functions of surface mount technology (SMT) such as, but not limited to, leadless chip carriers. The current trend in technology is to make components smaller, more manufacturable, more affordable, and thus more creative designs are required. We intend to research current problem areas in the industry as well as materials used in the field. Research will include current uses and the intended environment for these products. We will contact companies and experts within the field in order to increase our understanding of SMT as it stands today as well as its future. Once we have a grasp of the current status of SMT, we will outline the course of our methodology. This methodology will focus on optimizing facets of SMT. Learning about surface mount devices will allow us to see how smaller microelectronic components are conducive to a wider range of applications than their larger counterparts. Having smaller components will permit a higher density of circuitry. Proximity of electrical connections creates a challenge for effective solder connections and thermal management. Technical difficulties in the manufacturing process cause short circuiting or possible damage to the integrated circuit or circuit board. We will consider the various compositions of solder and their respective properties. Materials respond differently to heat and stress cycles which determine the point of failure due to

operating loads. Having such close connections, cooling often becomes problematic. The potential benefits of this project are improved thermal management and more reliable connections. Packaging of integrated circuits also plays a role in thermal diffusion. While the demand for smaller components is great, it increases the number of complexities and may increase cost. To measure the improvement of our design, our group will develop criteria for reliability using uncertainty analysis and tolerances. We will perform stress analysis with reference to fatigue cycles, strain cycles, and other failure simulations. We will also conduct stress and thermal analysis during power cycles, with special consideration of materials. Such analysis will be completed with the aid of such software programs as AutoCAD, SolidWorks, MathCAD, TAS, and ANSYS, but will not be limited to these software packages alone. In addition to this, we will also initiate cost analysis and evaluate potential manufacturing methods in order to better optimize the usage of SMT. We will use the wealth of resources available to us from WPI which includes access to numerous scientific and engineering journals, technical handbooks, and previous related projects. Ultimately, the goal of this project is to produce a prototype design for further testing, a technical document with our findings, and areas for potential future MQPs.

OBJECTIVE

The objective of this project was to research and simulate BGAs thermally since the microelectronics industry has moved towards smaller components making heat dissipation a major concern in thermal management considerations. The industry is attempting to phase out the use of lead (Pb) due to environmental and health concerns, but by doing so, the Pb-free alternatives alter the components response to thermal loads and adversely affect thermal management efforts.

ABSTRACT

This project describes heat dissipation and mechanical deformation in BGAs. In contemporary industries, demand for smaller packages has increased the concern of thermal management. The lead-free movement has altered the properties of BGAs and comes with its own set of concerns. Packages were simulated and analyzed thermo-electrically using CAD and ANSYS software. The goal was to improve thermal management of electrical loads in CSP BGAs. Lead-based solder simulations demonstrated higher reliability than lead-free alternatives. Results indicate that maximum temperature and stresses were concentrated at the perimeter, especially the corners. This project resulted in suggestions for improvements for existing packaging and opportunities for future projects.

NOMENCLATURE

A	Area (m^2)
ADC	Analog to Digital Converter
ANSYS	Computational Analysis Software
Ag	Silver
Au	Gold
BGA	Ball Grid Array
°C	Degrees Celsius
CAD	Computer Aided Drawing
CBGA	Ceramic Ball Grid Array
CCGA	Ceramic Column Grid Array
Cd	Cadmium
CLASP	Column Last Attach Solder Process
Cu	Copper
CPU	Central Processing Unit
CSP	Chip Size Package
DAC	Digital to Analog Converter
DIP	Dual In-line Package
DVI	Digital Video Interface
ECE	Electrical and Computer Engineering
FCBGA	Flip Chip Ball Grid Array
HDMI	High-Density Multichip Interconnect
He	Helium
I	Current (amp)
IBM	International Business Machines Corporation
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers, Incorporated
IGES	Initial Graphics Exchange Specification
IMAPS	International Microelectronics and Packaging Society
IP	Intellectual Property
In	Indium
I/O	Input/Output
L	Length (m)
L_z	Lorenz number
LCC	Leadless Chip Carrier
LED	Light Emitting Diode
mm	Millimeter
MQP	Major Qualifying Project
N_2	Nitrogen
Ni	Nickel

Pb	Lead
Pd	Palladium
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PCT	Patent Cooperation Treaty
PWB	Printed Wiring Board
Q	Joule heat (ohms/m^2)
QFN	Quad Flat No-lead
QFP	Quad Flat Package
R	Resistance (ohms)
RoHS	Restriction of Use of Certain Hazardous Substances in Electrical and Electronic Equipment
SiO_2	Silicon Dioxide
SMT	Surface Mount Technology
Sn	Tin
T	Temperature (°C)
T_∞	Atmospheric Temperature
TAS	Thermal Analysis Software
THT	Through Hole Technology
TSOP	The Single Outline Package
TSV	Through-Silicon-Via
V	Voltage (V)
WEEE	Waste Electrical and Electronic Equipment Directive
WLP	Wafer Level Packaging
μm	Micrometer
ρ	Density

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1. Introduction

The electronics industry has always strived to develop smaller and more compact circuits. One major development in this endeavor has been the creation of surface mount technology (SMT). SMT has been a major progression in electronic circuits since it utilizes less space than through-hole technology (THT) and can easily decrease the size of the printed circuit board (PCB). By eliminating THT pins that go through the circuit board, integrated circuits (ICs) can now be mounted on both surfaces of the board. Surface mounted leads do not perforate PCBs so both sides of the board may be used to create connections. The elimination of pins also decreases the average package size of ICs by moving solder points from the pins to either along the edges or underneath the IC. The decrease in size and lack of pins make heat dissipation more difficult for ICs with a high concentration of connections. Where THT pins used to be more exposed to the surrounding environment, SMT leads are sandwiched between the IC package and the PCB.

1.1 SMT Definition and Description

SMT is focused on designing components that may be attached to PCBs without pins in order to save space. Its predecessor, THT, required pins that went right through a circuit board, shown in Fig. 1 (University of Bolton, 2010). Using THT, only one side of a circuit board could form electrical connections since the pins perforated the other side. In SMT, this is not true since connections are made at solder joints, which may be mounted on either side of a PCB. One of the many benefits of using SMT is that they can

be mounted to both sides of a PCB since the components are mounted on the surface and require only one side of a PCB. SMT devices also do not need large pins in order to connect to the PCB. All of these factors allow circuits utilizing SMT to perform the same tasks as THT options in a much smaller footprint (Kollipara, et. al., 2005). Part of creating double-sided printed wiring boards (PWBs) requires a process called reflow soldering.

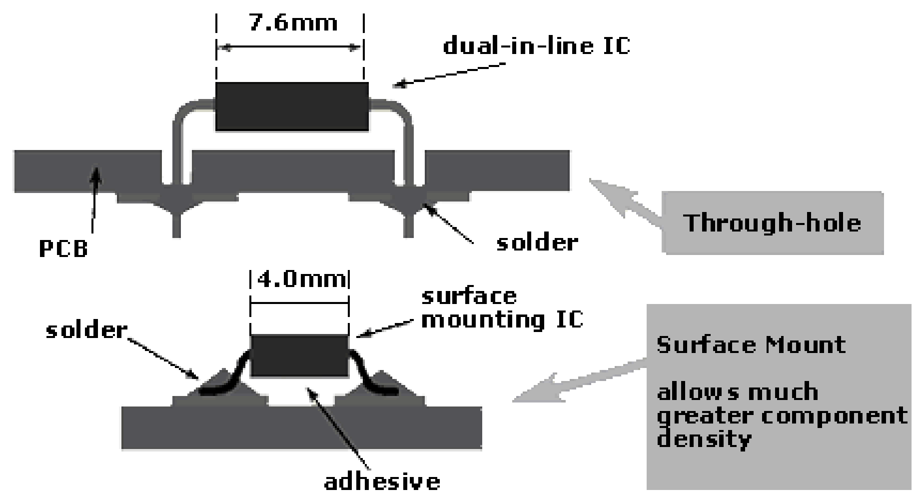

Fig. 1. Diagram of THT versus SMT.

Over the decades, new technologies have been designed and challenged, constantly changing the market as well as the industry of microelectronic packaging. Table 1 is a chart reproduced here from Solder Joint Reliability Prediction for Multiple Environments (Perkins and Sitaraman, 2009). This chart illustrates how quickly such advancements are made and how far this field has come.

Table 1. Improvements in electronic packaging by decade.

Time period	New packaging technology
1970s	Through Hole Technology (THT)
	Dual In-line Package (DIP)
1980s	Surface Mount Technology (SMT)
	Quad Flat Package (QFP)
	The Single Outline Package (TSOP)
1990s	Ball Grid Array (BGA)
	Plastic Ball Grid Array (PBGA)
Mid-1990s	Flip Chip Ball Grid Array (FCBGA)
	Ceramic Ball Grid Array (CBGA)
	Ceramic Column Grid Array (CCGA)
2000s	Chip Scale Packages (CSP)
Mid-2000s	Wafer Level Packaging (WLP)
	Through-Silicon-Via (TSV)
	Stacked Die

1.2 SMT Design Considerations

Reflow soldering is a process by which SMT components are soldered onto PCBs in batches for mass production. Reflow exists in many forms but the industry standard is

infrared or forced convection (Intel Corporation, 2000). The first step in the process is to preheat the ovens to a temperature that is hot but not high enough to bring the solder paste to liquidus. This is important because it allows the solder paste to dry out and evaporates any unstable ingredients within the paste. One part of the solder paste is the flux, which starts cleaning the connection surface when activated. This process reduces oxides, ensuring that the solder joint will be formed as perfectly as possible without any obstructions caused by oxidation. The temperature then rises to very high reflow levels so that all solder melts evenly and completely (Altera Corporation, 1999). Finally, the oven cools so that the solder forms solid and reliable joints without cracks (Blackwell, 2000A). Fast cooling rates reduce the grain size of intermetallic compounds, strengthening the solder joints (Altera Corporation, 1999), Fig. 2 illustrates this process.

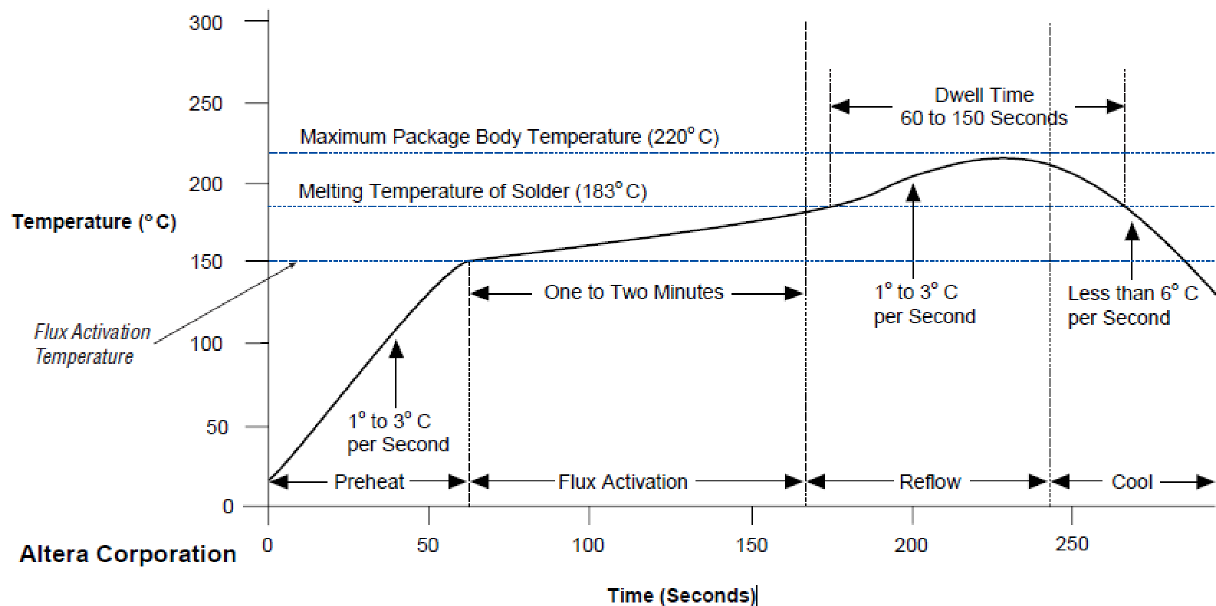

Fig. 2. Convective reflow temperature profile.

The type of connection and the number of connection points must be considered to ensure that electrical signals are sent effectively. The connector brings a signal from

the wires within the package to a via or other similar point on a PCB or substrate. Any package must have reliable connections that do not move or shift easily. In the case of all SMT components, solder is used to form these delicate connections which serve as both an electrical and mechanical connection. In mass production of SMT, connections often cannot be guaranteed to be 100% effective or correct in the same way that THT could. Because all connection points must be soldered together, the effectiveness of each connection is determined by the soldering process. If large numbers of packages are being soldered to a PCB at once, in reflow or wave soldering for example, then there exists a chance that the solder may render the connection between the contacts between the chip and the PCB defective in some way (Blackwell, 2000).

A number of forces must be considered when a solder contact is made. One of which is the normal force, which is perpendicular to the surface connection. This force is exerted by the package on a substrate. This is crucial to the chip's function because it ensures that the chip maintains enough pressure to keep the electrical flow going. Another important factor, mating force, is required to insert or extract connectors from a substrate or PWB. Mating force is directly related to reliability because the best solder joints require a high mating force (Blackwell, 2000).

Another essential consideration is the temperature. Each chip scale package (CSP) is built from a number of materials which protect the transistors inside it from particular hazards. These hazards typically exist as heat damage and corrosion but are not limited to these. Manufacturers generally divulge the temperature rating of CSPs to consumers in order to best protect their products. This rating is the difference between the initial

temperature and the heightened temperature from flowing electrical current (Blackwell, 2000).

1.3 Ceramic Column Grid Arrays

Ceramic column grid arrays (CCGAs) are becoming increasingly popular. They are similar to ceramic ball grid arrays (CBGAs) in their structure and makeup. They also have ceramic substrates featuring grid arrays with solder connectors to a PCB (Actel Corporation, 2008). The greatest difference between CBGAs and CCGAs is that the latter use columns to create a more stable connection. BGAs use solder balls to form electrical connections. Because solder balls are spherical, it is very easy for them to deform over time. This process alters their connections, which makes them less reliable after a number of thermal fatigue cycles. With solder columns, thermal connections are generally more flexible and withstand thermal changes better at the solder joint (Perkins and Sitaraman, 2009). Shown below in Fig. 3 and Fig. 4 are a CBGA (Digi-Key A) and CCGA (Actel, 2008) for comparison.

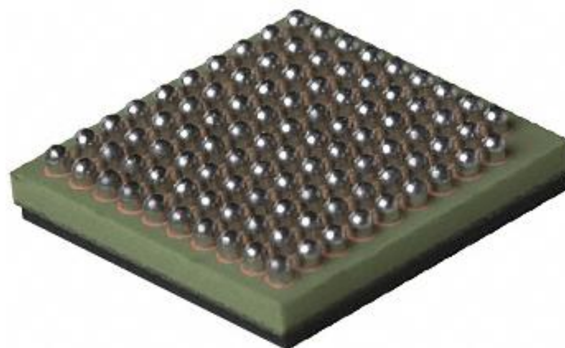

Fig. 3. Ceramic ball grid array.

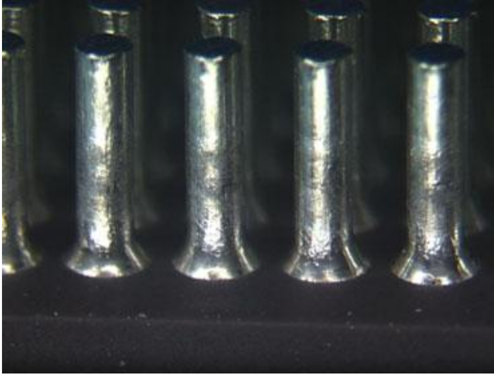

Fig. 4. Ceramic column grid array.

CCGAs have improved thermo-mechanical reliability than CBGA packages. Solder columns have added height compared to CBGAs so they are more flexible during thermal fatigue cycles. As a result, solder joints are more reliable as thermal changes take place (Actel Corporation). For this reason these are gaining popularity in high input/output (I/O) applications (Perkins and Sitaraman, 2009). Some applications which have a high I/O density include analog microcontrollers, high-density multichip interconnect (HDMI)/ digital video interface (DVI) transmitters commonly used in computer monitors and newer televisions, and embedded processors for use in computer central processing units (CPUs) (Analog Devices, 2009A; Analog Devices 2010A). CCGAs use solder columns contain 90% tin (Sn) and 10% lead (Pb) to form a 90Sn10Pb composition. This composition results in a high melting point for each column. More specifically, the International Business Machines Corporation (IBM) has produced a new CCGA package manufacturing process called the Column Last Attach Solder Process (CLASP) (Perkins and Sitaraman, 2009), which can be seen in Fig. 5 (Ray, et. al., 1999). This process features a 63Sn37Pb solder fillet doped with palladium (Pd) on one end of the column and a eutectic 63Sn37Pb solder fillet on the other end. This process results in

two connections per column, such that the doped end connects to the substrate and the standard eutectic lead-tin solder fillet connects to the PCB. The doped connection on the substrate side features a higher reflow temperature than the board side so that the solder fillets will not reflow onto the substrate side, possibly damaging the chip and any data within it.

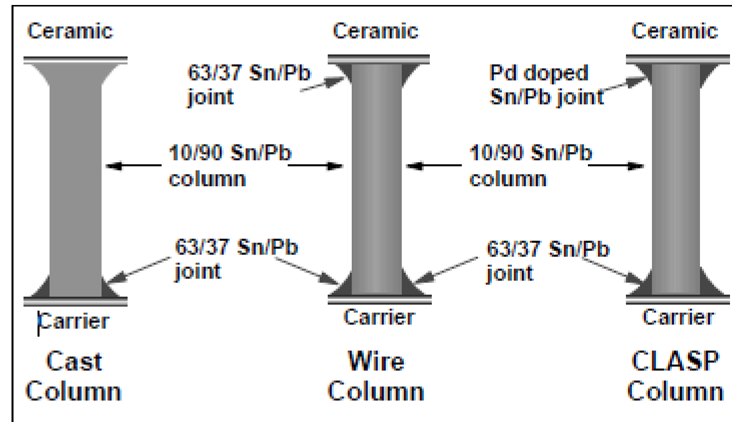

Fig. 5. IBM ceramic column grid array processes.

A data sheet from IBM from 1999 states that CLASP will become the standard CCGA process. Perkins and Sitaraman confirmed this in 2009 while describing CCGA packaging. CLASP technology is used mainly for flip chip processes. Before CLASP, IBM developed wire columns in 1991, which connected a 90Sn10Pb solder column to a substrate and a PCB using eutectic solder on both connections Figure 6. In 1993, IBM created a newer method: cast columns. This involved melting a 90Sn10Pb solder column down into a filleted mold to attach one end to the substrate. The other end connected to the board by using eutectic solder. Cast columns performed better in the industry because the columns were already attached to the substrate before starting the reflow process. This process became more popular than wire casting as a result (Ray, et. al., 1999).

1.4 The IMAPS Experience

As part of the research for the project our advisor recommended that we attend the local International Microelectronics and Packaging Society (IMAPS) monthly meeting. This meeting's special guest was Mr. Victor Champagne Jr., the advanced materials and processing team technical leader (Champagne Jr., 2009). His lecture was on one of the United States Army's new advancements in thermal spray. This process, called cold spray, applies the same idea as thermal spray but performs at room temperature. While the temperature may stay low the speed of the practical stream can reach speed up to 1500 m/s. Fig. 6 is of a test of Al particles being fired in nitrogen (N_2) gas. The process involves injecting very fine particles, with diameters of one to forty microns, into a heated gas that is then fired at the appropriate material or surface. In Fig. 7 the process has been simplified in a flow diagram (U.S. Army Research Laboratory, 2008).

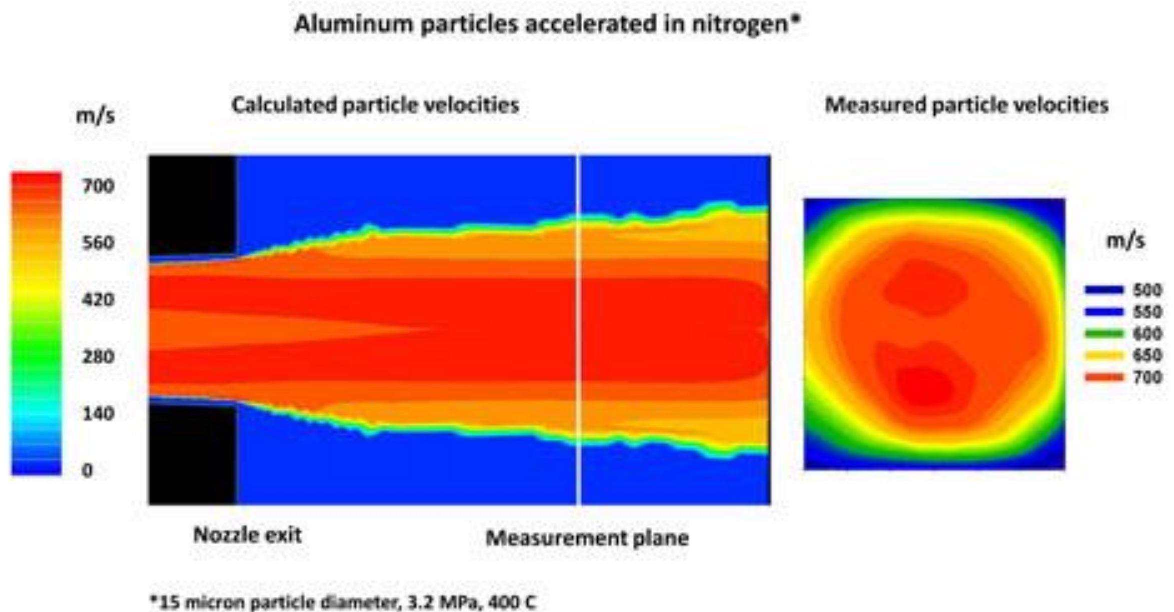

Fig. 6. Aluminum particles accelerated in nitrogen.

Cold spray has many advantages and applications. For example, warzone medical facilities often do not have the time to properly sterilize equipment or work surfaces. In such cases, infections can be common. With cold spray technology, workers can lay a microscopic layer of copper (Cu) on medical equipment and surfaces which assists in disinfecting bacteria. Fig. 7 illustrates the cold spray process (U.S. Army Research Laboratory, 2008). The process begins with nitrogen or helium (He) gas flowing into a tank. This gas is then heated and then filtered into powder. It travels into a high-powered nozzle to create a spray which may be streamed onto surfaces for disinfection or other purposes.

Current research suggests using this technology in constructing and possibly even manufacturing microchips. Cold spray is still in developmental stages but it has a large following and eventually may be a very useful advancement (Champagne, Jr., 2009).

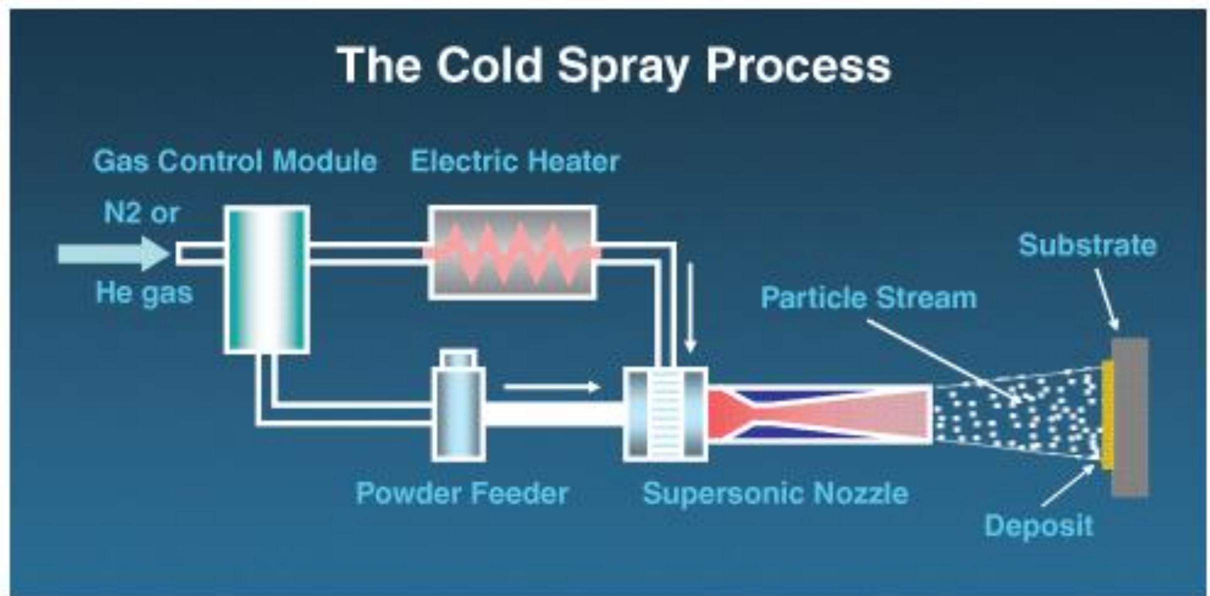

Fig. 7. Simplified cold spray process.

A member of the project team attended the IMAPS Conference on February 23, 2010. Mario Scalzo, a representative from Indium Inc. presented on the subject of light emitting diodes (LEDs) and recycling (Scalzo, 2010). One subject he discussed was the availability of solder performs for both Pb-based and Pb-free alternatives. On the same token, Indium Inc. has created NanoFoil, which is a self reacting solder that gives a consistent bond line, acts as a heat sink, has superior conductivity to soft solders, builds high strength bonds, and will not propagate fractures over time. NanoFoil is Pb-free and has two compositions because it is designed to react, forming a new composition from the old. The initial composition before the reaction consists of alternating layers of nickel (Ni) and aluminum (Al). The final composition following the reaction is 50Ni50Al.

NanoFoil is also creep resistant and may be used in a number of applications, such as LEDs, thermal management, and optical component attachments. Haitz's Law applies to all LEDs, stating that every decade the cost per lumen or unit of light decreases by a factor of ten but, in the same ten years, the total amount of light generated by the LED increases twenty-fold within the same color (Nature Photonics, 2010). Such changes require a relatively consistent and stable electrical connection which manages heat fairly well.

Soft solders, such as tin-silver (SnAg), have high melting points compared to eutectic solders. Gold (Au)-based solders, e.g. AuSn are harder, and have 50°C between operating temperature and liquidus temperature. Soft solder needs additional flux or an inert atmosphere to prevent oxidation. NanoFoil's reaction is similar to a hard solder since it does not have a tendency to oxidize. For this reason, no flux or additional

adhesives are needed with this special solder. This product is available as solder paste, pre-forms, and sheets.

There is a major movement within industry to be greener and more environmentally conscious. This has caused a heightened awareness of recycling and proper disposal of potentially hazardous materials. Currently, the United States generally recycles harmful waste such as batteries and computer parts. Many other countries, however, do not have recycling protocols in place. This has also led to Pb-free alternatives in Europe, the United States, and the rest of the world. Pb, along with a number of other substances and compounds found in engineering materials, when improperly handled may cause illness or other harm.

The third and final IMAPS meeting that the team attended was about patents and other forms of legal protection for new ideas. Two speakers presented: Robert J. Sayre and Joseph B. Milstein (Sayre, 2010; Milstein, 2010). The most important reasons to get a patent are to exclude others from using ideas, to gain pricing power, improve financing, provide licensing or cross-licensing, and to defend intellectual property (IP). A patent may be granted only if it is an obvious new composition or physical structure, product, component, process, software, or business method. While it is important to protect one's own IP rights, patents are not the only form of protection. Patents require three years and incur an average lifetime cost of approximately $30,000.

Patents tend to be so expensive because they require hiring experts with a decent understanding of domestic and international patent law. For maximum protection, apply within nations that follow the Patent Cooperation Treaty (PCT). This way all or most of the protections granted within the United States may be honored overseas as well.

Always secure patents where they would be relevant. If a product is manufactured quickly in Korea, it makes sense to get a patent in that country as well as in the United States where it might be sold. It might also make sense to patent internationally if competitors exist in those countries (Sayre, 2010).

In many cases, patents are not the best option for a company or individual. Patents generally last only about 20 years and are costly. Trade secrets do not have a set time limit and cost. Trade secrets are best for products or ideas that cannot be reverse engineered because, unlike patents, they do not require that the rest of the world is informed about how to make them. Trade secrets require that an entire company never tells how their processes or operations work. If a competing business learns their secret, the first company may be out of commission (Milstein, 2010).

Since technology is changing so quickly, the patent system is becoming relatively outdated. To combat this, the United States Patent and Trademark Office (USPTO) is facing reform in the near future as the Patent Reform Act of 2010 is going into effect (Patently O, 2010). The list of items which may be patented is growing fast. New protections are required to protect a new age of intellectual property.

1.5 Problem Description

Insufficient heat dissipation can cause several problems for the IC and PCB. Over multiple power cycles, the IC and the board do not expand at the same rate and microfractures may occur, ultimately leading to the eventual failure of the part. If heat

cannot escape, it accumulates to a point where it damages the parts and in extreme cases, melts the solder and short circuits the component.

This project focused on researching of two major styles of SMT: ball grid arrays (BGAs) and quad flat no-leads (QFNs). Both styles have varying dimensions, materials, and functions, all of which have an effect on the thermal behavior of the chip. BGAs have several styles in which the array is oriented. While most have a square footprint, there are some that have a rectangular array. Most BGAs have a linear array, but there are some which condense the leads by staggering the rows. Within the square-shaped BGAs, there are many types of arrays which affect the way in which heat transfers away from the chip. QFNs sometimes include a metal contact along the bottom in addition to the leads to help facilitate heat transfer by increasing the amount of conduction. Some variations of a QFN only have contacts along two edges of the chip seen in Fig. 8 (Amkor). Other models have dual rows of leads on each side. Fig. 9 shows BGA samples used in this project.

Fig. 8. Quad flat no-leads.

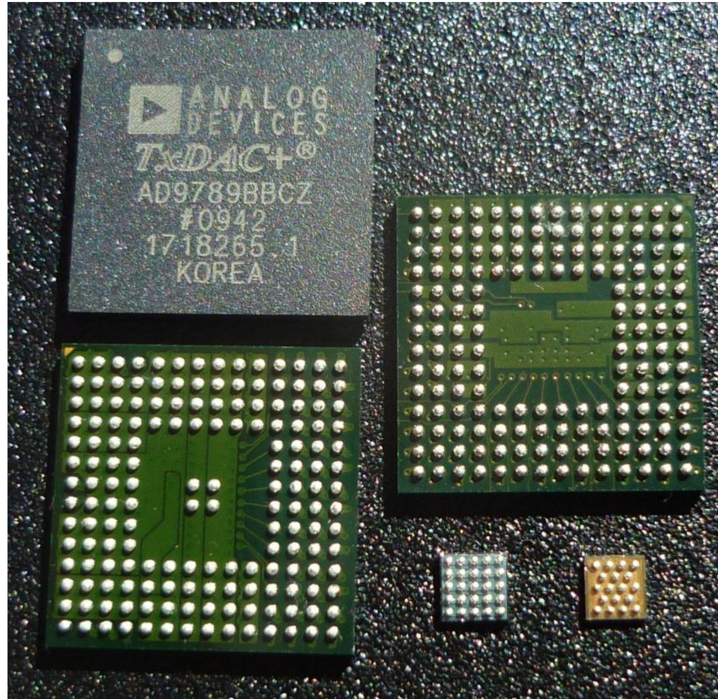

Fig. 9. Samples of some BGAs obtained by the group. Photograph courtesy of Julie Hitchcock.

The materials used in the IC package also greatly affect the heat dissipation of the component because they have different thermal coefficients as well as thermal conductivities. Packaging may be ceramic or plastic, with ceramics being able to withstand more heat. Contact points can also have different metal compositions that have their own electrical and thermal properties that influence the effectiveness of the component. Solders used to attach the surface mount components can also vary greatly, with the biggest distinction being with or without Pb. That can change how the chip functions electrically while altering thermal properties. Solders with distinctive material compositions experience thermal and mechanical loads differently. Each of these factors affects how the heat transfers away from the chip. Some designs are more thermally efficient than others, which is what this project sought to determine.

There are many styles of SMT, especially BGAs. Some include plastic ball grid arrays (PBGAs) as shown in Fig. 10 (Digi-Key B) or CBGAs depicted in Fig. 11 (Digi-Key C).

Fig. 10. Plastic ball grid arrays.

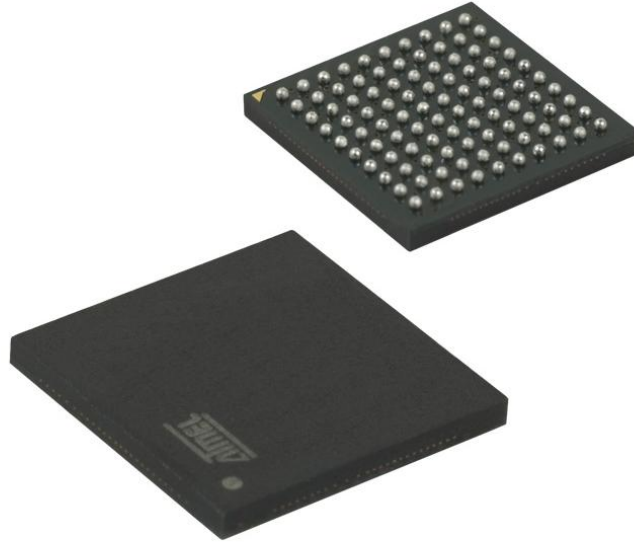

Fig. 11. Ceramic ball grid arrays.

By conducting thermal analysis of different solders and SMT package designs, the optimum design for efficient heat dissipation can be determined. This can help influence the design of future SMT components from the actual dimensions and style of the chip and the materials used in the chip.

1.6 Materials

Materials and their properties are always an important consideration for the design, manufacture and use of any product. In the case of BGAs and any other SMT products, proper solder and package selection of materials is fundamental. The leads need a higher melting temperature than the solder; otherwise during manufacture or any reflow processes, both the lead and the connection would melt and could create electrical shorts or otherwise render the component useless. The package needs to withstand the melting temperature of the solder connections, otherwise the encased silicon chip and internal

gold wires will be exposed to undesirable conditions and loads. These materials also dictate the behavior of mechanical and thermal loads on the component. With the concern about the use of Pb, alternatives to various solders have been developed, a number of which contain three different metals within them, some of which can be seen in Table 2 (National Semiconductor Corporation).

Table 2. Solder composition and applications.

Package Type	Option	Solder Composition	Solder Plating Thickness
Leaded Packages	Standard	85% Sn, 15% Pb	5.08 microns minimum
	Pb-Free	Matte Sn	8 microns minimum, 12 microns nominal
LLP, TSOT	Standard	85% Sn, 15% Pb	5.08 microns minimum
	Pb-Free	Matte Sn	8 microns minimum, 12 microns nominal
		NiPdAu	0.53 microns minimum
TO-92	Standard	85% Sn, 15% Pb	5.08 microns minimum
	Pb-Free	99.3% Sn, 0.7% Cu	15-20 microns (solder dipped)
Micro SMD	Standard	63% Sn, 37% Pb	N/A
	Pb-Free	98.3% Sn, 1.2% Ag, 0.5% Cu or 95.5% Sn, 4.0% Ag, 0.5% Cu	
Micro SMDxt	Pb-Free	96.5% Sn, 3.5% Ag	N/A
Ball Grid Array	Standard	63% Sn, 37% Pb	N/A
	Pb-Free	95.5% Sn, 4.0% Ag, 0.5% Cu	
Metal Can (TO-3, TO-5, TO-46)	Standard	63% Sn, 37% Pb	
	Pb-Free	96.5% Sn, 3.0% Ag, 0.5% Cu	8 microns minimum (solder dipped)
Cerpak	Standard	63% Sn, 37% Pb	5.08 microns minimum
	Pb-Free	96.5% Sn, 3.0% Ag, 0.5% Cu	8 microns minimum

Some of the alternatives to using lead include: Ni, Au, Ag, Cu, and indium (In). With these alternatives, the thermal and mechanical properties of the overall SMT components have changed. Components that were considered reliable with Pb alloys may not be as reliable when replaced by Pb-free alternatives, unless reliability criteria are redefined to take into consideration Pb-free solders.

In Europe in July 2006 the new Restriction of Hazardous Substances Directive (RoHS) took effect. This legislation restricts the use of hazardous materials in technical devices to help cut down on the ever growing e-waste problem. The fear is that as the e-waste builds in landfills and dumps that the hazardous waste will began to be absorbed in to underground water supplies. It is well documented that ingested Pb can cause many life threatening illnesses. The push to remove Pb has many drawbacks, thought it is an environmentally responsible decision. While Pb was one of the best options on the solder market there are other Pb-free alternatives. Many of the alternatives involve Sn, Ag, and Cu. The Pb-free options, while viable, come with several disadvantages such as cost, temperature dissipation, and whiskering.

Improper exposure to Pb has also been found to be very harmful to the human body. In the past it was common to find Pb in many common household items from plumbing pipes i to the paint on the walls to gasoline in cars. As time went on, Pb’s harmful qualities became apparent to communities and governments. This led to the outlawing of Pb in many products to help prevent exposure. Pb is found commonly in nature and even in the human body, but as it becomes more concentrated it becomes more dangerous. One of the larger concerns associated with Pb the fact that it has polluted natural water supplies in the past. This can happen through corrosion of leaded pipes,

dumping of lead waste, or rain water carrying it away (Agency for Toxic Substances and Disease Registry, 2007).

One of the problems with Pb-free solder is the growth of whiskers on the Pb-free solders. The problem is not new but has been brought to the foreground because of the increased use of the Pb-free solders. One of the first documented cases of whiskering was during World War II by a man by the name of H. Cobb. He noticed this phenomenon when some radio equipment began to fail that the cadmium (Cd) coated plates within the equipment had grown whiskers. These whiskers caused a bridge between the plates resulting in a short and the failure of the system. A few years later, Bell Laboratories began running long term testing on whiskering (Brusse and Leidecker, 2007; Brusse, Leidecker, and Panashchenko, 2008). The problem was solved many years ago by adding a small amount of Pb to the solder. Fig. 12 displays Sn whiskering on a PCB with SMT components (Answers Corporation, 2010).

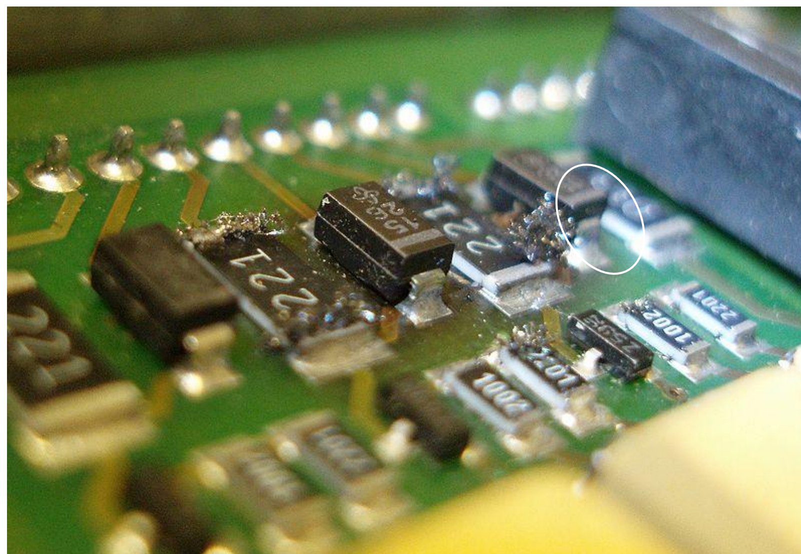

Fig. 12. Tin whiskering.

Whiskering refers to growth that occurs on metals more specifically in Sn, zinc (Zn), and Cd. It is not limited to these metals but they are the most prone (Panashchenko, 2009).

Whiskers can have varying levels of effects on electoral system. For instance a whisker that grows and never touches any other part is a crude heat sink, but if it touches some other component it causes the system to short circuit or fail. When a whisker makes contact with some other component, two different things can happen. The first is that it makes contact and starts shorting the system, this can cause a number of problems. The second is when the whisker makes contact it heats up from the current running through itself and if the temperature is greater than the melting point of the whisker it melts and the short stops. While this still may be very problematic, the short lasts a shorter time frame. The resistance of a whisker can be measured by the following formula:

$$R_{wire} = \frac{\rho * L}{A} \quad . \tag{1}$$

Where rho (ρ) is the resistivity of the material and R is the resistivity of the whisker. The next two equations show the current and voltage needed to melt a whisker. These equations where developed in ideal situations using a vacuum to eliminate outside influences.

$$I_{melt} = \left(\frac{2\sqrt{L_Z * T_0}}{R_0}\right) * \cos^{-1}\left(\frac{T_\infty}{T_{melt}}\right). \tag{2}$$

$$V_{melt} = 2\sqrt{L_z} * \sqrt{{T_{melt}}^2 - {T_\infty}^2} \quad . \tag{3}$$

The variable L_Z represents the Lorenz number while the T_0 and R_0 refer to the reference temperature and resistance, respectively (Brusse, Leidecker, and Panashchenko, 2008).

Whiskers' sizes vary but are on the magnitude of several micrometers (μm) in diameter and millimeters (mm) in length. When a large amount of current passes through it, the whisker can often melt. If the temperature surpasses the melting point of the metal, however, the whisker could vaporize and lead to problems for a system. When the whisker vaporizes it becomes an ionized cloud within the system, which has negative effects. Due to its ionized nature, the cloud may cause an electrical arc. For this arc to occur, the gap in which it crosses must be very small. This arc can transfer large amounts of current to parts of the system that cannot handle that level of power.

Another reason for the Pb-free movement is cost. Over the years, the prices on varying metals have fluctuated but always within a certain set of relation to each other. While the price of silver might drop it is highly unlikely that it will ever drop below the price of Pb or Cu. Figure 13 displays a comparative graph of the cost of Pb, Cu, Sn, and Ag over the last five years (Investment Mine, 2010).

Fig. 13. Cost of Pb, Cu, Sn, and Ag over the last five years.

In Fig. 14, each metal has its own scale on the side with a color to match and the price range. Of the four metals, Ag, Cu, Pb and Sn, Pb has had the lowest prices in the past five years ranging from approximately \$1/kg to \$4/kg. While not the largest proportion of many solder compositions, Pb is a considerable component. Pb is significantly less than these other metals and keeps the overall price of solder low. With growing concerns over the use of Pb, one solution has been to change the proportion of Sn to Pb to include more Sn. This increases the cost of solder as Sn has ranged between \$6/kg and \$24/kg over the past five years. Another solution has been to remove Pb altogether and use other metals in junction with Sn. By replacing Pb with these more

expensive materials, the cost of solder increases. Along with the increase in cost, the material properties of the solder change as well. This changes the manufacturing process since many of the favored Pb-free solders have higher melting points. Higher melting points mean that the equipment used for reflow soldering need to reach higher temperatures to properly solder electrical components to PCB. Companies may need to purchase new machinery if their current equipment cannot reach these higher temperatures. Some smaller companies cannot handle retooling their process and are being forced out of business.

For executing analysis on SMT components and their solder connections, a battery of specific properties is required to sufficiently model them. The most important properties to the mechanical and thermal analysis are density, the coefficient of thermal expansion and its reference temperature, the isotropic elasticity in terms of Young's Modulus (also known as the Modulus of Elasticity) and Poisson's Ratio, tensile yield strength, compressive yield strength, isentropic thermal conductivity, and isotropic resistivity (Table 3). One of the challenges the project encountered was to obtain the necessary material properties for adequate simulation.

Table 3: Four solders and their respective properties

Name of material	Composition percent wt.							
	Ag	As	Bi	Cu	Pb	Sb	Sn	Other
60-40 Tin Lead	0	0.03	0.25	0.08	45	0.5	61.5	0.02
63-37 Tin Lead	0	0.03	0.25	0.08	37.5	0.5	63.5	0.02
70-30 Tin Lead	0	0.03	0.25	0.08	35	0.5	71.5	0.02
97-3 Tin Silver	3.5	0	0.15	0.08	0.1	0.12	96.6	0.02

Name of material	Mechanical properties							
	density (kg/m^3)	Young's modulus (Pa)	shear modulus (Pa)	Poisson's ratio	yield strength (Pa)	tensile strength (Pa)	compressive strength (Pa)	fatigue strength at 10^7 cycles (Pa)
60-40 Tin Lead	8.60E+03	3.20E+10	1.50E+10	0.4	4.00E+07	6.00E+07	4.00E+07	3.00E+07
63-37 Tin Lead	8.50E+03	4.00E+10	1.50E+10	0.4	4.00E+07	6.00E+07	4.00E+07	3.00E+07
70-30 Tin Lead	8.40E+03	4.50E+10	2.00E+10	0.39	3.00E+10	5.00E+07	3.00E+07	2.50E+07
97-3 Tin Silver	7.33E+03	6.00E+10	2.50E+10	0.365	2.80E+07	4.10E+07	2.80E+07	2.10E+07

Name of material	Thermal properties						
	Melting point (°C)	Max. service temp. (°C)	Min. service temp. (°C)	Thermal conductivity (W/m*K)	Specific heat capacity (J/kg*K)	Thermal expansion coefficient (/K)	Latent heat of fusion (J/kg)
60-40 Tin Lead	188	27	-148	60	170	2.50E-05	4.50E+04
63-37 Tin Lead	184	27	-148	55	170	2.60E-05	4.50E+04
70-30 Tin Lead	192	27	-148	60	170	2.22E-05	4.50E+04
97-3 Tin Silver	222	27	-273	70	230	2.50E-05	6.40E+04

Name of material	Electrical resistivity (ohm*m)	Price (USD/kg)
60-40 Tin Lead	1.60E-07	7.96
63-37 Tin Lead	1.55E-07	8.22
70-30 Tin Lead	1.55E-07	9.09
97-3 Tin Silver	2.20E-07	26.9

1.7 Encapsulation

The concept of encapsulation involves isolating a component and simplifying its inner workings. This way, all that matters in this case is what is put into the system and what comes out as a return. This allows for simplifications in the overall system. For example, consider an electrical motor that is plugged in to a normal US wall outlet the motor will produce an output of 120V at a frequency of 60 Hz (Global Electric and Phone Directory, 2010). Now this information can be used to determine whether or not it may perform certain tasks. In this example, the motor was determined to provide an output without knowing the specifics of how it was able to convert an electrical input into a mechanical output.

This concept is used in electrical and computer engineering (ECE) when there is a large circuit that has many different components which serve different operations. The different circuit areas that have a defined operation may be shown as one object in order to simplify it. If each part was to be simplified in his way and then strung together in a path or operational diagram, a non-technical picture can be formed. The depiction of the circuit will often take the form of a flowchart. Fig. 14 displays a diagram of a circuit that performs the relatively simple task of measuring the stress on a beam. If the stress is above a given magnitude, a red light emitting diode (LED) turns on and if it is below that magnitude a green LED turns on. The circuit is large and complex; however, the different parts were converted into flowchart, as seen in Fig. 15, making the function of the circuit easier to comprehend. Encapsulation can be taken a step further. A part that was previously simplified may be encapsulated again as part of a larger component in an

iterative process (Fig.16). Depending on the scenario and what information is necessary, the encapsulated part may be more useful than a full diagram.

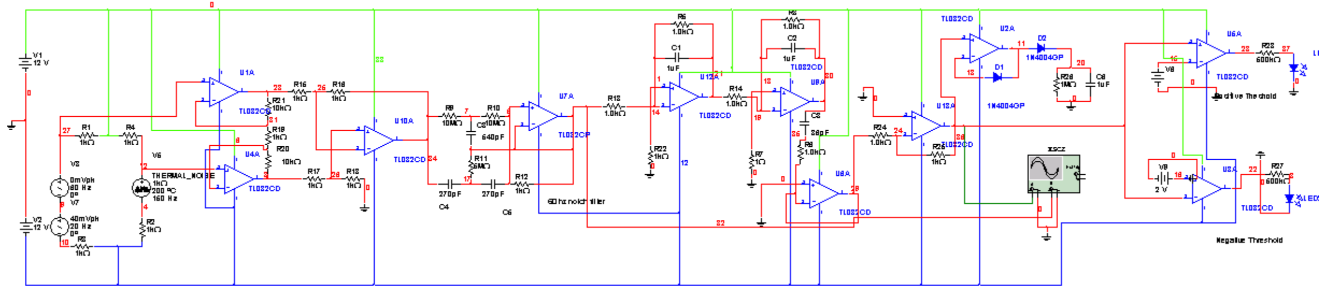

Fig. 14. Electrical Schematic of Load Sensitive LED System.

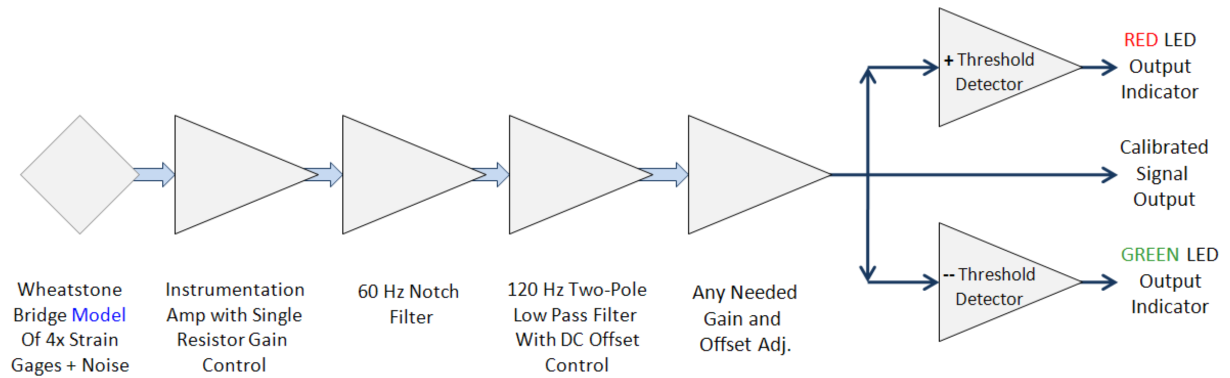

Fig. 15. Descriptive Flowchart of Electrical Schematic.

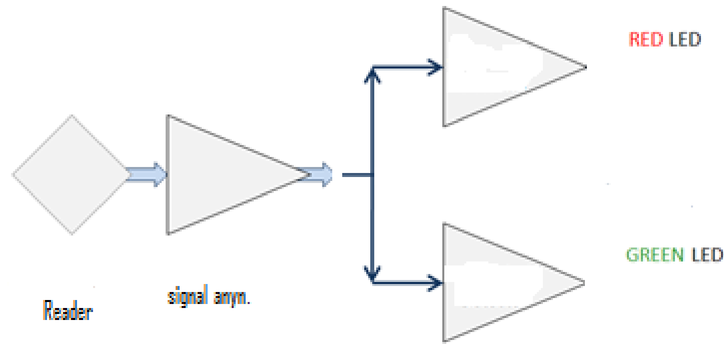

Fig. 16. Encapsulated Simplification of Load Sensitive LED System.

The typical ball grid array package is layered. It consists of solder ball leads, a die, a chip, a substrate, and several wire bonds. The substrate is an outer covering, usually made of ceramic or plastic, which holds the die within it. The die houses the chip inside the BGA. Wire bonds connect the die and the solder ball leads to one another and are generally made of gold. These bonds carry electrical signals from the chip to the board. Many substrates contain heat spreaders to help dissipate heat and air flow. Depending on the design of the BGA, these components may change slightly. Some packages will have other features such as liquid encapsulant or additional epoxies and adhesives to make the BGA more compact. Fig. 17 shows two types of BGAs: tape ball grid arrays (TBGAs) and closed loop tape ball grid arrays (CLTBGAs). In general, it is not important to know the specific components and adhesives inside of a BGA, especially with respect to thermal management. This is why encapsulation is important in the scope of this project. A fundamental understanding of BGAs is all that is required to perform the type of thermal analysis that is delineated in this project.

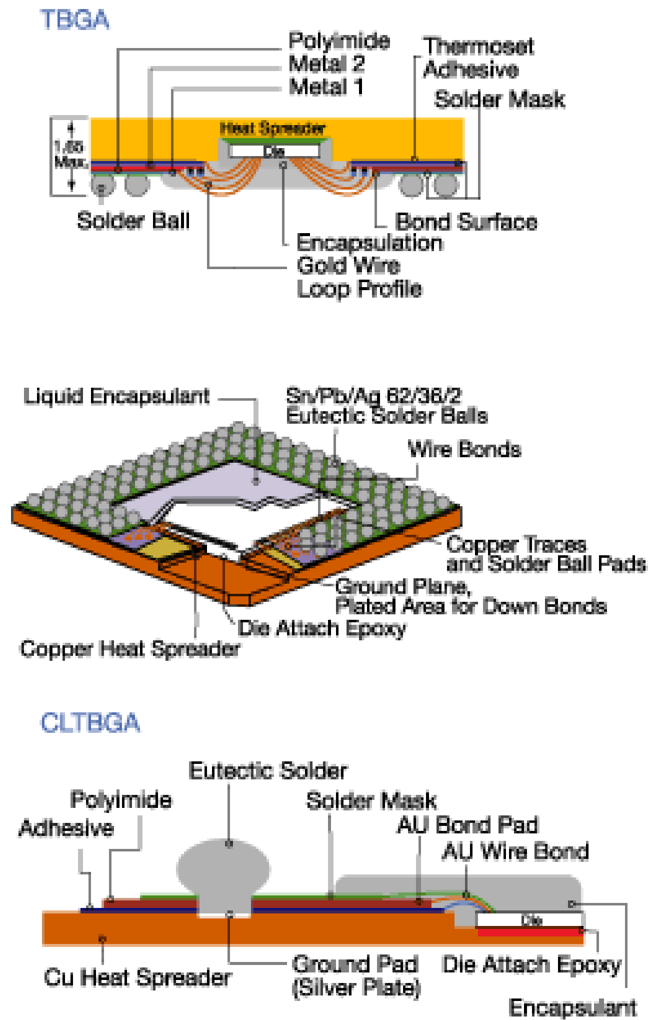

Fig. 17. Internal structure of a typical BGA.

This idea has been very useful to this project for several reasons. First, due to the time restraints of the project it is impossible to thoroughly understand every aspect of a microchip. The background of the project is more focused on the thermo-mechanical aspects rather than the specifics of ECE inner workings. In the scope of the project, microchips will be considered black boxes. The loads that can generate heat and stresses on the components and the direct effects from those loads will be the only things taken into consideration during analysis. The specific electrical processes within the package

are not relevant to this project. While this is not the most accurate method, it makes the goals of the project more achievable with given resources.

1.8 Applications

SMT has applications in a plethora of fields. The IMAPS website includes a table (Table 4) that indicates which industries use SMT components and how they are used within each one. SMT can be used in systems and applications, design or materials and process within each of industry. Some industries do not have a use for SMT yet, but this technology already has numerous uses in the automotive, biomedical, energy and military/security industries.

Table 4: IMAPS table of SMT uses in industry

Industry	Systems & Applications	Design	Materials & Process
Automotive	• Power/Hybrid Modules • Powertrain Control • Collision Avoidance and Safety • X-by-Wire • Driver Comfort/ Information/Audio Systems • Telematics	• Thermal and Power Management • RF/Wireless/mmWave/ RADAR/LIDAR/IR • Harsh Environment • MEMS and Sensors • High Performance Interconnects • Systems on Chip	• Thermal and Power Packaging • Sensor and MEMS Packaging • Advanced Interconnects, Connectors and Wirebonding • Ceramic Substrates and Ceramic Technologies • High Density and High Performance Organic Substrates • Underfill/Encapsulants and Adhesives • Solder Materials, Processes, and Reliability • Flip-Chip and Bumping: Processes, Reliability • LED Packaging • Embedded and Integrated Passives • Green Packaging/Compliance with RoHS
Biomedical	• Implantable • Imaging and Optics • Biosensors • MEMS/NEMS • Nano Technology • Hearing/Vision Aids • Neurological Devices • Cardiovascular Diagnostics • Disposable Electronics • Biometric Identification	• Power Management • Wireless/RF Telemetry • Microfluidics • Environmental Constraints for Medical Products • EMI • Thermal	• Biocompatible Materials • Reliability Assessments • Qualification Approaches • RoHS Compliance • Regulations • Outsourcing Issues • Flipchip • LTCC • Wirebonding • Substrates
Energy	• Solar Energy (Photovoltaics) • BioFuels and Energy from Waste • Fuel Cells • Wind Energy • Batteries and Hybrids	• Thermal and Power Management • Environmental Regulations • Design for Efficiency	• Materials & Reliability Qualification Approaches • RoHS Compliance & Regulations • Outsourcing Issues • Government Policies
Military, Aerospace, Space and Homeland Security	• Space Systems • Homeland Security Systems • Microwave Systems • High Speed Digital Systems • Communication Systems • Vision Systems • Energy Systems	• Mobile Military Electronics • Display Modules • Filters • Antenna • Transmitters/ Receivers • High Speed Digital Design • Energy Sources • Sensors • Biometric Access • Smart Cards	• 3D Packaging and High Density Substrates • Sensor and MEMS Packaging • Underfill/Encapsulants and Adhesives • Pb-free Solder Materials • Flip-Chip and Bumping Technologies • Fuel-Cell Packaging • Packaging for Extreme Environments • Advanced Interconnects and Wirebonding • Embedded and Integrated Passives • Advanced Ceramic and Conductive Materials • Cu/Low-K • Reliability

An example of SMT used in everyday life is mobile phones. Cell phones contain a number of SMT components within them. As their development has progressed, cell phones have more capabilities while still becoming smaller. Consumers demand higher mobility and more functions in their cell phones and the SMT industry has advances to respond to this. The progressing development of SMT devices has enabled the manufacture of smaller and more capable mobile devices. Cell phones are noted for their

use of Digital to Analog Converters (DACs) and Analog to Digital Converters (ADCs). The mouthpiece of the phone contains a microphone that captures the local sound waves and converts them into an analog signal. This analog signal goes to an ADC so the signal can be processed by microprocessors and relayed to a cell carrier's tower via radio signal. The signal is then relayed to another cell tower to the receiving cell tower, which relays the digital signal via radio to the receiving mobile device. The device takes this signal, sends it through the DAC to the speaker as an analog signal which is then converted into sound.

With creating smaller devices that can accomplish more, the power consumption per unit volume increases. Many mobile devices heat up over prolonged usage. Common storage places for these devices are in closed areas that do not allow much ventilation such as bags, purses, and pockets. With the smaller footprints and poor ventilation, overheating cell phone components are a legitimate concern.

Based on this background research and available information, the team focused its efforts on BGA CSPs and solder materials. This style of SMT offers many applications within a variety of industries. A wealth of technical information can be found regarding BGAs since they are prevalent and adaptable to diverse applications. Using this information, thermo-electric and structural simulations of various BGA components were conducted.

2. Methods Used

2.1 Design of Simulations

The team designed computations to determine which leadless chip carrier (LCC) packages perform best in terms of thermal management. This project's experiments are entirely simulated. This comes as a direct result of the small scale of the components chosen for the project. As undergraduate students, it is not possible to obtain the proper tools and equipment to analyze microtechnology such as BGA and QFN packages without damaging them. Also, a high level of precision is necessary to properly analyze and understand the behaviors of these packages. The team does not have access to state-of-the-art equipment designed for this purpose so computer simulations are the best solution.

2.2 Description of Simulation Methods

To start, the team collected samples from a number of companies specializing in manufacturing SMT and other electrical packaging. During that period, the team gathered materials data for different samples, solders, and printed circuit boards (PCBs). CES EduPack, a materials database program, helped to provide materials properties (Ashby, 1992; Cebon and Ashby, 1994; Young, 1989). A number of materials properties were found from other sources (ASM International Handbook Committee, 1989; Bauccio, 1993; Cverna,, 2002; Jackson and Schröter, 2000). Material declarations from manufacturers which previously provided samples were an informative resource (Analog

Devices, 2002A-2010C). The best and most accessible method for organizing this data was to put it all into a series of spreadsheets.

During the initial research and data collection phase, the team built models of existing IC packages in SolidWorks, computer-aided design (CAD) software. In general, the group focused on BGA and QFN models but later in the project switched to solely BGAs. The team attempted to import the models from SolidWorks into TAS several times unsuccessfully. At first the software was unable to open its own help menus. The team discovered that the version of TAS which is currently installed on the computers we are using is incompatible with Windows Vista. The operating system was preventing the help menus from opening. Soon after pinpointing the issue, patch was added to correct this. As time went on, the department updated the computers, rendering the help menus useless once more.

The project moved on, changing its methodology to creating nodes and using them to build the SMT packages within TAS itself. It quickly became apparent that not many professors or faculty are proficient with TAS anymore, which was difficult to overcome. This was in part to ANSYS's acquisition of TAS several years earlier, making the independent TAS software outdated. This is when the team made the decision to switch to a more current and effective simulation analysis software package. With minimal background in ANSYS 11, the group began to use that program instead. Similar to TAS, the user could not simply import complex three-dimensional models into ANSYS 11. While this would still be a challenge, a nodal approach seemed to be the only option. At this point, the department updated the programs available on lab computers so the team could no longer access ANSYS 11 and proceed with the latest approach.

Quickly, the group gained access to another lab that had ANSYS. Group members learned to use ANSYS 12 Workbench, the most current version of the software that had a much better user interface, to perform simulations. This program is capable of importing SolidWorks files saved into the Initial Graphics Exchange Specification (IGES) format, which saved time and made use of the models from previous efforts. The program was able to perform several types of thermal analysis, including electric, transient, and steady state. In addition to these, it allowed users to combine different types of analysis, such as electric-thermal and static structural in this case. It also enabled the team to use custom materials data while applying various thermal and structural loads such as initial temperature, voltage per connection, current between connections, heat flux, stress from the weight of the chip on the PCB, and so on. ANSYS 12 Workbench provides numerical solvers as well as visual solutions including color changes to signify high and low values for certain attributes and a view that shows deformation in structures. Both of these functions proved to be essential to the project.

After switching to ANSYS Workbench, more problems presented themselves. The next issue was learning to assign the materials properties within the ANSYS program. Materials and their properties acquired through CES EduPack can be recorded as Engineering Data into ANSYS Workbench. Unfortunately, the original models had been created as a single part, thus only one material could be applied to the model. Since there could not be multiple materials present in the model, each package would behave uniformly throughout which was of little use for the purposes of the project. The group found it difficult to apply these properties to the models created in SolidWorks. This problem was corrected by changing materials and their respective properties in

SolidWorks so that when models are imported into ANSYS, they retain these properties. This allowed the team to assign specific material properties directly to different components of the packages we modeled. Creating more accurate models, allows the group to gain a better simulation of the complex behaviors of small chips.

Currently we are facing a newer concern. Many of the chips that we are analyzing consist of silicon dioxide (SiO_2) resin. Silicon dioxide resin is not a material that is easily available to us through CES EduPack or the materials declarations provided to us from manufacturers. For now, we are modeling these parts as though they are made of SiO_2, not the resin.

These computer simulations tested different styles of BGA packages. The tests took many factors into account, including: array patterns, number and closeness of contact surfaces, materials, and manufacturing processes. The computer simulations were all performed in ANSYS Workbench. The team performed analysis on models of various BGA and QFN packages to determine their thermal management capabilities. Research showed that different patterns, arrays, and orientations of leads resulted in different levels of heat dissipation.

2.3 Description of Procedure

Several analysis systems are available for use in ANSYS Workbench 12. This project necessitated the use of the static structural system, but relied more heavily on the thermal-electric system. These systems were selected from the list and dragged into the project schematic as seen in Fig. 18. In Fig. 19, the first three components of both

systems were linked in these two systems. The engineering data, geometry are all the same between the two systems. Material properties of various metals and package types are used in both types of analysis. These properties were obtained through CES EduPack 2009. The analysis of both systems is performed on the same geometry and will be run with the same time and loads.

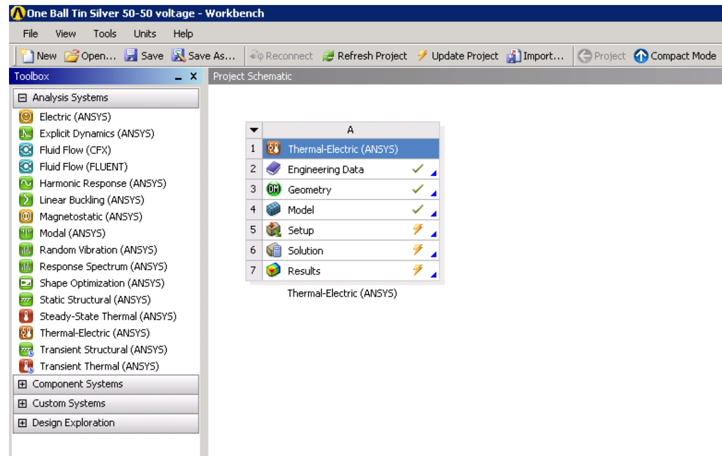

Fig. 18. Project schematic.

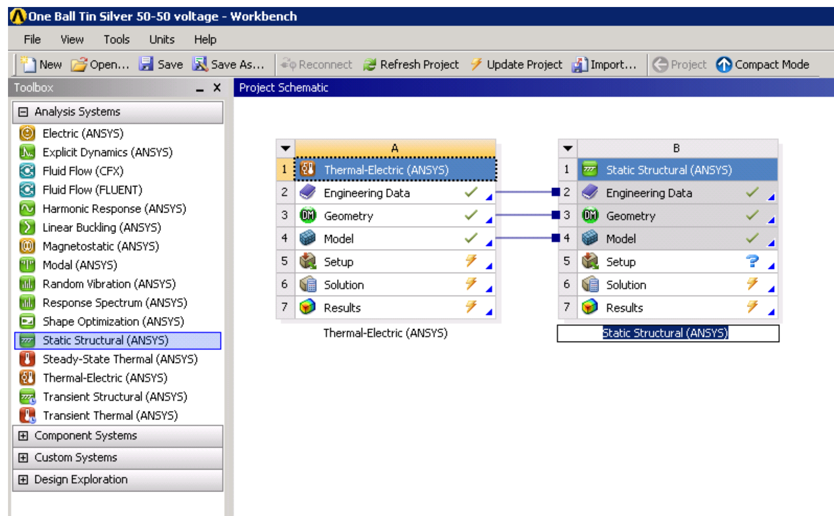

Fig. 19. Project schematic with linked systems.

In the first portion of the analysis, material properties were entered into the Engineering Data windows. The program has several predefined material libraries in which the user can easily select (Fig. 20). The user can create their own libraries of materials which can be seen in Fig. 21. Various properties were selected for their relevance to the analysis desired. For each material, the density, the coefficient of thermal expansion and its reference temperature, the isotropic elasticity in terms of Young's Modulus and Poisson's Ratio, tensile yield strength, compressive yield strength, isentropic thermal conductivity and isotropic resistivity were loaded into the program (Fig. 22).

Outline Filter

	A	B	C	D
1	Data Source		Location	Description
2	Engineering Data		A2, B2	Contents filtered for Thermal-Electric (ANSYS), Static Structural (ANSYS).
3	General Materials			General use material samples for use in various analyses.
4	General Non-linear Materials			General use material samples for use in non-linear analyses.
5	Explicit Materials			Material samples for use in an explicit anaylsis.
6	Hyperelastic Materials			Material stress-strain data samples for curve fitting.
7	Magnetic B-H Curves			B-H Curve samples specific for use in a magnetic analysis.
8	MQP materials			
9	Favorites			Quick access list and default items
*	Click here to add a new library		...	

Fig. 20. List of material libraries.

Outline of MQP materials

	A	B	C	D	E
1	Contents of MQP materials	Add		S..	Description
2	Material				
3	60-40 Tin Lead				
4	63-37 Tin Lead				
5	70-30 Tin Lead				
6	Silica				
7	Tin Silver				

Fig. 21. List of materials in user-made library.

Properties of Chart : Density 60-40 Tin Lead

	A	B	C
1	Property	Value	Unit
2	Density	8600	kg m^-3
3	Coefficient of Thermal Expansion		
4	Coefficient of Thermal Expansion	2.5E-05	C^-1
5	Reference Temperature	25	C
6	Isotropic Elasticity		
7	Young's Modulus	3.2E+10	Pa
8	Poisson's Ratio	0.4	
9	Tensile Yield Strength	6E+07	Pa
10	Compressive Yield Strength	4E+07	Pa
11	Isotropic Thermal Conductivity	60	W m^-1 C^-1
12	Isotropic Resistivity	1.6E-07	ohm m

Fig. 22. Material properties chart and values.

Any properties associated with files imported into ANSYS will not be retained and must be applied in ANSYS. Otherwise, the program will assume that the material is structural steel and will greatly alter the subsequent solutions.

Reference temperatures for each property of each material needed to be defined as seen in Fig. 23. If this is not done, temperature ranges in the solution will be unrealistic.

Temperatures will range from beyond absolute zero and above the melting temperatures of both the package and solders.

Table of Properties Row 2: Density

	A	B
1	Temperature (C)	Density (kg m^-3)
2	25	8600

Fig. 23. Property data table with reference temperature.

The CAD model of the BGA can be imported into the project in the geometry window as seen in Figure 24. In the file menu, the import external geometry option, shown in Fig. 25, allows the user to import IGES files created in a CAD program such as SolidWorks.

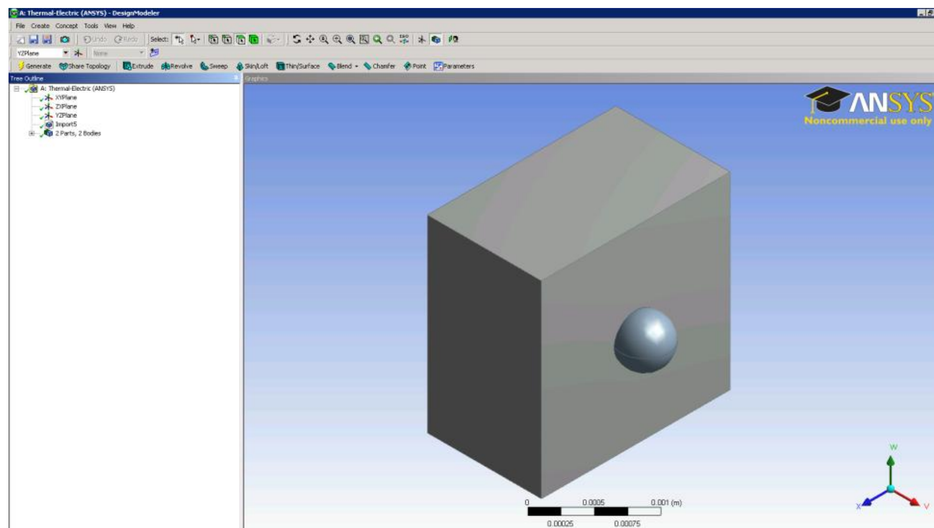

Fig. 24. Geometry window.

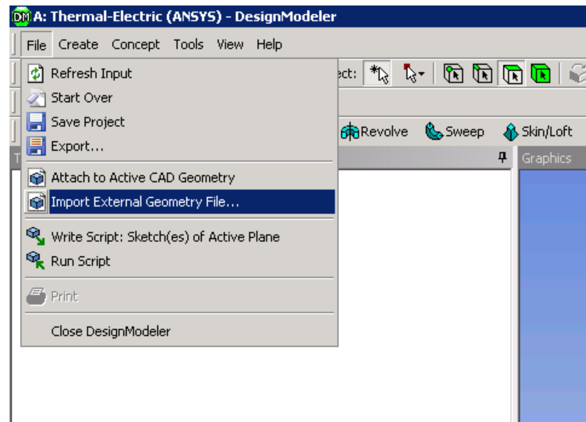

Fig. 25. Import external geometry option in File menu.

The model window, depicted in Fig. 26, is where particular loads are applied to specific points surfaces and bodies on the model uploaded into the project. Underneath the geometry option, each body within the assembly is listed. Here, different bodies can be assigned to particular materials and the associated properties.

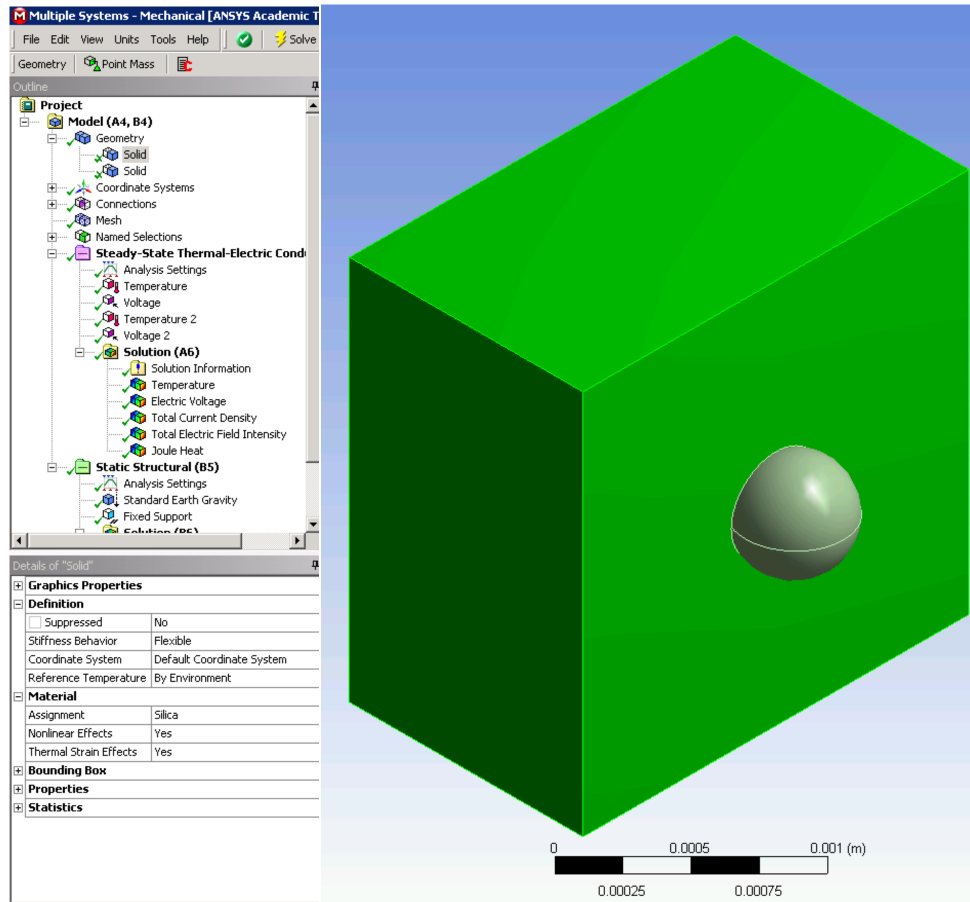

Fig. 26. Geometry window with body selection.

Parameters of the analysis are defined within the analysis settings option in each of the systems' folder, Fig. 27. The number of steps is defined along with the length of each of these steps. The primary loads in the thermal-electric module were voltage and temperature applied to the surface of the solder ball and outer surface of the package. Loads can be constant over the course of the analysis, or can be dictated in the tabular data tab. In the solution folder, specific types of solutions can be selected and calculated for when the project is asked to solve.

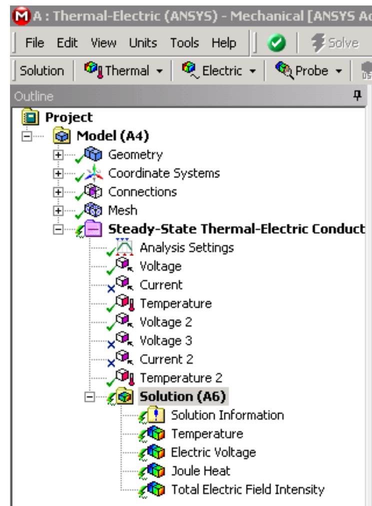

Fig. 27. Example system, loads and solution folders.

To further investigate the effect of the various loads on the BGA, section planes can be added to view interior cross sections as demonstrated in Fig. 28. The behavior of the material can be further investigated by observing and comparing the locations of minimum and maximum values in these cross sections after the system is solved.

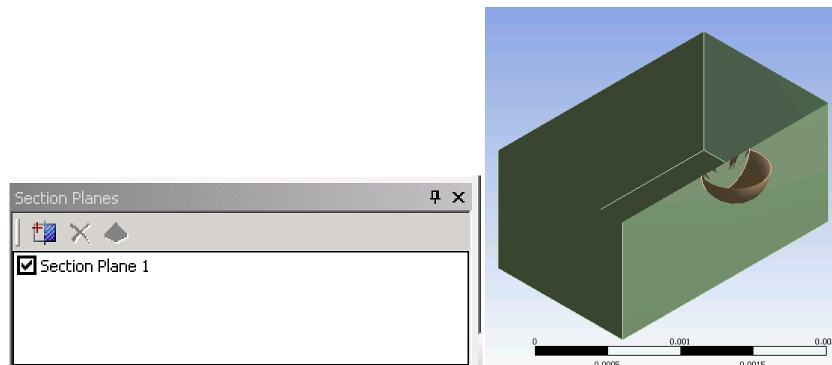

Fig. 28. Section plane option and example.

After initiating the solve procedure, the Solution Information folder, shown in Figure 29, will indicate which step of the process that it is currently evaluating under the load step

options. Any errors and warnings the program may encounter are also recorded in this page and can be used for troubleshooting.

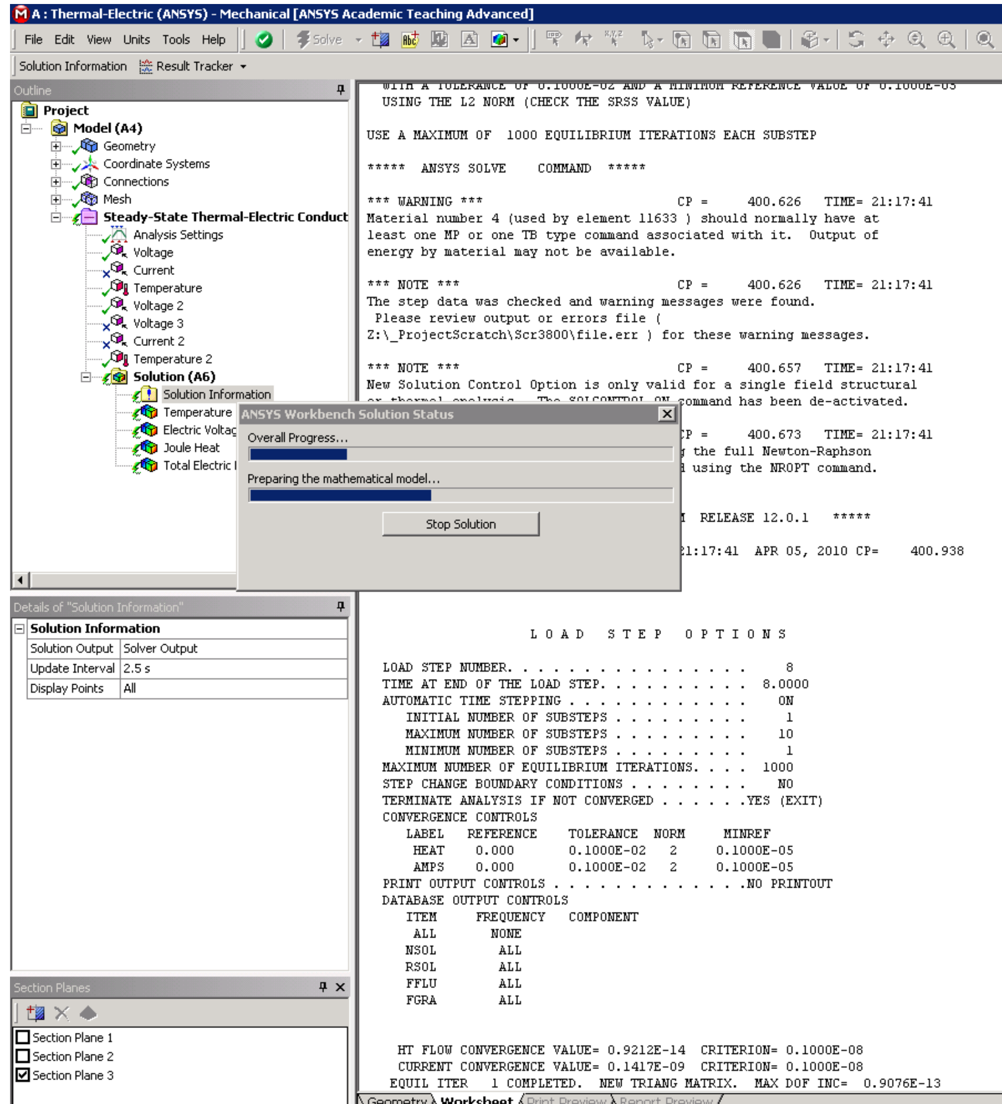

Fig. 29. Solution information and progress folder.

After the program has reached a solution, tabular data, minimum and maximum values, and colored contour plots of value distribution for each type of solution, as can be seen in Fig. 30.

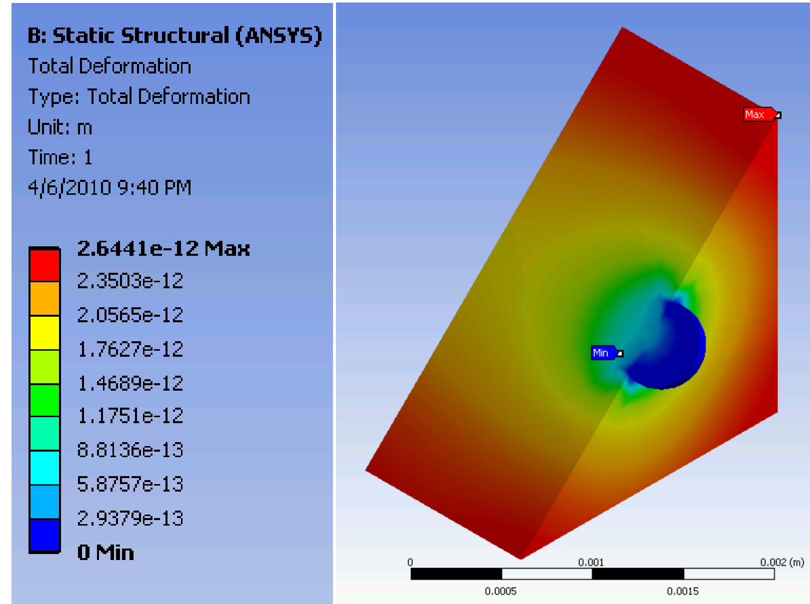

Fig. 30. Screenshot of example results.

Using the procedure outlined in the methodology section, the team developed several tests to adequately observe the behavior of heat within several types of BGAs. Initial tests to develop procedure and troubleshoot earlier problems were conducted with a single ball and proportioned package to determine the functionality of test systems with realistic loads. The dimensions of the single-ball model are shown in Fig. 31. The single-lead tests were run testing four types of solder to ascertain if ANSYS could calculate minute differences between materials.

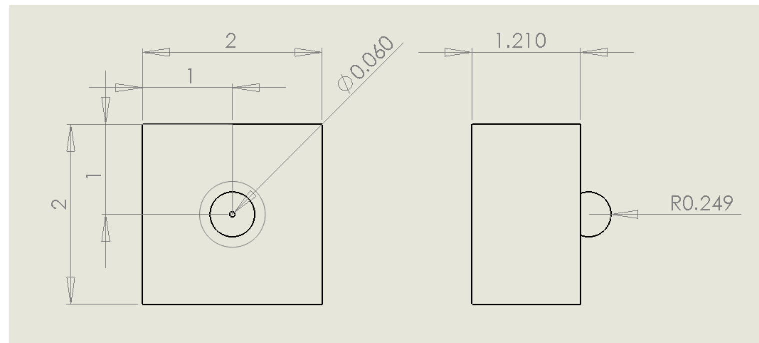

Fig. 31: Bottom and side dimensions of single-lead BGA in mm.

Most tests were done with a 256-lead BGA, modeled after Analog Devices' part numbered AD6636 whose dimensions are shown in Fig. 32 (Analog Devices, 2005A). As with most Analog Devices' parts, there are extensive data sheets available regarding the function, dimensions, and performance of AD6636. AD6636 is one of the larger BGA products that Analog Devices produces with a full array. After observing unexpected behavior in each quadrant of the 256-lead BGA, the team simulated a 64-lead utilizing the same package thickness, lead diameter, and distance between each lead, resulting in an independent package one quarter of the size of the original test (Figure 33). The 256-lead and the 64-lead models underwent simulations testing the effect varying voltage, temperature, and material has on the overall temperature and its distribution.

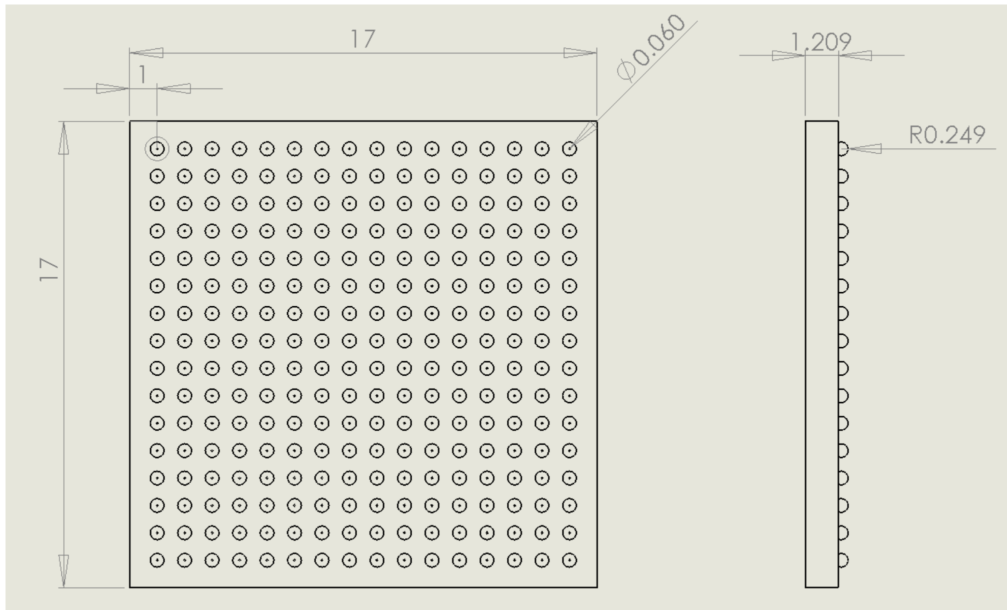

Fig. 32. Bottom and side dimensions of AD6636 (256-lead BGA) in mm.

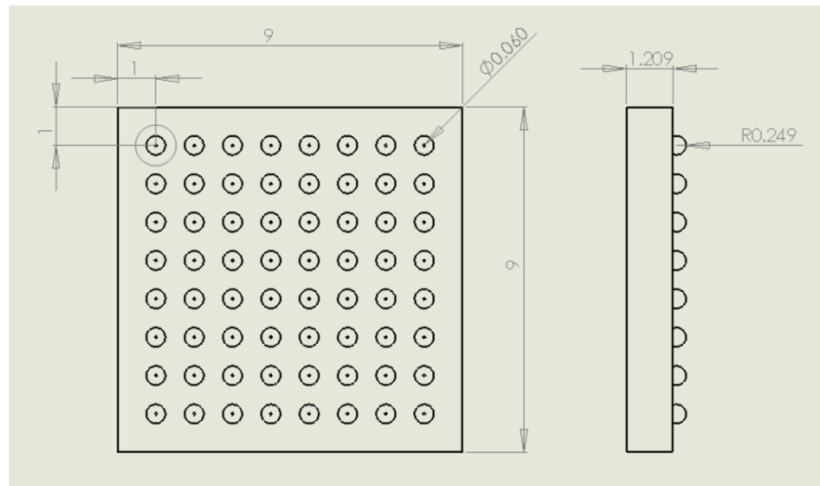

Fig. 33. Bottom and side dimensions of 64-lead BGA in mm.

The majority of the simulations define the outer 5 faces of the package (all faces excluding the carrier side face which connected with the leads) at a constant temperature of 22°C. In later simulations, the outer temperature was not regulated to observe the effects on the environment for each of the tests was kept at 22°C.

For most tests not involving voltage as a factor, BGAs were initially tested around 5V but was then decreased to 0.25V in later tests after observing temperature values above the recommended operating temperatures defined for many of Analog Devices' data sheet (Analog Devices, 2002A-2010C). The outer package was defined as 0V under the assumption that the external package is electrically neutral and acts as an insulator. In the 256-lead simulations, the surfaces for voltage application were divided into four 64-lead quadrants, only because selecting all 256 surfaces simultaneously and correctly proved to be a challenge in itself.

Some structural deformation tests were conducted upon the 256-lead BGA. Each of the BGA models has small, flat surfaces on each of the solder which were defined as fixed supports. Standard atmospheric pressure was applied to the package. Standard gravity was defined to be acting in the direction from the blank side of the package to the side with the leads, Fig. 34, essentially mimicking the effects of gravity if the BGA was sitting on a table.

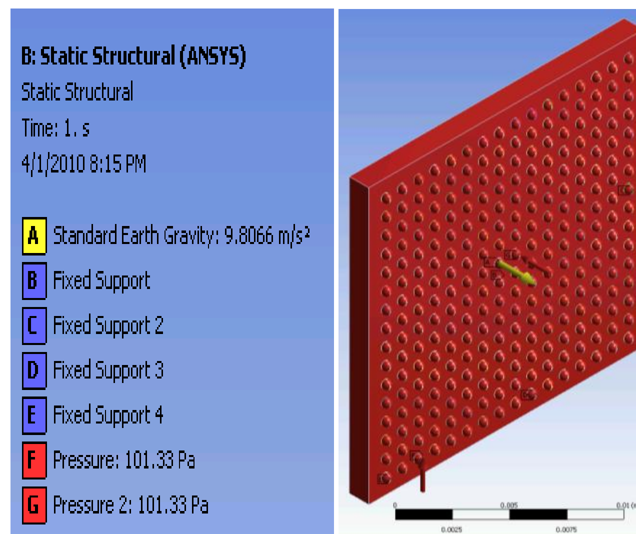

Fig. 34. Initial conditions of structural 256-lead test.

3. Facilities

This project required computers with certain software packages on them to simulate the thermal and structural conditions of BGA and QFN packages of various orientations. Such software included SolidWorks 2009, CES EduPack 2009 and ANSYS 12 Workbench Academic Edition.

The team also used samples from two companies in order to become more familiar with different kinds of SMT electrical components. These samples came from Analog Devices and ST Microelectronics. Several of the products available from Analog Devices are shown in the Appendix A to illustrate the diversity of components used for research and modeling in this project.

4. Results and Discussion

When using the temperature as the independent variable, the distribution of heat maintains the same pattern throughout the series when increased by 5 degrees each time. The full pattern of the heat distribution appears as it does in Fig. 35. Subsequent temperature screenshots have been cut down to show the upper left 10x10 array since each of the trials demonstrated symmetry across each of the 8x8 lead quadrants.

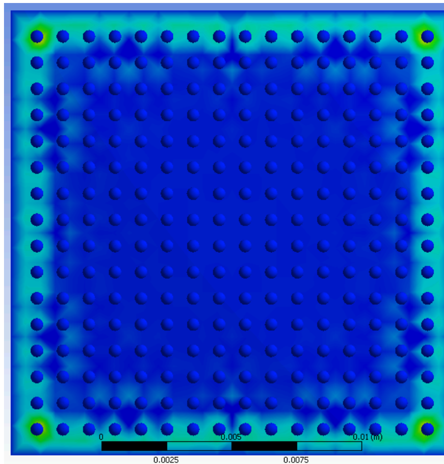

Fig. 35. Typical heat distribution in a 256-lead BGA.

During simulations that varied the temperature applied on the leads. Only when the temperature is at 47°C or higher did the bottom of the package even out in temperature, compared to the cooler trials where heat was concentrated along the perimeter and corners. The minimum temperature peaked at 22°C when the applied temperature exceeded 42°C as seen in Table 5. While the minimum of 22°C is expected, values below 22°C are unexpected since there are no cooling agents within this system which may be a product of the program. The function describing the minimum temperature can be seen in Fig. 36 where a cubic trend line was fit to the minimum

temperature values. In every case, the perimeter leads are the ones that experience the highest temperatures.

Table 5. Table of applied lead temperature and resulting values for 256-lead BGA.

Lead temp.	Temp. (°C)		Voltage (V)		Electricity field (V/m)		Joule heat (W/m3)	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
22	-15.051	603.58	0	5.092	4.96E-10	11066	3.13E-12	1.39E+13
27	3.9083	378.3	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12
32	8.8413	383.18	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12
37	13.774	388.06	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
42	18.707	392.95	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
47	22.000	397.83	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
52	22.000	402.71	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
57	22.000	407.59	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
75	22.000	425.17	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
100	22.000	449.58	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12

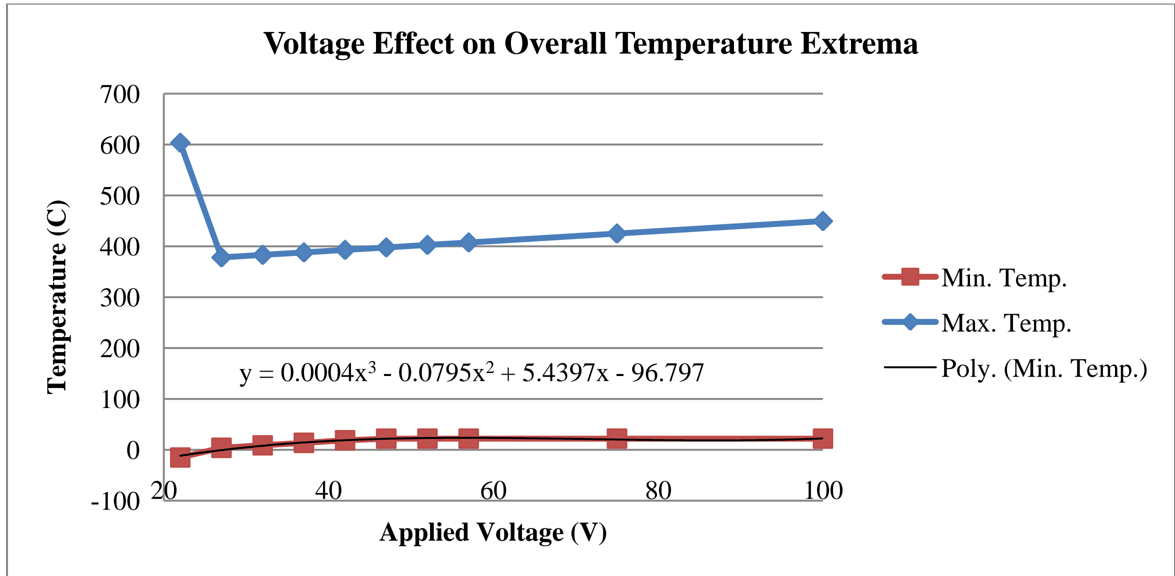

Fig. 36. Graph of min. and max. 256-lead BGA temperatures in relation to voltage.

Figs. 37 through 46 show the temperature distribution of one quadrant from each of the temperature trials. The maximum temperatures increased linearly, but the

distribution remained consistent until temperatures at or above 57°C. The lead-side of the chip demonstrated more even heat distribution than the lower temperature simulations.

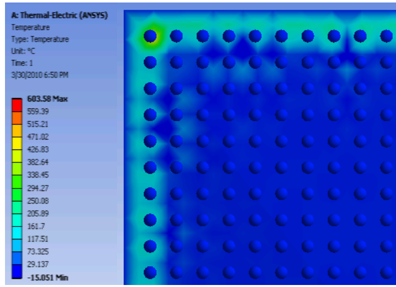

Fig. 37.22°C trial on 256-lead BGA.

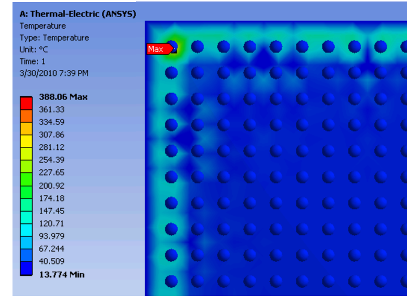

Figure 41: 42°C trial on 256-lead BGA.

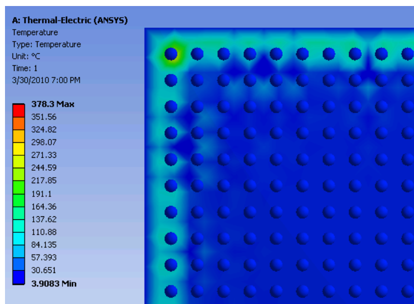

Fig. 38. 27°C trial on 256-lead BGA.

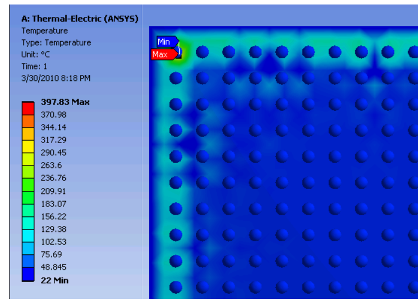

Fig. 42. 47°C trial on 256-lead BGA.

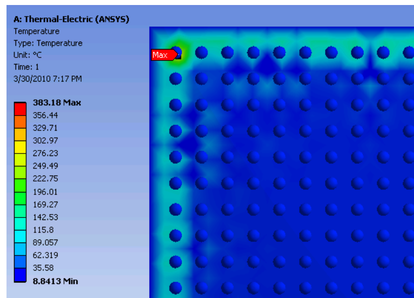

Fig. 39: 32°C trial on 256-lead BGA.

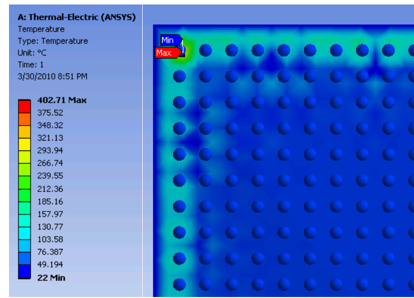

Fig. 43: 52°C trial on 256-lead BGA.

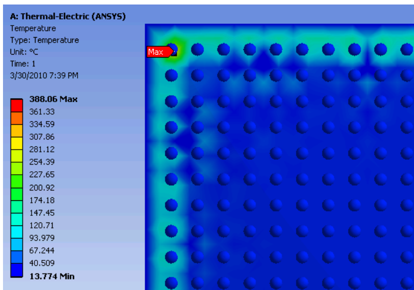

Fig. 40. 37°C trial on 256-lead BGA.

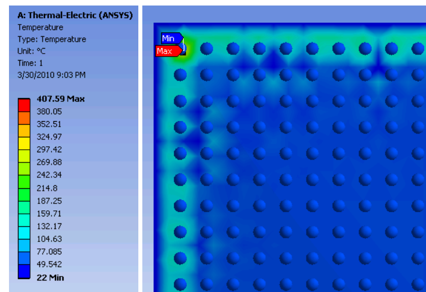

Fig. 44. 57°C trial on 256-lead BGA.

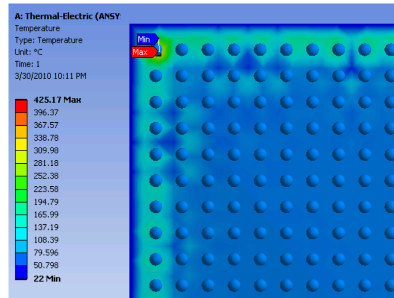

Fig. 45. 57°C trial on 256-lead BGA.

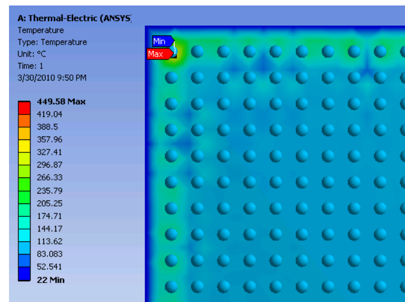

Fig. 46. 100°C trial on 256-lead BGA.

Each of the corner leads exhibit a loop like pattern internally. The loop has the highest temperature in the area closest to the center of the chip package and at the junction between the lead and the package. The highest temperature of the silica substrate occurs at the corner ball junction but does not exhibit as much heat as the loop within the solder ball as seen in Fig. 47. When applying 27°C to the solder leads, the heat loop is approximately 100°C greater than the closest and warmest silica package. We have not found any data or previous research that would indicate the causation for the occurrence of this heat loop.

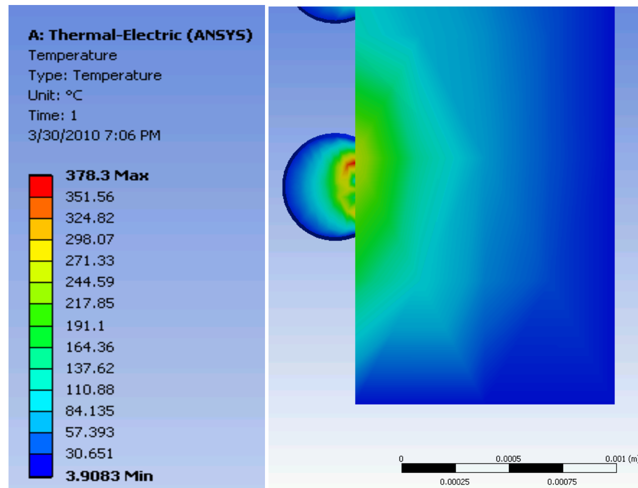

Fig. 47. Internal heat loop in corner lead of 256-lead BGA.

Altering the temperature applied to each of the lead surfaces does not change the voltage, total electric density, or Joule heat distribution and magnitude across the chip. This is expected since voltage (*V*) is a product resistance (*R*) and current (*I*). Temperature is not involved in this relationship and would have no bearing on the electrical performance of the component.

$$V = I * R. \tag{4}$$

Another test was run using 22°C as the ambient and as the outer package temperature for a 64-lead BGA, but applied 27°C and 0.25V on each of the leads. This was done with each of the four solders of which the group had sufficient material properties. Tin silver experienced the lowest maximum temperature at 27.396°C, but the eutectic 63Sn37Pb solder was the one that exhibited the highest temperature at 27.435°C (Fig. 48). The difference between each of these is minimal and would not impose any immediate concerns, but over prolonged usage, this could be a major issue. The slightest increase in temperature and thus thermal expansion in one cycle can result in a dramatic

increase in the stresses experienced by the solder joints over the lifetime of the part. This small increase indicates that part would reach its failure point sooner, making the component less reliable.

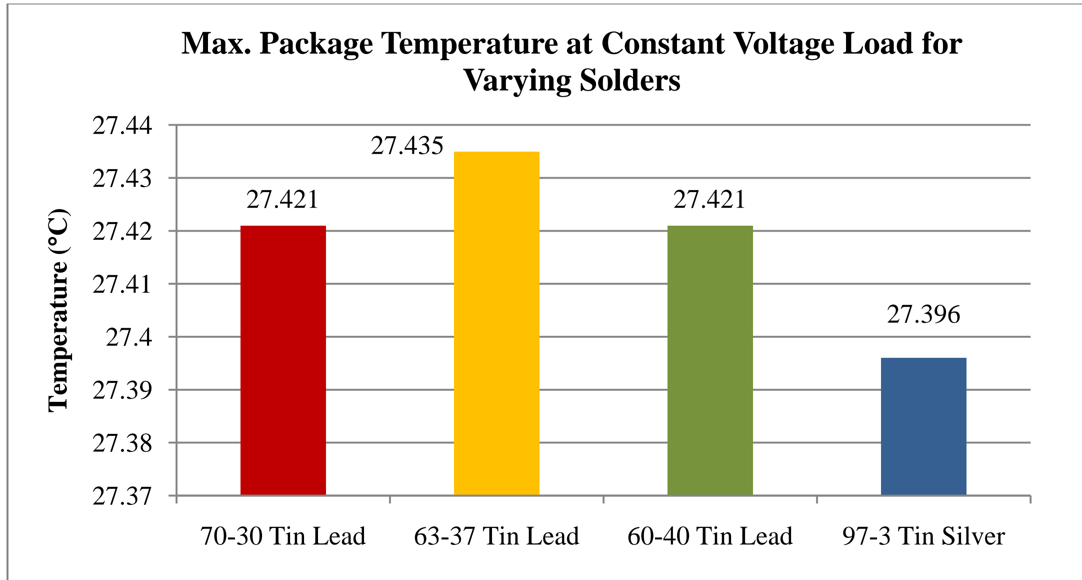

Fig. 48. Maximum temperatures for varying solders in 64-lead BGA.

Altering the voltage alters all four simulated values across the BGA when all other variables are held constant shown in Table 6. During the 256-voltage trials, the maximum temperature increased exponentially. When fitting a trend line to the data, the cubic function demonstrated the highest correlation to the given data points found in Fig. 49. In the lower voltage trials (the ones below 1V) exhibited the most evenly distributed heat along the lead-side of the chip. In each of these trials, the minimum voltage value was 0V as expected, but the experienced voltage of the package was minimally greater in the 256-lead tests, for which the group cannot account. Figure 50 demonstrates that the relationship between the applied voltage and maximum voltage experienced by the

package is a positive linear relationship, but not a slope of one as expected. The maximum voltage for each simulation is slightly higher in each test than the applied voltage. This phenomenon did not repeat itself in the 64-lead trials of temperature, voltage or material variations. Screenshots of the heat distribution of the voltage trials can be found in Figs. 51 through 59. The lower voltage figures include a diagonal cross-section of the corner lead, which also show the same loop that occurred in the temperature simulations

Table 6. Summary of applied voltage data on a 256-lead BGA

Applied Voltage	Temp. (CC)		Voltage (V)		Electricity Field (V/m)		Joule heat (W/m3)	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
0.25	22.000	27.831	0	0.25446	2.35E-11	553.31	7.82E-15	2.45E+10
0.5	22.000	30.396	0	0.50920	4.96E-11	1106.6	3.13E-14	9.79E+10
0.75	22.000	34.789	0	0.76381	7.46E-11	1659.9	7.04E-14	2.20E+11
1	22.000	40.939	0	1.0184	9.92E-11	2213.2	1.25E-13	3.91E+11
2	22.000	83.109	0	2.0368	1.98E-10	4426.5	5.01E-13	1.57E+12
3	18.644	153.39	0	3.0552	2.98E-10	6639.7	1.13E-12	3.52E+12
4	12.197	251.79	0	4.0736	3.97E-10	8853.0	2.00E-12	6.26E+12
5	3.9083	378.30	0	5.0920	4.96E-10	11066	3.13E-12	9.79E+12
10	-65.166	1432.6	0	10.184	9.93E-10	22132	1.25E-11	3.91E+13

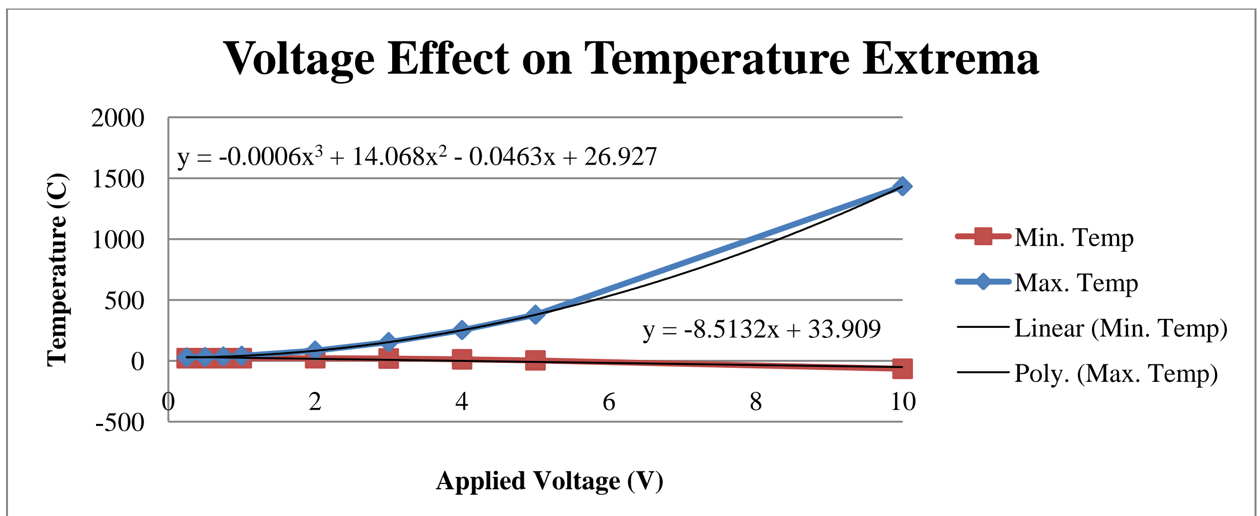

Fig. 49. Voltage v. temperature in a 256-lead BGA.

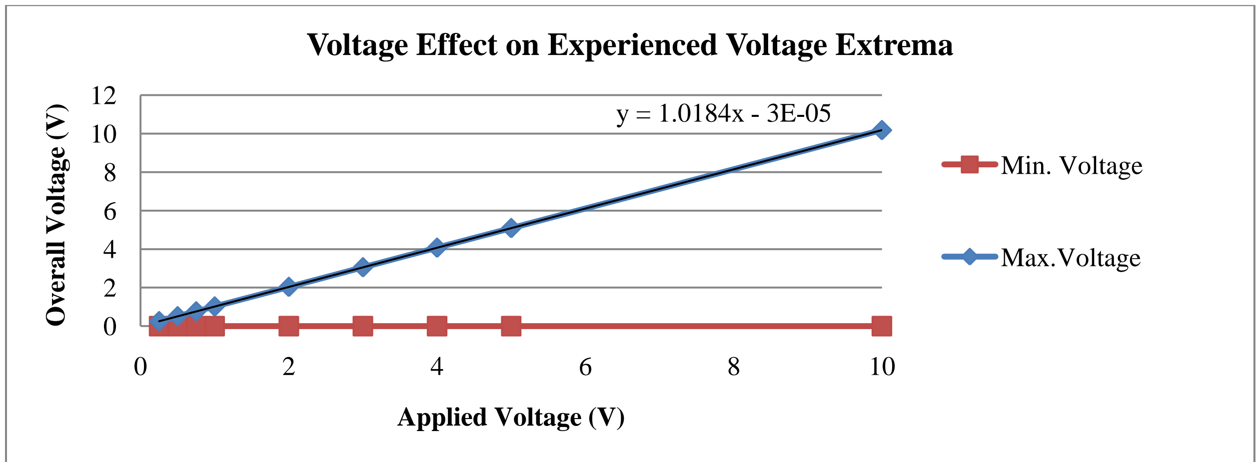

Fig. 50. Voltage v. experienced voltage in a 256-lead BGA.

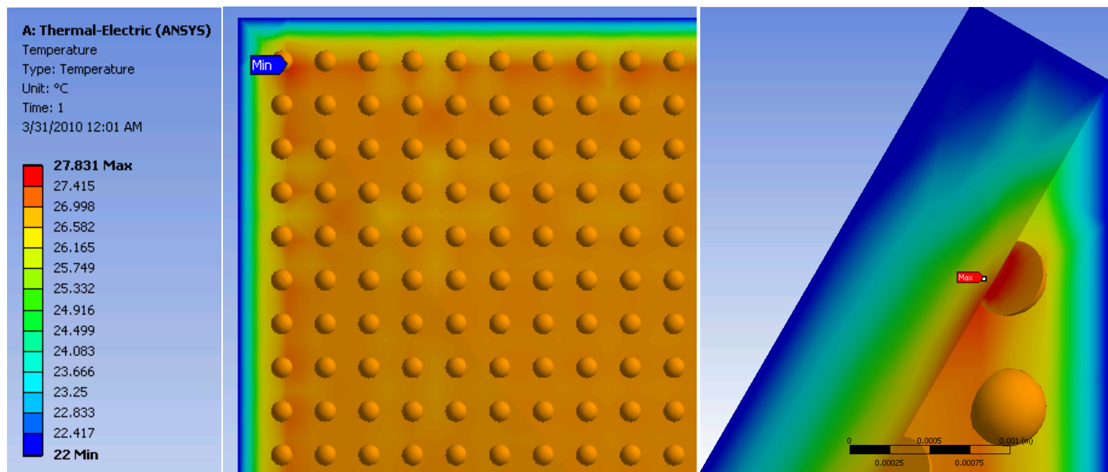

Fig. 51. 0.25V trial on 256-lead BGA.

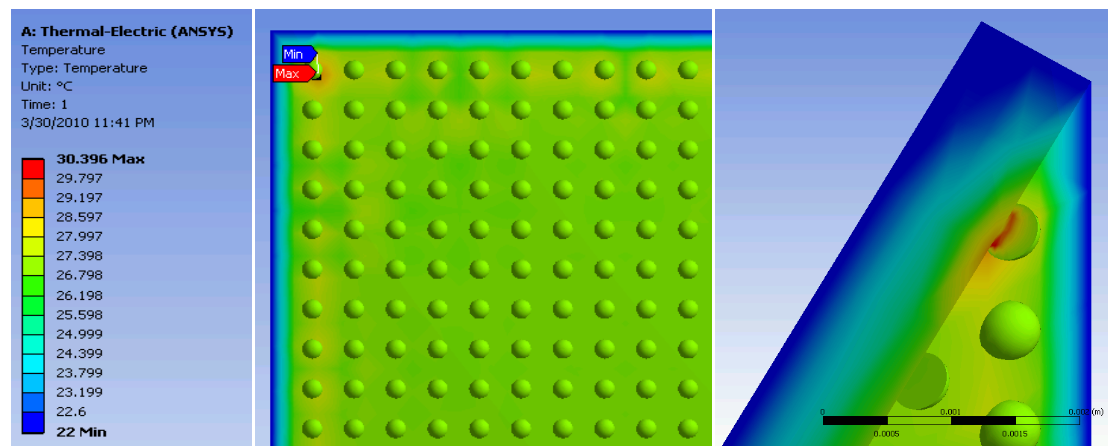

Fig. 52. 0.5V trial on 256-lead BGA.

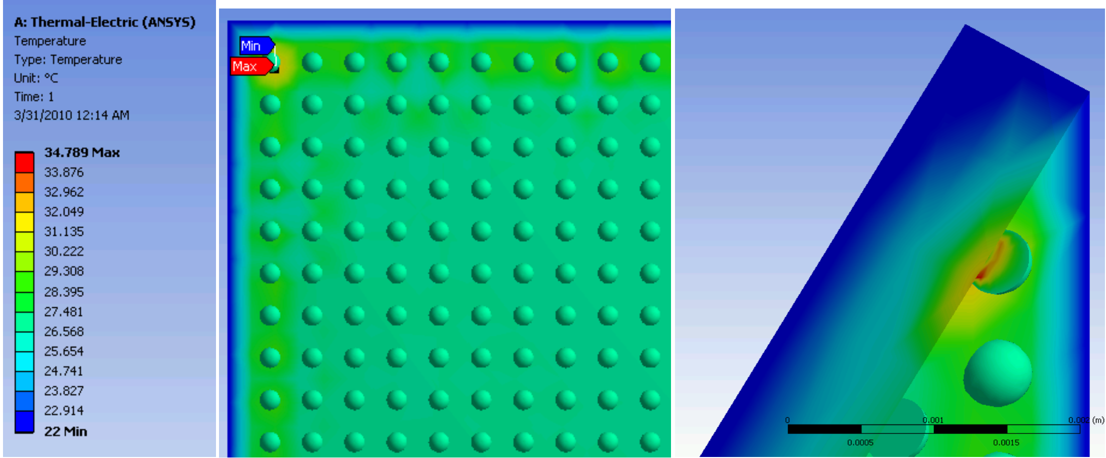

Fig. 53. 0.75V trial on 256-lead BGA.

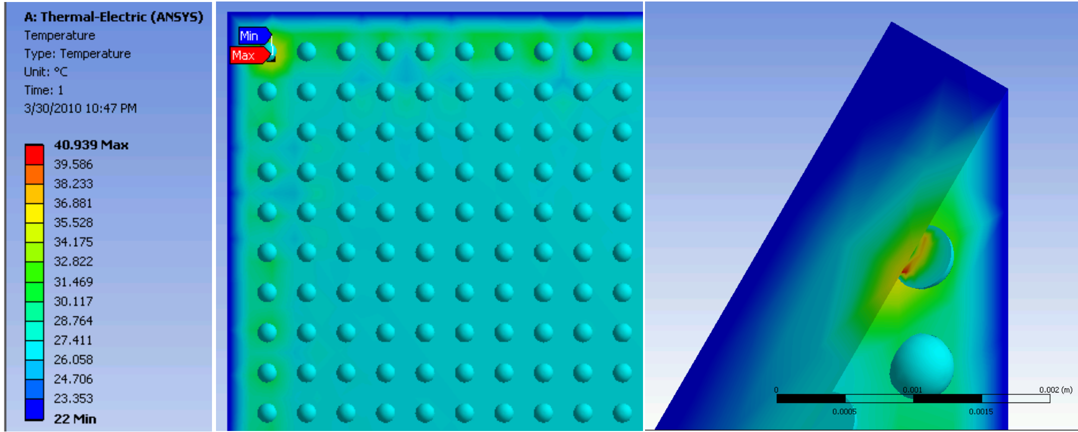

Fig. 54. 1.0V trial on 256-lead BGA.

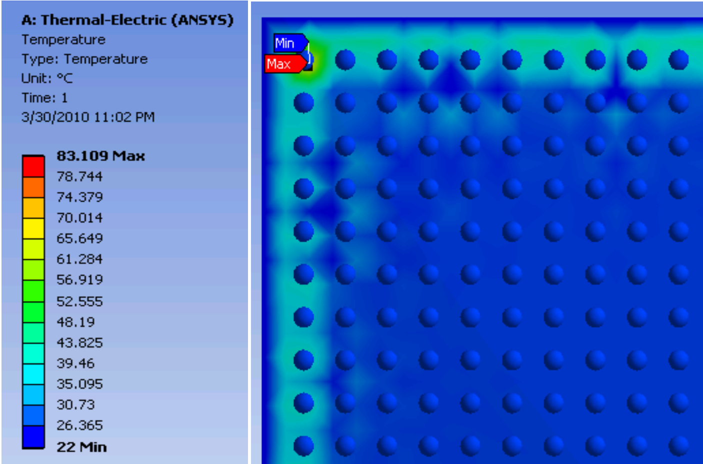

Fig. 55: 2.0V trial on 256-lead BGA.

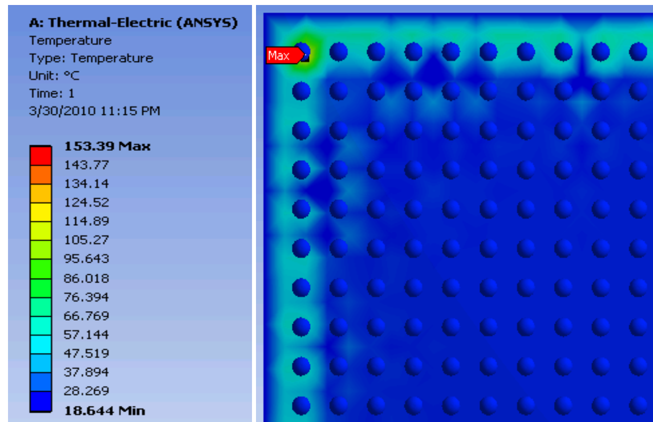

Fig. 56. 3.0V trial on 256-lead BGA.

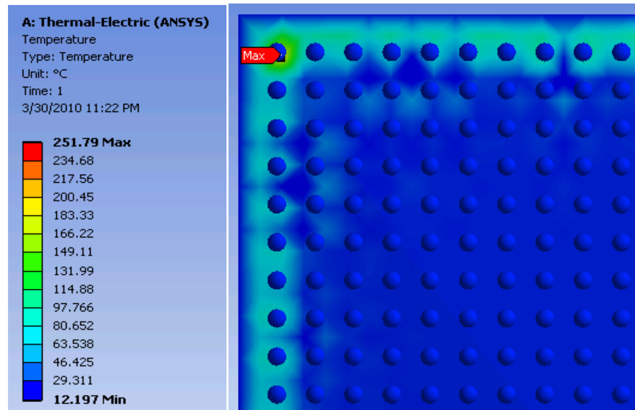

Fig. 57. 4.0V trial on 256-lead BGA.

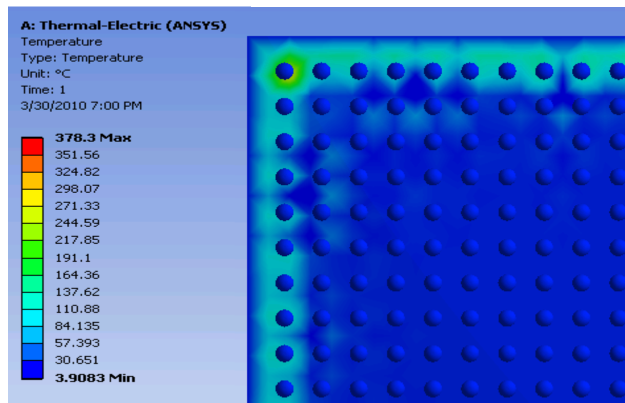

Fig. 58. 5.0V trial on 256-lead BGA.

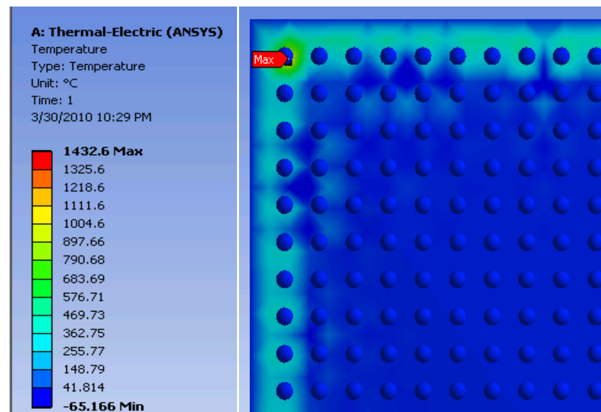

Fig. 59. 10.0V trial on 256-lead BGA.

When any amount of voltage was applied to the leads, it distributed consistently and evenly in every trial. The carrier-side of the package experienced the greatest amount of voltage and the outer portion, which was defined as 0V, had the lowest voltage as expected. The 256-lead trials exhibited the same behavior as the 64-lead trials (Fig. 60, 61 and 62). This even distribution could be a result of using encapsulation and our disregard of the internal aspects of the package. In each of these trials, two corners, always opposite from each other, are much cooler than the other two corners. In Fig. 60, this phenomenon can be seen in the upper left and lower right corners of the package. The 64-lead BGA simulations also followed this trend in Fig. 62. This may also have been a result of the limitations of the academic license of ANSYS Workbench, specifically the limitations on the quantity of nodes allowable for the mesh. Note that the voltage correlates more with the edge of the packaging rather than the lead surfaces where the original voltage was applied.

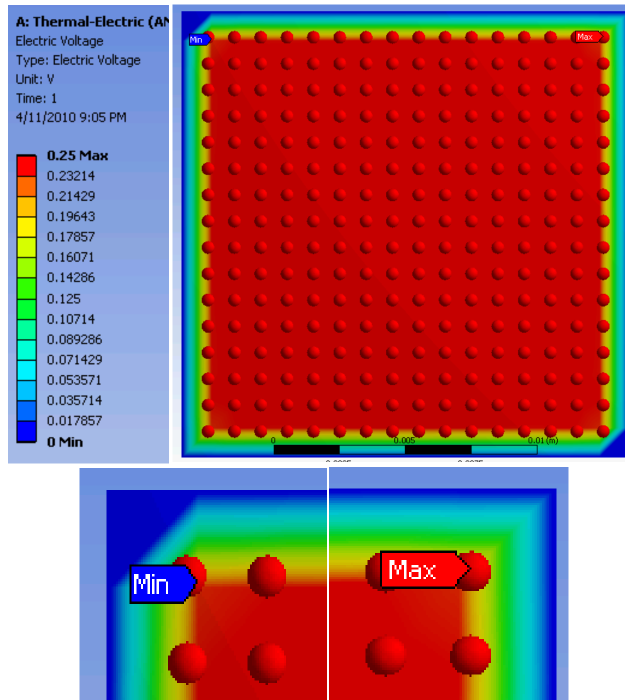

Fig. 60. Example voltage distribution on a 256-lead BGA.

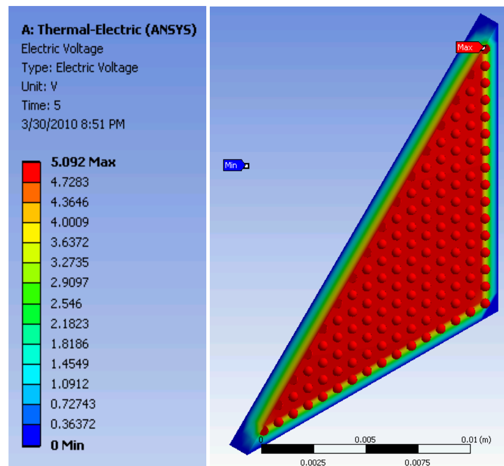

Fig. 61. Diagonal cross section of voltage distribution on 256-lead BGA.

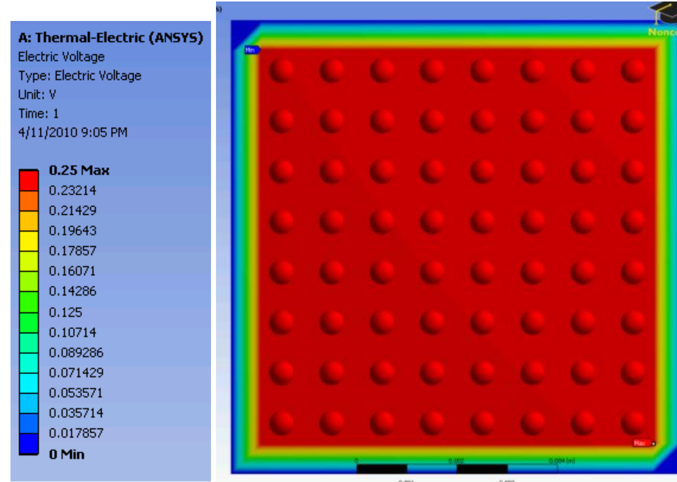

Fig. 62. Example voltage distribution on a 64-lead BGA.

Electric field intensity concentrates at the lead-side edges of the packages but not at the corners. Electric density, can be expressed as the ratio between the electrical impedance (Q) and the cross sectional area (A):

$$\frac{Q}{A} = electric\ density\ = \frac{\Omega}{m^2}. \tag{5}$$

The corners on the top of the package actually experience the minimum values of electric field intensity shown in Fig. 63. The pattern seen in Fig. 63 is consistent with the 64-lead trials which also exhibit the same areas of maximum and minimum values of electric field intensity. Fig. 64 shows a positive linear relationship between the applied voltage and the maximum electric intensity.

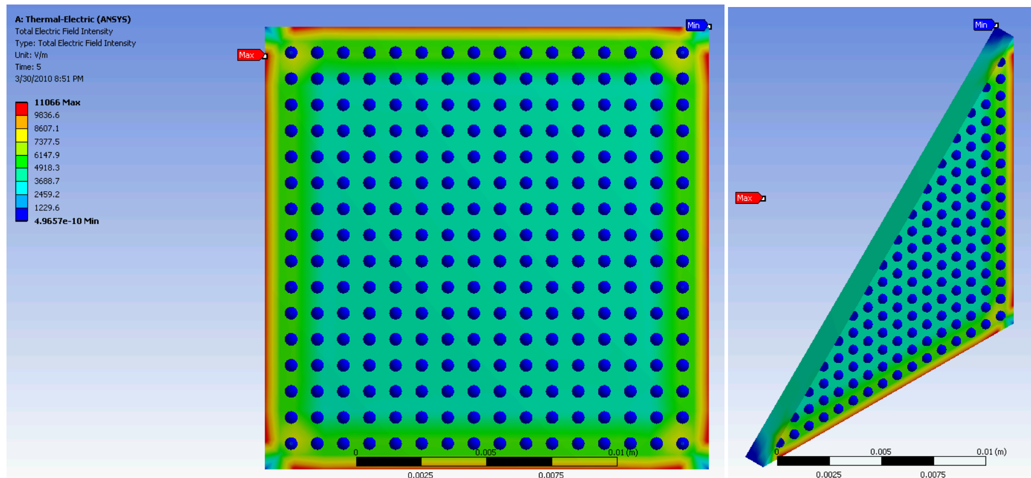

Fig. 63. Example of electric field intensity results in a 256-lead BGA.

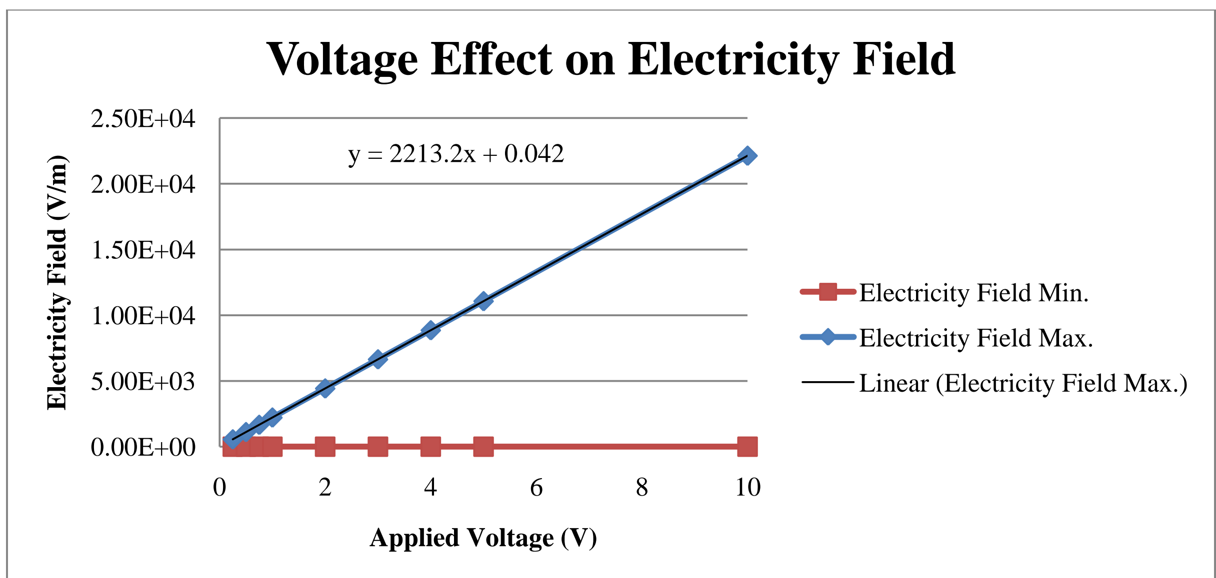

Fig. 64. Voltage effect on electric field density256-lead BGA.

Joule heat is proportional to the product of resistance and the square of current, the ratio of voltage to the resistance:

$$Q \propto I^2 * R. \tag{6}$$

The majority of the package initially appears as though it does not experience any variance in the Joule heat, but upon closer inspection of the lead-package joints, larger

values of heat can be found , as seen in Fig. 65. Joule heat is concentrated along the package-lead joint and has greater intensity on the perimeter and corner leads. The BGA experiences the greatest amount of Joule heat at the solder ball-package junction, with the maximum occurring on the corner leads, furthest away from the center of the package. The Joule heat appears in blocks, but this is most likely due to the limitation of the mesh size of academic license of the software. A cross section of one of the perimeter rows can be seen in Fig. 66, where the maximum values can be seen on either of the corner leads. The highest values of $9.8*10^{12}$ W/m^2 were at the wedge within the solder ball closest to the package corners. The overall effect of voltage on Joule heat can be seen in Fig. 67.

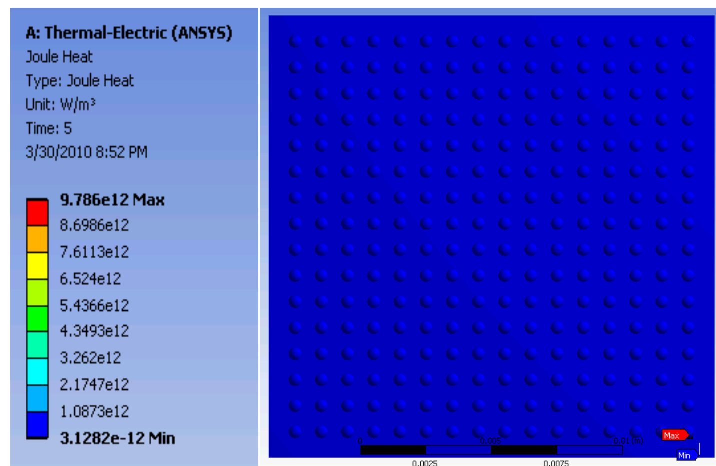

Fig. 65. Joule heat distribution in 256-lead BGA.

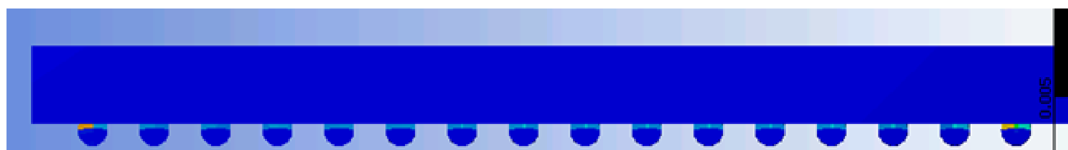

Fig. 66. Perimeter cross section of Joule heat in 256-lead BGA.

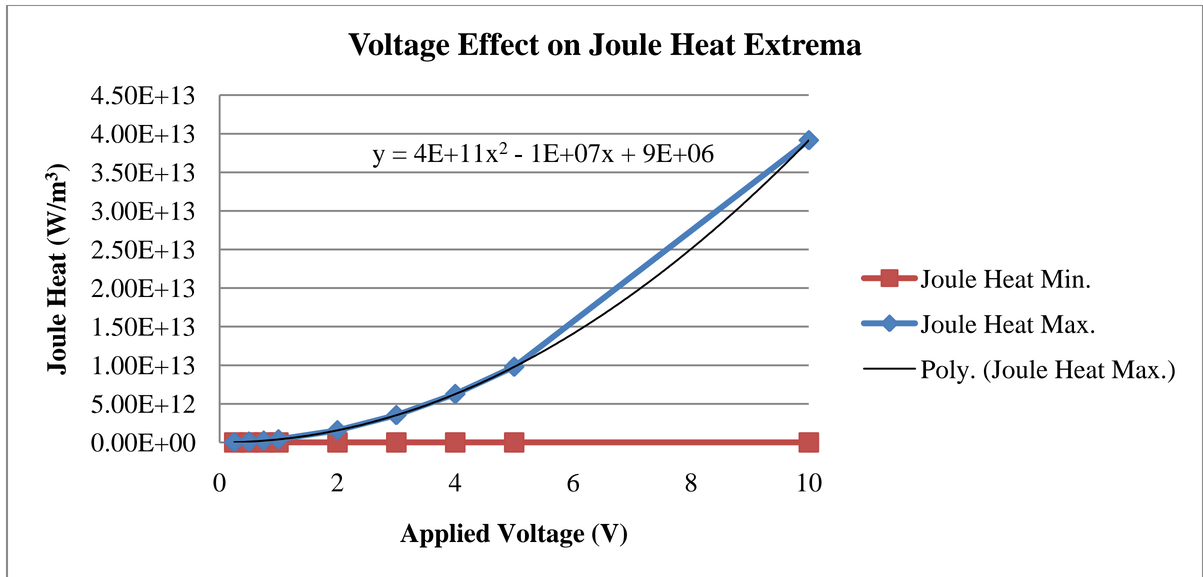

Fig. 67. Effect of varying voltage on joule heat in a 256-lead BGA.

Further trials were conducted to better imitate the convection a package would have by not maintaining the temperature of the outer package at 22°C. Fig. 68 indicates all the minimum and maximum temperatures for each of the solders. These maximum values reflect what was done in earlier testing. Fig. 69 demonstrates the common distribution of heat in each of these material trials along with a diagonal cross section of a corner lead which also has a heat loop that appeared in previous tests, which can be seen in the upper right view. The coldest temperatures of 25.3°C occur in four places near the corners, but on only two of the side faces of the package. On the other two sides, the cold spots are not as cold as the other four. The lower right view in Fig. 69 shows an example of this behavior.

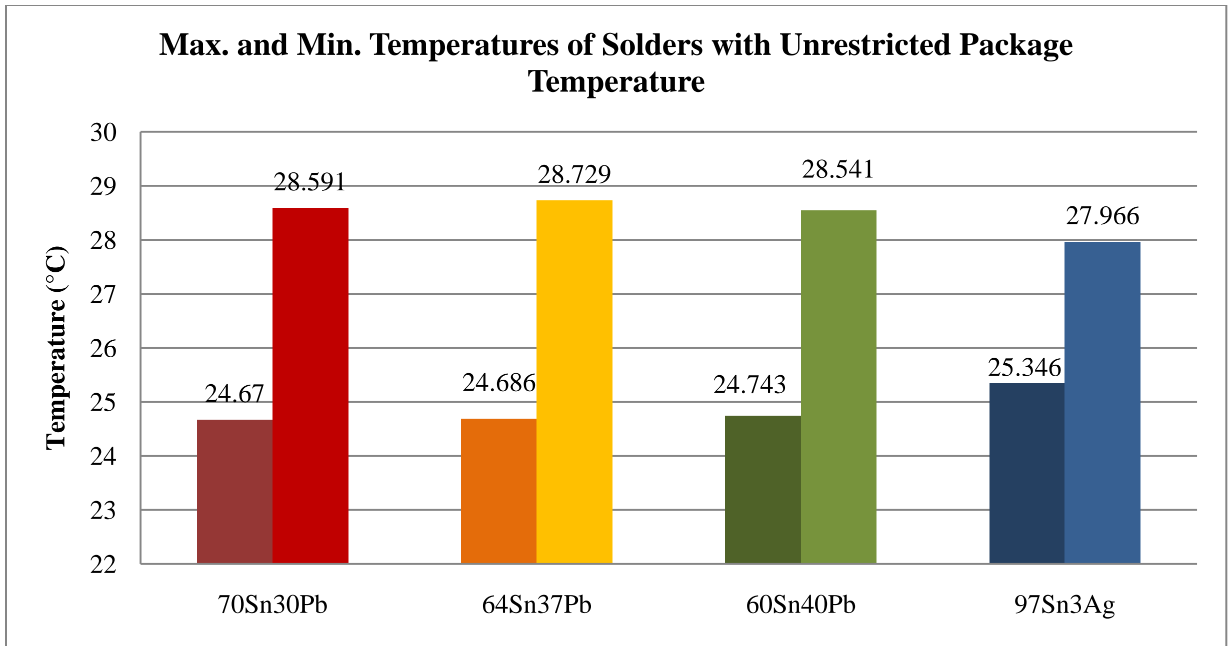

Fig. 68: Unrestricted package temperature comparison of different lead materials of a 256-lead BGA.

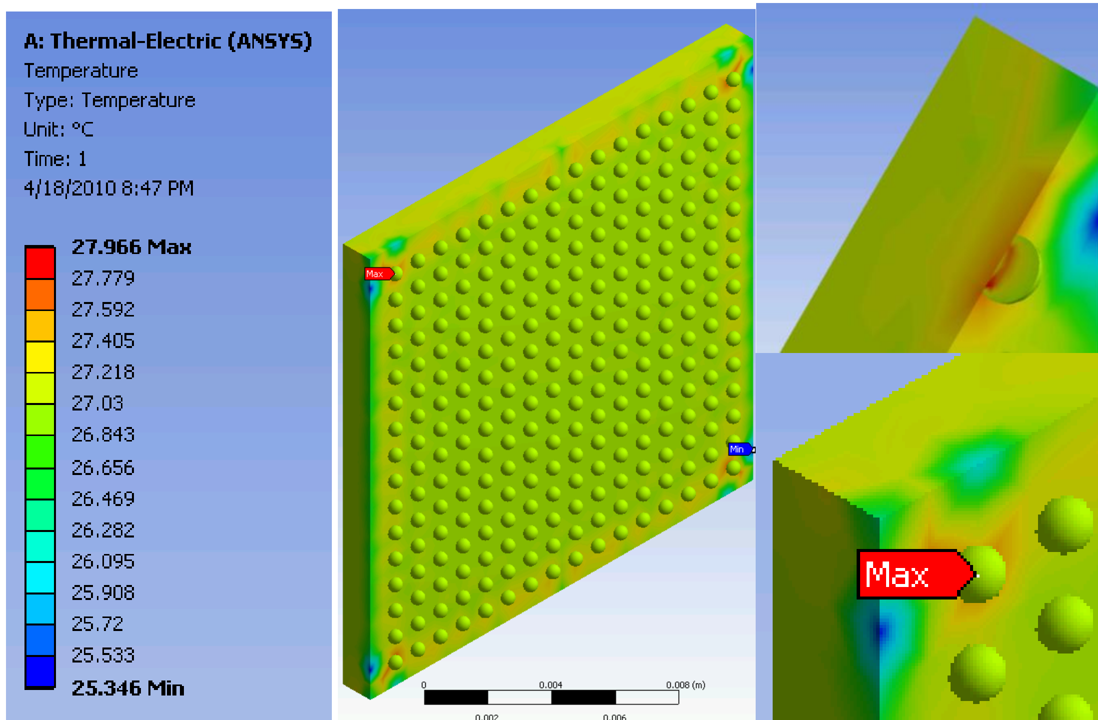

Fig. 69. Unrestricted Package temperature of 256-lead BGA.

In deformation tests that simulated the simple effects of gravity, the perimeter and corners of the package deflect the most, indicating that they undergo the highest structural deformation. Of the leads, the corners experience the greatest deformation indicating that gravity has the highest effect upon the corners of the package and the corner leads of the package. Fig. 70 is a screenshot of the highest and lowest points of deformation in a 256-lead BGA. 97Sn3Pb deflects the least of the 4 tested solders at 0.015 nm, while 60Sn40Pb deflects the most, 0.023 nm, of the 4 tested solders. While these values are small, they can accumulate and lead to failure over many power cycles. The chart in Fig.71 compares these values, indicating that the 97Sn3Pb is the most brittle of these materials and is more likely to fracture. During a power cycle, if the material is more brittle, it is less able to deform when the PCB and the BGA expand at different rates. This causes more strain on the solder joints and increased strain over repeated power cycles can shorten the overall lifespan of a BGA.

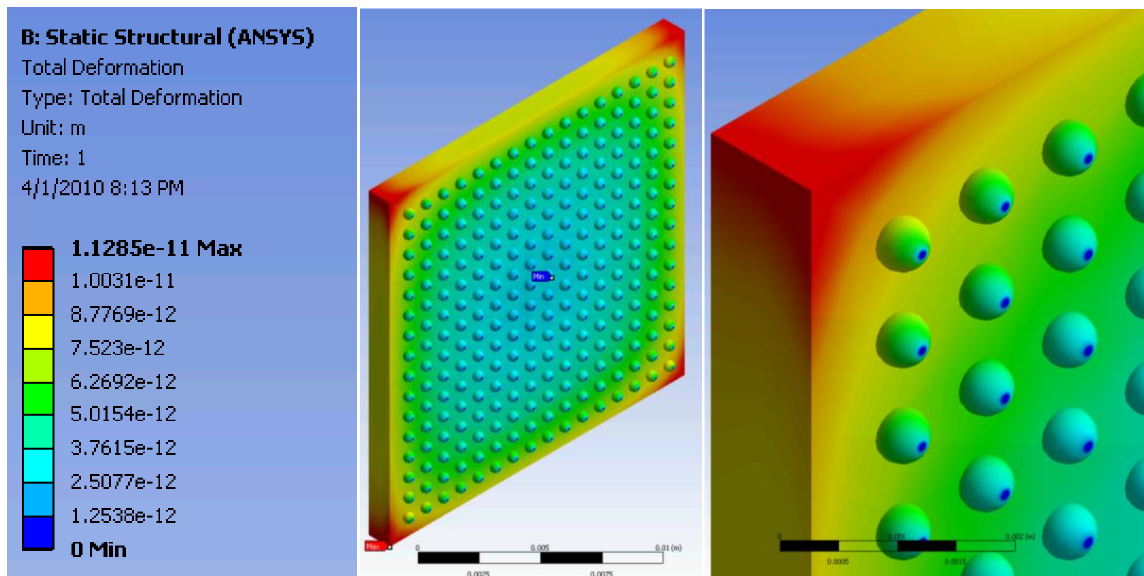

Fig. 70 Total deformation of a 256-lead BGA under the effects of gravity

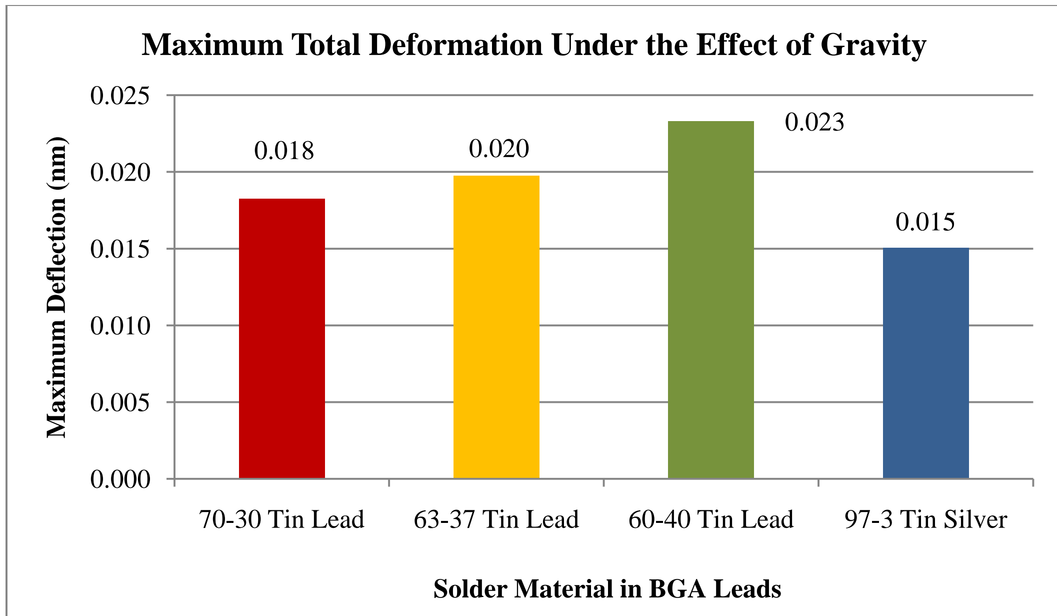

Fig. 71. Comparison of the maximum deformation of different solders.

5. Conclusions and Recommendations

Over the course of this project, BGAs demonstrate the lowest and most even heat distribution when low voltages are applied to the lead surfaces. Corner and perimeter leads undergo the highest temperatures, deformation and Joule heat. If failure is to occur, it will most likely occur along the perimeter leads of the package. Perimeter leads experience the highest temperature and temperature gradients with the coolest portions of the component, the package corners, nearby. Structural deformation is also greatest at the perimeter leads under standard gravity. The package heats at a different rate than the PCB, which adds to the strain of the leads, specifically the leads furthest from the center, the corners.

Voltage is distributed uniformly over every trial and corresponds more to the package boundaries rather than the points at which they were applied. These BGAs work best in lower voltage scenarios since any voltage greater than 2.5V will increase the temperature of the component past the melting temperature of the solders.

The argument for Pb is positive in the sense that Pb-based solders do not have the complication of whiskering. Without the risk of whiskering, the expected life of Pb-based components is longer. The solders with higher concentrations of Sn tend to be more brittle, thus more prone to fracture. Pb is a ductile metal that can deflect when the PCB expands at a different rate than the BGA component. In this sense, components containing Pb are more reliable than their Pb-free counterparts.

Despite the benefits of Pb in solders, legislation is starting to mandate the elimination of Pb in electrical components, forcing manufacturers to accommodate their processes to follow new regulations. Since many of the PB-free alternatives vary greatly in their composition, melting points and other properties, manufacturers must adjust their

methods to these alternate materials which they may not have the facilities to do so or would be too expensive to update their machines. The highest risk that lead has is when it is not recycled properly and not while it is in use in an electrical component.

The project determined that while ANSYS is a powerful tool for thermal-electric simulation, it has its limitations. Apart from the learning curve, the software is limited by the computing power of the academic license which can only solve a mesh that has fewer than 250000 nodes. This was one of the greatest limitations of the project by limiting the types of tests the group had wished to do as well as the resolution of the results.

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Appendix A: List of applications of the Analog Devices BGAs

The following information comes from materials declarations provided by Analog Devices (Analog Devices, 2002A-2010C).

Part number	Component description	Applications
AD9739	14-Bit, 2500 MSPS, RF Digital-to-Analog Converter	Broadband communications systems CMTS/VOD Cellular infrastructure Point-to-point wireless Instrumentation, automatic test equipment Radar, avionics
AD9789	14-Bit, 2400 MSPS RF DAC with 4-Channel Signal Processing	Broadband communications systems CMTS/DVB Cellular infrastructure Point-to-point wireless
AD9889A	High Performance HDMI/DVI Transmitter	DVD players and recorders Digital set-top boxes A/V receivers Digital cameras and camcorders HDMI repeater/splitter
AD9889B	High Performance HDMI/DVI Transmitter	DVD players and recorders Digital set-top boxes A/V receivers Digital cameras and camcorders HDMI repeater/splitter
AD9891 AD9895	CCD Signal Processors with Precision Timing™ Generator	Digital Still Cameras Digital Video Camcorders Industrial Imaging
AD9920A	12-Bit CCD Signal Processor with V-Driver and Precision Timing Generator	Digital still cameras
AD9923A	CCD Signal Processor with V-Driver and	Digital still cameras
AD9925	Precision Timing Generator CCD Signal Processor	Digital still cameras Digital video camcorders

	with Vertical Driver and Precision Timing ™ Generator	CCD camera modules
AD9927	14-Bit CCD Signal Processor with V-Driver and Precision TimingTM Generator	Digital still cameras
AD9929	CCD Signal Processor with Precision Timing™ Generator	Digital still cameras Digital video camcorders
AD9942	Dual-Channel, 14-Bit CCD Signal Processor with Precision Timing™ Core	Signal processor for dual-channel CCD outputs Digital still cameras Digital video cameras High speed digital imaging applications
AD9972	Dual-Channel, 14-Bit, CCD Signal Processor with Precision Timing™ Core	Professional HDTV camcorders Professional/high end digital cameras Broadcast cameras Industrial high speed cameras
AD9973	Dual-Channel, 14-Bit CCD Signal Processor with Precision Timing™ Core	Professional HDTV camcorders Professional, high-end digital cameras Broadcast cameras Industrial high speed cameras
AD9974	Dual-Channel, 14-Bit, CCD Signal Processor with Precision Timing Core	Professional HDTV camcorders Professional/high end digital cameras Broadcast cameras Industrial high speed cameras
AD9990	Dual-Channel, 14-Bit CCD Signal Processor and Precision Timing Core	Digital still cameras
AD9992	12-Bit CCD Signal Processor with	Digital still cameras

	Precision Timing Generator	
AD73460	Six-Input Channel Analog Front End	n/a
ADATE209	4.0 Gbps Dual Driver	Automatic test equipment Semiconductor test systems Board test systems Instrumentation and characterization equipment High speed memory testing (DDR2/DDR3/DDR4) HDMI testing
ADATE302-02	500 MHz Dual Integrated DCL with Differential Drive/Receive, Level Setting DACs, and Per Pin PMU	Automatic test equipment Semiconductor test systems Board test systems Instrumentation and characterization equipment
ADATE304	200 MHz Dual Integrated DCL with Level Setting DACs, Per Pin PMU, and Per Chip VHH	Automatic test equipment Semiconductor test systems Board test systems Instrumentation and characterization equipment
ADN2928	XFP Single Chip Transceiver IC	XFP MSA module receive/transmit signal conditioner SONET OC-192, (+FEC) transponders 10 gigabit Ethernet optical transceivers 10 gigabit small form factor modules Test equipment Serial backplane applications
ADSP-218xN Series	DSP Microcomputer	n/a
ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L	DSP Microcomputer	n/a
ADSP-21065L	DSP Microcomputer	n/a

ADSP-21161N	SHARC Processor	n/a
ADSP-21261/ADSP-21262/ADSP-21266	Embedded Processor	n/a
ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366	SHARC Processors	n/a
ADSP-21990	Mixed-Signal DSP Controller	n/a
ADSP-21992	Mixed-Signal DSP Controller with CAN	
ADSP-21462W/ADSP-21465W/ADSP-21467/ADSP-21469/ADSP-21469W	SHARC Processors	
ADSP-BF512/BF512F, BF514/BF514F, BF516/BF516F, BF518/BF518F	Embedded Processor	
ADSP-BF522/ADSP-BF523/ADSP-BF524/ADSP-BF525/ADSP-BF526/ADSP-BF527	Blackfin Embedded Processor	
ADSP-BF522C/ADSP-BF523C/ADSP-BF524C/ADSP-BF525C/ADSP-BF526C/ADSP-BF527C		
ADSP-BF531/ADSP-BF532/ADSP-BF533	Blackfin Embedded Processor	

ADSP-BF534/ADSP-BF536/ADSP-BF537	Blackfin Embedded Processor	
ADSP-BF538/ADSP-BF538F	Blackfin Embedded Processor	
ADSP-BF539/ADSP-BF539F	Blackfin Embedded Processor	
ADSP-BF542/ADSP-BF544/ADSP-BF547/ADSP-BF548/ADSP-BF549	Blackfin Embedded Processor	
ADSP-BF561	Blackfin Embedded Symmetric Multiprocessor	
ADuC7019/20/21/22/24/25/26/27/28/29	Precision Analog Microcontroller, 12-Bit Analog I/O, ARM7TDMI MCU	Industrial control and automation systems Smart sensors, precision instrumentation Base station systems, optical networking
ADuC7122	Precision Analog Microcontroller, 12-Bit Analog I/O, ARM7TDMI® MCU	Optical networking, industrial control, and automation Systems Smart sensors, precision instrumentation, base station Systems
ADV202	JPEG2000 Video Codec	Networked video and image distribution systems Wireless video and image distribution Image archival/retrieval Digital CCTV and surveillance systems Digital cinema systems Professional video editing and recording Digital still cameras Digital camcorders

ADV212	JPEG2000 Video Codec	Networked video and image distribution systems Wireless video and image distribution Image archival/retrieval Digital CCTV and surveillance systems Digital cinema systems Professional video editing and recording Digital still cameras Digital camcorders
ADV7520NK	Low Power HDMI/DVI Transmitter with Consumer Electronic Control (CEC)	Digital video cameras Digital still cameras Personal media players Cellular handsets DVD players and recorders Digital set-top boxes A/V receivers HDMI repeater/splitter
ADV7614	12-Bit Deep Color Quad HDMI 1.3 Receiver	Advanced TVs AVR video receivers PDP HDTVs LCD TVs (HDTV ready) OLED HDTVs LCD/DLP front projectors HDMI switchers
ADXRS150	±150°/s Single Chip Yaw Rate Gyro with Signal Conditioning	GPS navigation systems Vehicle stability control Inertial measurement units Guidance and control Platform stabilization
ADXRS300	±300°/s Single Chip Yaw Rate Gyro with Signal Conditioning	Vehicle chassis rollover sensing Inertial measurement units Platform stabilization
ADXRS401	±75°/s Single Chip Yaw Rate Gyro with Signal Conditioning	GPS navigation systems Image stabilization Inertial measurement units Platform stabilization
SST-Melody®-SHARC®	High End, Multichannel,	

	32-Bit Floating-Point Audio Processor	

Appendix B: List of ANSYS errors

In operating ANSYS 12 for the first time, the project group encountered many errors during the course of this project. Most errors were due to incorrect input and had relatively simple solutions. Others only appeared for a few simulations and did not appear in later tests.

"Although the solution failed to solve completely at all points, partial results at some points have been able to be solved. Check Troubleshooting."

This error was typically when there were conflicting inputs in the system. Once removed, the program was able to converge on a solution.

"One or more contact regions may not be in initial contact. Check the results carefully.

An unknown error occurred during the ANSYS solve. Check solver output on solution information object for possible causes."

This error was one of the more difficult ones to solve. When the files were imported into ANSYS, they maintained their mating to other bodies, but ANSYS did not register them properly. The group did extensive research to find the root cause of this error, but WPI faculty well versed in the software were unable to assist the team. The ANSYS Help files indicated what the various types of contact were, but did not offer a course of action to correct this error. No solution was ever procured for this particular error, and occurred throughout the project.

“Invalid scoping for current analysis; different loads/conditions scoped to adjacent entities. Solver pivot warnings have been encountered during the solution. This is usually a result of an ill conditioned matrix possibly due to an unreasonable material properties, an under constrained model or contact related issues.”

The solution to this error was to assure every material property was assigned a reference value.

“The unconverged solution (Identified as sub step 999999) is output for analysis debugging purposes. Results at this time should not be used for any other purpose.”

This happened when either the mesh was too refined or when the computer drive the program was running on did not have enough disk space to complete the solution convergence.

“An internal solution magnitude limit was exceeded. Please check your environment for inappropriate load values or insufficient supports. Also check that your mesh has more than one element in at least 2 directions if solid brick elements are present. Please see troubleshooting.”

This error only occurred in the structural deformation trials and only appeared several times. The group hypothesizes that the fixed supports were selected incorrectly. The group corrected the models and reapplied the loads and did not encounter this error again.

“Air contains invalid property data.

These problems are: Density is required, but is currently undefined.

These problems must be corrected before you can continue.

Please switch to Engineering Data and correct the invalid property data.”

This error was simply due to a selection of the wrong material for the model. Air was not properly defined in the Engineering Data, thus could not run the simulation with air as a material.

“An unknown error occurred during the ANSYS solve. Check the Solver Output on the Solution Information object for possible causes.”

“A general failure occurred during the solution process.”

These two errors were typically a result of too little disk space. By making a courser mesh, the error typically did not appear.

Appendix C: ANSYS Analysis Figures for Temperature Trials

The following data was documented from ANSYS when altering the temperature applied onto the leads. For each trial, the ambient and package temperatures were kept at 22°C and the temperature applied to the leads was increased by 5°C increments until 57°C, where two extra tests were done at 75°C and 100°C.

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	6:53 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		22 degC		5	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	-15.051	603.58	0	5.092	4.96E-10	11066	3.13E-12	1.39E+13
2	-15.051	603.58	0	5.092	4.96E-10	11066	3.13E-12	1.39E+13
3	-15.051	603.58	0	5.092	4.96E-10	11066	3.13E-12	1.39E+13
4	-15.051	603.58	0	5.092	4.96E-10	11066	3.13E-12	1.39E+13
5	-15.051	603.58	0	5.092	4.96E-10	11066	3.13E-12	1.39E+13

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	7:07 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		27 degC		5	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	3.9083	378.3	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12
2	3.9083	378.3	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12
3	3.9083	378.3	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12
4	3.9083	378.3	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12
5	3.9083	378.3	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	7:17 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		32 degC		5	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	8.8413	383.18	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12
2	8.8413	383.18	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12
3	8.8413	383.18	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12
4	8.8413	383.18	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12
5	8.8413	383.18	0	5.092	4.96E-10	11066	3.13E-12	9.79E+12

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	7:54 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		42 degC		5	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	18.707	392.95	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
2	18.707	392.95	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
3	18.707	392.95	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
4	18.707	392.95	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
5	18.707	392.95	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	8:18 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		47 degC		5	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	22	397.83	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
2	22	397.83	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
3	22	397.83	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
4	22	397.83	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
5	22	397.83	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	8:51 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		52 degC		5	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	22	402.71	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
2	22	402.71	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
3	22	402.71	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
4	22	402.71	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
5	22	402.71	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	9:06 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		57 degC		5	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	22	407.59	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
2	22	407.59	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
3	22	407.59	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
4	22	407.59	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
5	22	407.59	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	10:16 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		75 degC		5	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	22	425.17	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
2	22	425.17	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
3	22	425.17	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
4	22	425.17	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
5	22	425.17	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	9:52 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		100 degC		5	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	22	449.58	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
2	22	449.58	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
3	22	449.58	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
4	22	449.58	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12
5	22	449.58	0	5.092	4.97E-10	11066	3.13E-12	9.79E+12

Appendix D: ANSYS Analysis Figures for Voltage Trials

Date:	3/31/2010		Material		App. Temp.		App. Voltage	
Time:	12:03 AM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		27 degC		0.25	
Time (s)	Temp. (CC)		Voltage (V)		Electricity Field (V/m)		Joule heat (W/m3)	
	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	22	27.831	0	0.25446	2.35E-11	553.31	7.82E-15	2.45E+10
2	22	27.831	0	0.25446	2.35E-11	553.31	7.82E-15	2.45E+10
3	22	27.831	0	0.25446	2.35E-11	553.31	7.82E-15	2.45E+10
4	22	27.831	0	0.25446	2.35E-11	553.31	7.82E-15	2.45E+10
5	22	27.831	0	0.25446	2.35E-11	553.31	7.82E-15	2.45E+10

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	11:42 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		27 degC		0.5	
Time (s)	Temp. (CC)		Voltage (V)		Electricity Field (V/m)		Joule heat (W/m3)	
	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	22	30.396	0	0.5092	4.96E-11	1106.6	3.13E-14	9.79E+10
2	22	30.396	0	0.5092	4.96E-11	1106.6	3.13E-14	9.79E+10
3	22	30.396	0	0.5092	4.96E-11	1106.6	3.13E-14	9.79E+10
4	22	30.396	0	0.5092	4.96E-11	1106.6	3.13E-14	9.79E+10
5	22	30.396	0	0.5092	4.96E-11	1106.6	3.13E-14	9.79E+10

Date:	3/31/2010		Material		App. Temp.		App. Voltage	
Time:	12:15 AM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		27 degC		0.25	
Time (s)	Temp. (CC)		Voltage (V)		Electricity Field (V/m)		Joule heat (W/m3)	
	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	22	34.789	0	0.76381	7.46E-11	1659.9	7.04E-14	2.20E+11
2	22	34.789	0	0.76381	7.46E-11	1659.9	7.04E-14	2.20E+11
3	22	34.789	0	0.76381	7.46E-11	1659.9	7.04E-14	2.20E+11
4	22	34.789	0	0.76381	7.46E-11	1659.9	7.04E-14	2.20E+11
5	22	34.789	0	0.76381	7.46E-11	1659.9	7.04E-14	2.20E+11

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	10:47 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		27 degC		1	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	22	40.939	0	1.0184	9.92E-11	2213.2	1.25E-13	3.91E+11
2	22	40.939	0	1.0184	9.92E-11	2213.2	1.25E-13	3.91E+11
3	22	40.939	0	1.0184	9.92E-11	2213.2	1.25E-13	3.91E+11
4	22	40.939	0	1.0184	9.92E-11	2213.2	1.25E-13	3.91E+11
5	22	40.939	0	1.0184	9.92E-11	2213.2	1.25E-13	3.91E+11

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	11:03 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		27 degC		2	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	22	40.939	0	2.0368	1.98E-10	4426.5	5.01E-13	1.57E+12
2	22	40.939	0	2.0368	1.98E-10	4426.5	5.01E-13	1.57E+12
3	22	40.939	0	2.0368	1.98E-10	4426.5	5.01E-13	1.57E+12
4	22	40.939	0	2.0368	1.98E-10	4426.5	5.01E-13	1.57E+12
5	22	40.939	0	2.0368	1.98E-10	4426.5	5.01E-13	1.57E+12

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	11:16 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		27 degC		3	
	Temp.	(CC)	Voltage	(V)	Electricity Field (V/m)		Joule heat (W/m3)	
Time (s)	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	18.644	153.39	0	3.0552	2.98E-10	6639.7	1.13E-12	3.52E+12
2	18.644	153.39	0	3.0552	2.98E-10	6639.7	1.13E-12	3.52E+12
3	18.644	153.39	0	3.0552	2.98E-10	6639.7	1.13E-12	3.52E+12
4	18.644	153.39	0	3.0552	2.98E-10	6639.7	1.13E-12	3.52E+12
5	18.644	153.39	0	3.0552	2.98E-10	6639.7	1.13E-12	3.52E+12

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	11:24 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		27 degC		4	
Time (s)	Temp. (CC)		Voltage (V)		Electricity Field (V/m)		Joule heat (W/m3)	
	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	12.197	251.79	0	4.0736	3.97E-10	8853	2.00E-12	6 .263e12
2	12.197	251.79	0	4.0736	3.97E-10	8853	2.00E-12	6 .263e12
3	12.197	251.79	0	4.0736	3.97E-10	8853	2.00E-12	6 .263e12
4	12.197	251.79	0	4.0736	3.97E-10	8853	2.00E-12	6 .263e12
5	12.197	251.79	0	4.0736	3.97E-10	8853	2.00E-12	6 .263e12

Date:	3/30/2010		Material		App. Temp.		App. Voltage	
Time:	10:31 PM	Package	Silica		22 degC		0	
		Leads	70-30 Tin lead		27 degC		10	
Time (s)	Temp. (CC)		Voltage (V)		Electricity Field (V/m)		Joule heat (W/m3)	
	Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.
1	-65.166	1432.6	0	10.184	9.93E-10	22132	1.25E-11	3.91E+13
2	-65.166	1432.6	0	10.184	9.93E-10	22132	1.25E-11	3.91E+13
3	-65.166	1432.6	0	10.184	9.93E-10	22132	1.25E-11	3.91E+13
4	-65.166	1432.6	0	10.184	9.93E-10	22132	1.25E-11	3.91E+13
5	-65.166	1432.6	0	10.184	9.93E-10	22132	1.25E-11	3.91E+13

Appendix E: Poster for WPI Project Presentation Day

Optimization of Surface Mount Technology Specializing in Heat Dissipation in BGA CSPs

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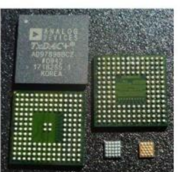
2010

Abstract

This project describes heat dissipation and mechanical deformation in BGAs. In contemporary industries, demand for smaller packages has increased the concern of thermal management. The lead-free movement has altered the properties of BGAs and comes with its own set of concerns. Packages were simulated and analyzed thermal-electrically using CAD and ANSYS software. The goal was to improve thermal management of electrical loads in CSP BGAs. Lead-based solder simulations demonstrated higher reliability than lead-free alternatives. Maximum temperature and stresses were concentrated at the perimeter, especially the corners. This project resulted in suggestions for improvements for existing packaging and opportunities for future projects.



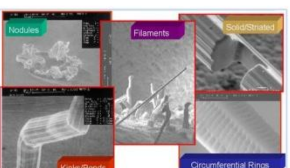
These are some of the BGA samples that we acquired from various generous manufacturers. The larger ones are from Analog Devices while the two smaller ones were obtained from ST Microelectronics. The 3 large ones are 1.2 mm x 1.2 mm and the smaller two are approximately 2.5 mm x 2.5 mm.

Lead and Solder Compositions

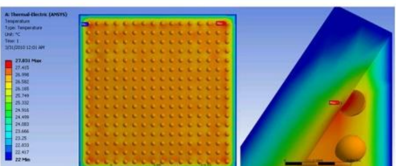
In Europe in July 2006, the new Restriction of Hazardous Substances Directive (RoHS) took effect. This legislation restricts the use of hazardous materials in technical devices to prevent the ever growing electronic waste problem. The fear is that as it builds in landfills and dumps, the hazardous waste will begin to be absorbed in to underground water supplies. It is well documented that lead when ingested can cause many life threatening illnesses. The push to remove lead, while environmentally responsible, has many drawbacks.
Although lead is one of the best options on the solder market there are other lead-free alternatives. Many of the alternatives involve a tin base mixed with other metals such as gold, silver, and copper. The lead free options, while practical, come with several disadvantages such as cost, temperature dissipation, whiskering.

One of the problems that have been occurring is the growth of whiskers on the lead-free solders. The problem is not a new one but has been brought to the foreground because of the increased use of lead-free solders. The whiskers can have many effects on electrical system. For instance, a whisker that grows and never touches any other part is a very crude heat sink but if it touches another component this causes the system to short-circuit or fail. Whiskers' sizes vary but are on the magnitude of forty micrometers in diameter. When a large amount of current passes through it, the whisker can often melt or vaporize. If the temperature exceeds the vaporization temperature this can be very problematic for a system. This can be averted by adding small amounts of lead to the solder, but as lead is being phased out, this has become an issue again.

Part of this project was to submit a technical document for the IMAPS (International Microelectronics and Packaging Society) symposium. The group attended several New England chapter meetings as a resource of the project. The technical document, titled *Improvement of Lead-based Solders until the Development of more Optimized and Sustainable Solutions*, will be presented the fourth of May, 2010.

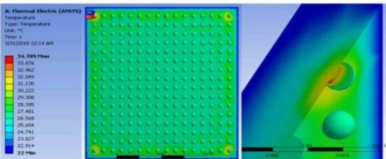


This image depicts five examples of metallic whiskering which often occurs in tin (Sn), zinc (Zn), and indium (In). This problem was once solved in solders by mixing lead (Pb) in but many lead-free alternatives are becoming a necessity as lead is being phased out of solders. Whiskers can range from 5mm and in extraneous cases up to 10mm in length (NASA, 2010).

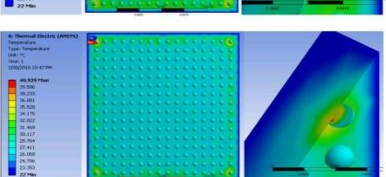


This set of images indicate the temperature changes that occur within a 256-lead BGA when a constant voltage is applied for a period of 10 seconds. The temperatures range from room temperature at 22°C to 27.8°C. This image is after 0.25V were applied over time. The highest temperature is concentrated at the junction within the ball and the substrate at the corner of the array.

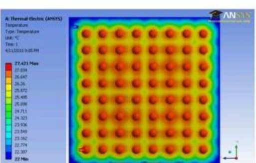
0.5V were applied to this BGA for 10 seconds. The temperature ranges from 22°C to 30.4°C. The highest temperature exists within the connection between the corner ball and the substrate.



This image depicts 0.75V being applied to the BGA. The temperature ranges from 22°C to 34.8C. The highest temperature occurs near the junction of the substrate and the solder ball.



In this 1V test, the temperature ranges from 22°C to 40.9°C. The highest temperature exists near the connection between the substrate and the solder ball in the corner of the array. Increases in voltage after this test do not greatly alter the heat distribution and dissipation. This series indicates that even though voltage may change, the incidences of the highest temperatures occur along the perimeter lead-package junctions, especially the corner leads.

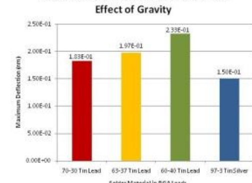


In simulating a 64-lead BGA (one eighth the size of the 256-lead BGA), higher temperatures concentrate around the balls and the immediately surrounding package. The maximum temperature occurs on one of the corner leads at 27.4°C.

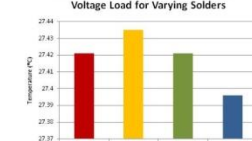
Acknowledgements

We would like to acknowledge the gracious help from John Roman and the samples provided from Analog Devices and ST Microelectronics.

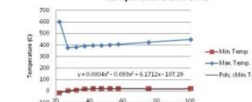
Results and Discussion



In static structural tests, the common Pb-free solder, 97Sn3Ag, demonstrated the least amount of defection under gravity indicating that it is the most brittle of these solders and more susceptible to mechanical fatigue failures.



The highest maximum temperature occurs in the 63Sn37Pb solder given constant environmental conditions and applied voltage. The 70Sn30Pb and 63Sn37Pb (eutectic) have the same maximum temperature. The lowest maximum temperature is achieved by the 97Sn3Ag solder, likely because of its lack of lead.



When applying increasing temperature loads on the leads, the maximum temperature increases linearly, while the minimum temperature also increases, but in a cubic fashion

Conclusion

Lead-based solders are not prone to whiskering which increases the reliability and expected life of BGA components. Although they can whisker, lead-free solders have a wide range of compositions and applications, but also tend to be more brittle, usually from the higher concentration of tin, which can lead to mechanical failures. These alternatives to the original tin-lead solders can also vary widely in their properties, including their melting temperature, which alters the manufacturing process and may require new and expensive equipment to use the lead-free alternatives. The highest risk that lead has is when it is not recycled properly and not while it is in use in an electrical component.

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