

Software Safety Assurance for the Boot Power Management Processor on NVIDIA's Tegra SoC

A Major Qualifying Project submitted to the faculty of the Worcester Polytechnic Institute in partial fulfillment of the requirements for the Degree of Bachelor of Science

Goutham Deva Robert Harrison Tejas Rao

Submitted to Professor Mark Claypool, Department of Computer Science, WPI Sponsored by NVIDIA Corporation



Abstract

NVIDIA's Tegra System-on-a-Chip (SoC) contains a small coprocessor responsible for initializing every other component of the chip, called the Boot Power Management Processor (BPMP). NVIDIA intends to deploy the Tegra SoC inside autonomous vehicles, but in order to do this, the code running on each of its components (beginning with the BPMP) needs to be heavily refactored in order to comply with international safety standards. Our project is to assist the Tegra System Software team with these changes by writing unit tests to achieve complete code coverage, refactoring individual modules to ensure source code compliance with the MISRA C:2012 standard, and writing documentation on each functional module in the system. We performed each of these tasks successfully, contributing over five thousand lines of changes and writing one full set of architecture and design documents. These changes ought to reduce the probability of a fault in the software that would lead to a fatal error.