Department of Electrical and Computer Engineering

NECAMSID

High Voltage DC-DC Converter

Project #SJB 2A06

A Major Qualifying Project
submitted to the faculty of
Worcester Polytechnic Institute
in partial fulfillment of the requirements for the
Degree of Bachelor of Science

Submitted By:

Larry Nelson Jr.
Eric Ruscitti

Sponsoring Agency:

NECAMSID Lab

Submitted To:

Project Advisors:

Stephen J. Bitar

April 26, 2007

lnelson@wpi.edu
ericr@wpi.edu

Stephen J. Bitar	**Larry Nelson Jr.**	**Eric Ruscitti**

1 Abstract

This project involved the design of a high-voltage DC-DC converter capable of converting 12VDC into 170VDC and delivering 250W of power. The design is based on a push-pull topology utilizing power MOSFET switches, a custom center-tapped transformer, and an all-analog feedback control system. The design comprised the front-end of a DC-AC sinewave inverter and was implemented using a custom PCB and tested. The control circuitry worked as expected, however the power-side switching posed several issues that remain to be resolved.

Table of Contents

Table of Figures

Table of Tables

2 Introduction

AC inverters are a common device in today's society. They are often used to take a low voltage DC source, such as the battery in a motor vehicle, and supply a 120 volt ac source running at 60 Hz. Since the market for such a product is so large, many competitors have entered with various implementations. Cheap designs use a "modified sine wave" which looks like a square wave. Although this is able to power devices which need the 120 volts, substantial amounts of noise are introduced into the circuits. This introduced noise is highly undesirable with audio devices. To avoid this problem, a true sine wave must be generated from the DC source. Such products exist in the market, but have a high cost associated with them. In an attempt to lower costs, a method of generating a pure sine wave with Pulse Width Modulation is being implemented. One stipulation to using Pulse width modulation is the assumption that the source voltage be larger than the output voltage. This introduces a need for a DC-DC converter which can provide the inverter with a high voltage source. Because the desired output of the inverter is 120 volts RMS, the DC-DC converter must supply 170 volts consistently.

3 Product Requirements

In order for the DC-DC converter to be integrated into the AC inverter, the design must meet the following requirements.

3.1 170 volt output

The output voltage should be 170 volts in order to accommodate the input to the DC-AC inverter. The source should be able to stay constant with a varying load. If the voltage does drop due to a large change in load, the recovery time of the supply should not interfere with the inverter's operation.

3.2 High efficiency

Since the Dc-Dc converter is only ½ of the final product, the efficiency must be high in order for the final product to be economical. However minor improvements in efficiency should not be substituted for greatly increased price. This would take away from the purpose of the design.

3.3 The output power should be larger than 250 watts.

The converter should be able to handle loads in excess of 250 watts. Since the goal of the inverter is to provide a load with 250 watts of useable power, the converter must be designed to handle a larger power load. It must be able to compensate for the losses of power within itself, along with the power losses in the DC-AC step.

4 Current Method of Implementation

There are many methods of making a DC-DC converter. For this project, most of them were ruled out because the output was not isolated from the input or they did not operate in the necessary power range. This section takes into consideration the three topologies that were seriously considered and the controls circuit that will be used for implementation of this project.

A generic block diagram of how one of these converters works with feedback loop can be seen in Figure 1.

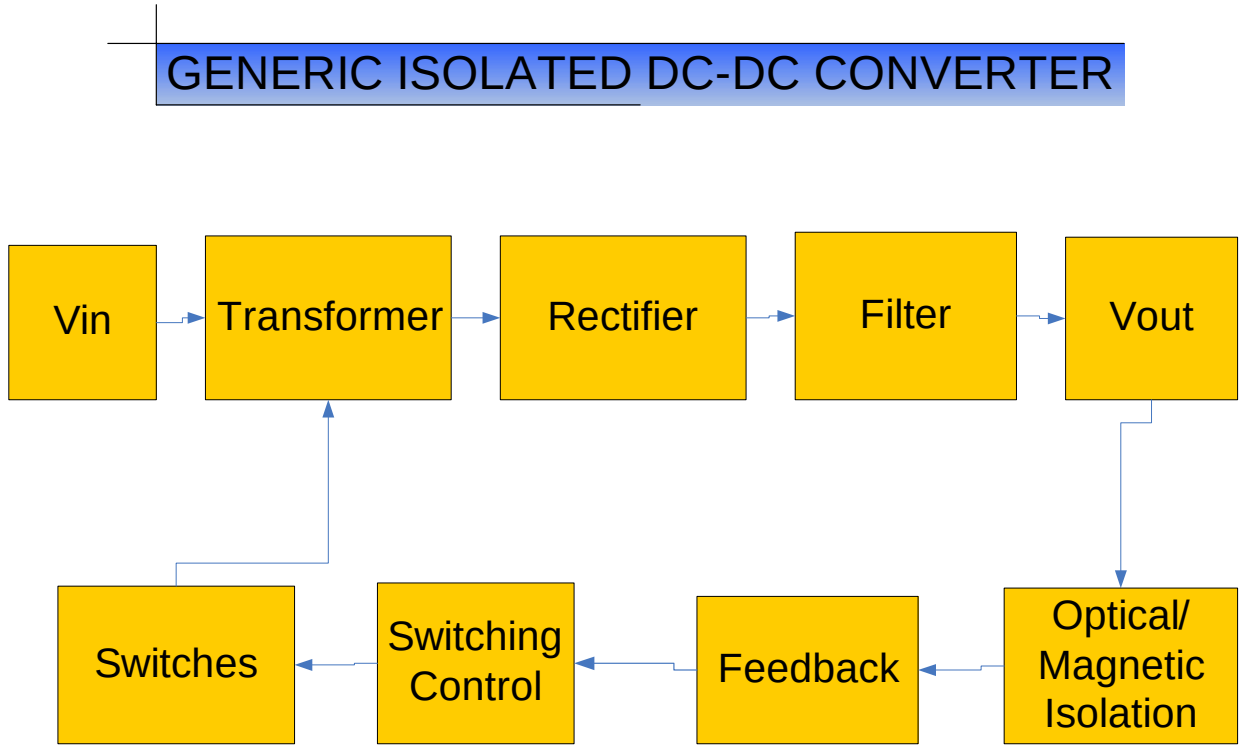


Figure 1: Block diagram of generic DC-DC converter

From this block diagram it is easy to see that the switches control the current that gets fed into the transformer. From there, the transformer creates a magnetic field which induces a voltage on the secondary side of the transformer. This voltage then turns on a part of the rectifying circuit and charges a capacitor. From there the signal is passed through an LC filter to remove ripples, forming the output of the DC converter. The output is continuously monitored by the switching controller to adjust the duty cycle of the switches. This feedback loop is normally isolated through optical or magnetic means when using an isolated topology.

4.1 Half Bridge Topology

The half bridge converter has eighty percent efficiency at five hundred watts of power. It also has a fifty percent duty cycle and isolates the input from the output through a two winding transformer.

For the half bridge converter, shown in Figure 2[1], when switch Q1 is on, current flows through the top half of the primary side of T1, expanding the magnetic field in T1. The expanding magnetic field induces a voltage across T1 secondary, such that diode D2 is forward biased and diode D1 is reverse biased. D2 conducts and charges capacitor C3 via L1.

When Q1 turns off, the magnetic field in T1 collapses and after a period of dead time, Q2 switches on. Current flows through the bottom half of the transformer and the magnetic field in T1 expands. The direction of the magnetic flux is opposite that of Q1, so now D1 is forward biased and D2 is reverse biased. D1 conducts and charges C3 via L1. After a period of dead time, Q1 conducts and the cycle repeats.

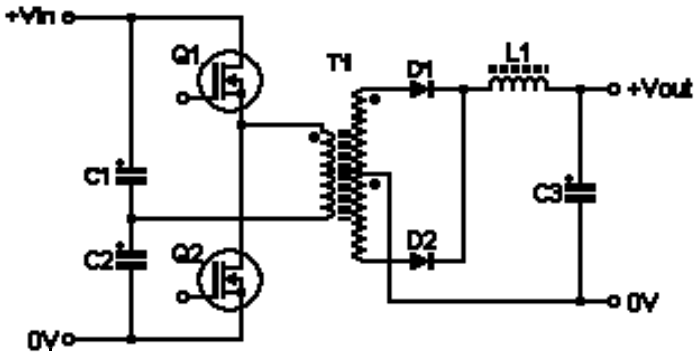


Figure 2: Schematic for half bridge topology

It is very important that Q1 and Q2 are not turned on at the same time. If they were, they would short circuit the supply. Therefore the conduction time of each transistor must not exceed half of the total period for one complete cycle.

It is also important to make sure the magnetic behavior is uniform; otherwise the transformer will saturate and destroy Q1 and Q2. This requires that the individual conduction times of Q1 and Q2 be exactly equal. For a larger picture of the half bridge schematic, please reference Appendix A: Half Bridge.

[1] http://www.hills2.u-net.com/electron/smps.htm

4.1.1 Waveforms

The waveforms for the half bridge converter can be seen in Figure 3[2]. V_{GS}(Q1) is the voltage from the gate terminal to the source terminal of the switch Q1. V_{DS}(Q1) is the voltage from the drain terminal to the source terminal of the switch Q1. V_{SW2} is another view of the voltages of the switch. I_{SW2} is the current through the switch which also flows through the primary winding of the transformer.

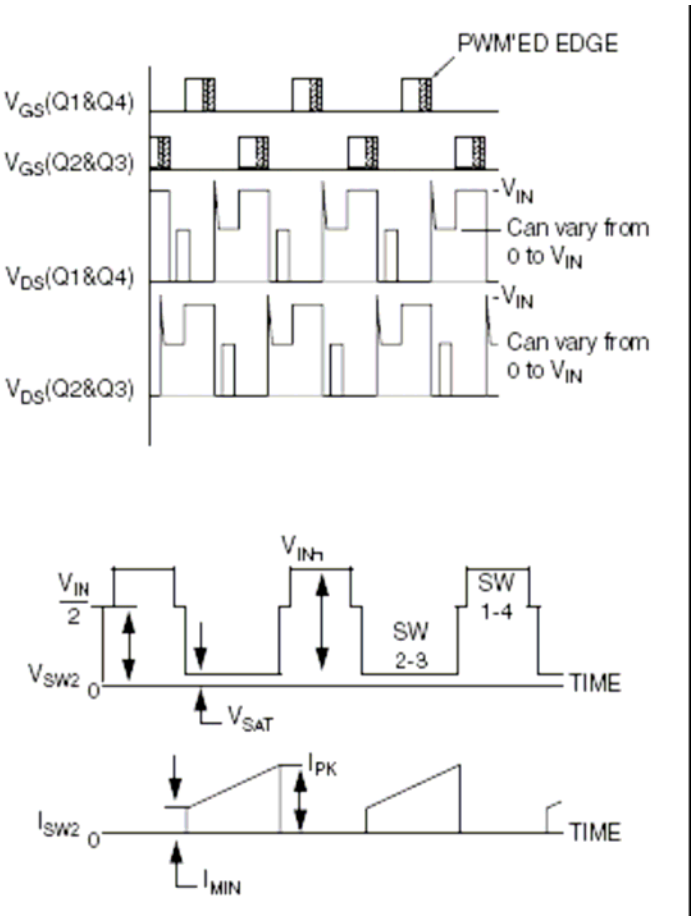


Figure 3: Waveforms for half bridge topology

For a larger picture of the half bridge waveforms please reference Appendix A: Half Bridge.

[2] http://www.hills2.u-net.com/electron/smps.htm

4.1.2 Pros/Cons

Pros	Cons
• Transformer design is not critical	• Unstable voltage from capacitors on primary side • Switching losses

4.2 Full Bridge Topology

The full bridge converter has eighty-five percent efficiency at one thousand watts of power. It also has a fifty percent duty cycle and isolates the input from the output through a two winding transformer.

The full bridge converter, shown in Figure 4[3], is very similar to that of the half bridge converter. Instead of Q1 in the half bridge, the full bridge has Q1 and Q4 on at the same time and Q2 and Q3 on instead of Q2. There is no floating source in the full bridge design (caused by the capacitors C1 and C2 in the half bridge design). Instead of the diodes charging capacitor C3, they charge capacitor C2. Other than that, this circuit works the exact same way as the half bridge.

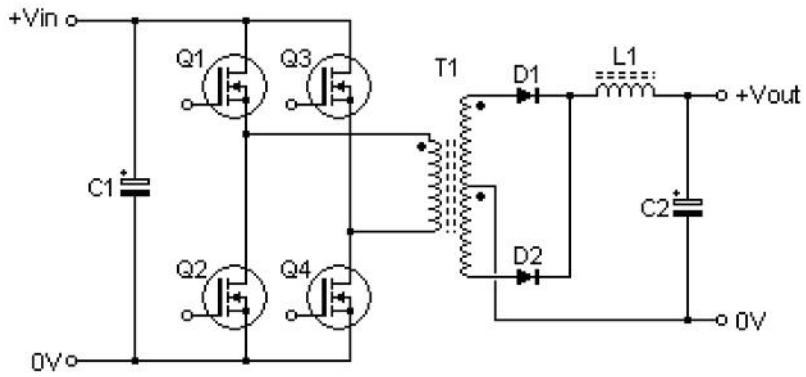


Figure 4: Schematic for full bridge topology

The same warnings about conduction time and magnetic behavior also exist for the full bridge. For a larger picture of the full bridge schematic, please reference Appendix B: Full Bridge.

[3] http://www.hills2.u-net.com/electron/smps.htm

4.2.1 Waveforms

The waveforms for the full bridge converter can be seen in Figure 5[4]. V_{GS}(Q1 & Q4) is the voltage from the gate terminal to the source terminal of the switches Q1 & Q4. V_{DS}(Q1 & Q4) is the voltage from the drain terminal to the source terminal of the switches Q1 & Q4. V_{SW2} is another view of the voltages of the switch. I_{SW2} is the current through the switch which also flows through the primary winding of the transformer.

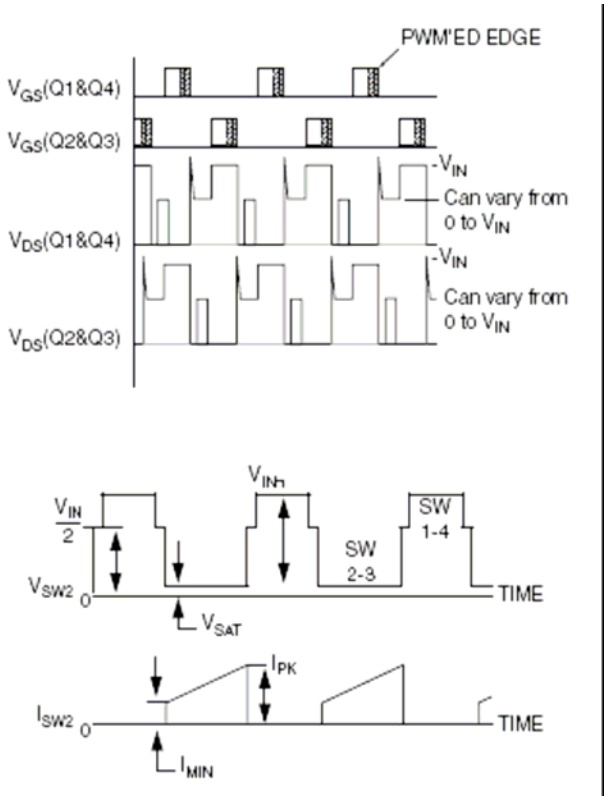


Figure 5: Waveforms for full bridge topology

For a larger picture of the full bridge waveforms, please reference Appendix B: Full Bridge.

4.2.2 Pros/Cons

Pros	Cons
• Most efficient type of converter • Handles high power applications	• Higher efficiency at higher power • Highest switching losses

[4] http://www.hills2.u-net.com/electron/smps.htm

4.3 Push Pull Topology

The push pull converter has eighty-five percent efficiency at three hundred fifty watts of power. It also has a fifty percent duty cycle and isolates the input from the output through a three winding transformer.

The push pull converter, shown in Figure 6[5], works similar to that of the half bridge converter.

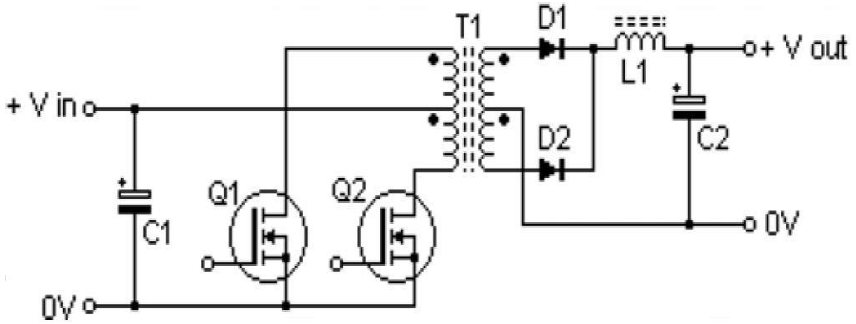


Figure 6: Schematic for push pull topology

The same warnings about conduction time and magnetic behavior also exist for the full bridge. Due to the fact that the push pull converter implements a three winding transformer, it must also satisfy the condition that the two halves of the centre-tapped transformer primary be magnetically identical. For a larger picture of the push pull schematic, please reference Appendix C: Push Pull.

4.3.1 Waveforms

The waveforms for the half bridge converter can be seen in Figure 7[6]. V_{GS}(Q1) is the voltage from the gate terminal to the source terminal of the switch Q1. V_{DS}(Q1) is the voltage from the drain terminal to the source terminal of the switch Q1. V_{SW2} is another view of the voltages of the switch. I_{SW2} is the current through the switch which also flows through the primary winding of the transformer.

[5] http://www.hills2.u-net.com/electron/smps.htm
[6] http://www.hills2.u-net.com/electron/smps.htm

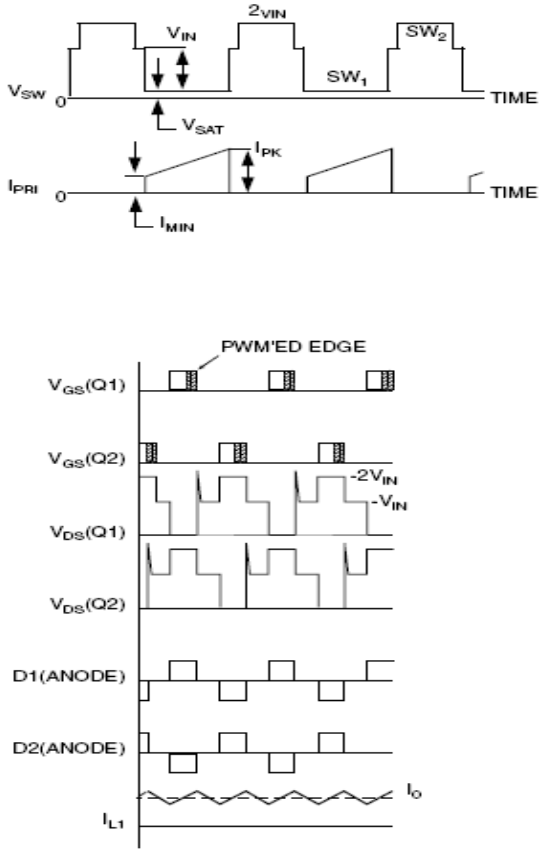


Figure 7: Waveforms for push pull topology

For a larger picture of the push pull waveforms, please reference Appendix C: Push Pull.

4.3.2 Pros/Cons

Pros	Cons
• Frequently preferred in desired power range • Simple Switching	• Switches require higher voltage rating • Voltage spikes

4.4 Controls

As with any product where the output is desired to be at a certain level, there must be a way of comparing the actual output with the desired output. This control will have to isolate the output from the input, but still be able to give feedback. For the feedback loop, an opto-isolator will be used. This will provide optical or magnetic isolation from the output to the input. The actual control circuit will be specified in the next part of the project. Figure 8 is the flowchart of one possible implementation of controlling the output voltage using Pulse Width Modulation, PWM.

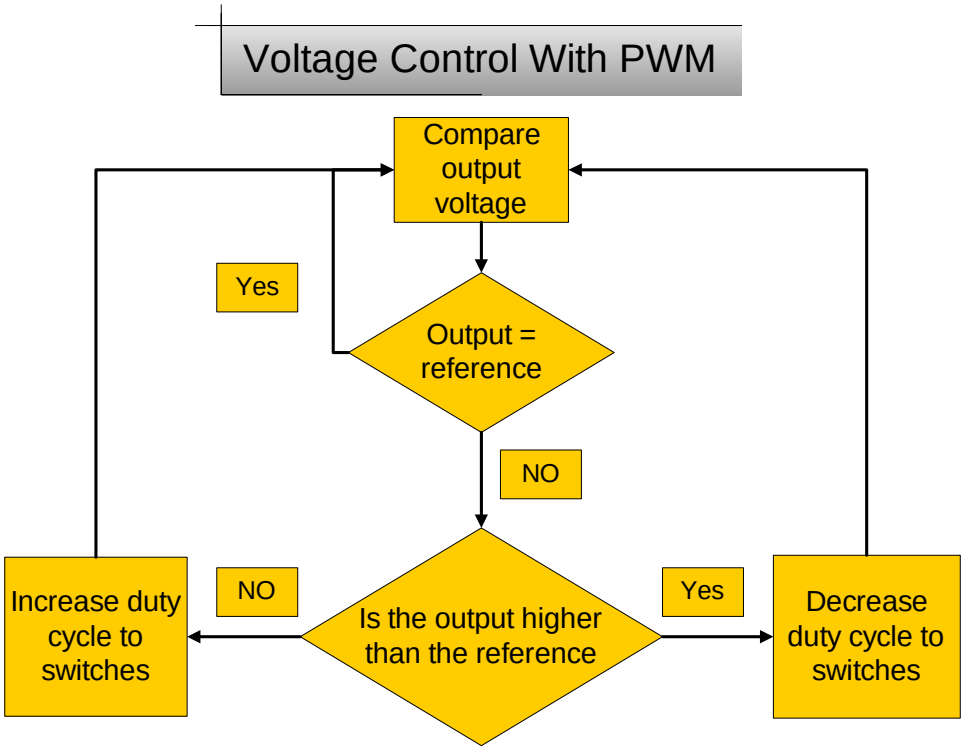


Figure 8: Flowchart of control scheme

5 Proposed Implementation

It took some research and analysis of what is important to this project to decide on a topology to use.

5.1 Value Analysis Chart

To compare all the different topologies and all the criteria that are important in a dc-to-dc converter, a value analysis chart was chosen. The chart itself is displayed in Appendix D: Value Analysis Chart. The result of the chart was to use a full bridge topology because it was the most efficient topology, albeit most complicated as well.

5.2 Chosen Topology

According to the value analysis chart, the topology to use is the full bridge. However, after more research it was found that the full bridge only attained high efficiency at high power ratings. For what this project needs, the push pull is a more realistic choice.

The push pull topology is isolated just like the full bridge, has high efficiency in the desired power range and is relatively simple to design.

5.3 Specifications

As a result of the research into different methods and current implementations of DC-DC switching supplies, broad specifications have been determined, these can be seen in Table 1. The purpose for the specifications are to steer the direction of further investigation and experimentation of the proposed design. The following chart contains the proposed specs

Table 1: Proposed specifications

Proposed specifications	
Topology:	Push Pull
Efficiency:	85%
Controls:	Isolated voltage feedback
Ripple:	<2%
Power output:	>250 watts
Cooling:	Passive

Below is a brief description as to the why each specification has been chosen.

5.3.1 Push pull topology

The push pull topology is an ideal choice for this Dc-Dc converter for multiple reasons. The most important reason is the isolation between the source and output provided by the magnetics in the transformer. Another deciding factor is the simplicity of the switching over a full bridge design. By only having to turn on 1 switch at a time, timing issues become less critical. The other important factor is that the push pull topology is commonly used at this power level. This makes the research on the topology more reliable and achievable.

5.3.2 85 % efficient

Even though the push pull topology has been documented to have efficiencies, above 90%, they are for very specialized designs and are using high end components. Within consumer goods they can be purchased with efficiencies around 80%, which is common. Based on this background knowledge, an efficiency of 85% seems a reasonable goal in the allotted time.

5.3.3 Passive cooling

With the desire to reduce complexity of the design and improve efficiency, the DC-DC supply should be designed with passive cooling. Although the amount of heat produced will be substantial from the I^2R losses in the primary winding, proper layout of the components should suffice for temperature considerations of the components.

5.3.4 Less than 2% ripple

A ripple of no greater than 2% of the output voltage should be observed from the supply. The reason behind establishing the maximum ripple is to ensure minimal noise is introduced into the system during the DC-AC stage. It is likely though this arbitrary value of an acceptable ripple will change based on the needs of the inverter.

5.3.5 Isolated feedback control

A feedback control scheme will be used to actively regulate the output voltage. By changing the duty cycle of the switches on the primary side of the transformer, based on the controls, the voltage will stay constant as current is increased to the output. The feedback loop will be isolated either optically or magnetically, to ensure complete isolation of the input and output.

6 Market Research

When starting a new project, before even thinking about the design, the first thing that should be done is market research. Market research can save a lot of time and money, both of which are precious commodities.

According to Norman T. Brust, founder of NTB Associates, a client of his spent months worth of time and over twenty-thousand dollars of his own money to develop a device to blow the meat out of the claw of a small crab. Since whole crab claw meat is worth more than partial crab claw meat, his client wanted to sell this device to fisheries to help them maximize the amount of crab meat they get from the claws. After talking with Mr. Brust, the client only had to wait approximately twenty-four hours before getting a result.

The result was that there was a world-wide customer base of two companies, both in the U.S. Both of these companies hired the wives of the fishermen to extract the meat from the claw. They were uninterested in this new device. Even though it would improve profits, it would harm employees and their families.

The client then decided to modify the device for a different type of crab, but his wife refused to let him proceed. He had already spent too much time and money. Had he started out with doing market research, he would not have wasted so many resources.

With this project, the first thing that was done was market research. What was found was that, yes there are high voltage DC-to-DC converters, but they are about 85% efficient and are costly, upwards of one hundred dollars. The purpose of this project is to at the very least maintain, and at best improve efficiency while driving down the cost.

Based on market research, there is a need for a 12vdc-to-170vdc converter. It is just a matter of making it efficient and affordable. Competing devices are too expensive or not efficient enough.

7 Proposed Implementation Challenges

As nice as it would be to have a design without flaws or any kind of problems leading up to the actual manufacturing of the device, that is unrealistic. Every product that is designed runs into problems, whether expected or unexpected. Some expected challenges of this project are as follows:

- Determining optimum switching frequency
- Minimizing transformer losses
- Sufficiently protecting driver switches without reducing efficiency
- Integrating feedback loop to switching controller
- Accurately simulating transformer and switches within converter

One of the major challenges will be accurately simulating the design prior to the testing. If the design can be modeled, then steps to optimize various components can be taken prior to assembly and testing. The challenge in modeling this design is in the magnetics and switches. Losses which are based on frequency, material constants of the core, and coupling will all need to be taken into consideration if estimations in efficiency are to be believed. As for the switching, timing as losses on the junctions and parasitic capacitances due to the high frequency will need to be accounted for.

Another challenge is the integration of the feedback loop into the switching controller. When the load increases, the controller will need to sense the difference in real time and make adjustments within the next time step within the circuit. Due to the high frequencies the methods used to adjust the switches will be handled in an analog manner.

The sooner potential problems are identified, the sooner measures can be taken to make sure they don't arise, or if it is inevitable, to minimize the effect of the problem. There is nothing worse than running into an unexpected problem, and then having to stop all other aspects of research to deal with that problem.

8 Research Conclusion

After doing much research, it was found that there is a need for a 12vdc to 170vdc converter as part of an AC inverter. It was also shown that for the power range of 250W, the best topology to use is the push pull converter because it gets 85% efficiency at 350W whereas the half bridge and full bridge operate at 500W and 1000W respectively.

9 Design

Shown in Figure 9 is the schematic for the implementation of converting 12 VDC to 170 VDC. Basically how this circuit works is that the 12VDC battery is connected to two N-MOS transistors which are being used as switches. Each transistor will be on at different times to induce a current through the transformer. If the transistors are on at the same time, they will short circuit the supply and saturate the transformer. The transformer has a 1:14 turns ratio so the 12VDC on the primary side of the transformer becomes 168 VDC on the secondary side.

The two diodes on the secondary side of the transformer create a full wave rectifier. In order to protect the diodes from voltage spikes, each diode is placed in parallel with an RC snubber circuit. At this point, the voltage is passed through an LC filter. This filter acts as a low-pass filter – allowing only signals with frequencies lower than the cut-off frequency through, while blocking all others. After going through the filter, the voltage is then scaled down to a 5V scale using resistor R4.

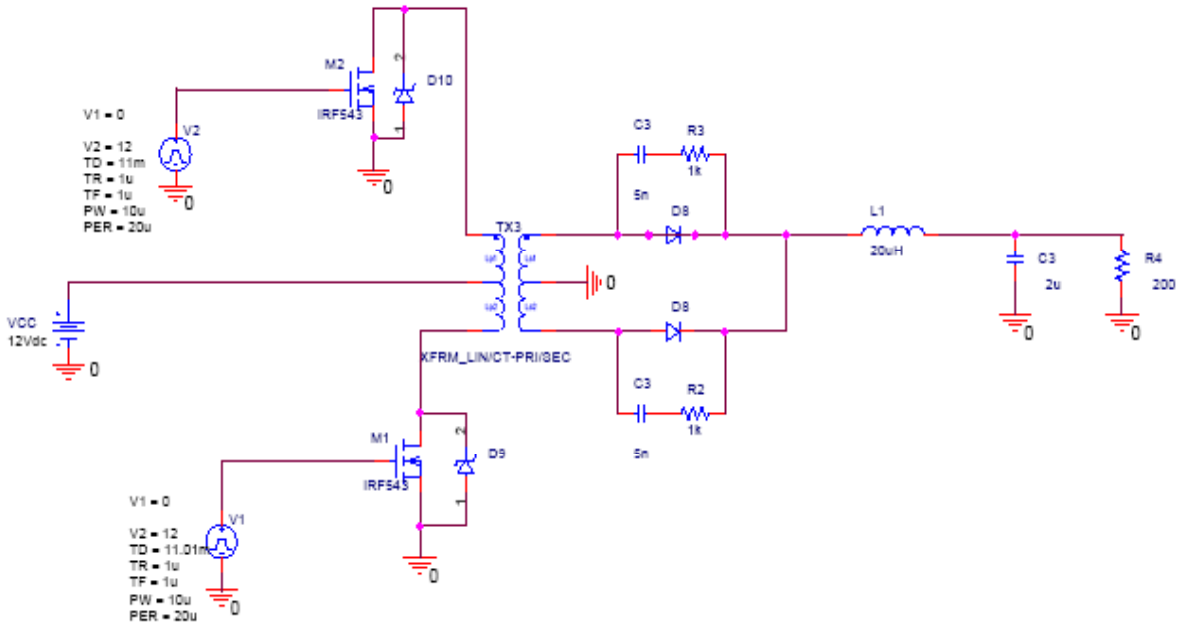


Figure 9: Push pull schematic

At this point in the overview of the circuit, it is important to go over the control scheme shown in Figure 10. The scaled down voltage is connected to an opto-isolator to isolate the power part of the circuit from the control part. Now that the voltage is isolated, it is compared to a 5VDC source through a differential amplifier. As the name suggests, this device amplifies the difference

between the two signals. This amplified "error" signal is then used as input to another op-amp which is being used to bias the error signal. This biased error signal is then compared to a triangular waveform using a third op-amp. This op-amp compares the triangle waveform with the DC bias from the previous op-amp to adjust the duty cycle of the MOSFET switches. Connecting the duty cycle to the switches is gate driver for the switches. The gate driver allows the MOSFETs to change state as quickly as possible and also prevents both MOSFETs from being turned on at the same time.

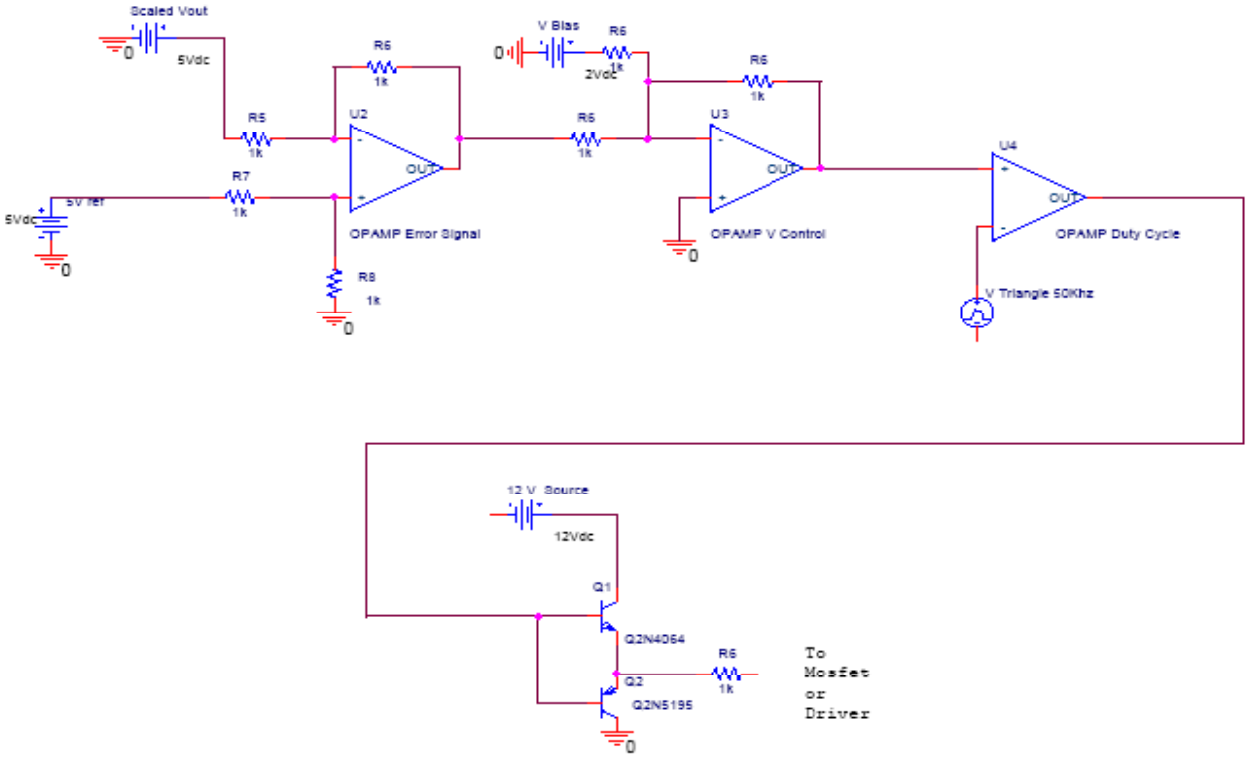


Figure 10: Control loop schematic

Currently, the control loop is in the process of being revised. The reason for this is because there are too many op-amps in the feedback circuit doing minor adjustments to the signal at each step. With a few more calculations and simulations, the circuit will be able to be reduced to one op-amp comparing the scaled down Vout with VRef, then biasing it with VBias, and then filtering before being fed into the op-amp for the duty cycle. Essentially, the new design will make the op-amp for VControl obsolete since the operations being done there will be done in the op-amp for VError.

9.1 Switching

The push pull topology relies on two switches to cycle current through the transformer at high frequencies. There are two types of switches which can be used within the design; MOSFETs (Metal Oxide Silicon Field Effect Transistors) or BJT's (Bi-Polar Junction Transistors). In each case the transistor would be running in saturation mode when turned on. This enables the transistors to resemble the characteristics of an ideal switch. There is however with both transistors, a resistance present when in saturation mode. The resistance causes energy to be wasted as heat within the device. Since the goal of this design is to be highly efficient, the on resistance of transistor should be minimal. A model of one of the switches can be seen in Figure 11.

Another important factor in choosing the transistor is the speed at which the device is capable of switching. The transistor must be able to switch states from on to off quickly for two reasons. The first is so that it can switch at the operating frequency. In this push pull design, the operating frequency is 50 kHz. However, with a push pull design, each transistor must be able to operate at twice the frequency. This is because each switch must be open for some duty cycle of one half of the operating frequency. During the second half of the cycle, the transistor is off, allowing the magnetic flux in the core to reset. The second reason the switching speed is important with the transistor, is the energy dissipation. When a switch is transitioning from off to on, it is in a linear region, which has a high resistance. Since the current can not reduce due to the inductance of the transformer, power (current squared multiplied by the resistance of the device) is being wasted. With a faster switching time, less energy can be wasted, thus improving the efficiency of the design.

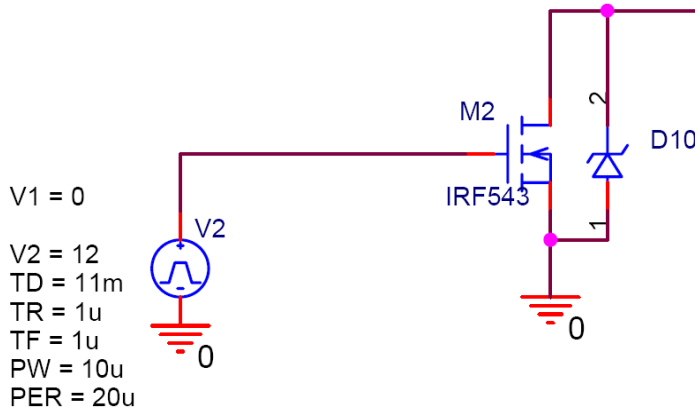


Figure 11: Schematic of switch with zener diode protection

The maximum voltage the transistor can accommodate should also be considered when choosing the device. This voltage should be larger than the voltage source which will be across the switch. To protect from Voltage spikes, an additional zener diode should be placed across each switch.

Based on the described parameters, a MOSFET which has a very low on resistance is the best choice. The maximum voltage the MOSFET should be able to handle needs to surpass 12 volts DC. The MOSFET should be N-MOS because it does not need a larger voltage than the source to bias it on. N-MOS should also be used because it typically performs at faster speeds than P-MOS and will reduce switching losses.

9.2 Transformer

When examining the design of a transformer, shown in Figure 12, there are a few key parameters which need to be chosen before the design of the transformer can be done. These parameters are based on the general formula[7], Equation 1.0 which governs how a push pull topology will behave which is as follows

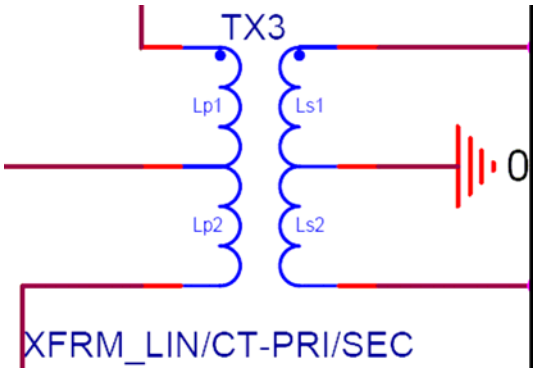


Figure 12: Schematic of transformer

$$V_{out} = 2 \cdot \frac{N_2}{N_1} \cdot D \cdot V_{in} \qquad \text{[Eq. 1.0]}$$

The first is input and output voltages. This design specifies 12 volts dc will be applied as the input, and about 170 volts dc will be the output. The other parameter which must be chosen is at what duty cycle of the switches should this voltage be obtained. In order for our design to have room to accommodate for losses within the system, a duty cycle of 0.5 was chosen. Based on these choices we can determine a turns ratio of the transformer. Unfortunately the turns ratio solved for

[7] Emanual, Alexander.

does not equal an integer. However if we reduce the expected output voltage to 168 volts, a turns ratio of 28 works perfectly. Having an output voltage of 168 volts is not an issue because it is assuming 50% duty cycle. Once the duty cycle is increased to 0.5059, the output becomes the 170 volts.

Transformers used in push-pull designs normally have multiple windings. In this design there will be 4 windings, two primary and two secondary windings. The primary windings will be $1/28^{th}$ the amount of turns as the secondary windings. Each set of windings will be attached together so that the transformer behaves like one transformer with a center tap on the primary and secondary side.

Next the core dimensions and material were chosen from the Magnetics Company catalog. The core needed to be large enough to allow large wires to be wound due to the average dc input current being 20 amps. The core also needed to be large enough to not saturate the flux during peak use. As for the material of the core, it should be designed for high frequency and have very low losses, especially since the transformer is hand wound. The core chosen is from Magnetics' MMP line which is designed to have the lowest losses. This makes the core more expensive compared to similar cores. The core achieves low losses at the frequency being operated because it is a powder core. Ferrite powder is epoxied together. This insulation of the particles almost completely eliminates eddy currents in the core.

The particular part is the MMP 55906. The important parameters of this core include the inner diameter which is 1.9 inches, the permeability of the core, μ_r which is 125, the mean length of the core, 0.1995m and the cross sectional area of 0.0227m.

9.2.1 Using the formula

To determine how many times each wire should be wrapped around the core, the delta change in the input current needs to be chosen, see Equation 2.0. This value determines the approximate inductance L of the core for the first winding.

$$\Delta I_{in} = \frac{V_{in}}{L_{core}} \cdot 0.5 \cdot \frac{t}{2} \qquad \text{[Eq. 2.0]}$$

$$2 = \frac{12}{L_{core}} \cdot 0.5 \cdot \frac{20x10^{-6}}{2} \longrightarrow L_{core} = 30uH$$

Now with L approximated for the design, the calculations of the number of turns needed can be done, Equation 3.0.

$$N_1 = \sqrt{\frac{Length_{core} \cdot L_{core}}{U_0 \cdot U_r \cdot Area_{core}}} \qquad \text{[Eq. 3.0]}$$

$$N_1 = \sqrt{\frac{0.1995 \cdot 30x10^{-6}}{125 \cdot 4 \cdot \pi \cdot 10^{-7} \cdot 0.0227}} = 1.29 \longrightarrow 2turns$$

Once N1 is determined, N2 can be determined

$$N_2 = 28 \cdot N_1 = 56turns$$

Since N2 was rounded up to 2, the inductance of the winding has changed as follows

$$2 = \sqrt{\frac{0.1995 \cdot L_{core}}{125 \cdot 4 \cdot \pi \cdot 10^{-7} \cdot 0.0227}} \longrightarrow L_{core} = 71.5uH$$

With the inductance change, the delta of the current in also changed as follows

$$\Delta I_{new} = \frac{12}{71.5x10^{-6}} \cdot 0.5 \cdot \frac{20x10^{-6}}{2} \longrightarrow \Delta I_{new} = 0.839A$$

Based on these calculations the core will perform well and have plenty of space for the two sets of the 2 turns of the primary and 56 turns of the secondary winding.

9.3 Rectifier

The two diodes in this circuit form a full bridge rectifier. Diode D8 on the top of the

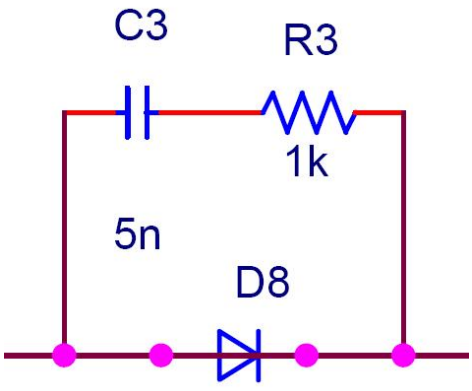


Figure 13: Schematic of rectifier diode with RC snubber protection

schematic, shown in Figure 13, is turned on when switch M1 is turned on. Diode D8 on the bottom of the schematic is turned on when switch M2 is turned on. The diodes are never on at the same time because the switches are never on at the same time. To protect the diodes an RC snubber

circuit is connected in parallel with each diode. The way the snubber circuit works is that it suppresses electrical transients by limiting the rate of rise in the voltage. Without the snubber in place, there is a chance of a voltage spike across the diodes which would permanently damage the diodes.

9.4 Filter

The combination of the inductor L1 and capacitor C3 create an LC second order low-pass filter, shown in Figure 14. The low-pass filter allows only signals with frequencies lower than the cut-off frequency to pass through, while blocking others. For this circuit, the cut-off frequency is 25165 Hz (158116 rad). Ideally the low-pass filter has a flat pass band – no gain and no attenuation – and completely attenuates all other frequencies. However, an ideal filter is not possible and after the cut-off frequency, the pass band will be falling off at the rate of -40dB/Dec.

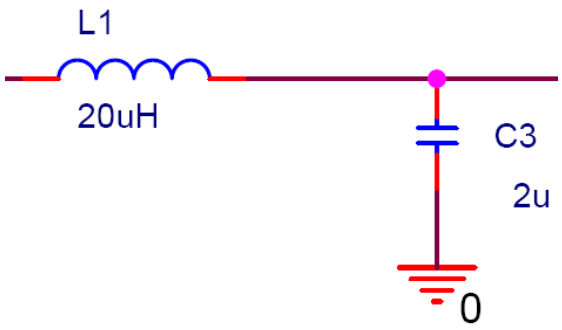


Figure 14: Schematic of LC Filter

9.5 Isolation

In order to keep the output voltage at 170VDC, it is necessary to control the amount of time the switches are turned on. The first step in this process is to scale down and isolate the output voltage. The output voltage of 170VDC needs to be scaled down to a 5VDC scale. To do this, a large R, shown in Figure 15, is necessary. The most common way of implementing an isolator is by using an LED and a light sensor. When the LED turns on, the light sensor activates and detects the amount of light being emitted and produces a current that is proportional to the amount of light.

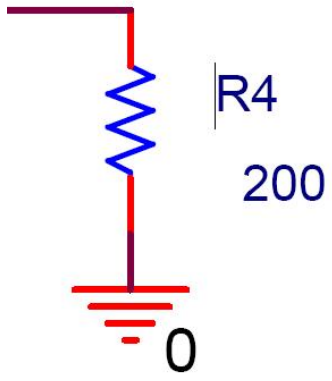


Figure 15: Schematic of resistor for scaling

9.6 Differential Amplifier

The differential amplifier, shown in Figure 16, takes two inputs and amplifies the difference between the two signals as its output. At this point in the control scheme, the scaled down output

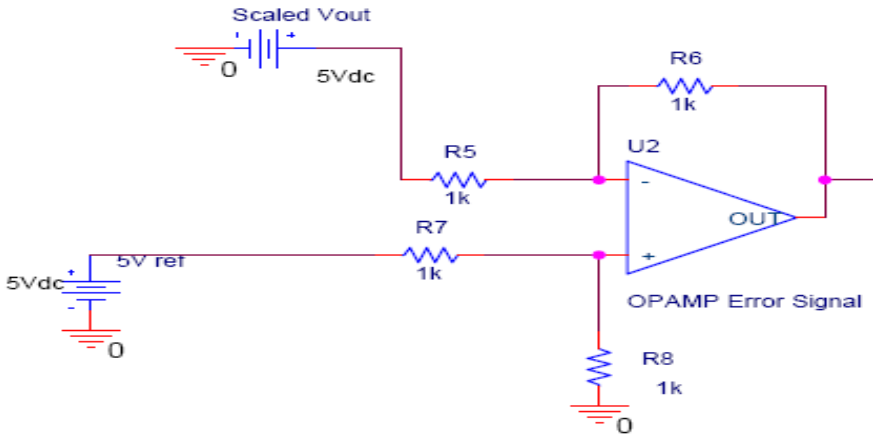


Figure 16: Schematic of differential amplifier

voltage is compared with the 5VDC reference voltage. The difference between the two inputs is then amplified by a constant determined by the resistors. The scaled Vout is attached to the V- terminal and the reference voltage is attached to the V+ terminal. When the voltages are exactly the same, there will be no output from this device. However, when the two voltages are different the difference between them is used as input to the Vcontrol part of the control circuit.

9.7 Voltage control

The voltage control loop, shown in Figure 17, sets a biased low voltage level based on feedback from the 170 volt output from the converter. This voltage is used to determine the necessary duty cycle for maintaining a constant output. The voltage control circuit has 4 steps. First the output must be reduced to a scaled low voltage through isolation. The purpose of the isolation is to protect the ICs from damage which could come from a high voltage spike. The scaling and isolation is accomplished with a resister and a current fed optical isolation IC. The amount of current into the component is proportional to the voltage at the output and thus makes

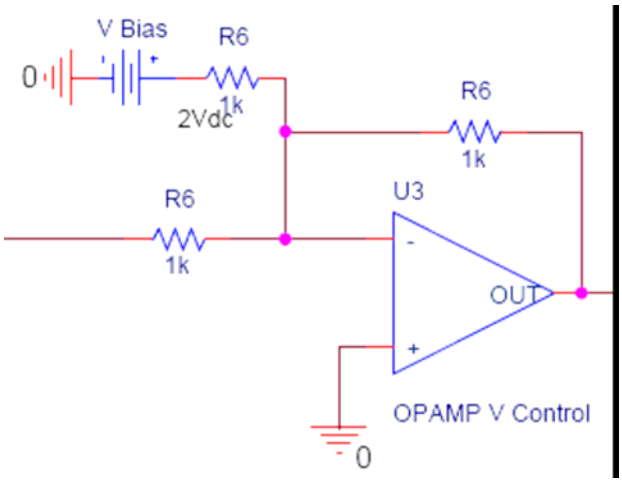


Figure 17: Schematic of V_Control

a proportional voltage on the output of the IC. Next a reference voltage is subtracted from the input. This value represents the delta which the voltage must change to reach the desired value. At this point in the circuit, a gain is applied to the error. The purpose of this amplification is to make the returned signal correct the delta quickly. If the gain is too low, the time required to reduce the error to 0 will be too long. However if the gain is increased too high, the control loop is liable to become unstable with large spikes in the error correction and have uncontrollable oscillations. After the error is amplified, a biased voltage is added to the signal. This v bias sets what the duty cycle should be when the error is 0 for the switches. A schematic of the implementation of these steps is attached.

9.8 Duty cycle control

The duty cycles of the switches are determined based on the output voltage of the converter. As the voltage drops below the desired value, the duty cycle is increased to supply more power

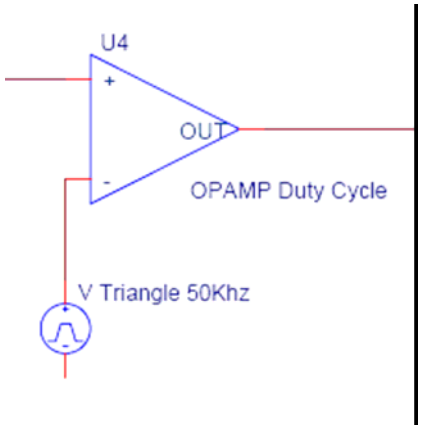


Figure 18: Schematic of duty cycle controller

through the transformer. Once the voltage reaches and begins to exceed the correct output voltage, the duty cycle of the switches is reduced to hold the value. The input in to this control circuit, shown in Figure 18, is the control voltage and a triangle wave which is running at the operating frequency of 50 kHz. The triangle wave is generated using an a-stable multivibrator out of some opamps, resistors and a capacitor. Both signals, the triangle and control, are attached to a comparator. The triangle is attached to the V- terminal and the control is attached to the V+ terminal. The V+ rail for the comparator is set to the necessary voltage to saturate the MOSFET switches. When the control voltage is less than the triangle, the duty cycle is 0 and the MOSFETs will not turn on. As the control voltage increases, a larger proportion of the triangle wave becomes less than the control, turning the comparator high along with the MOSFETs longer. Once the control voltage is larger than the triangle waves, the duty cycle is 100%. For the push pull design however, the duty cycle must be kept below 100% so the core of the transformer can reset.

9.9 Switching driver

The purpose of the switching driver, shown in Figure 19, is to make the MOSFET change states as quickly as possible. The input to the driver circuit is the PWM pulses which represent the duty cycle that the MOSFET will operate at. The voltage of the input pulses will be based on the

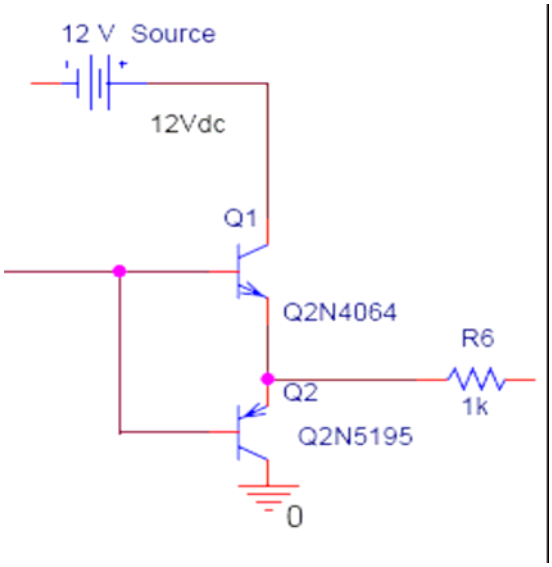


Figure 19: Schematic of switching driver

requirements of the MOSFET's requirements. Most MOSFETs which would be used in this design would only need a gate voltage of between 3.6 to 6 volts. One of the important requirements for the switching driver is the ability to introduce a delay into the signal. The reason is that there will be one PWM signal being produced from the control loop and one of the two switches must react exactly at T/2 where T is the duration of time for one cycle. Although the task of having the two signals could be approached earlier in the control loop, adding a time delay to the signal as it goes into one of the switches ensures better matching of the duty cycle to each switch. It is because of this desire for a time delay, that a MOSFET driver IC is appropriate to be used. The IC's output will attach directly to the MOSFET switch's gate. The IC will be designed to drive N-MOS MOSFETs and will not require bootstrapping to raise the gate voltage. The IC will also have a low power consumption, to improve efficiency of the design.

10 Simulations

To gain an understanding of how this circuit is going to work, a simulation was made using Pspice in conjunction with OrCad Capture. The purpose of the simulation was to examine how the current flowed through the system, specifically through the diodes, and filter. Simplifications were made in the simulation for the switches. As a substitute for the MOSFETs a voltage controlled switch was implemented in the simulation with a series resistance equaling the Rds-on value from the datasheet for the MOSFET planned on being used. Certain non-linear characteristics, i.e. hysterisis and saturation of the core, of the transformer could not be modeled because Pspice is a linear simulation tool. As a simplifying assumption in the model the transformer was made to be ideal with a coupling constant of 0.99. In the simulation the load was represented by a 200 Ohm resistor which

10.1 Results

The results of the simulation we were able to produce multiple waveform graphs which helped us understand the characteristics of some of the components. All graphs that were found to be relevant in determining parameters are in the following sections. The most notable parameters were:

- Expected power losses from the MOSFETs
- Break-down voltage of the rectifier diodes
- Average forward current through the diodes
- Snubber circuit
- L and C filter values

10.1.1 Expected Power Losses from the MOSFETs

The calculated power loss in each of the MOSFETs, when on, was determined by examining the current multiplied by the Rds-on multiplied by the duty cycle. A graph of this can be seen in Figure 20. To ensure the value graphed was realistic a quick calculation of $P=I^2$Rds-on*duty cycle equals

$$P = 20^2 \cdot 0.0038 \cdot 0.5 = 0.76$$

This value is reasonably close to the value in the simulation so we can conclude the simulation should have accurate data.

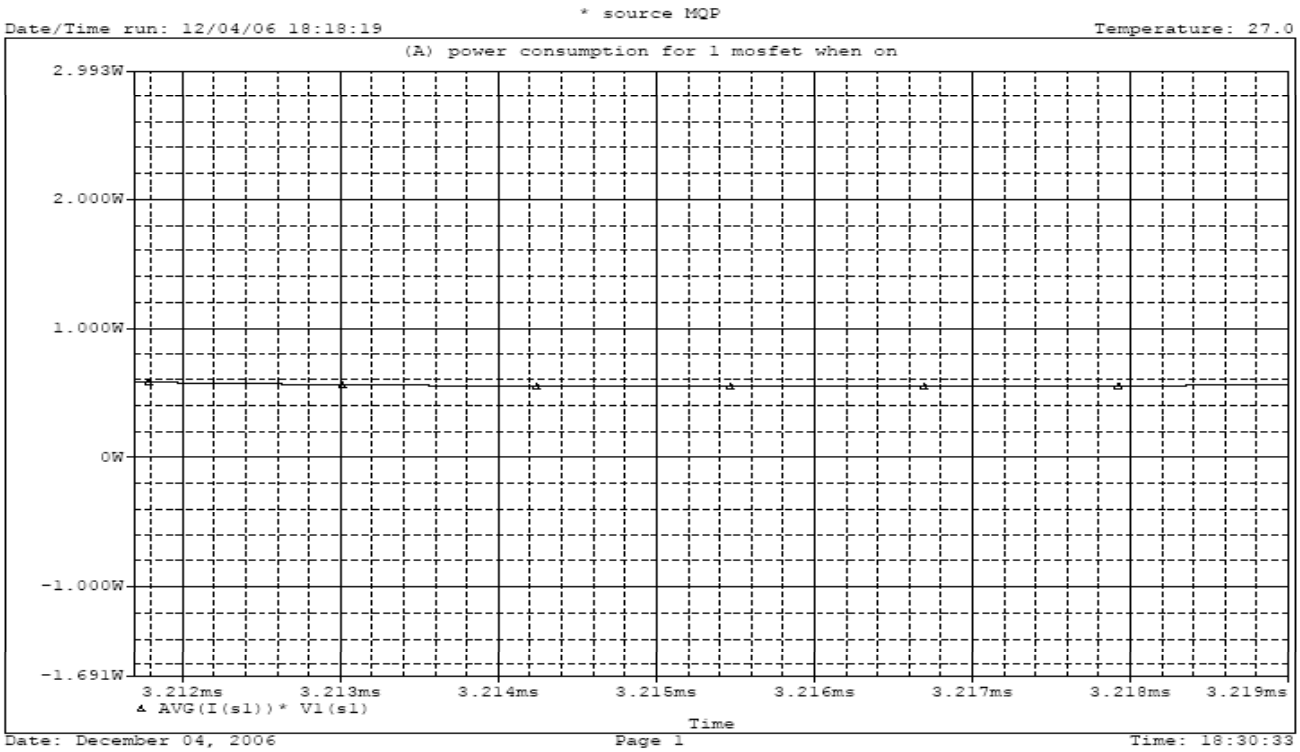


Figure 20: Power loss in MOSFET

10.1.2 Diode Break-down Voltage

The diode break-down voltages were simulated with a real diode STTH5L06 which is an ultra-fast high voltage rectifier. There were extremely large voltage spikes and a snubber circuit was added to remove the voltage spikes. During the initial start-up of the circuit, the diode experiences a voltage spike around 440V as shown in Figure 21. Once the circuit reached a steady state the voltage stayed around 400V as shown in Figure 22.

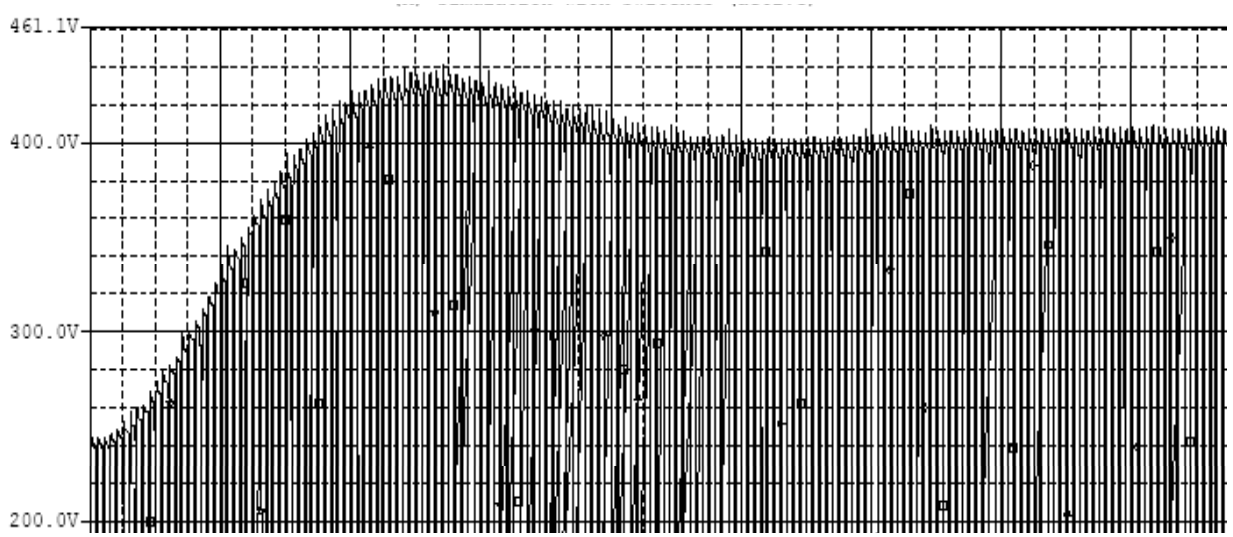


Figure 21: Transient of voltage across diodes

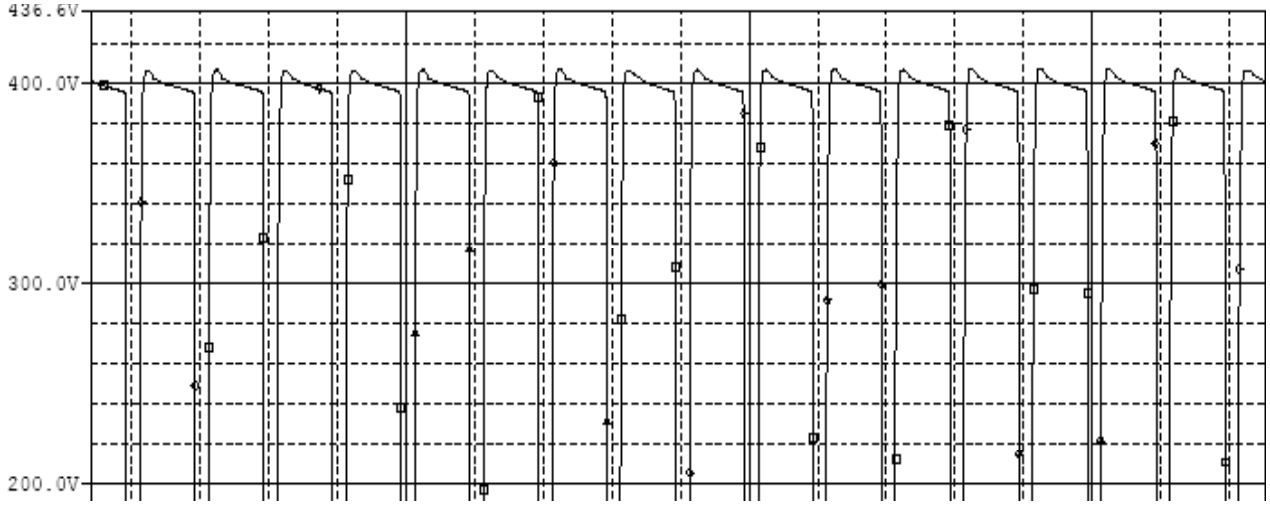


Figure 22: Steady state diode voltage

10.1.3 Average Forward Current through the Diodes

The forward current through the diodes was simulated with a real diode STTH5L06 which is an ultra-fast high voltage rectifier. During the initial start-up of the circuit, the diode experiences a current spike around 2.1A as shown in Figure 23. Once the circuit reached a steady state the current stayed around 1.45A as shown in Figure 24.

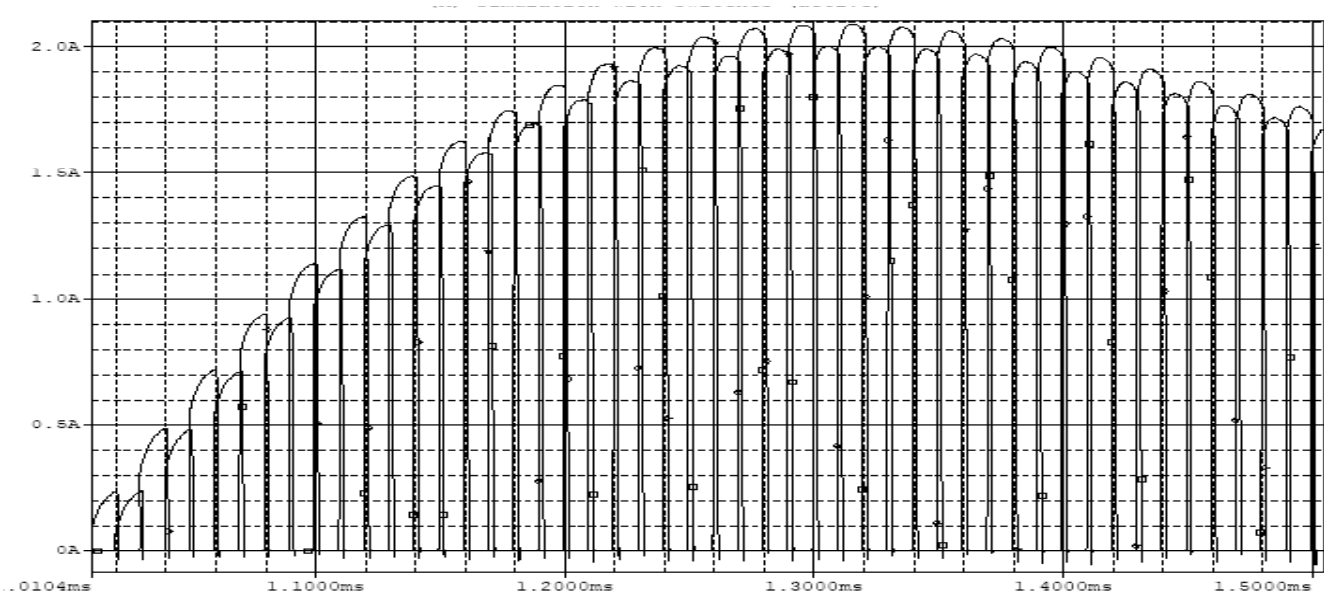


Figure 23: Transient of current through diode

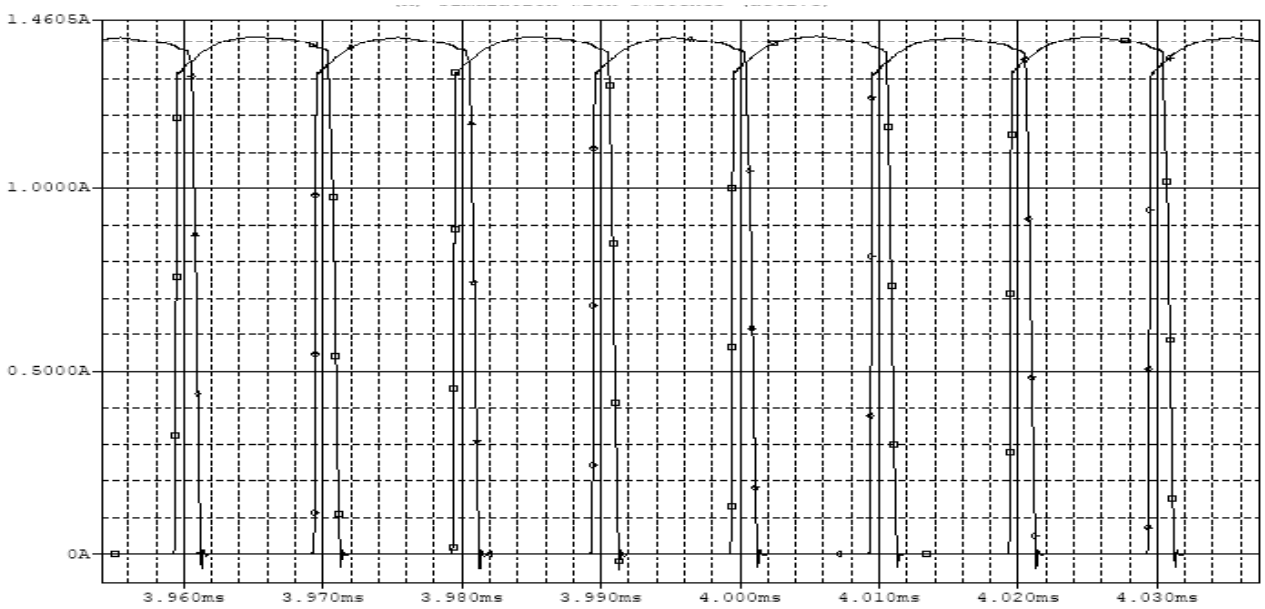


Figure 24: Steady state current through diode

10.1.4 Snubber Circuit

The need for a snubber circuit was realized when high voltage spikes were seen across the diode. The purpose of the snubber circuit is to remove the high frequency spikes by having the capacitor collect the charge and then discharge through the resistor. Through multiple simulations, it was found that the values of C=5nF and R=1kΩ minimized the amount of voltage spiking across the diodes.

10.1.5 L and C Filter Values

The values for the LC filter were determined by using the formula

$$\Delta V = \frac{(1 - 2 \cdot [DutyCycle]) \cdot Vout}{32 \cdot F^2 \cdot L \cdot C}$$

Choosing L=20µH and C=2µF the Vout is a smooth line after 4ms. This represents a very low ΔV therefore the LC values will accomplish the goal of 2% ripple according to the simulation.

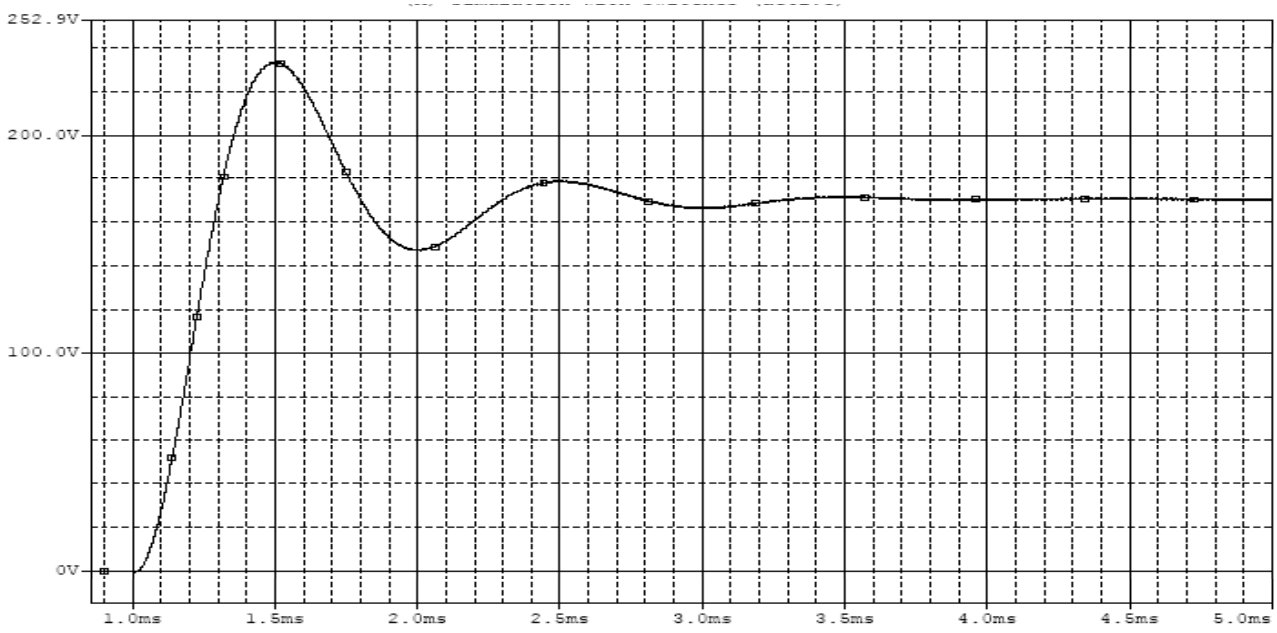


Figure 25: LC Filter

Design Conclusion

Based on these schematics and simulations, the circuit will work. A triangle wave generator will be assembled so the circuit will not require the use of a function generator. The only problem that remains is how to ensure only one MOSFET is on at any given time.

11 Block Diagram

A generic block diagram is good to have when starting the design of a project, but once you're ready to actually start implementing the design and building the device, it is even better to have a specific block diagram. Just like having a very detailed outline makes writing a paper easy, a very detailed block diagram makes drawing a schematic using a schematic capture software program very easy.

When this project was started, a generic block diagram was used to describe how the device was going to be designed, this can be seen in Figure 1, and for ease of comparison can also be seen here in Figure 26. Since then, most of the blocks haven't changed, but more specific information has been added to show how the device will work, this specific block diagram is shown in Figure 27.

The Optical/Magnetic Isolation block in the original block diagram was removed from the specific block diagram and the Feedback block was broken down into blocks pertaining to the specific tasks of the control scheme (these changes will be explained later in this report). If you were to take the specific block diagram and hold it next to the schematic, you would be able to see where each of the blocks is implemented.

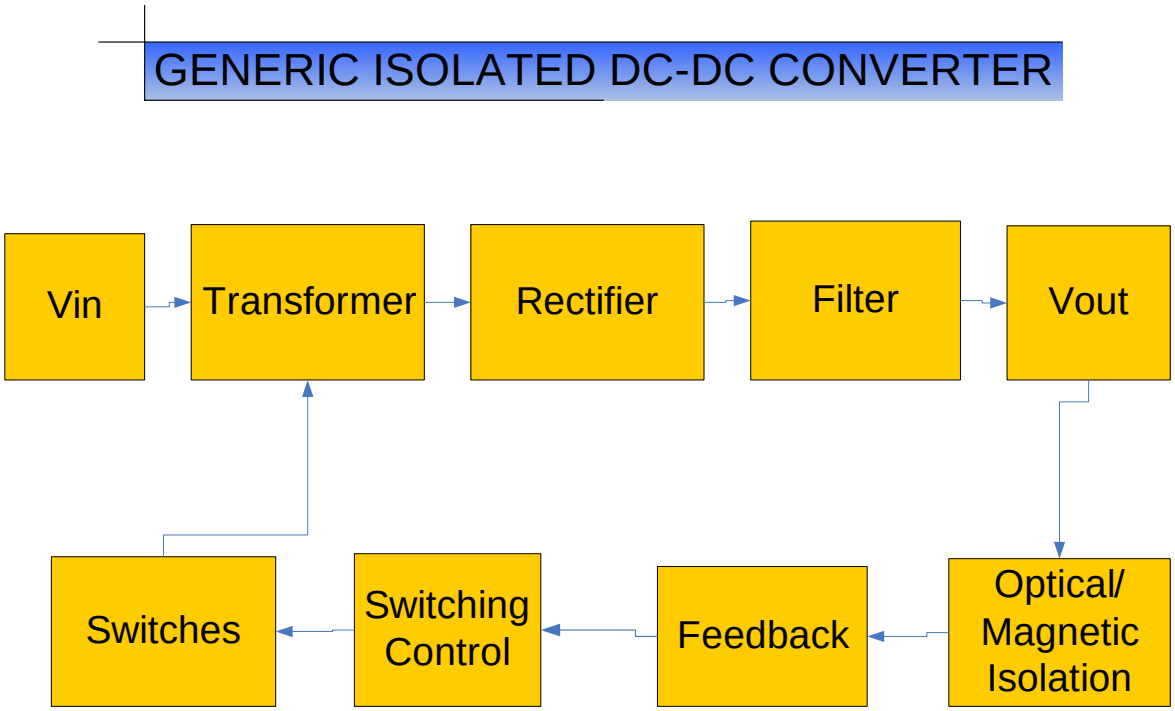


Figure 26: Generic block diagram of DC-DC converter

One other change in the block diagram is the use of arrows of different widths. The thicker arrows in Figure 27 show the flow of energy through the device, while the thinner arrows show the control circuitry. This distinction was not made in Figure 26.

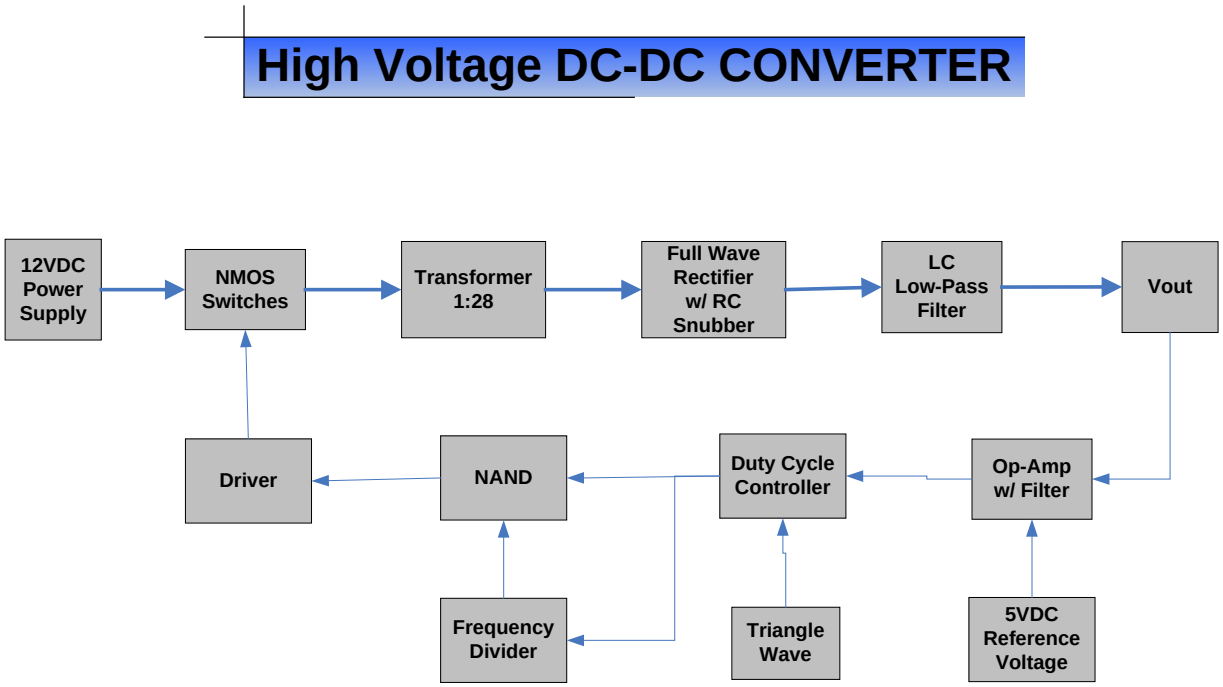


Figure 27: Specific block diagram of high voltage DC-DC converter

12 Revisions to Design before Prototype

As mentioned before changes were made to the block diagram, which led to changes in the schematic, and ultimately the prototype. Some of the changes were to take out parts that were not going to be implemented others were to add in parts that were to be implemented.

12.1 Isolation

Based on the original block diagram, a device was to be used to provide optical/magnetic isolation. In the final implementation of this device, that component was not used. It was not from lack of finding a device to do this, to the contrary there were plenty of devices that would isolate the output from the controls the problem was with not fully understanding how the component works and how it would affect the functionality of the device. Instead of using an opto-isolator to isolate the output from the controls and give a proportional voltage to the control side, a very common and non-isolated technique was used to test the controls. A voltage divider was used to obtain a voltage of 4.4V when the output is 170V.

12.2 New Control Design

The original control design, shown in Figure 10 and here in Figure 28 was very simplistic compared to what it evolved to when the prototype was being designed, shown in Figure 29. The original control circuit used a function generator to create a triangle wave and

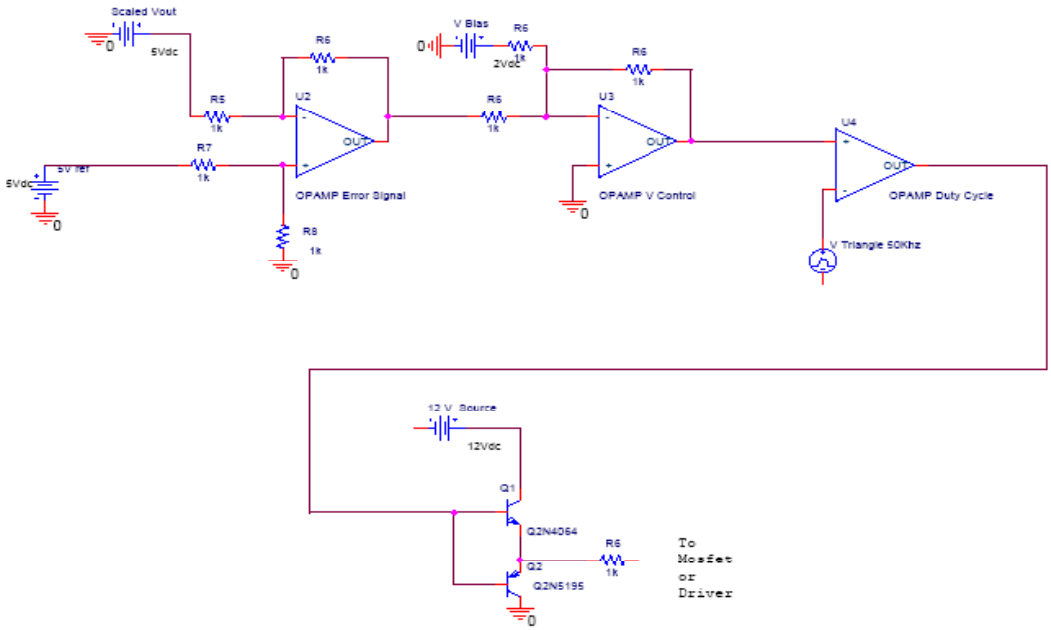


Figure 28: Original control schematic

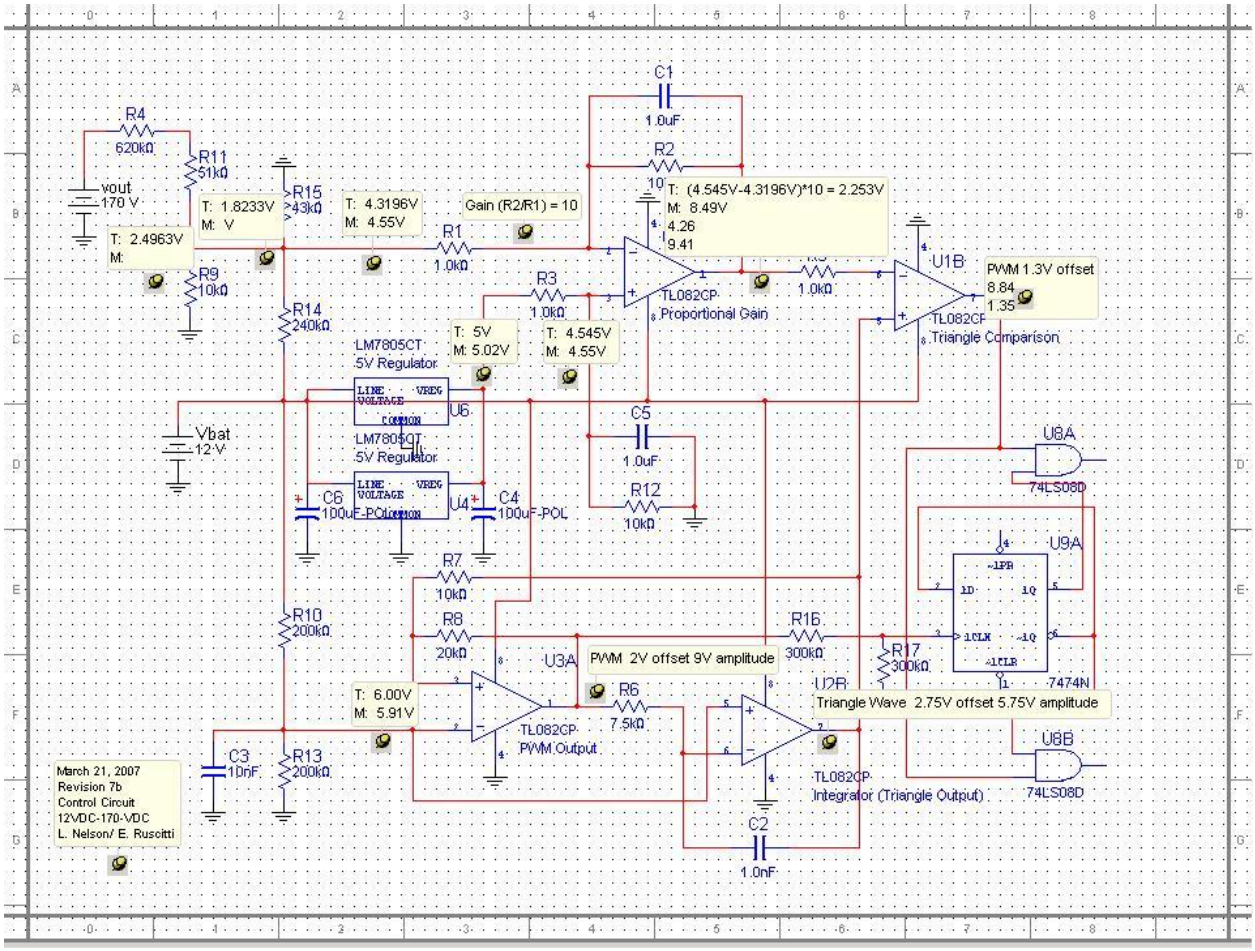


Figure 29: Control circuit used for prototype

was using a lot of resistors and operational amplifiers each doing one task that was simplified in just a couple resistors and op-amps doing the same tasks. The seven resistors associated with U2 and U3 and U2 and U3 themselves were simplified to one op-amp and nine resistors. A Schmidt Trigger was used to produce a square wave running at 55k Hz, the output of which is then used as the input for an integrator, generating as an output a triangle wave. This self-sustaining circuit means the function generator initially used to create the triangle wave will no longer be necessary and changes to other parts of the circuit will not affect the triangle wave generator.

To obtain a 5 volt reference for the differential amplifier, a 5 volt regulator was used. This component takes as its input, the 12 volts from the battery and outputs a constant 5 volts. The difference between this voltage and the scaled down output is then amplified by a factor of ten, and ideally gives as an output 6 volts. This DC voltage is then compared with the triangle wave generator giving as an output a PWM. With an output voltage of 170 volts, the output of the comparator should have a 50% duty cycle and automatically adjust to a less than 50% duty cycle if

the output is greater than 170 volts and greater than a 50% duty cycle if the output is less than 170 volts.

Only one MOSFET can be turned on at one time, otherwise the core of the transformer is at risk for saturation. To prevent both MOSFETs from being turned on at the same time, a frequency divider had to be implemented. The last step of the control circuit is to take the output of the square wave and use it as input to a frequency divider. Both the inverting and non-inverting output of the frequency divider is ANDed with the PWM output. The output of each of the AND gates is used as input for one of the gate drivers. This configuration ensures that only one MOSFET will be turned on at a time.

12.3 Inductor

An inductor of the order of 20 μH was used in the initial design of the output LC filter. However, this inductor is not capable of handling the current on the output side of the transformer. In order to handle the current, the 20 μH needed to be replaced by a 6.8 mH inductor. Just changing the inductor would change the resonant frequency, which can be found by using Eq. 4.0, of the LC filter. The frequency of the control circuitry is 55k Hz, the frequency of the filter should be a factor of ten greater or smaller than that. To make the LC filter have a resonant frequency of 5k Hz, Eq. 4.0 needs to be solved for C, yielding Eq. 4.1. Using this equation a 150nF capacitor is needed.

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \qquad \text{[Eq. 4.0]}$$

$$C = \frac{1}{(2\pi f_0)^2 L} \qquad \text{[Eq. 4.1]}$$

13 Transformer Building

The design and building of the transformer is an integral part of the entire DC-DC converter. Because the turns ratio required was not a standard design, and the fact that our current requirements were larger than most stocked transformers, it became apparent the transformer would need to be hand wound. However, determining how to safely handle 21 amps of current led to an approach which was more complicated than just 2 times around with 1 wire and 56 times around with a separate wire.

Based on the American Wire Gauge standard, a single wire of size 10 or larger would be needed to handle current spikes over 30 amps. The problem is when the wire is that thick, it does not conform well to the square shape it would be wrapped around, leading to a lower coupling with the core, and thus lower efficiency. To solve the problem, multiple sets of windings were attached in parallel. Besides enabling the wire to be thinner and thus wrap closer, it also allowed the current to be spread evenly throughout the core and leads to a better coupling between the primary and secondary side. In the final design, 3 sets of AWG 14 wire with a voltage insulation of 250 volts were used.

On the secondary side, since the current would only be around 1.5 amps, the wire did not need to be paralleled. In both cases the wire used was stranded copper since the switching frequency was not large enough to worry about losses from eddy currents. However if the design needed to be more efficient, litz wire should be used to replace the current implementation.

When assembled, the transformer has 12 turns of the primary, 6 sets of 2m and 112 turns of the secondary, 2 sets of 56. Each set of the secondary and 3 sets of the primary represent 1 side of the center tapped transformer, with an identical count for the other side. To create these nodes, the soldering of each of the wires was done directly to the board, eliminating the need for splicing wire connections. Since the inner diameter of the core chosen was large enough, only 2 layers of wires were needed. The secondary wires are closest to the core, with the larger, primary sets of wires being wrapped tightly around them. A photo of the completed transformer being attached to the PCB board can be seen Figure 30:

Figure 30: Hand wound core, 1:28 turns ratio

14 Part selection

When choosing parts to be used for the prototype, some general rules were followed to facilitate in the building stages. The most important was to use through hole components whenever possible. Through hole allows us to quickly assemble the prototype by hand and do not require special soldering equipment like some smaller surface mount forms. We also determined through hole components allow for quicker and neater reworking of the PCB. Wires can easily be tacked onto the bottom of the board to the pins. The only downside is through hole components would take up larger amounts of space and effect traces and layout on both layers of the board.

Another general rule followed for part selection was to avoid specialty components wherever possible. By using readily stocked components, our ability to replace any item damaged during testing becomes cheaper and significantly reduces downtime between tests. The TL082 op-amp, along with the 74 series D-Flip-Flop and NAND gates were chosen for this reason.

Current carrying ability was also very important in the part selection, especially in the power side of the design. Based on the simulations and calculations of the current levels, the switching MOSFETs, rectifier diodes, and filter components were chosen to handle well above the anticipated current at full load. The MOSFETs for example are rated at 140 amps continuous, even though, they should have an average current of 21 amps. To see a full list of part numbers of the components used in the design, refer to Appendix E: Bill of Materials

15 PCB Layout

The PCB board was designed using Ultiboard layout software. The advantage of Ultiboard is because it interlinks with Mutlisim so well. Ultiboard allows the schematic to be imported and can actually check the connections between parts to ensure proper wiring. Unfortunately since our power and control design were completed separately and integrated as a last step, the wiring checks were not used at this stage. Since this board was designed to test the circuitry and not fit into a certain form factor. The dimensions chosen for the board were 10 inches by 6 inches. This allowed plenty of space to mount all the components directly to the board including the 3 inch diameter transformer. Also by having a large board, the layout could be done to intuitively understand the flow of energy in the circuit. The layout actually is very similar to the block diagram of the system. The 12 volts enters the circuit on the left, flowing through the switches, transformer and filter along the upper part of the board from left to right. Then from the 170 volt output on the right, the control circuitry flows right to left from the triangle wave generator, to the PWM, to the logic circuits and driver chips. To monitor the whole design, in the upper left side of the board, there are various test points in the circuit.

Since the board is large enough, only 2 layers for traces are needed to interconnect all the points. On the bottom layer, a ground plane is used to reduce noise and allow for larger currents to flow. However due to the size of some traces used, there are some signal wires which are also run through the bottom layer with vias. These traces were isolated by a 20mil clearance on every side from the ground plane.

15.1 Power

Within the power side of the design, there are a couple of unique requirements which were implemented into the PCB. One of the most obvious features of the power side of the PCB is the trace widths used. When the converter is running at full load, approximately 21 amps of current will be flowing through the primary side of the circuit, the traces needed to be made as wide as possible. At some points the trace is as wide as 900 mils. One of the reasons for such wide traces was from limiting the trace thickness. Normally PCB manufactures offer multiple steps in thickness, starting at 1 oz copper, up to 3 and even 4 oz copper; 2 oz copper being twice as thick as 1oz. The downside to choosing a thicker copper is the significant increase in manufacturing cost, whereas in this situation, increasing the width did not affect the cost directly. The widths chosen for

the traces were calculated based on a trace width calculator. The formula implemented by the calculator is as follows:

$$I = 0.0647 \cdot dT^{0.4281} \cdot A^{0.6732} \text{ for external traces}$$

where:

I = maximum current in Amps

dT = temperature rise above ambient in °C

A = cross-sectional area in mils²

Another result of having such large currents at the input side of the converter is the double banana jack terminals used. Each banana jack is capable of 15 amps continuous, so by adding the ability to connect 2 in parallel, the board would be capable of approximately 30 amps from the power source. Since the output should never have over 1.5 amps flowing, only one set of terminals was used.

The last part which makes the layout of our power side is the traces used with the transformer. 3 custom circles of approximately 600 mils wide were used as the footprint of the primary side. The secondary side was connected to the rectifier diodes with vias and 100 mil wide traces. The purpose of the 3 circles were to simplify the wiring of the transformer. Each circle represents a node; the outer circle is the center tap where the 12 volts is connected. Each of the other circles are connected to ground through the power MOSFETs. On the outer ring, there are 6 holes used to solder the parallel sets of windings, while the inner 2 circles have 3 each. These circles are on the bottom layer of the board and therefore are on the same plane as the ground plane. This reduces the chances of the board acting as a parallel plate capacitor within the large surface area.

15.2 Controls

The op-amps used in the control circuitry are TL082's. This is an eight pin DIP with two op-amps on each chip, and was chosen for this reason and because they have a very fast slew rate of 13 volts/µs. Each op-amp in the schematic corresponded to one TL082 on the board just incase an op-amp was blown; the other side of the chip could still be used, after some rewiring to obtain desired outputs.

In the PCB layout software, the controls were laid out in a fashion that allowed for grouping of components that worked closely with one another. The op-amps for the square wave and triangle

wave are right next to each other as are the ones for the DC bias voltage and the comparator. The frequency divider is near the PWM output, the benefit of this will be explained later in this paper. The AND gates are near the driver chips to minimize the possibility of a time delay causing both MOSFETs to be turned on at the same time.

16 Revisions to Prototype

While assembling and testing the completed printed circuit board a few mistakes were found in the design. Most of the mistakes were easily fixed by removing unnecessary components, cutting traces, changing where a wire goes, adding circuitry that was in the schematic but was accidentally left out of the PCB design. All the revisions to the control side can be seen at the end of this section in Figure 31. The revisions to the power side were just adding in components that were in the schematic, but were accidentally left out of the PCB design so there is no new schematic for that.

16.1 5 volt Regulator

During testing before the PCB was made, the 5 volt regulator was not giving 5 volts as an output; in fact, the output was not even in the specified range. To fix this problem on the breadboard, a second 5 volt regulator was added in parallel, doing this provided 5 volts on the output pin. While testing the PCB, it was found that only one regulator was needed because it was providing the expected 5 volt output; the second regulator in parallel was never soldered to the board.

16.2 Triangle Wave Generator

The integrator chip which should be producing a triangle wave for an output was not producing this output. While making the traces in Ultiboard, the traces to pins 5 and 6 of the integrator got swapped. To solve this problem, the traces leading to these pins were cut, and the proper wiring was made on the bottom of the board. With this change made, a triangle wave was produced at the output.

16.3 DC Bias

During the design of the PCB four resistors were used to scale down the 170 volt output of the power side to 2.5 volts and provide a DC bias level of 1.9 volts. Now the same result, a voltage of 4.4 volts, is achieved using just two resistors.

16.4 Differential Amplifier

The resistors on the differential amplifier were swapped out for resistors of higher resistance to reduce power losses. Increasing the value of the resistor in the filter means the value of the capacitor needs to be reduced to keep the same time constant.

16.5 Frequency Divider

Initially, the input to the frequency divider was the square wave output. However, this was giving unexpected results at the output of the logic gates. What was happening was one driver would turn off, then immediately the other one would turn on, not giving the transformer time to reset itself. After trying to delay the signal from the frequency divider and not having much success, it was decided to change the input to the frequency divider. The input was changed from the square wave to the signal containing the PWM. This solved the issue of having one of the logic gates turn off and immediately having the other one turn on.

16.6 (N)AND

On the PCB, two AND gates are being used to AND the PWM with the non-inverting output of the frequency divider on one gate, and with the inverting output on the other gate. Since the input of the frequency divider was changed the output of the AND gates no longer interfered with one another (no more sharp off of one and sharp on of the other). Now the problem was the MOSFET driver was changing the signal from the AND gate.

The low side of the driver is an inverter because of the Schmidt trigger in the driver chip. So it would invert the signal, when it is in a closed loop. It's only an issue when the PWM is not 50%. To fix this, the output of the AND has to be inverted and easiest way is to use a NAND. The pins on the NAND are the exact same as the AND. The NAND gate also has a faster propagation delay.

16.7 Driver Chip

To make the driver chip work correctly, the high side MOSFET had to be faked. In order to do this a few changes had to be made. A capacitor had to be added to the bootstrap (pins 2 to 4). Pin 4, the low rail of the high side driver was then tied to ground through a resistor. A delay resistor was also added from Pin 5 to ground. With these changes, the driver was able to turn the MOSFET on and off.

16.8 RC Snubber

The RC snubber circuitry used to protect the rectifying diodes was accidentally left out of the PCB design. These components were added across the diodes on the underside of the board.

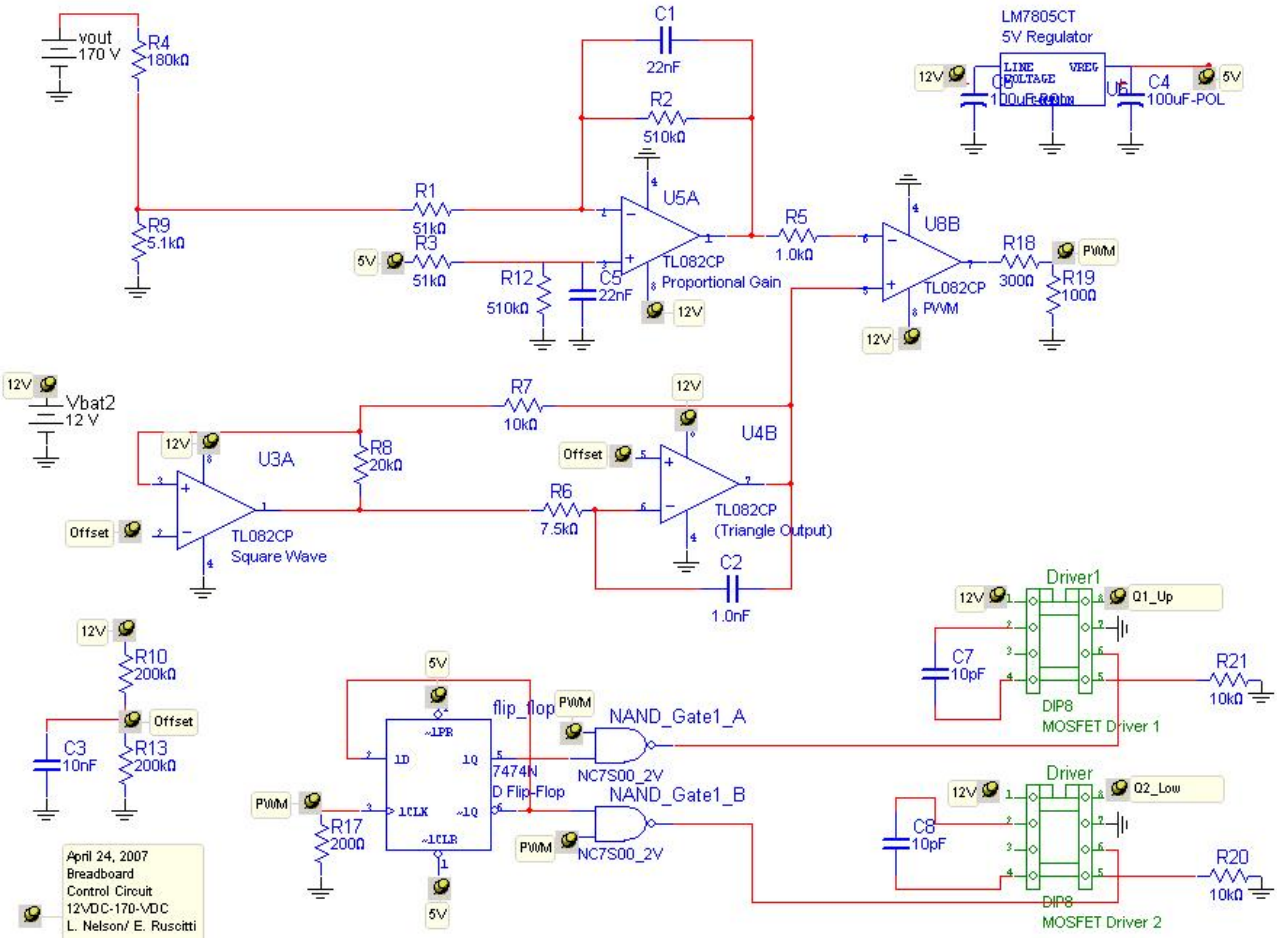


Figure 31: Revised control schematic

17 Testing

After making the changes to the board, it was time to make sure the changes would work. Here are explanations of the tests performed and the outcomes.

17.1 Controls

Testing the controls meant simulating a 170 volt output and observing the output waveforms of the triangle oscillator, the PWM, the frequency divider and the NAND gates, along with measuring the power used.

17.1.1 Output Waveforms

The output of the square wave integrator resulted in a triangle wave which was compared with a DC bias to produce a PWM; this wave form is shown in Figure 32. Ideally with a 170 volt output this PWM has a duty cycle of 50%.

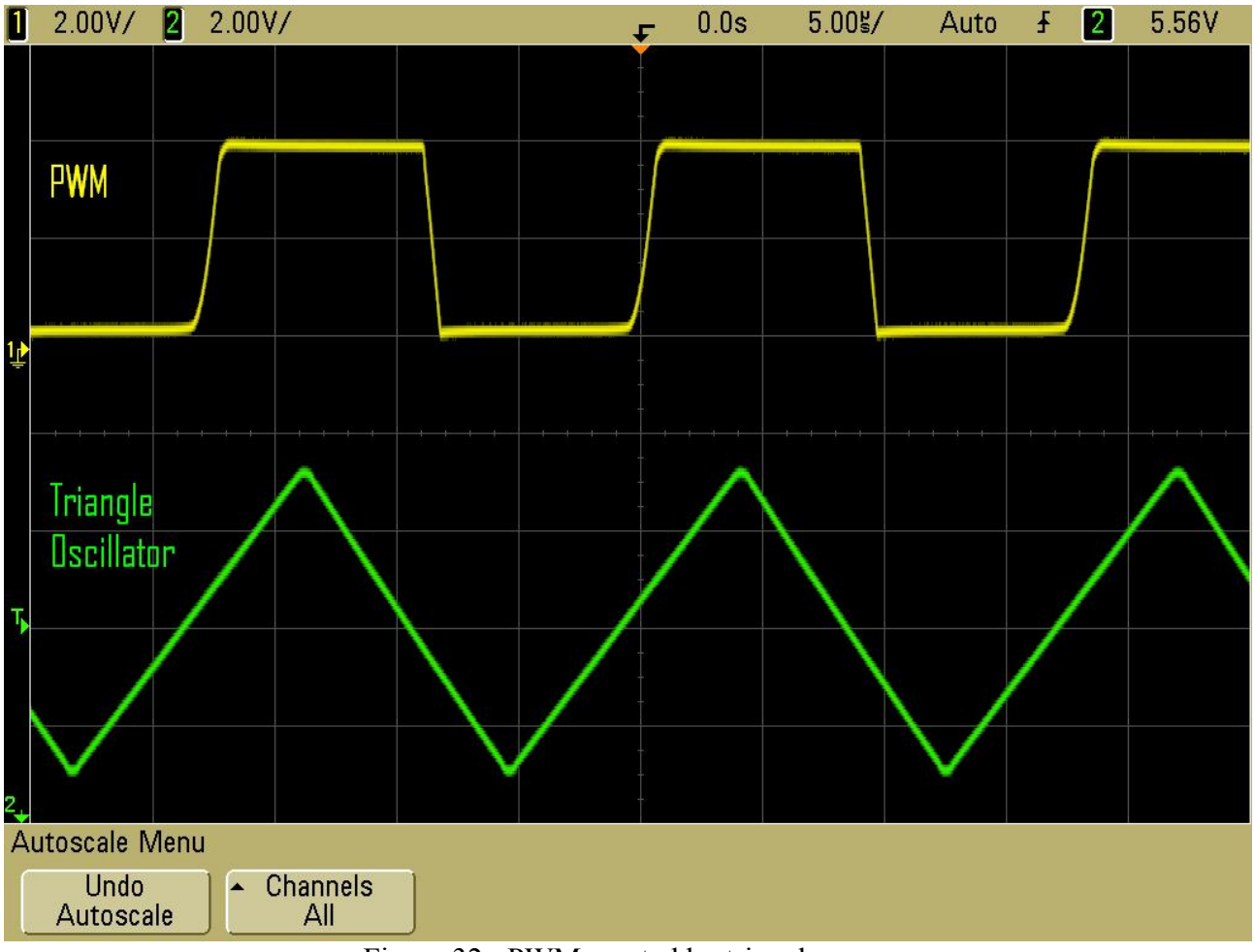


Figure 32: PWM created by triangle wave

The PWM signal is then used as input to the frequency divider. This will divide the frequency of the PWM by a factor of two, as can be seen in

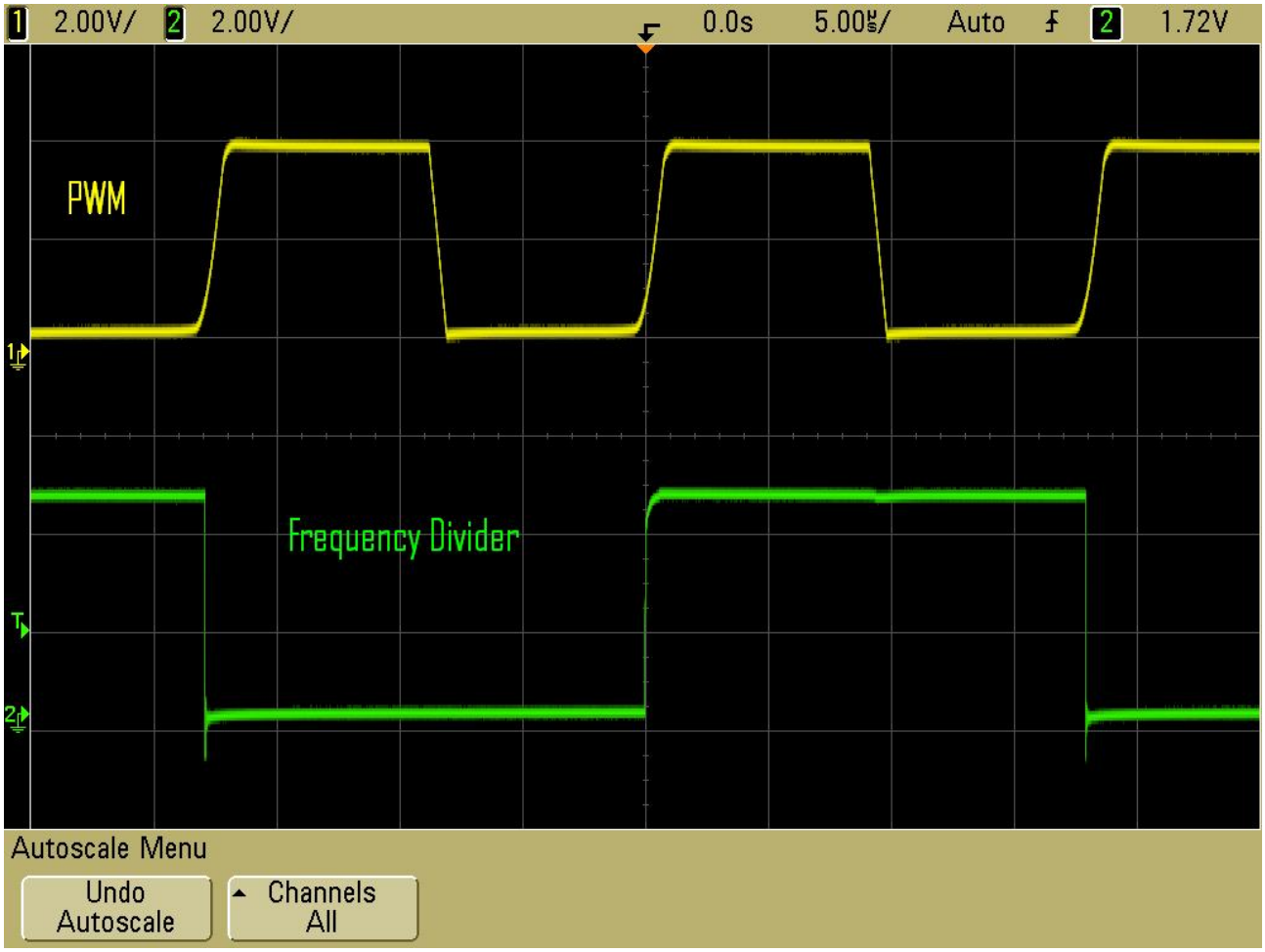


Figure 33: PWM used in frequency divider

The NAND gates as inputs take the PWM and then either the inverting or non-inverting input of the frequency divider and produces the output shown in Figure 34. This signal is then used as input to the drivers which tell the MOSFETs when to turn on. Using this implementation also prevents the MOSFETs from being turned on at the same time.

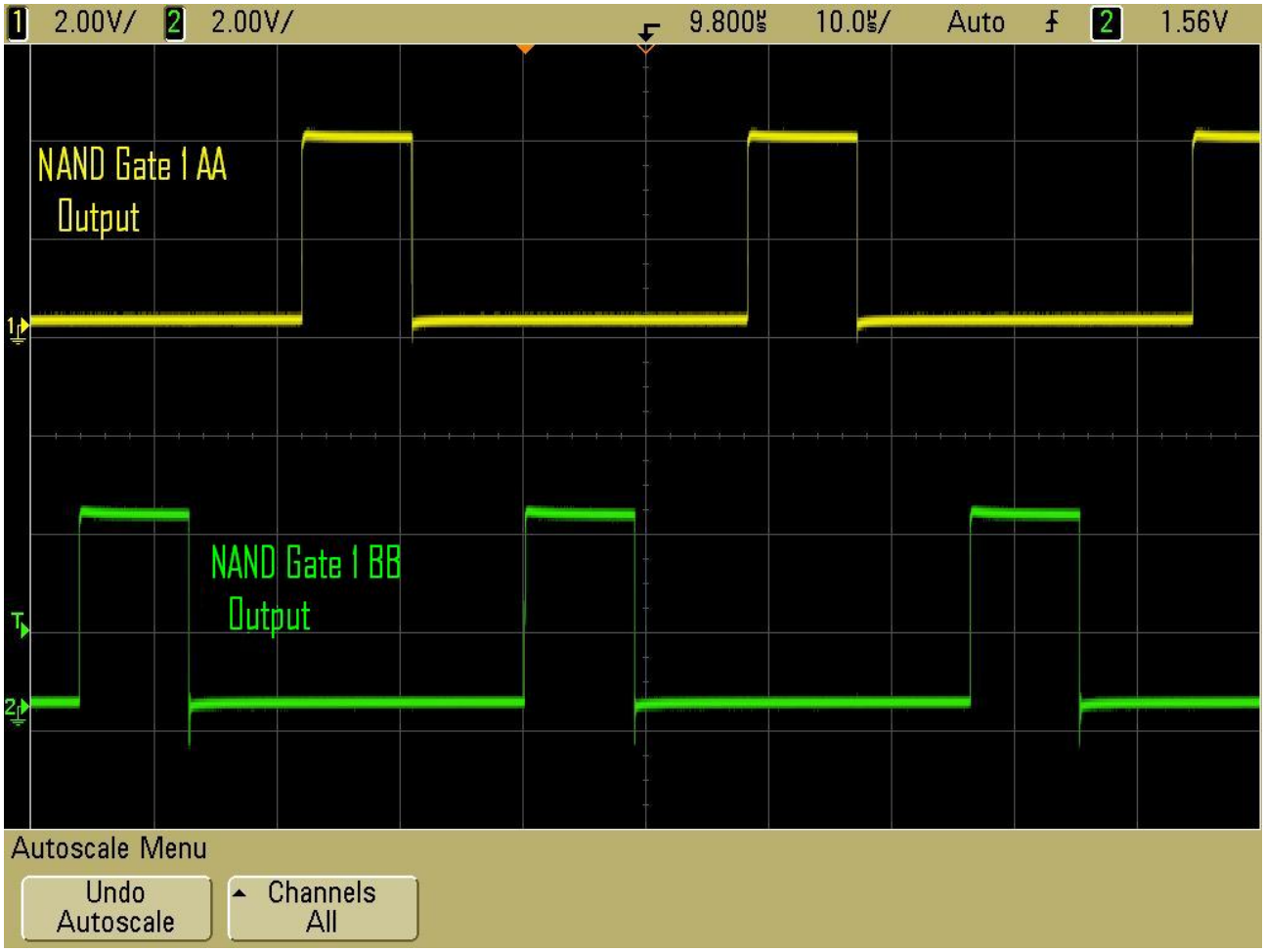


Figure 34: NAND gate output

17.1.2 Control Side Current Draw

After discussing with a couple professors, it was found that the power consumed on the control side of the board was too high. The control side was drawing 1.12 W, at 12 volts means there was 93 mA of current. After some analysis, it was found that the D Flip-Flop and the NAND gate were drawing extra current because the unused sides of those IC's were tied to ground. When IC's have their unused inputs tied to ground they don't draw extra current, but when the unused outputs are tied to ground, they are going to draw more current. With this known, the unused outputs were removed from ground, but the unused inputs were left tied to ground. This significantly reduced the amount of current being drawn, and the power used as well. Now the control side is drawing 30 mA of current at 12 volts, meaning it uses 360 mW of power – that's more than a one-third reduction in the amount of power used!

17.2 Power testing

The testing of the power side was completed in two steps. The first stage was using a power supply to source the 12 volts input to the converter. The purpose of the power supply is to be able to limit the current entering the system. By limiting the current to a few amps, the likelihood of components overheating from a short circuit is reduced. The power supply also allowed for a precise input voltage. The second stage was to do a high current test. The source for this test was a 12 volt car battery. On the high current test, a high power load was also used to ensure power transfer through the circuit.

17.2.1 Current limited

To safely test and find any shorts in the circuit, a power supply was used by providing 12 volts and 2 amps. The fuse being used during this test had too high of a current rating – the traces on the board would melt before the fuse blew – so a light bulb was used in place of the fuse. This helped verify that the MOSFETs were switching accurately without burning them out. To remove noise on the gate of the MOSFET, a 330µF capacitor (by-pass cap) was added across the power supply, a revised schematic of the power side can be seen in Figure 35.

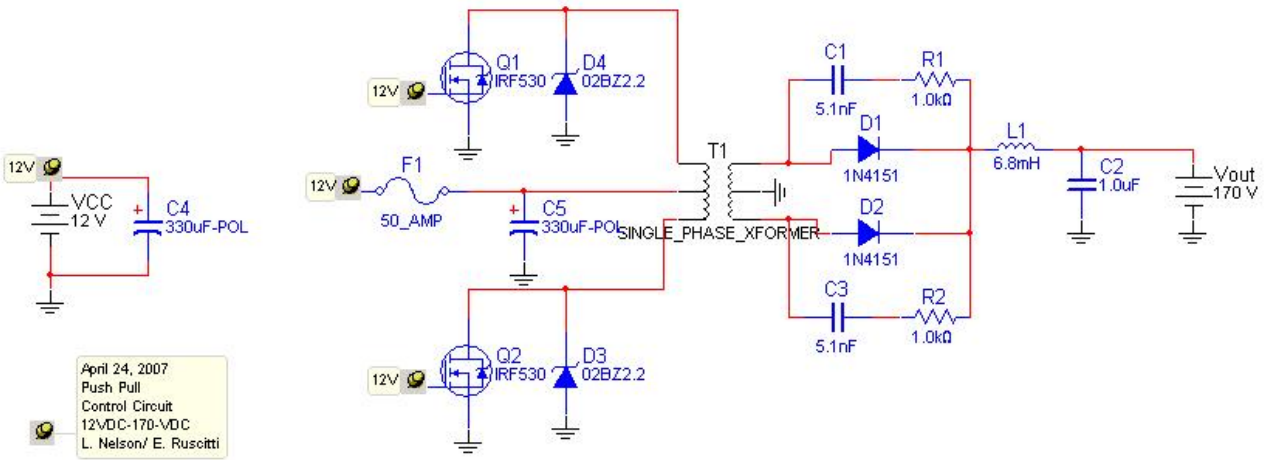


Figure 35: Final power schematic

As expected, when the duty cycle was adjusted the output voltage changed proportionally. However, the proportional change was inversely proportional, which was not expected – they should be directly proportional to one another. The reason for this turned out to be the two pairs of wires on the transformer's secondary side were inverted on the board. The wires that were tied to ground were supposed to be connected to the diodes, and vice-versa. To fix this, the wires were un-

soldered, then re-soldered in the correct configuration. When this was done, the current through the transformer increased as the duty cycle increased, which is what was expected from simulations. To more accurately see what was happening at the output, the inductor of the LC filter was removed to minimize the amount of oscillation. With the inductor temporarily removed, voltage peaks were seen around 95 volts with a duty cycle of just 10%!

17.2.2 Full scale test

The high current test was done using a 12 volt car battery as the source, shown in Figure 36. To protect the circuitry, the first power up test was completed using a 5 amp fuse to the switching MOSFETs. When the current draw increased over 5 amps, the power would disconnect from the transformer, allowing the control loop to function normally. All testing at the high current level was done in pulses, so that the converter was not operating for more than a few seconds at a time to diagnose issues found. To control the PWM during the high current test, a power supply was used to set the biased point of the comparator instead of through the closed loop. As a load, a 100 volt, 40 watt light bulb was attached to the output.

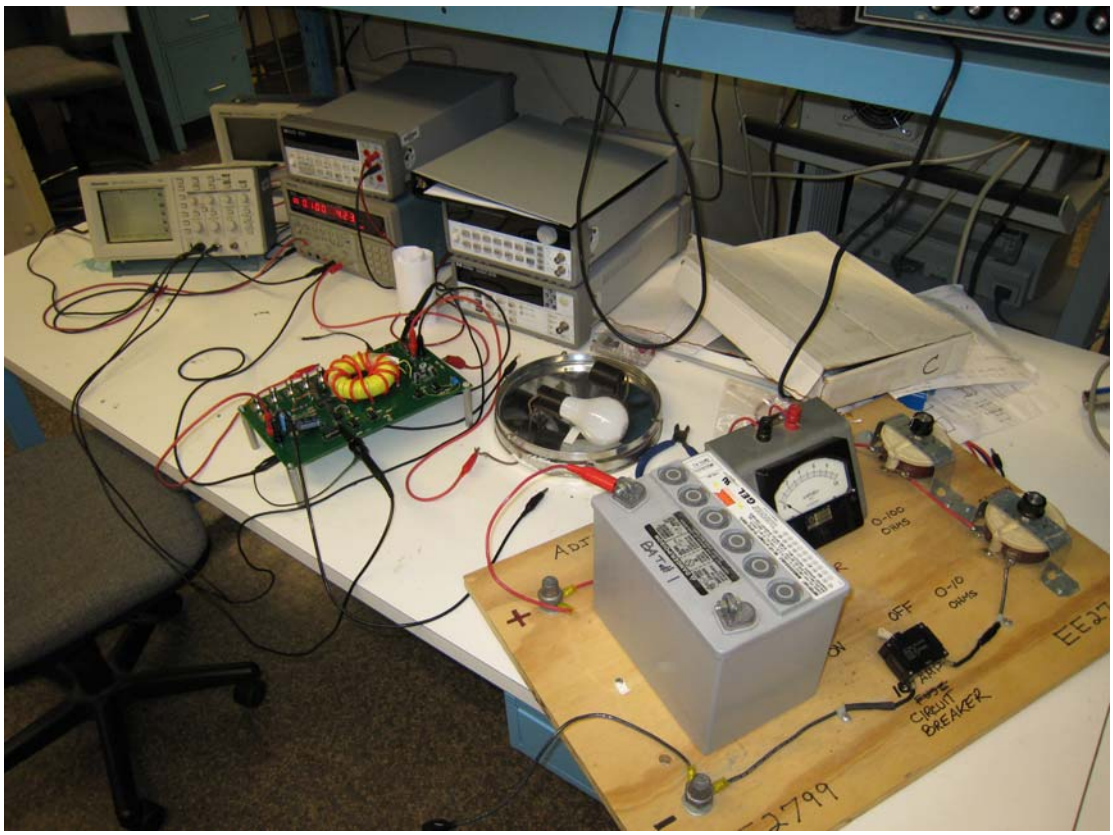


Figure 36: Setting up the high power test

The first power up lasted approximately two seconds. Within that amount of time the 5 amp fuse melted. However the light bulb did become very bright for that duration. At this point it was determined to increase the fuse to 15 amps. When powered up again, the light bulb stayed lit and the fuse did not blow instantly. During the 15 amp test, the waveforms of the output and gate voltages were measured, shown in Figure 37. The correlation between when the gate turned on and ripple in the output was very noticeable. During this stage the output ripple was ~50 volts with a dc level of ~125 volts. The size of the ripple was due to the lack of inductor in the circuit for the testing.

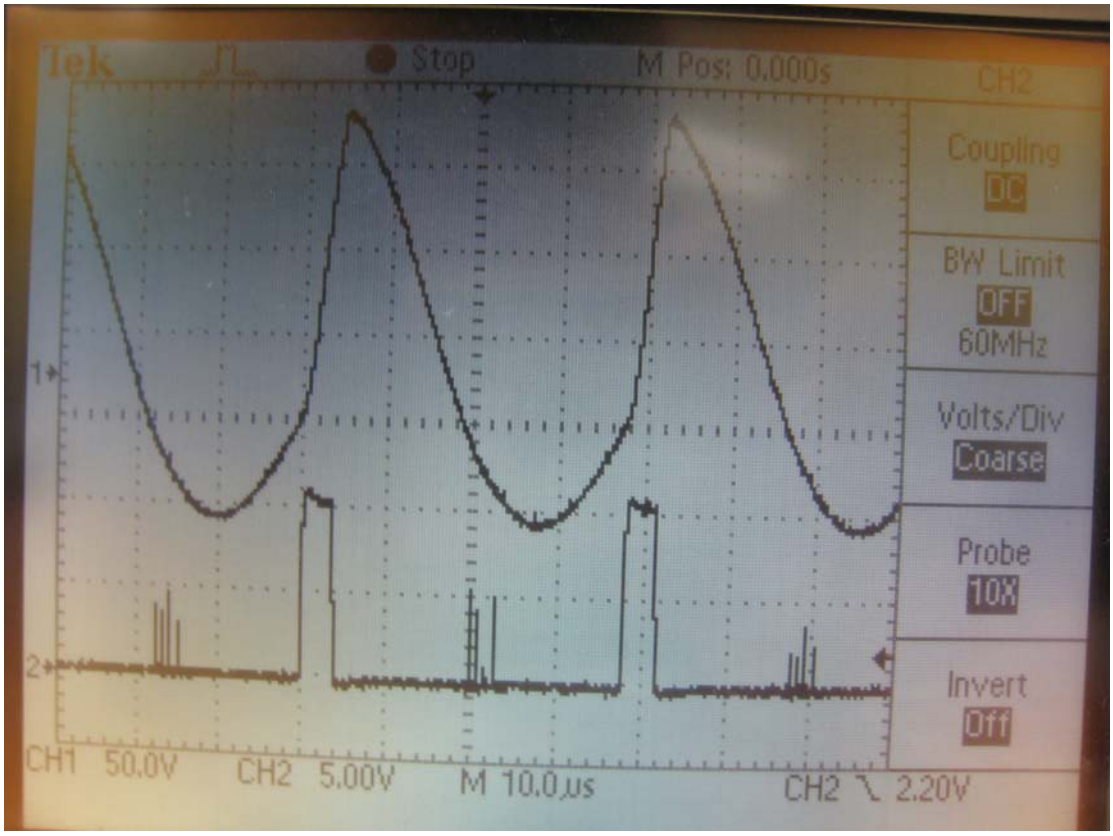


Figure 37: Output of high power test

In order to see if the brightness, and therefore power output of the converter could be increased, the duty cycle of the PWM was increased to ~40%. At this point two major observations in the operation occurred. The RC snubber circuits were designed with a resister not capable of dissipating the amount of energy being fed into them. During the next power up, the resistors emitted smoke and then began to shoot blue sparks. The remains of the snubber circuit can be seen in Figure 38. The other observation was that only one of the two MOSFETs were switching. After

turning off the circuit and checking the driver circuit on the non functional MOSFET, no issues were found. This leads to the assumption that the MOSFET was damaged either by heat applied to the gate when re-soldering a joint, or some unpredicted interaction with the transformer's inductance.

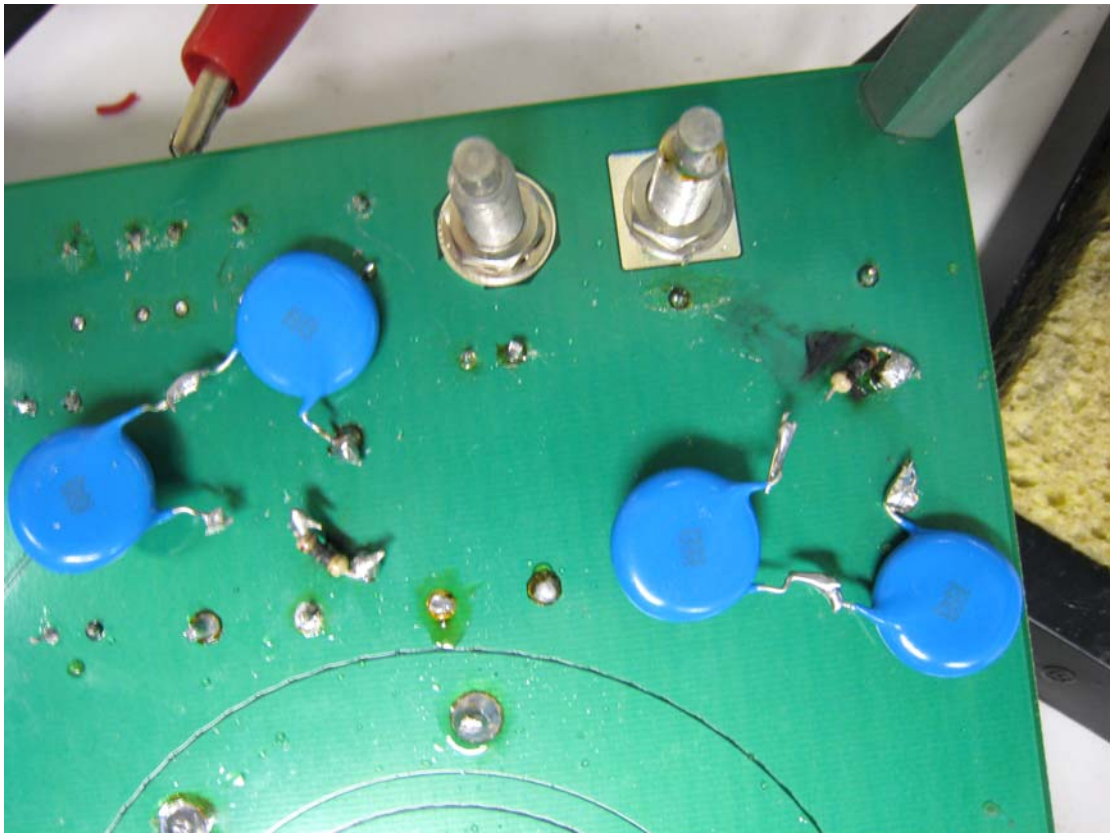


Figure 38: RC snubber

18 Results

With all the re-work done to the board, Figure 39, an output was finally obtained!

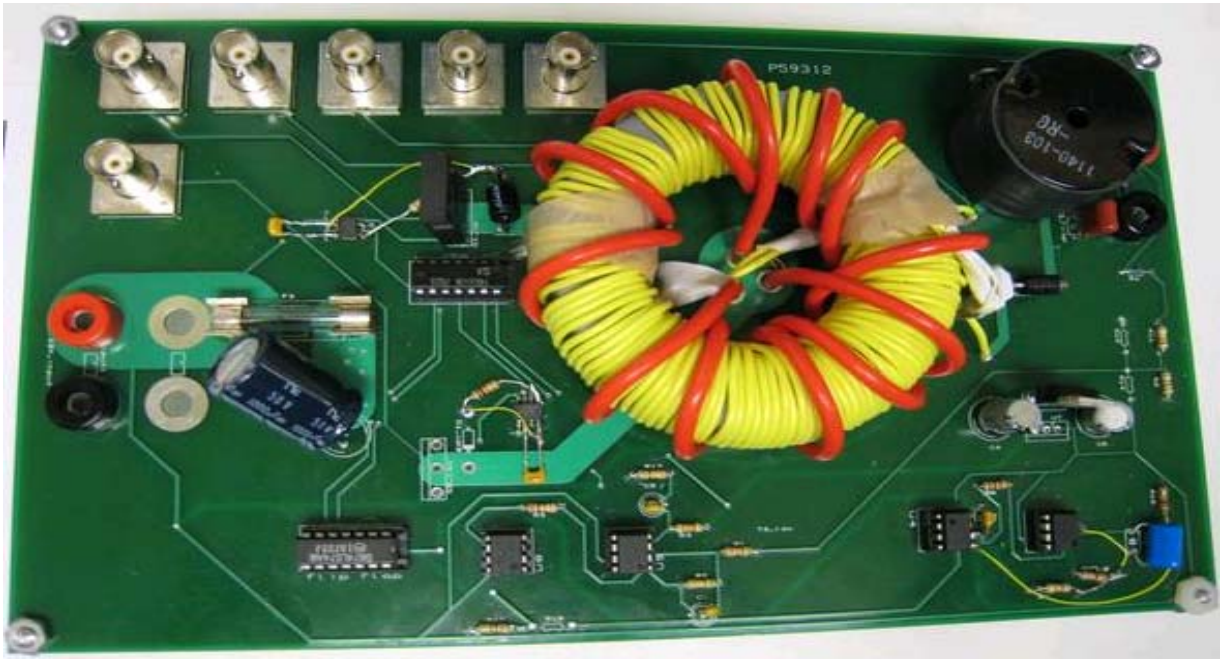


Figure 39: PCB with revisions

As can be seen from the graphs in the testing section, the circuit is working. The controls are working perfectly and only have a power loss of 360 mW. The power side has some room for improvement. The switching MOSFETs are not working as expected. One of the two MOSFETs is turning on and off; the other would not turn on during high current testing, but worked afterwards during low current testing. The MOSFET that was switching was getting extremely hot, using an infrared temperature sensor, a temperature of over 180°F was recorded after short durations of testing. When working off one switching MOSFET, voltages around 120 volts with a ripple of approximately 50 volts were observed when tested without an inductor in the LC filter.

19 Design Conclusion

Changes were made to the design of the PCB both before and after it was received. Had all the necessary changes been caught before the board was sent out to be made, it would have saved a lot of time and frustration later on. The controls are working, but there are issues getting the MOSFETs to switch as expected during high current testing. Adjustments in the input voltage to the controls changes the duty cycle of the PWM as expected. The first time the transformer was turned on, there was smoke – a few components had to be replaced. After taking another look at the data sheets and revising the board a little an output was obtained, although it was just able to power a 40 W light bulb with a voltage of approximately 120 volts.

20 Costs

One question you might have at this point is if the device was fully operational and you had a sine wave inverter to attach to the 170 volt output, how much would the DC-DC converter cost? To answer your question, let's look at Figure 40. As you can see from this Bill of Materials, it will cost approximately $81 just for the components to assemble this device, with the transformer consisting of about half the cost. The full Bill of Materials with vendor names and part numbers can be found in Appendix E: Bill of Materials. Please note that these prices are based on Digikey and ECE shop prices. Also note that all components ordered were in small quantities so there might be volume discounts that do not apply here.

Quantity	Description	Price
2	RESISTOR, 1.0kOhm_5%	$ 0.10000
2	CAPACITOR, 5.1nF	$ 0.47200
1	CAPACITOR, 1.0uF	$ 0.25000
2	ZENER, 02BZ2.2	$ 0.99000
2	POWER_MOS_N, IRF530	$13.00000
1	Transformer	$39.76000
1	INDUCTOR, 10mH	$ 9.56000
2	DIODE, 1N4151	$ 0.01050
1	50_AMP, 50_AMP	$ 0.25000
1	Banana Jack	$ 7.93000
1	RESISTOR, 1.0kOhm_5%	$ 0.10000
1	RESISTOR, 10kOhm_5%	$ 0.10000
5	RESISTOR, 20kOhm_5%	$ 0.10000
1	CAPACITOR, 1.0nF	$ 0.25000
1	CAPACITOR, 10nF	$ 0.25000
2	CAP_ELECTROLIT, 100uF-POL	$ 1.00000
1	RESISTOR, 7.5kOhm_5%	$ 0.10000
2	RESISTOR, 200kOhm_5%	$ 0.10000
1	VOLTAGE_REGULATOR, LM7805CT	$ 0.60000
4	OPAMP, TL082CP	$ 0.64000
2	74LS, 74LS08D	$ 0.53000
1	74STD, 7474N	$ 0.53000
2	SOCKETS, DIP8	$ 3.20000
1	RESISTOR, 200Ohm_5%	$ 0.10000
1	RESISTOR, 100Ohm_5%	$ 0.10000
1	RESISTOR, 180kOhm_5%	$ 0.10000
1	RESISTOR, 5.1kOhm_5%	$ 0.10000
2	RESISTOR, 510kOhm_5%	$ 0.10000
2	RESISTOR, 51kOhm_5%	$ 0.10000
2	CAPACITOR, 22nF	$ 0.25000
1	RESISTOR, 300Ohm_5%	$ 0.10000
		$80.77250

Figure 40: Bill of Materials for DC-DC converter

21 Recommendations

After completing this project and learning what to do and some things not to do, some recommendations are going to be made for any future groups working on this or any similar project.

The first recommendation is to consult more with power engineers. These engineers deal with power all day, they will be able to help you a lot and you will be able to make more progress on the project in a shorter amount of time.

The next couple of recommendations have to do with component selection. When picking components, make sure they are capable of handling the expected voltages/currents. Be aware of any offset or inverting properties of the components being chosen and where unused pins should be connected. Use DIP or TO components. These types of components are easy to test on breadboards and on PCBs. When soldering onto the PCB, use as many sockets as possible. In this project a couple of frequency dividers and logic gates were blown. It would have been very tedious and time-consuming to unsolder the chip and solder in a new one. By soldering sockets into the PCB, you are making it as easy to swap out components as if you were working on your breadboard.

Isolation. Learn about the different types of isolation early and start testing them to see how they respond. Isolation is very important in power applications.

These last couple recommendations deal with PCB layout. Make sure all IC's are facing the same direction. If you have four op-amps, and three of them are facing one way, do not turn the fourth on in another direction even if it does make it easier to draw traces. If someone is just putting the components in and not paying attention to the schematic, there is a very real possibility the IC will be put in backwards. Double and even triple check that all traces are correct before sending the PCB to be made. Its one thing to have to add resistors and capacitors to make an IC work, but if you have to cut traces and then physically re-wire the circuit, it is going to take a lot of time. If you are making a large board, have holes drilled in each of the four corners for legs to be inserted to hold it up, depending on size, you might even want a fifth hole drilled near the center of the board where it is more pliable. Although it might make things a bit more visually difficult to understand, make good use of your board space. Spacing components out and grouping them by task may make it easier to visually pick out what is going on, but if an engineer were to see it, he or she might think you don't know what you're doing.

These are all the recommendations that are going to be made. Hopefully it will help future groups make better use of their time and resources.

22 Overall Conclusion

Based on the research that was done, there is a need for 12 volt to 170 volt DC-DC converters, especially when being used with sine wave inverters. For the desired power rating of 250W, a push pull topology seems to work best with an efficiency rating of 85% at 350W. Half bridge and full bridge operate at much higher power ratings.

Based on schematics and simulations, the device should have worked, however before the design could even be tested changes were made to ensure it worked. Once testing began, revisions to the board continued with each change that was made, an updated schematic was made as well. This was in case there was time to get a new board printed that had all the corrections on it.

Even with modifications to the design, the board still did not work the first time it was connected to power. More changes were made and now the device works, although not as expected. The MOSFETs are not switching as expected during high current tests. On a slightly more upbeat note, the power lost through the control circuitry is only 360 mW.

Although the board might not work as expected, a lot was learned by both team members in terms of researching existing products, finding components to give desired results, schematic and PCB layout skills, debugging and on-demand circuit re-work skills. These skills and experiences they have gained will be kept in their “ECE toolbox” for later use.

Works Cited

Hill, C. J. Switch Mode Power Supplies. Ed. C. J. Hill. 15 Mar. 1998. 16 Sept. 2006 <http://www.hills2.u-net.com/electron/smps.htm>.

Push-pull converter. 2006. Wikipedia. 15 Sept. 2006 <http://www.answers.com/topic/push-pull-converter>.

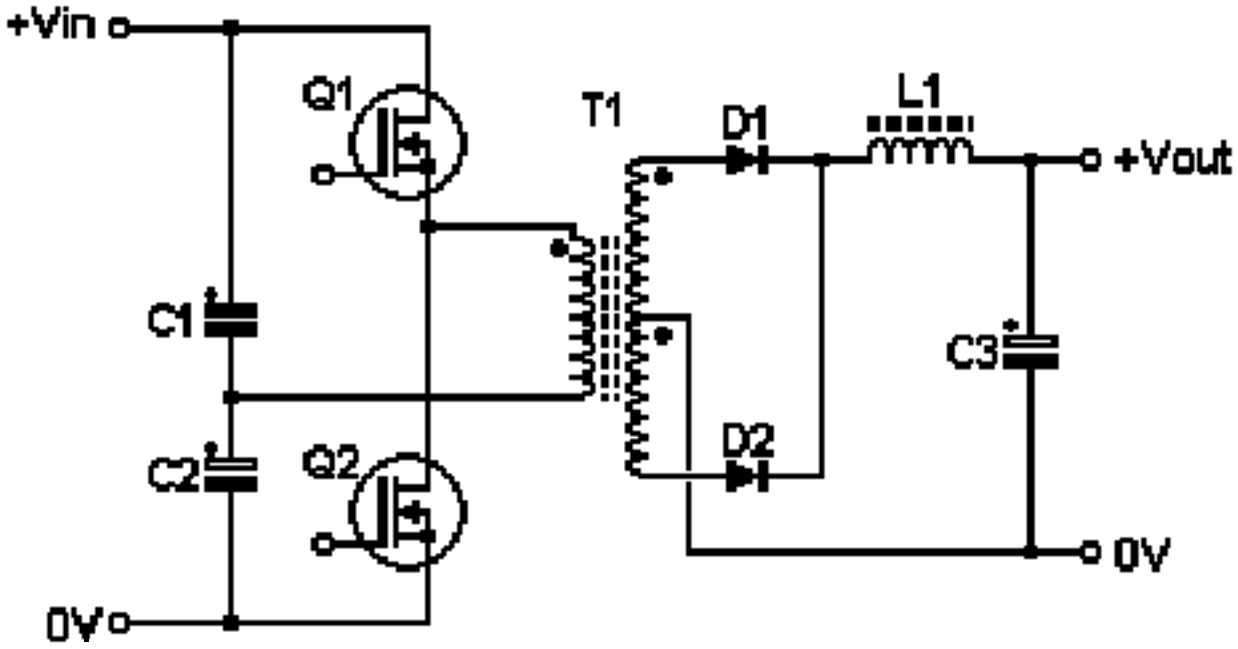
Switched-mode power supply. 28 Sept. 2006. 30 Sept. 2006 <http://en.wikipedia.org/wiki/Switched_mode_power_supply>.

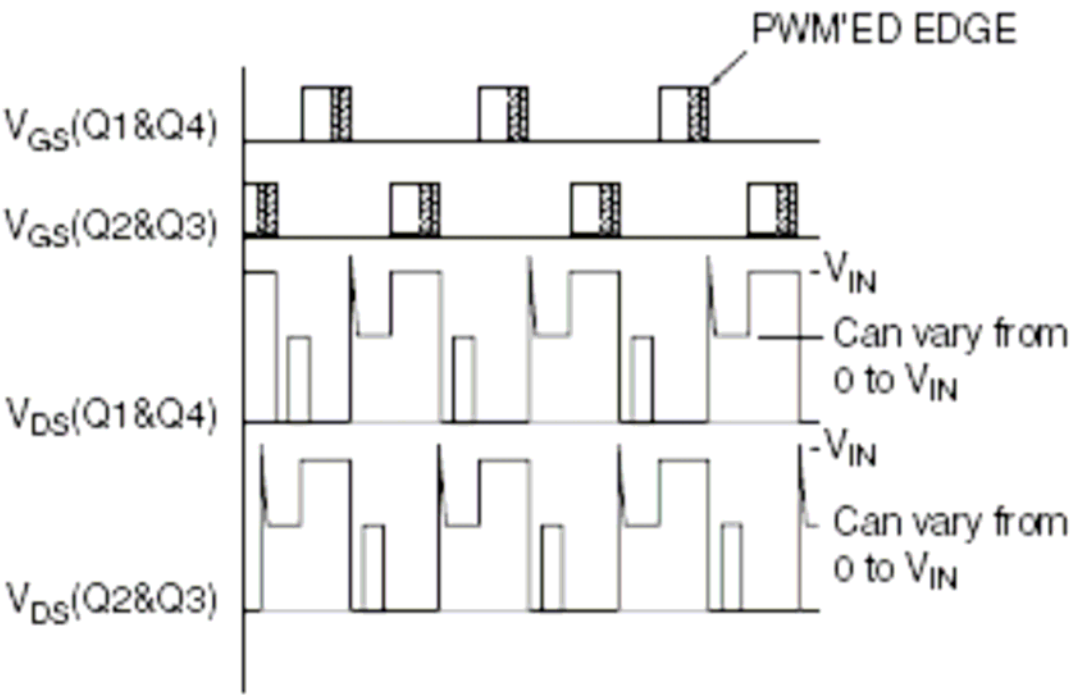
Wagner, J. Solid state tesla coils - general notes. Ed. J. Wagner. 2003. 27 Sept. 2006 <http://users.tkk.fi/~jwagner/tesla/SSTC/general-sstc-notes-topology.htm>.

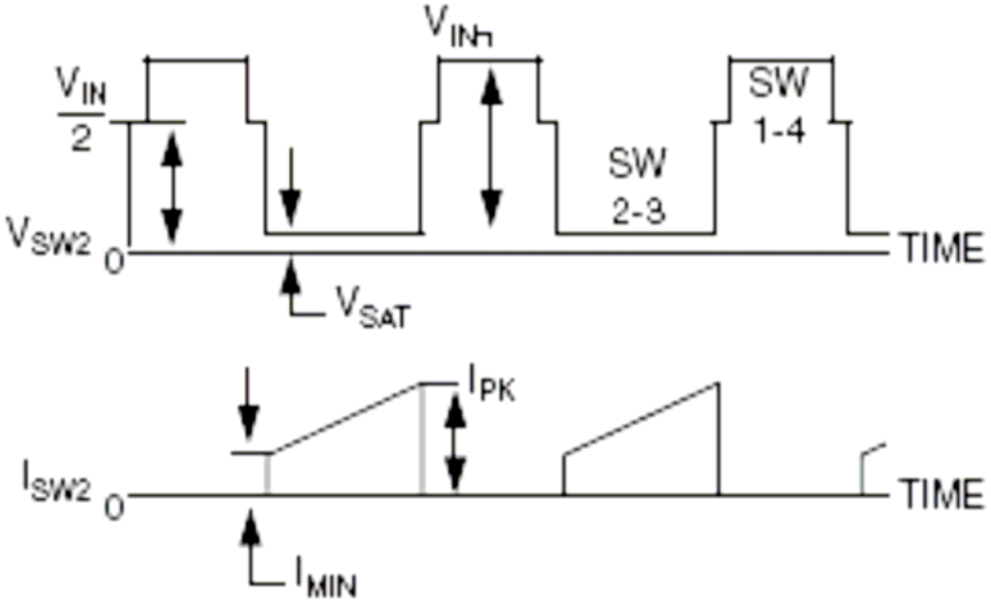
Emanual, Alexander. "Transformer design." WPI, WPI campus. 20 Nov. 2006

ANSI PCB Trace Width Calculator. Nick de Smith. 2 Dec. 2004. 18 April 2007. <http://www.desmith.com/NMdS/Electronics/TraceWidth.html>

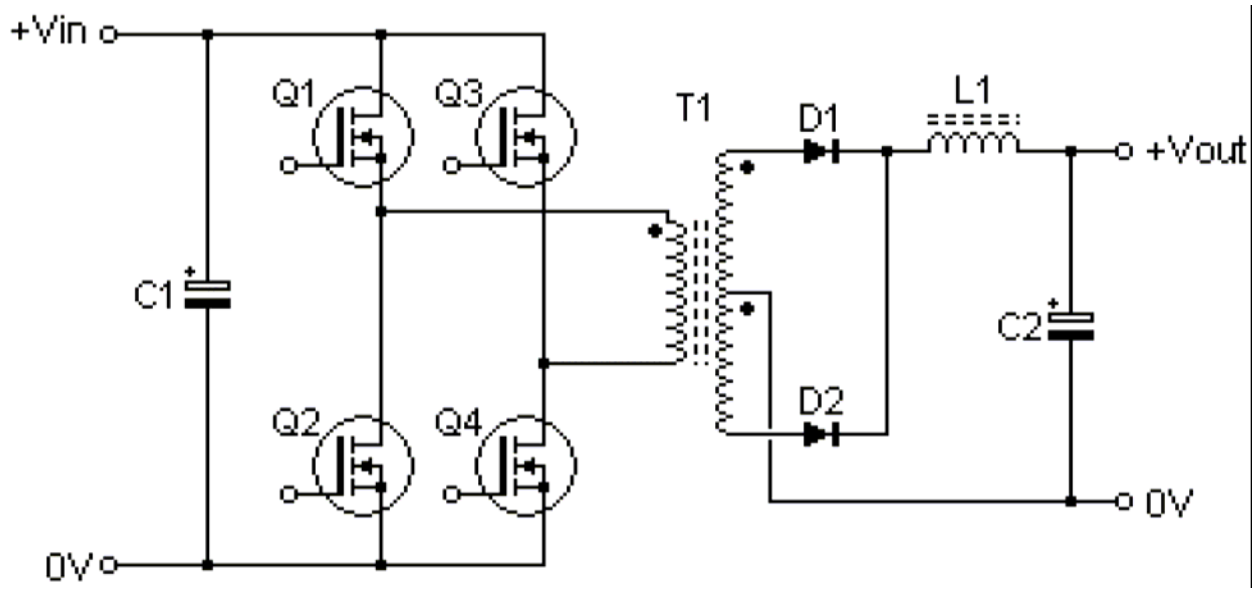
Appendix A: Half Bridge

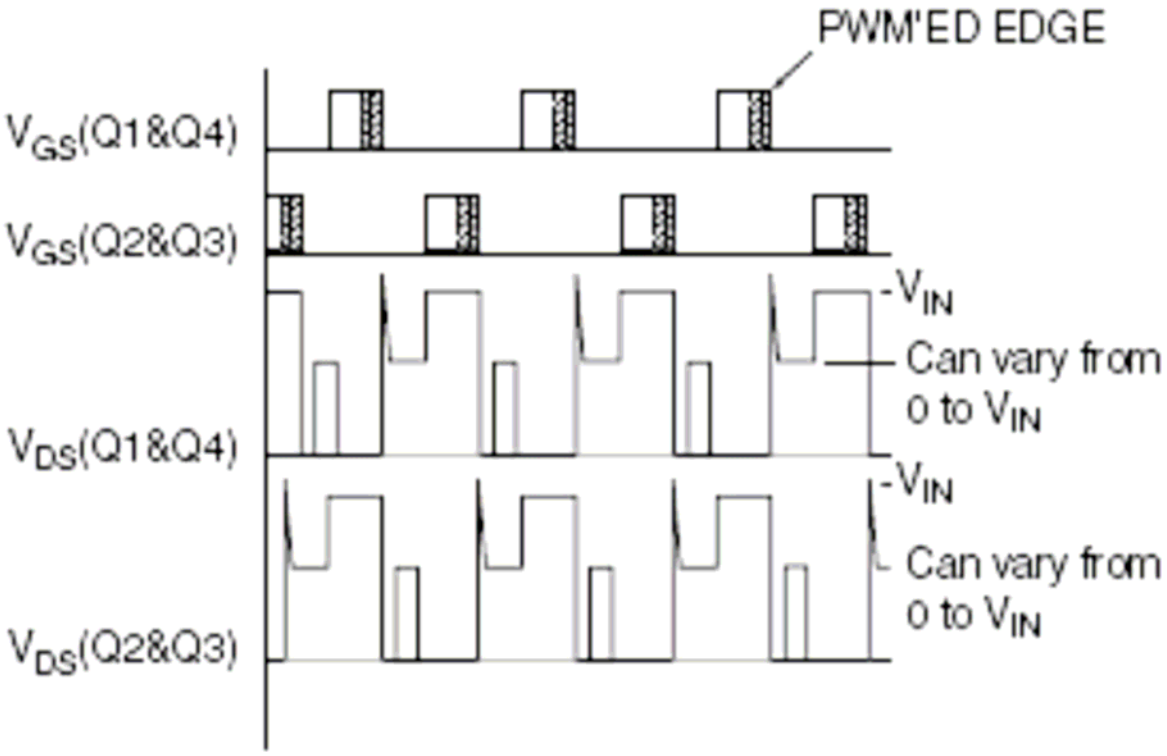


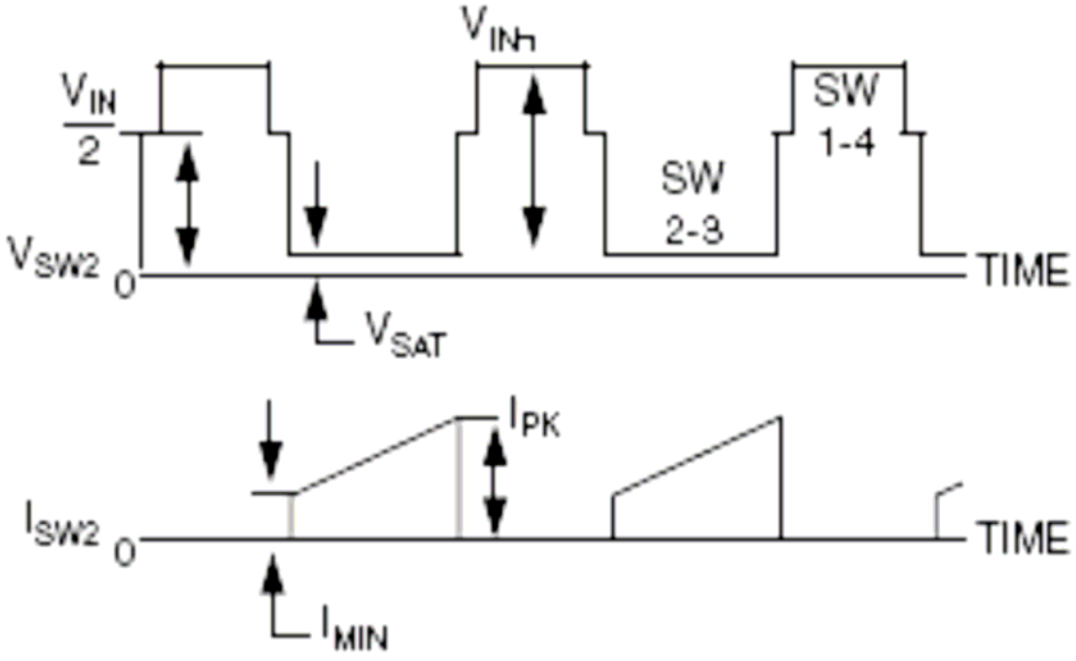

PWM'ED EDGE
V_{GS}(Q1&Q4)
V_{GS}(Q2&Q3)
V_{DS}(Q1&Q4)
V_{DS}(Q2&Q3)
V_{IN}
Can vary from 0 to V_{IN}
V_{IN}
Can vary from 0 to V_{IN}


V_{IN}
$\frac{V_{IN}}{2}$
SW 1-4
SW 2-3
V_{SW2}
0
TIME
V_{SAT}
I_{PK}
I_{SW2}
0
TIME
I_{MIN}

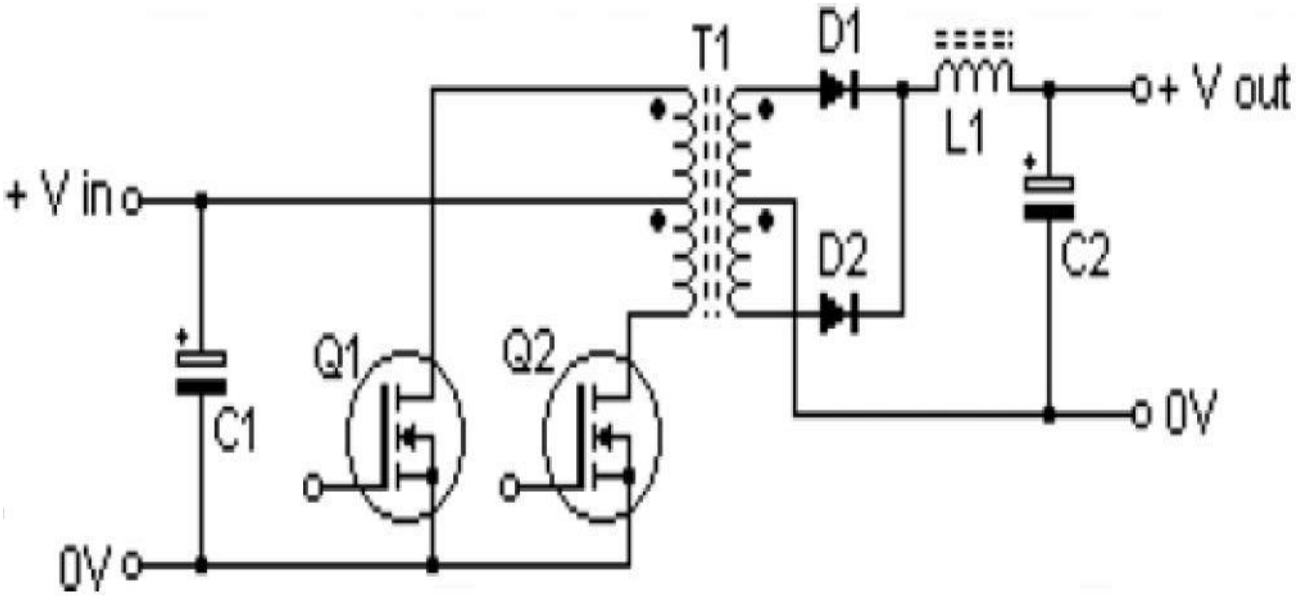
Appendix B: Full Bridge

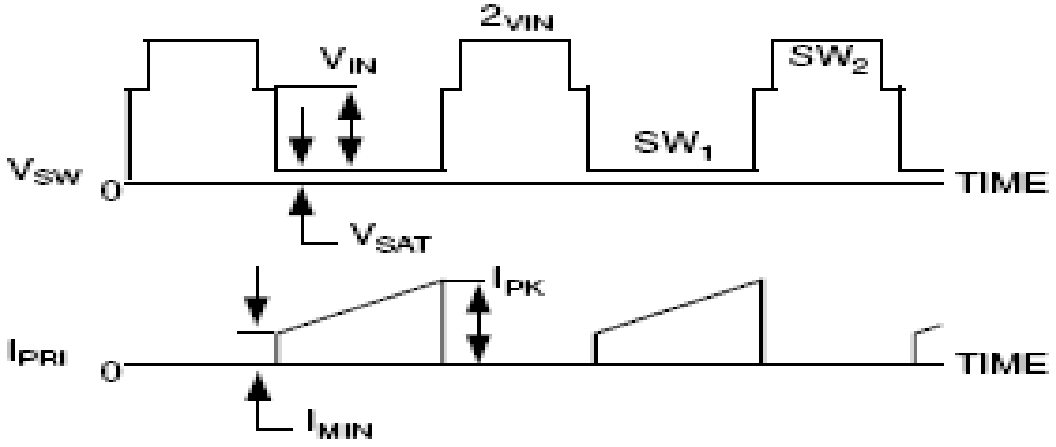


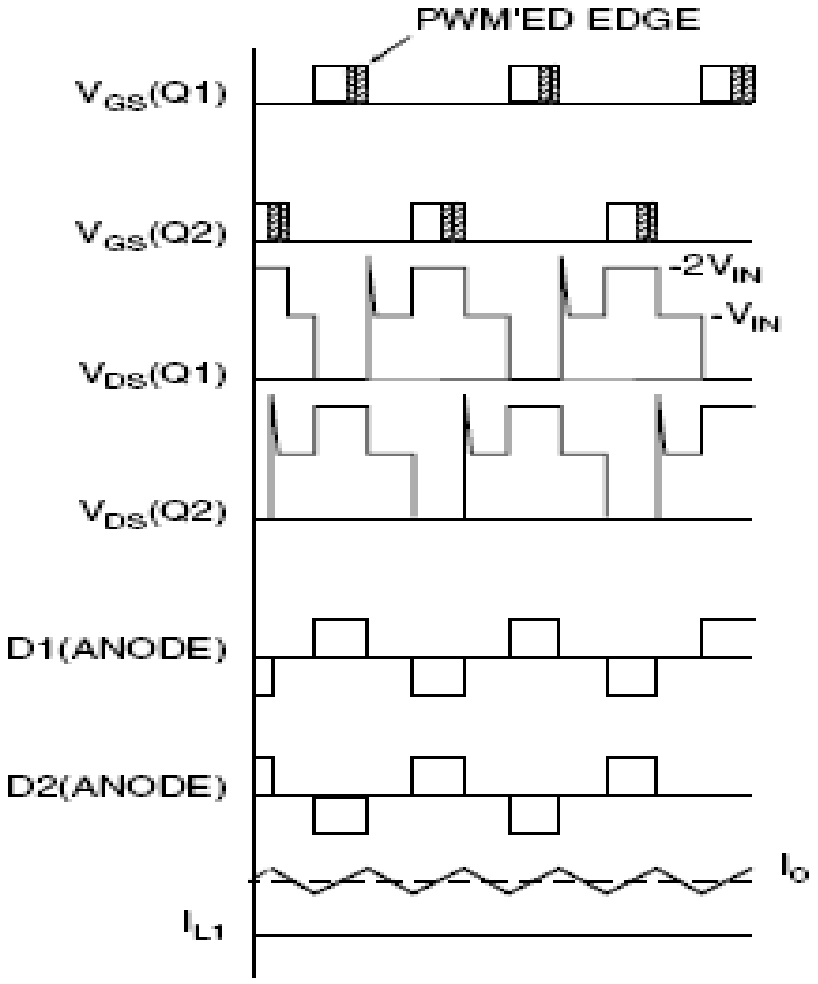

PWM'ED EDGE
V_{GS}(Q1&Q4)
V_{GS}(Q2&Q3)
V_{DS}(Q1&Q4)
V_{DS}(Q2&Q3)
V_{IN}
Can vary from 0 to V_{IN}
V_{IN}
Can vary from 0 to V_{IN}


V_{IN}
$\frac{V_{IN}}{2}$
SW 1-4
SW 2-3
V_{SW2}
0
TIME
V_{SAT}
I_{PK}
I_{SW2}
0
TIME
I_{MIN}

Appendix C: Push Pull




2VIN
VIN
SW2
SW1
VSW
0
TIME
VSAT
IPK
IPRI
0
TIME
IMIN


PWM'ED EDGE
VGS(Q1)
VGS(Q2)
-2VIN
-VIN
VDS(Q1)
VDS(Q2)
D1(ANODE)
D2(ANODE)
Io
IL1

Appendix D: Value Analysis Chart

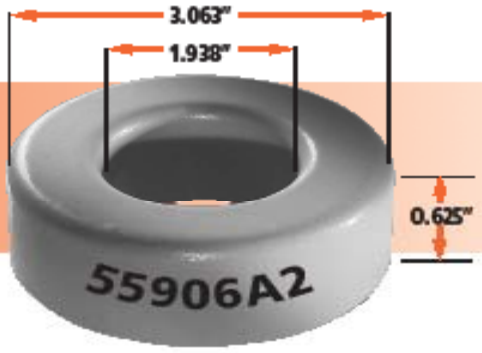
	Transformer windings	Max Duty Cycle per MOSFET	Efficiency	Cost (relative percent)	Cost (Digi-Key)	Complexity (# component)	Max Output Power	Power density	Raw Score	Weighted Score
Weighting	85	70	100	10	50	30	60	35	RS	WS
Buck-Boost			4		4	5			13	750
Forward	3	0	3	5		4	1		16	785
Flyback	2	0	2	5	2	4	0		15	640
Half-Bridge	2	1	4	1		2	2	1	13	865
Full-Bridge	2	1	4	1		1	4	2	15	990
Push-Pull	3	1	3	2	0	2	4		15	945
Zero Voltage			3				4		7	540

Appendix E: Bill of Materials

Quantity	Description	RefDes	Package	Vendor	Status	Price	Vendor Part	Manufacture	Manufacture
2	RESISTOR, 1.0kOh	R2, R1	Generic\RES	ECE Shop		$ 0.10000			
2	CAPACITOR, 5.1nF	C3, C1	Generic\CAP	Digikey		$ 0.47200	445-2429-ND	TDK Corpor	CS17-F2GA
1	CAPACITOR, 1.0uF	C2	Generic\CAP	ECE Shop		$ 0.25000			
2	ZENER, 02BZ2.2	D4, D3	Generic\DO-35			$ 0.99000		ST Microele	STTH5L06R
2	POWER_MOS_N, I	Q2, Q1	Generic\TO-220AB			$ 13.00000		ST Microele	Y140NS10
1	Transformer			Magnetics		$ 39.76000			
1	INDUCTOR, 10mH	L1	Generic\IND5			$ 9.56000		JW Miller A	1140-103K-I
2	DIODE, 1N4151	D2, D1	Generic\DO-35			$ 0.01050		Fairchild Se	1N4151
1	50_AMP, 50_AMP	F1	Generic\FUS	ECE Shop		$ 0.25000			
1	Banana Jack	12V input1		Digikey		$ 7.93000		Pomona Ele	MDP-02
1	RESISTOR, 1.0kOh	R5	Generic\RES	ECE Shop		$ 0.10000			
1	RESISTOR, 10kOhr	R7	Generic\RES	ECE Shop		$ 0.10000			
5	RESISTOR, 20kOhr	R8, R11, R14,	Generic\RES	ECE Shop		$ 0.10000			
1	CAPACITOR, 1.0nF	C2	Generic\CAP	ECE Shop		$ 0.25000			
1	CAPACITOR, 10nF	C3	Generic\CAP	ECE Shop		$ 0.25000			
2	CAP_ELECTROLIT,	C4, C6	Generic\ELK	ECE Shop		$ 1.00000			
1	RESISTOR, 7.5kOh	R6	Generic\RES	ECE Shop		$ 0.10000			
2	RESISTOR, 200kOh	R10, R13	Generic\RES	ECE Shop		$ 0.10000			
1	VOLTAGE_REGULA	U6	Generic\TO-	ECE Shop		$ 0.60000		ST Microele	L7805CV
4	OPAMP, TL082CP	U3, U8, U4, U5	Generic\PDI	ECE Shop		$ 0.64000		Texas Instru	TL082CP
2	74LS, 74LS08D	AND_Gate1_A	Generic\DO1	ECE Shop		$ 0.53000		Fairchild Se	74LS08
1	74STD, 7474N	flip_flop	Generic\NO1	ECE Shop		$ 0.53000		Texas Instru	7474N
2	SOCKETS, DIP8	Driver1, Driver	Generic\DIP-8			$ 3.20000		National Se	LM5104
1	RESISTOR, 200Ohr	R17	Generic\RES	ECE Shop		$ 0.10000			
1	RESISTOR, 100Ohr	R19	Generic\RES	ECE Shop		$ 0.10000			
1	RESISTOR, 180kOh	R4	Generic\RES	ECE Shop		$ 0.10000			
1	RESISTOR, 5.1kOh	R9	Generic\RES	ECE Shop		$ 0.10000			
2	RESISTOR, 510kOh	R2, R12	Generic\RES	ECE Shop		$ 0.10000			
2	RESISTOR, 51kOhr	R1, R3	Generic\RES	ECE Shop		$ 0.10000			
2	CAPACITOR, 22nF	C1, C5	Generic\CAP	ECE Shop		$ 0.25000			
1	RESISTOR, 300Ohr	R18	Generic\RES	ECE Shop		$ 0.10000			

Appendix F: Transformer Spec Sheet

77.8 mm O.D.
49.2 mm I.D. x 15.9 mm HT.



Core Dimensions (after finish)		
O.D. (max.)	78.9 mm	3.108 in
I.D. (min.)	48.2 mm	1.898 in
HT. (max.)	17.02 mm	0.670 in

Permeability (μ)	A_L ± 8%	Part Number			Nominal DC Resistance Ohms/mH*	B/NI Gauss per Amp. Turn*
		MPP	High Flux	Kool Mμ		
14	20	55909	58909	-	-	-
26	37	55908	58908	77908	-	-
60	85	55907	58907	-	-	-
125	178	55906	58906	-	-	-

Physical Characteristics		
Window Area	17.99 cm²	3,550,000 c.mils
Cross Section	2.27 cm²	0.352 in²
Path Length	19.95 cm	7.86 in
Volume	45.3 cm³	2.77 in³
Weight- MPP	377 gm	0.832 lb
Weight- High Flux	356 gm	0.785 lb
Weight- Kool Mμ	279 gm	0.615 lb
Area Product	40.8 cm⁴	0.982 in⁴

Winding Turn Length		
WINDING FACTOR	LENGTH/TURN	
100% (Unity)	11.00 cm	0.361 ft
60%	9.24 cm	0.303 ft
40%	7.53 cm	0.247 ft
20%	6.80 cm	0.223 ft
0%	6.52 cm	0.214 ft

Wound Coil Dimensions		
Max. O.D. (u.w.f.)	113 mm	4.45 in
Max. HT. (u.w.f.)	57.7 mm	2.27 in

Surface Area		
Unwound Core	130 cm²	20.1 in²
40% Winding Factor	225.2 cm²	34.90 in²

AWG Wire Size	Turns (u.w.f.)	Rdc (Ohms, Ω) (u.w.f.)	Single Layer Turns	Single Layer Rdc. (Ohms, Ω)
8	197	0.0418	41	0.00612
9	248	0.0705	47	0.0088
10	309	0.1115	53	0.0125
11	388	0.1766	60	0.018
12	486	0.278	67	0.0253
13	608	0.437	76	0.036
14	760	0.69	84	0.0503
15	944	1.085	95	0.0716
16	1182	1.716	106	0.101
17	1465	2.67	119	0.143
18	1830	4.23	134	0.203
19	2275	6.61	150	0.286
20	2840	10.4	168	0.404
21	3550	16.4	188	0.57
22	4390	25.7	211	0.812
23	5470	39.7	235	1.13
24	6770	62.9	263	1.44
25	8350	97.7	295	2.04
26	10450	154.8	330	2.89
27	13150	243.1	365	4.01

Core Data

* These values are only applicable for MPP Cores.

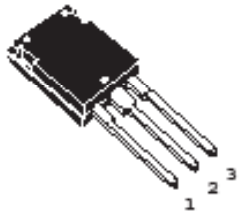
Appendix G: MOSFET Spec Sheet

STY140NS10

N-CHANNEL 100V - 0.009 Ω - 140A MAX247™
MESH OVERLAY™ POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STY140NS10	100V	<0.011Ω	140A

- TYPICAL $R_{DS}(on)$ = 0.009Ω
- STANDARD THRESHOLD DRIVE
- 100% AVALANCHE TESTED

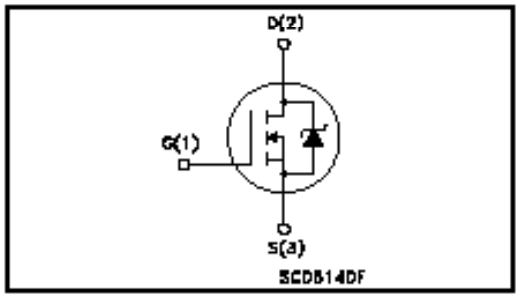


Max247™

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SWITCHING SPEED
- SWITCH MODE POWER SUPPLY (SMPS)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	100	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuos) at T_C = 25°C	140	A
I_D	Drain Current (continuos) at T_C = 100°C	99	A
I_{DM}(•)	Drain Current (pulsed)	560	A
P_{tot}	Total Dissipation at T_C = 25°C	450	W
	Derating Factor	3	W/°C
E_{AS}(1)	Single Pulse Avalanche Energy	2900	mJ
dv/dt (2)	Peak Diode Recovery voltage slope	5	V/ns
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Operating Junction Temperature	-55 to 175	°C

(•) Pulse width limited by safe operating area.

(1) Starting T_j = 25 °C, ID = 70A, VDD= 50V
(2) I_{SD} ≤140A, di/dt ≤200A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$

Appendix H: Driver Spec Sheet

National Semiconductor

February 2005

LM5104
High Voltage Half-Bridge Gate Driver with Adaptive Delay

General Description

The LM5104 High Voltage Gate Driver is designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck configuration. The floating high-side driver is capable of working with supply voltages up to 100V. The high side and low side gate drivers are controlled from a single input. Each change in state is controlled in an adaptive manner to prevent shoot-through issues. In addition to the adaptive transition timing, an additional delay time can be added, proportional to an external setting resistor. An integrated high voltage diode is provided to charge high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails. This device is available in the standard SOIC-8 pin and the LLP-10 pin packages.

Features

- Drives both a high side and low side N-channel MOSFET
- Adaptive rising and falling edges with programmable additional delay
- Single input control
- Bootstrap supply voltage range up to 118V DC
- Fast turn-off propagation delay (25 ns typical)
- Drives 1000 pF loads with 15 ns rise and fall times
- Supply rail under-voltage lockout

Typical Applications

- Current Fed Push-Pull Power Converters
- High Voltage Buck Regulators
- Active Clamp Forward Power Converters
- Half and Full Bridge Converters

Package

- SOIC-8
- LLP-10 (4 mm x 4 mm)

Simplified Block Diagram

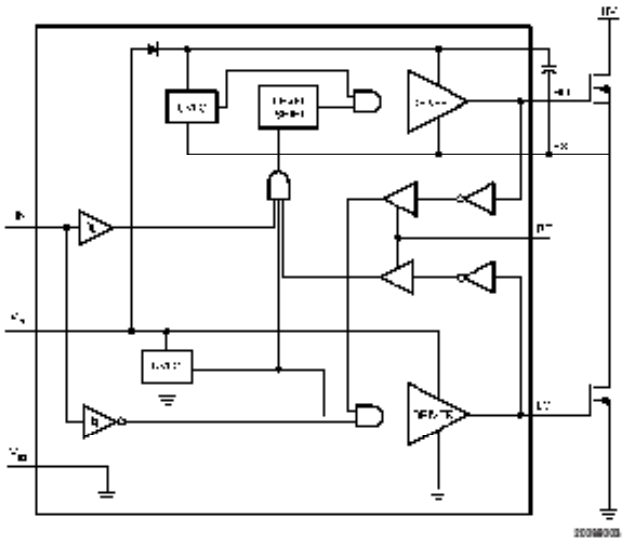


FIGURE 1.

 DS200690 www.national.com

LM5104 High Voltage Half-Bridge Gate Driver with Adaptive Delay

Appendix I: Filter Inductor Spec Sheet

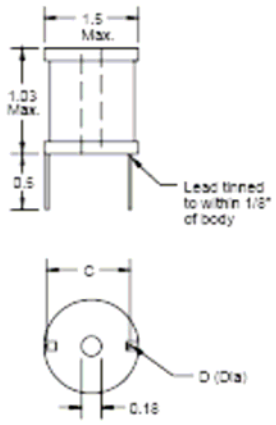
High Current Chokes

Special Features

- Very high current capacity
- Low DCR
- Epoxy coated ferrite bobbin core
- VW-1 rated shrink tubing to cover winding
- Self-leaded
- Fixed lead spacing
- Center hole for mechanical mounting
- Dielectric withstanding voltage:
  2500 Vrms terminal to shrink tube cover;
  1000 Vrms terminal to core
- Operating temperature -55 to +105 °C

Notes

* Rated current to cause 50 °C max. temperature rise and 5 % max. inductance drop



Dimensions: Inches

1140 Series					
Part Number	L (µH) ±20 % @ 1 MHz	DCR Ω Max.	I, dc* (A)	Dim. C Approx.	Dim. D Nom.
1140-1R8M-RC	1.8	0.002	27	1.11	0.081
1140-2R2M-RC	2.2	0.002	27	1.11	0.081
1140-2R7M-RC	2.7	0.003	27	1.11	0.081
1140-3R3M-RC	3.3	0.003	27	1.11	0.081
1140-3R9M-RC	3.9	0.003	27	1.11	0.081
1140-4R7M-RC	4.7	0.003	27	1.11	0.081
1140-5R6M-RC	5.6	0.004	27	1.11	0.081
1140-6R8M-RC	6.8	0.004	27	1.15	0.081
1140-8R2M-RC	8.2	0.004	27	1.15	0.081
	± 10 %				
1140-100K-RC	10	0.005	27	1.15	0.081
1140-120K-RC	12	0.005	27	1.15	0.081
1140-150K-RC	15	0.006	27	1.15	0.081
1140-180K-RC	18	0.008	27	1.15	0.081
1140-220K-RC	22	0.009	21	1.15	0.081
1140-270K-RC	27	0.010	21	1.15	0.081
1140-330K-RC	33	0.011	21	1.15	0.072
1140-390K-RC	39	0.012	21	1.15	0.072
1140-470K-RC	47	0.018	14.4	1.15	0.072
1140-560K-RC	56	0.019	14.4	1.15	0.064
1140-680K-RC	68	0.021	14.4	1.15	0.064
1140-820K-RC	82	0.023	14.4	1.15	0.064
1140-101K-RC	100	0.025	14.4	1.15	0.064
1140-121K-RC	120	0.028	14.4	1.15	0.057
1140-151K-RC	150	0.040	11.4	1.15	0.057
1140-181K-RC	180	0.045	11.4	1.15	0.057
1140-221K-RC	220	0.050	11.4	1.15	0.051
1140-271K-RC	270	0.056	11.4	1.15	0.051
1140-331K-RC	330	0.074	11.4	1.15	0.051
1140-391K-RC	390	0.082	9	1.15	0.045
1140-471K-RC	470	0.114	7.2	1.15	0.045
1140-561K-RC	560	0.125	7.2	1.15	0.040
1140-681K-RC	680	0.139	7.2	1.15	0.040
1140-821K-RC	820	0.154	7.2	1.15	0.040
1140-102K-RC	1000	0.216	5.5	1.15	0.040
1140-122K-RC	1200	0.232	5.5	1.14	0.036
1140-152K-RC	1500	0.324	4.5	1.14	0.036
1140-182K-RC	1800	0.360	4.5	1.14	0.036
1140-222K-RC	2200	0.404	4	1.10	0.032
1140-272K-RC	2700	0.555	4	1.12	0.032
1140-332K-RC	3300	0.773	2.8	1.10	0.029
1140-392K-RC	3900	0.845	2.8	1.10	0.029
1140-472K-RC	4700	1.14	2	1.12	0.029
1140-562K-RC	5600	1.60	2	1.09	0.025
1140-682K-RC	6800	1.76	1.6	1.12	0.025
1140-822K-RC	8200	1.95	1.6	1.09	0.023
1140-103K-RC	10,000	2.76	1.3	1.11	0.023
1140-123K-RC	12,000	3.04	1.3	1.08	0.020
1140-153K-RC	15,000	3.39	1.3	1.10	0.020

Available only as RoHS compliant beginning July 2007.
When ordering non-RoHS compliant versions before July 2007, do not include the -RC suffix in the part number.

BOURNS®

Tel. (877) 426-8767 • Fax (951) 781-5006
www.bourns.com

22.4

REV. 02/07

Appendix J: Flip-Flop Spec Sheet

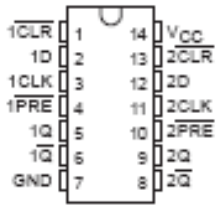
SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

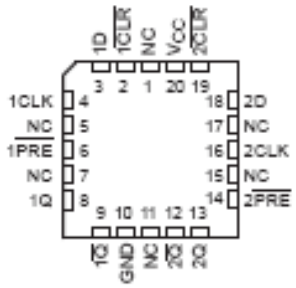
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (C_L = 60 pF) (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS74A	50	6
'AS74A	134	25

SN54ALS74A, SN54AS74A . . . J PACKAGE
SN74ALS74A, SN74AS74A . . . D OR N PACKAGE
(TOP VIEW)



SN64ALS74A, SN64AS74A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent positive-edge-triggered D-type flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54ALS74A and SN54AS74A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS74A and SN74AS74A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

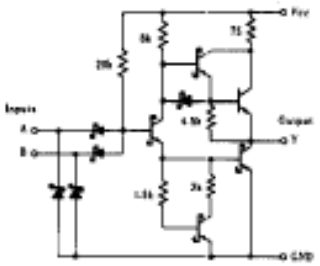
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration are not specified to meet the minimum levels for V_{OH} if the lows at $\overline{PRE}$ and $\overline{CLR}$ are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

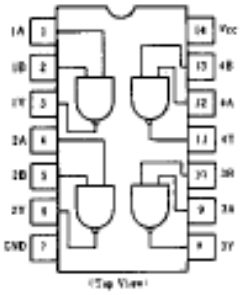
Appendix K: NAND Gate Spec Sheet

HD74LS00 ●Quadruple 2-input Positive NAND Gates

■CIRCUIT SCHEMATIC(¼)



■PIN ARRANGEMENT



■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75℃$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	–	–	V
	V_{IL}			–	–	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=8mA$	–	–	0.5	V
			$I_{OL}=4mA$	–	–	0.4	
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current	I_{CCH}	$V_{CC}=5.25V$		–	0.8	1.6	mA
	I_{CCL}	$V_{CC}=5.25V$		–	2.4	4.4	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* $V_{CC}=5V$, $Ta=25°C$

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25℃$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$	–	9	15	ns
	t_{PHL}		–	10	15	ns

Note) Refer to Test Circuit and Waveform of the Common Item

Appendix L: Rectifier Diode Spec Sheet

STTH5L06

TURBO 2 ULTRAFAST HIGH VOLTAGE RECTIFIER

MAIN PRODUCT CHARACTERISTICS

$I_{F(AV)}$	5 A
V_{RRM}	600 V
I_R (max)	150 µA
Tj (max)	175 °C
V_F (max)	1.05 V
trr (max)	95 ns

DO-201AD
STTH5L06

FEATURES AND BENEFITS

- Ultrafast switching
- Low reverse recovery current
- Reduces switching & conduction losses
- Low thermal resistance

DESCRIPTION

The STTH5L06, which is using ST Turbo 2 600V technology, is specially suited as boost diode in discontinuous or critical mode power factor corrections.
The device is also intended for use as a free wheeling diode in power supplies and other power switching applications.

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage		600	V
$I_{F(RMS)}$	RMS forward current		20	A
$I_{F(AV)}$	Average forward current	Tl = 50°C δ =0.5	5	A
I_{FSM}	Surge non repetitive forward current	tp = 10 ms Sinusoidal	110	A
T_{stg}	Storage temperature range		- 65 + 175	°C
Tj	Maximum operating junction temperature		+ 175	°C

November 2001 - Ed: 1A

Appendix M: Opamp Spec Sheet

TL082
TL082A - TL082B

GENERAL PURPOSE J-FET DUAL OPERATIONAL AMPLIFIERS

- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)

N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

P
TSSOP8
(Thin Shrink Small Outline Package)

ORDER CODE

Part Number	Temperature Range	Package		
		N	D	P
TL082M/AM/BM	-55°C, +125°C	•	•	•
TL082I/AI/BI	-40°C, +105°C	•	•	•
TL082C/AC/BC	0°C, +70°C	•	•	•
Example : TL082CD, TL082IN				

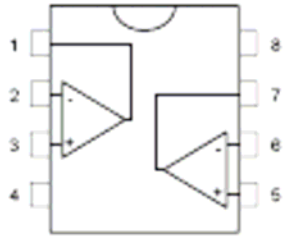
N = Dual In Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)
P = Thin Shrink Small Outline Package (TSSOP) - only available in Tape & Reel (PT)

DESCRIPTION

The TL082, TL082A and TL082B are high speed J-FET input dual operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

PIN CONNECTIONS (top view)



1 - Offset null 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

March 2002 1/11