PROJECT REL-MQP-7990

LDMOS POWER AMPLIFIER DESIGN

By

Mustafa Konca Steven J. Miller

Date: April 24, 2008

Major Qualifying Project Report submitted to the Faculty of

WORCESTER POLYTECHNIC INSTITUTE

in partial fulfillment of the requirements for the degree of
Bachelor of Science

1. LDMOS
2. POWER AMPLIFIER
3. RF

Approved:

Professor Reinhold Ludwig, Advisor

Abstract

The following report documents the Major Qualifying Project involving the design, implementation and testing of an RF power amplifier designed for an operating spectrum between 1930-1990MHz. The report reflects a design approach relying on computer simulations (using ADS software). The project then uses the results of these simulations toward the development of a physical circuit. The circuit is then refined for greater performance through testing and tuning. The main design focus of the project was the improvement of video bandwidth.

Acknowledgements

This project was made possible through the generous contributions of Korne Vennema and his colleagues at NXP Semiconductors. More specifically, the project team would like to thank Yong Yang for his guidance in system modeling and simulation in ADS. The project team would also like to thank Timothy Wood for his efforts in ordering the final layout, sourcing components, obtaining part information and helping in the construction of the amplifier. Special thanks go to Korne Vennema for his support and guidance throughout the project, which consisted of not only providing important device documentation and performance data, but also access to sophisticated laboratory equipment and his valuable insights regarding RF circuit design and engineering in general.

Table of Contents

Table of Figures

1-Introduction

For over 20 years, there has been an increasing demand for personal wireless communications. This has spurred competition among various providers for greater signal range, increased signal clarity and multimedia access. Therefore there is a constant drive within the wireless communications industry to use the most advanced, yet cost-effective technology available. Several firms have risen to serve this need, among them is NXP Semiconductors.

NXP Semiconductors, formerly a division of Philips Electronics, designs and sells a wide range of products, including RF power transistors typically used in base stations. As part of their product development, NXP has introduced their sixth-generation Laterally-Diffused Metal-Oxide Semiconductor (LDMOS) transistor. This transistor design has been used successfully in previous RF power amplifier designs, but for a 45dBm (32W) application it presents challenging design problems, particularly with respect to video bandwidth. It is therefore the goal of this project to analyze this new transistor and understand how it can be best implemented for RF power amplification. While the implementation will be designed to various specifications such as efficiency, gain and peak power, the main objective will be to maximize the device's video bandwidth.

This document describes the approach to this problem and its results. Relevant background topics that may not be well-understood by a general audience are discussed first. A formal problem statement with objectives is presented next. Following the project statement, the project's methodology will be discussed. The methodology will include steps that attempt to simulate solutions to the problem and reproduce them in a physical form. The results will lead to conclusions and recommendations for future steps.

2-Background Information

2.1-Code Division Multiple Access

As mentioned before, the use of mobile communications has enjoyed continued growth since its introduction as a technological novelty in the early 1980's. This growth was the motivating factor in the creation of not only unique cell phone designs, but also communication standards. In 1995, the Code Division Multiple Access (CDMA, also known as IS-95 or CDMAOne) standard was introduced by Qualcomm in order to address concerns of increased data within limited bandwidths.

CDMA uses a different kind of signal processing known as spread-spectrum modulation. Instead of simply dividing a frequency spectrum amongst users, CDMA assigns each user a distinct pseudo-random code. This gives all users access to an entire frequency spectrum. To receive a signal, all a device must do is detect a required code throughout a frequency spectrum and piece the signal together. Through CDMA, every user has access to the entire spectrum. Therefore, many more users can be served by a given number of cell-sites and greater amounts of data can be transmitted within a given amount of bandwidth.

CDMA2000 (IS-2000) is a newer standard that is backwards-compatible with the original IS-95 CDMA and used by major service providers such as Sprint Nextel Corp. and Verizon Wireless. Given the popularity of this standard and the theory behind its operation, CDMA will be an important factor as the project progresses. The amplifier design produced by this project must maintain its functionality throughout the given frequency spectrum of 1930-1990MHz. Otherwise, it may damage the CDMA signals that pass through it, causing distortion and reducing signal clarity. Please note that CDMAOne and CDMA2000 are not to be confused with other standards such as W-CDMA that, while using similar techniques, are completely incompatible.

2.2-Multi-Carrier vs. Single-Carrier Configurations

RF power amplifiers can be implemented in either a single-carrier configuration (SCPA) or multi-carrier configuration (MCPA). Each implementation has its strengths and weaknesses in a given application. SCPA operates through a parallel arrangement of amplifiers. Each of these amplifiers is responsible for signals of one particular carrier. The outputs from each amplifier are combined to form one, multiple-carrier signal. MCPA uses the opposite approach. Rather than combining signals after amplification, MCPA combines signals before amplification so that only one amplifier is required to process the incoming signals. Therefore MCPA requires a more powerful amplifier with a broader range of operating frequencies than that of SCPA.

Now that MCPA and SCPA have been briefly described, comparisons can be drawn. SCPA configurations require separate amplifiers for each signal carrier. Installation of these multiple amplifiers will require more physical space compared to MCPA, especially if they are to be cooled properly. Multiple amplifiers will also increase the overall power consumption of the base station. MCPA, on the other hand, reduces the number of amplifiers required by taking in multiple carriers per individual amplifier. Given a required RF output power, this can reduce power consumption, therefore lowering operating temperature and increasing the power efficiency of the base station. Such characteristics explain the popularity of MCPA, especially in more urban areas where many carrier frequencies are used. However, with MCPA one must consider the side-effects of multi-carrier signal processing such as Inter-Modular Distortion (IMD), which will be discussed later in this section.

It should be noted that the amplifier design produced by this project will be designed for MCPA. Therefore as the project progresses great care will be taken to ensure that the design operates at a very wide range of frequencies so as to ensure proper operation given the multiple carriers it will receive.

2.3-Inter-Modular Distortion (IMD) Products

IMD products are produced whenever a multi-carrier signal is amplified through a non-linear system. It is very important to minimize IMD products, as they are the cause of extraneous frequencies found in a device's output signal. Also lower frequency second-order IMD products can interfere with the DC bias of the transistor, increasing the non-linearity of the transistor and decreasing efficiency. Third-order products can appear at frequencies that are very close to that of the signal carrier, making them very difficult, if not impossible, to filter out. These third-order IMD products will require the most attention and will be among this project's most pressing concerns. The best way to minimize IMD products is to use a stable transistor and operate it in its linear region. However in the case of this project, the transistor is being operated in the non-linear region below the linear range, also known as AB-class operation. AB-class designs sacrifice linearity in favor of efficiency.

In RF power amplifiers, IMD magnitudes can increase with carrier spacing and can pollute the output signal significantly as wider bandwidths are explored. Therefore, it is important to minimize IMD products as much as possible when designing amplifiers for wide bandwidths, such as the one being designed for this project. The extraneous frequencies that result from the amplification of a two-carrier signal through a non-linear system are illustrated in Figure 1 below:

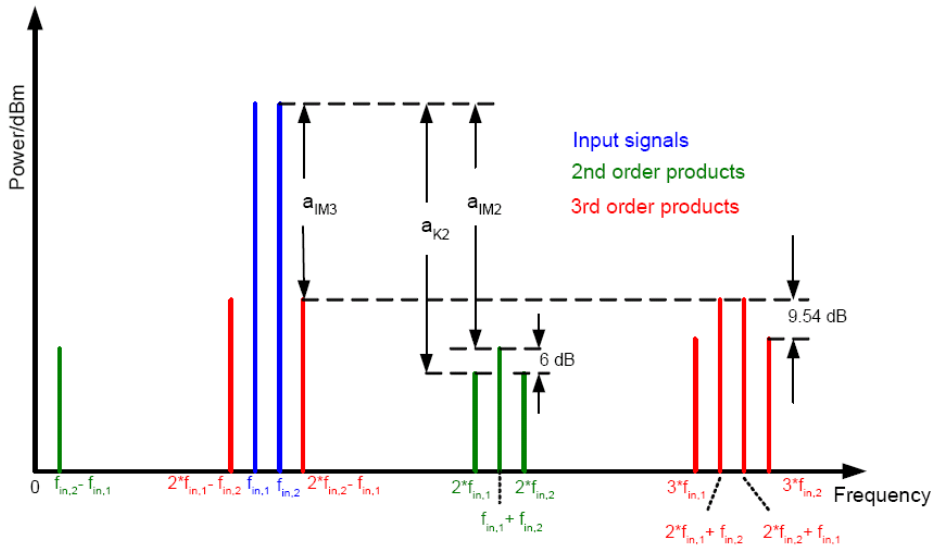


Figure 1: Inter-Modular Distortion (IMD) in the presence of a two-carrier input signal (courtesy of NXP)

3-Project Statement and Objectives

As the personal wireless communications industry progresses, there is an increasing demand for greater signal ranges, better signal clarity and faster access to multimedia content. RF power amplifier designs must be able to meet these challenges at reasonable cost if they are to be profitable. Therefore, given today's market demands and state-of-the-art amplifier design principles, the objective of this project is to analyze NXP's BLF6G20LS-140 LDMOS transistor and use it towards the design of a AB-class RF power amplifier. The design must meet several exacting specifications, but of particular interest will be to maximize video bandwidth.

Maximizing video bandwidth is best achieved by minimizing Third-order Inter-Modular Distortion (IMD3) products. A successful design will keep the magnitude of these products below -33dBc over a very wide carrier spacing. The IMD3 performance of the final design will be evaluated by providing a two-tone signal to the amplifier while it operates at an RF output power level of 45dBm (32W). The spacing between the two tones will be swept to a maximum of 100MHz. The maximum carrier spacing tolerated by the amplifier will be determined by the point at which IMD3 products exceed -33dBc (amplitude relative to that of the signal carrier). The final design must be able to operate in a MCPA configuration within a 60MHz spectrum between 1930-1990MHz.

To this end, the project will follow a logical design process that divides a complete amplifier topology into sections, or "design blocks". Individual design blocks will be studied and optimized given ideal conditions. The design blocks will then be assembled around NXP's power transistor model, forming a complete amplifier prototype that can be further analyzed and optimized for the above criteria. Analyses will rely on computer simulations using Agilent's Advanced Design System (ADS) and a transistor model provided by NXP Semiconductors. Once complete, the amplifier prototype will be evaluated in terms of its strengths and weaknesses in amplifying two-carrier CDMA signals of varying carrier spacing. The complete amplifier will include components such as the active-bias network and impedance matching networks. A table containing the objective specifications of the amplifier has been included in Appendix A.

4-Computer Simulations

The methodology of this project can be split into two distinct categories; theoretical computer simulation and practical circuit performance testing. The theoretical portion utilized Agilent's Advanced Design System (ADS) and will be discussed first. ADS was used to simulate the circuit in distinct parts. Computer simulation began with the characterization of a transistor model provided by ADS, then progressed to the analysis of NXP's active bias network. S-parameter tests then allowed for the simulation and development of input and output matching networks. By the time this phase of the project was complete, the entire system was simulated and analyzed.

4.1-Transistor Characterization

4.1.1-DC Analysis

An LDMOS transistor functions much the same way as any other MOSFET device in that it requires voltage at its gate terminal to effect a current though its channel. The objective statement defined earlier specified a quiescent drain current (I_{DQ}) of 1200mA. With this in mind, a DC analysis was required as a first step in characterizing the transistor assigned to this project. The purpose of the DC analysis was to sweep the bias voltage at the transistor's gate in order to identify its linear and nonlinear regions. The results of this analysis provided a better understanding of the bias voltage requirements of the transistor and how it operated at an I_{DQ} of 1200mA.

DC analysis of NXP's transistor model was performed in ADS. This was among the simplest computer simulations to perform as it required only the transistor model, two voltage sources and a current probe. One voltage source was applied at the transistor's drain to represent the 28V that will be supplied in the complete design. The complete setup and the results of the voltage sweep can be seen on the next page.

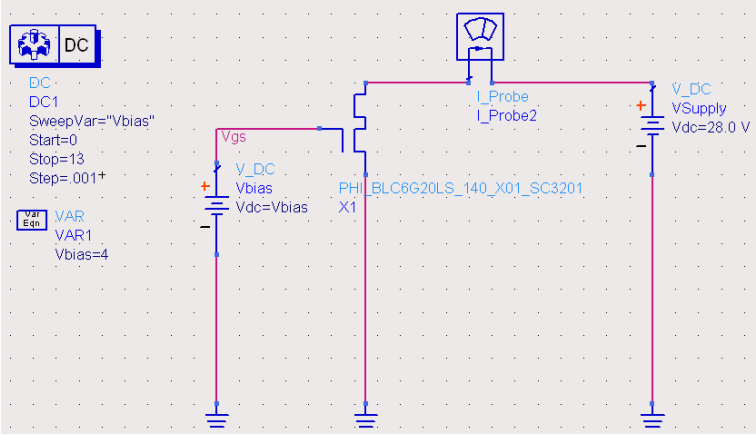


Figure 2: Test setup for the DC Analysis of NXP's transistor model

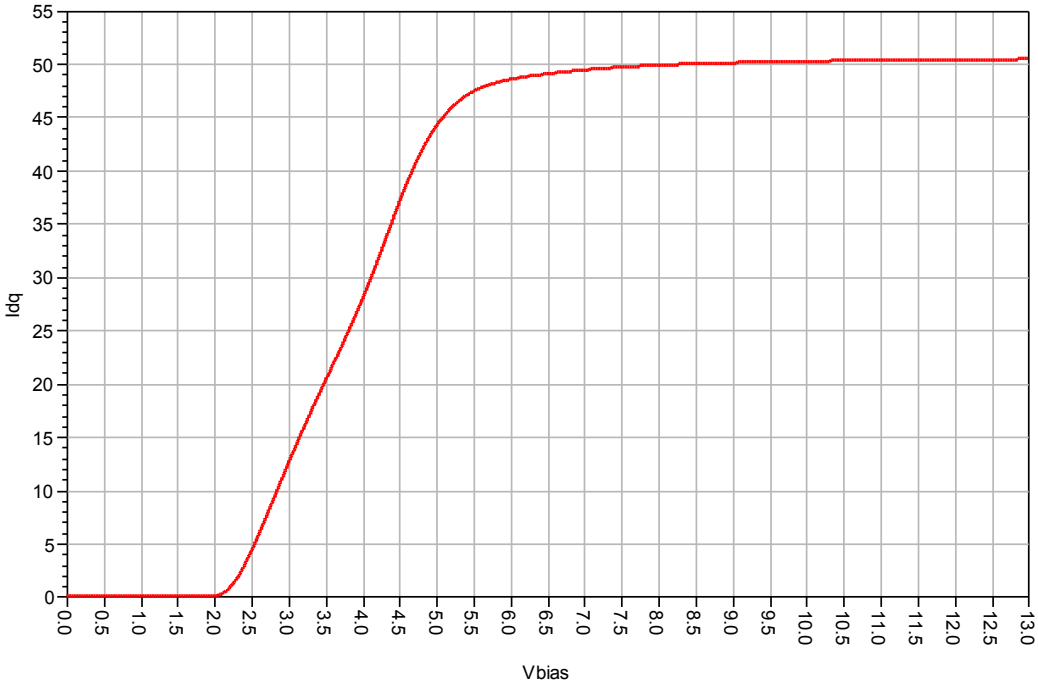


Figure 3: Transistor model's quiescent current (I_{DQ}) as a function bias voltage

The graph above clearly illustrates the transistor's linear and nonlinear regions as described by NXP's transistor model. The horizontal axis indicates the swept values of voltage at the transistor's gate. This voltage is commonly referred to as gate-to-source voltage or V_{GS}. The vertical axis indicates the drain current experienced by the transistor as V_{GS} is swept. It can be seen that NXP's model predicts a rapidly increasing drain current as V_{GS} exceeds 2V with saturation occurring at around 5.5V. It is highly doubtful that actual transistors will see such a high voltage in practice, as NXP specifies that the drain current should not exceed 39A. It is also very doubtful that these transistors will be run in the linear region, as they become very inefficient when operated linearly.

Even in AB-class operation these transistors would be considered to operate very well at 30% drain efficiency! Therefore, for more meaningful results attention must be directed toward the nonlinear region where V_{GS} is swept between 2-3V.

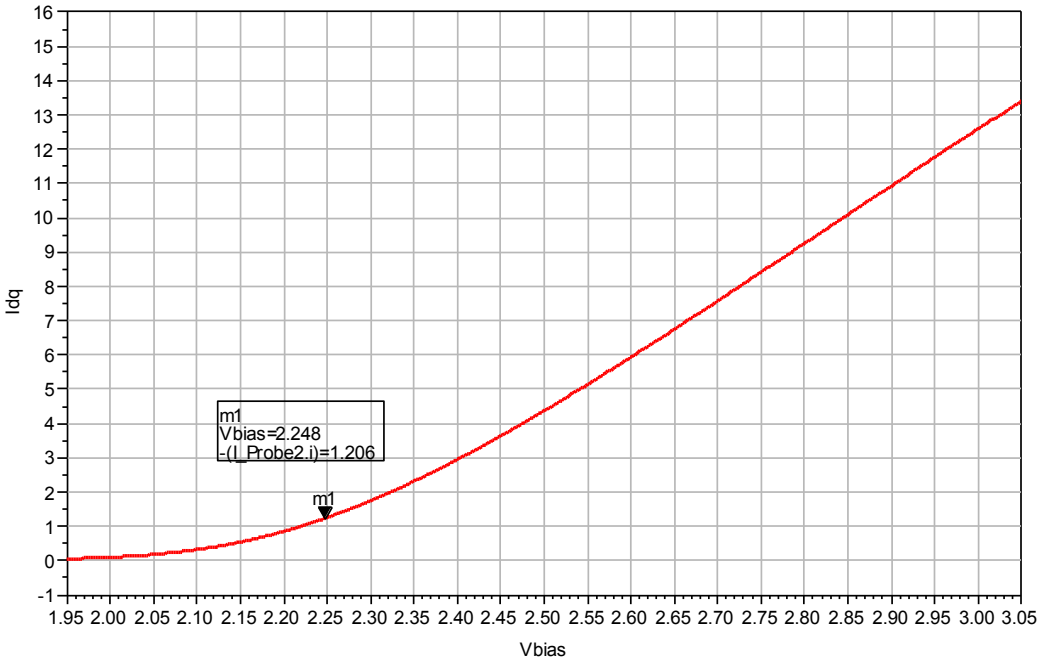


Figure 4: 2.247V must be applied at the transistor's gate to reach the required I_{DQ}

In the above graph the required V_{GS} can be clearly seen. For an I_{DQ} equal to 1200mA, NXP's transistor model requires a V_{GS} roughly equal to 2.247V. Such an operating point will allow for AB-class operation of the transistor, the best compromise between device linearity and efficiency. This simulation data was later verified by NXP.

4.1.2-Large Signal S-Parameters (LSSP)

Large signal s-parameter tests are used to obtain the s-parameters of nonlinear systems. LSSP test requires the use of a power source, because nonlinear systems may have different s-parameters at different power levels. For this test, a power level of 28dBm (631mW) was used to measure the s-parameters of the transistor at 1960MHz. The transistor was also biased to the desired operating point as defined in the previous section. The test setup can be seen in Figure 5.

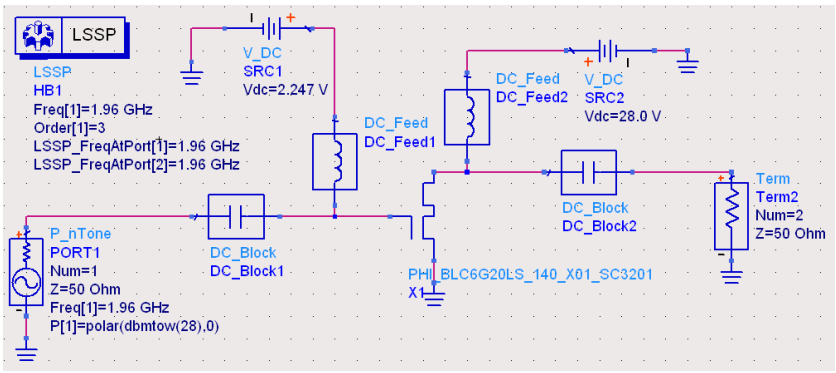


Figure 5: Test setup for large-signal s-parameter tests of NXP's transistor model

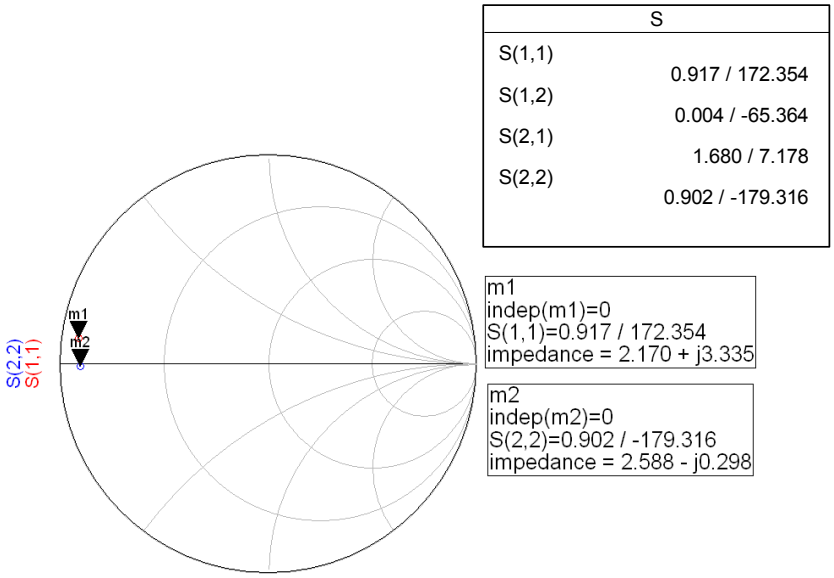


Figure 6: Results of large-signal s-parameter tests

It was not possible to directly compare the results obtained from these tests to the real transistor, because no s-parameter data had been recorded for the physical transistor. The closest data that could be used for comparison were the results from the loadpull test performed with the physical transistor. The loadpull test does not provide s-parameters for the transistor. However, the optimum load conditions determined by the loadpull test should be very close to the "complex conjugate of the s-parameters of the transistor" for good matching. The resulting values of the LSSP test were relatively close to the values obtained from NXP's loadpull report, which indicated that the LSSP test results were a good estimation of the transistor's s-parameters. However it was concluded that the model provided was not accurate enough to be the sole basis for a physical design.

4.1.3-Loadpull Test

Loadpull simulations were another important step to understanding the transistor model. These simulations show the performance of the transistor under different load conditions using harmonic balance analysis. Both single tone and dual tone tests were performed. The loadpull test templates in ADS were used to perform these tests, because it would have been too complex of a task to write all the equations required to display the contour graphs. The results were relatively accurate for such a complex transistor model. However this data was not used as a basis for the physical implementation due to imperfections of the transistor model.

4.1.3.1-Single Tone Load-Pull Test

Single-tone tests were used to find power added efficiency (PAE) and power delivered to the load (PDL) for a range of load impedances. For this test, the center frequency (1.96GHz) was chosen at the source and the input power was set to 28dBm (631mW). The bias voltage was set to 2.247V for 1200mA of I_{DQ} and the source voltage was chosen to be 28V. The test setup for this simulation can be seen in Figure 7.

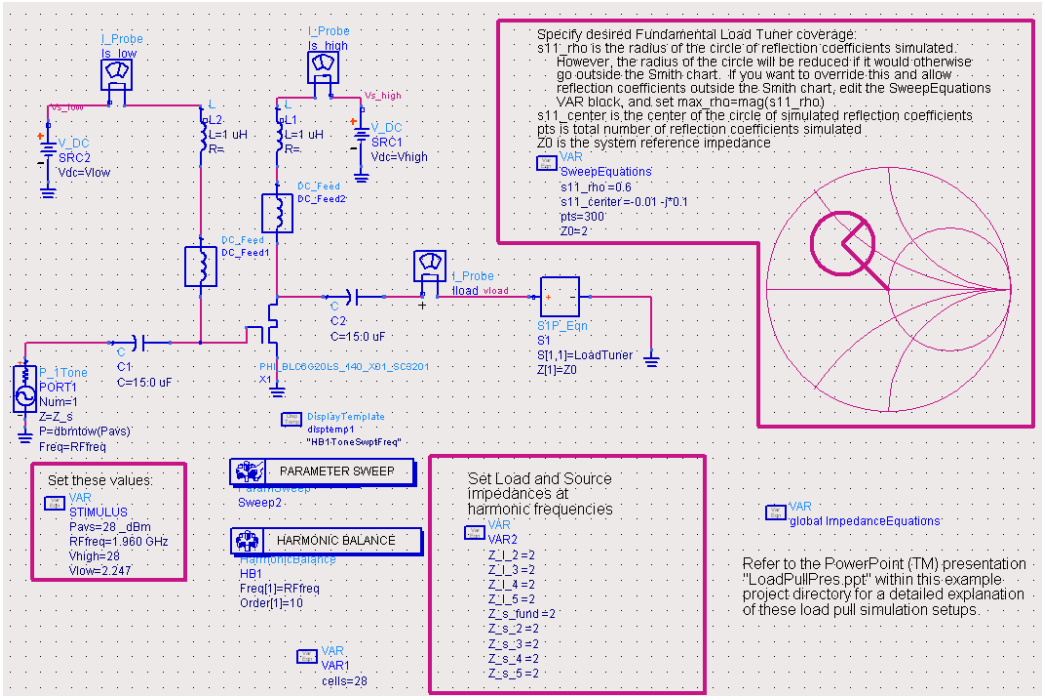


Figure 7: Single tone loadpull test setup

Figure 8 and Figure 9 show the PAE and power delivered to the load (PDL) as contour lines. Every contour line represents a level of PAE or PDL. Therefore similar values of PAE and PDL can be attained with many different impedance values, as long as the impedances occur along a single contour. By this logic it is easy to see that the highest values of PDL and PAE are represented by their innermost contours. The step size between the contours and the number of contour lines to be displayed can be set by changing the variables in the box next to the graph. In this test, the maximum PAE was found to be 37.99% and the maximum PDL was 45.37dBm (34W).

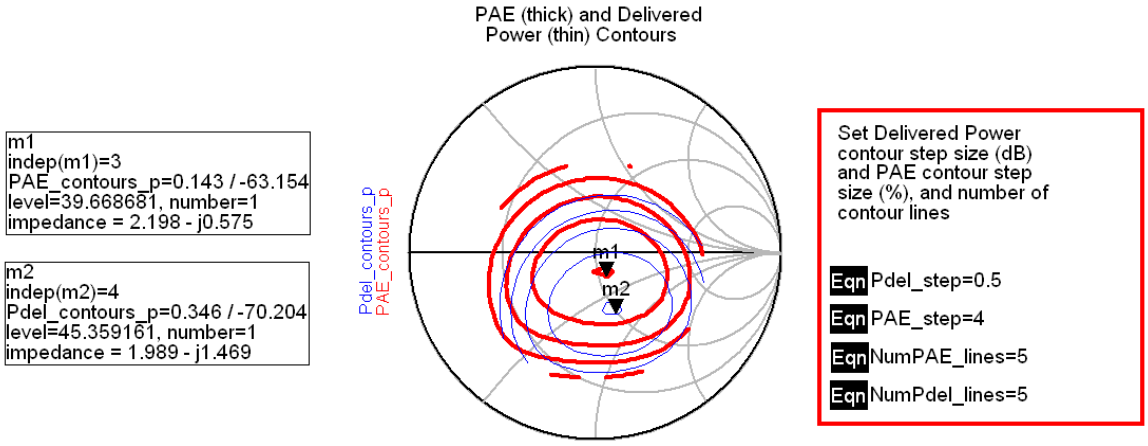


Figure 8: PAE and PDL contours on a smith chart normalized to 2Ω (single tone)

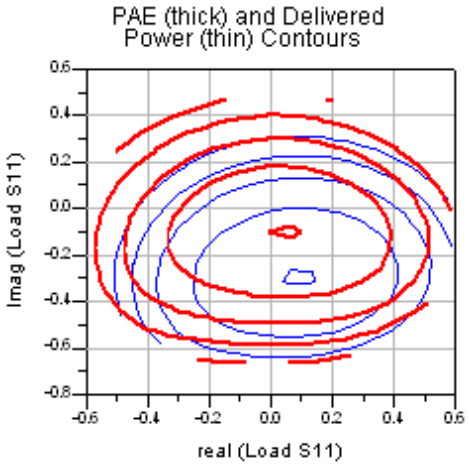


Figure 9: PAE and PDL contours on a linear plot (single tone)

In the physical test, maximum PAE was achieved at 1.55-j1.77Ω and the maximum PDL was achieved at 1.17-j1.78Ω, versus 2.2-j0.6Ω and 2-j1.5Ω obtained in ADS simulations. These results are fairly close to each other, especially when the different I_{DQ} used is taken into account. In the physical test an I_{DQ} of 1000mA was used while 1200mA was used for the ADS simulations, since

this was the planned quiescent current. Although the simulation results were close to the real world values, they were not accurate enough to be the basis for a physical design.

The smith chart and displays in Figure 10 work as an interactive tool. Every cross on the smith chart is a different impedance point that was used in the loadpull analysis. With this tool it is possible to see the PAE and PDL at a specific load impedance value by moving the marker (m3) from one impedance value to another.

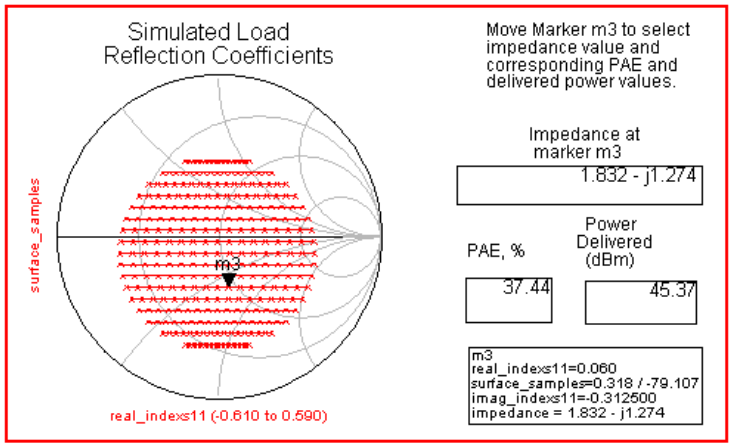


Figure 10: Set of simulated load impedances (single tone)

4.1.3.1-Dual Tone Load-Pull Test

As implied by its name, two carriers are used in this type of a simulation. Dual tone tests can be used to obtain the full output spectrum, power figures and essential IMD figures. The setup for this test was very similar to the single tone test's setup except that a dual tone source was used and different equations were required to do the contour calculations. Tests were performed at 20MHz and 60MHz carrier spacings to observe the effect of carrier spacing on the performance of the transistor.

Although some of the measurements were shown in the single tone test, these results are shown again to demonstrate the nonlinear nature of the transistor. As seen in Figure 11, there is a noticeable change in the PAE and PDL contours, even though the input power and all the bias conditions were kept the same. Only the test results for a 20MHz spacing were shown for the PAE and PDL, because the 60MHz test results were very similar. In this test, the maximum PAE was found to be 37.04% and the maximum PDL was 44.97dBm (31W).

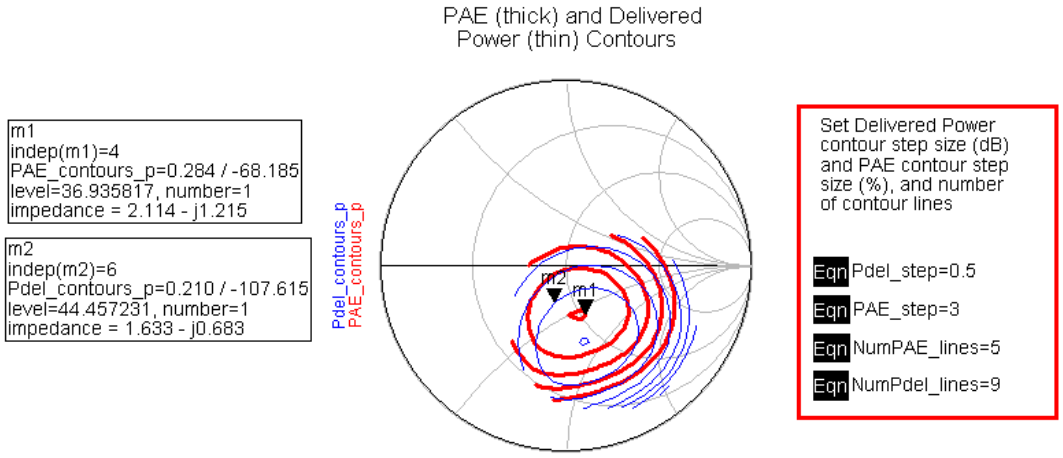


Figure 11: PAE and PDL contours on a smith chart normalized to 2Ω (dual tone)

The most crucial part of the dual tone test was the IMD figures. The results for IMD figures are shown in Figure 12 and Figure 13. IMD figures varied noticeably when the carrier spacing was increased. It was observed that the performance was not necessarily worse at higher frequency spacings; it was just different. For example, at a load impedance value of 0.55-j3.16Ω, IMD3 level was -33.88dBc at 20MHz spacing while it was -34.28dBc at 60MHz spacing. This kind of a result was unexpected. No explanation was found for this behavior, other than the imperfections of the transistor model.

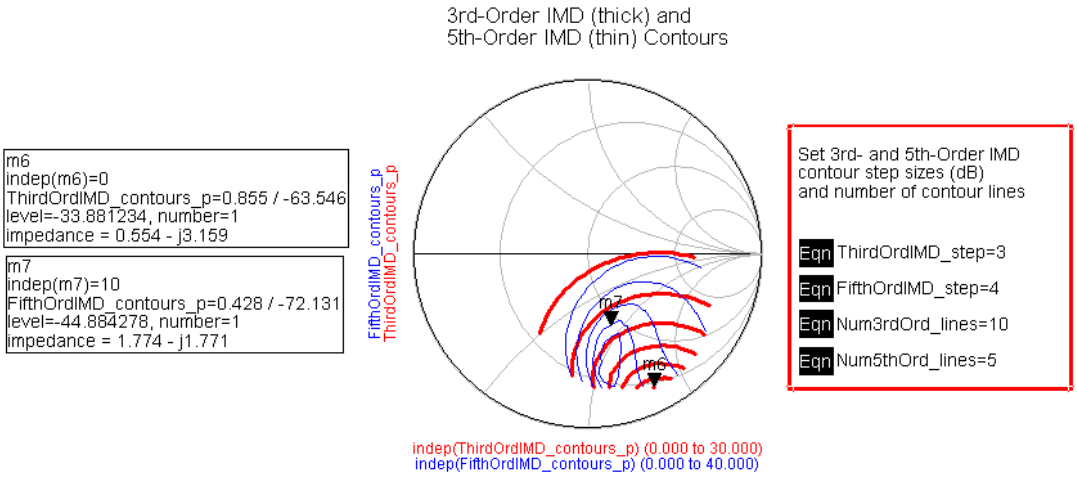


Figure 12: IMD performance 20MHz spacing

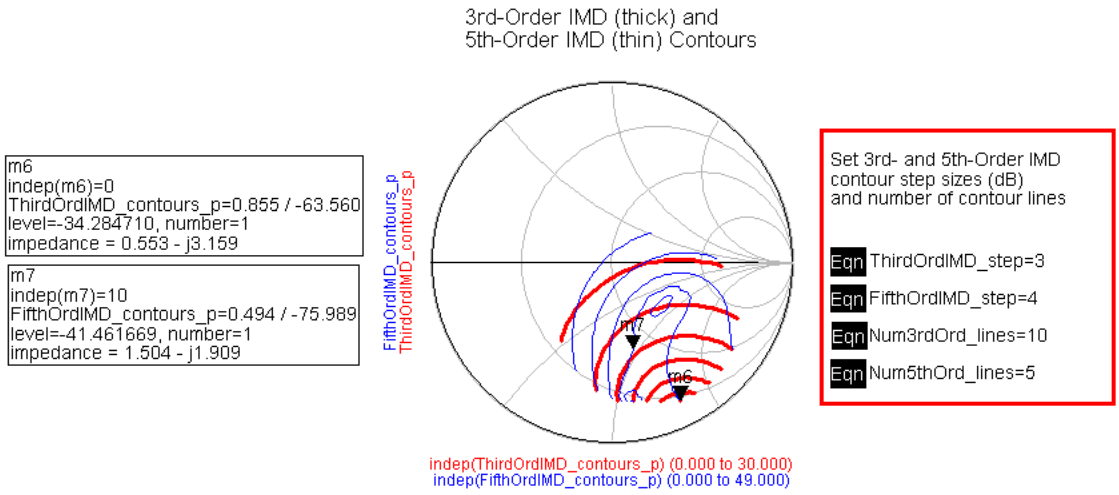


Figure 13: IMD performance at 60MHz spacing

The smith chart and displays in Figure 14 are similar to the ones explained before in Figure 10. However using the two tone test, it was also possible to see the full spectrum of the signal as well as the PAE, PDL, IMD3 and IMD5 figures. The changes in these values and the spectrum graph can be observed as another load impedance value is chosen.

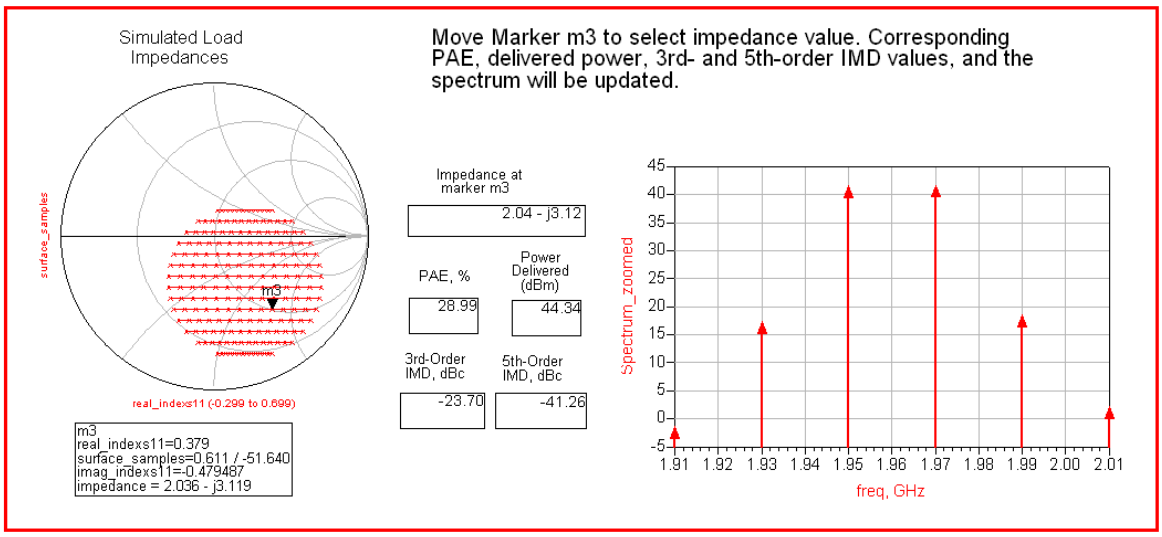


Figure 14: Simulated impedances (dual tone)

The loadpull test was useful for understanding the characteristic changes associated by using different load impedance values. For example, results clearly indicated that different impedance values are required for achieving best efficiency and peak power. Therefore it is impossible to get the best possible efficiency and peak power from any single design; there has to be a tradeoff between these figures.

4.2-Input Networks

4.2.1-Active Bias Network

If the transistor is to perform efficiently and consistently, it must be able to maintain its operating point throughout a variety of operating conditions. Therefore NXP has included with its transistor an active bias network designed to maintain a constant output voltage by compensating for fluctuations in input power and operating temperature. Input power quality is ensured by a 78L08 voltage regulator and temperature compensation is achieved with the use of a 2N2222 Bi-polar Junction Transistor (BJT) that is external from the LDMOS transistor but placed as close as possible to it. The voltage generated by this network can be tuned via a 200Ω potentiometer. The active bias network also features decoupling capacitors to minimize the RF interference from the adjacent input matching network. The active bias network was reproduced from NXP layout schematics for use in ADS and can be seen in Figure 15.

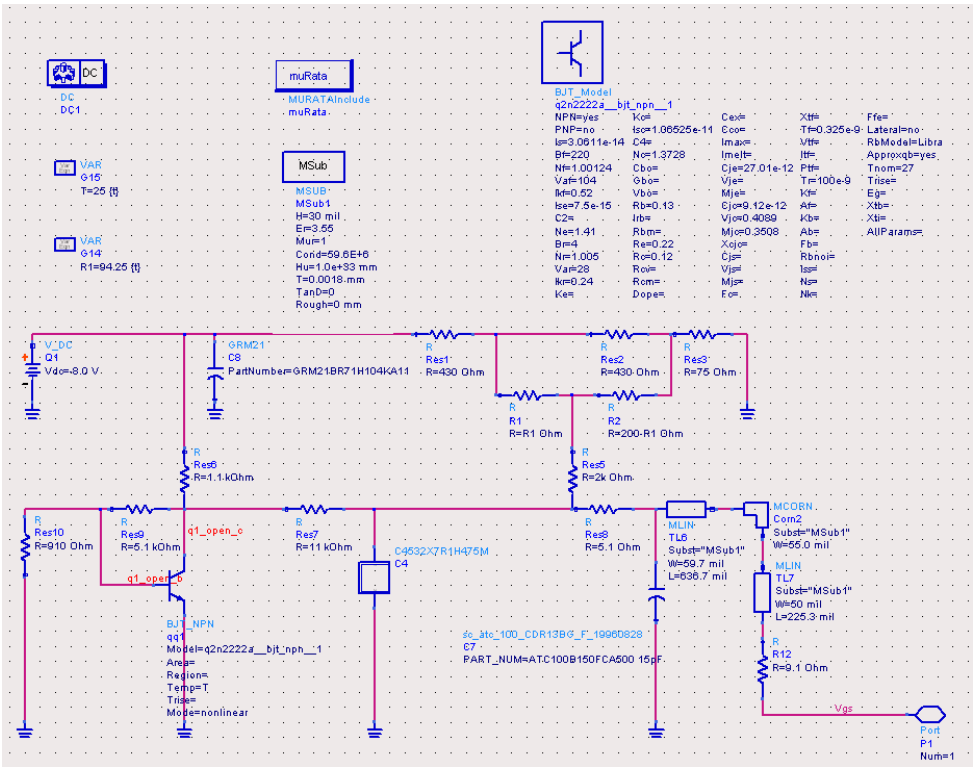


Figure 15: ADS schematic of NXP's active bias network

The active bias network was modeled to be as accurate as possible. This meant using circuit models of actual components rather than using simple lumped element models. The resistors and

voltage regulator were excluded from this practice. A simple 8V source was used to represent the output of the voltage regulator, a SPICE model was used to represent the BJT and two variable resistors were used to model the potentiometer. The schematic also features microstrip lines to facilitate the simulation of RF effects in later analyses.

Once the schematic was completed and verified to match NXP's layout, another DC analysis was conducted. This time, the DC analysis was to study the circuit's behavior and verify that the schematic can supply the required 2.247V to the transistor's gate. This was achieved by sweeping the potentiometer and reading the circuit's output voltage (labeled as V_{GS}, as it represents the voltage applied to the transistor's gate). Since NXP's LDMOS model does not account for changes in temperature, thermal effects could not be studied. Therefore, operating temperature was kept to a constant 25°C, the same temperature specified in NXP's physical tests. The results of the analysis can be seen below:

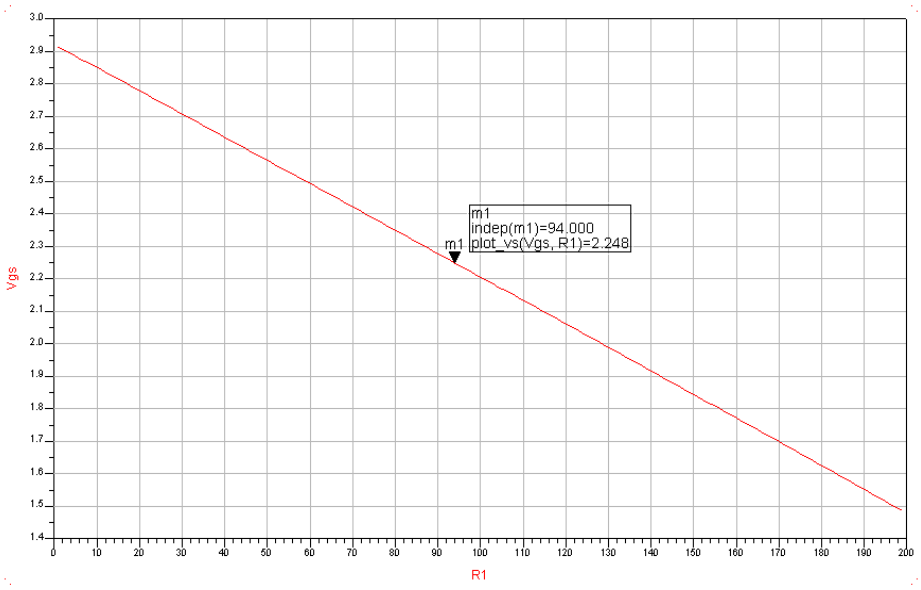


Figure 16: Gate voltage as a function of potentiometer resistance

As mentioned before, the potentiometer was modeled as two variable resistors (one resistor of variable value R1 and the other of value 200Ω minus R1). The above graph indicates that with this 200Ω potentiometer, gate voltages between 1.5-2.9V can be achieved. This allows for quiescent drain currents between 3.5μA-10.9A. For the specifications of the project (I_{DQ} = 1200mA and V_{GS} = 2.247V), this DC analysis indicates that the potentiometer should be somewhere in the middle of its range, with R1 roughly equal to 94Ω and R2 roughly equal to 106Ω.

4.2.2-Input Matching Network

S-parameter simulations were used extensively for designing the matching networks. The networks were designed to match the impedance values obtained from NXP's loadpull test results. Although this process did not result in a significantly improved input matching network, it was extremely helpful in terms of gaining experience in using ADS.

The first matching network design consisted of quarter-wavelength (commonly known as λ/4 length) sections with different widths thereby creating different characteristic impedances. The impedance matching provided by this design is illustrated in the smith chart in Figure 17. The source is a 50Ω impedance, which appears in the center. The input impedance of the transistor is featured toward the leftmost region of the smith chart. It was soon realized that, despite the design's good quality factor and elimination of capacitors, it would be impractical for use in the project. This design is impractical because every strip line is about λ/4 long, creating a network with a total length that exceeds NXP's standard board dimensions.

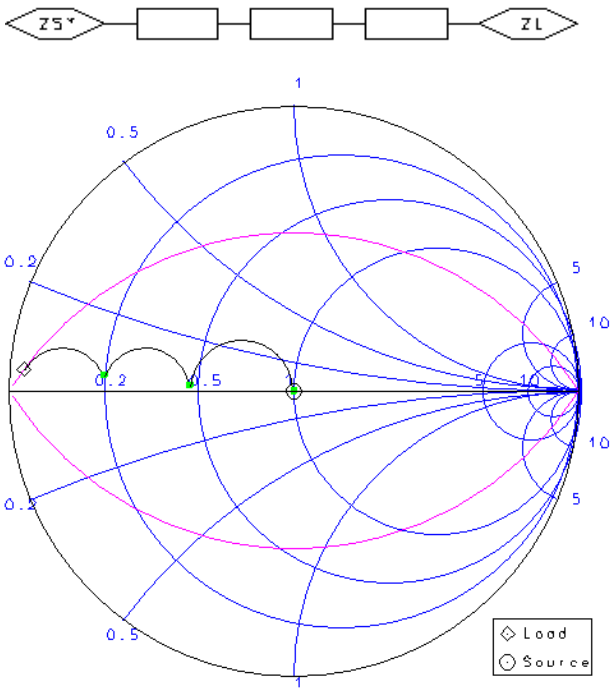


Figure 17: λ/4 design schematic and impedance matching

Other designs were made that were derived from those of NXP. One of the designs explored featured no capacitors, yet was compact enough to fit on the board. However, this design made use of really wide strips which can increase the presence of circulation currents and reflections in the line, making it impractical for physical implementation. It was later found that capacitors would be helpful for tuning the circuit's Input Return Loss (IRL) and gain flatness with much less power loss than what was previously expected. With this in mind, the next design made use of several small capacitors. A part of the bias network was also included for better accuracy. A termination load of 1.3+j3.09Ω (from NXP's loadpull report) was used to imitate the input impedance of the transistor that must be matched. The schematic for this new design can be seen in Figure 18:

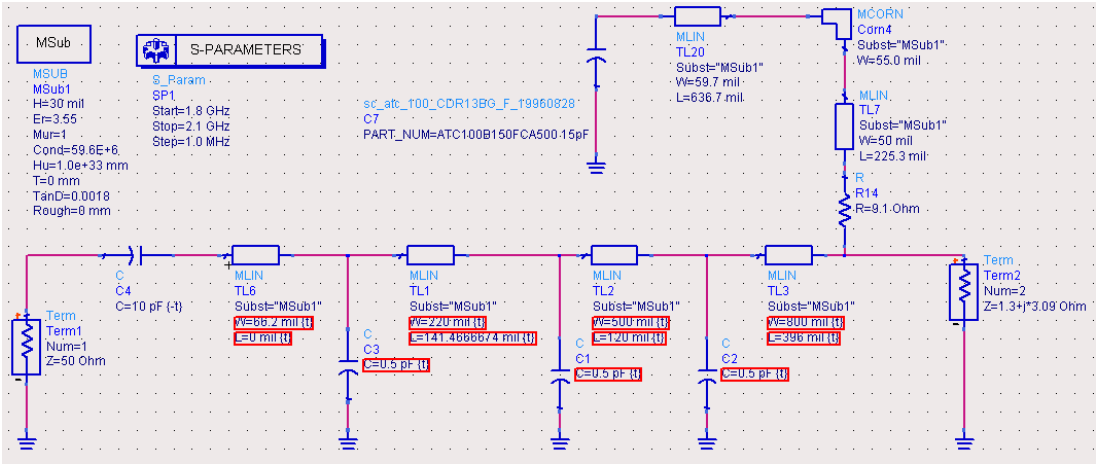


Figure 18: Input matching network design using capacitors

The red squares around the component values indicate that they are being used in the tuning process. The components called MLIN are micro-strip lines with defined length, width and substrate properties. The substrate properties (indicated as MSUB) resemble the properties of the RF-35 substrate used by NXP such as height, loss tangent and relative dielectric constant. Using MLIN instead of ideal micro-strip lines results in more accurate and realistic results. Next to MSUB there is a simulation controller for s-parameter tests. The controllers are used to tell ADS which simulation to run and which parameters to use. Parameters, such as the range of frequencies, can be swept via the simulation controller.

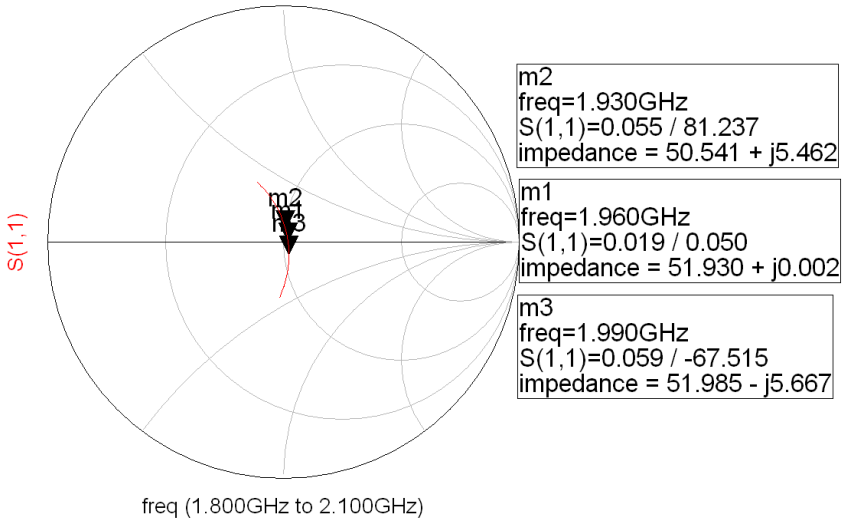


Figure 19: S11 performance of the design shown in Figure 18

This design did not aim for a perfect match at the center frequency, because it was found that perfect matching at the center frequency could be sacrificed in exchange for better matching over the whole band. This tradeoff was expected to result in improved gain flatness. The tuning capability in ADS allowed for a relatively short development time and better understanding of the finer details of matching network design, such as modifying components and the trends associated with these modifications. Knowing these trends would prove helpful in the physical testing stages of the project. The tuning window used for the design in Figure 18 can be seen in Figure 20.

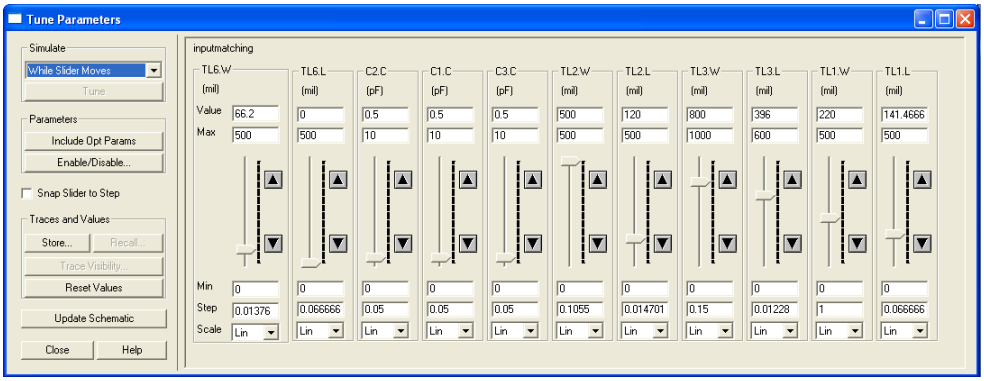


Figure 20: ADS Tune Parameters window

In Figure 20, TL stands for transmission line followed by its number which is followed by a ".W" or ".L" which indicate microstrip width and length respectively. For example, using the slider labeled "TL1.L", one would be able to change the length of the component called "TL1" and see the simulation results change almost instantaneously in the data window. There are also options for storing component values at different tuning stages and updating the schematic with the current values.

Input return loss was another important design criteria explicitly stated within the project's design requirements. IRL is equal to the magnitude of S11 in decibels. Since S11 was the criteria used to design the input matching network, results were expected to be satisfactory. These results can be seen in Figure 22. The markers were set at 1930, 1960 and 1990MHz to verify network performance across the network's intended operating spectrum. It is clearly seen that IRL is well below -10dB, which is within specification.

$$IRL = 10 * \log(|S11|)$$

Figure 21: Input Return Loss as a function of S11

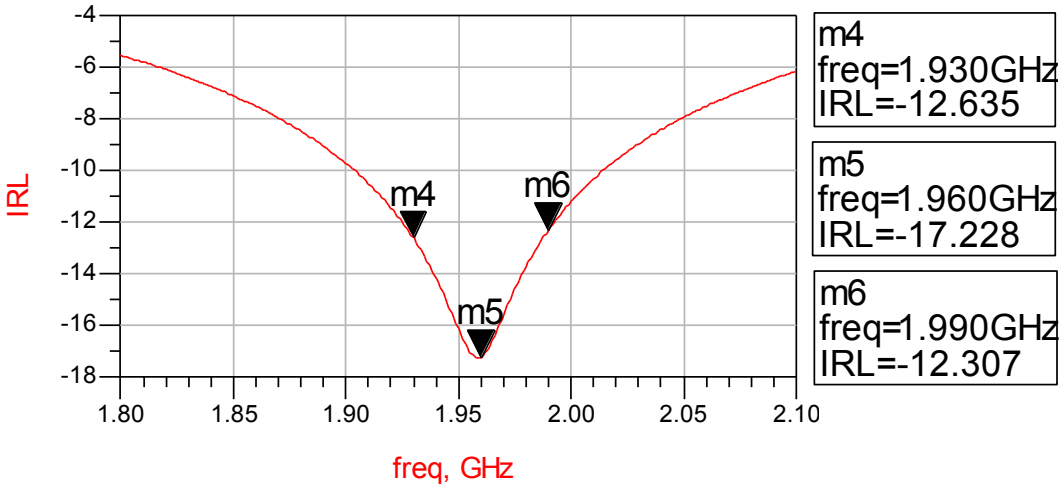


Figure 22: IRL performance of the design in Figure 18

Now that design opportunities had been explored, it was time to give NXP's design a similar analysis. The exact dimensions of NXP's input matching network were recorded from an AutoCAD file so that they could be constructed in ADS and compared to the above design. A schematic of NXP's design in ADS can be seen in Figure 23. In this design, microstrip components called

MSTEP were used. These components accounted for step discontinuities between two microstrips of different widths. The results obtained from this circuit seemed to be somewhat worse than what was observed in the designs previously discussed. However, considering the inherent inaccuracy of computer simulation it was still a good match.

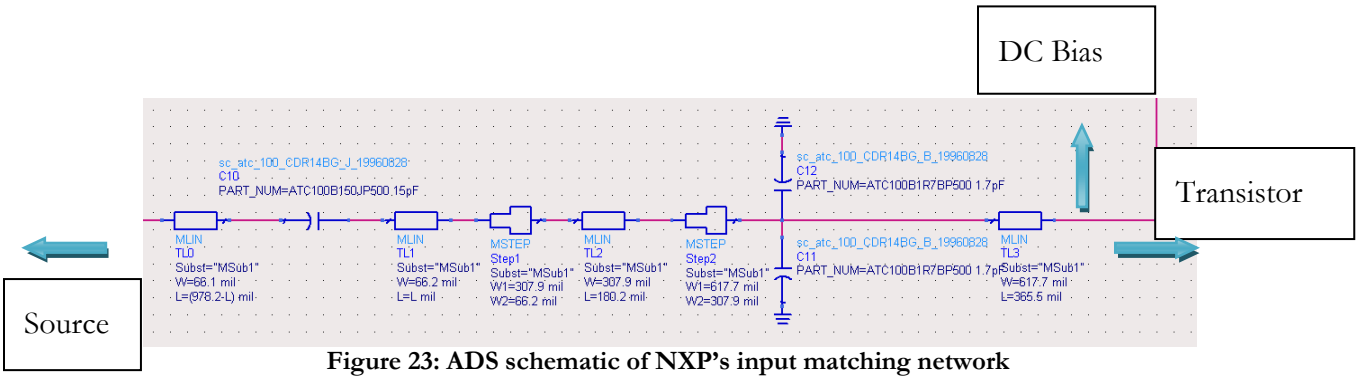


Figure 23: ADS schematic of NXP's input matching network

It was concluded that it would be best to keep the existing input matching network, since it was a physically tested design and sufficient for NXP's purposes. The final step, then, was to create a ADS Momentum model that would provide an even more accurate performance simulation. The Momentum model was required because MLIN and MCROS components used in the schematic were not very accurate when wide strips-lines were used. The Momentum simulation creates a mesh and uses electromagnetic field analysis to create a set of s-parameters for the drawn model. This allowed for more informed design decisions based on more realistic data. Figure 24 shows the final Momentum model drawn in ADS.

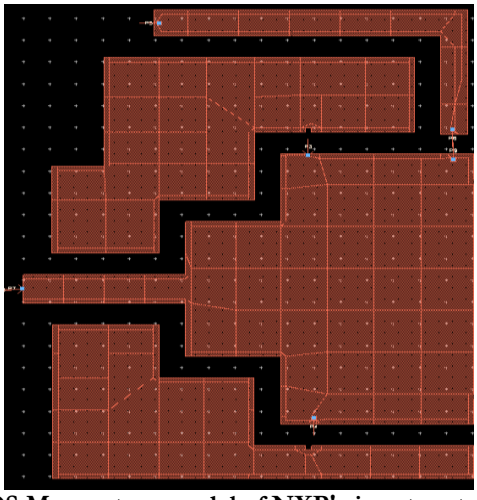


Figure 24: ADS Momentum model of NXP's input matching network

It was possible to use the Momentum model to create a schematic component that could be connected to other components such as capacitors and resistors to create a fully functional input matching network. This design could later be used in a complete system test, which was not attempted due to time constraints. The schematic shown in Figure 25 shows the nine port input matching network component with external components attached.

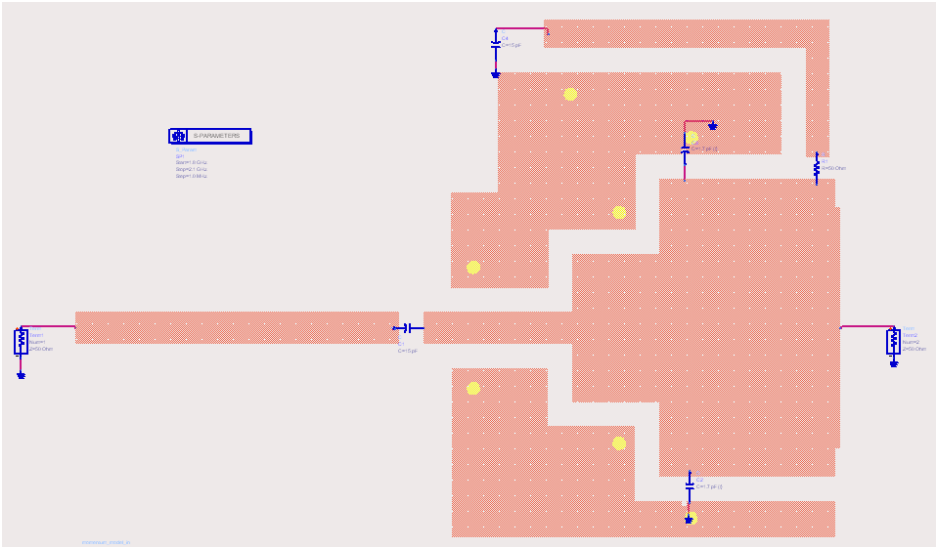


Figure 25: The input side schematic model

4.3-Output Networks

Once the input matching network was thoroughly analyzed, the project could start focusing on what NXP considered to be the root cause of the amplifier's poor video bandwidth: the output matching network. More specifically, it was suggested by NXP that the decoupling network that connects to the output matching network was the key to improving IMD performance and therefore video bandwidth. The next strategy was to make the necessary changes in the decoupling network and then adjust the matching network to fix any impedance mismatches caused by the modifications.

Once again, using NXP's AutoCAD layout file and the dimensions encoded in them, the output matching network was replicated in ADS. The schematic for this network can be seen in Figure 26. Unfortunately, the accuracy of the schematic was called into question due to the use of wide microstrip lines. A Momentum model was necessary to produce more accurate data.

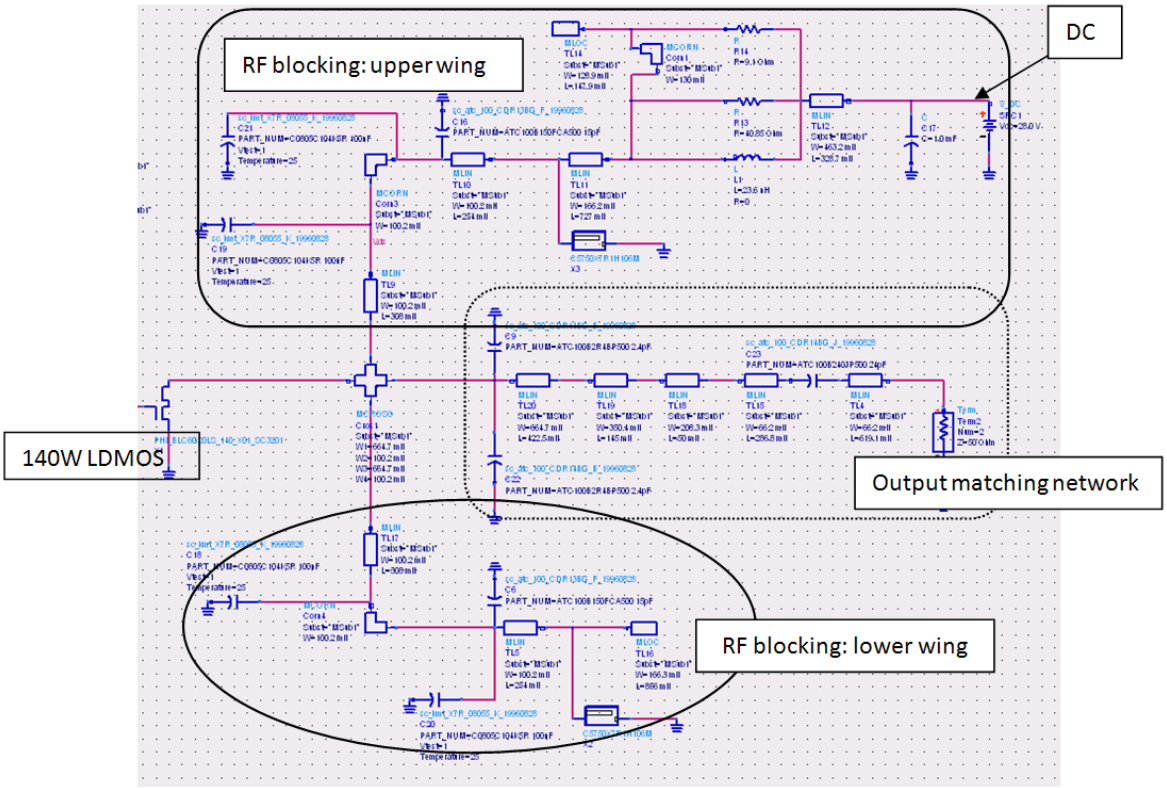


Figure 26: ADS schematic of NXP's output network

4.3.1-Decoupling Network

In general, decoupling is achieved by placing one or more capacitors across the terminals of a DC power source to serve as an extra power reserve in the event of power irregularities. In the case of this project, however, there were many powerful, spurious frequencies which affected the DC source voltage. This phenomenon made RF decoupling methods relatively complex. In principle, RF decoupling networks act as filters that are supposed to block all signals except DC. This filtering effect is achieved through a combination of capacitors and microstrip lines that act as inductors. The network designed by NXP consisted of two open-ended microstrip lines (one on each side of the matching network) with capacitors placed along them that provided high-frequency paths to ground. These "wings" also acted as part of the output matching network. DC power was fed into the upper wing while the lower wing provided symmetry about the transistor's drain terminal.

Although the best way of testing the IMD performance of the amplifier was to perform a two-tone harmonic balance simulation, simpler s-parameter simulations were used during tuning as they were much faster. Harmonic balance tests were avoided during the tuning process, as they tended to fail to execute when run at intermediate tuning steps. Once a single parameter or component was changed, the rest of the circuit usually needed to be modified to make the design sufficiently stable.

The prototype shown in Figure 26 did a fairly good job at decoupling the source. However the performance was not good when used with the transistor. The problem can be seen during the analysis of the system's input impedance (Z_{IN}) as seen through the transistor's internal matching network. The transistor's input impedance was measured by grounding the small-signal transistor model, as seen in Figure 27. This change significantly decreased input impedance and indicated that the problem did not originate solely from the transistor's internal matching network but also the decoupling networks.

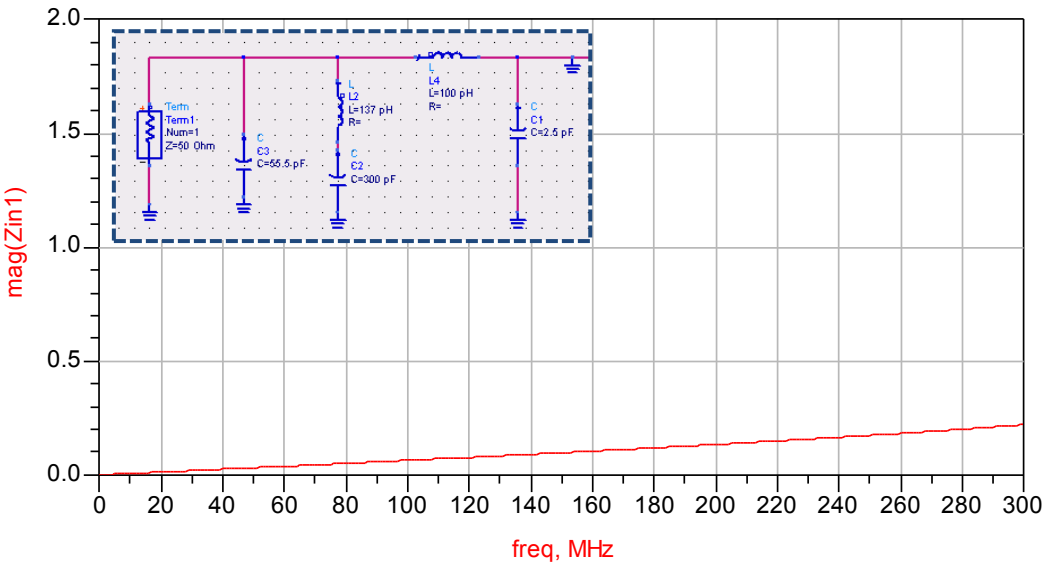


Figure 27: Transistor model grounded

The first step in the design process was to determine the current performance of the system, so that it could be compared to results after making changes. The test setup for measuring Z_{IN} can be seen in Figure 28.

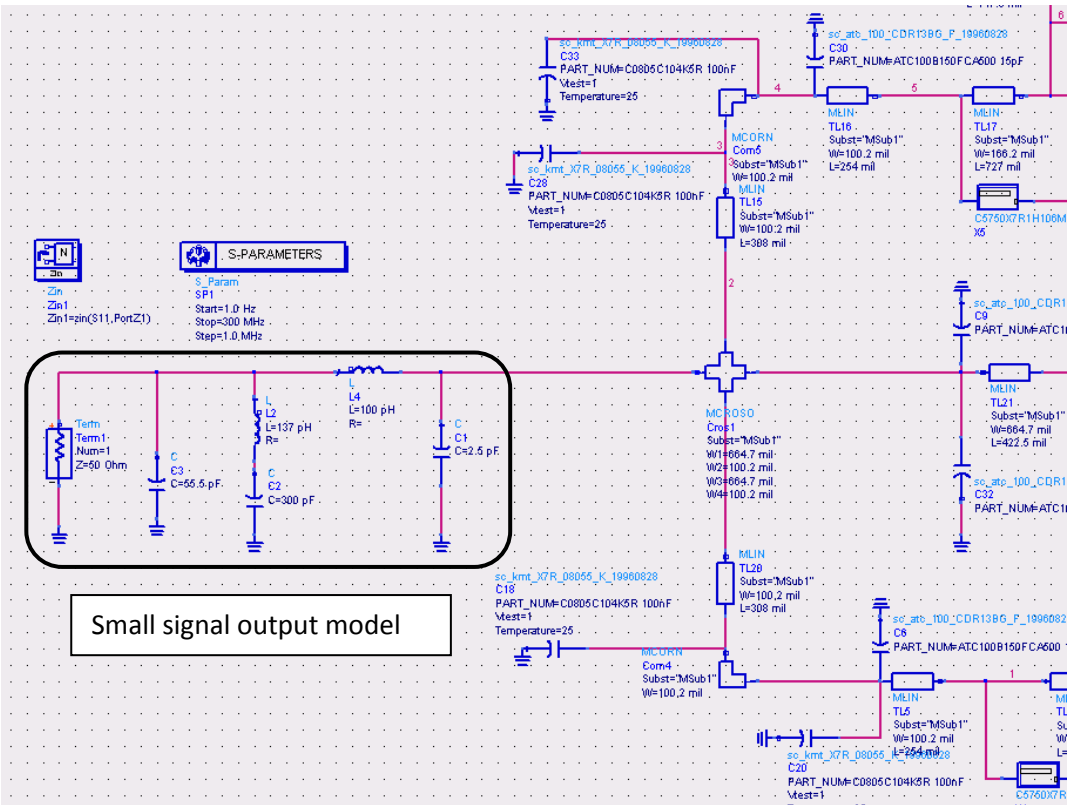


Figure 28: S-parameter test setup for measuring Z_{IN}

The original decoupling network resonated with the transistor such that high impedances were created at frequencies up to 300MHz. This was the range where second-order IMD products were created as a result of the transistor's nonlinear AB-class operation. These spurious frequencies tended to disturb the DC supply, causing further increases in nonlinearity which in turn resulted in increases in third-order inter-modulation (IMD3) products. The increase in IMD3 products caused a drop in the gain compression point and distorted the output signal since they fell within the desired signal bandwidth. By adjusting the decoupling network, it was possible to change the resonance point and create a low impedance path to ground for the second-order IMD products. With these effects in mind, the main goal was to design low input impedances up to 100MHz in an attempt to force low frequency signals to ground. The test results for the original design are illustrated in Figure 29. Any improvement was expected to result in a peak that either diminished or shifted toward higher frequencies. This behavior would indicate that the circuit has lower impedance at lower frequencies, sending unwanted frequencies to ground.

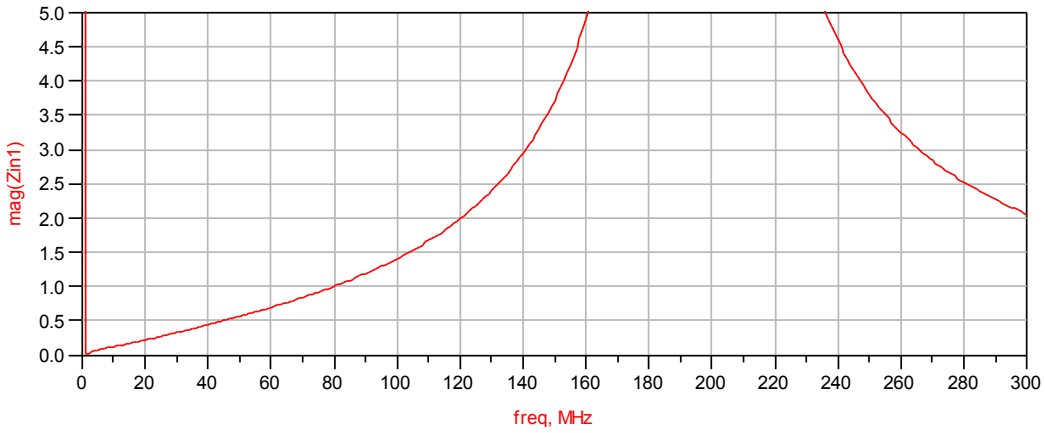


Figure 29: Z_{IN} magnitude as a function of frequency (initial performance)

Figure 30 shows the effect of shortening the length of the microstrip between the first decoupling capacitor and the transistor. The first line (red) indicates initial performance, the second line (blue) shows the effects of bringing the capacitors closer by 100mils (2.54mm) and the third line (green) shows the effect of bringing the capacitors closer by 200mils (5.08mm). This clearly illustrated that bringing the decoupling capacitors closer to the transistor moved the resonance point out of the critical range, thus improving IMD performance.

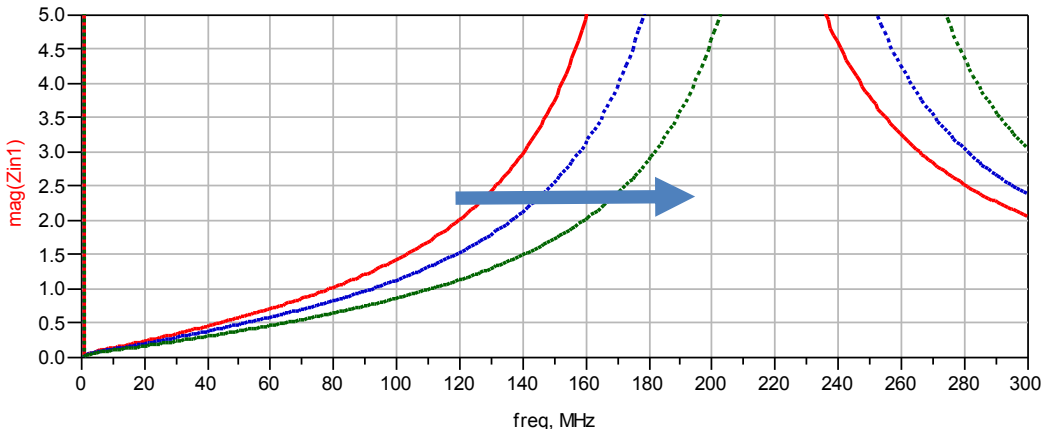


Figure 30: Effects of bringing the decoupling capacitors closer

Many other methods were tested in order to shift this resonance frequency, but they were found to be either ineffective or counterproductive. Some of the tested methods included:

- Using a lumped element filter to replace a part of the current decoupling network.
- Using different capacitor values at the decoupling network
- A grounded lambda quarter length stripline connecting to the transistor's drain, which would work by acting as an open circuit for wanted frequencies but letting the lower frequencies to ground.

The conclusion drawn from the above figures was that an improvement to the transistors internal matching network would result in a more dramatic change. Unfortunately, changes to the internal structure of the transistor were unfeasible given the scope and time constraints of the project. Therefore attention was paid to improving the decoupling network. Based on this information, it was finally concluded that by placing the decoupling network closer to the transistor, better performance could be attained. Such a modification would undoubtedly affect the impedance matching of the output matching network. Therefore, it was required to conduct further s-parameter tests to tune the output matching network to optimal matching conditions.

4.3.2-Output Matching Network

The output matching network had to be updated after making changes to the decoupling networks. Since the simulations were insufficiently accurate, the output network was not designed to match the transistor model or to an impedance value obtained from loadpull tests. Here are the steps of the output matching network design process:

1. S-parameters for NXP's matching network were recorded.
2. Decoupling wings were shortened in order to improve the IMD3 performance.
3. S-parameters were measured again after modifying the decoupling network.
4. Dimensions of the matching network were adjusted to maintain the original s-parameter values. This would ensure that the matching conditions would be equivalent between the modified matching network and NXP's original prototype.
5. Several tuning blocks were added to the final layout design to leave room for physical tuning.

After a period of testing, it was discovered that wide strip lines caused inaccuracies in the schematic representation of the output matching network. Such dimensions caused convergence issues in ADS' harmonic balance solver engine. Therefore a Momentum model, as seen in Figure 31, was constructed to overcome this problem.

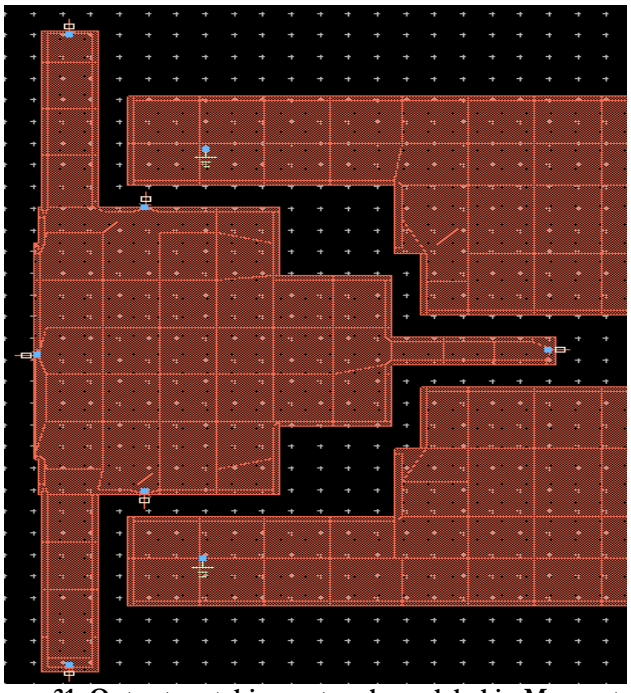


Figure 31: Output matching network modeled in Momentum

The decoupling network was cut short in the Momentum model since it was assumed that RF effects were negligible beyond the first decoupling capacitor. The model had eight ports for connecting to the rest of the circuit and other lumped elements. The s-parameter measurements used in the design process were obtained using this model. The decoupling wings on both sides were made shorter by 100 mils (2.54mm) to represent the effect of bringing the capacitors closer. Then the tapers in the matching network were adjusted to obtain the original s-parameter values.

In order to use this model in the harmonic balance simulation, it had to be transferred into a schematic where it could be treated as an eight-port component. After the model was populated with the surrounding elements, an s-parameters test was performed. Using these results, a two-port model of the output network could be generated for use in a complete system test, which was not attempted due to time constraints. The populated output model in an s-parameter test configuration can be seen in Figure 32.

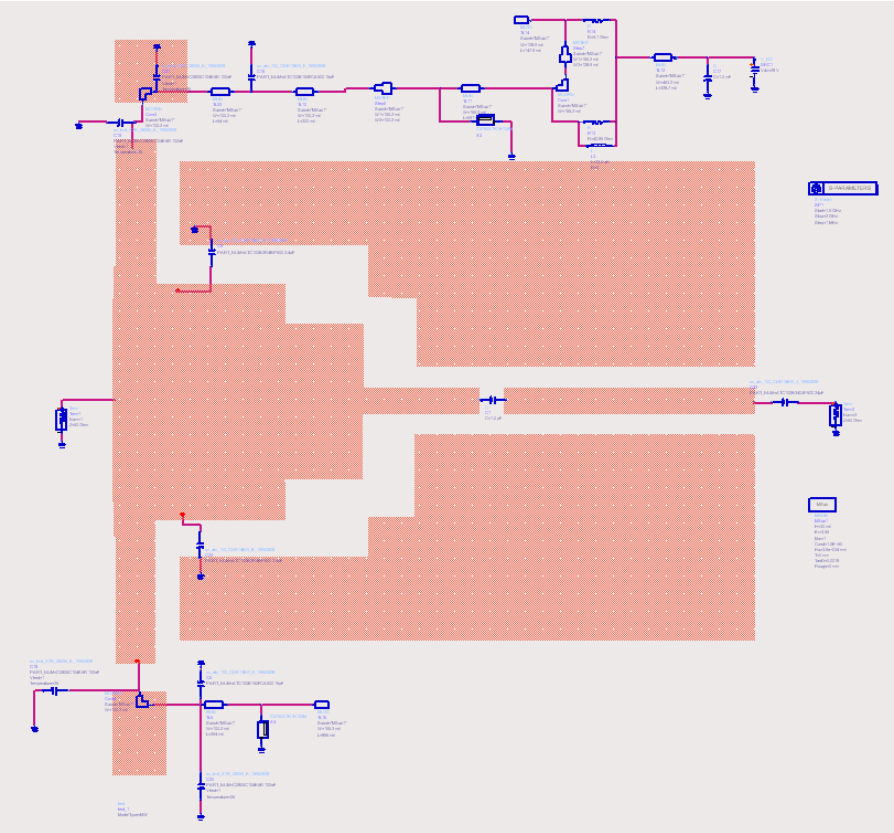


Figure 32: The populated Momentum model of the output side

5-Physical Implementation

Extensive simulation soon led to practical application, when a final layout was chosen to reflect what was learned in ADS. The layout was constructed according to the project's as well as NXP's design requirements. This latter half of the methodology called for precise measurements and consistent procedure with advanced instrumentation and data acquisition software. It was in this phase where the success of the project would be determined.

5.1-Construction

When the final layout was designed in AutoCAD, the design was presented to NXP for review. Once the design was approved, it was sent to be processed, which included updating the design with new components. These new components included more compact active bias and DC supply circuitry designed to work with a variety of amplifier designs. This processing also included the addition of AutoCAD layers necessary to manufacture the layout, including layers for etching, masking and labeling. NXP received the finished boards approximately one week after the AutoCAD design was submitted. A total of 12 sets were made using Taconic RF-35 substrate. The completed microstrip layout can be seen in Figure 33 below:

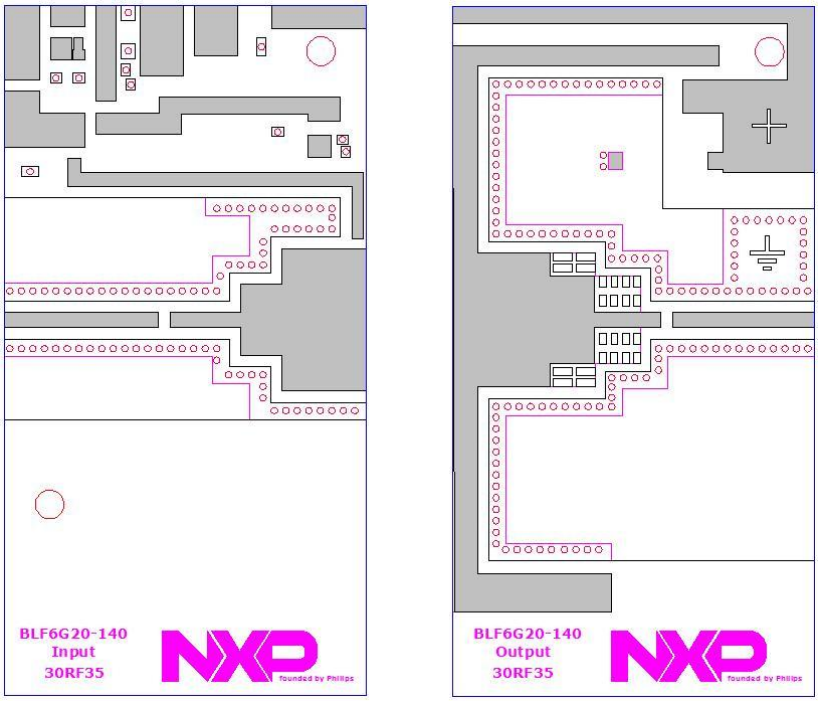


Figure 33: Final layout of the new amplifier design

The test board was constructed on February 1, 2008 using standard NXP procedures. The first step in this procedure was to prepare the boards and brass heat sinks (one of each for the input side and output side) for joining by cleaning the surfaces with rubbing alcohol and applying a layer of flux. The flux allowed for easier solder flow as both surfaces required an even coat of solder. Once excess solder was removed, the boards were bolted to the heat sinks to ensure proper placement while they were pressed together in a fixture. The fixture was then placed on a hot plate until it reached a temperature of 150°C and the solder joint was formed. A photograph of this step can be seen in Figure 34 below:

Figure 34: Fixture and hot plate for placing boards on heat sinks

The boards were populated once they were air cooled and inspected. Inspection ensured that the boards were properly placed on the heat sinks (the circuit ground) and that the microstrip traces remained uncompromised. The board featured standard NXP components, ports and power supply terminals. However, an unconventional feature of this new board was the placement of two tuning capacitors on the input matching network, where NXP normally uses only one. The extra capacitor was chosen for added design flexibility and to ensure input return loss symmetry about 1960MHz. Once the input board and output board were populated, they were bolted together with a smaller copper heat sink in between. The copper heat sink was where the LDMOS transistor was mounted (via the transistor's source terminal). Once the boards were joined, the transistor's gate terminal was soldered to the input matching network and the drain terminal was soldered to the output matching network. The circuit was complete with the attachment of a jumper wire connecting the DC power supply to the active bias network. The completed circuit was bolted to another brass plate at the test bench that featured passages for water cooling. A photo of the complete circuit (except the jumper connection) can be seen in Figure 35.

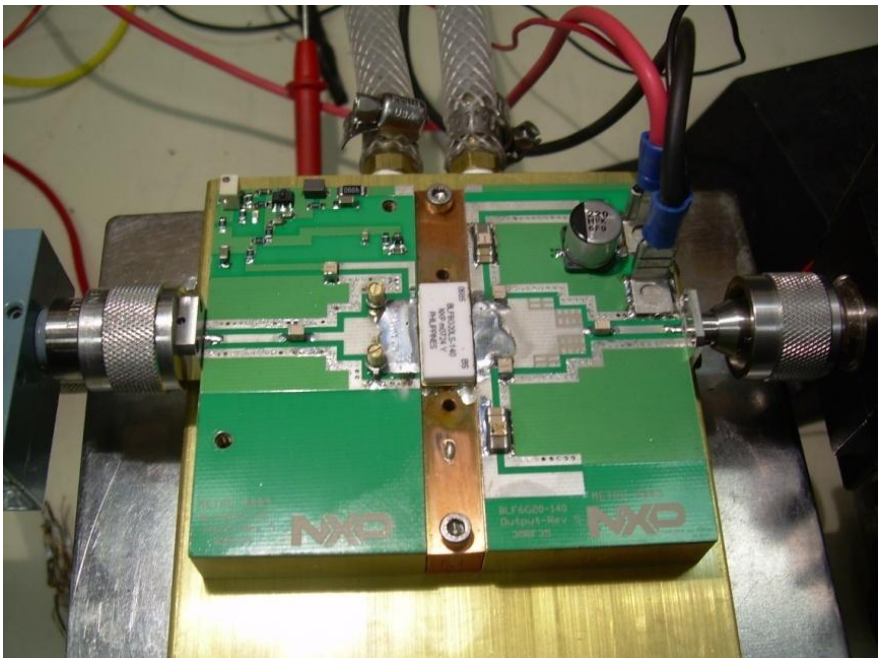


Figure 35: Circuit assembly and placement in test bench

5.2-Testing and Tuning

A bench for the physical testing of the new amplifier circuit was assigned while the boards were still in the manufacturing process. The test bench was similar to others used at NXP for the analysis and testing of amplifier circuits. Figure 36 describes the test bench and how the data is acquired. The test bench included the following equipment:

- Network Analyzer: Hewlett-Packard 8753ES
- Digital Multimeter: Hewlett-Packard 34401A
- DC Power Supply: Hewlett-Packard 6653A
- Spectrum Analyzer: Rohde & Schwarz FSEM 20
- Vector Signal Analyzer: Agilent E4406A
- Water cooling circuit regulated to 25°C
- 2 Signal Generators:
    - Agilent E4433B
    - Rohde & Schwarz SMIQ 03B
- PCS power amplifier of NXP's own design
- Power Meter and 2 Power Sensors:
    - Hewlett-Packard E4419A
    - Hewlett-Packard 8481A (Qty. of 2)
- Computer with Agilent VEEPro and SoftPlot installed

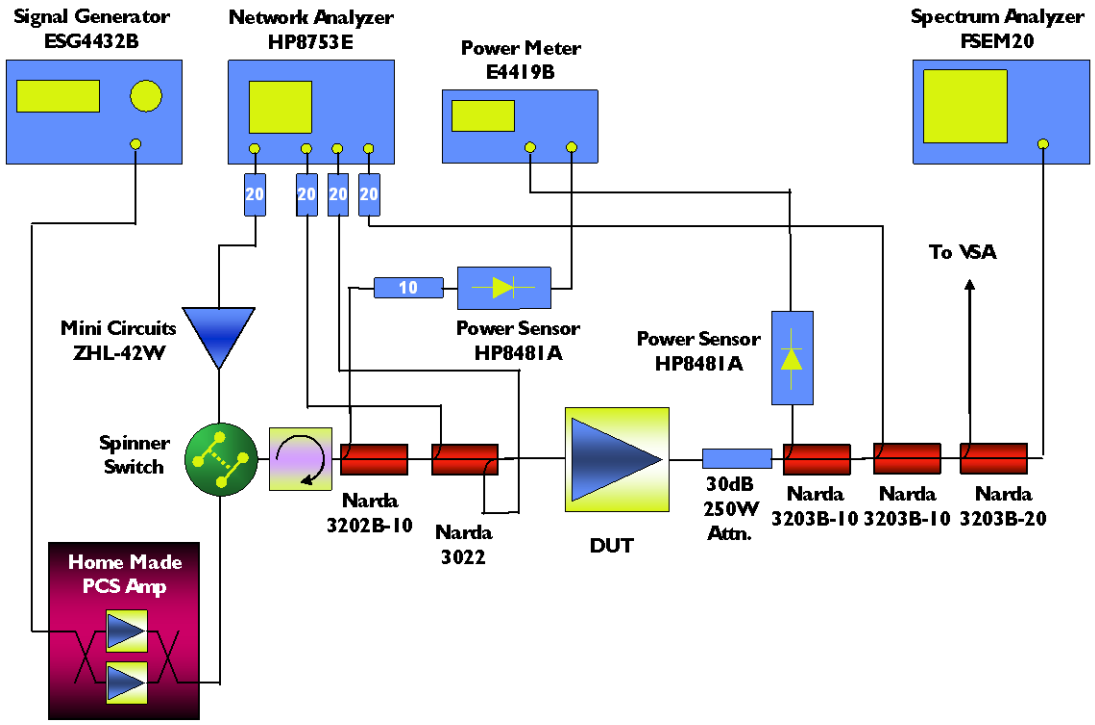


Figure 36: Diagram of test bench (courtesy of NXP)

In the above diagram, numbered blocks represent signal attenuators that protect the instruments from excessive power levels. The blocks labeled "Narda" represent directional and bi-directional couplers that transfer RF power. "DUT" represents the device under test, which in this case was the new amplifier design. Initial tests were performed manually by changing the power level and frequency, then recording the measurements from the spectrum analyzer. For complex test routines that required many data points, automated measurements were recorded via computer using VEEPro software. VEEPro allowed the computer to interface with the instruments, perform controlled parameter sweeps and make calculations based on recorded measurements.

Some of the first measurements taken from the new design were those for Input Return Loss (IRL), power gain, peak output power and Adjacent Channel Power Ratio (ACPR). These initial results represent circuit performance without any modifications and minimal tuning.

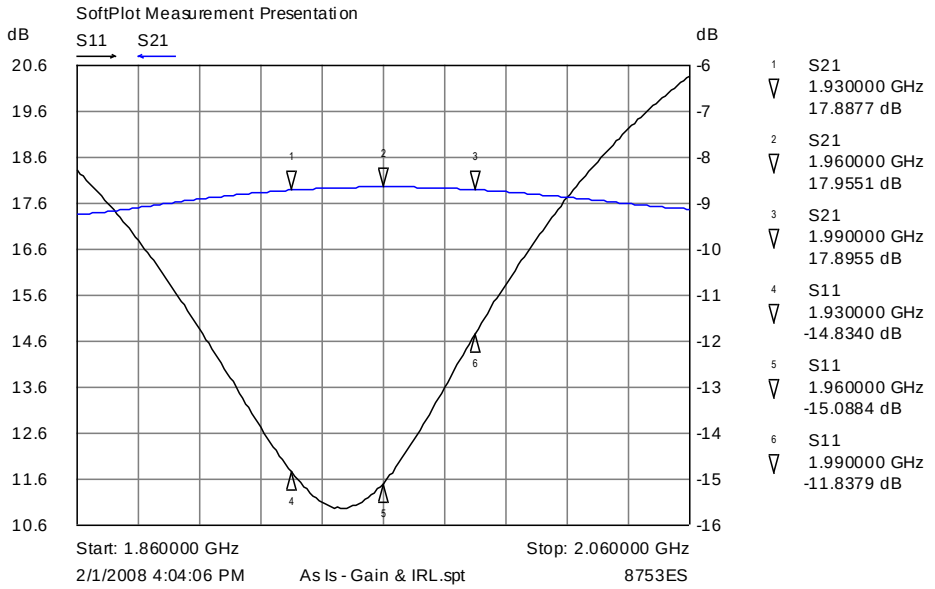


Figure 37: Initial IRL (S11) and power gain (S21) performance was within specification

To measure the peak power output of the circuit, an IS-95 modulated input signal was applied and the input RF power was increased until the signal's Complementary Cumulative Distribution Function (CCDF) was compressed by 3dB. This was found by increasing the input power until the peak power of the output signal decreased to 6.7dB above average for 0.01% of the signal's time span (a measurement obtained from the vector signal analyzer). Therefore, the sum of the average power with the peak increase at 0.01% probability produced the peak output power of the system as defined by NXP. The circuit's ability to accept momentary spikes in input RF power without compressing digital signals is directly proportional to this figure. Peak power measurements for the initial design were within specification and are presented in **Error! Reference source not found.** below:

Freq. (MHz)	Avg. Pout (dBm)	Power Increase @ 0.01% Prob. (dB)	Ppeak (dBm)	Ppeak (W)
1930	46	6.75	52.75	188.4
1960	46.11	6.72	52.83	191.9
1990	46.09	6.77	52.86	193.2

Table 1: Initial peak power performance was within specification

A sweep of the circuit's input RF power yielded more data. These results have been reported at three different frequencies at an output power of roughly 45dBm (32W) as presented in Table 2:

Freq. (MHz)	Pout (dBm)	Pin (dBm)	Idrain (A)	Power Gain (dB)	Drain Efficiency (%)	ACPR (dBc)	
						at 1.98 MHz	at 885 kHz
1930	45.06	27.19	3.71	17.88	30.87	-63.25	-45.95
1960	45.04	27.05	3.73	17.99	30.59	-63.27	-46.33
1990	45.05	27.18	3.70	17.87	30.83	-62.94	-46.24

Table 2: Initial power sweep results were satisfactory

Even at this point the data collected had been substantial. Nevertheless, the amplifier's maximum carrier spacing was still to be determined. Maximum carrier spacing is defined as the carrier spacing above which 3rd-order Inter-Modular Distortion (IMD3) products exceed -33dBc. Normally IMD3 magnitudes are determined by conducting a test where one signal generator is set at the center frequency while a second signal generator conducts two sweeps. One sweep would increase the frequency to 100MHz above the center while the next sweep would decrease the frequency to 100MHz below center. For this test, it was decided to conduct the sweeps such that the fixed frequencies were within the bounds of the circuit's intended operating spectrum. That is, one sweep would increase the frequency 100MHz above a 1930MHz fixed frequency while the next sweep decreases the frequency 100MHz below a 1990MHz fixed frequency. The results of these two sweeps can be seen in Figure 38 and Figure 39.

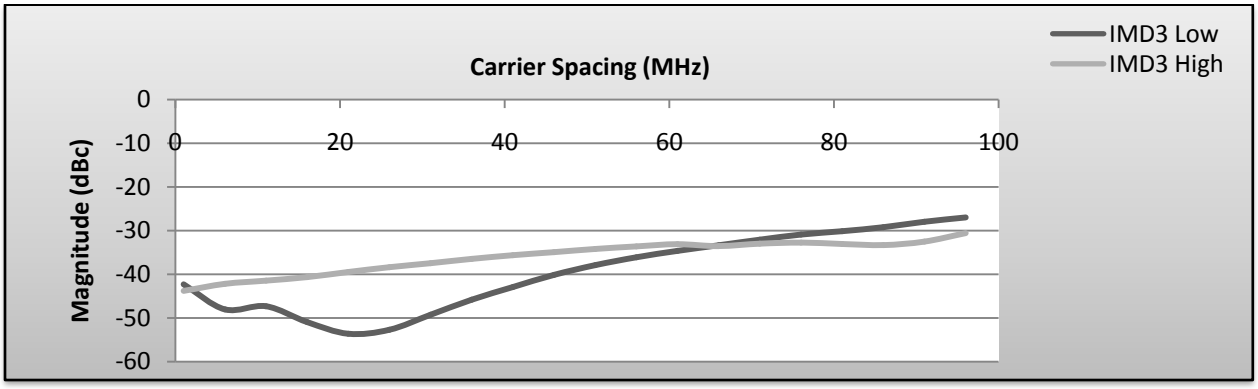


Figure 38: Initial IMD3 performance (carrier sweep from 1930MHz to 2030MHz)

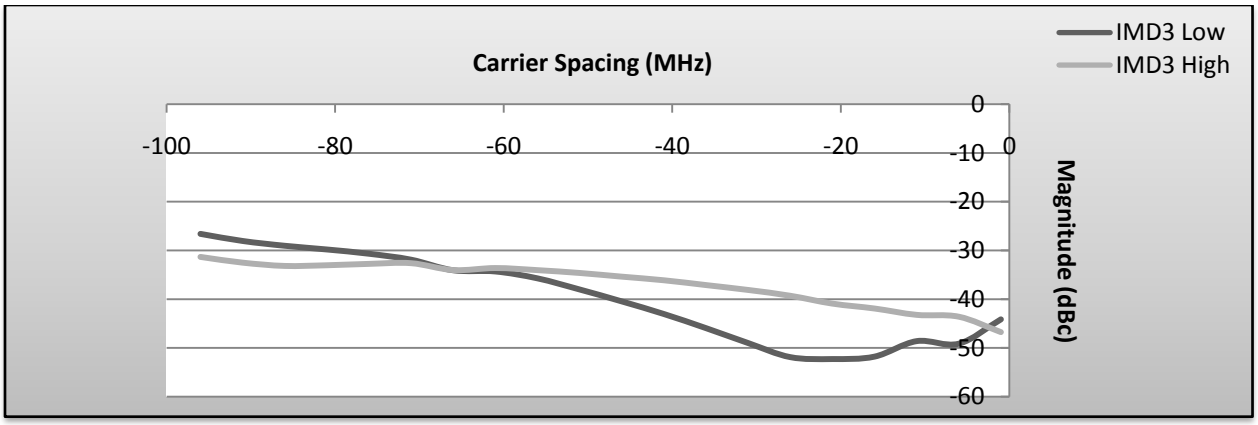


Figure 39: Initial IMD3 performance (carrier sweep from 1990MHz to 1890MHz)

While the design performed well in peak power and power sweep testing, the same could not be said for maximum carrier spacing. Indeed, the above IMD tests illustrate the true nature of the challenge that this project addressed. The results of this first test indicated a maximum carrier spacing of 60MHz before IMD3 magnitude became excessive. This left no margin for error or variation, making it insufficient for a practical application where carriers between 1930-1990MHz may be experienced. Making matters worse was the wide variation in IMD3 magnitude as well as the extreme asymmetry from one IMD3 product to another. The ideal IMD3 response is one where both IMD3 products are roughly equivalent in magnitude and constant as carrier spacing increases. These initial tests indicated that there was still much work to be done if this ideal response was to be achieved.

Given the wide variation and asymmetry observed in IMD testing, the first attempt at improving performance was to optimize the tuning of the input matching network such that IRL was symmetrical about 1960MHz. Unfortunately, this did little to improve performance as the circuit was still constrained to a maximum carrier spacing of 60MHz. IMD3 variation and symmetry were still poor. This can be seen in Figure 41.

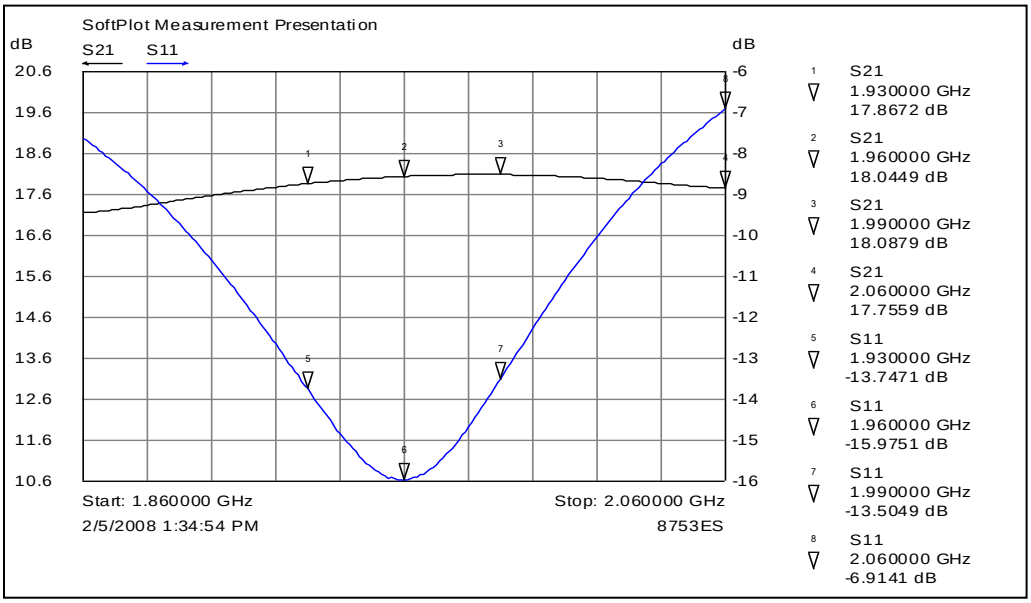


Figure 40: Tuning for symmetrical IRL

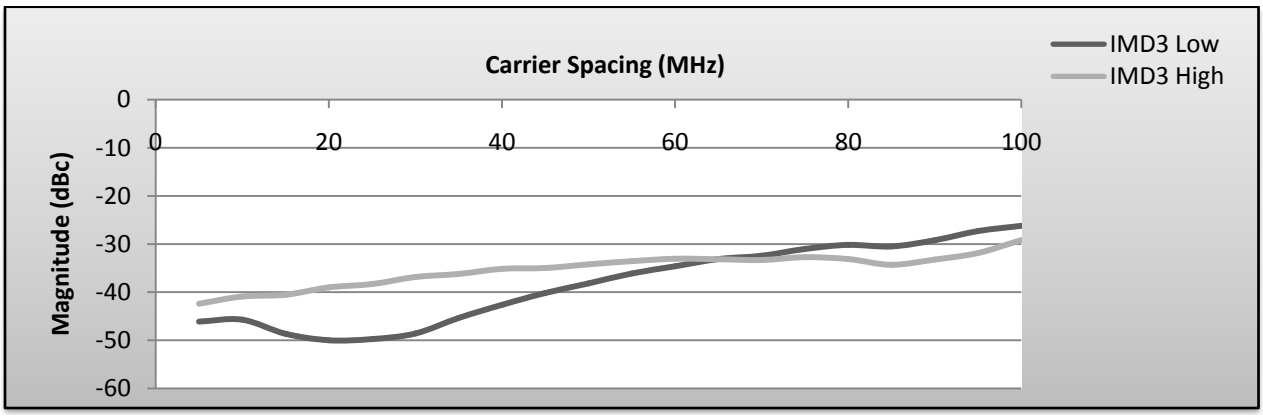


Figure 41: IRL tuning did not improve IMD3 performance significantly (sweep from 1930MHz to 2030MHz)

By this point it was clear that a new strategy for improving IMD3 was required. It was soon suggested by NXP that the cause of this poor performance may not be the output network, but rather the new active bias network introduced during the final steps of the layout design. To pursue this possibility, one of the resistors in the active bias network (highlighted in Figure 41) was replaced with one of greater resistance (200Ω). The capacitor to the left of this resistor charges and discharges through the transistor's internal ESD (Electro-Static Discharge) protection circuit. The larger resistance increased the RC time constant in that particular region of the network, which slowed the discharging of the capacitor and stabilized the bias voltage.

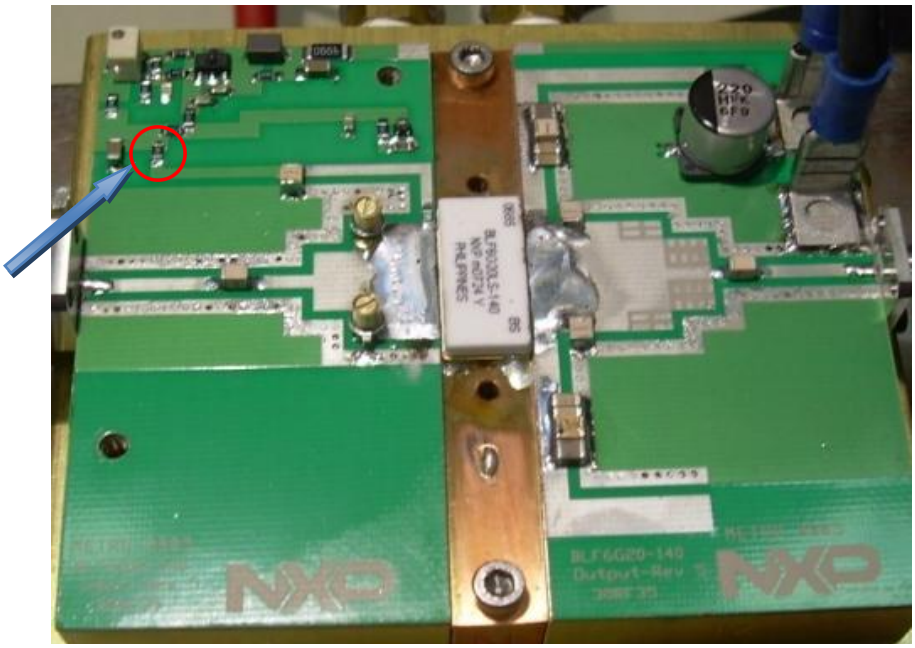


Figure 42: The circled resistor was replaced in an attempt to improve IMD3.

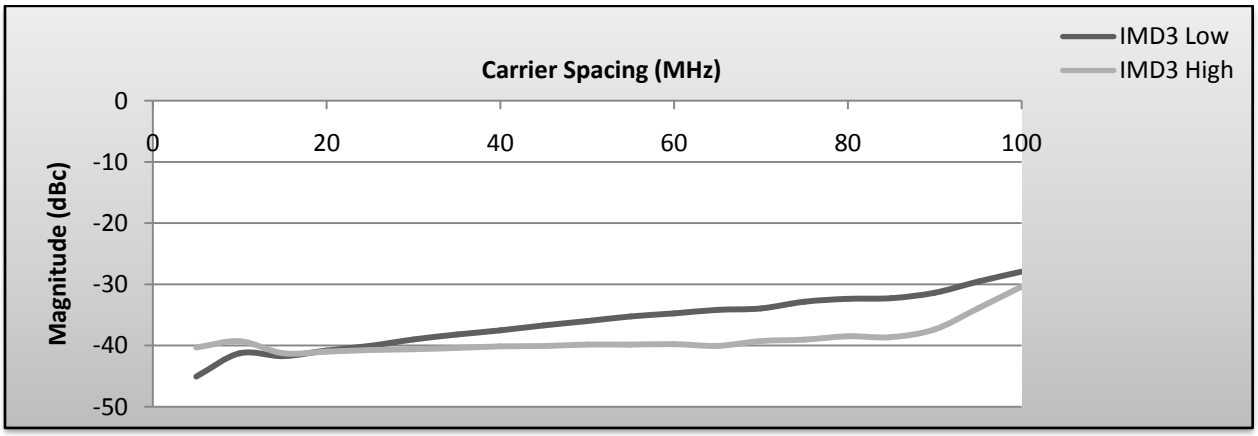


Figure 43: Greater resistance improved IMD3 performance (carrier sweep from 1930MHz to 2030MHz)

Another round of testing revealed that increasing the resistance in that particular part of the active bias network had indeed improved IMD3 performance. More specifically, this modification alone had decreased IMD3 such that a maximum carrier spacing of 70MHz could be achieved before IMD3 magnitude became excessive. Symmetry between the two products had also improved slightly and the magnitude variation in the higher-frequency IMD3 product appeared to be minimized. Unfortunately, variation in the low IMD3 product still appeared to be a problem.

By this point, it was time to test the effects of decoupling capacitor placement on IMD3. During the computer simulation phase it was concluded that moving these capacitors closer to the

transistor's drain terminal would improve the amplifier's IMD performance. These capacitors have been highlighted in Figure 44:

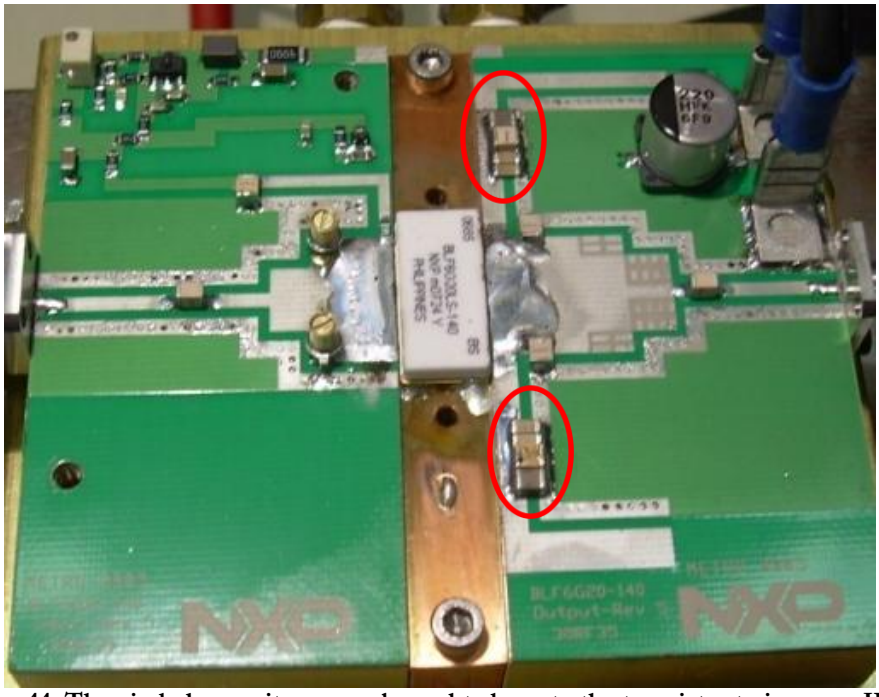


Figure 44: The circled capacitors were brought closer to the transistor to improve IMD3

This latest modification would prove to confirm the capacitor placement hypothesis, as the amplifier's maximum carrier spacing increased to 75MHz. Again, the amplifier's maximum carrier spacing is defined as the carrier spacing above which IMD3 products exceed -33dBc in magnitude. Placing the decoupling capacitors closer also brought the system closer to an ideal IMD3 response. IMD3 symmetry was maintained throughout a larger portion of the operating band and magnitude variation had decreased among both IMD3 products.

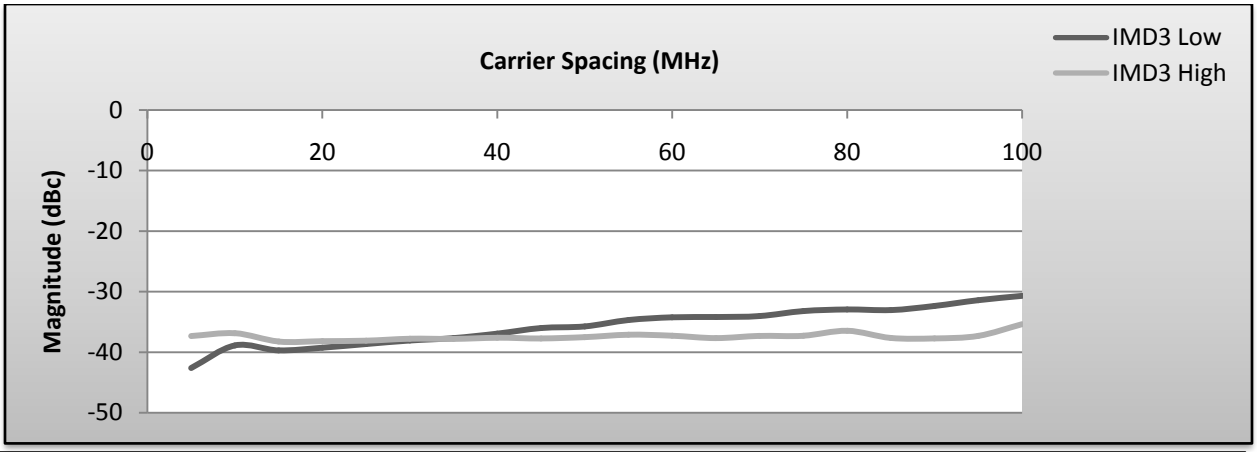


Figure 45: Closer placement of capacitors to the transistor improved IMD3 (carrier sweep from 1930MHz to 2030MHz)

Encouraged by this development as well as the results from the increase in resistance, the next step was to observe the effects of further increasing the value of the resistor highlighted in Figure 42 to 1kΩ. At first glance, this latest modification did not appear to have changed the system's IMD3 response. Indeed, the amplifier's maximum carrier spacing was the same before and after the increase in resistance. However, it is interesting to note how the modification had affected IMD3 magnitude and variation. In Figure 46, both IMD3 products seemed to be within 3dB of each other for up to 60MHz in carrier spacing! The magnitude of the higher-frequency IMD3 product was almost perfectly flat throughout the sweep and magnitude variation in the lower-frequency product seemed to have diminished as well.

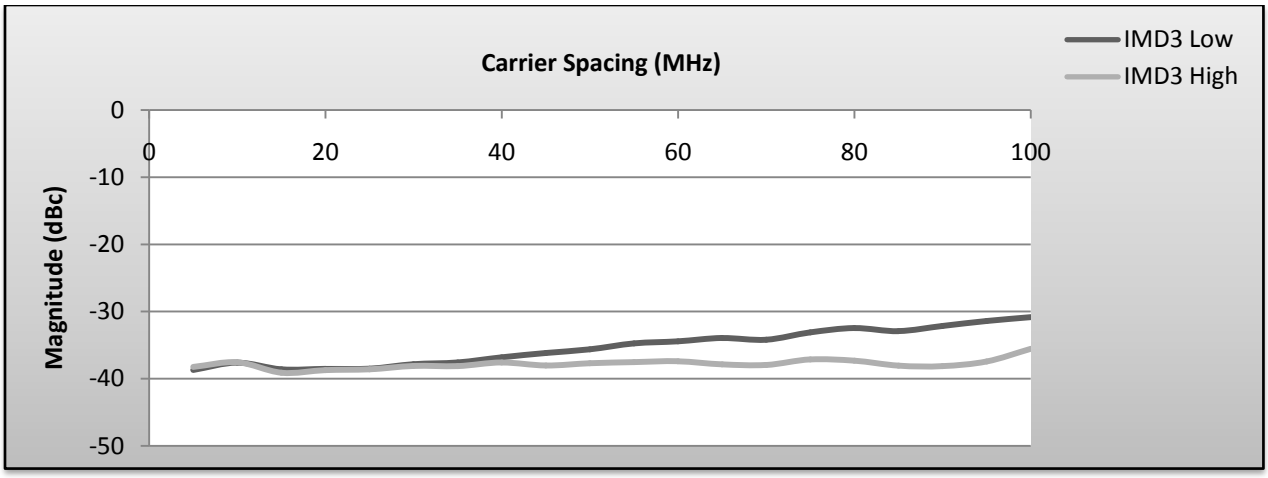


Figure 46: IMD3 after increasing active bias resistance to 1kΩ (sweep from 1930MHz to 2030MHz)

While the project was making significant progress as far as IMD3 flatness and symmetry were concerned, IMD3 magnitude still needed to decrease if the amplifier's maximum carrier spacing was to increase. A radical suggestion by NXP was to adjust the transistor's quiescent current. This suggestion was met with apprehension as it would cause a change in the transistor's operating point and potentially further decrease linearity. After testing with different I_{DQ} points, it was found that an I_{DQ} of 1000mA resulted in better performance. As Figure 47 will show, this modification resulted in significant performance gains.

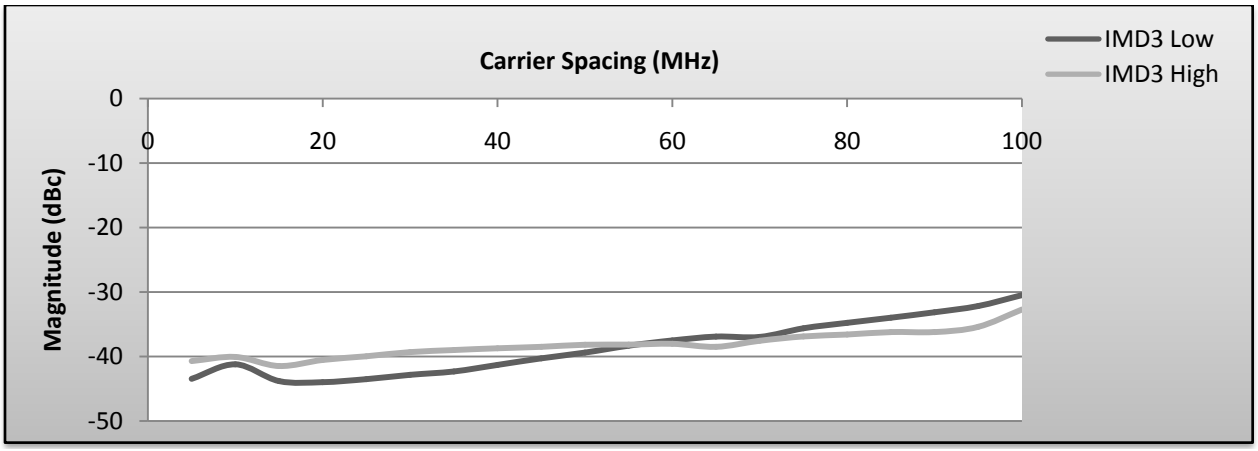


Figure 47: Reduction of I_{DQ} further improved IMD3 performance (carrier sweep from 1930MHz to 2030MHz)

The amplifier appeared to have benefited from the reduction in I_{DQ}. Given a constant power output of 45dBm (32W), the transistor's drain efficiency had improved. The amplifier's maximum carrier spacing also experienced a significant increase to 90MHz, as the system was able to handle a 90MHz spacing between signal carriers before IMD3 products exceeded -33dBc. However, it can be clearly seen that IMD3 magnitude variation has significantly increased as well as the asymmetry between the two IMD3 products. This meant that the active bias and decoupling networks required further refinement.

The next step in optimizing the performance of the amplifier was to further increase the RC time constant in the active bias network. This measure led to good results the last time it was attempted. This time, the resistance was increased to 6.2kΩ and the capacitance was increased to 10μF. It was expected that such a design change would yield better results. Unfortunately, this was not the case as IMD3 symmetry and variation only slightly improved as seen in Figure 48. Based on this data, it would appear that these changes to the active bias network only have a significant effect up to a certain RC constant. Beyond this point, only minimal effects are experienced by the system.

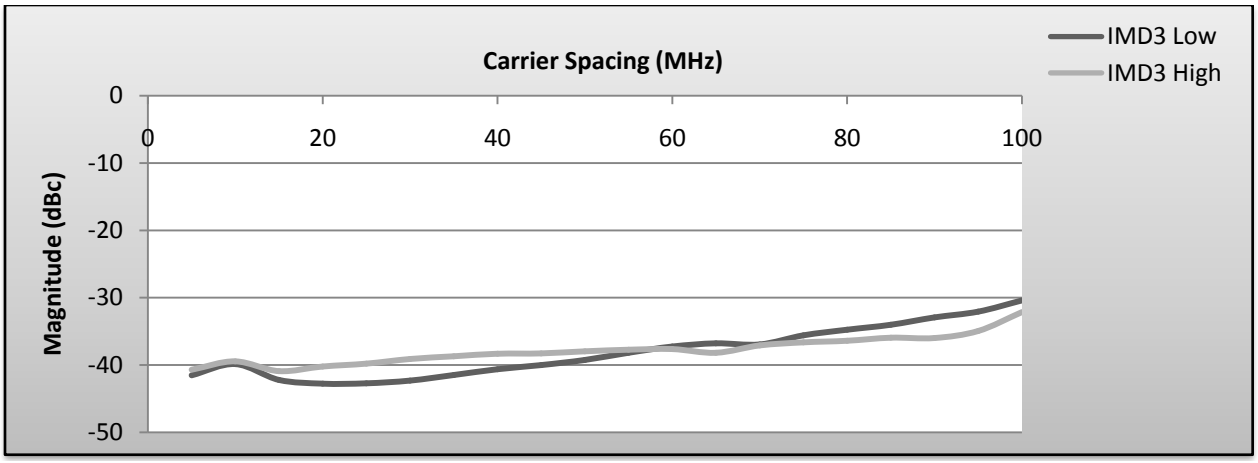


Figure 48: IMD3 performance after further modifications to the active bias network (carrier sweep from 1930MHz to 2030MHz)

By this point in the project, it was decided to view IMD3 from a different perspective. Recall from the beginning of this section that IMD3 tests are normally conducted by setting the fixed frequency at the center of a system's operating spectrum (1960MHz in this case) and that the majority of the tests discussed in this report were conducted with the fixed frequency set at 1930MHz (where the system's operating spectrum starts). Review of the IMD3 test procedure indicated that with the fixed frequency set at 1930MHz, the lower-frequency IMD3 product is generated outside of the system's operating spectrum at narrower carrier spacings. This realization led to another IMD3 test using the normal procedure where two sweeps are conducted from 1960MHz. The first sweep goes up to 2060MHz and the second sweep goes down to 1860MHz. Such a procedure ensured that IMD3 products generated from narrow carrier spacings remained within the amplifier's operating spectrum, leading to a more thorough analysis of the amplifier's IMD3 performance.

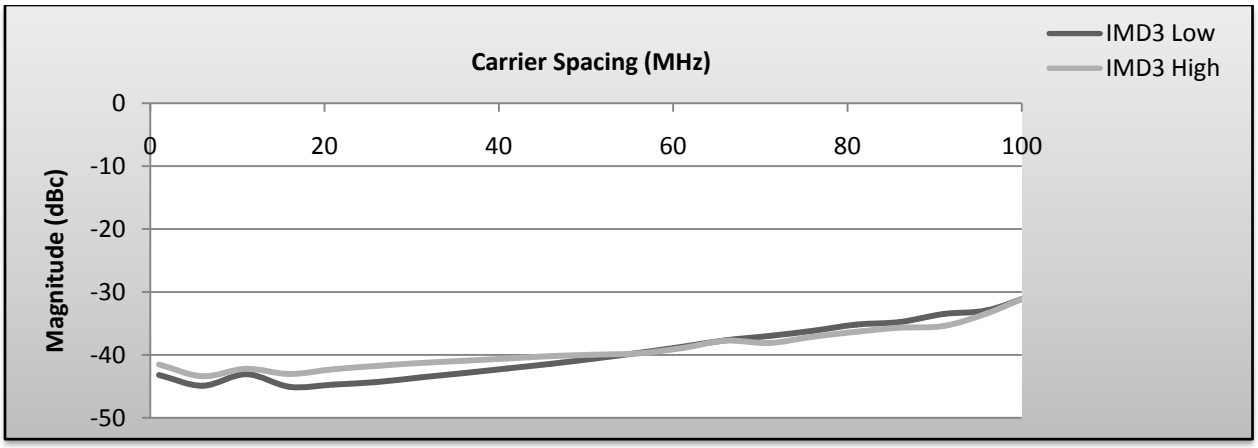


Figure 49: IMD3 performance using normal testing procedures (carrier sweep from 1960MHz to 2060MHz)

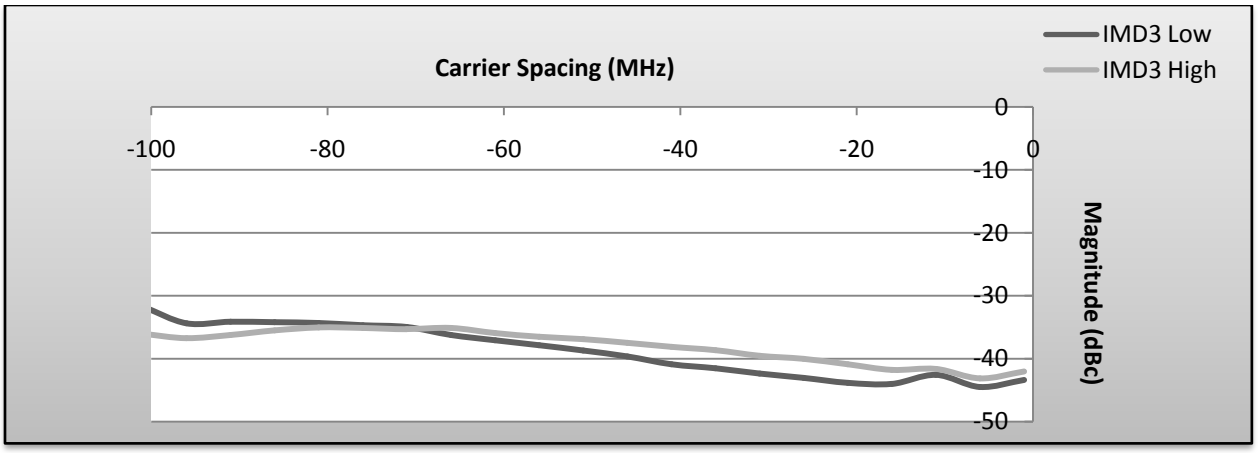


Figure 50: IMD3 performance using normal testing procedures (carrier sweep from 1960MHz to 1860MHz)

With this testing strategy (NXP's standard procedure), two sets of data are generated with the data from Figure 49 analyzed first. From this first sweep, it was concluded that if one carrier was set at 1960MHz, then another carrier can reach as high as 2050 MHz (a 90MHz carrier spacing) before IMD3 reached excessive levels. A similar analysis of the second sweep suggests that for the same fixed-frequency carrier, another carrier can reach as low as 1865MHz before excessive IMD3 was generated. These results are similar to those of the previous test in that they indicate a 90MHz maximum carrier spacing for the amplifier. To summarize, these new tests have reconfirmed previous test results while providing a new perspective of the system's IMD performance.

Based on the data that was collected, it seemed that the active bias network could be improved no further. Therefore attention was directed back to the decoupling and input matching networks. However, this time it was desired to not only improve IMD, but also improve peak power. While the main objective of the project was to increase maximum carrier spacing (thereby increasing video bandwidth), peak power could not be neglected as it determines the system's ability to handle momentary spikes of input RF power without compressing them. This makes peak power an important practical consideration when applying power amplifiers in cellular communication networks. NXP specified a minimum peak power rating of 52.7dBm (186W).

To improve IMD performance, the decoupling capacitors needed to be moved closer to the transistor. However, these adjustments also required that the output matching network be reshaped to compensate for the changes in matching conditions and maintain or increase peak power. Modification to the output matching network involved both shortening and widening a section of the output line. Shortening was achieved by carefully trimming the output line with a knife.

Widening the output line involved soldering squares of copper foil over the tuning blocks designed around the output line. All proposed modifications had to be checked before they were applied, because changes to matching networks are hard to reverse. Checking proposed modifications involved pressing down a piece of copper foil attached to a wooden stick and noting the changes in peak power output. If a proposed modification caused an improvement in peak power, then the modification was applied to the circuit for IMD3 testing. This process resulted in modifications that seemed to decrease IMD3 performance. The modified output network is highlighted below:

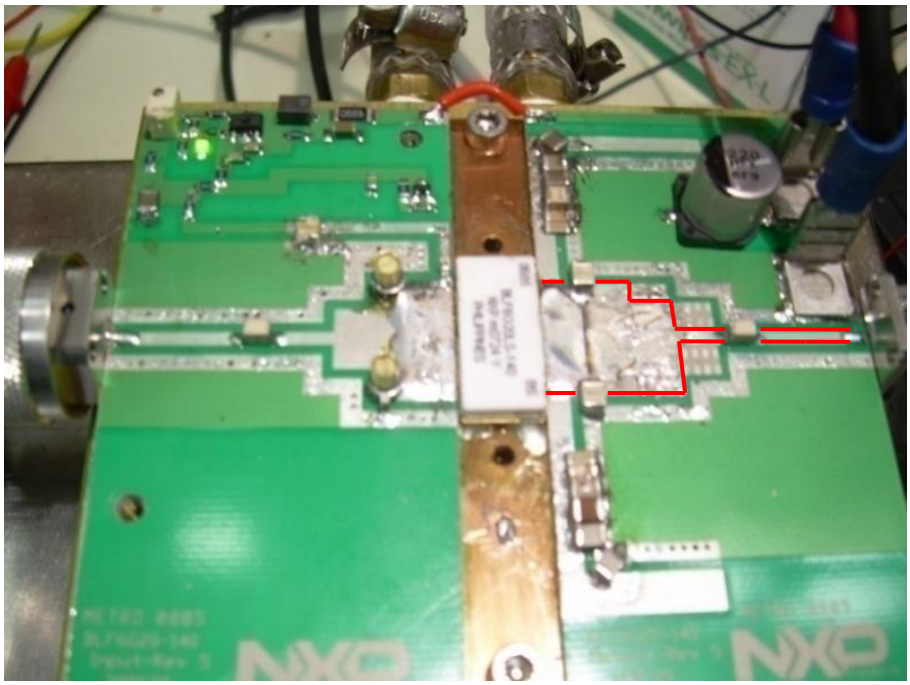


Figure 51: Decoupling capacitors were moved closer to the transistor's drain and microstrip area was increased in the output matching network

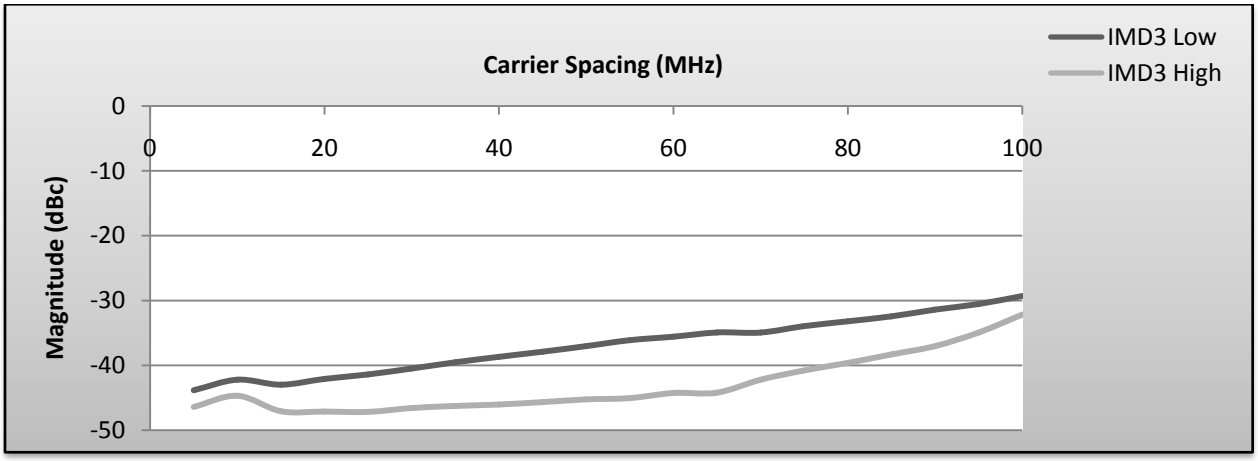


Figure 52: IMD3 as a result of modifications made in Figure 51 (sweep from 1930MHz to 2030MHz)

Before analyzing the results in Figure 52, it is important to note that the test procedure was changed back to the procedure involving one carrier sweep where one carrier was fixed at 1930MHz and the other was swept from 1930MHz to 2030MHz. This was done in order to expedite the optimization of the amplifier, as optimization with the more accurate two-sweep IMD3 test would have taken much longer.

Analysis of the results illustrated in Figure 52 indicated a drastic decrease in performance. The amplifier's maximum carrier spacing decreased to 80MHz and asymmetry results were the worst seen during the course of the project. This development illustrated just how challenging it is to design a power amplifier for both low IMD and high peak power. There was clearly a need for a better compromise between both goals. Therefore it was decided to move the decoupling capacitors farther back from the transistor.

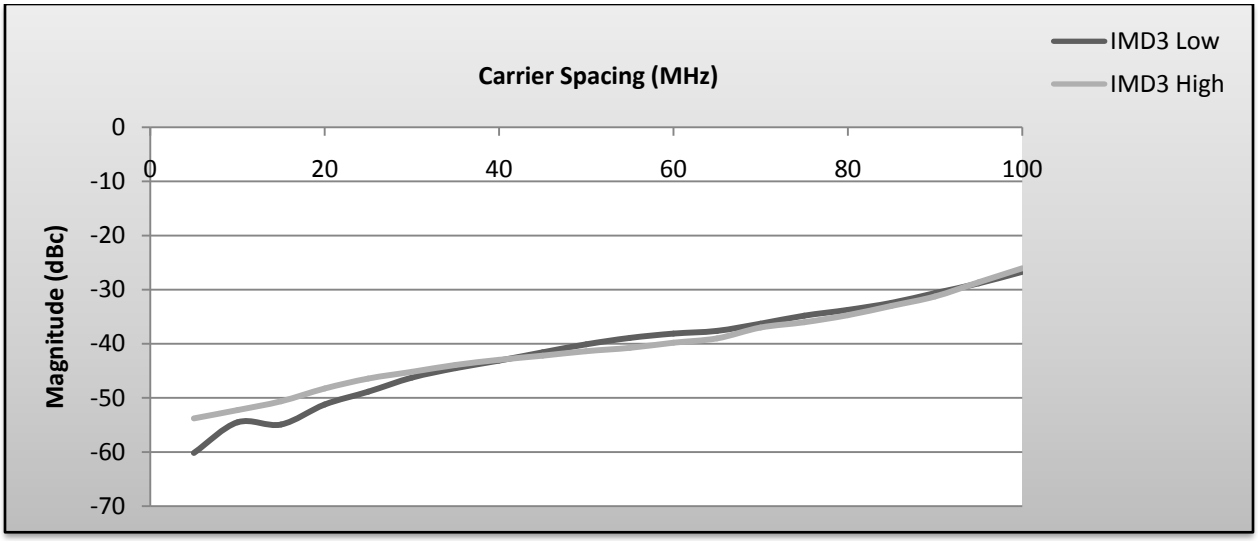


Figure 53: Final development in IMD3 improvement (carrier sweep from 1930MHz to 2030MHz)

Moving the capacitors back seemed to have greatly improved IMD3 symmetry, but IMD3 variation and magnitude were still far too high. These results give the amplifier a maximum carrier spacing of 80MHz. By this point the time allocated to testing and tuning had drawn to a close and no more improvements could be developed for the circuit. However, the circuit design showed great promise and it is believed that, given more time, even better performance could be achieved.

5.3-Final Results

Now that the design and development of the amplifier circuit has been discussed, comparisons can be made between NXP's initial design and the design created from this project. Final results reflect the data collected from the final development of the amplifier design created from this project. The comparison will begin with the peak power performance of both designs.

Peak Power BLF6G20LS-140 Board 632 (Designed by NXP) Vds=28V, Idq=1200mA				
Freq. (MHz)	Avg. Pout (dBm)	Power Increase @ 0.01% Prob.	Ppeak (dBm)	Ppeak (W)
1930	46.36	6.65	53.01	200.0
1960	46.36	6.72	53.08	203.2
1990	46.34	6.68	53.02	200.4
Peak Power BLF6G20LS-140 Amplifier (Designed by WPI) Vds =28V, Idq=1000mA				
Freq. (MHz)	Avg. Pout (dBm)	Power Increase @ 0.01% Prob.	Ppeak (dBm)	Ppeak (W)
1930	46.18	6.71	52.89	194.5
1960	46.2	6.7	52.9	195.0
1990	46.1	6.7	52.8	190.5

Table 3: Peak power performance of WPI's design is comparable to that of NXP's design

Analysis of the peak power data suggested that the new design had less peak power capacity compared to NXP's design. This data also indicated that, despite several modifications, the new design still met the 52.7dBm (186W) minimum peak power requirement set by NXP.

The next set of data to be compared will be the IMD performances of the two designs. For this comparison, NXP's standard test procedure was followed. This standard procedure involved two carrier sweeps where one signal generator was fixed at 1960MHz. One sweep involved a second signal generator increasing its frequency from 1960 to 2060MHz while the second sweep had the second signal generator decrease its frequency from 1960 to 1860MHz. The data from the sweeps performed on NXP's design are displayed on the next page.

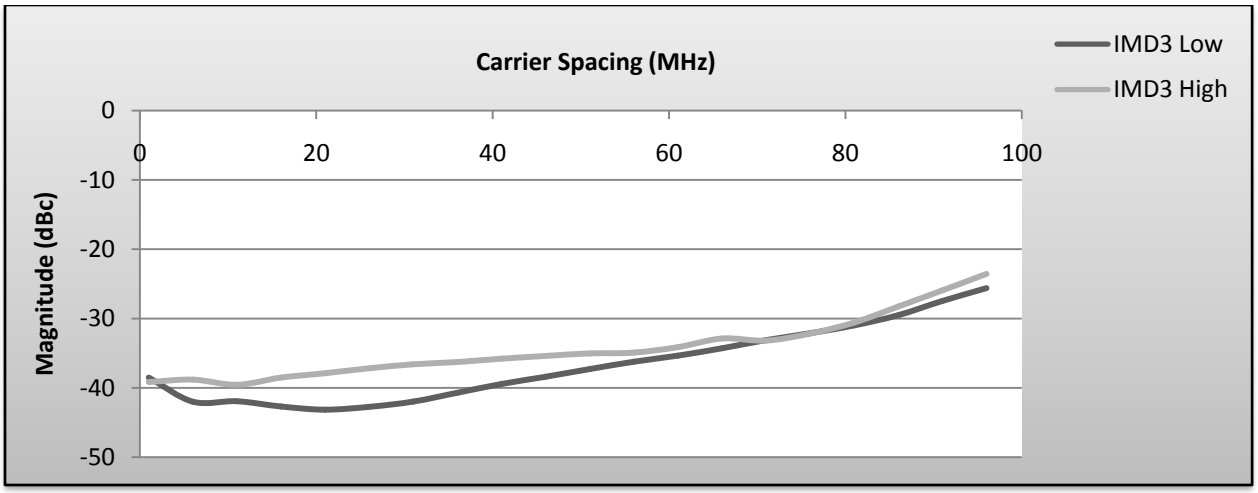


Figure 54: IMD3 performance of NXP's design (carrier sweep from 1960 to 2060MHz)

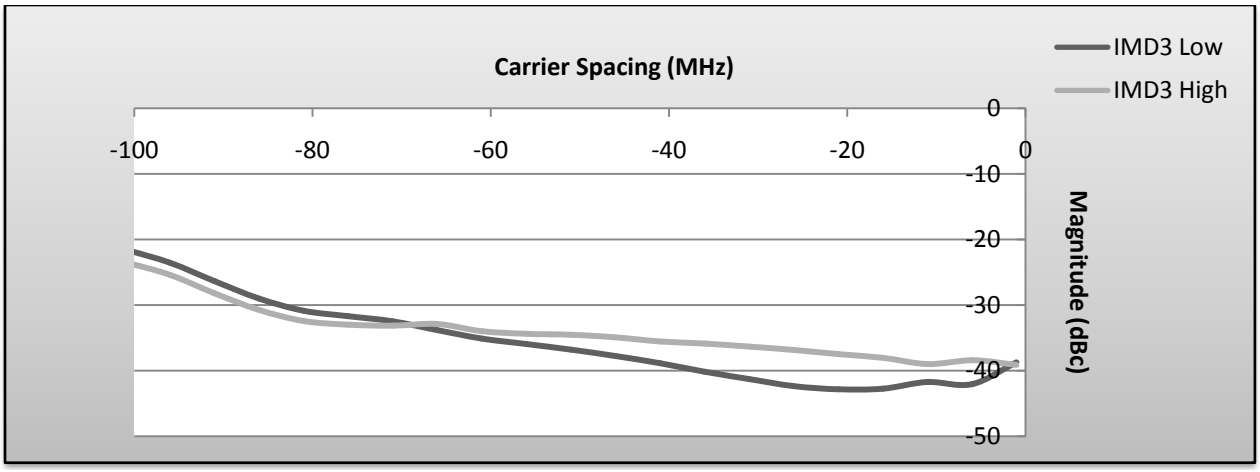


Figure 55: IMD3 performance of NXP's design (carrier sweep from 1960 to 1860MHz)

According to the above figures, NXP's original design exhibited a wide variation in IMD3 magnitude with significant asymmetry when the carrier frequencies are between 10 to 50MHz apart. These results indicate a benchmark maximum carrier spacing of 60MHz. An improved design should exceed this specification while meeting other requirements for peak power, IMD3 variation and IMD3 asymmetry. The graphs on the next page illustrate how successful the project was in achieving these goals.

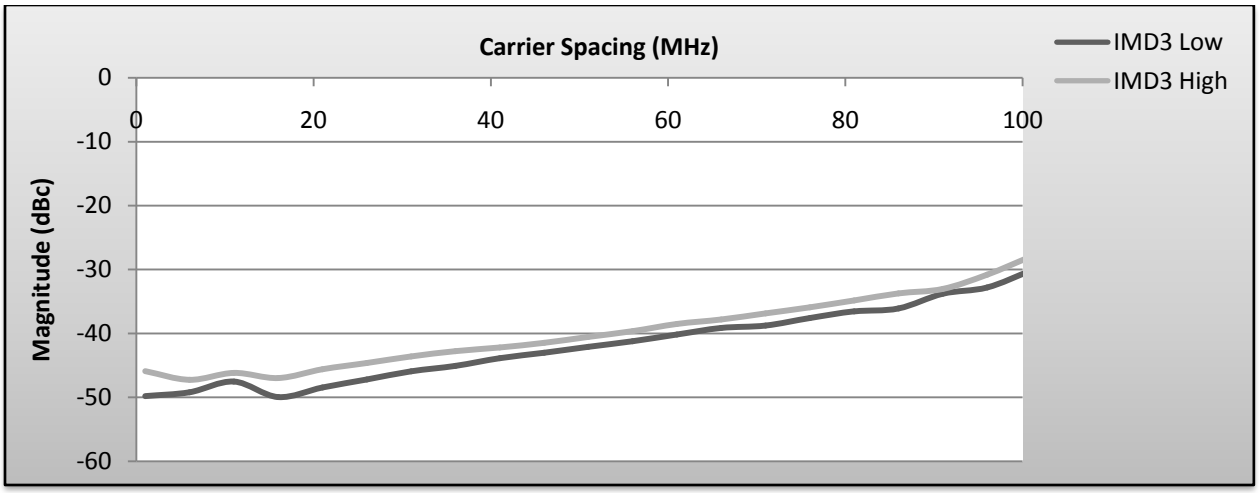


Figure 56: IMD3 performance of WPI's design (carrier sweep from 1960 to 2060MHz)

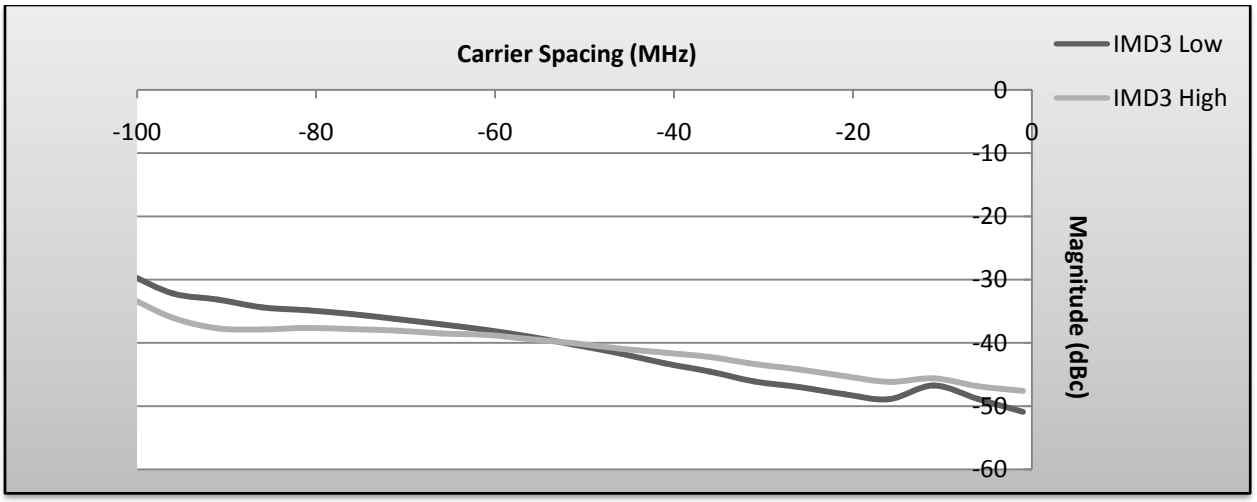


Figure 57: IMD3 performance of WPI's design (carrier sweep from 1960 to 1860MHz)

When compared to NXP's benchmark design, the figures above indicate a significant improvement in IMD3 performance. Both sweeps indicate not only decreased asymmetry but also an increase in maximum carrier spacing to 90MHz! However, IMD3 variation remained a persistent problem throughout the course of the physical implementation phase of the project. Since the variation in IMD3 magnitude is common to both designs, this could indicate a problem within the transistor itself.

Other important performance data were gathered from what is known as a power level sweep. This automated routine recorded and calculated performance data such as drain current, gain and efficiency for different input power levels at 3 different frequencies within the operating spectrum. Since the objective statement specifies a nominal output power level of 45dBm (32W),

this analysis will only consider data collected at that level. The results have further demonstrated the improved performance of new amplifier design, the exception being the design's ACPR (Adjacent Channel Power Ratio) performance. However, the project has been reasonably successful in producing an amplifier design that meets most of NXP's objective specifications. Power level sweep results (for a 1000mA quiescent current) from both NXP's design and WPI's design are presented below for a direct comparison.

Power Level Sweep Results (NXP Design, Idq = 1000mA)							
Freq.(MHz)	Pout (dBm)	Pin (dBm)	Idrain (A)	Power Gain (dB)	Drain Efficiency (%)	ACPR (dBc)	
						at 1.98 MHz	at 885 kHz
1930	45.05	27.92	3.74	17.13	30.58	-62.10	-47.06
1960	45.03	27.80	3.73	17.24	30.56	-62.16	-47.14
1990	45.06	27.65	3.69	17.41	31.07	-61.63	-46.79
Power Level Sweep Results (WPI Design, Idq = 1000mA)							
Freq.(MHz)	Pout (dBm)	Pin (dBm)	Idrain (A)	Power Gain (dB)	Drain Efficiency (%)	ACPR (dBc)	
						at 1.98 MHz	at 885 kHz
1930	45.08	27.19	3.62	17.88	31.81	-62.40	-45.59
1960	45.07	26.93	3.61	18.14	31.77	-62.33	-45.69
1990	45.09	26.96	3.58	18.13	32.21	-61.55	-44.81

Table 4: The project produced a design that offered improved performance

To test the repeatability of these results, the IMD testing procedure used previously was repeated on the same WPI-designed amplifier circuit. The only difference between this repeated test and the previous test was the replacement of the LDMOS transistor with another LDMOS transistor of identical design and construction. The original transistor was marked m0724, indicating that it was manufactured on the 24th week of 2007. The replacement transistor was marked m0749, therefore it was manufactured on the 49th week of 2007. Ideally, there would be no significant change in performance from one transistor to another. However, amplifier performance with the replacement transistor deviated from what was observed previously. Such variation in performance was expected by NXP, but caused alarm among those associated with the project, fearing that this may lessen the practicality of the new circuit. Such deviation in performance can be minimized through further development of the transistor. In any event, the test results from this project have sufficiently proven that it is possible to design a power amplifier for greater video bandwidth with the BLF6G20LS-140 transistor.

6-Recommendations for Improving the Transistor

It was known that the design's performance was limited to the abilities of the transistor used in the amplifier, so one of the more advanced goals of the project was to investigate possible ways in which the LDMOS transistor could be improved. Time was spent on finding ways to improve the transistor while the board was being built. Considering that semiconductor physics was beyond the project's scope, only the transistor's small-signal model was used for improving the transistor. The LDMOS has an internal matching network which consists of bond-wires and tiny capacitors (C2, L2 and L4) in addition to the generic die capacitance (C3). A small capacitance (C1) is also used to model the lead capacitance. The small signal model described above can be seen in Figure 58.

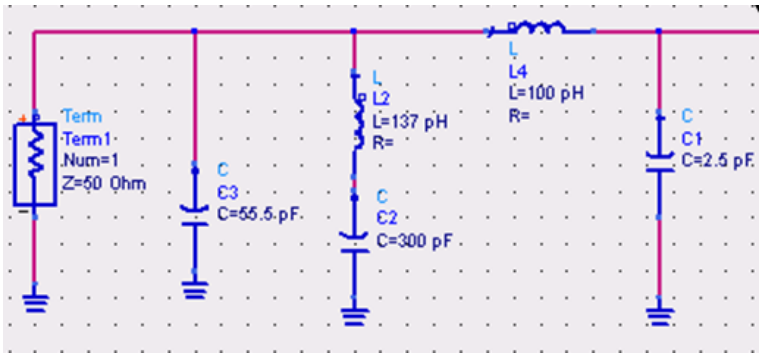


Figure 58: Small signal output model of BLF6G20LS-140

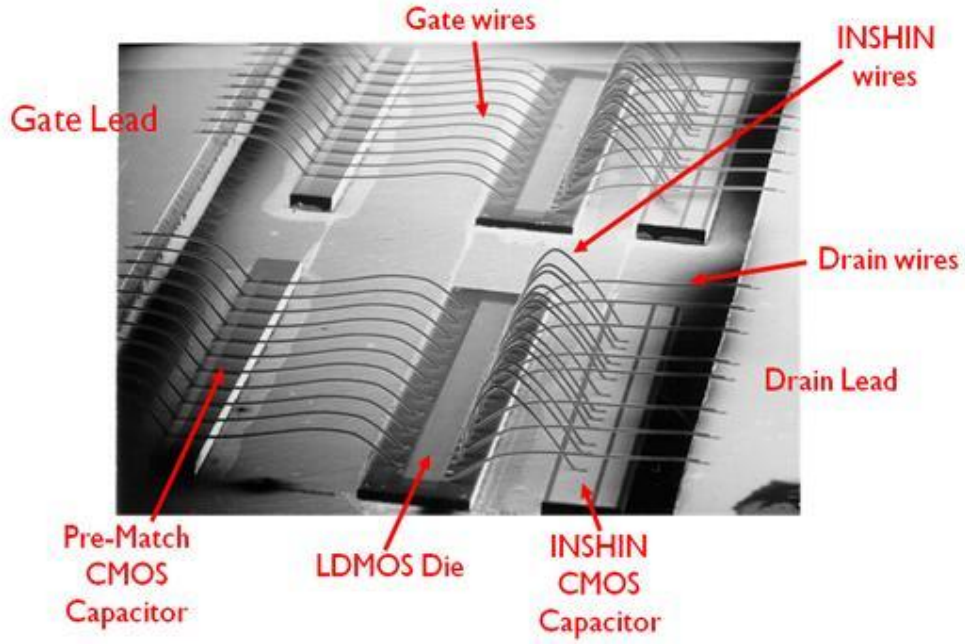


Figure 59: Inside the transistor (courtesy of NXP)

It was known that the VBW performance could be improved by creating a low impedance route to ground in the 1-100MHz range. However any modification to the internal matching network must not diminish the output impedance of the transistor within the 1930-1990 MHz range for matching purposes. The small signal model had a resonance point at around 200 MHz when used in tandem with the decoupling network as illustrated in section 4.3.1. The analysis began by tuning the values in the internal matching network such that peak transistor impedance was minimized. It was concluded that the 300pF capacitor in the middle had a great effect on shifting the resonance point. Capacitances over 20nF could improve the performance greatly. However a capacitor this big would be impossible to fit inside the transistor. This problem could be solved by adding an extra lead to the transistor which would enable the connection of a larger external capacitor. With this in mind, a 100nF capacitor was added in series with an inductor (for blocking desired frequencies) to different points in the small signal model. The most suitable position was right above C2 since other possible locations were on the main power line. The results of this modification can be seen in Figure 61.

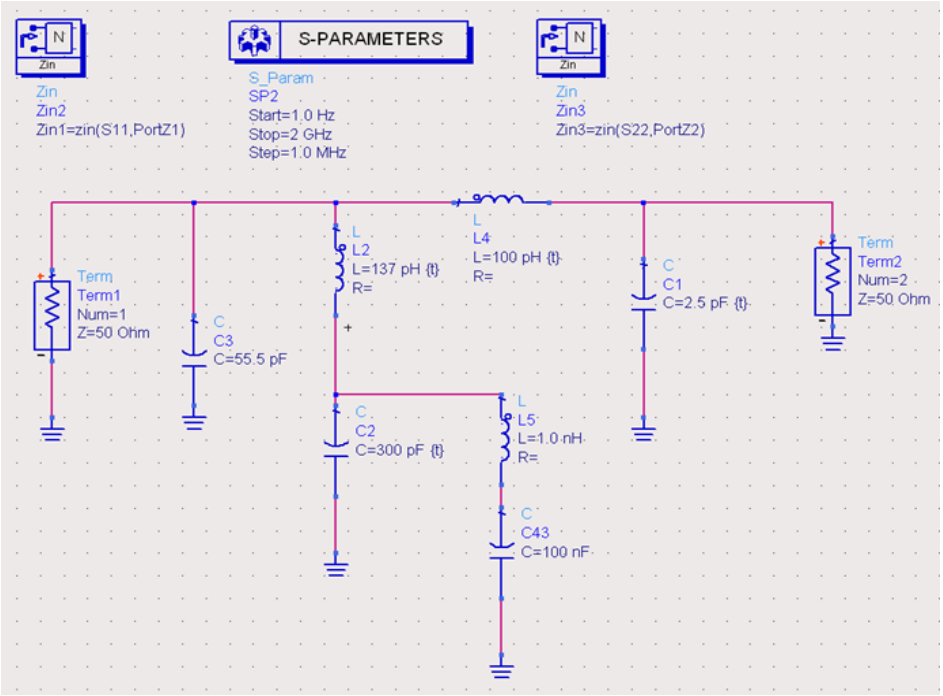


Figure 60: The modification to the transistor

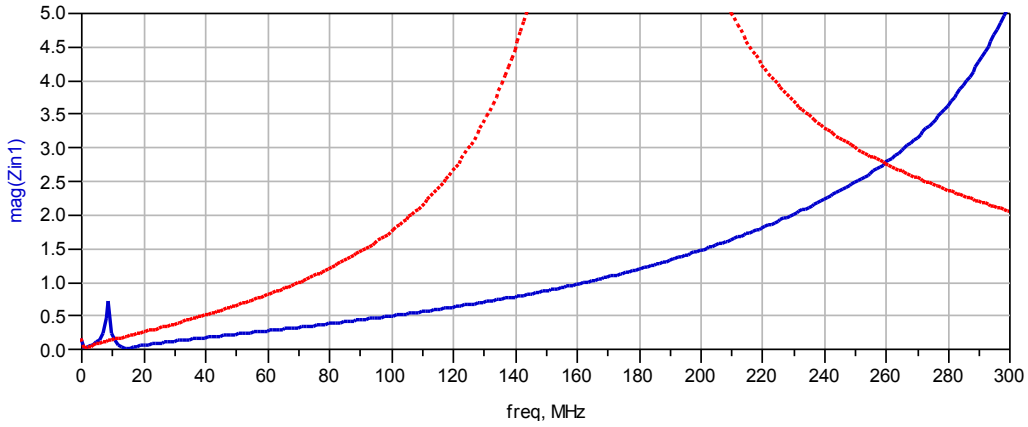


Figure 61: Improved performance of the transistor (in blue)

This model was then refined by adding a transmission line in order to take into account the lead of the transistor, which provided further inductance to the circuit and eliminated the need for an inductor component. This modification was duplicated on the other side in order to maintain symmetry about the drain terminal. Such symmetry was important, as the transistor featured multiple dies and matching networks with leads coming out of both sides of the drain.

7-Safety and Cost Analysis

The beginning stages of the design project required extensive computer simulation and posed little, if any risk to the safety of those involved. However, later project stages required the use of powerful, specialized equipment that could pose a risk of injury should the equipment be used improperly or otherwise abused. Therefore all work conducted at NXP's laboratory facilities conformed to the standards of the Occupational Health and Safety Administration (OSHA), NXP's internal laboratory safety standards and practices, and the operating instructions outlined in the documentation of the laboratory equipment. Conformity to all of these standards ensured minimal risk of personal injury and property damage.

Computer simulation was performed at WPI's Atwater Kent laboratories. This facility featured several Dell Optiplex GX620 computer systems that were purchased at reduced rate from the manufacturer. A similarly-equipped computer setup with monitor, keyboard and mouse can be purchased for around $1,400 (not including utilities such as Microsoft Office and antivirus protection). Licensing for the ADS software used in simulations can be purchased at a rate of $2,500 per year, although this figure can vary depending on the number of different licenses desired.

Travel expenses throughout the project can be calculated as follows: Given an average fuel cost of $2.85 per gallon and an average fuel efficiency of 20 miles per gallon, round-trip travel cost from WPI to NXP's office in Cumberland, RI equaled approximately $9.98 per trip.

Clearly the largest expenses involved with this project came during the physical implementation phase. It should also be noted that the cost to manufacture the layout was approximately $1500 for 12 sets. Heatsinks and board components used in the complete assembly easily exceeded $200 with another $120 for the LDMOS transistor alone. As far as laboratory costs are concerned, NXP's research laboratory maintains a collection of powerful, specialized equipment and test-benches used for the prototyping and construction of various RF circuit designs. To get an appreciation of what this means financially, a network analyzer (of which they have several) can cost anywhere between $15,000-$50,000 for RF applications and upwards of $75,000 for microwave applications. Please note that this is a general cost analysis and that other considerations such as so-called "burden rates" and other indirect costs have not been discussed.

8-Ethics Statement

It should go without saying that through the duration of this project, the design team held themselves to highest degree of professionalism and honesty as outlined by the IEEE Code of Ethics. Examples of these behaviors included:

- Striving to be honest and realistic when reporting test results
- Accepting constructive criticism of their practices when the need arises
- Striving to increase technical competency whenever possible

Compliance with the IEEE Code of Ethics ensured the professional growth of all involved. Most importantly, following this code of conduct ensured that the partnership between WPI and NXP was maintained throughout the course of the project.

9-Conclusion

This document has outlined the knowledge and methods necessary for a successful project in the design of a RF power amplifier. Given design objectives and specifications outlined by NXP, the project was carried out in logical design process that sought to simulate the performance of an amplifier prototype and apply that knowledge toward the development of an improved amplifier design.

The design process began by simulating separate sections of the amplifier's topology and designing them around NXP's transistor model. The first step was to gain familiarity with the transistor through various tests. The active bias network, which supplies the correct voltage to the transistor, was built and simulated in ADS simultaneously. The next step in the project was designing matching networks for the transistor. Several different designs were produced for the input matching network, which promised to give slightly better results according to simulations. However, the original input matching network was retained, considering the risks associated with using a new design and the deviations of simulations from the real world. In the end, this experience was useful for learning about general characteristics of matching networks. The focus of the project was the output side which included the decoupling network. In this phase some changes were made to the decoupling network to lower the IMD3 products and the output matching network was adjusted afterwards to maintain the optimal matching conditions.

Once the design was thoroughly simulated and analyzed, work began on designing, constructing and testing a new amplifier layout that could be further optimized and presented for review by NXP. Initial power tests gave satisfactory results with gain and peak power levels that were well within specification. However, IMD3 performance was lacking and became the main focus of the project. IMD3 effects were minimized through various techniques and design modifications including those made to the active bias network, decoupling network and output matching network. The design process lead to the design of an RF amplifier met most of NXP's expected outcomes.

Appendix

A.1-Objective Specifications

These are the target specifications and respective test conditions that were given by NXP. Some of the technical terms and acronyms are explained on the following page.

BLF6G20LS-140 Compliance Sheet					
Parameter	Note	Min.	Typ.	Max.	Unit
Power Gain	1930-1990MHz	16.5	17.5		dB
Gain flatness	1930-1990MHz		0.1	0.3	dB-pp
Drain Efficiency	1930-1990MHz	30.5	32		%
ACPR @ 885kHz	1930-1990MHz		-45	-43.5	dBc
ACPR @ 1.98MHz	1930-1990MHz		-62	-60	dBc
IRL	1930-1990MHz		-13	-10	dB
Peak Power	With IS-95 1930-1990MHz	52.7	53.0		dBm
IMD3 (VBW)	1930-1990MHz		-35	-33	dBc
IMD3 variation	1930-1990MHz			3	dB
IMD3 asymmetry	1930-1990MHz			3	
Package		SOT502B (Earless – CuCuMoCu – Thin gold on leads)			

Test conditions:

- **V_{DS}=28V**, I_{DQ}=1200mA, T_H=25°C, P_{OUT}=45.5dBm.
- f=1930-1990MHz
- Test signal: IS-95, with Pilot, Paging, Sync and 6 traffic channels (Walsh Codes 8-13) with PAR=9.7dB @ 0.01% probability on the CCDF.
- Channel bandwidth is 1.2288MHz, ACPR measured at 885kHz and 1.98MHz offset, both in 30kHz integration bandwidth.
- Peak power measured with IS-95 signal. IS-95 signal properties: Pilot, paging, sync, 6 traffic channels with Walsh codes 8-13. PAR=9.7dB @ 0.01% probability on the CCDF.
- Peak power is the power where the CCDF is compressed by 3dB. Peak power is P_{OUT}+6.7dB (the 3dB compression of the CCDF).
- *1) Video Bandwidth is recorded with two W-CDMA carriers (TM1, 64DPCH, no clipping) at P_{OUT}=45dBm total up to a maximum carrier spacing of 100MHz. Any other distortion products must be more suppressed than the IMD3 products.

Power Gain: This is the ratio of power output to power input in decibels.

$$PowerGain = 10\log\left(\frac{P_{out}}{P_{in}}\right)\text{dB}$$

Gain Flatness: This is a measure of the fluctuation of the gain throughout the frequency range.

$$GainFlatness = \frac{Max.Gain - Min.Gain}{2} \qquad \text{(H.2)}$$

Drain efficiency: The ratio of RF power output of an amplifier to DC input power.

$$\eta_D = \frac{P_{RFout}}{P_{dc}} = \frac{P_{RFout}}{V_{ds} \cdot I_d}$$

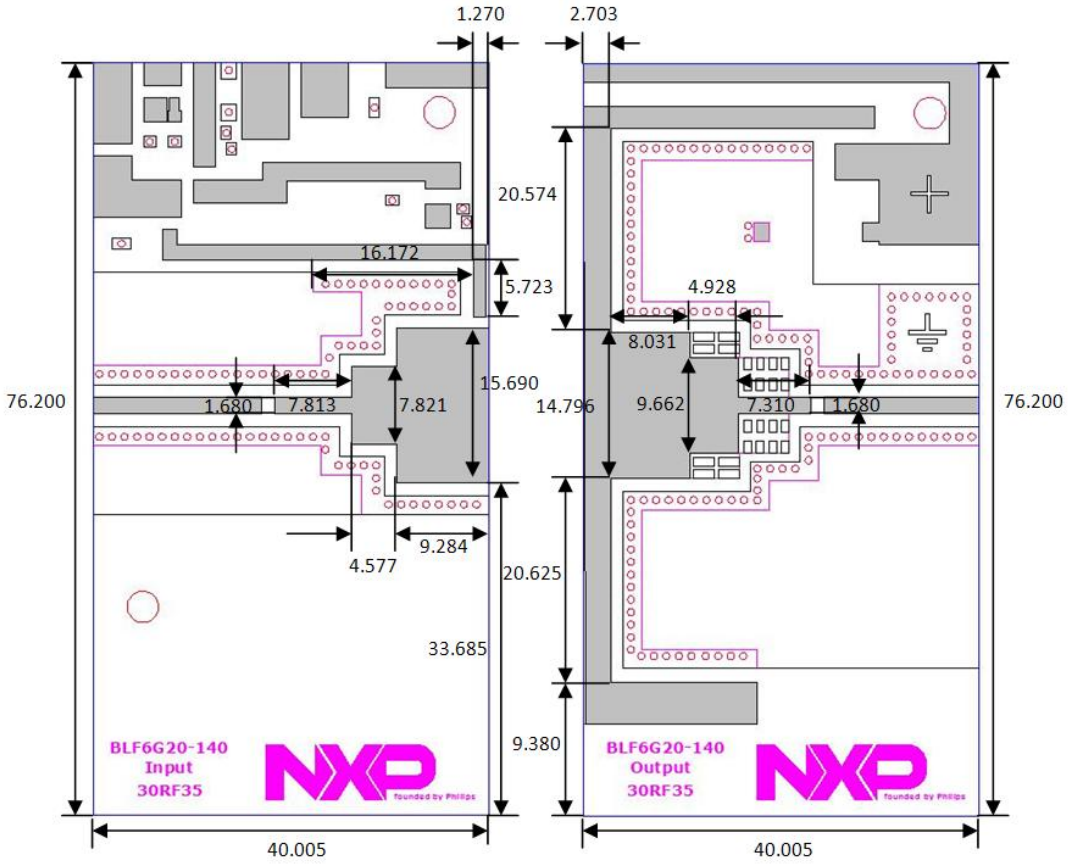
ACPR: Adjacent Channel Power Ratio is the ratio of the power of the wanted signal output to the power of the output at adjacent channels.

IRL: Input return loss is a measure of how much energy is lost as a result of the reflections at the input terminal due to mismatches. It is defined by the formula below:

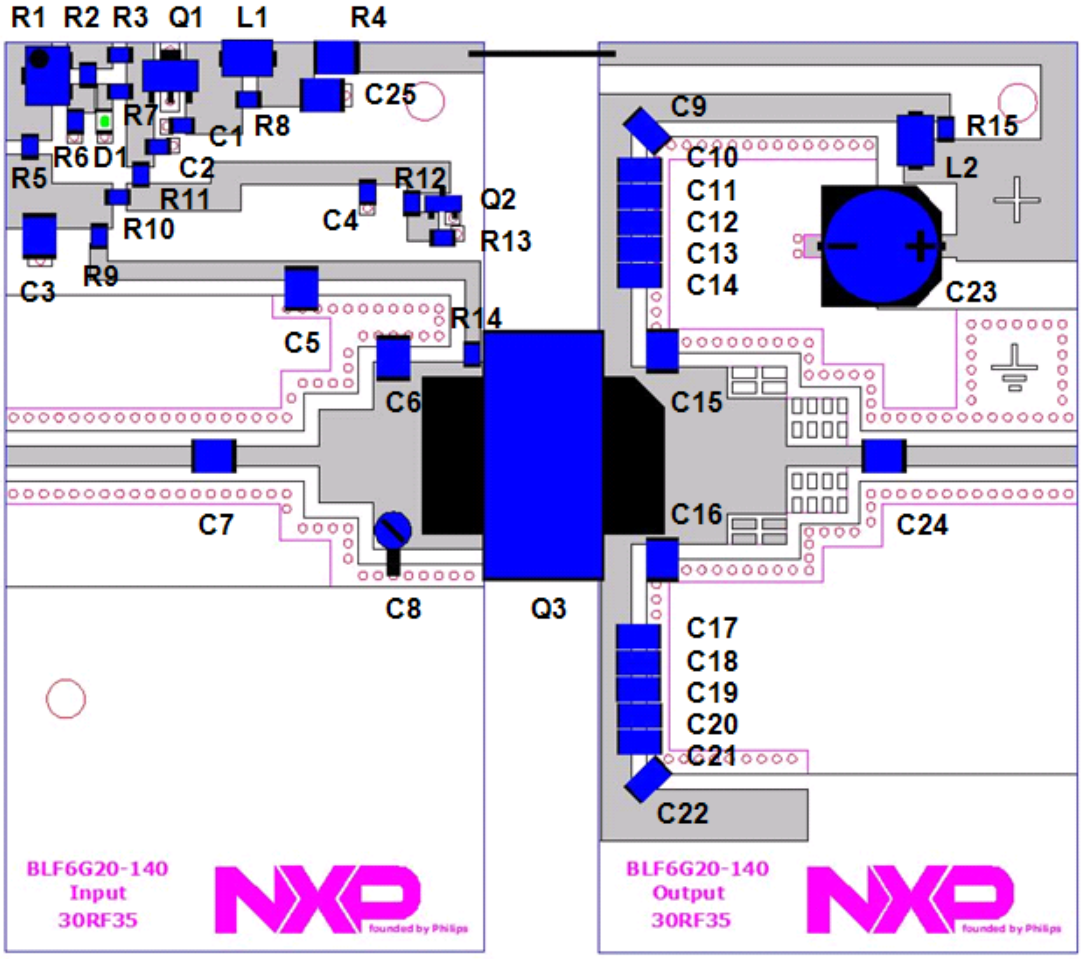
$$IRL = 20\log\left(\frac{SWR}{SWR - 1}\right)\text{dB}\ 7$$

A.2-Final Layout Design Dimensions

The following schematic describes the physical dimensions of the microstrip layout that are vital to maintaining RF performance should the final design be replicated. All dimensions are reported in millimeters.



A.3-Final Layout Design and Components



C1, C2, C4, C13, C14, C17, C18:	0805 100nF
C3, C9, C10, C11, C20, C21, C22:	10µF
C5, C7, C12, C19	ATC 100B150KP 15pF
C6:	1.7pF
C8:	2pF Trimming Capacitor
C15, C16:	ATC 100A2R4CP 2.4pF
C23:	Panasonic EEV-FK1H221P 220µF
C24:	ATC 100B240JP 24pF
C25:	Murata GRM31MR71H105KA88L 1µF
Q1:	SOT89 8V, 100mA 78L08 Voltage Regulator
Q2:	SOT23 NXP PMBT 2N2222 NPN BJT
Q3:	NXP BLF6G20LS-140 LDMOS
L1, L2:	Fair Rite 2743019447 Ferrite Bead

R1:	200Ω Potentiometer
R2, R3:	430Ω
R4:	499Ω, 0.5W
R5:	2kΩ
R6:	75Ω
R7, R11:	1.1kΩ
R8, R14, R15:	9.1Ω
R9:	6.2kΩ
R10:	11kΩ
R12:	5.1kΩ
R13:	910Ω
D1:	0805 Green LED
Substrate:	Taconic RF-35 (30 mils)

*IMPORTANT NOTES:
0805 refers to the package size of a particular component. C6 was a trimming capacitor but was replaced with a fixed capacitor for final testing.

Bibliography

Asbeck, Peter, Steve Cripps, Peter B. Kenington, Zoya B. Popovic, Nick Pothecary, Frederick H. Raab, John F. Sevic, and Nathan O. Sokal. "RF and Microwave Power Amplifier and Transmitter Technologies." *High Frequency Electronics* (May 2003).

Budimirl, D, H. Koulouzisl, and C. Williams. "LDMOS RF Power Amplifiers with Improved IMD Performance" *34th European Microwave Conference - Amsterdam* (2004): 1185

Coleman, Christopher. *An Introduction to Radio Frequency Engineering.* Cambridge University Press, 2004.

Crean, Ed. "RF Power Amplifier Testing." *Evaluation Engineering* (November 2005).

Cripps, Steve. *RF Power Amplifiers for Wireless Communications.* Artech House, Incorporated, 2006.

Advanced Techniques in RF Power Amplifier Design. Artech House, Incorporated, 2002.

Fager, Christian, José Carlos Pedro, Nuno Borges de Carvalho, Herbert Zirath, Fernando Fortes, and Maria João Rosário. "A Comprehensive Analysis of IMD Behavior in RF CMOS Power Amplifiers" *IEEE Journal of Solid-State Circuits* 39, no. 1 (January 2004): 24.

Hanson, Brett, and John Pritiskutch. *Understanding LDMOS Device Fundamentals.* ST Microelectronics, 2000.

Kenington, Peter B. *High Linearity RF Amplifier Design.* Artech House, Incorporated, 2000.

Khanifar, Ahmad. "Introduction to Memory Effects." (2004).

Kim, Jin-pil, Seong-su Park, and Sang-gug Lee. "Linearity Vs. Q-Factor of Loads for RF Amplifiers." *Microwave and Optical Technology Letters* 37, no. 4 (May 20 2003): 286.

Ludwig, Reinhold, and Pavel Bretchko. *RF Circuit Design: Theory and Applications.* Prentice Hall, 2000.

Manninen, Jani P. A., Timo Rahkonen, and Joel H. K. Vuolevi. "Measurement Technique for Characterizing Memory Effects in RF Power Amplifiers." *IEEE Transactions on Microwave Theory and Techniques* 49, no. 8 (August 2001).

Minihold, Roland. *Application Note: Measuring the Nonlinearities of RF Amplifiers using Signal Generators and a Spectrum Analyzer.* Rohde & Schwarz, 2003.

Pedro, Jose, and Nuno Carvalho. *Intermodulation Distortion in Microwave and Wireless Circuits.* Artech House, Incorporated, 2003.

Pozar, David M. *Microwave Engineering.* John Wiley & Sons, 2005.

Taylor, Mark S., William Waung, and Mohsen Bahnan. *Internetwork Mobility: The CDPD Approach.* Prentice Hall Professional Technical Reference, 2000.

Vennema, Korne. *Application Note: MCPA for UMTS using the BLC6G22-100 LDMOS Transistor.* Philips Semiconductors, 2005.

Vuolevi, Joel. "Analysis, Measurement and Cancellation of the Bandwidth and Amplitude Dependence of Intermodulation Distortion in RF Power Amplifiers." University of Oulu, 2001.

"CDMA." [cited 2007]. Available from http://www.telecomspace.com/index.php?q=cdma.html.

"FET Bias Networks." [cited 2007]. Available from http://www.microwaves101.com/encyclopedia/FETs.cfm#FETbiasnetworks.

"How to relate LMOS device parameters to RF performance." [cited 2007]. Available from http://us1.st.com/stonline/products/literature/an/6980.pdf

"Move Over, SCPAs." [cited 2007]. Available from http://telephonyonline.com/wireless/mag/wireless_move_scpas/.

"RF Power Amplifier Design using LDMOS Semiconductors." [cited 2007]. Available from http://www.ieee.li/pdf/viewgraphs_rf_power_amp_ldmos.pdf.

"USA Wireless 3G Market - 2003." in UMTSWorld.com [cited 2007]. Available from http://umtsworld.com/industry/usa.htm.

"Wireless Base Station Technology Evolution." [cited 2007]. Available from http://ieeexplore.ieee.org/iel5/9586/30304/01392468.pdf.

The following materials were provided by NXP Semiconductors and used as reference material throughout the course of the project:

Loadpull Report: *"Loadpull BLC6G20LS-140 Using IS95" (Rev. 0.1 - March 13 2006)*

Preliminary Data Sheet: *"BLF6G20LS-140 UHF Power LDMOS Transistor" (Rev. 00.03 – October 25 2006)*

Report: *"BLF6G20LS-140 Reference Demo; Board 632" (August 1 2007)*