Kodiak Electric Vessel MQP

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Abstract

This project involved the collaboration and improvement of a novel inverter design with the primary aim of use in Alaskan fishing boats. A programmable power converter was designed such that diesel engines in generators could vary their rotational speed based on electrical load. This improves on the widely-adopted generator design, which requires that the engine spin at 1,800 RPM constantly in order to generate 60Hz power. The design that this project elaborates on has been tested and proven to work. The result of this project is a 30%-50% more efficient and expandable model for the inverter.

Acknowledgments

We would like to thank Professor Bitar, our advisor, for his help and guidance with this project. We would also like to thank Father Joshua Resnick and Seraphim McGann, our sponsors, for their help and for allowing us to work on this project.

Abbreviations

BJT Bipolar Junction Transistor

CAD Computer-Aided Design

FPGA Field Programmable Gate Array

GPIC General Purpose Inverter Controller

IGBT Insulated Gate Bipolar Transistor

KEV Kodiak Electric Vessel

MOSFET Metal Oxide Semiconductor Field-Effect Transistor

NI National Instruments

PCB Printed Circuit Board

sbRIO Single-Board Reconfigurable Input/Output

TI Texas Instruments

UMIC Universal Modular Inverter Controller

UPS Uninterruptible Power supply

VSI Voltage-Source Inverter

WPI Worcester Polytechnic Institute

Chapter 1

Introduction

The state of Alaska relies heavily on the fishing industry as a source of income. It is estimated that the Alaskan economy generates $5.8 billion annually from its fishing industries [3]. Alaska also supplies over half of the fish that the US consumes [2]. As such, any changes to the costs of catching fish in Alaska greatly affects the price of fish in the rest of the US.

All fisheries rely on special fishing and/or diving boats to catch fish. These boats use large diesel generators to power spot lights, bilge bumps, and other electrical systems on board. Diesel engines should be run at 60-75% of their maximum rated load otherwise the engine can be damaged. Common problems that occur from running diesel engines under a light load are carbon build up, internal glazing, and poor piston ring-sealing [6]. This means that the fishing boats often run extra electrical equipment in order to load down the diesel generators even if they don't need to use all of the equipment. Another source of wasted fuel is that in order to generate 60Hz AC, the motors are commonly fixed at 1800 or 3600 RPM. Depending on the current load of the system, the optimal speed of the diesel engine varies greatly.

Unfortunately, Alaska consistently has the highest diesel prices than any other west coast state [3]. The high fuel prices coupled with heavily loaded diesel generators means that extra money is spent on fuel. By using an inverter in line with the diesel generators, upwards of 30% could be saved on fuel costs. The generators produce 3-phase power which varies in frequency depending on the RPM the engine is set to. An inverter could convert this 3-phase power, regardless of frequency, into 60Hz AC power for the boats electrical systems.

The Kodiak Electric Vessel company (KeV LLC) is a small startup company in Kodiak, Alaska. The Universal Modular Inverter Controller (UMIC) is an inverter they started designing to increase the efficiency of diesel electric generator systems. A unique capability of the UMIC is that it is scalable. Multiple UMICs can be stacked to handle more power if necessary. This project focuses on improving the design of the controller by creating schematics, PCB layouts, and testing certain key components of the design. Where this project leaves off is where KeV plans to pick up and make it marketable to the fishing industry.

Chapter 2

Background

2.1 Kodiak Island and Alaska

2.1.1 Alaska

The Kodiak Electric Vessel (KEV) project is a unique project taking place in a unique location. The KEV project is being primarily researched and funded through our project sponsors, Joshua Resnick and Seraphim McGann, on Kodiak Island in Alaska. The project location greatly defines the specifications that must be met and adds great meaning to the inverter project. Due to the remoteness and weather in Alaska, technologies must be created and designed to be long lasting and efficient because of the lack of freely available resources, such as diesel fuel. The more efficient a technology, the more useful and reliable it can be for the user in Alaska. In this section, the unique location and characteristics of Alaska and Kodiak Island will be discussed.

The state of Alaska officially became part of the United States in January 1959, as the 49th state. The territory was purchased from the Russians in the 19th century, and has been a hub for Russian, American, and Native American cultures ever since [5]. The Alaskan economy is dominated by oil, natural gas and fishing. The state is the largest state in the United States by area, but the 4th least populous (ranking at 47th) and also the least densely populated in the United States. On average, there are about 1.26 people per square mile [9]. Below in Figure 2.1, Alaska is shown, note its remote location and size.

Because of its location, land area and population density, resources and costs of living are higher priced. In the more remote areas of Alaska, outside of main cities, residents must conserve what they have and be efficient in their daily lives. The purpose of the KEV inverter project is to enable more efficient usage of electric vehicle on-board generators for electricity as well as propulsion, in order to save money and resources. The primary application of this project will be used to complement on-board generators on commercial fishing vessels.

2.1.2 History of Alaska

Alaska has been part of the United States since 1959 but has been home to indigenous tribes for thousands of years before the arrival of Europeans [5]. The natural resources of Alaska have always been used as means for survival, and Alaska supplies many resources, such as oil, natural gas and seafood, to the rest of the United States. The first permanent European settlements were founded in the late 1700s, and Alaska has been a source of natural resources since [5].

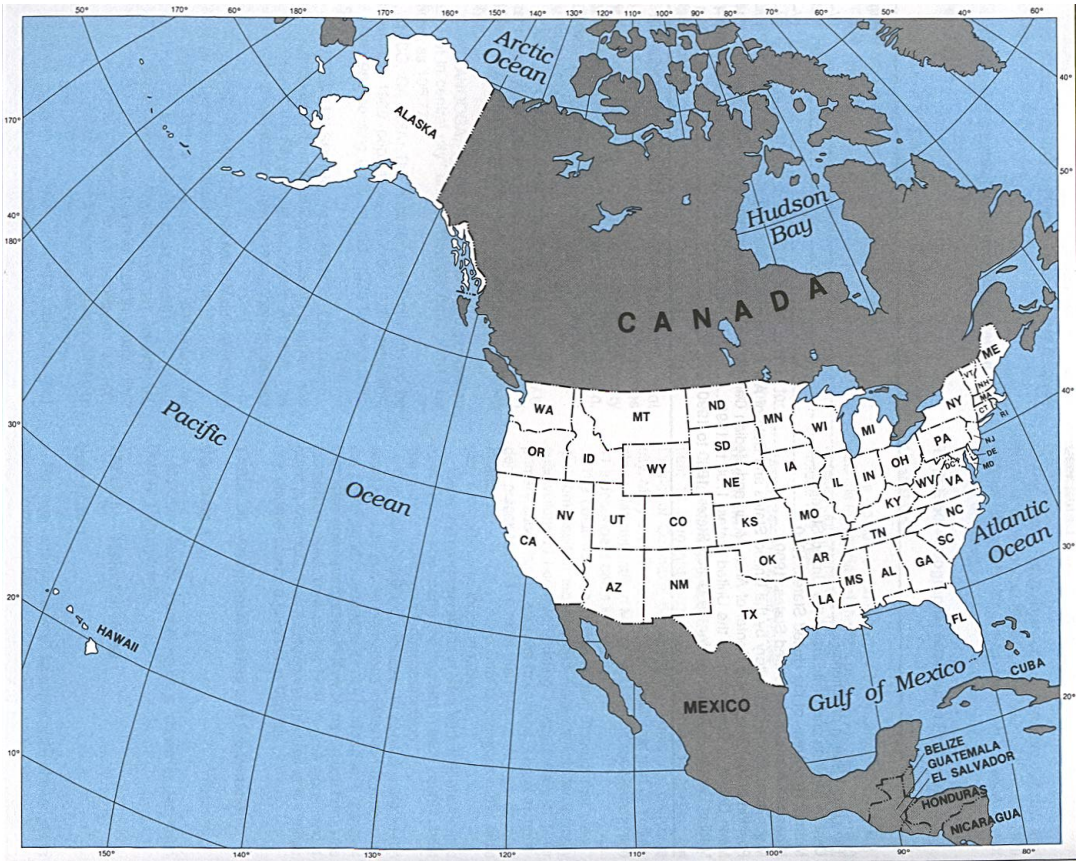


Figure 2.1: Map of North America

2.1.3 Alaskan Climate

The climate of Alaska differs greatly depending on the location of the state. Because it is such a large state, there are several different climate zones which effect lifestyles accordingly. This project is based on Kodiak Island, shown in Figure 2.2 below. This puts Kodiak Island in the "maritime" climate region, although commercial fishermen would be prone to the climate in nearly all of these regions.

In northern Alaska, the winters are very long and cold, with very short, cool summers. In July, the average low temperature is only 34 degrees Fahrenheit. In western Alaska, the "Transitional" region, there are extreme varieties in precipitation, ranging anywhere from 10 to 100 inches of precipitation each year. Finally, the interior of Alaska is subarctic. Both the highest and lowest recorded temperatures in Alaska have been recorded in the interior of the state. The summers sometimes reach as high as 90 degrees Fahrenheit, while the winters can fall below -60 degrees Fahrenheit [1].

The capital city, Anchorage, as well as Kodiak Island, are located in southern Alaska. The weather is very dependent on the coast in that region. It is a subarctic climate, with little rain, but large amounts of snow accumulation each year [1]. Projects in this environment, including the KEV project, will have to be able to adapt and incorporate these drastic climate ranges.

2.1.4 Kodiak Island

The Kodiak Electric Vessel project is based in Kodiak Island, Alaska (highlighted in Figure 2.3). Kodiak Island is an island off the south coast of the state. It is the second largest island

Figure 2.2: Climate Regions of Alaska

in the United States and is heavily forested and mountainous [8]. There are seven different communities that make up the Island, with the main city being Kodiak. To gain access to the island, one must take a boat or fly in to Kodiak's airport.

Since being purchased by the United States in 1867, Kodiak Island has become a center for commercial fishing. Kodiak Island is a boating community and many things revolve around this industry. Fishermen, boat mechanics, and many other fishing related professionals live on the island. The largest U.S. Coast Guard base in the United States also resides on Kodiak Island, further proving the need for such a KEV inverter project. The base is known as "Coast Guard Base Kodiak" and holds many other defense units, such as the "Integrated Support Command Kodiak", "Air Station Kodiak", "Communications Station Kodiak", and "Aids to Navigation Station Kodiak". There are about 400 combined officers and enlisted personnel who help operate the base. Their primary role is aerial search and rescue missions throughout Alaska [4].

Kodiak Island has long and cold winters and mild summers with heavy precipitation throughout the year. Throughout this report, we will see how all of the aspects and characteristics of Alaska and Kodiak Island go into the engineering decisions of the KEV inverter project.

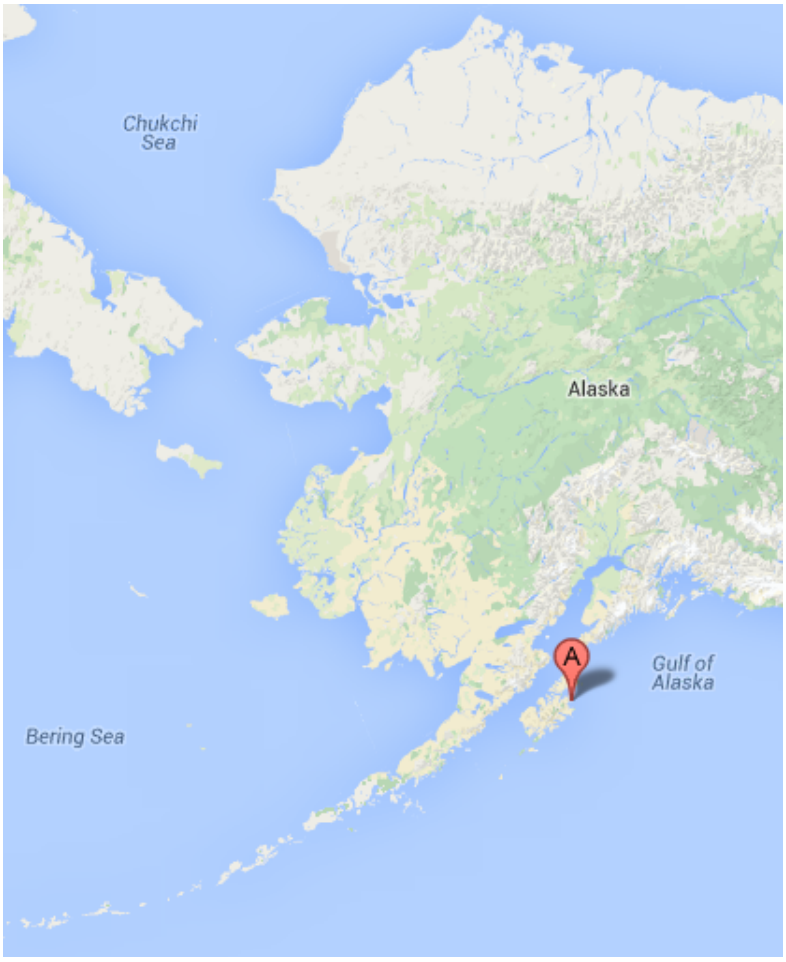


Figure 2.3: Map of Alaska, with Kodiak Island

2.2 Power Devices

2.2.1 Inverters

An inverter is an electronic device or circuitry that changes direct current (DC) to alternating current (AC) [10]. The opposite of inverters are rectifiers which convert AC power to DC. Inverters are used in a wide variety of applications such as power generation (solar panel arrays), frequency control (induction heating), power grid applications (high voltage DC transmission and grid-tied inverters), uninterruptible power supply (UPS) systems, and electric motor speed control for any application with electric motors.

This project uses inverters for electric motor speed control. A standard generator must operate at a fixed RPM in order to output 60Hz power. However, the most efficient operating RPM varies according to the load on the generator. This load/RPM mismatch causes standard diesel generators to waste between 30% - 50% of their fuel due to operational inefficiency [12].

This problem is circumvented with the use of power inverters. A UMIC Controller (Universal Modular Inverter Controller) is placed between the generator and the load. Load matching and efficient operation can now occur as the inverter can output consistent 60Hz power while the generator runs in the most efficient region on its fuel consumption map for any given load. Decoupling the load from the generator means additional energy conversions via the UMIC and a slight loss of power in each conversion. However, these losses are completely offset the by

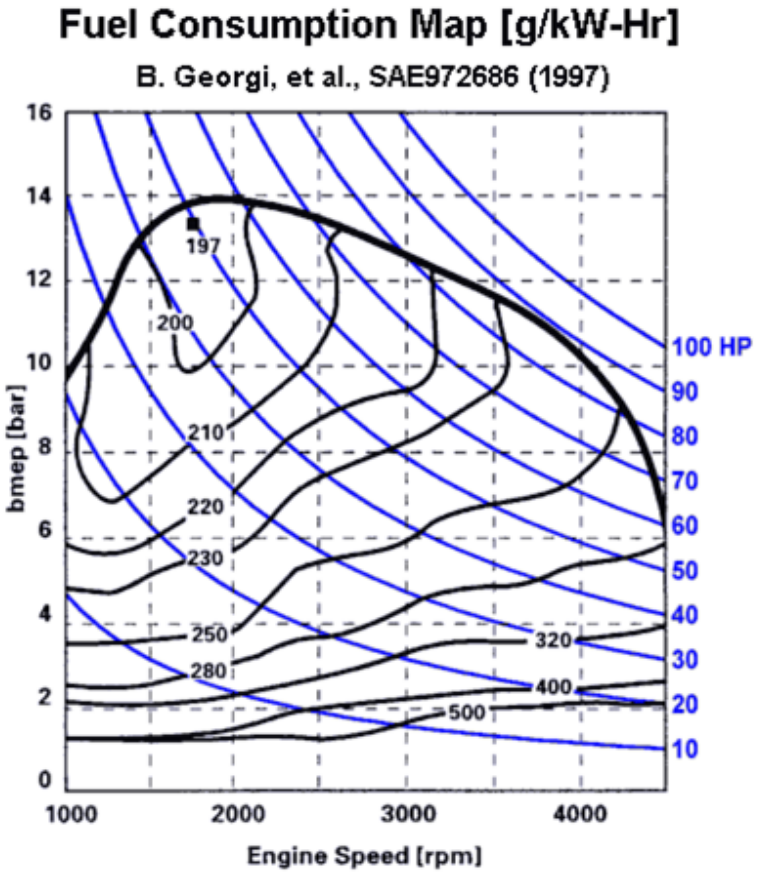


Figure 2.4: Diesel Efficiency Map

fuel savings associated with the motor operating at the most efficient speed and led to a total efficiency improvement by as much as 30% according to KeV, from the preliminary results of TRL-6.

2.2.2 Genset

A genset is a diesel engine and an electric generator otherwise known as a diesel-electric generator. Gensets are used to provide power to marine vessels and other independent electrical networks. Drawbacks of typical gensets are that they are large, requiring lots of boat real estate, exposed to corrosion, prone to multiple types of failure, difficult to service/replace, and expensive. This project replaces the typical genset with a Power Dense Motor (PDM). Advantages of PDMs over typical diesel-electric generators are: there is no exciter stage and thus they are much smaller; it is a protected, sealed, and oil cooled unit; and they have no rotating winding or diodes and are less prone to these types of failures. Figure 2.5 shows the location of the PDM within the system.

2.2.3 Storage Devices

Batteries have become an everyday part of life. We rely on them to power the numerous electrical devices we use every day. For this reason, when someone says the term 'energy storage', batteries are what most often comes to mind, but there are a variety of energy storage devices available each with their own advantages, applications and limitations, shown in Figures 2.6 and 2.7.

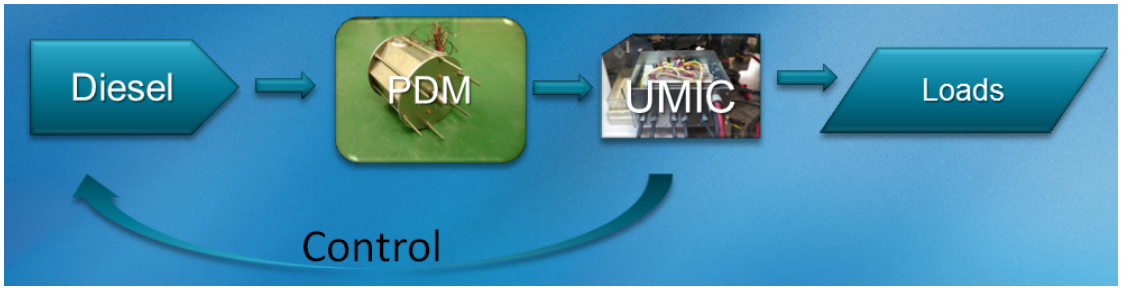


Figure 2.5: Control Flow Diagram

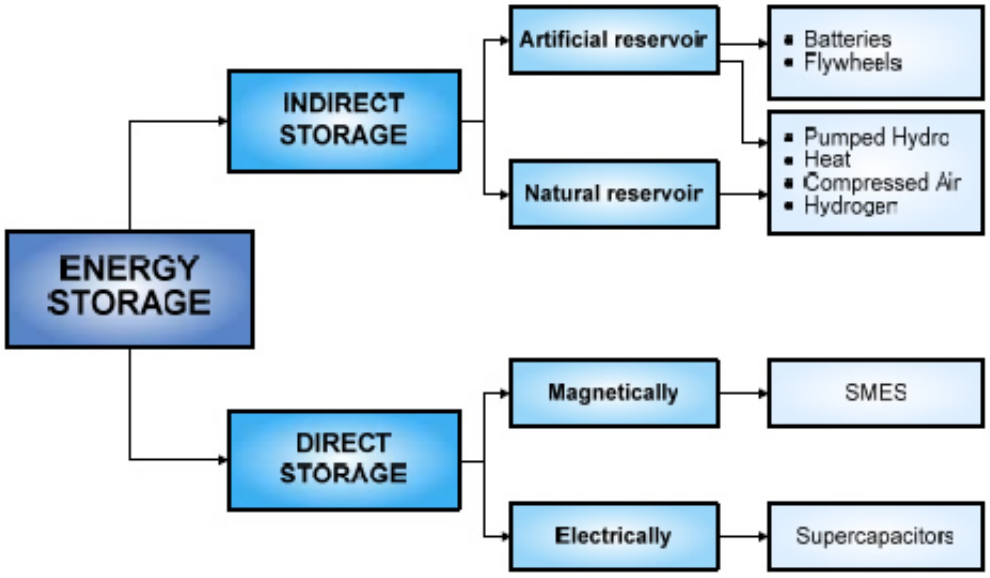


Figure 2.6: Tree Diagram of Energy Storage options

In many electronic applications, capacitors are becoming the energy storage avenue of choice. Particularly, capacitors outperform other storage methods in applications that require high power density without necessarily needing high energy density.

2.2.4 Insulated Gate Bipolar Transistor

An Insulated Gate Bipolar Transistor (IGBT) is a three terminal semiconductor power device. Introduced in the 1980s, it is mostly used in switching applications due to its high efficiency and fast switching speeds. An IGBT is a four layer device that combines the input characteristics typical of MOSFETs with the output characteristics of BJTs. This gives the IGBT a very high voltage rating with a low voltage drop per unit area. The circuit symbol and its equivalent are show in Figure 2.8 [11]. IGBTs have an I-V characteristic quite similar to those of the BJT. They differ in that the controlling parameter is the gate-source voltage for the IGBT while the BJT is controlled via the input current. These characteristics have made IGBTs the device of choice for most modern high-power switching applications.

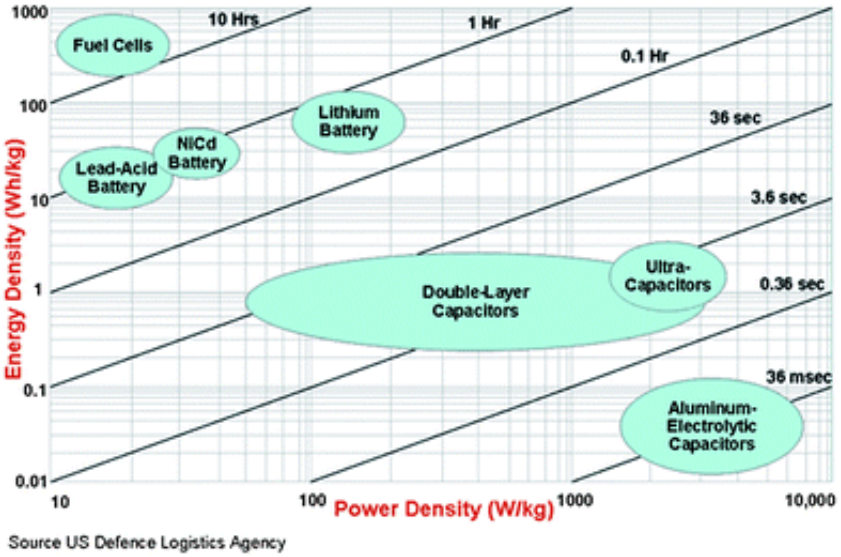


Figure 2.7: Ragone Chart comparing storage devices

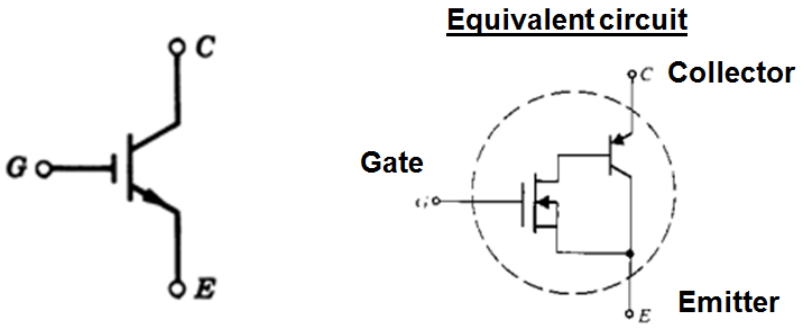


Figure 2.8: IGBT circuit symbol

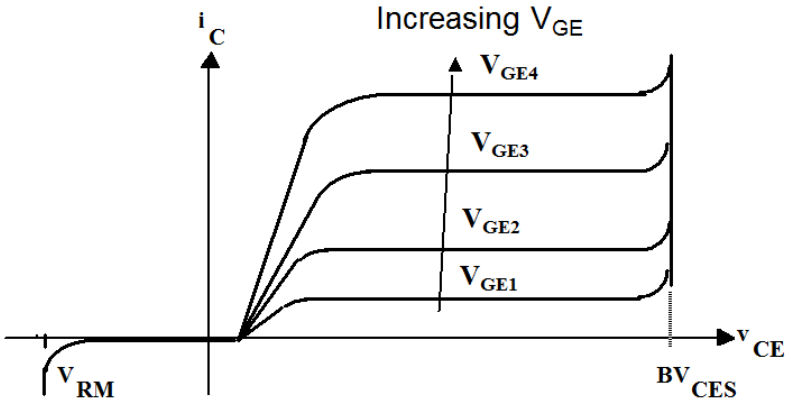


Figure 2.9: IGBT I-V characteristic

Chapter 3

Problem Statement

As shown in the Background section of the paper, a large number of Alaskans depend on the fishing industry for their income and way of life. In addition, the largest United States Coast Guard bases are located in Alaska. Many Alaskans depend on boats and industrial fishing vessels which have been shown to be quite inefficient. With more efficient vessels, Alaskans will be able to save money on fuel, lower their operational costs, and decrease harmful fossil fuel emissions. This would allow for Alaskans to take home more income while reducing the chance of breakdown in generators.

The goal of this project is to create a scalable modular power inverter that is able to control any existing diesel generator system to supply any type of electrical load. This power inverter must maintain 60Hz power while varying the rotations per minute (RPM) of the generator to match the power load. Generators normally operate at a set RPM which may or may not be their most efficient operational point. The usage of this power inverter will allow the generator to operate at variable RPM while continuously storing/discharging energy to supply the load. The inverter cost must be low so the typical Alaskan would be able to afford it and be able to make their money back in a reasonable amount of time. Lastly, this inverter must be able to convert any combination of DC and AC.

This inverter uses multiple printed circuit boards within a sealed enclosure. In addition, the inverter will be expandable through multiple layers in order to handle larger amounts of power and larger, more complex electrical systems. This MQP project focuses on the design, development, and testing of several of the boards needed for the larger inverter project. These boards are as follows:

- IGBT Platform Board
- Voltage Sensing Board
- Current Sensing Board
- Pre-charge Circuit

These boards are discussed in the following sections of the paper. Through the time of our project, several new boards were created in order to fit new constraints. The following boards need to be developed further:

- Status Board
- IGBT Driver Board

In order to complete this inverter project, more design, development, and testing must be done. The remaining objectives for this project include developing the Status and IGBT Driver boards. After these boards are completed, the entire inverter must be tested as a single unit. Testing has been done for several of the boards individually, but all of the boards must operate together.

Chapter 4

Methodology

Since a part of this project was pre-existing, the report will detail the current implementation in Section 4.1 and the project's changes in Section 4.2.

4.1 Original Implementation

At the beginning of the project, the KeV inverter topology looked very different than it currently does. The original design used only one National Instruments Single-Board Reconfigurable Input/Output (sbRIO) 9606 board, which was meant to control all layers of the inverter. It also used NI's General Purpose Inverter Controller (GPIC), which was a large riser board for the sbRIO 9606 that provided a limited amount of I/O and other functionality that was unneeded by our inverter design.

4.2 Proposed Implementation

Over the course of the project, the group has made many changes to the proposed implementation of the new design. We recommend the replacement of the GPIC with a custom Printed Circuit Board (PCB) that would be more tailored to suit the needs of the design. We worked with the KEV team to design such a board. The design evolved into a system using several linked PCBs that are custom-fit to a sealed enclosure that will house the inverter. Due to the movement towards a sealed black-box system for each inverter layer, the design was changed so that each layer would have its own sbRIO. This introduced the complexity of allowing each layer to communicate and share high-speed data between the FPGAs on the sbRIO devices. To mitigate this need, we developed an isolated parallel data bus that could link the different layers together.

4.2.1 Sealed Enclosure

This system is designed to be operated in harsh marine environments. Since it contains many sensitive electronic components, there is a need for a dust- and water-proof enclosure to house the inverter. KeV has designed such an enclosure, to be milled out of steel. A CAD model of the enclosure is shown in Figure 4.1.

This enclosure represents one "layer" of the inverter. Layers can be stacked using the connectors shown on the top and bottom of each one. As mentioned in the next section, each layer is independently operable due to a distributed control topology.

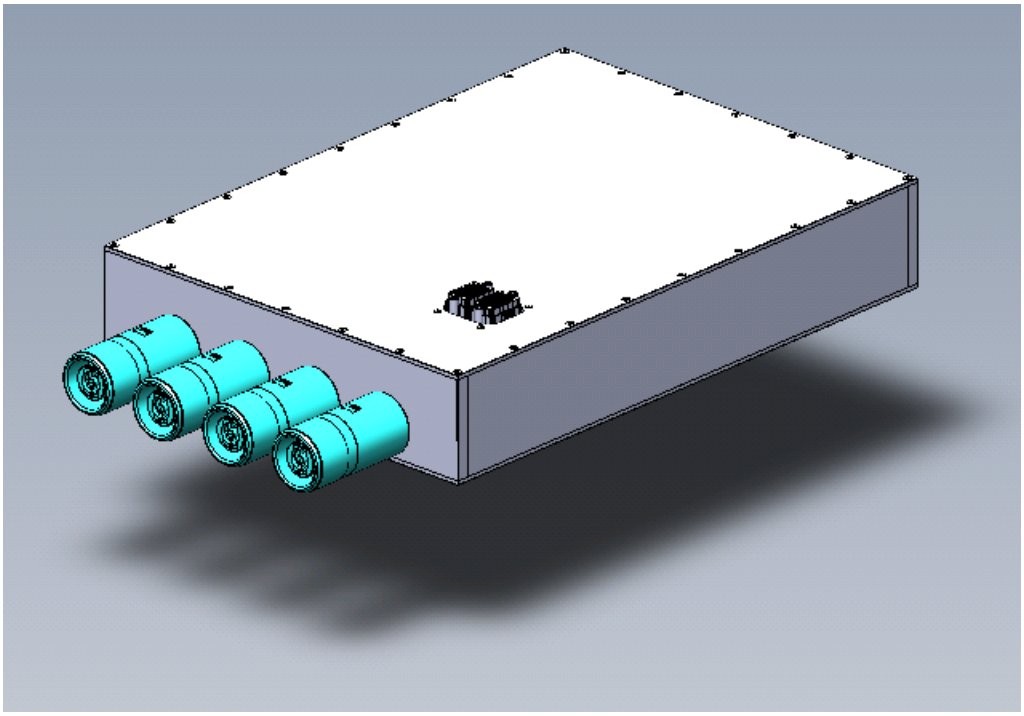


Figure 4.1: CAD Model of Sealed Enclosure

4.2.2 Distributed Layout

Initially, the system was formed around a single FPGA. This required routing high-speed buses along PCB traces and placed a high computational load on the FPGA. The load has therefore been distributed across the layers. In addition to allowing more powerful computation on the FPGA, it allows for a much larger number of layers than were previously possible. This allows KeV to build more powerful and larger inverters. We put an sbRIO 9606 on each layer instead of one centralized unit. This also reduces the number of high-speed pins that must be run between the layers. It does, however, introduce additional complexity as a result of keeping many sbRIO devices in sync and allowing them to share data quickly and efficiently.

4.2.3 Direct-to-Digital Conversion

In the initial design, analog signal lines from the sensors were run back to the GPIC before they were converted into digital signals. In addition, not all of the sensors had a differential output so the signals would be subject to large amounts of interference without additional hardware. We suggested converting the signal to a digital one as physically close to the sensor as possible. This conversion, coupled with differential digital signaling, means we are able to run the signal lines near power without worrying about interference or signal degradation due on the trace path (to a certain extent).

For these conversions we chose the ADS85364 converter from Texas Instruments. The datasheet for this component can be found in Appendix B. This ADC features 6 differential inputs, and has a throughput of 4µs per channel. This allows it to sample at 250kSPS at 16-bit resolution. A high sampling rate is necessary to make precise adjustments to the regulation of the system to ensure peak efficiency.

4.2.4 AD/DC Sensor Boards

Since the start of the project, the AC/DC Sensor boards have remained largely the same. One of the only changes was with the "sensor mezzanine" boards The originally designed inverter included a separate location for "sensor mezzanines". These mezzanines were separate boards that were able to attach and detach from the board, allowing the customer to measure and keep track of several currents in the system, according to the needs of the customer. This board was to consist of a TAMURA current sensor, the necessary resistors for this current sensor (see data sheet in Appendix B), and connections to the Current Sensing Board. These current sensors were going to be directly attached to the mezzanine boards, which would then plug into the inverter.

Chapter 5

Design Description

The full scope of the Universal Modular Inverter Controller (UMIC) design is broken out into a block diagram in Appendix C. No block has been fully designed yet, but a lot of progress was made designing sub-components of all of the blocks. The DC current sensor, AC voltage sensor, capacitor pre-charger, backplane and general differential signal routing have all been completed. More work needs to be done designing the Ethernet power display board, Rogowski coil circuit, and IGBT driver link board.

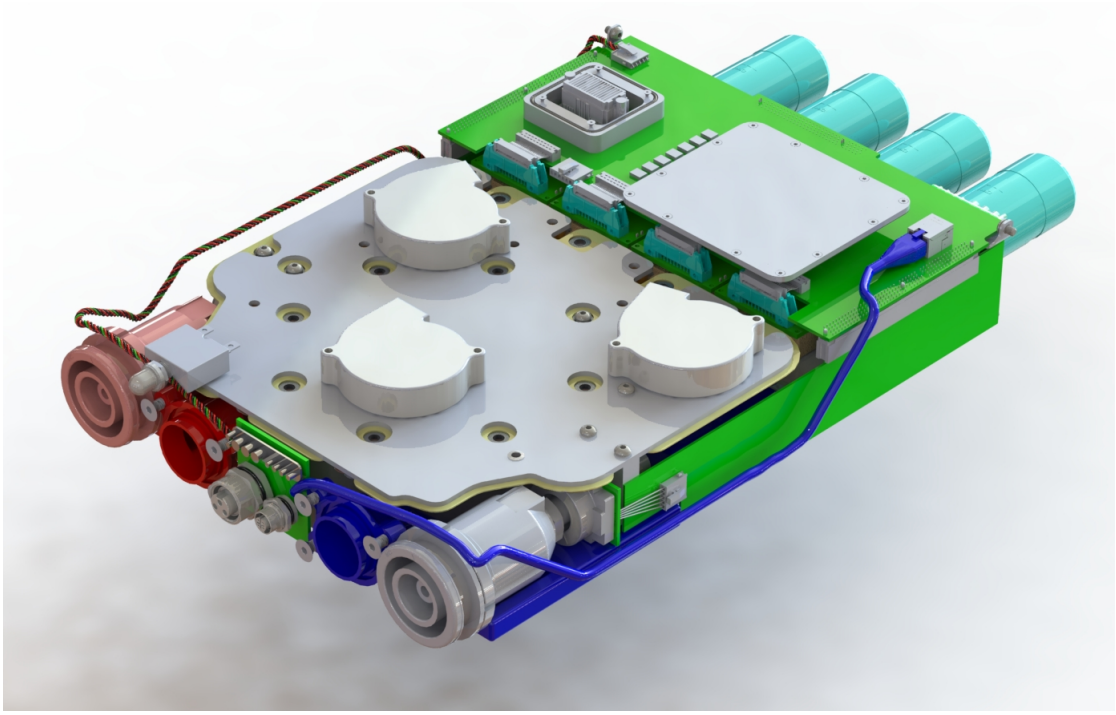


Figure 5.1: 3D rendering of the inverter without the enclosure

5.1 Voltage Sensing Board

As part of the inverter functionality, it is necessary to constantly monitor and adjust settings in order to continue the most efficient operation. In order to control a generator load and be a diverse, flexible inverter controller, the device must monitor several key characteristics of the system. According to the specifications of the project, the UMIC, will be placed between the

generators (on a commercial fishing vessel) and the load. The UMIC will allow the generator to supply 60Hz of power, while varying the engine RPM in order to become more fuel efficient.

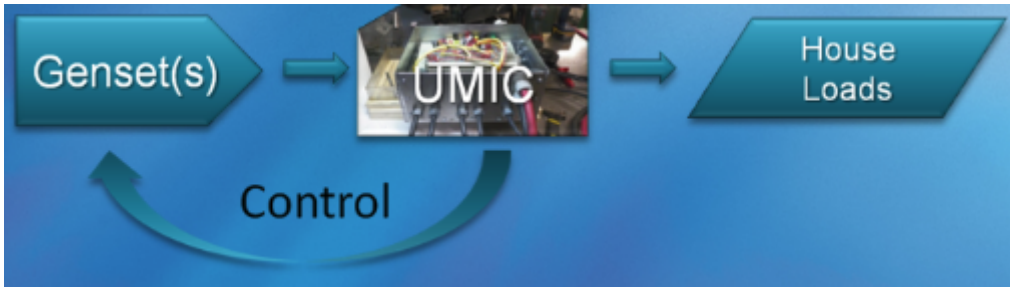


Figure 5.2: Layout of Inverter

In order to properly control the generators, the UMIC must know what is happening in the entire system. The two more important values that must be monitored in the system are voltage and current, thus the total power can also be calculated and measured. Each UMIC will be able to handle and constantly monitor up to 600kW of continuous three-phase power. With such high power levels, monitoring the system is of the utmost of importance. This section will describe the circuit board that will measure the voltage levels and pass that signal on to the rest of the board so it can be properly interpreted.

5.1.1 Schematic of Voltage Sensing Board

As previously discussed, this circuit board will be responsible for monitoring the voltage levels of the system. This board will be identically replicated four times. The same board will be used in order to monitor the voltage between phase A and B, V_{AB}, the voltage between phase B and C, V_{BC}, the voltage between phase C and neutral (N), V_{CN}, and the DC voltage. The layout of the sensing boards are shown below in Figure 5.3.

These sensing boards (the voltage sensing board and current sensing board) are responsible for isolating the appropriate signals, translating that signal into a scaled output, and passing that output to the interpreting board (FPGA). In the figure above, you can see the high speed differential Analog to Digital converters which will convert the analog signal provided by the sensor boards to a digital signal which the interpreting boards can then analyze. These sensing boards are labeled as “Powerstage” boards and at the lowest level of the inverter. The schematic of the circuit is shown below.

Input Voltages

The input voltages to the voltage sensing board will be taken directly from the generator and its conductors. Each phase of the AC components will have a sensing board associated with it so that each of the three phase-to-phase voltages can be measured and accounted for. These sensing boards will be responsible for measuring the voltage between phase A and B, V_{AB}, the voltage between phase B and C, V_{BC}, the voltage between phase C and neutral (N), V_{CN}, and the DC voltage. The AC voltages should be around 385 V_{PP} while the DC voltages may occasionally reach up to 900V on the DC link capacitor. The voltage sensing boards must be able to deal with this range because the UMIC needs to be flexible and able to be used on many different systems with different electrical needs. One important aspect of this board is that the input voltage and the secondary voltages must remain isolated at all times for safety and reliability, which will be accomplished using the AVAGO Opto-Isolator. However, before

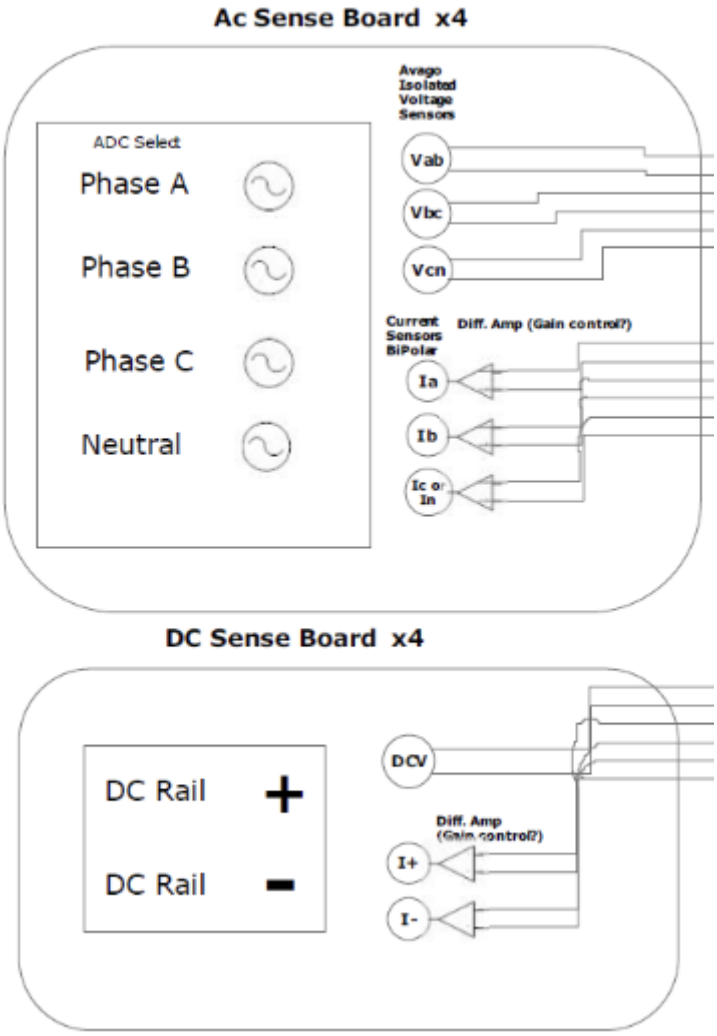


Figure 5.3: Layout diagram of AC/DC sensing boards

this high voltages can be analyzed and electrically isolated, they must be scaled down using a voltage divider.

The voltage divider used in the circuit is a simple device which consists of two resistors. Because the voltage levels are rather high and based on the needs of the AVAGO Opto-Isolator, the voltages must be scaled down. The amount that the voltage is scaled down depends on the ratio of the resistors in series in the voltage divider. The schematic shows a 1MΩ resistor and a 1500Ω resistor in series. In the designed circuit, these resistor values will certainly change. For example, in the prototype circuit, a resistor value of 51kΩ with the potentiometer was used. With this ratio, the voltage input to the AVAGO chip is roughly 10% of the input voltage. The resulting output voltage of a voltage divider can be mathematically expressed using the following Equation 5.1.

$$V_{out} = \frac{R_2}{R_1 + R_2} * V_{in} \tag{5.1}$$

Each of the above variables is explained in Figure 5.5

Based on the needs of the customer and their electrical system, these resistor value can be changed. The customer will need to know what voltage levels their system is operating at and use resistor values that can convert to the ±200mV recommended input for the AVAGO Opto-

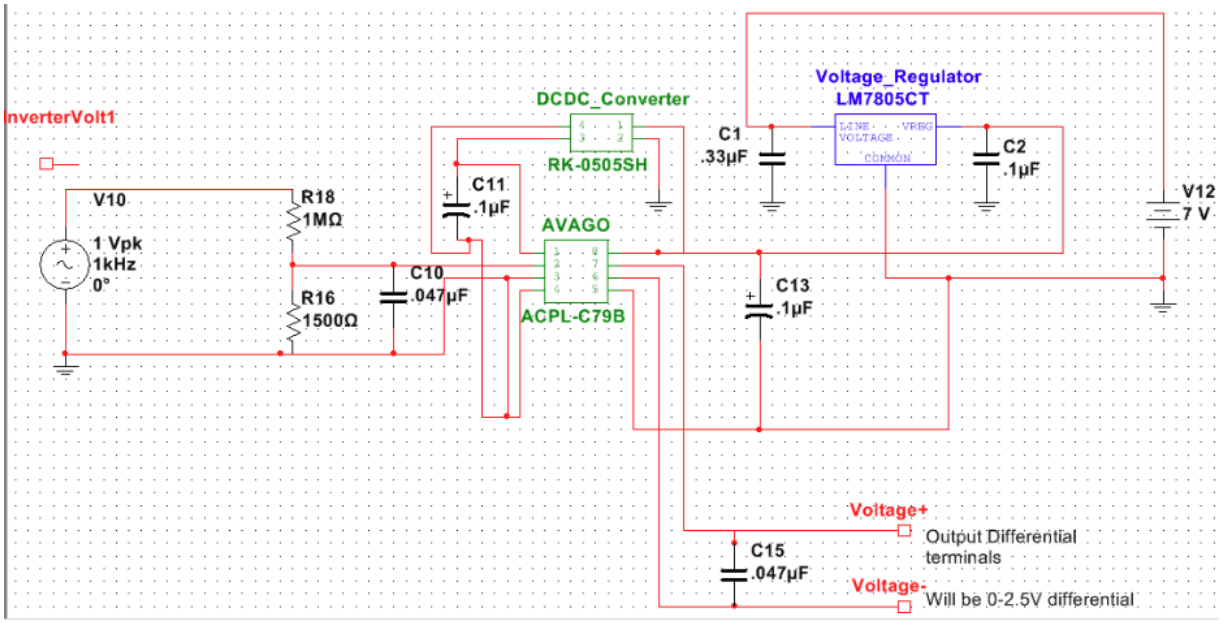


Figure 5.4: Schematic of a single Voltage Sensing circuit

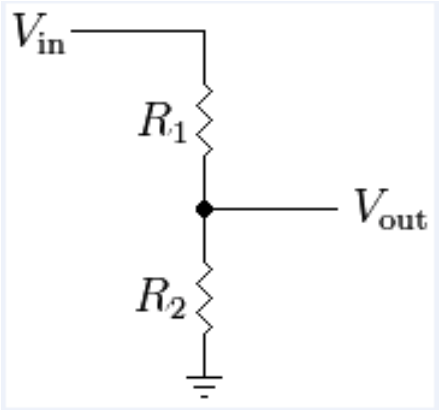


Figure 5.5: Voltage Divider Layout

Isolator chip. An important thing to note with the usage of the AVAGO Opto-Isolator chip is its input resistance between the input (pin 2) and grounds (pins 3 and 4). This resistance is shown in the data sheet (see below) and is typically 20 kΩ. This is important because it adds another resistance that is equivalent to a resistance in parallel with R2 (which will lower the actual resistance value). In the designed prototype, using the 5 kΩ potentiometer, it is the same as having an R2 value of 4 kΩ.

In order for the customer to easily change the resistor values on the device, based on their needs, the design has been created with R2 (in Figure 5.5) as a potentiometer. A potentiometer is a variable resistor. The resistor value can be altered (in this case) by using a small screw driver and turning an adjustable knob on the potentiometer. For our design, the Bourns 3214J – 5-Turn Trimpot Trimming Potentiometer will be used. This design is a surface mount device. The part number for this potentiometer is 3214J-1-502E. The initial value of the potentiometer is 5,000Ω. The device can be turned to change the resistance value from anywhere from 5,000Ω to 0Ω. Some arbitrary values are shown below.

The table shows the various turns of the potentiometer. By turning the knob on the po-

Resistance Value(Ω)	Input resistance of AVAGO (Ω)	Proportion of Voltage Divider	Percentage of voltage into AVAGO
5000	4000	4000/51000	7.8%
4000	3333.33	3333.33/51000	6.5%
3000	2608.70	2608.70/51000	5.1%
2000	1818.18	1818.18/51000	3.6%
1000	952.38	952.38/51000	1.9%
0	Undefined	0/51000	0%

Table 5.1: Resistance Values for Potentiometer

tentiometer, the resistance value will therefore change. The values of the resistances based on the number of turns on the knob are shown below. Based on these values, and the fixed resistor (R1), the output voltage of the divider (which will become the input to the AVAGO Opto-Isolator chip) changes as a proportion based on the description of the voltage divider. These values are also shown in Table 5.1. Depending on the voltage levels of the customer, the potentiometer will have to be adjusted accordingly. The potentiometer limits the amount of voltage into the AVAGO chip, so that it can function correctly.

In order to correctly use the potentiometer, the leads must be attached correctly. There are three pins on the potentiometer, and are shown below in Figure 5.6.

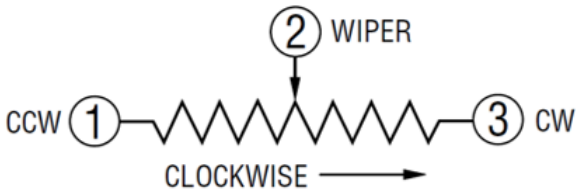


Figure 5.6: Potentiometer Layout

In order to use the full 5,000 Ω, the leads must be connected across pins 1 and 3. In order to use a resistance value less than or equal to 5,000 Ω, the leads must be attached pins 1 and 2 and the screw must be turned to adjust to the necessary resistance value.

As for every component, the product dimensions are important to consider to ensure every part will fit on the board designed for the inverter. The Bourns Potentiometer layout and mechanical specifications can be found in the datasheet location in Appendix **??**.

The usage of a potentiometer rather than a regular resistor allows for the inverter to be more flexible, and deal with a larger range of voltages, based on the customer needs.

AVAGO Opto-Isolator

The AVAGO Opto-Isolator chip is what the entire voltage sensing board revolves around. In this design, we are going to be using the AVAGO Opto-Isolator chip (ACPL-C79B-000E). This isolation amplifier is designed for both current and voltage sensing needs. This chip is able to be used for current and voltage sensing circuits along with many other applications. The primary reason for choosing this chip rather than another is because the AVAGO chip is especially useful for isolating precision analog signals in a noisy environment. The voltage measurements need to be precise and accurate and cannot be improperly measured due to noise of the surrounding

circuit and electrical system. In addition, this chip is able to scale the voltage signal back up to a level that the FPGA can use and understand. The output voltage is approximately 8.2 times higher than the input voltage, which would give us an output voltage range of -1.6V to 1.6V.

As mentioned earlier, for safety and reliability reasons, the input voltage from the generator must be electrically isolated from the output voltage, which will be passed on to the upstream boards. Improper isolation could lead to damaged parts, inaccurate readings, and safety hazards. One feature of the AVAGO Opto-Isolator board is electrical isolation between pins 1-4 (input side) and pins 5-8 (output side). The usage of this electrical isolation is incredibly important for the function of this inverter, which is one of the reasons it was chosen.

The last main feature that led to the usage of the AVAGO Opto-Isolator chip in this design was the fact that it provides differential outputs. This chip has the ability to take either single-ended or differential inputs and automatically provides a differential output. Referring back to the initial requirements and features of the chip, the differential output is useful for distinguishing the noise in the circuit and eliminating it. The positive and negative output voltages allow for two voltage signals which can eventually be subtracted from one another in order to remove the noise from the original signal. Based on the combination of these features with the AVAGO Opto-Isolator chip, it will be used in the design of the inverter.

Now that this chip has been selected, more information will be discussed on its operation and layout. There are eight pins on the AVAGO Opto-Isolator. The functional diagram of the chip is shown below followed by the description of each pin.

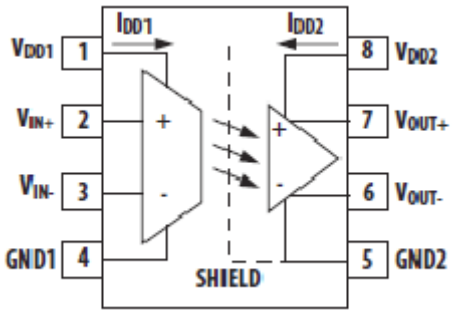


Figure 5.7: Layout of AVAGO Opto-Isolator chip

Pin No.	Symbol	Description
1	V_{DD1}	Supply voltage for input side (4.5 V to 5.5 V), relative to GND1
2	V_{IN+}	Positive input (± 200 mV recommended)
3	V_{IN-}	Negative input (normally connected to GND1)
4	GND1	Input side ground
5	GND2	Output side ground
6	V_{OUT-}	Negative output
7	V_{OUT+}	Positive output
8	V_{DD2}	Supply voltage for output side (3 V to 5.5 V), relative to GND2

Figure 5.8: Description of Pin Layout of AVAGO Opto-Isolator chip

The eight pins of the AVAGO chip each has a unique purpose in the greater voltage sensing circuit. In order to power the chip, a supply voltage must be provided. Pin 1 is the supply voltage for the input side, and must remain relatively steady, at 4.5 to 5.5V, which is relative

to GND1 (pin 4). Because the chip is isolated between the input and output sides, an output supply voltage must also be provided. This supply voltage must be between 3 to 5.5V, which is relative to GND2 (pin 8). In order to provide these steady voltages, a DC-DC converter, voltage regulator, and voltage supply must also be included in the design.

A voltage regulator is an electronic device that is designed to maintain a constant voltage level. This device in the circuit is used in conjunction with the DC/DC Converter in order to provide a constant 5V voltage supply to both the input and output voltage supply pins. In this design, the Fairchild Semiconductor 3-Terminal Positive Voltage Regulator (LM7805CT) has been chosen. Supplied by a customer provided 7V (or higher) source, the voltage regulator is placed to remove fluctuation and noise from the voltage supply. In order for the AVAGO Opto-Isolator chip to function correctly and consistently, it must receive a constant, steady voltage supply. Because of the voltage regulators drop-out voltage; the supply voltage must be higher than the output voltage. According to the data sheet, the input supply voltage must be 7V or higher, due to the 2V drop-out voltage (loss from input to output). In addition, in common practice, two capacitors must be added to the input and output sides of the regulator to ground similar to the Figure 5.9.

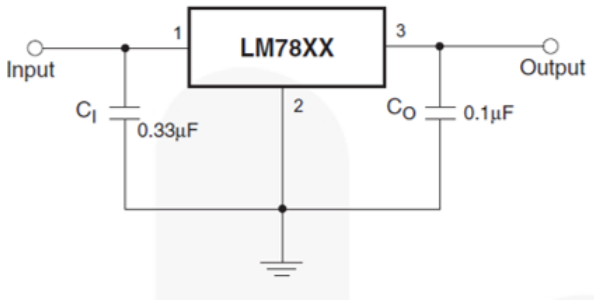


Figure 5.9: Voltage Regulator Connections

This voltage regulator will provide an output voltage anywhere from 4.75V to 5.25V, both of which are within the specifications of the AVAGO chip, and directly correlates to the voltage regulator's 4% output voltage tolerance.

In addition, the voltage regulator provides thermal overload and short-circuit protection in order to protect the circuit from the malfunctions of the voltage source. This further isolates the system and will protect it if something malfunctions. The pin layout and descriptions are shown in the Figure 5.10 below.

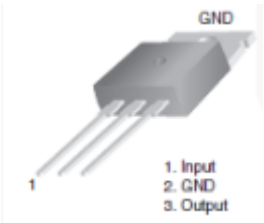


Figure 5.10: Voltage Regulator Pin Layout

According to these pin layouts and pin descriptions, the circuit schematic and design has been connected accordingly. The data sheet for this device can be found in the Appendix B. This device works in conjunction with the DC/DC Converter which will be described next.

A DC-DC converter is an electronic device that converts a DC voltage from one voltage level to another. In this circuit, it is important to provide the AVAGO chip with the proper voltage

so it can continue to function properly. The chosen DC-DC Converter for this project was the RECOM Econoline DC/DC Converter (Rk-0505S/H). The primary function of this device is to receive the regulated voltage (from the voltage regulator), provide further electrical isolation, and provide a steady 5V output.

This device has up to 4,000 VDC of isolation and can receive a wide range of input voltages. No matter the received voltage, it will provide a steady 5V source for the input voltage supply (pin 1) and continue to isolate it from the output side. The main purpose of this device is to ensure that both the input and output voltage supply pins receive the proper voltage source while keeping the circuit electrically isolated.

The layout of the RECOM 5V DC/DC Converter is shown below which is followed by the pin descriptions.

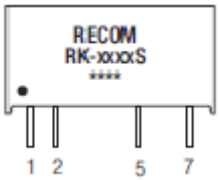


Figure 5.11: DC/DC Converter Pin Layout

Pin Connections
RK-xxxxS

Pin #	Single
1	+Vin
2	−Vin
5	−Vout
7	+Vout

Figure 5.12: DC/DC Converter Pin Descriptions

The circuit diagram discussed at the beginning of the voltage sensing circuit section shows the proper connections for this device to the rest of circuit. The data sheet for this device can be found in Appendix B.

In order for the AVAGO Opto-Isolator chip to work correctly, it also needs bypass capacitors connected between some of its pins. According to the data sheet, it is recommended that bypass capacitors are connected pins 1 and 4 and pins 5 and 8. These capacitors are 0.1µF and must not be electrolytic capacitors due to their nature of being polarized. This could lead to malfunctions and destruction of capacitors. These capacitors are required because of the high-speed digital nature of the signals inside the isolation amplifier. These capacitors should be placed as close to the AVAGO Opto-Isolator pins as possible. It is important to note that for testing purposes, across a large frequency range (BODE plots, etc.) it is necessary to remove these bypass capacitors, because they will block higher frequency AC signals (as a lowpass filter).

Bypass capacitors that are 47nF are also needed between pins 2 and 3 and pins 6 and 7. These capacitors are placed in between the positive and negative input voltage signals as well as the positive and negative output voltage signals. These capacitors are recommended due to the switched-capacitor nature of the input circuit. These capacitors are also used to prevent high-frequency noise from interfering with the input signal.

These capacitors are critical in ensuring that the AVAGO chip can function properly as well as translate an input voltage signal into an amplified output differential signal with as little

noise and distortion as possible. With less noise and distortion, the readings will be much more accurate, and lead to greater efficiencies for the entire system.

The last component required by the AVAGO Opto-Isolating chip is a voltage supply. This voltage supply will be supplied by the customer, and the customer would have a range of choices. With the selected DC/DC Converter and Voltage Regulator, it is recommended that a 5V source is used. This voltage source is required in order to power the AVAGO chip. Using the voltage straight from this voltage source is risky, and could potentially be noisy or unreliable. Because of this possibility, the DC/DC Converter and Voltage Regulator is placed in between the voltage source and AVAGO chip.

Returning to the overall discussion of the AVAGO Opto-Isolator chip, the remaining pins must be explained. In order to analyze and isolate the voltage signal, the voltage signal must first be passed into the device. There are two inputs on the chip, the positive and negative inputs (pins 2 and 3 respectively). Typically, a single ended input would be used, so in this case, the output from the voltage divider would become the input to the AVAGO chip. Because a single-ended input is being used, the negative input (pin 3) is typically connected to GND1 (pin 4), and grounded (different ground than GND2 on output side).

The output of AVAGO chip is a differential output. The negative output voltage signal is pin 6, while the positive output voltage signal is pin 7. By using both of these pins as the output signal, the two signals are able to be compared, and the FPGA will be able to remove any noise before it analyzes the signal waveform. Lastly, because this chip is electrically isolated, there are two grounds, one for the input and one for the output side, so pin 5 is used as the GND2 for the output side.

It is important to also consider the physical layout of the device. On the UMIC, there is limited space to work with, so all larger chips and components must be carefully considered. The typical package type for the AVAGO chip is a stretched SO-8 Package (SSO-8). The measurements of this package are shown in Figure 5.13.

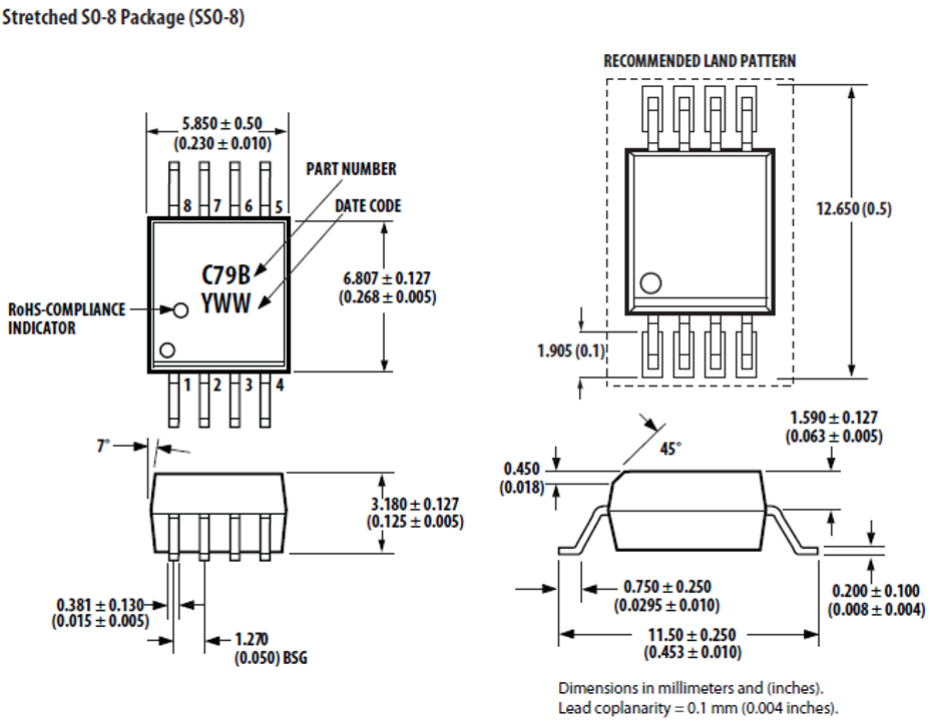


Figure 5.13: AVAGO Opto-Isolator Package details

As mentioned previously, the entire voltage sensing circuit board revolves around the usage of the AVAGO Opto-Isolator chip. All of these components must come together to support the correct functionality of the AVAGO chip and the entire voltage sensing circuit. If done correctly, two output voltage signals should be produced that will be an amplified version of the input voltage signals.

Output Voltages

The final outcome of the voltage sensing circuit is the output voltage signals. Coming directly from the AVAGO Opto-Isolator chip, a differential output will be seen. Pin 6 is the negative output voltage signal and Pin 7 is the positive output voltage signal. When these two signals are compared, another circuit is able to determine what noise there is in the system. Therefore, the noise can be eliminated, and a much cleaner signal can be used. The gain of the AVAGO chip is typically 8.2, which means the output voltage range will be anywhere from -1.6V to 1.6V. These two output voltage signals will then be passed to the high speed, differential analog-digital converters (on an adjacent board) for further signal processing. After the signal is passed on to the ADC, this marks the end of the requirements and design of the voltage sensing board.

5.2 Current Sensing Board

5.2.1 Description of circuit

As described in the previous section about the voltage sensing circuit, it is necessary for the UMIC to constantly monitor and process voltage and current information, in order to create a constantly self-adjusting, negative feedback loop. The purpose of this circuit is to constantly monitor the AC and DC current in the system, rather than the voltage as previously discussed. For this design, it is necessary to have four identical current sensing boards in order to measure the three different phase inputs (A, B, C) and the DC currents. This section will describe how the current levels are captured using sensors, translated to a differential signal, and then output to an ADC to eventually be interpreted by the FPGA.

5.2.2 Schematic of Circuit

The first portion of the board is the sensing portion, which extracts a proportional (based on the current flow) voltage that will be the inputs for the current sensing chip. The second portion of this board is the actual current sensing chip, which will take these proportional voltages and translate them into differential outputs, which will then be passed further down the chain to be interpreted. The layout of the current sensing boards are shown below (alongside the voltage sensing boards) in Figure 5.14.

These sensing boards (the voltage sensing board and current sensing board) are responsible for isolating the appropriate signals, translating that signal into a scaled output, and passing that output to the interpreting boards (FGPA). In the figure above, you can see the high speed differential Analog to Digital converters which will convert the analog signal provided by the sensor boards to a digital signal which the interpreting boards can then analyze. These sensing boards are labeled as “Powerstage” boards and at the lowest level of the inverter. The schematic of the actual Current Sensing circuit is shown in Figure 5.15.

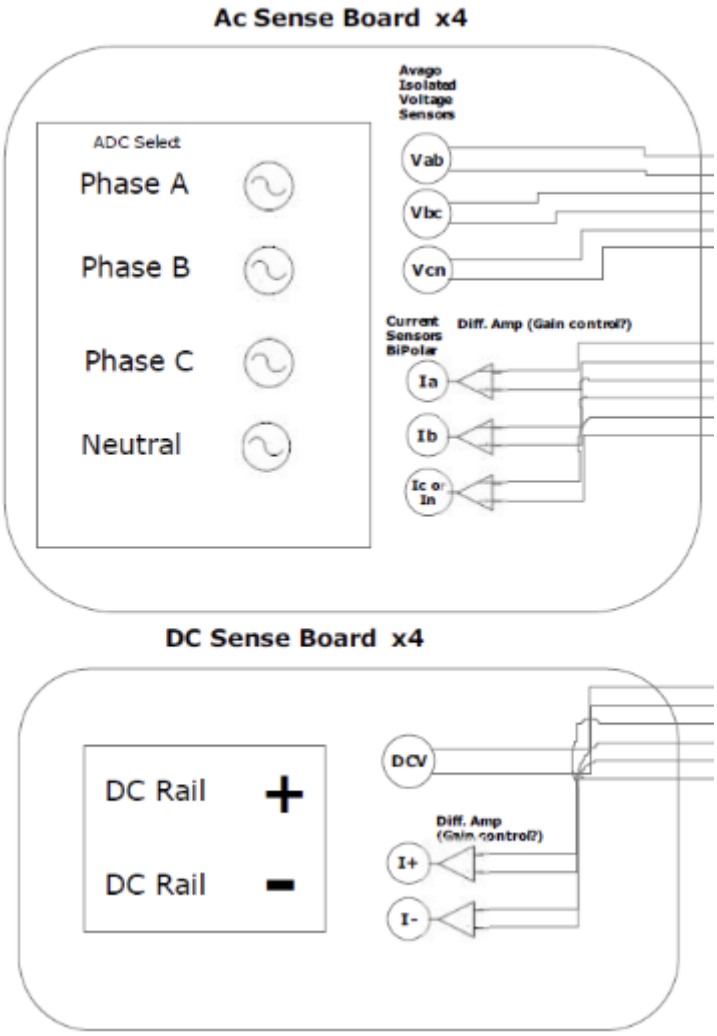


Figure 5.14: Layout diagram of AC/DC Sense Boards

Input Currents

The input currents to the current sensing boards will be taken directly from the customer's electrical system. Each phase of the AC components, as well as the DC component will have cables between the generator and the load in order to deliver the necessary power. These cables will run directly through the current sensor (which is the shape of an O-ring). Because of the "Hall Effect", a voltage will then be induced based on current flowing and strength of the magnetic field. The current levels vary based on the user. The current sensing boards must be able to deal with this range in order to provide accurate readings at all times. These characteristics allow the designer several options in choosing the necessary parts. In order for the current to be accurately detected and measured, a proper current sensor must first be chosen. In Figure 5.16, the power cables (between the generator and load) running through the current sensor is shown. In the next section, the current sensors will be described in detail.

TAMURA Hall Effect Current Sensors

The current sensors just described above are used in a similar fashion as current transformers. Based on the "Hall Effect", the current of the device travels through the core of the current

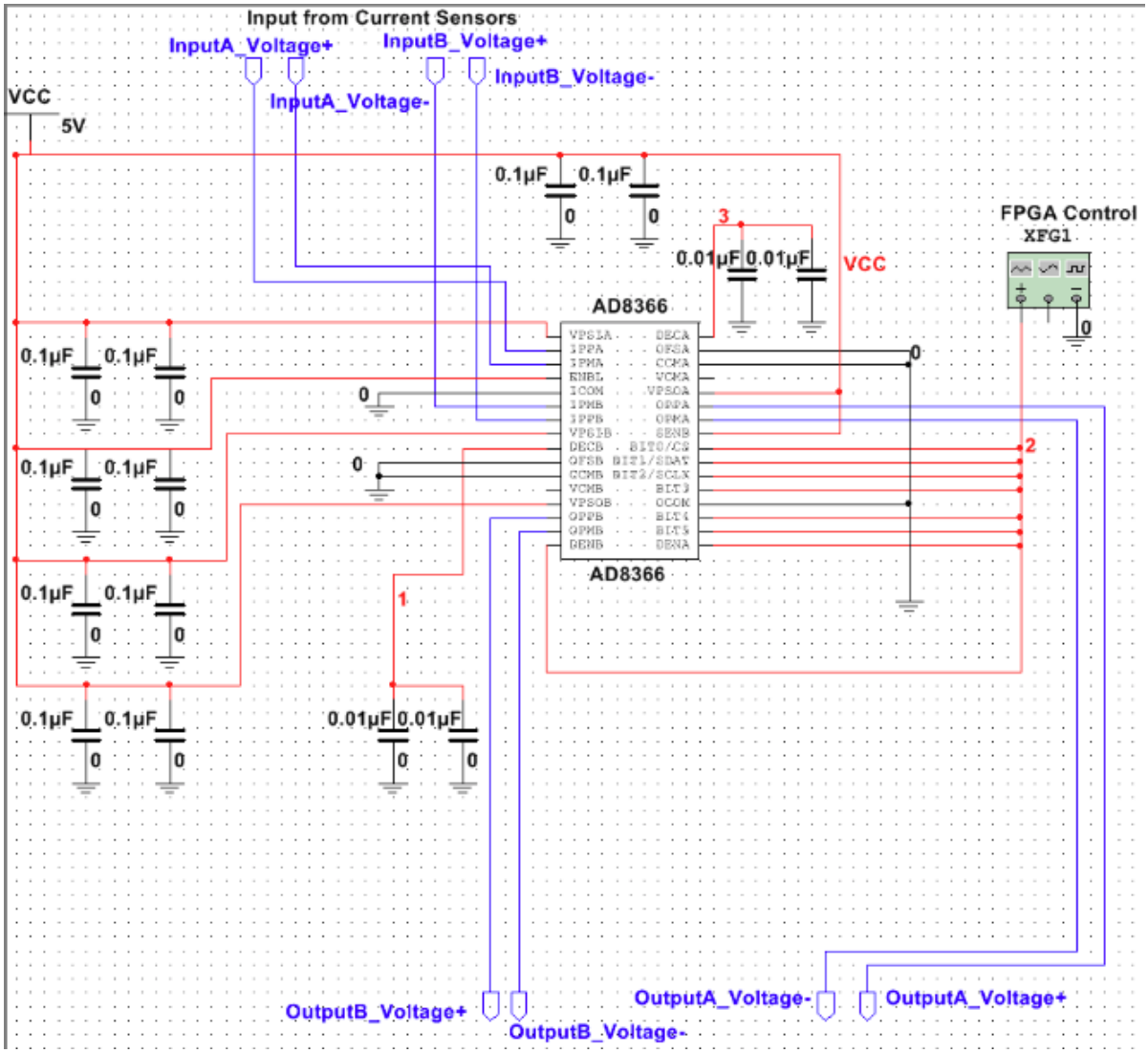


Figure 5.15: Schematic of Current Sensing Board

sensor and induces a voltage based on the characteristics and amplitude of the current source. Based on these characteristics, a unique (to the current sensor design) voltage will be created, which will directly correlate to the current level in the wires. This information will be added to the coding and configuration of the FPGA which will then be able to interpret the current levels in the system by receiving a scaled down voltage. For this design, two different TAMURA Hall Effect Current Sensors have been selected. Part of the design will be based on the customer's needs and current levels. The two TAMURA Current Sensors that have been chosen are based on the average current levels that the user expects to see in their system. For lower currents, the TAMURA L31S***S05FS Series was chosen. It is anticipated that this current sensor will be used for anywhere from 50A to 300A. For higher currents, the TAMURA L06P***S05 Series was chosen. It is anticipated that this current sensor will be used anywhere from 400A to 800A.

For lower power applications, the L31S***S05FS Series Current Sensor might be chosen. This particular sensor would be used on applications that have nominal primary current values from 50A to 300A. Although this particular sensor has models up to 600A, the TAMURA L06P***S05 is typically a better choice at higher current levels. The design of this sensor differs slightly from the original picture above, but the same "Hall Effect" concept applies.

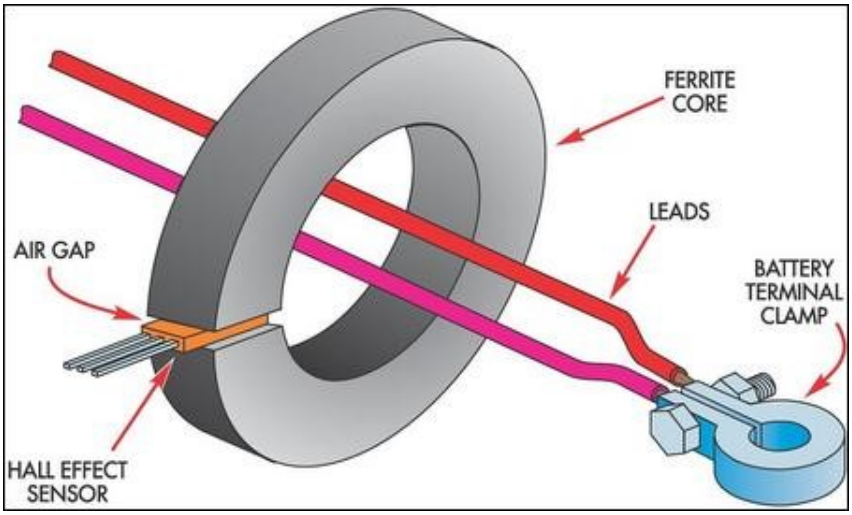


Figure 5.16: Diagram of Hall Effect Current Sensor source: http://archive.siliconchip.com.au/static/images/articles/i305/30551_15lo.jpg

Figure 5.17, is the exact current sensor used for this design is shown.

Figure 5.17: Picture of TAMURA L31S***S05FS Current Sensor

This specific current sensor was chosen based on its excellent accuracy and linear saturation characteristics. This allows for extremely accurate current readings to take place, and easier programming in regards to the FPGA. In addition, this design should be flexible and easy to adapt to the customer's needs. This current sensor is able to be used on a wide range of frequencies, with little adjustment from the user. Lastly, this current sensor has a high immunity to external interference, so for usage in a noisy, dirty, hot environment such as an engine room on a commercial shipping vessel, this current sensor will still be able to provide accurate readings and measurements.

Similar to the overall schematic of the current sensing board previously described, the current sensor is one of the two main components on this board. The TAMURA Current Sensor has a rather simple electrical set up, and only has one main purpose. This simple device is shown below in Figure 5.18.

This current sensor accepts the primary conductor which carries a current, I_f, through normal usage. This current flows through the inverter as it is transferred from the generator to

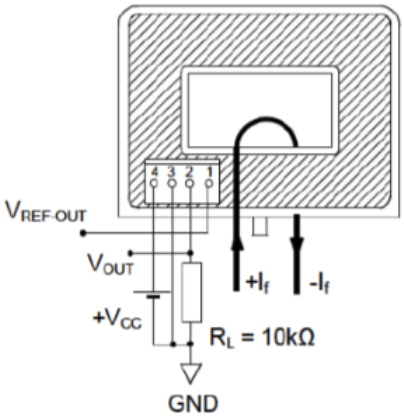


Figure 5.18: Schematic of the TAMURA L31S***S05FS Current Sensor

the load. The current sensor, how it is designed, extracts an induced voltage from the current running through it. There are four pins on the current sensor. According to the schematic of the circuit as well as the current sensing board, the circuit was set up according to the following Table 5.2.

Pin	Description
1	Voltage Reference
2	Output Voltage (connected with resistor)
3	Ground
4	Supply Voltage (5V)

Table 5.2: Connections for TAMURA L31S***05FS Current Sensor

Like any electrical device, this connections must meet certain parameters in order to function correctly. Depending on the typical current levels of the customer, a current sensor can be chosen. As discussed earlier, this current sensor is best from 50A – 300A. This device also calls for a 5V supply among other things. The reference voltage can be set to whatever the user wants, and this value will be reflected in the rated output voltage as shown in the datasheet in the Appendix B. With the L31S***05FS Current Sensors, it is possible to take advantage of the differential inputs of the AD8366. Because there is a Output Voltage (pin 2) and a Reference Voltage (pin 1), it is suggested that both pins connect to either of the differential inputs of the Analog Devices AD8366 for more effective noise cancellation. In the "Results" section, basic testing is done using the different inputs.

This TAMURA L31S***05FS Current Sensor requires its own voltage supply in order to operate correctly. In this case, the current sensor requires a 5V supply, ±5% (±0.25V). In testing it is adequate to use a power supply, but in actual implementation it would connect to a common 5V rail, whose power source would be supplied by the customer.

Also shown in the schematic, the proper usage of this current sensor requires the use of a resistor (to limit current). This resistor is specified by the manufacturer to be 10,000 Ω. This resistor is placed between the output voltage and ground.

In order to meet the tight packaging requirements of the UMIC, each devices physical requirements must be considered, as well as the shape of the device. Although this is a relatively small device, it is perhaps the second largest electrical component in the entire inverter. The reason why these measurements are so important is that four of these current sensors must fit

in the inverter. The exact dimensions can be found in the datasheet.

The last important characteristics to consider when using this current sensor is how the various primary nominal currents (at various current levels) proportionally affect the voltage levels, including at different frequencies. This first graph, Figure 5.19, shows the linear relationship between the input current (A) and output voltage (V).

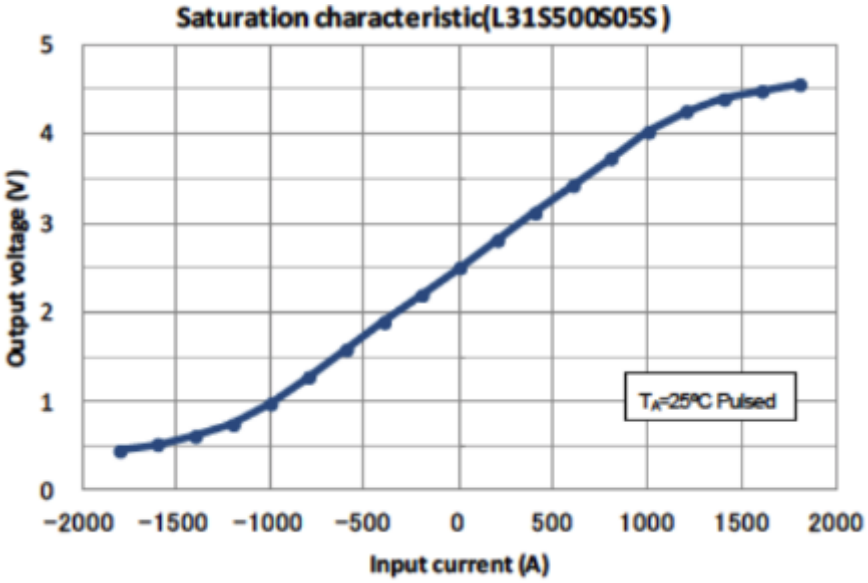


Figure 5.19: Saturation Curve of the TAMURA L31S***S05FS Current Sensor

This particular linear relationship makes it much easier to calculate the current flowing through the primary conductor when reading the output voltage. Although this graph is for the 500A version of the current sensor, all of the current sensors in this family have similar linear relationships between the input current and output voltage. For example, if the generator is providing power to the load, and there are 500A flowing through this particular conductor to the load to provide power, the output voltage would be roughly 0.6V (plus offset voltage), which would then be read by the FPGA, and interpreted as 500A. In this case, the offset voltage is 2.5V (shown at 0A input), which matches up with the rest of the graph. The output voltage (with no added offset voltage) Saturation Table will confirm these data in the datasheet.

Finally, the last characteristic that is worth delving into is the frequency response of the current sensor. In order to ensure this device is as versatile as possible, it is important that the current sensor will work across the majority of frequencies with little deviation and little error. This current sensor was chosen partially because of its frequency response. In Figure 5.20, the attenuation (dB) is shown for a test current (which was chosen to be 30A RMS) over different frequencies. Even up to 100 kHz, the current sensor provides similar results in output voltage, only skewing the results at 100 kHz by about -1 dB.

In the test cases, the output voltage response changed up to 4V difference from 100 Hz to 100 kHz. In most systems the frequency will not be changing this drastically, and the attenuation can be accounted for if necessary by scaling a certain amount.

This is one of two potential current sensors to be used in this design. This current sensor that was just discussed, the TAMURA L31S***S05FS Current Sensor will be used for customers who need to sense currents in the range of 50A to 300A, while the following section will discuss the TAMURA L06P***S05 Series Current Sensor for higher current levels, namely, 400A to 800A.

For higher power applications, the L06P***S05 Series Current Sensor might be chosen.

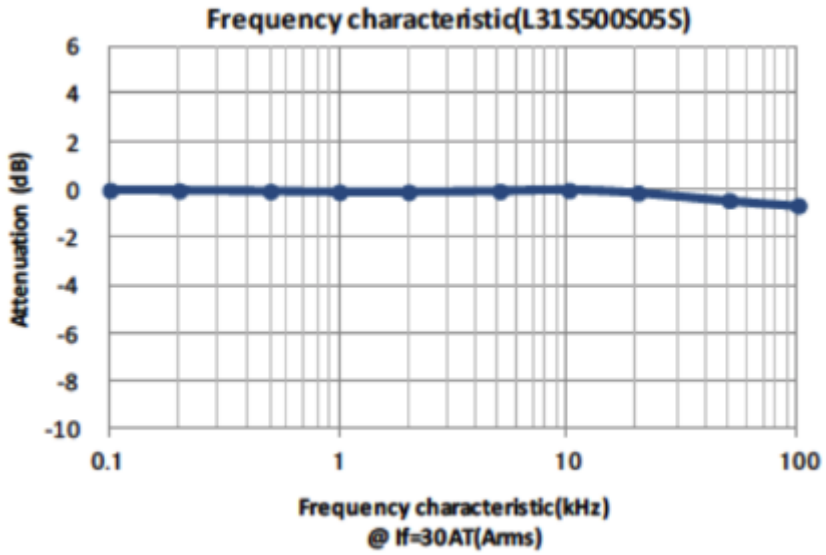


Figure 5.20: Frequency Curve of the TAMURA L31S***S05FS Current Sensor

This particular sensor would be used on applications that have nominal primary current values from 400A to 800A. Although this particular sensor has models up to 600A, the TAMURA L06P***S05 is typically a better choice at higher current levels. Below in Figure 5.21, the exact current sensor used for this design is shown.

Figure 5.21: Picture of the TAMURA L06S***S05 Current Sensor

This specific current sensor was chosen based on its excellent accuracy and linear saturation characteristics. This allows for extremely accurate current readings to take place, and easier programming in regards to the FPGA. In addition, this design should be flexible and easy to adapt to the customer's needs. This current sensor is able to be used on a wide range of frequencies, with little adjustment from the user. Lastly, this current sensor has a high immunity to external interference, so for usage in a noisy, dirty, hot environment such as an engine room on a commercial shipping vessel, this current sensor will still be able to provide accurate readings and measurements.

Similar to the overall schematic of the current sensing board previously described, the current sensor is one of the two main components on this board. The TAMURA L06P***S05 Current

Sensor has a rather simple electrical set up, and only has one main purpose. This simple device is shown below in Figure 5.22.

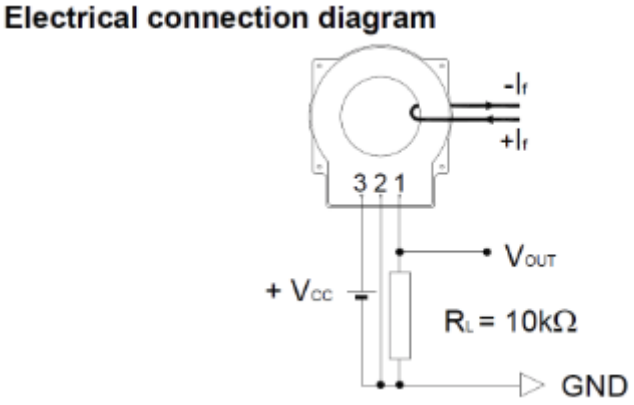


Figure 5.22: Electrical Schematic of the TAMURA L06S***S05 Current Sensor

This current sensor accepts the primary conductor which carries a current, If, through normal usage. This current flows through the inverter as it is transferred from the generator to the load. The current sensor, how it is designed, extracts an induced voltage from the current running through it. There are four pins on the current sensor. According to the schematic of the circuit as well as the current sensing board, the circuit was set up according to the following Table 5.3.

Pin	Description
1	Output Voltage (connected with resistor)
2	Ground
3	Supply (5V)

Table 5.3: Connections for TAMURA L06P***S05 Current Sensor

Like any electrical device, this connections must meet certain parameters in order to function correctly. Depending on the typical current levels of the customer, a current sensor can be chosen. As discussed earlier, this current sensor is best from 400A – 800A. This device also calls for a 5V supply among other things. The exact electrical specifications can be found in the datasheet. With the L06P***S05 Current Sensors, it is only possible to use a single-ended input into the AD8366. Because there is only an Output Voltage (pin 1) and no Reference Voltage pin, this current sensor can only send a single-ended input to the Analog Devices AD8366. In the "Results" section, basic testing is done using the single-ended inputs.

This TAMURA L06P***S05 Current Sensor requires its own voltage supply in order to operate correctly. In this case, the current sensor requires a 5V supply, ±0.1. In testing it is adequate to use a power supply, but in actual implementation it would connect to a common 5V rail, whose power source would be supplied by the customer. Also shown in the schematic, the proper usage of this current sensor requires the use of a resistor (to limit current). This resistor is specified by the manufacturer to be 10,000 Ω. This resistor is placed between the output voltage and ground.

In order to meet the tight packaging requirements of the UMIC, each devices physical requirements must be considered, as well as the shape of the device. Although this is a relatively small device, it is perhaps the second largest electrical component in the entire inverter. The

reason why these measurements are so important is that four of these current sensors must fit in the inverter. The exact measurements and shapes are shown in the datasheet.

The last important characteristics to consider when using this current sensor is how the various primary nominal currents (at various current levels) proportionally affect the voltage levels, including at different frequencies. This first graph, Figure 5.23, shows the linear relationship between the input current (A) and output voltage (V).

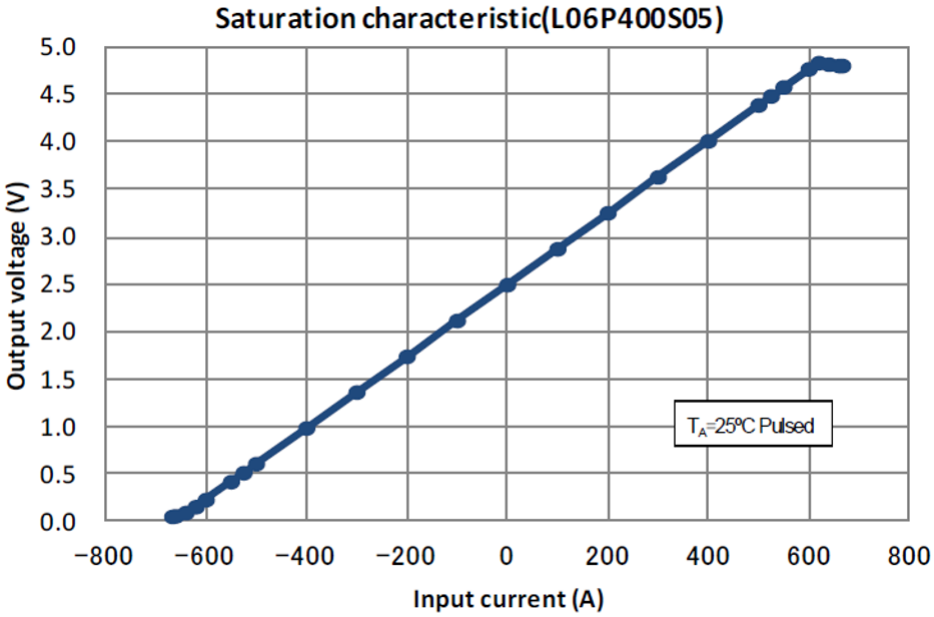


Figure 5.23: Saturation Curve of the TAMURA L06S***S05 Current Sensor

This particular linear relationship makes it much easier to calculate the current flowing through the primary conductor when reading the output voltage. Although this graph is for the 400A version of the current sensor, all of the current sensors in this family have similar linear relationships between the input current and output voltage. For example, if the generator is providing power to the load, and there are 400A flowing through this particular conductor to the load to provide power, the output voltage would be roughly 4.0V, which would then be read by the FPGA, and interpreted as 400A.

Finally, the last characteristic that is worth delving into is the frequency response of the current sensor. In order to ensure this device is as versatile as possible, it is important that the current sensor will work across the majority of frequencies with little deviation and little error. This current sensor was chosen partially because of its frequency response. In Figure 5.24 below, the attenuation (dB) is shown for a test current (which was chosen to be 40A RMS) over different frequencies. Even up to 100 kHz, the current sensor provides similar results in output voltage, only skewing the results at 100 kHz by about -2 dB. However, where this device differs from the L31S***05FS Current Sensor is from the 3000 Hz – 50,000 Hz. In the case of this current sensor, it actually overcompensates, and reaches up to about 1 dB of attenuation in these ranges.

As discussed previously, this is one of two potential current sensors to be used in this design. This current sensor that was just discussed, the TAMURA L06P***S05 Current Sensor will be used for customers who need to sense currents in the range of 400A to 800A. After the customer has chosen the appropriate current sensor, the rest of the circuit can be put in place, namely the Analog Devices AD8366 Digital Voltage Gain Amplifier.

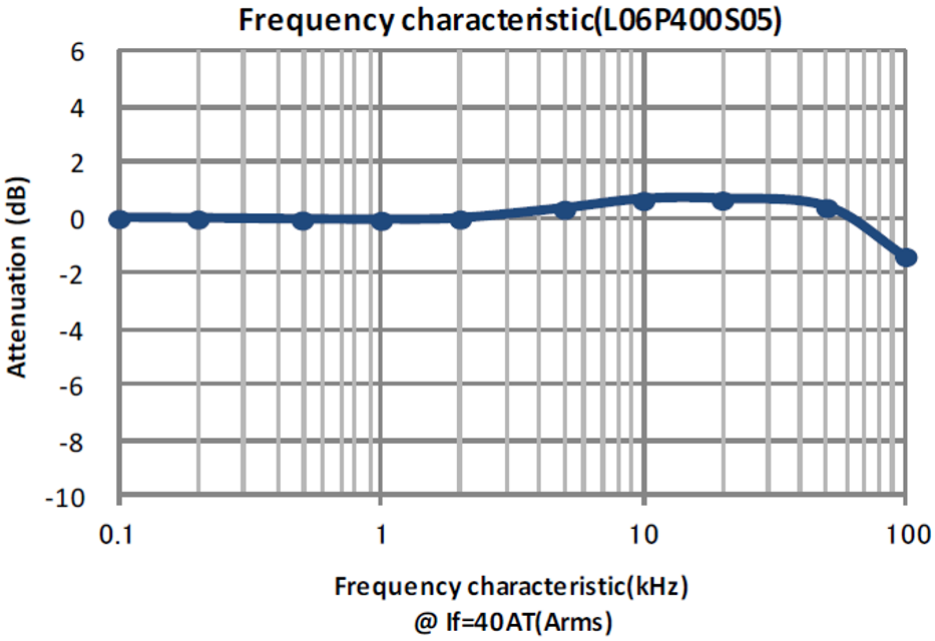


Figure 5.24: Frequency Curve of the TAMURA L06S***S05 Current Sensor

Analog Devices Digital Voltage Gain Amplifier

The Analog Devices AD8366, Digital Voltage Gain Amplifier is the most complex chip used on either of the two sensing boards. With 32 different pins, it is important to fully understand the usage and functionality of the AD8366 before implementing it into a design. The reason this chip was chosen was due to its flexibility, dual inputs, and variable gain abilities.

This chip is essentially two digital variable gain amplifiers placed on a single chip. This chip has the ability to take two different differential inputs (although this inverter design uses single-ended inputs) which then are altered to become amplified differential outputs. This chip gives much control to the FPGA, which will be able to enable or disable the chip, change programming modes, enable or disable chip programming, and adjust gain amplification via the AD8366's pins (see Pin Descriptions below). This chip allows for great control and flexibility, which is a perfect fit for this application. The input signal will be taken from the current sensor and brought to the inputs of the AD8366. For this design, dual inputs will be used, taking a different input signal from two different current sensors. Each signal will be amplified between 4.5dB to 20.25dB. The exact amplification will be set via the FPGA using parallel mode programming on the chip. The two inputs can be amplified at the same dB value, or entirely different values. Lastly, the output signals will be differential, which will help determine and eliminate noise on upstream boards. Because of these many reasons, the AD8366 Dual-Digital Variable Gain Amplifier chip was chosen for this inverter project. One important consideration for this chip is the rather high current requirements. This chip requires several 5V sources, with a current consumption of about 180mA. When in use, the chip requires about 900mW of power.

As far as the sensing circuits are concerned, the AD8366 DVGA chip is the most complex and has the most inputs and outputs, and therefore the most pins. It is important that each pin is utilized correctly to get the right function needed for current sensing. The data sheet provides some insight into the pin connections, but some gaps must be filled and testing is required to fully understand the connections.

First it is important to understand the layout of the chip and the layout of the 32 pins, they

can be seen in Figure 5.25.

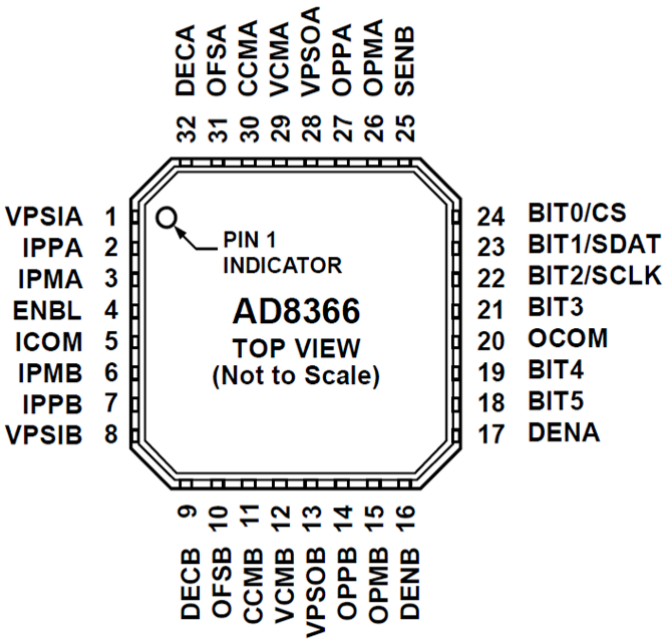


Figure 5.25: Pin Layout of the Analog Devices AD8366 DVGA

Based on the above pin considerations, the following Figure 5.26 shows and describes how each pin should be connected.

Pin No.	Mnemonic	Description
1, 8, 13, 28	VPSIA, VPSIB, VPSOB, VPSOA	Input and Output Stage Positive Supply Voltage (4.75 V to 5.25 V).
2, 3, 6, 7	IPPA, IPMA, IPMB, IPPB	Differential Inputs.
4	ENBL	Chip Enable. Pull this pin high to enable.
5, 20	ICOM, OCOM	Input and Output Ground Pins. Connect these pins via the lowest possible impedance to ground.
9, 32	DECB, DECA	$V_{POS}/2$ Reference Decoupling Node. Connect a decoupling capacitor from these nodes to ground.
10, 31	OFSB, OFSA	Output Offset Correction Loop Compensation. Connect a capacitor from these nodes to ground to enable the correction loop. Tie this pin to ground to disable.
11, 30	CCMB, CCMA	Connect These Nodes to Ground.
12, 29	VCMB, VCMA	Output Common-Mode Setpoint. These pins default to $V_{POS}/2$ if left open. Drive these pins from a low impedance source to change the output common-mode voltage.
14, 15, 26, 27	OPPB, OPMB, OPMA, OPPA	Differential Outputs.
16, 17	DENB, DENA	Data Enable. Pull these pins high to address each or both channels for parallel gain programming. These pins are not used in serial mode.
18, 19, 21, 22, 23, 24	BIT5, BIT4, BIT3, BIT2/SCLK, BIT1/SDAT, BIT0/CS	Parallel Data Path (When SENB Is Low). When SENB is high, BIT0 becomes a chip select (CS), BIT1 becomes a serial data input (SDAT), and BIT2 becomes a serial clock (SCLK). BIT3 to BIT5 are not used in serial mode.
25	SENB	Serial Interface Enable. Pull this pin high for serial gain programming mode and pull this pin low for parallel gain programming mode.
	EPAD	The exposed pad must be connected to ground.

Figure 5.26: Pin Descriptions of the Analog Devices AD8366 DVGA

These pin descriptions are a good starting point, but more research must be done in order to fully understand the connections needed. Table 5.4 fully describes the pin connections with more detail to this specific inverter application.

Pin	Mnemonic	Description

1, 8, 13, 28	VPSIA, VPSIB, VPSOB, VPSOA	These pins are the supply voltages of the chip. All four pins can be connected to the same voltage source, preferably at 5V, but can be ±0.25V. Each supply pin should also be decoupled with at least one low inductance, surface-mount ceramic capacitor of 0.1uF, placed as close as possible to the pin.
2, 3, 6, 7	IPPA, IPMA, IPMB, IPPB	These are the inputs of the chip, the signals being "sensed". This chip allows for two signals to be controlled and amplified at once. The device is able to handle differential inputs, but for our application, we are only interested in single-ended inputs. Pin 2 and 6 will be used as inputs from the current sensor, while Pin 3 and 7 will be grounded (because we are not using differential inputs).
4	ENBL	This is the enable for the entire chip. If the chip needs to be used, it needs to first be enabled. The enable pin must be set to HIGH in order for the chip to function. In this design, the FPGA will control when the chip will be used, but for most cases, will remain HIGH. It should receive about 5V (not to exceed 5.5V) in order to set the pin to HIGH. When the pin is LOW, the current consumption significantly decreases, to 3mA.
5, 20	ICOM, OCOM	These pins should be connected to ground, the lowest possible impedance (Z) ground.

9, 32	DECB, DECA	These two pins are used as the reference decoupling node. They are to be connected from pin to ground. The capacitors should be 0.01uF. It is recommended to use one or two capacitors to ground for each pin.
10, 31	OFSB, OFSA	The pins are each connected to a 8200pF capacitor if the user wants output offset correction to be enabled. For this design, this pin will be grounded, to disable this function.
11, 30	CCMB, CCMA	These pins are connected to ground.
12, 29	VCMB, VCMA	These pins to set the output common mode set-point. If the user wanted to change this value, they would do so at this pin. For this design, it will be left open (unconnected) and the default value will remain at $V_{POS/2}$.
14, 15, 26, 27	OPPB, OPBM, OPMA, OPPA	These are the two sets of differential outputs. These outputs are an amplified differential version of the single-ended inputs from the current sensor. In this case, the differential function is used, which requires two outputs (one positive and one negative output each). Pin 26 and 27 refer to the Channel A input (Pin 2 and 3) while Pin 14,15 refer to the Channel B input (Pin 6 and 7). These signals will be passed to the differential ADCs located on another board.

16, 17	DENB, DENA	These two pins are used in order to address either or both channels for parallel gain programming. Pins 18, 19, 21, 22, 23 and 24 are used for Parallel Programming. In order to enable this programming, these pins must be enabled. To enable Channel A programming, pull pin 17 HIGH (2.2V, 5.5V maximum), to enable Channel B programming, pull pin 16 HIGH (2.2V, 5.5V maximum). In order to address both pins at once, pull them both HIGH. These pins must be enabled in order to change the voltage gain amplifier value, or it will remain the current value.
18, 19, 21, 22, 23, 24	BIT5, BIT4, BIT3, BIT2, BIT1, BIT0	In parallel programming mode (used in this design), these pins will be used as logic input from the FPGA. Based on the values of each BIT (LOW or HIGH, $\leq$1.2V or +2.2V), the gain will decrease/increase by 0.25dB for each logic step (logic 000000 to 111111, creating 64 unique steps). This will enable the user and FPGA to control the gain amplifier (from input signal to amplified output signal) from any gain value in the range of 4.5dB to 20.25 dB gain.
25	SENB	This pin is used to set the chip to either serial or parallel gain programming mode. For this application and design, this pin will be grounded to set it to parallel programming mode. This will enable to usage of the six bits (pin 18, 19, 21, 22, 23, and 24) for parallel programming.

Table 5.4: Detailed Pin Descriptions for AD8366 DVGA

Please note that the exposed pad, EPAD, is grounded on either the breakout board (for breadboard usage) or in the PCB design.

Based on these design criteria and descriptions, the circuit has been set up in order to function most appropriately for this inverter design.

Now that each pin has been discussed, it is also critical to identify and understand the characteristics and specifications needed to supply each pin. In this design, the typical values are aimed for, and it is key to not exceed the minimum or maximum rated values to keep the chip functioning correctly and to not damage it. The data sheet provides some key insight into the necessary values at each pin.

This typical values should be strived for in each and every design that uses the AD8366. Of course, sometimes it is not possible to meet every single one of these specifications. However, for the chip to continue to function reliably and accurately, the maximum values must not be exceed.

The next constraints that must be met are not electrical, but rather mechanical restraints in fitting the inverter package into the smallest possible area. The package details and size of the component will be discussed in the next section.

The mechanical specifications of this chip are just as important as the electrical specifications in order to ensure each board fits within the smallest possible area in order to create a physically smaller inverter. Although this AD8366 chip is potentially the most complex, it is also one of the smallest chips, in fact the total area of the chip is less than 25mm^2. The exact dimensions are shown below in Figure 5.27.

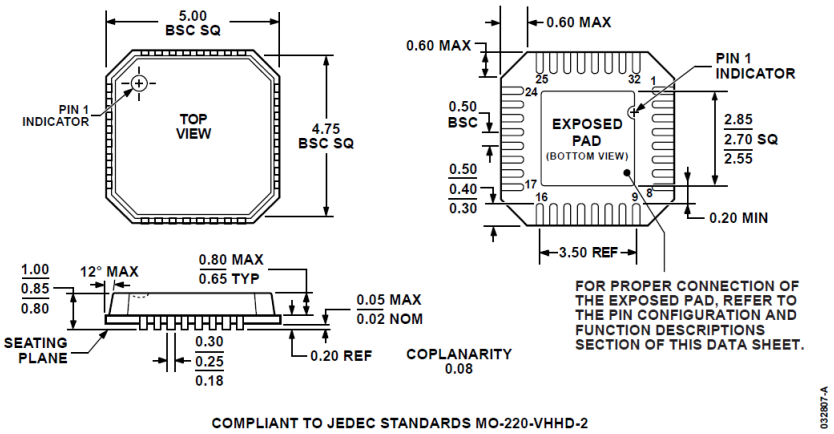


Figure 63. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8366ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-8
AD8366-EVALZ		Evaluation Board	

Figure 5.27: Mechanical Specifications for the Analog Devices AD8366 DVGA

The input voltages into the differential input pins (2, 3, 6, and 7) are taken in from the current sensors. The current sensors send a proportional voltage signal based on the current levels in the main electrical system. This proportional voltage signal is sent to the AD8366 in order to refine the signal and amplify it further. The input voltages have the potential to be differential inputs, but in this inverter, it will only use single-ended inputs, meaning pins 3 and 7 will remain grounded.

There are several bypass capacitors used in this circuit in order to help eliminate noise and ripple at the pins. For this chip to function accurately and reliably, it is important to add these bypass capacitors. There are three types of pins on the AD8366 that require bypass capacitors (voltage supply pins, decoupling capacitor pins, and potentially the Output Offset Correction Loop pins).

The voltage sources pins (1, 8, 13 and 28) require the usage of 0.1uF bypass capacitors. Each pin requires at least one of these low inductance, surface-mount ceramic capacitor of 0.1uF, placed as close as possible to the pin. It is also recommended to add a capacitor of this value to the Enable pin (4).

In addition, for the Reference Decoupling Nodes (pins 9 and 32) require the use of a decoupling capacitor to ground. These pins require a 0.01uF capacitor.

Lastly, if deemed necessary by the customer or for the application, the chip can enable the "Output Offset Correction Loop". If these pins (10 and 31) are enabled, they require an 8200pF capacitor at each pin to ground. Otherwise, they can be grounded to disable the feature.

In order for this chip to function and have power, it requires several voltage supplies. The actual voltage supply pins (1, 8, 13, and 28) are what power the AD8366. These voltage supplies must be at 5V $\pm$0.25V. In addition, the Enable pin (4) must also be supplied with the same voltage level in order to input HIGH and enable the chip. If this is not done, the chip will enter disabled mode, which consumes less current.

In addition to the 5V supply, a lower logic voltage is needed around 2.2V. This voltage supply is used for the DIGITAL LOGIC (pins 16, 17, 18, 19, 21, 22, 23, and 24) and will determine whether the pin is LOW or HIGH. This voltage will be supplied by the FPGA which will directly be controlling the DIGITAL LOGIC of the AD8366. Using this voltage level, the FPGA will be able to control the Data Enable, and Parallel Data Path pins.

Output Voltages

The current sensing board and AD8366 chip end at the output differential voltage pins (14, 15, 26, and 27). Inside of the AD8366 chip, the input voltage signal is transformed into a differential signal, and this signal is amplified a certain amount (depending on settings controlled by the FPGA). These output differential signals will be transferred to the differential ADCs on a separate board. The reason these signals have been amplified and made differential is for increased resolution and minimization of noise on the signal. These signals will be much more easily interpreted in the process.

Based on the following Equation 5.2, the voltage multiplier can be calculated based on the logic input from the FPGA. Ranging from logic 000000 to 111111, the amplifier multiplier can range from 4.5 to 20.25 dB, which multiplies the voltage anywhere from 1.69 to 10.59 times the input value. There are 64 unique multiplier values for voltage, between 1.67 and 10.59 times the original input value. However, it is important to stay within the range of the chip. The differential input can vary 3.6V peak-to-peak and the differential output can vary 6V peak-to-peak. The "Results" section describes the functionality more which is accompanied by test results.

$$G_{dB} = 20 * log(\frac{V_1}{V_0}) \tag{5.2}$$

Shown in the Table 5.5, the Logic Values each are designated with a specific Gain Code. Each gain code has a respective Amplifier Multiplier, which then translates to a Voltage Multiplier.

Based on the various input Logic Values into the AD8366 (using parallel programming mode), the output voltages will be amplified some amount larger than the input. These output

Logic Value (Parallel Programming mode)	Gain Code	Amplifier Multiplier (dB)	Voltage Multiplier
000000	0	4.5	1.67
000001	1	4.75	1.73
000010	2	5.0	1.78
000011	3	5.25	1.83
...	...	...	...
111101	62	19.75	9.72
111110	63	20.0	9.72
111111	64	20.25	10.59

Table 5.5: Amplifier values based on Parallel Programming

voltages will then be transferred to the ADCs on the next board, and further passed down eventually to be interpreted by the FPGA.

The voltage and current sensing boards are key to the functionality and proper monitoring of the entire inverter system. These two boards are located at the lower levels of the inverter hierarchy, but provide data for the FPGA in order for the inverter to have the ability to constantly monitor functionality. As the data from the voltage and sensing boards is monitored and captured, it will be passed up the hierarchy to the other boards, eventually reaching the FPGA.

5.3 IGBT Driver Link Board

This part of the circuit is designed to control the Insulated Gate Bipolar Transistor (IGBT) switches. These switches make up the core of the inverter, since they allow us to switch the lines at high speeds to effectively change the frequency of the AC power passing through the inverter.

Due to design changes made late in the project, this board is still under development and requires more work.

5.4 DC Link Capacitor

The DC link capacitor (SBE Power Ring Film Capacitor – Part 700D10897-547) is a key component to the entire functionality of the inverter. The DC link capacitor stores energy from the generator and acts as a DC rail for the IGBT's. The IGBT's pull power from this capacitor and switch the waveform to create synchronous three phase power at a specified frequency, in our case 60Hz. The DC link capacitor is simultaneously and continuously being charged (by the generator) and discharged (by the IGBT's). The usage of such a capacitor in an inverter system allows the generator(s) to constantly operate at the most efficient speed for any load, while the IGBT's in the inverter maintain the required power quality (output and frequency) required by the load devices. A diagram of the capacitor is shown below in the Figure 5.28 and the mechanical specifications are shown in Figure 5.29.

The inverter is based around new technology implemented in the SBE Power Ring Film Capacitor. This design wasn't feasible just a few years ago when capacitor's with the electrical properties of the SBE 700D10897-547 didn't exist. This specific capacitor was chosen for several reasons.

This capacitor is relatively high voltage (700V) with a high capacitance (1000uF). Additionally, it can be pulsed to higher voltages (900V) for short periods of time to increase power

Figure 5.28: DC Link Capacitor diagram

density. The energy stored on a capacitor is equivalent to Equation 5.3.

$$E = \frac{1}{2} * C * V^2 \tag{5.3}$$

Based on the values that this capacitor is rated for, upwards of 400J of energy can and will be stored in the capacitor during operation.

Another reason that this capacitor was chosen was because of its low inductance. Currently, this capacitor is among the lowest inductance capacitors on the market. The reason that a low inductance capacitor is necessary is because it is being used on a system that is already quite inductive. By adding almost no inductance, the power factor will remain unaffected by the addition of large capacitor on the system. Lastly, and potentially most importantly, the usage of a low inductance capacitor allows for near instantaneous transfer of power between the capacitor and IGBTs. This is especially important for our application because power needs to be transferred almost instantaneously into and out of the capacitor as needed by the load.

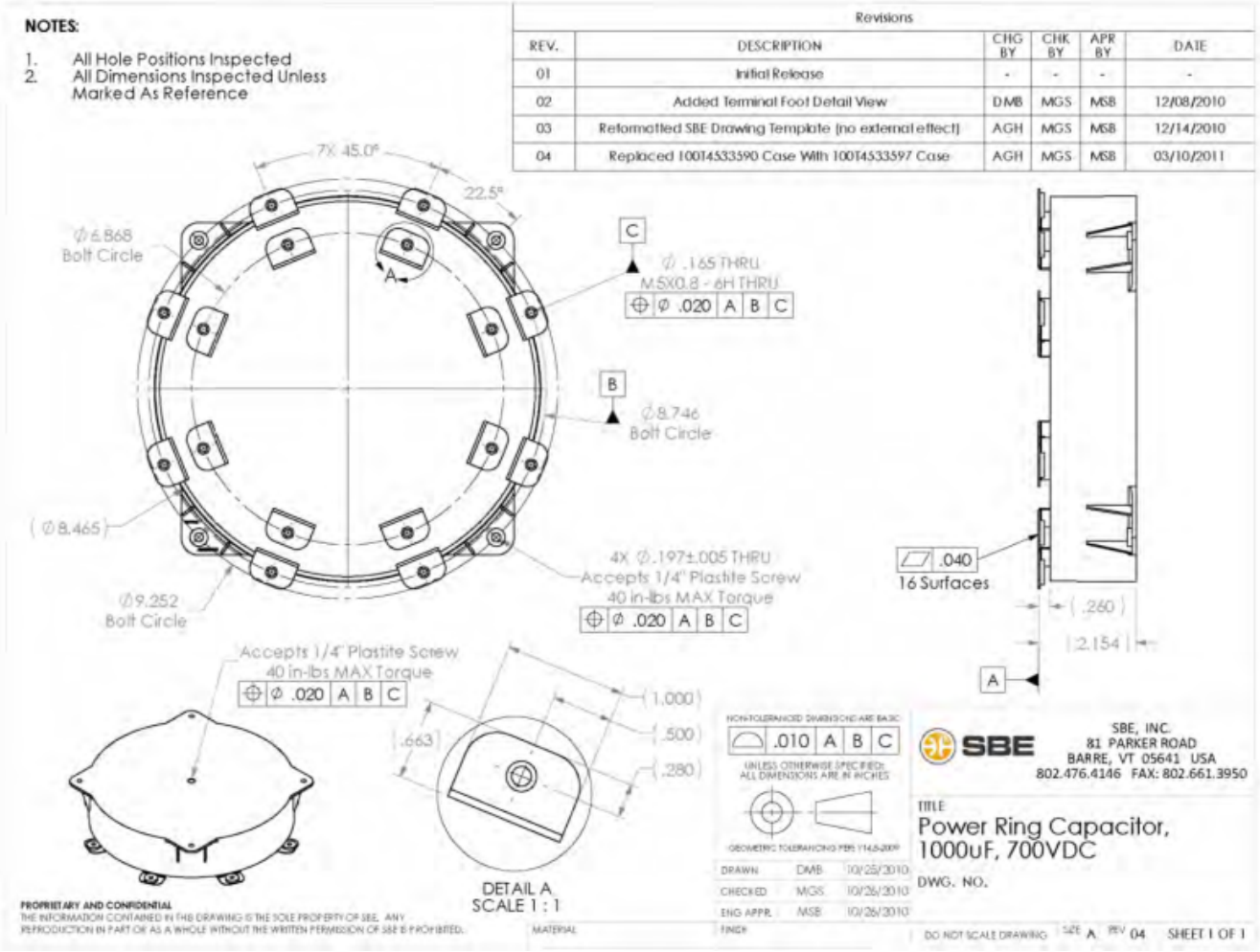


Figure 5.29: DC Link Capacitor Mechanical Layout

5.5 Flyback Transformer - "Pre-Charge Circuit"

The purpose of the flyback transformer circuit is to pre-charge the capacitor up to operational voltage, prior to the rest of the inverter being turned on, in order to prevent large in-rush current (10,000A) and malfunction. The power ring capacitor has very low inductance, <5 nH. If it is not charged when the inverter is first switched on, it will act like a short circuit and create a large current surge. This inrush current, on the order of a 10,000A surge, is large enough to blow the main fuses in the system. Therefore, to protect the inverter, a sub-circuit is needed to pre-charge the capacitor before operation. A flyback converter, originally derived from the buck-boost converter, was chosen for this purpose. We chose a flyback converter circuit because it is relatively simple in its design, only requiring four components: a switch, a transformer, a diode and a capacitor. Our design started with just four components and evolved over the course of the project; the final schematic is shown in Figure 5.30. The design requirements for this circuit are to charge the 1000µF DC link Capacitor (SBE Power Ring Film Capacitor – Part 700D10897-547) up to 700+ Volts in less than 10 seconds.

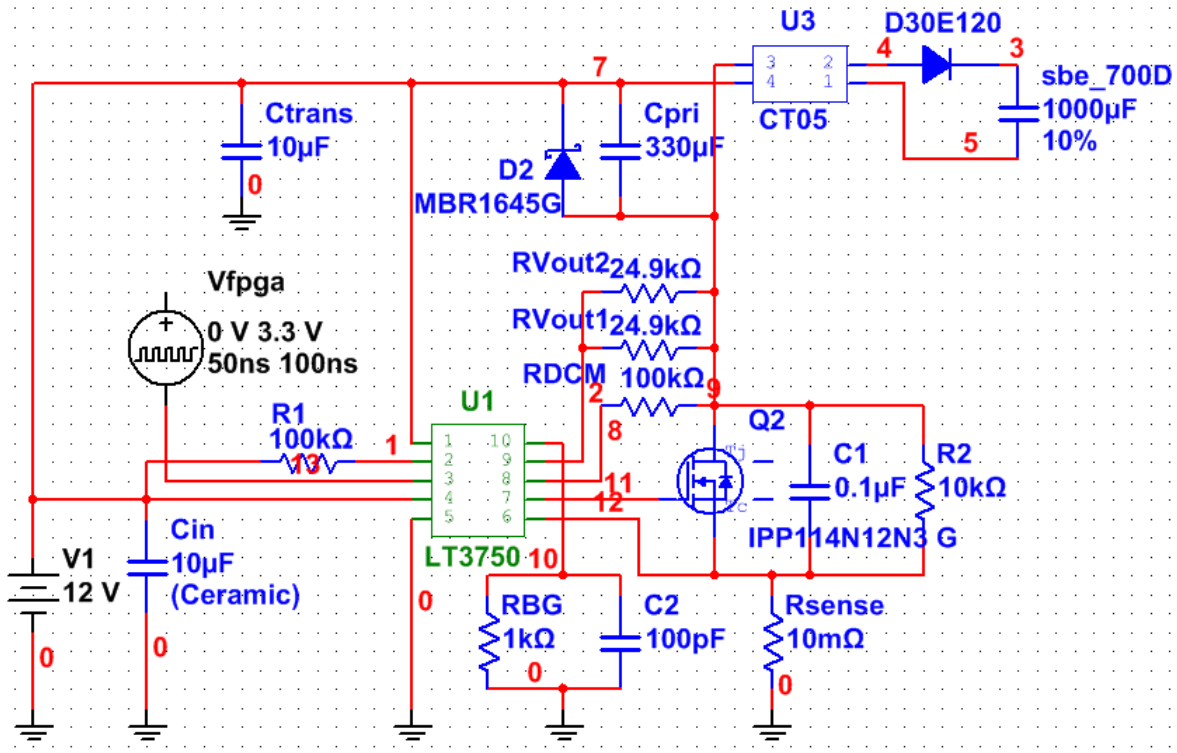


Figure 5.30: Capacitor Pre-Charge Circuit

5.5.1 LT3750

The LT3750 Capacitor Charger Controller microchip produced by Linear Technologies in used in our design. The LT3750 was chosen for the following reasons:

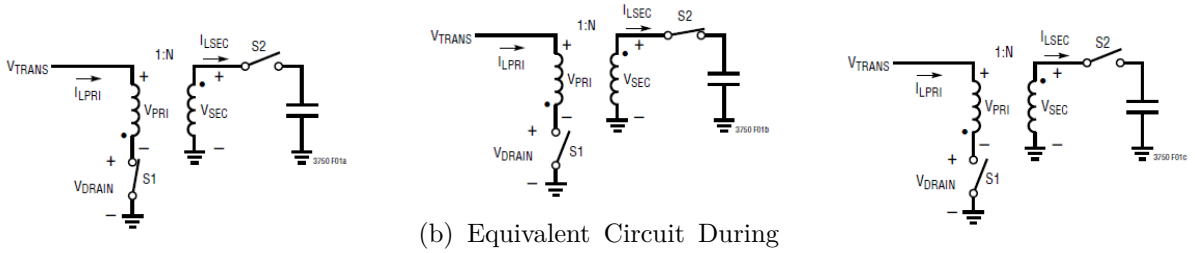
- LT3750 can charge large capacitors quickly; fits with our design requirements
- LT3750 has a wide input range: 3-24V; Inverter uses 3.3V logic and has 12V supply rails
- LT3750 comes in the small 10-lead MS package; smaller size is better as there is limited available board space for the pre-charge circuit
- LT3750 accurately charges to a specific output voltage which is easily adjustable by two resistors
- LT3750 drives Gate output to Vcc - 2V; initial testing determined that the switch would need additional voltage driving circuitry for optimal switching
- LT3750 has primary-side sensing so no output voltage divider circuit is needed

The LT3750 has four operational states.

1. Start up occurs for 20μs during which a one shot enables the master latch and turns on the NMOS. The master latch will remain enabled until the target output voltage is reached or a fault condition occurs.
2. Primary-side charging (Figure 5.31a) occurs when the NMOS latch is set. The gate driver pin charges to Vcc - 2V turning the external NMOS ON. Current rises linearly in the transformer and the diode is reverse biased. Energy is stored in the transformer core.

3. Secondary energy transfer (Figure 5.31b) occurs when the current limit is reached and the NMOS resets. The diode forward biases and stored energy flows into the output capacitor. If the voltage limit Vout is reached the master is reset and the Done pin goes low, otherwise the final state occurs.

4. Discontinuous mode detection (Figure 5.31c) occurs while the LT3750 waits for the drain of the NMOS to ring down below Vtrans + 36mV, at this point the NMOS latch resets and a new charging cycle begins.



(a) Equivalent Circuit During Primary-Side Charging

(b) Equivalent Circuit During Secondary Energy Transfer and Output Detection

(c) Equivalent Circuit During Discontinuous Mode Detection

Figure 5.31: States of Flyback Converter

5.5.2 Voltage Source

The DC link capacitor needs to be charged up to several hundreds of volts from a low powered circuit. Our pre-charge circuit will run off of a 12V battery supplied by the customer. These batteries are extremely common and every ship with a genset on-board already has such a battery.

5.5.3 Transformer

The selected transformer is the CT05-050 from ICE Components. This transformer was selected because:

- CT05-050 has a high turns ratio N, 50:1; allowing transformation to higher voltages
- CT05-050 is electrically tested and rated to 4,000 Volts
- CT05-050 was designed for DC/DC and AC/AC applications
- CT05-050 has a small package size: 17mm by 15mm by 12mm

5.5.4 Bypass Capacitors

Several bypass capacitors are used in this circuit design. Bypass capacitors are used to decouple various parts of an electrical network from each other. Their primary use is to:

- Prevent AC signals from propagation on DC power lines
- Prevent switching from one section of a circuit from negatively effecting other components
- Prevent voltage spikes throughout the circuit
- Reduce noise experienced in circuit

Capacitor selection and sizing was performed based off of the recommendations given in the datasheet for the LT3750 (Appendix B). C_{Trans} is at pin 1 of the LT3750. C_{Pri} is to be as close to the transformer as possible and is to prevent voltage spikes. C_{In} is at pin 4 of the LT3750. C1 is part of a snubber circuit to protect the external NMOS switch. C2 is parallel to the RBG resistor.

5.5.5 Resistors

Resistor selection is based off of the design requirements and recommendation within the LT750 datasheet (Appendix B). R1 = 100kΩ; is a pull-up resistor on pin 2 of the LT3750. R_{Sense} = 10mΩ; is used to find the output voltage on the capacitor and determines the current limit of the LT3750. The current is 78mV/R_{Sense} which gives a current limit of 7.8A. R_{CDM} = 100kΩ; is used in Discontinuous Mode Detection. R2 = 10k Ω; is part of a snubber circuit to protect the external NMOS switch. R_{BG} is used along with R_{Vout1} and R_{Vout2} to determine the output voltage limit. The output voltage is set using Equation 5.4. For the desired output of 700+ Volts, we substitute the values in Equation 5.5. Solving for the ratio of the two resistors, we obtain Equation 5.6.

$$V_{\text{Out}} = (1.24V * \frac{R_{\text{Vout}}}{R_{\text{BG}}} * N) - V_{\text{Diode}} \tag{5.4}$$

$$700V \leq (1.24V * \frac{R_{\text{Vout}}}{R_{\text{BG}}} * 50) - 2.15V \tag{5.5}$$

$$R_{\text{Vout}} \geq 11.26 * R_{\text{BG}}. \tag{5.6}$$

Additionally the LT3750 datasheet specifies $R_{BG} \leq$ 2.5kΩ. Therefore, R_{BG} was chosen to be 1.0kΩ.

A higher power version of the inverter may be offered using a SBE power ring capacitor rated up to 1500V with the same footprint and physical dimensions as the SBE 700D10897-547 for the DC link capacitor. To accommodate this need, two output resistors were selected: R_{Vout1} and R_{Vout2}. Both resistors have the value 24.9kΩ. The parallel combination of the two output resistors will have a value, $R_{Vout1}||R_{Vout2}$ = 12.45kΩ. Using 5.4, the pre-charge circuit can charge the DC link capacitor up to 770V for lower voltage applications. The higher power version of the inverter will only use one output resistor. Using 5.4, the pre-charge circuit can charge the DC link capacitor up to 1540V for higher voltage applications.

5.5.6 FPGA Control

The FPGA is connected to the LT3750 at pin 3, the Charge pin. This pin controls the operation of the LT3750 chip. To enable, it must be driven above 1.1V and to disable driven below 0.2V. The FPGA operates at 0-3.3V logic which is compatible with this chip. For proper functioning, the FPGA input signal must rate at a rate ≥1V/µS. The FPGA ramps well above this so it is not a concern.

The LT3750 can send a signal, via pin 2 (DONE) to indicate that the capacitor is fully charged. This signal would indicate that the inverter can now begin operation as no short circuit current pulses should occur. However this feature won't be used as the voltage on the capacitor is already being monitored by the Voltage Sensing Board Sec 5.1. Pin 2 is left unconnected in the design.

5.5.7 Diodes

There are two diodes used in the circuit, they are used to control the flow of current. A diode has low resistance to current in one direction, with high resistance in the other direction, limiting the current flow to one direction. Their usage provides protection of electrical devices and ensures the circuit to work as expected.

On the primary side of the transformer, the MBR1645G diode is used across the transformer terminals. The MBR1645G diode was chosen because this diode is able to handle high currents (up to 150A peak) at lower voltages (45V), see Appendix B. On the primary side of the transformer, there will be about 12V used from the customer(s) battery, and higher current levels. This diode will limit the current flow to one direction, while adequately handling the current (up to 16A continously) in the forward direction.

On the secondary side of the transformer, a diode is used in series with the capacitor. The diode on the secondary side of the transformer is used to ensure that the capacitor is able to charge. If there was no diode in place, the output from the transformer (which is a sinusoidal waveform) would charge and discharge the capacitor with each positive and negative pulse of voltage. The placement of the diode acts as a rectifier to create a single positive wave for each cycle, which allows the capacitor to charge and its voltage to rise.

For our design, the Infineon IDP30E120 diode was chosen. This diode was chose because:

- IDP30E120 is capable of handling high voltages and currents so it is good for this application.
- IDP30E120 can handle up to 1200V.
- IDP30E120 is a fast switching diode, that can switch at speeds up to 4MHz.

In the higher power model of the inverter, where the DC link capacitor could be charged to above 1200V a new diode must be selected. The IDP30E120 diode would have to be changed to another fast switching diode with a higher voltage rating. Additionally, for any speed application above 4MHz, a faster switching diode should be chosen.

5.5.8 MOSFET

The MOSFET of the circuit is a key component to the correct operation of the flyback transformer. Since this design uses a customer supplied DC voltage battery as a power source, a MOSFET is certainly needed. A DC voltage source is inadequate to use with a transformer. Transformer design, and the principles in which they operate (electromagnetic induction, varying magnetic flux), require AC voltage to function. The MOSFET in the circuit converts the constant DC voltage source to an AC voltage source. Switching on and off, connecting and disconnecting the voltage supply, it creates a pulse, or an AC voltage signal, through its switching. With the AC voltage signal, the transformer is able to operate.

The MOSFET controls the flow of power into the transformer and the maximum output voltage via the duty cycle, D. The duty cycle is a key determinant on the output voltage as a function of input voltage, duty cycle and turns ratio. The following Equation 5.7 shows this relationship.

$$V_0 = \frac{D * V_{cc}}{1 - D} * \frac{N_2}{N_1} \tag{5.7}$$

Using Equation 5.7, we can determine the necessary duty cycle of the MOSFET and turns ratio of the transformer to create a 700V output voltage level from a 12V battery source. For every duty cycle, it can be expected to alter the voltage levels from the original based on the

percentage of time high or low. This is shown in the second column. Based on this voltage gain, the turns ratio of the transformer will need to be responsible for the remainder of the voltage gain. This calculated turns ratio is shown in the third column. This information shown in Table 5.6.

Duty Cycle	Voltage Gain	Turns ratio required (N2/N1)
0.1	0.111	525
0.2	0.250	233
0.3	0.429	136
0.4	0.667	88
0.5	1.00	58
0.6	1.50	39
0.7	2.33	25
0.8	4.00	15
0.9	9.00	6.5
0.95	19.00	3.07
0.96	24.00	2.43
0.97	32.33	1.80
0.98	49.00	1.19
0.99	99.00	0.589

Table 5.6: Relationship between duty cycle, voltage gain and turns ratio to reach 700V with 12V source

There are many combinations of duty cycle and turns ratio in order to reach an output voltage of 700V. However, we are limited by the available selection of current transformers and the turns ratios they utilize. For this prototype, the CT05-050 current transformer with a turns ratio of 50:1 was chosen. The necessary duty cycle is found with Equation 5.7 which gives a duty cycle of approximately 54%. This combination allowed the 50:1 current transformer to be used, with a 54% duty cycle, in order to create a flyback transformer that would convert a 12V source to a 700V output.

For this design, the Infineon OptiMOS 3 Power Transistor (IPP114N12N3 G) MOSFET was chosen. This MOSFET was chosen because of its ability to deal with high voltage spikes (which will hopefully be reduced with a snubber circuit), high current levels, and ability to switch at high frequencies.

5.5.9 Snubber Circuit

The snubber circuit component of our larger flyback circuit is used for protection. The MOSFET will be switching at high speeds which will therefore put it through a tremendous amount of electrical stress. The MOSFET is used to continuously open and close the circuit in order for the larger flyback circuit to work correctly. In order to eliminate some of this stress, a snubber circuit is used in parallel with the MOSFET. As previously discussed, a snubber circuit consists of a capacitor and a resistor. The values of these devices are not easily calculated, so they must be manually tested for effectiveness. This will depend on the final MOSFET chosen and the voltage/current levels.

The usage of this snubber circuit will reduce voltage and current spikes in the system, stabilizing the levels at the MOSFET. Using a snubber circuit will reduce stress on the switching

component and increase MOSFET lifetime. This increases the circuits reliability by reducing the chance of and time between failures.

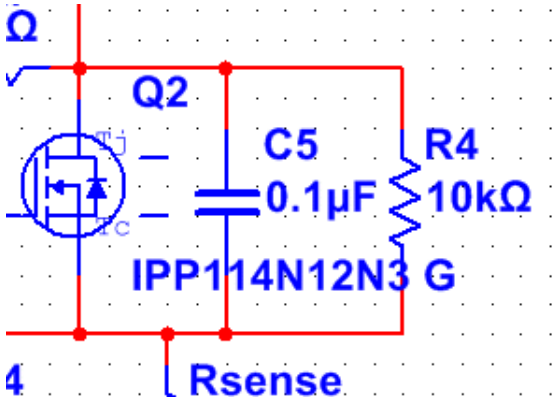


Figure 5.32: RC Snubber Circuit protecting MOSFET

5.5.10 Voltage Divider

The voltage divider described in this section, is not formally in the Pre-Charge Circuit. The voltage divider in parallel with the capacitor has a very specific purpose. This circuit is a necessary safety precaution and useful during testing of the Pre-Charge Circuit. In testing, this voltage divider will act as a "bleeder" resistance and therefore discharge the capacitor to a safe voltage over time. Otherwise, the capacitor will remain charged and represents a safety hazard due to it's energy density and potential power output. Although the voltage divider is not technically in this circuit, it represents the voltage divider on the Voltage Sensing Board. With a connection to the Voltage Sensing Board, the voltage will be able to be constantly monitored on the capacitor (at a safe level after going through a voltage divider). An example of the what the voltage divider circuit could look like is shown in Figure 5.33.

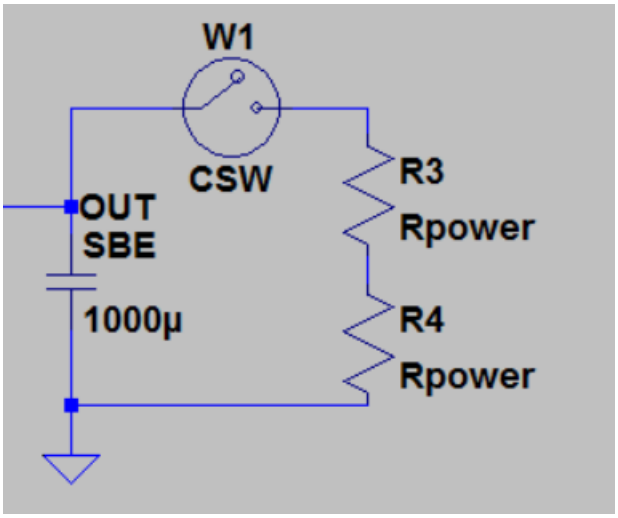


Figure 5.33: Potential circuit for power 'bleeding' voltage divider

5.6 UMIC Communications

Each layer of the inverter will contain a Xilinx Spartan 6 FPGA as well as a PowerPC co-processor on NI's sbRIO 9606 control board. The additional processing power offered by using one FPGA per layer instead of one for the entire system will allow the system to be highly expandable and reconfigurable. Each UMIC can have another UMIC stacked on top to form layers, this allows for more power to be handled by the inverter. Every sbRIO needs to communicate to many devices in its own layer as well as sbRIO's in other layers. In order to communicate without the data getting distorted from noise, all signals are run through differential line drivers. A differential line driver works by splitting one data line into two lines (a "differential pair"). Each split pair is driven opposite of each other, one high and one low, depending on the input signal. A differential receiver compares the two signals to recreate the initial input. Any noise induced on the lines will be approximately the same amplitude and phase which means the receiver can subtract it out, see Figure 5.34. Not shown in Figure 5.34 are the load resistors that are in parallel with the differential pair output. These resistors are used to properly load down the output and ensure correct signaling, see Appendix D

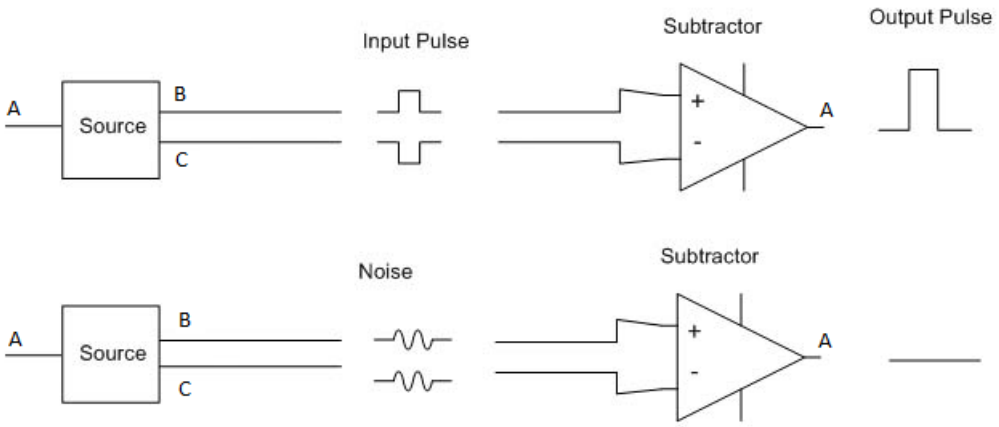


Figure 5.34: Example of differential pair signaling

5.6.1 Backplane Connectors

Each layer can communicate to the one above or below it through a 192 pin molex connector. 37 data lines need to travel though the connector, which will take up 74 pins. The SN75LBC170 is a three channel differential transceiver which means it can transmit differential pair signals and receive from a differential pair depending on how you configure the chip. Each individual channel can be set to receive or send data which is set by a "direction" pin on the chip, see Figure 5.35. Instead of wiring each individual "direction" pin to the FGPA, they are controlled via a shift register. Texas Instrument's SN74HC595 is an 8 channel shift register that only needs 4 pins connected to the FPGA in order to control all 37 "direction" pins.

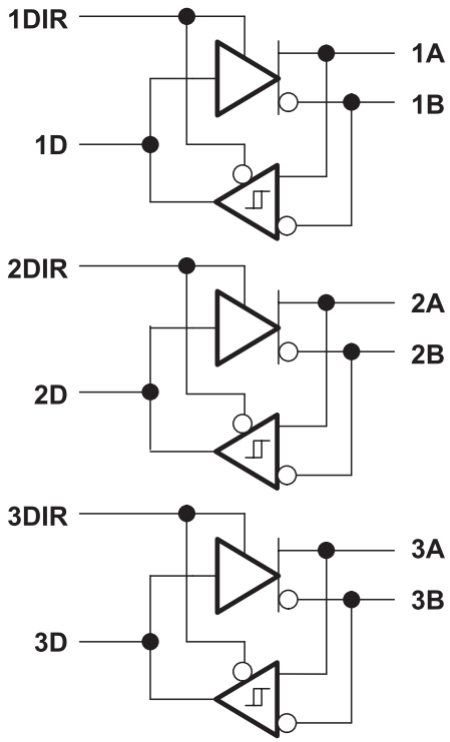


Figure 5.35: Logic Diagram of the SN75LBC170

5.6.2 Positive/Negative Side Boards

Every power module has a positive side board and a negative side board PCB. The positive side board routes signals from the IGBT platform board to the capacitor Pre-Charger, AVAGO isolator, as well as the positive side DC current sense board through a VGA controller. The negative side board controlls the negative side DC current sense board in the same manner but does not have the Pre-Charge circuit or isolators. In total, the side boards need 11 signals routed as a differential pair. These signals are also processed through differential line drivers on the IGBT platform board.

Chapter 6

Results

6.1 Voltage Sensing Board

6.1.1 Basic Functionality - DC

The first test that was completed for the Voltage Sensing circuit was a basic functionality test. After designing and prototyping this board, it is important that it works correctly and can calculate and send the voltage signals on down the board. The first functionality test performed was the DC voltage test.

For this test, the input voltage to the circuit was between 1 and 30V, although this does not necessarily matter. The voltage divider is what matters, and will change dramatically depending on the customer system. The voltage divider will determine what percentage of this voltage actually reaches the AVAGO chip, which for all cases should be ±200mV. The voltage divider proportions should adjust accordingly. For this particular test, the R1 resistor was a 510kΩ resistor. The R2 resistor was the potentiometer, whose value was fixed (for this test) at 5000Ω. Therefore, the voltage range of 1 to 30V was roughly 0.009V to 0.290V into the AVAGO chip. Table 6.1 below shows the test results and the measurements of each differential output, and the calculated voltage on the output.

Input Voltage (V)	Voltage into AVAGO (after divider) (mV)	Positive Output Voltage (V)	Negative Output Voltage (V)	Theoretical Voltage with Gain (8.2x)(V)	Calculated Voltage Level (Positive - Negative)(V)
1	8	1.28	1.20	0.064	0.08
5	40	1.41	1.07	0.328	0.34
10	81	1.58	0.91	0.6642	0.67
15	121	1.74	0.74	0.9922	1.0
20	161	1.91	0.576	1.3202	1.334
25	202	2.07	0.405	1.656	1.665
30	234	2.22	0.231	1.902	1.989

Table 6.1: Lab Results for Basic DC Functionality Testing

This simple test proves that the circuit functions as designed. Based on the input voltage, the voltage divider scales the voltage to about 0.9% (based on the resistor proportions). The

second column shows that the voltage into the AVAGO is correctly scaled and this part of the circuit works. The next two columns show the measurements of the differential output from the AVAGO chip (pins 7 and 6, positive and negative outputs respectively). The fifth column shows what the output voltage should be, based on the voltage into the AVAGO and the advertised gain of the chip. This number matches up almost identically with the last column, which is the output voltage signal after being differentiated. This simple test shows that the circuit will work for DC voltages and measurements.

6.1.2 AC Functionality Tests and BODE Plots

The next test that was done with the Voltage Sensing Circuit was a BODE plot to test for attenuation and phase shift with different frequencies between the input and output signals. For this particular test, the bypass capacitors were removed so they would not act as a lowpass filter, and block the higher frequencies which were being tested.

For this test, the following characteristics were used:

- Sinusoidal waveform input signal (4V peak to peak, centered at 0V)
- The oscilloscope probes were both set at 10X attenuation
- Oscillopscope was set to DC coupling with High Z Impendance
- The voltage divider had R1 = 51kΩ and R2 (potentiometer) = 5kΩ
- The DC offset (of 1.23V of the AVAGO chip) was ignored and canceled because the oscilloscope probes were connected to positive and negative inputs (canceling it)
- Bypass capacitors removed for testing of higher frequency because these caps attenuate the signal after 67 Hz.

With these exact settings, an input signal was added to the Voltage Sensing Board where the customer electrical system would normally be. The results were measured and/or calculated in the Table 6.2.

For all circumstances, except 1 Hz (when the input voltage could not reach the set peak to peak value), the output voltage was slightly higher (with gain subtracted) than the input signal. This could be due to error or just because the gain of the AVAGO chip (#630-ACPL-C79B-000E) can range from 8.16 to 8.24 V/V (±0.5%). However, because we are using this particular model AVAGO chip, there should be very little variation of gain between frequencies. Because of this, there is most likely a small amount of attenuation between the input and output signals. To compare these values, it is important to compare the peak to peak voltages of the input to the AVAGO and the peak to peak voltages of the output. These values should be almost identical because they are the same signal, just separated by the AVAGO Opto-Isolator. Once the gain is calculated out, these values should be nearly identical. The BODE plots created from the above data from the above Table 6.2 are compared below to the BODE plots (Figure 6.1 and Figure 6.2) provided from the AVAGO Opto-Isolator data sheets.

These BODE plot tests were tested for up to 100,000 Hz, compared to the data sheet which tested up to 1,000,000 Hz. The reason this test stopped at 100,000 Hz is because there are no applications which this inverter will be used up to this frequency. Clearly, the trends are similar for each of the graphs which helps prove that this design of the prototype for the Voltage Sensing Board will be able to handle high frequencies (typically much higher than it will ever see). Up to 100,000 Hz, there will not be extreme amounts of signal attenuation or phase shift.

Voltage Input Amplitude pk-pk (V)	Voltage Input to AVAGO Amplitude pk-pk (V)	Frequency (Hz)	Voltage Output Amplitude pk-pk (V)	Voltage Amplitude Without Gain (8.2x)(V)	Attenuation (% difference between input and output)	Phase Shift between Input to AVAGO and output voltage (degrees)
3.00	0.172	1.0	0.960	0.117073	46.91688	0
4.20	0.308	10	2.62	0.319512	-3.60299	0
4.12	0.304	100	2.58	0.314624	-3.3798	0
4.12	0.304	1000	2.62	0.319512	-4.8549	0
4.20	0.316	10,000	2.62	0.319512	-1.09918	-3.6
4.20	0.312	20,000	2.60	0.317073	-1.59995	-8.64
4.20	0.308	30,000	2.60	0.317073	-2.86149	-15.12
4.24	0.308	40,000	2.60	0.317073	-2.86149	-21.60
4.24	0.308	50,000	2.60	0.317073	-2.86149	-24.30
4.24	0.308	60,000	2.62	0.319512	-3.60299	-24.84
4.24	0.308	70,000	2.62	0.319512	-3.60299	-31.50
4.24	0.304	80,000	2.60	0.317073	-4.12303	-36.00
4.24	0.300	90,000	2.60	0.317073	-5.38456	-42.12
4.24	0.300	100,000	2.60	0.317073	-5.38456	-46.80

Table 6.2: Lab Results for Basic DC Functionality Testing

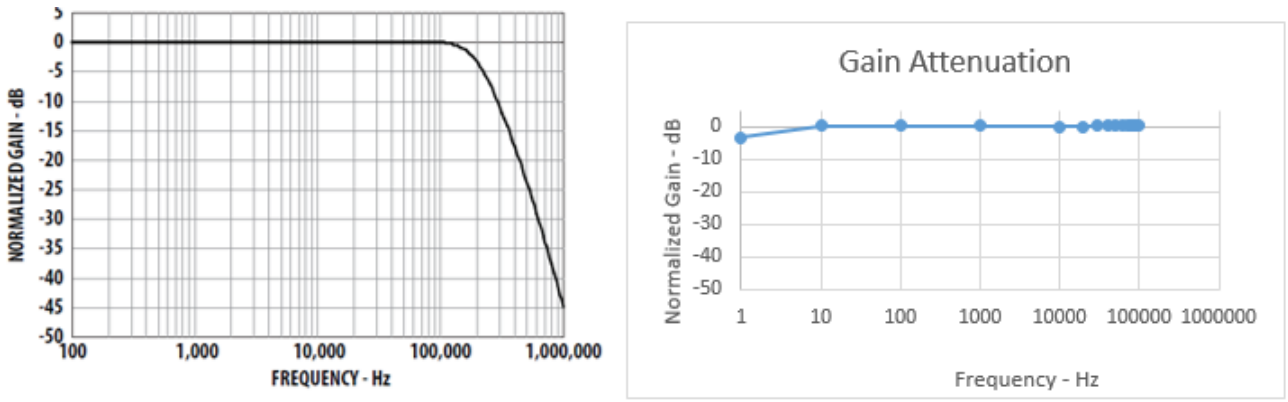
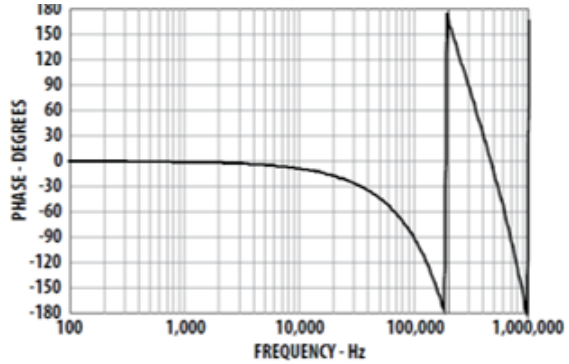


Figure 6.1: Gain Response for the AVAGO Opto-Isolator compared to Experiment Results



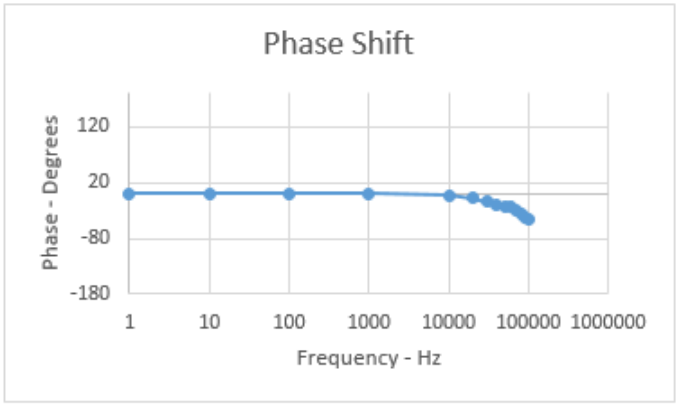


Figure 6.2: Phase Shift Response for the AVAGO Opto-Isolator compared to Experiment Results

6.2 Current Sensing Board

In order to test the Current Sensing board, the entire functionality revolves around the Analog Devices AD8366. Because there are two potential types of Current Sensors used in this project, a basic test for a single-ended and differential inputs have been done. A single-ended input provides a single voltage signal while grounding the other input pin. The differential input accepts two voltage signals, which helps in noise elimination.

This basic testing was done to ensure that the Analog Devices AD8366 chip operates as expected and described in the data sheet. A steady input voltage was applied to a channel on the AD8366. The gain was changed through various stages (chosen arbitrarily with a good spread) to cover all potential gains. This gain was changed using Parallel Programming mode and manually providing logic which would normally be supplied by the FPGA in the final inverter design. The output voltage was measured, and compared to the theoretical voltage (assuming a theoretical voltage gain). These values were compared and percent error was calculated.

The single-ended inputs were tested first followed by the differential inputs. Each was tested with both 0.5 and 1V inputs with the same applied gains (Gain Codes 0, 2, 4, 8, 16, 32, 34, 36, 40, and 64). The AD8366 datasheet (Appendix B) provides more information on these codes. For a good mix of values, 10 of the possible 64 gain combinations were tested.

The Theoretical Gain was calculated using the Equation 5.2.

6.2.1 Single Ended Input

This test is relevant for the L06S***S05 TAMURA Current Sensor with only a single ended input to the AD8366.

In order to test the single-ended input, using a WPI voltage supply (and potentially other power supplies), some small circuitry was needed in addition to the typical Current Sensing schematic. Due to the nature of the power supply; it can only provide current in one direction, and the voltage will be pulled up if connected to a higher potential (the AD8366 at 5V supply). Because of this, the voltage is pulled to equal the potential it is connected to, and it is impossible to test at lower voltages. In order to deal with this, for testing, a potentiometer was used to control the input voltage signal into the input pins. This potentiometer (three pin) was inserted in series with the voltage supply and ground, with the variable resistor connecting to the input pin on the AD8366. The test results for the Single-Ended Input to the AD8366 is shown in Table 6.3.

After analyzing the data, it is clear that the AD8366 functions correctly, but some more testing and fine tuning should be done. Based on these preliminary test results, the AD8366 operates as needed, but important conclusions must be considered. Error can be eliminated with further testing and PCB design. It appears from this testing that around 0.7V would be best to input to the AD8366 in order to have full range of gain, and better accuracy.

Before any data analysis is done, the Differential Input results will be shown and then both tests will be discussed.

6.2.2 Differential Input

This test is relevant for the L31S***05FS TAMURA Current Sensor with differential inputs into the AD8366.

In order to test the differential inputs, no additional circuitry was needed aside from the Current Sensing board schematic parts. The input voltages of 0.5V and 1V were tested with various gain amplifiers.

Input Voltage (V)	Programming Logic	Gain Code	Amplifier Multiplier (dB)	Theor. Voltage Gain	Theor. Output Voltage	Measured Output Voltage	Actual Voltage Gain	Percent Error (%)
0.5	000000	0	4.5	1.68	0.84	0.65	1.3	22.56
0.5	000010	2	5	1.78	0.88	0.72	1.43	19.58
0.5	000100	4	5.5	1.88	0.94	0.76	1.53	18.88
0.5	001000	8	6.5	2.11	1.06	0.85	1.71	19.18
0.5	010000	16	8.5	2.66	1.33	1.22	2.44	8.30
0.5	100000	32	12.5	4.22	2.11	1.66	3.32	21.27
0.5	100010	34	13	4.47	2.23	1.78	3.56	20.30
0.5	100100	36	13.5	4.73	2.37	1.89	3.78	20.11
0.5	101000	40	14.5	5.31	2.65	2.12	4.24	20.13
0.5	111111	64	20.5	10.59	Above Threshold	2.58	5.16	n/a
1.0	000000	0	4.5	1.68	1.68	1.65	1.65	1.72
1.0	000010	2	5	1.78	1.78	1.79	1.79	0.66
1.0	000100	4	5.5	1.88	1.88	1.92	1.92	1.93
1.0	001000	8	6.5	2.11	2.11	2.17	2.17	2.67
1.0	010000	16	8.5	2.66	2.66	2.63	2.63	1.15
1.0	100000	32	12.5	4.22	Above Threshold	2.81	n/a	n/a
1.0	100010	34	13	4.47	Above Threshold	2.81	n/a	n/a
1.0	100100	36	13.5	4.73	Above Threshold	2.81	n/a	n/a
1.0	101000	40	14.5	5.31	Above Threshold	2.81	n/a	n/a
1.0	11111	64	20.5	10.59	Above Threshold	2.81	n/a	n/a

Table 6.3: Lab Results for Basic Single-Ended Functionality Testing

The results for the Differential Input Basic Functionality Test is shown in Table 6.4. Some important conclusions can be drawn:

- When output voltage is saturated, it measures 2.7-3.0V, otherwise the output should be below this.

  Based on specifications of input and output differential voltage swings in datasheet (Appendix B). 3.6V peak-to-peak for Input Differential and 6V peak-to-peak for Output Differential.

- It is best to operate around 0.5V for full range of gain availability.

- Gain is too high at the halfway mark for 1V. It saturates the output and measures 2.81V regardless
- 2+V is too high for an input into the AD8366
- A voltage divider may need to be used to match the current input of the sensor.

Clearly, the conditions of this test were not ideal. More testing should be done, preferably on a PCB, in order to finalize functionality for the AD8366. Some sources of error include:

- Using a potentiometer that was not as exact, need more precise instruments for input voltage
- Problem with voltage supply described above, requiring adding additional circuitry for test purposes.
- Using on breadboard could add lots of noise, attenuation, etc.

Based on these preliminary test results, the AD8366 operates as needed, but important conclusions must be considered. Error can be eliminated with further testing and PCB design. It appears from this testing that around 0.7V would be best to input to the AD8366 in order to have full range of gain, and better accuracy.

Input Voltage (V)	Programming Logic	Gain Code	Amplifier Multiplier (dB)	Theor. Voltage Gain	Theor. Output Voltage	Measured Output Voltage	Actual Voltage Gain	Percent Error (%)
0.5	000000	0	4.5	1.68	0.84	0.96	1.92	14.37
0.5	000010	2	5	1.78	0.88	1.03	2.06	15.84
0.5	000100	4	5.5	1.88	0.94	1.18	2.36	25.29
0.5	001000	8	6.5	2.11	1.06	1.34	2.68	26.8
0.5	010000	16	8.5	2.66	1.33	1.67	3.34	25.5
0.5	100000	32	12.5	4.22	2.11	2.69	5.38	27.58
0.5	100010	34	13	4.47	2.23	2.81	5.62	25.82
0.5	100100	36	13.5	4.73	2.37	3.05	6.1	28.92
0.5	101000	40	14.5	5.31	2.65	3.43	6.86	29.22
0.5	111111	64	20.5	10.59	Above Threshold	2.91	n/a	n/a
1.0	000000	0	4.5	1.68	1.68	1.88	1.88	11.98
1.0	000010	2	5	1.78	1.78	2.10	2.10	18.09
1.0	000100	4	5.5	1.88	1.88	2.24	2.24	18.92
1.0	001000	8	6.5	2.11	2.11	2.59	2.59	22.55
1.0	010000	16	8.5	2.66	2.66	2.89	2.89	8.617
1.0	100000	32	12.5	4.22	Above Threshold	2.90	n/a	n/a
1.0	100010	34	13	4.47	Above Threshold	2.90	n/a	n/a
1.0	100100	36	13.5	4.73	Above Threshold	2.90	n/a	n/a
1.0	101000	40	14.5	5.31	Above Threshold	2.90	n/a	n/a
1.0	11111	64	20.5	10.59	Above Threshold	2.90	n/a	n/a

Table 6.4: Lab Results for Basic Single-Ended Functionality Testing

6.3 Pre-Charge Circuit

While complete construction and testing of the Pre-Charge Circuit is still underway, the following provides an update of the current state of the design.

6.3.1 PCB

A PCB layout of the Pre-Charge Circuit on the positive side layer interconnect board of the inverter was designed and is shown in Figure 6.3. Figure 6.4 is a 3D rendering of how the Pre-

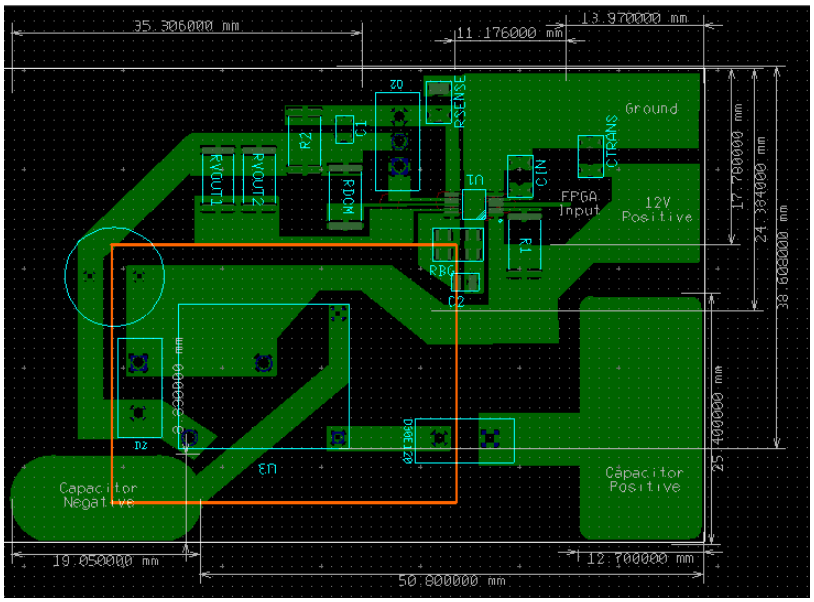


Figure 6.3: PCB Layout for Pre-Charge Circuit

Charge Circuit will look like once it is built. This image was generated using the 3D modeling tools available within the PCB design software Ultiboard 12.0.

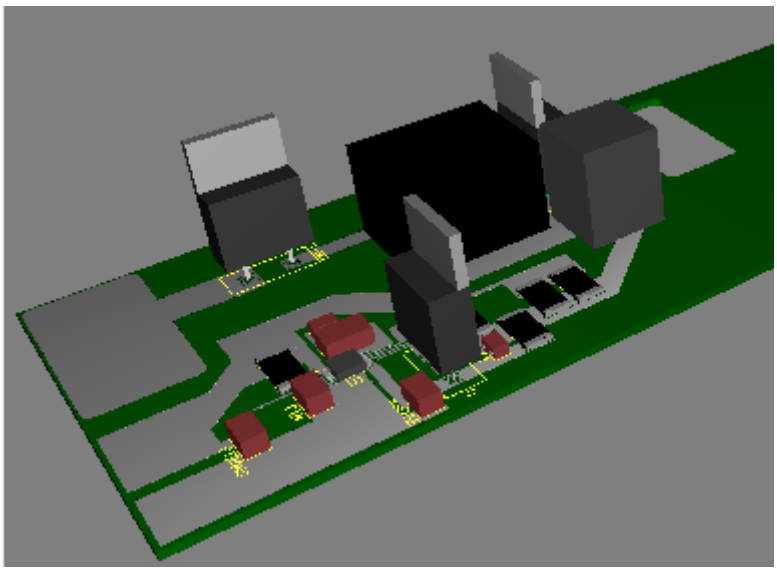


Figure 6.4: 3D rendering of Pre-Charge Circuit

6.3.2 Simulation

This circuit was simulated using LTSPICE IV from Linear Technologies to check functionality prior to physical testing. The circuit model for the LT3750 was provided from the Linear Technology website [7]. The circuit of Figure 6.5 is a modified version of the example capacitor charger provided with the LT3750 model from Linear Technologies. The following are positive aspects of this simulation:

- The transformer has been modified to represent the CT0-050 current transformer.
- The exact NMOS switch used in the pre-charge circuit (the IPP114N12N3 power transistor) existed in the LTSPICE database.
- All resistor values including the resistor ratio, R_{BG}:R_{vout} which controls output voltage, are accurate to the pre-charge circuit values.

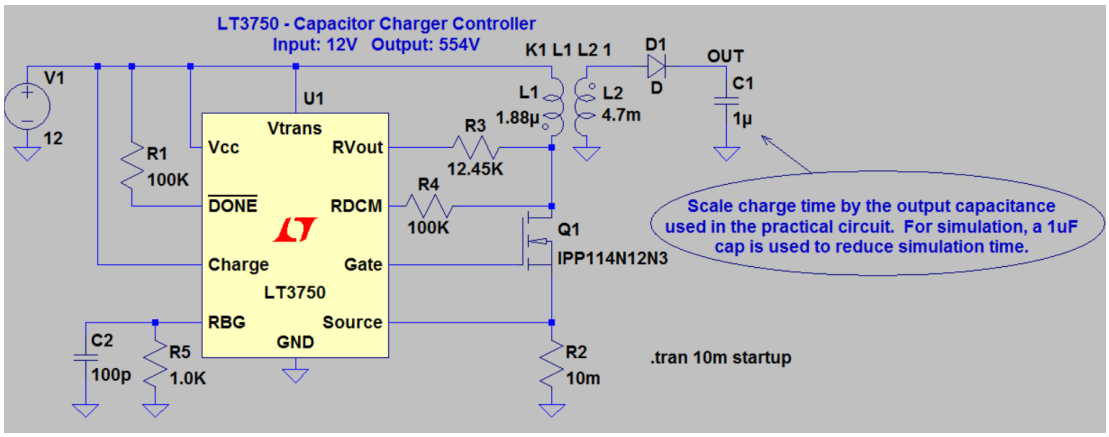


Figure 6.5: Circuit used for Simulation with LTSPICEIV

Figure 6.6 shows that the SBE capacitor can be charged from 0 to 554 volts in 10 seconds.

Note: to reduce required simulation run-time a 1µF capacitor is used on the output; the simulation runs for 10mS; expected charging time is the simulation time multiplied by the actual value of the output capacitor; for the SBE DC link capacitor, a scale of 1000; so actual charge time is 10 seconds.

Perfectly accurate simulations are time consuming and difficult to realize. As this simulation is only used to test the functionality of the pre-charge circuit prior to physical construction, an effective estimate is all that is required of it. Recognizing the drawbacks of this simulation: the output diode is considered ideal, the snubber circuit on the switch and the freewheeling diode of the transform are ignored, and the bypass capacitors are not included.

6.3.3 Testing

In order to test the Pre-Charge circuit a PCB was constructed. The manufacturer Osh Park was used to create the PCB, the result is shown in Figure 6.7.

In the inverter, the DC Link capacitor and 12V battery will have metallic terminals that will connect directly to the copper pads. For testing, loops of wire are soldered to these pads so that the capacitor and battery can be connected via alligator clips. This prevents the need to solder the capacitor and battery directly to the board. Additionally, connecting a control signal for the LT3750 (normally from the FPGA) directly would prove challenging and has the

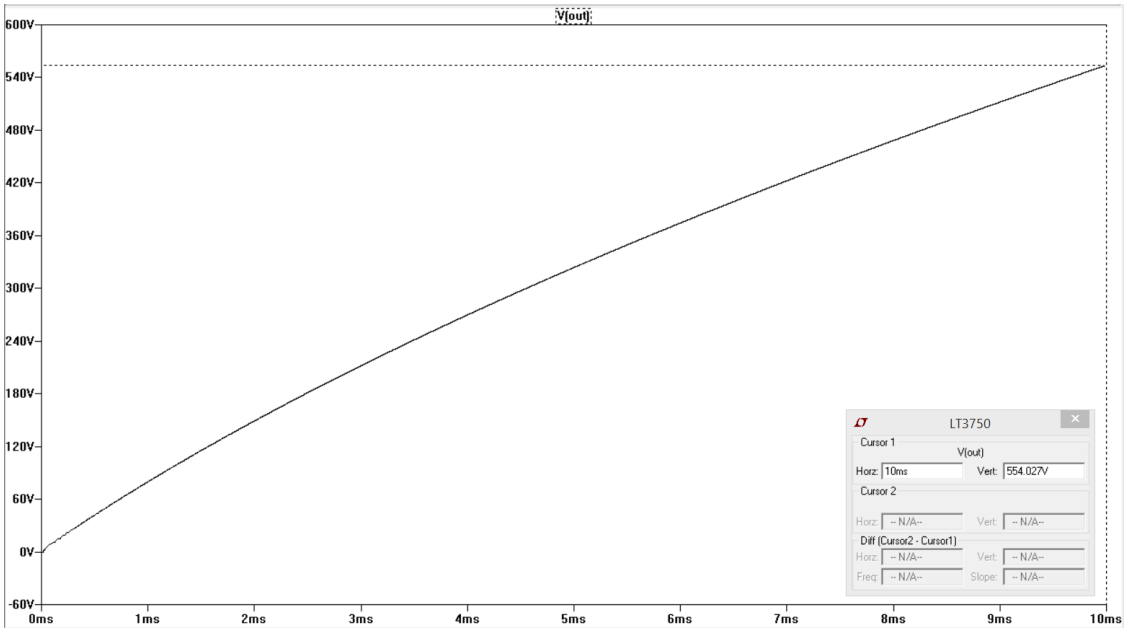


Figure 6.6: Charging characteristic curve

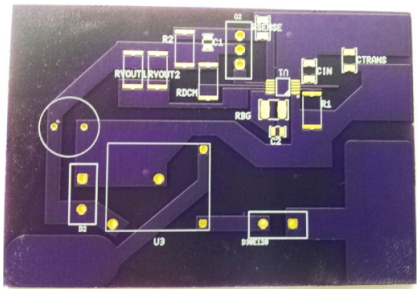
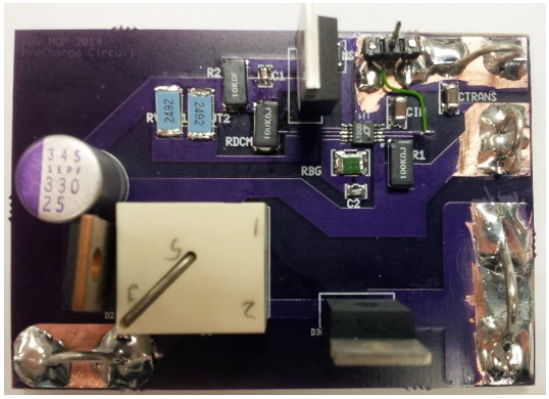
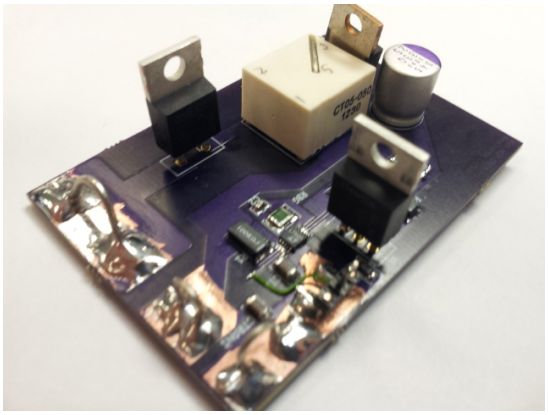


Figure 6.7: PCB as it arrived from Osh Park

potential to rip the copper pad off the board if the signal wire is accidentally tugged. Therefore the control signal for the LT3750 is connected, via a small wire, to a isolated pin soldered to the ground plane for stability. The finished product for testing is shown in Figures 6.8a and 6.8b



(a) Top View



(b) Isometric View

Figure 6.8: Pre-Charge Test Board

Unfortunately, due to time restrictions, there are no test results of the Pre-Charge Circuit in this report. During operation the DC Link capacitor may store over 400J of energy. Using the simulated charge voltage of 554V in ten seconds still provides over 150J of energy. This is a testing safety hazard as 150J could be potential lethal if it were to be dissipated very rapidly, such as shorting the terminals of the capacitor. Future testing needs to be done to validate the simulation results.

6.3.4 Thermal Modeling

The power lost in the OptiMOS IPP114N12N3 transistor is a combination of the thermal resistance of the package and the switching speed charging and discharging the internal capacitance. Maximum power power dissapaton in the TO220 package is $\approx$ 2 Watts. Internal resistance can be modeled as Figure 6.9.

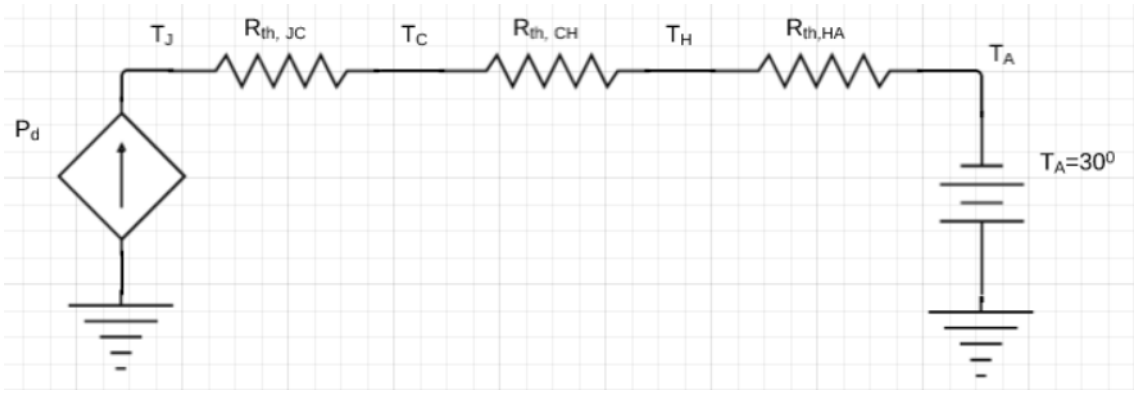


Figure 6.9: Thermal Model of heat flow in IPP114N12N3 Transistor

- T_A is the ambient temperature and is assumed to be 30°C inside the inverter.
- T_J is the junction temperature of the transistor $\leq$ 175°C.
- T_C is the case temperature of the transistor.
- T_H is the temperature of the heatsink (if used), $T_H \approx T_C$
- $T_{TH,JC}$ = 1.1°C/W; thermal resistance between the junction and case of the transistor.
- $T_{TH,JA}$ = 62°C/W; thermal resistance between the junction and ambient of the transistor. (no heatsink)

$$T_J = 175°C = 62°C/W * xWatts + T_A \tag{6.1}$$

$$P_d = I^2 * R_{\text{ds}} \tag{6.2}$$

Solving 6.1 for x yields 2.34 Watts that can be dissapated without a heatsink. The datasheet for the LT3750 gives 6.3 for calculating the average current in the external MOSFET. With $V_{out(pk)}$ = 1000V,, N = 50, V_{trans} = 12V power supply, and with a current limit of I_{pk} = 7.8A; Equation 6.3 yields $I_{AVG,M}$ = 2.44A.

$$I_{AVG,M} = (I_{pk} * V_{out(pk)})/(2(*V_{out(pk)} + N * V_{trans})) \tag{6.3}$$

Using the result from above and Equation 6.2, R_{ds} = 11.4mΩ (from the datasheet); the power dissipated in the transistor is: P_d = 0.0678 W. This is significantly less then the maximum allowable power dissipation, so no heatsink is likely required.

The other factor affecting power loss in the OptiMOS IPP114N12N3 transistor is switching speed. This loss is equivalent to the energy spent charging and discharging the internal capacitance of the transistor during each cycle. The power dissipated in charging internal capacitance is given in Equation 6.4. The datasheet of the IPP114N12N3 transistor gives the maximum $C_{internal}$ = 4310pF. The maximum voltage of the transistor is the driving gate voltage coming out of pin 7 of the LT3750. The LT3750's datasheet lists this value as V_{supply}-2. This makes the voltage ≈ 10.6 V for a typical fully charged 12V battery (batteries supply slightly higher voltages than specified as this value degrades over time). The #/cycles is 2; one charging, one discharging.

$$P_{diss} = (1/2) * C_{internal} * V_2 * (\#/cycles) * F_{SW} \tag{6.4}$$

Setting P_{diss} = No heatsink (P_d=2.34W) - the power dissipation (P_d=0.0678W) and solving Equation 6.4 for F_{SW} yields a maximum switching frequency of 4.7MHz. This is the maximum recommended speed the FPGA control signal can switch the pre-charge circuit at without the OptiMOS IPP114N12N3 transistor needing additional heat sinking.

Chapter 7

Conclusion & Recommendations

The original goal of this project was to build a working replica the UMIC at WPI. Although this wasn't achieved, the project provided a learning experience for all team members and pushed development of the TRL-7 inverter forwards. This was a constantly evolving and developing project. Over the course of this MQP during the weekly meetings with Father Joshua Resnick and Seraphim McGann of KEV we discussed the design of the inverter. These discussions prompted major design decisions such as:

- The use of a NI sbRIO-9606 on every module of the inverter.
- The removal of the Motherboard.
- The removal of the RF Isolators.
- The addition of Rogowski coils for precision measuring of the AC current output of the UMIC and for faster response time in case of any fault conditions.
- The potential for a higher power version of the UMIC with a higher operational voltage and larger DC Link capacitor.

Some of these design revisions made void certain aspects of the MQP's deliverables to the KeV team in Alaska, however without these discussions the project wouldn't have been pushed forwards.

7.1 Recommendations

Due to the constantly evolving nature of this project, there is ample opportunity to open this as a future MQP project. Through discussion with KeV we have created recommendations for changes to the design in order to improve the inverter's performance, modularity, or cost.

The first of these recommendations was the elimination of the GPIC. This board from NI was an expensive piece of hardware that was not being fully utilized by the project. By replicating the necessary pieces independently, we are saving money and not wasting valuable space inside the inverter enclosure.

We next reconfigured the placement of the ADC. The TRL-6 design used ADCs on the GPIC board, which meant that analog data from the sensors had to travel across the inverter from the sensors to the control board. By moving the ADCs as close to the sensors as possible, we reduce the possibility for analog noise to enter the signal lines. The digital lines then use differential signaling to prevent noise from corrupting the data.

7.1.1 Voltage Sensing

The Voltage Sensing Board has been tested and it's functionality confirmed. The voltage divider test shows that this board design accurately measures DC voltages. Additionally this board preformed well in the BODE plot test and will function with minimal attenuation and phase shift up to 100,000 Hz, the highest operational frequency of the UMIC. There are no recommendations for this board, it works as expected and intended.

7.1.2 Current Sensing

The Current Sensing Board has been tested and both the single ended input and differential pair functionality has been confirmed. Results from the single ended and differential testing indicate that 0.7V is the optimal input to the AD8366 in order to have full range of gain, and greatest accuracy. However, the test results were not ideal. Improvements for future testings include:

- Use a more precise potentiometer or other instrument on the input voltage
- Test on a PCB to eliminate noise and attenuation common with breadboards and non-soldered electrical connections.

7.1.3 Pre-Charge

- Simulation with LTSPICE IV show that the Pre-Charge Circuit should be able to charge the DC Link capacitor up to 554V in 10 seconds.

  This is not quite full operational voltage, but it will be enough to prevent the short circuit fault condition and damage to the UMIC.

- The MOSFET of the Pre-Charge Circuit does not need heatsinking as long as it is switched under 4.5MHz.
- If a higher power model of the UMIC is to be built only one Vout resistor is necessary.
- If a higher power model of the UMIC is to be built a new diode on the output side of the transformer with a voltage rating above the new operational voltage is necessary.

Bibliography

[1] Climate of alaska, . URL http://www.wrcc.dri.edu/narratives/ALASKA.htm.

[2] Alaska's fishing industry, . URL http://www.akrdc.org/issues/fisheries/overview.html.

[3] Comercial fisheries, . URL http://www.adfg.alaska.gov/index.cfm?adfg=fishingcommercial.main.

[4] Air station kodiak. URL http://www.globalsecurity.org/military/facility/kodiak.htm.

[5] Alaska. URL http://www.history.com/topics/us-states/alaska.

[6] Effects of diesel generator light loading. URL https://www.workspace-technology.com/blog/2011/02/27/effects-of-diesel-generator-light-load-running/.

[7] Lt3750 - capacitor charger controller. URL http://www.linear.com/product/LT3750.

[8] Turns out kodiak is largest u.s. island, depending on viewpoint. URL http://www.adn.com/2010/07/31/1389864/turns-out-kodiak-is-largest-us.html.

[9] Alaska, state & country quickfacts. URL http://quickfacts.census.gov/qfd/states/02000.html.

[10] *The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition*. Number 0-7381-2601-2. IEEE Press, 7 edition, 2000.

[11] *Power Electronics*. Number 0471226939. John Wiley & Sons, Inc., 3 edition, 2003.

[12] Joon-Hwan Lee; Seung-Hwan Lee; Seung-Ki Sul. Variable-speed engine generator with supercapacitor: Isolated power generation system and fuel efficiency. *Industry Applications, IEEE Transactions on*, 45(6), 2009.

Appendix A

Parts List

VOLTAGE SENSING BOARD

Item	Distributor	Distributor Part Number	Manufacturer	Manufacturer Part Number	Quantity	Cost Per Individual	Total Cost per parts
AVAGO Opto-isolator	Mouser	630-ACPL-C79B-000E	AVAGO Technologies	ACPL-C79B-000E	1	10.89	10.89
RECOM DC-DC Converter	Mouser	RK-0505S/H	RECOM	10001929	1	7.25	7.25
Fairchild Voltage Regulator	Mouser	512-LM7805CT	Fairchild	LM7805CT	1	0.459	0.46
2 Watt - 1Mohm 1% tolerance resistor	Mouser	71-ROX1-F-1M	Vishay	ROX1001M00FKLB	1	4.18	4.18
5K Potentiometer	Mouser	652-3214J-1-502E	Bourns	3214J-1-502E	1	2.65	2.65

0.1 and 0.047uF bypass capacitors	VARIOUS				2		0
Voltage supply					1		
Total Cost per board							25.43
CURRENT SENSING BOARD							
Item	**Distributor**	**Distributor Part Number**	**Manufacturer**	**Manufacturer Part Number**	**Quantity**	**Cost Per Individual**	**Total Cost per parts**
IC Dual Amp Voltage Gain Amplifier	Digikey	AD8366ACPZ-R7	Analog Devices	AD8366ACPZ-R7	1	13.42	13.42

Tamura Current Sensors (100A)	Pik Power	L31S100S05FS	Tamura	L31S100S05FS	1	17.73	17.73
Tamura Current Sensors(200A)	Pik Power	L31S200S05FS	Tamura	L31S200S05FS	1	18.82	18.82
Tamura Current Sensors (600A)	Pik Power	L06P600S05	Tamura	L06P600S05	1	17.39	17.39
10k Ohm - 1 Watt 1% Tolerance Resistors	Mouser	660-MF1DCT521R1002F		MF1DCT521R2001F	1	3.35	3.35
Various resistors and capacitors							
Voltage supply					1		
Total Cost per board							70.71

IGBT Platform Board

Item	Distributor	Distributor Part Number	Manufacturer	Manufacturer Part Number	Quantity	Cost Per Individual	Total Cost per parts
Triple Differential Transeciever	Verical	SN75LBC170DB	TI	SN75LBC170	16	5.78	92.48
8 Channel Shift Register	Mouser	595-SN74HC595DR	TI	SN74HC595	6	0.57	3.42
100 Ohm Resistor Array	Mouser	71-CRA06S-F-100	Vishay	CRA06S083100RFTA	12	0.11	1.32
High Density Connector RIO	Arrow	SEAM-40-03.0-S-06-2-A-KTR	Samtec	SEAM-40-03.0-S-06-2-A-KTR	1	32.7	32.7
PCIe Connector	Mouser	571-1-5145166-2	TE Connectivity	1-5145166-2	2	4.7	9.4
HD Mezz Plug	Heiland	MOL45802-1693	Molex	45802-1693	1		

Total Cost per board							139.32
Pre-Charge Circuit							
Item	**Distributor**	**Distributor Part Number**	**Manufacturer**	**Manufacturer Part Number**	**Quantity**	**Cost Per Individual**	**Total Cost per parts**
Power Ring Film Capacitor	SBE	700D10897-547	SBE	700D10897-547	1	165.35	165.35
Current Sense Transformer	Mouser	911-CT05-050	Ice Components	CT05-050	1	3.06	3.06
OptiMOS 3 Power Transistor	Mouser	726-IPP114N12N3G	Infineon	IPP114N12N3G	1	2.49	2.49
Fast Switching Diode	Mouser	726-IDP30E120	Infineon	IDP30E120	1	3.23	3.23
Switchmode Power Rectifiers	Mouser	863-MBR1635G	ON Semiconductor	MBR1635G	1	1.09	1.09
LT3750 Capacitive Charge Controller	Linear Technologies	Lt 3750	Linear Technologies	Lt 3750	1	5	5

0.1 Ohm - 1 Watt 1% Tolerant Resistor	Mouser	652-CRF1206FXR010ELF	Bourns	CRF1206-FX-R010ELF	1	0.6	0.6
1k Ohm - 500m Watt 1% Tolerant Resistor	Mouser	660-SG73P2ETTD1001F	KOA Speer	SG73P2ETTD1001F	1	0.22	0.22
10k Ohm - 1 Watt 1% Tolerant Resistor	Mosuer	660-SL1TTE1002F	KOA Speer	SL1TTE1002F	1	0.66	0.66
24.9k Ohm - 1 Watt 1% Tolerant Resistor	Mouser	660-RK73H3ATTE2492F	KOA Speer	RK73H3ATTE2492F	2	0.39	0.78
100k Ohm - 1 Watt 5% Tolerant Resistor	Mouser	660-SL1TTE104J	KOA Speer	SL1TTE104J	2	0.56	1.12
100p Farad - 25 Volts, 5% Tolerant Cap	Mouser	80-C0603C101J3G	Kemet	C0603C101J3GACTU	1	0.03	0.03
0.1u Farad - 25 Volts, 10% Tolerant Cap	Mouser	80-C0603C104K3R	Kemet	C0603C104K3RACTU	1	0.02	0.02

10u Farad - 25 Volts, 10% Tolerant Cap	Mouser	80-C1206C106K3P	Kemet	C1206C106K3PACTU	2	0.35	0.7
330u Farad - 25 Volts, 14m Ohm ESR	Mouser	667-25SEPF330M	Panasonic	25SEPF330M	1	1.88	1.88
Total Cost per board							20.88

Appendix B

Datasheets

B.1 ADS8364 A/D Converter

http://www.ti.com.cn/cn/lit/ds/symlink/ads8364.pdf

B.2 Voltage Sensing Circuit

B.2.1 Potentiometer

Bourns 5,000ΩPotentiometer http://www.mouser.com/ds/2/54/3214-62059.pdf

B.2.2 AVAGO Opto-Isolator

AVAGO Opto-Isolator http://www.avagotech.com/docs/AV02-2460EN

B.2.3 Voltage Regulator

Fairchild LM7805CT Voltage Regulator http://www.mouser.com/ds/2/149/LM7805-189995.pdf

B.2.4 DC/DC Converter

RECOM DC/DC Converter http://www.mouser.com/ds/2/468/RK_RH-225965.pdf

B.2.5 1MΩResistor

Vishay Metal Oxide - 1MΩ1% Tolerance Resistor, High Voltage http://www.mouser.com/ds/2/427/rox-222769.pdf

B.3 Current Sensing Circuit

B.3.1 TAMURA L31S***S05FS Current Sensor

Data Sheet for all L31S***S05FS Current Sensors For this project, the L31S100S05FS and the L31S200S05FS Current Sensors are of interest. http://www.mouser.com/ds/2/397/L31SXXXS05FS-267665.pdf

B.3.2 TAMURA L06P***S05 Current Sensor

Data Sheet for all L06P***S05 Current Sensors For this project, the L06P400S05 and L06P600S05 Current Sensors are of interest. http://www.mouser.com/ds/2/397/L06PXXXS05-22052.pdf

B.3.3 Analog Devices AD8366

Analog Devices Dual-Digital Variable Gain Amplifier AD8366 http://www.analog.com/static/imported-files/data_sheets/AD8366.pdf

B.3.4 10kΩResistor

KOA General Purpose Resistor - 10kΩ1 Watt 1% Tolerance http://www.koaspeer.com/catimages/Products/MF-MFS-RK/MF-MFS-RK.pdf

B.4 Flyback Transformer

B.4.1 CT05 Transformer

For this project, the CT05-050 transformer is of interest. http://www.mouser.com/ds/2/192/CT05-220090.pdf

B.4.2 LT3750 Capacitor Charge Controller

http://cds.linear.com/docs/en/datasheet/3750fa.pdf

B.4.3 MBR1645G Diode

For this project, the MBR1645 power rectifier is of interest http://www.mouser.com/ds/2/308/MBR1635-D-76328.pdf

B.4.4 IDP30E120 Diode

http://www.mouser.com/ds/2/196/IDP30E120_v2_3G[1]-78909.pdf

B.4.5 IPP114N12N3 OptiMOS 3 Power Transistor MOSFET

http://www.mouser.com/ds/2/196/IPP114N12N3%20G_Rev2.4-66942.pdf

B.4.6 Resistors

Bourns Current Sense Resister - 0.01Ω1 Watt 1% Tolerance For this project, the CRF1206 resistor is of interest. http://www.mouser.com/ds/2/54/CRF-56952.pdf

KOA Speer Thick Film Resistor - 1.0k Ohm, 1 Watt 1% Tolerance For this project, the SG73P2ETTD1001F resistor is of interest. http://www.koaspeer.com/catimages/Products/SG73/SG73.pdf

KOA Speer Current Sense Resistor - 10k Ohm, 1 Watt 1% Tolerance For this project, the SL1TTE1002F resistor is of interest. http://www.koaspeer.com/catimages/Products/SL1-SL2-SL3-TSL/SL1-SL2-SL3-TSL.pdf

KOA Speer Thick Film Resistor - 24.9k Ohm, 1 Watt 1% Tolerance For this project, the RK73H3ATTE2492F resistor is of interest. http://www.koaspeer.com/catimages/Products/RK73H/RK73H.pdf

KOA Speer Current Sense Resistor - 100k Ohm, 1 Watt 5% Tolerance For this project, the SL1TTE104J resistor is of interest. http://www.koaspeer.com/catimages/Products/SL1-SL2-SL3-TSL/SL1-SL2-SL3-TSL.pdf

B.4.7 Capacitors

Kemet Multilayer Ceramic Capacitors MLCC - 100p Farad, 25 Volts, 5% Tolerance For this project, the C0603C101J3GACTU capacitor is of interest.

Kemet Multilayer Ceramic Capacitors MLCC - 0.1u Farad, 25 Volts, 10% Tolerance For this project, the C0603C104K3RACTU capacitor is of interest.

Kemet Multilayer Ceramic Capacitors MLCC - 10u Farad, 25 Volts, 10% Tolerance For this project, the C1206C106K3PACTU capacitor is of interest.

Panasonic Aluminum Organic Polymer Capacitors - 330u Farad, 25 Volts, 14m Ohm ESR, 20$ tolerance For this project, the 25SEPF330M capacitor is of interest. http://www.mouser.com/ds/2/315/SEPF_OS-262370.pdf

B.5 IGBT Platform Board

B.5.1 TI SN**LBC170 Differential Transceiver

Data sheet for the SN**LBC170 family of differential transceivers. This project will specifically use the SN75LBC170. www.ti.com/lit/dis/symlink/sn75lbc170.pdf

B.5.2 TI SN**HC595 Shift Registers

Data sheet for the SN**HC595 family of shift registers. This project will specifically use the SN74HC595. http://www.ti.com/lit/ds/symlink/sn74hc595.pdf

B.5.3 100 Ohm Resistor Array

Data sheet for the CRA06S083100RFTA resistor array. http://www.mouser.com/ds/2/427/cra06es-73101.pdf

B.5.4 High Density Connector

Data sheet for the SEAM-40-03.0-S-06-2-A-KTR connector. This connects with the SbRIO board. http://download.siliconexpert.com/pdfs/2014/1/25/15/21/7/646/smt_/manual/23seam.pdf

B.5.5 PCIe Connector

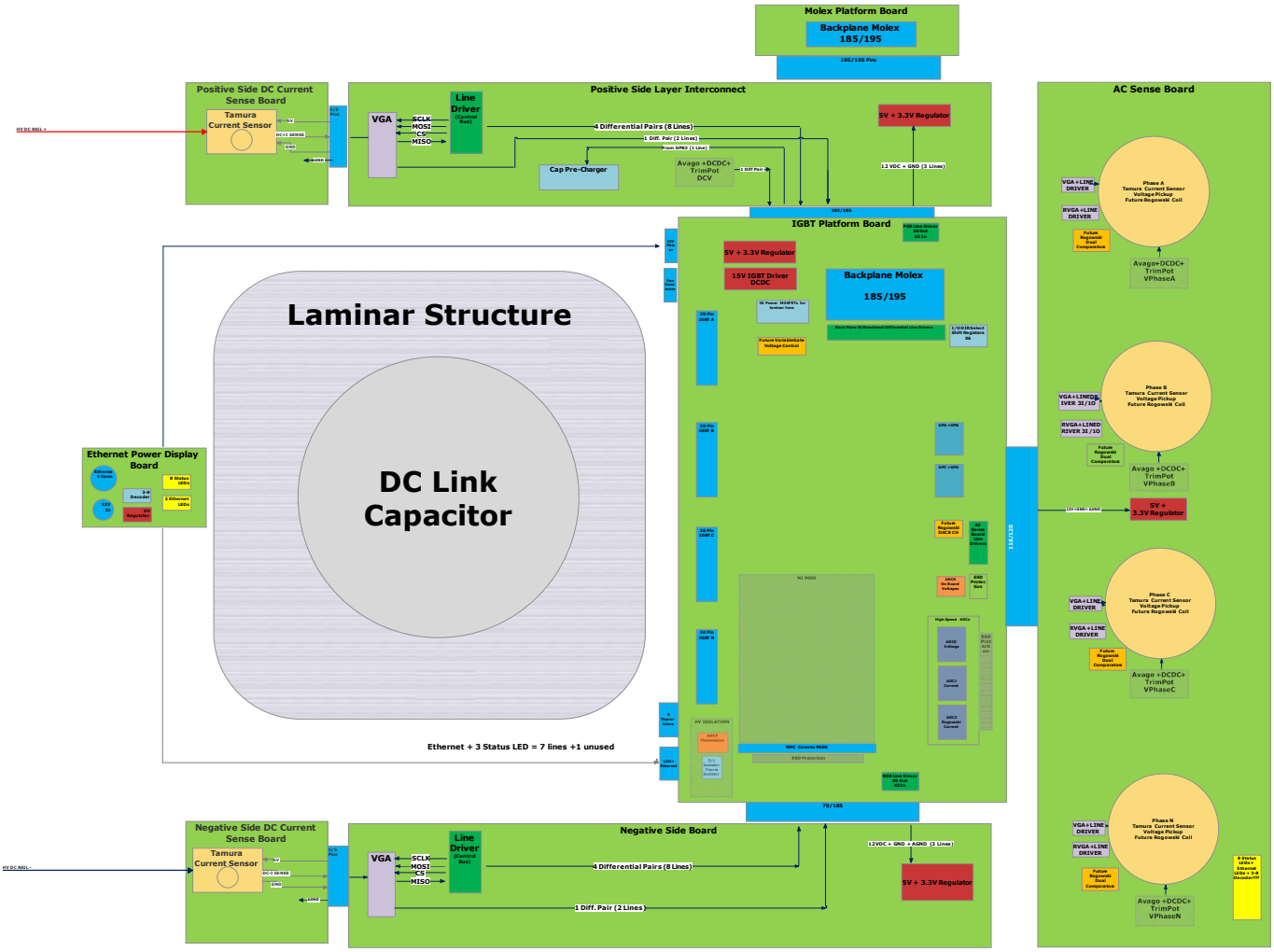
Data sheet for the 1-5145166-2 PCIe Connector. http://goo.gl/MJW1XM

B.5.6 Molex HD Mezz Plug

Data sheet for the 45802-1693 Backplane connector. http://www.molex.com/webdocs/datasheets/pdf/en-us/0458021693_PCB_RECEPTACLES.pdf

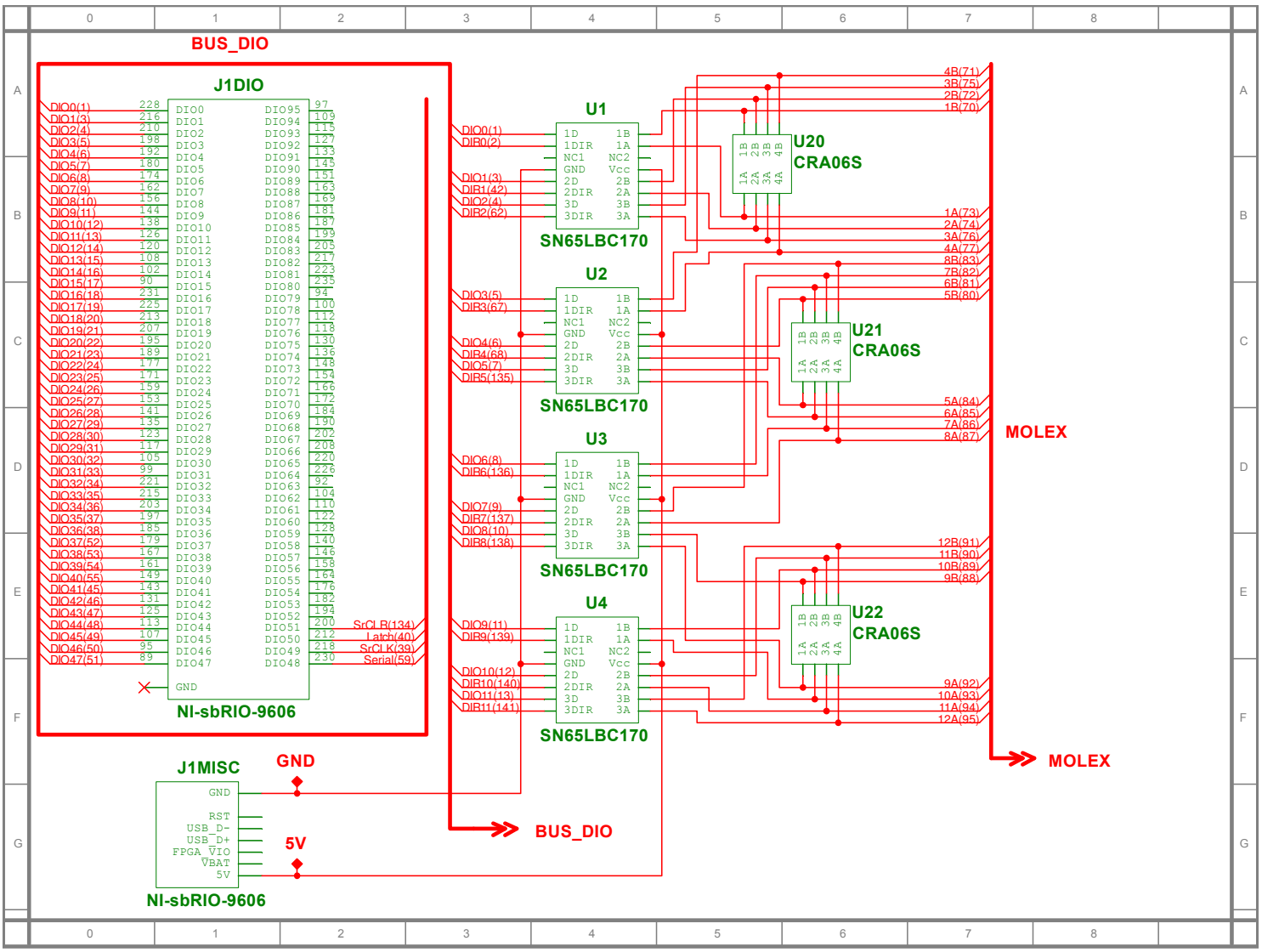
Appendix C

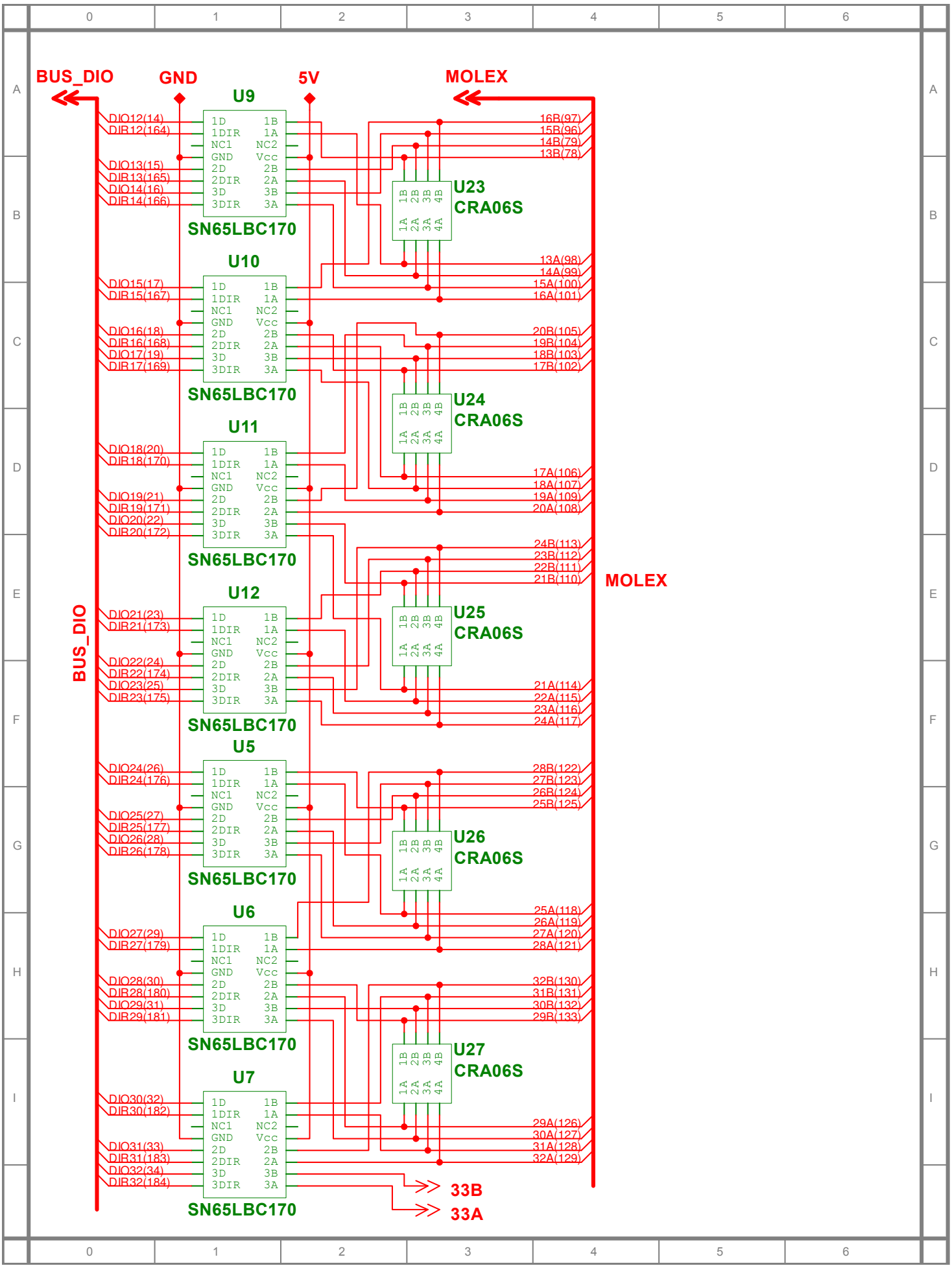
Inverter Block Diagram

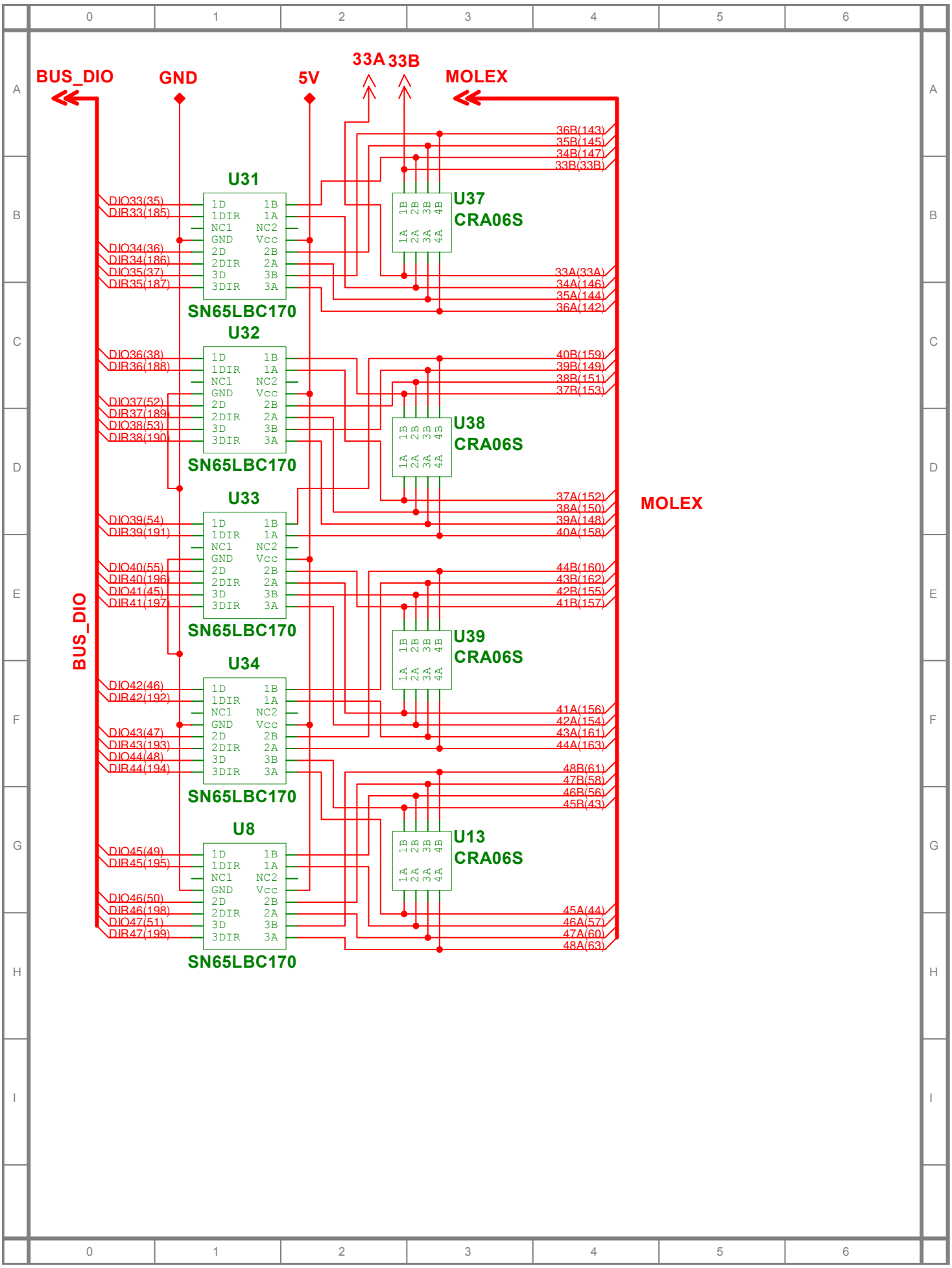

Molex Platform Board
Backplane Molex
185/195
185/195 Pins
Positive Side DC Current Sense Board
Tamura Current Sensor
Positive Side Layer Interconnect
VGA
SCLK
MOSI
CS
MISO
Line Driver (Control Bus)
4 Differential Pairs (8 Lines)
1 Diff. Pair (2 Lines)
from GPIO1 (1 Line)
Cap Pre-Charger
Avago +DCDC+ TrimPot DCV
1 Diff Pair
5V + 3.3V Regulator
12 VDC + GND (3 Lines)
AC Sense Board
Phase A Tamura Current Sensor Voltage Pickup Future Rogowski Coil
VGA +LINE DRIVER
RVGA +LINE DRIVER
Future Rogowski Dual Comparators
Avago+DCDC+ TrimPot VPhaseA
Phase B Tamura Current Sensor Voltage Pickup Future Rogowski Coil
VGA+ LINED IVER 3I/1O
RVGA+LINED RIVER 3I /1O
Avago +DCDC+ TrimPot VPhaseB
5V + 3.3V Regulator
Phase C Tamura Current Sensor Voltage Pickup Future Rogowski Coil
VGA +LINE DRIVER
RVGA +LINE DRIVER
Avago +DCDC+ TrimPot VPhaseC
Phase N Tamura Current Sensor Voltage Pickup Future Rogowski Coil
VGA+LINE DRIVER
RVGA +LINE DRIVER
Avago +DCDC+ TrimPot VPhaseN
IGBT Platform Board
5V + 3.3V Regulator
15V IGBT Driver DCDC
Backplane Molex
185/195
Laminar Structure
DC Link Capacitor
Ethernet Power Display Board
Ethernet 1 Conn
12V 3A
3-8 Decoder
5V Regulator
8 Status LEDs
3 Ethernet LEDs
Ethernet + 3 Status LED = 7 lines +1 unused
114/220
70/185
Negative Side DC Current Sense Board
Tamura Current Sensor
Negative Side Board
VGA
SCLK
MOSI
CS
MISO
Line Driver (Control Bus)
4 Differential Pairs (8 Lines)
1 Diff. Pair (2 Lines)
12VDC + GND + AGND (3 Lines)
5V + 3.3V Regulator

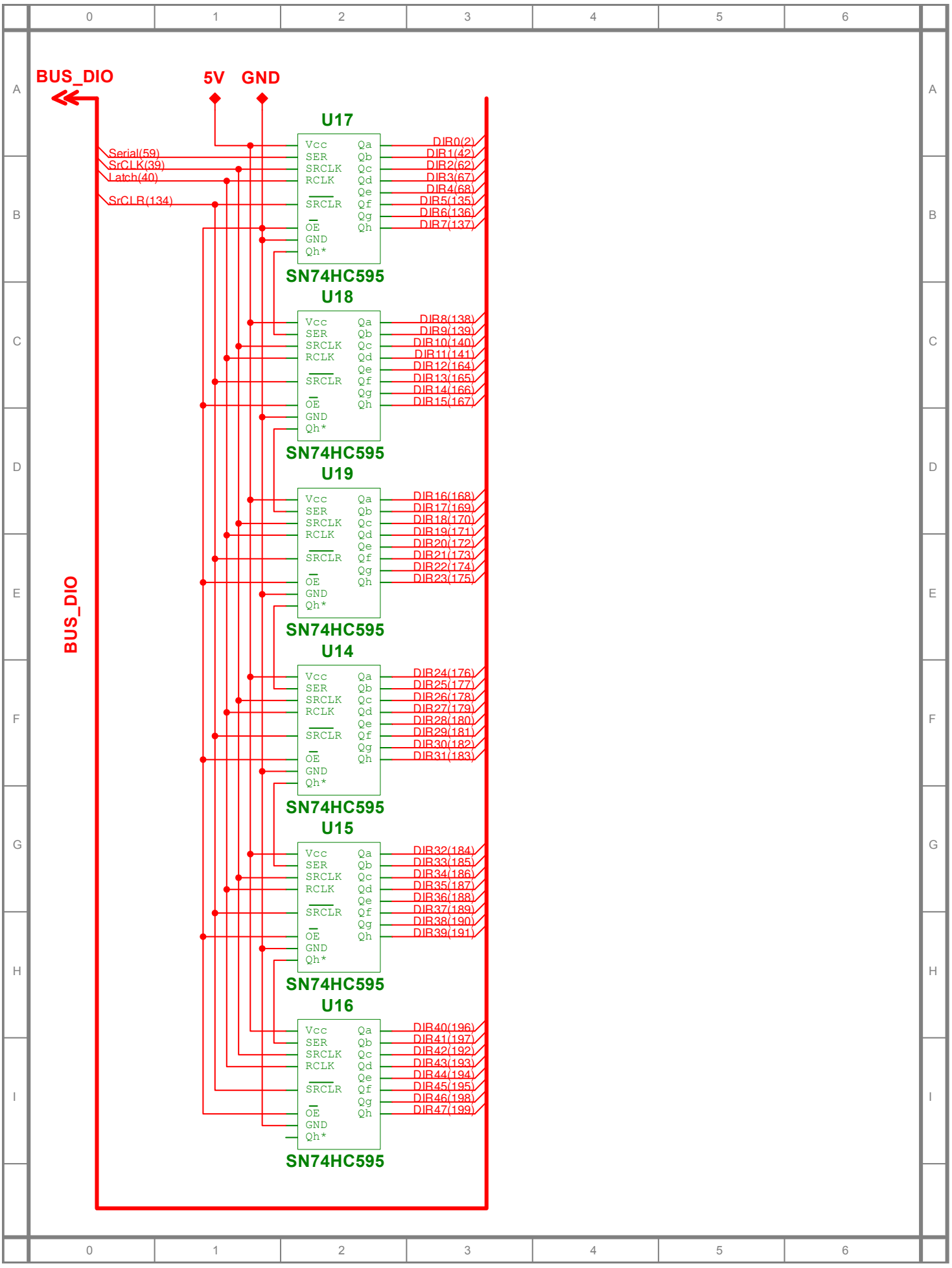
Appendix D

IGBT Platform Board Schematic


BUS_DIO
J1DIO
NI-sbRIO-9606
U1
U2
U3
U4
SN65LBC170
U20
U21
U22
CRA06S
MOLEX
J1MISC
GND
5V
NI-sbRIO-9606
BUS_DIO


BUS_DIO
GND
5V
MOLEX
U9
DIO12(14)
DIR12(164)
DIO13(15)
DIR13(165)
DIO14(16)
DIR14(166)
SN65LBC170
U23
CRA06S
16B(97)
15B(96)
14B(79)
13B(78)
13A(98)
14A(99)
15A(100)
16A(101)
U10
DIO15(17)
DIR15(167)
DIO16(18)
DIR16(168)
DIO17(19)
DIR17(169)
SN65LBC170
U24
CRA06S
20B(105)
19B(104)
18B(103)
17B(102)
17A(106)
18A(107)
19A(109)
20A(108)
U11
DIO18(20)
DIR18(170)
DIO19(21)
DIR19(171)
DIO20(22)
DIR20(172)
SN65LBC170
U25
CRA06S
24B(113)
23B(112)
22B(111)
21B(110)
21A(114)
22A(115)
23A(116)
24A(117)
U12
DIO21(23)
DIR21(173)
DIO22(24)
DIR22(174)
DIO23(25)
DIR23(175)
SN65LBC170
U26
CRA06S
28B(122)
27B(123)
26B(124)
25B(125)
25A(118)
26A(119)
27A(120)
28A(121)
U5
DIO24(26)
DIR24(176)
DIO25(27)
DIR25(177)
DIO26(28)
DIR26(178)
SN65LBC170
U27
CRA06S
32B(130)
31B(131)
30B(132)
29B(133)
29A(126)
30A(127)
31A(128)
32A(129)
U6
DIO27(29)
DIR27(179)
DIO28(30)
DIR28(180)
DIO29(31)
DIR29(181)
SN65LBC170
U7
DIO30(32)
DIR30(182)
DIO31(33)
DIR31(183)
DIO32(34)
DIR32(184)
SN65LBC170
33B
33A
MOLEX
BUS_DIO


BUS_DIO
GND
5V
33A
33B
MOLEX
U31
SN65LBC170
U32
SN65LBC170
U33
SN65LBC170
U34
SN65LBC170
U8
SN65LBC170
U37
CRA06S
U38
CRA06S
U39
CRA06S
U13
CRA06S
1D 1B
1DIR 1A
NC1 NC2
GND Vcc
2D 2B
2DIR 2A
3D 3B
3DIR 3A
1A 1B 2A 2B 3A 3B 4A 4B
DIO33(35)
DIR33(185)
DIO34(36)
DIR34(186)
DIO35(37)
DIR35(187)
DIO36(38)
DIR36(188)
DIO37(52)
DIR37(189)
DIO38(53)
DIR38(190)
DIO39(54)
DIR39(191)
DIO40(55)
DIR40(196)
DIO41(45)
DIR41(197)
DIO42(46)
DIR42(192)
DIO43(47)
DIR43(193)
DIO44(48)
DIR44(194)
DIO45(49)
DIR45(195)
DIO46(50)
DIR46(198)
DIO47(51)
DIR47(199)
36B(143)
35B(145)
34B(147)
33B(33B)
33A(33A)
34A(146)
35A(144)
36A(142)
40B(159)
39B(149)
38B(151)
37B(153)
37A(152)
38A(150)
39A(148)
40A(158)
44B(160)
43B(162)
42B(155)
41B(157)
41A(156)
42A(154)
43A(161)
44A(163)
48B(61)
47B(58)
46B(56)
45B(43)
45A(44)
46A(57)
47A(60)
48A(63)
MOLEX
BUS_DIO


BUS_DIO
5V
GND
U17
Vcc
SER
SRCLK
RCLK
SRCLR
OE
GND
Qh*
Qa
Qb
Qc
Qd
Qe
Qf
Qg
Qh
Serial(59)
SrCLK(39)
Latch(40)
SrCLR(134)
DIR0(2)
DIR1(42)
DIR2(62)
DIR3(67)
DIR4(68)
DIR5(135)
DIR6(136)
DIR7(137)
SN74HC595
U18
DIR8(138)
DIR9(139)
DIR10(140)
DIR11(141)
DIR12(164)
DIR13(165)
DIR14(166)
DIR15(167)
SN74HC595
U19
DIR16(168)
DIR17(169)
DIR18(170)
DIR19(171)
DIR20(172)
DIR21(173)
DIR22(174)
DIR23(175)
SN74HC595
U14
DIR24(176)
DIR25(177)
DIR26(178)
DIR27(179)
DIR28(180)
DIR29(181)
DIR30(182)
DIR31(183)
SN74HC595
U15
DIR32(184)
DIR33(185)
DIR34(186)
DIR35(187)
DIR36(188)
DIR37(189)
DIR38(190)
DIR39(191)
SN74HC595
U16
DIR40(196)
DIR41(197)
DIR42(192)
DIR43(193)
DIR44(194)
DIR45(195)
DIR46(198)
DIR47(199)
SN74HC595
BUS_DIO