Network Electrophysiology Sensor-On-A-Chip

by

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Abstract

Electroencephalogram (EEG), Electrocardiogram (ECG), and Electromyogram (EMG) bio-potential signals are commonly recorded in clinical practice. Typically, patients are connected to a bulky and mains-powered instrument, which reduces their mobility and creates discomfort. This limits the acquisition time, prevents the continuous monitoring of patients, and can affect the diagnosis of illness. Therefore, there is a great demand for low-power, small-size, and ambulatory bio-potential signal acquisition systems.

Recent work on instrumentation amplifier design for bio-potential signals can be broadly classified as using one or both of two popular techniques: In the first, an AC-coupled signal path with a MOS-Bipolar pseudoresistor is used to obtain a low-frequency cutoff that passes the signal of interest while rejecting large dc offsets. In the second, a chopper stabilization technique is designed to reduce 1/f noise at low frequencies. However, both of these existing techniques lack control of low-frequency cutoff.

This thesis presents the design of a mixed-signal integrated circuit (IC) prototype to provide complete, programmable analog signal conditioning and analog-to-digital conversion of an electrophysiologic signal. A front-end amplifier is designed with low input referred noise of 1 μ Vrms, and common mode rejection ratio 102 dB. A novel second order sigma-delta ($\Sigma\Delta$) analog-to-digital converter (ADC) with a feedback integrator from the $\Sigma\Delta$ output is presented to program the low-frequency cutoff, and to enable wide input common mode range of $\pm$0.3V. The overall system is implemented in Jazz Semiconductor 0.18 μm CMOS technology with power consumption 5.8 mW from $\pm 0.9V$ power supplies.

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Chapter 1

Introduction

Various clinical and scientific disciplines sense the electrical activity associated with various functions of the human body through electrophysiological signals such as Electroencephalogram (EEG), Electrocardiogram (ECG), and Electromyogram (EMG). At present, different instrumentation is designed for each electrophysiologic signal. This work presents a mixed-signal integrated circuit (IC) prototype to provide complete, programmable analog conditioning and analog-to-digital conversion suitable for a range of electrophysiologic signals. Section 1.1 of this chapter gives an overview and background of bio-potential signals. Section 1.2 describes the goals of this project. Section 1.3 describes the existing work as of project initiation in 2006. Finally, Section 1.4 presents the existing work in 2010 at project completion.

This thesis is organized as follows; Chapter 2 covers the design specifications required in order to extract weak bio-potential signals, over different frequency ranges, in the presence of large in-band and out-of-band interference. Chapter 3 describes the Sigma-Delta ($\Sigma\Delta$) analog-to-digital converter (ADC) architecture developed for this work, with a programmable built-in pre-amplifier to meet the design requirements for different signal applications. Sources of error, nonidealities, and their effects on the digital output are discussed. Chapter 4 covers the detailed circuit implementation of the $\Sigma\Delta$ ADC. Chapter 5 presents the results from the prototype IC fabricated in a 180nm CMOS process. Chapter 6 concludes by summarizing the developments and contributions of the thesis and possible future

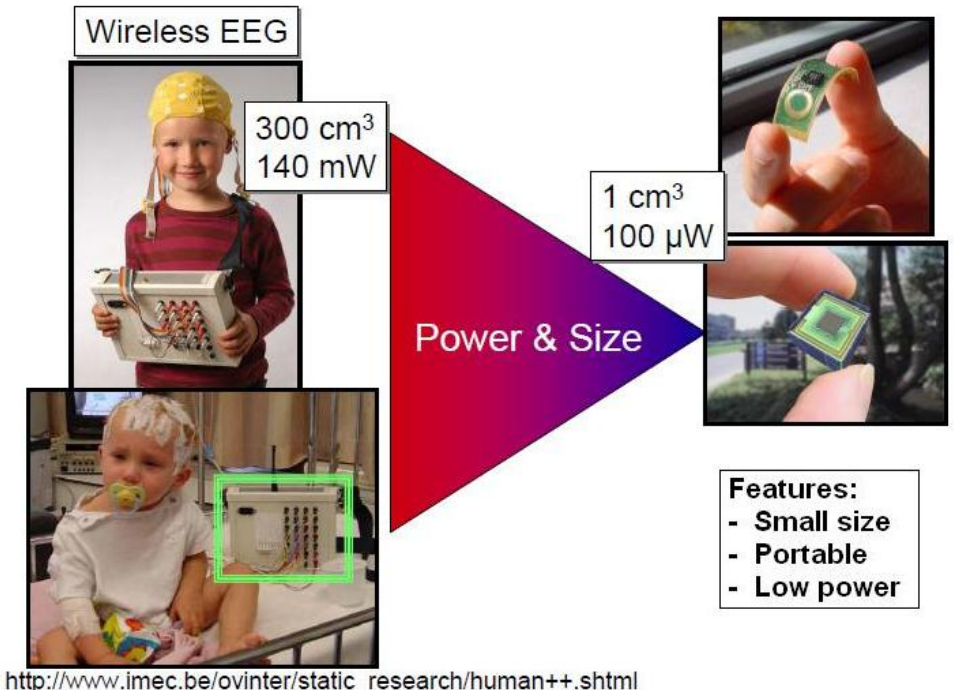

Figure 1.1: Traditional biomedical equipment and small-size integrated circuits.

work.

1.1 Background of Bio-Potential Signals

EEG, ECG, and EMG bio-potential signal waveforms are commonly measured, monitored, and/or recorded in clinical practice. Usually patients are connected to a bulky and mains-powered instrument, which reduces their mobility and creates discomfort. This limits the acquisition time, prevents the continuous monitoring of patients, and can affect the diagnosis of illness. Therefore, there is a great demand for low-power, small-size, and ambulatory bio-potential acquisition systems as shown in Figure 1.1. The goal of this project is to design a bio-potential acquisition system that is compatible with long-term power autonomy for different bio-potential signals. The purpose is not only to increase the patient's quality of life but also to enable extension of device application to areas such as sports, entertainment, and comfort monitoring.

1.2 Research Goal

EEG is used primarily in studying the properties of cerebral and neural networks in neurosciences, as well as to monitor the neurodevelopment and sleep patterns of infants in the intensive care unit and ultimately to use this information to improve daily medical care. EEG is also used to monitor epileptic seizures from patients.

The ECG is a diagnostic tool that measures and records the electrical activity of the heart. Interpretation of ECG waveform details allows diagnosis of a wide range of heart conditions, varying from minor to life threatening (e.g. symptoms of myocardial infarction). ECG is also used for assessment of patients with systemic disease or critical conditions, as well as patient monitoring during anesthesia.

EMG is a technique for evaluating and recording the electrical activity produced by skeletal muscles. It is used to diagnose diseases that generally may be classified into following categories: neuropathies, neuromuscular junction diseases and myopathies. Table 1.1 summaries the selected applications for differential bio-potential signals.

Bio-potential signals such as EEG, ECG, and EMG are considered to be weak signals since peak amplitudes range from 100 μV in the case of EEG signals up to 5 mV for ECG signals [1]. The bandwidth of these bio-potential signals ranges from 0.05 to 2000Hz in nor-

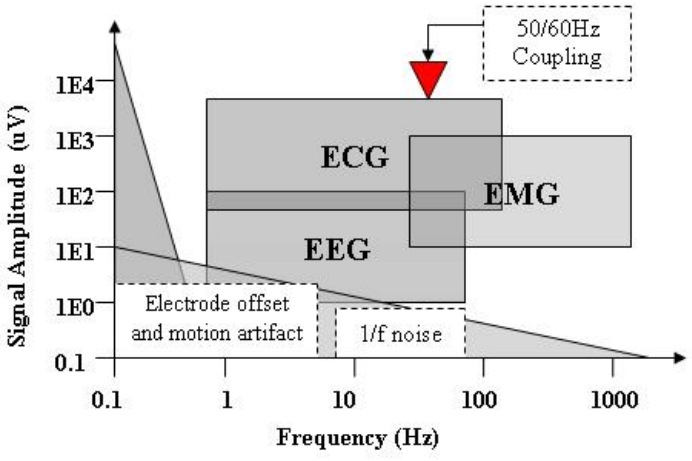

Figure 1.2: Frequency and amplitude characteristics of bio-potential signals, EEG, ECG, and EMG, and contaminating signals of the bio-potential signals.

Table 1.1: Bio-potential signals and Applications.

Bio-potential signals	Selected Applications
EEG	Sleep studies, seizure detection, cortical mapping
ECG	Diagnosis of ischemia, arrhymia, conduction defects
EMG	Eye position, sleep state, vetibulo-ocular reflex

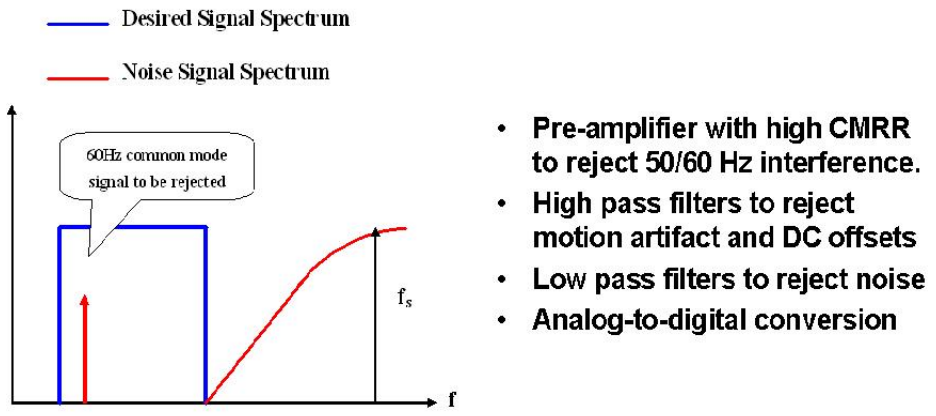

Figure 1.3: Frequency response for overall system.

mal operation [1]. In addition, due to electrochemical effects at the skin-electrode interface, dc offsets up to ± 0.3V are common across differential recording electrodes. Additionally, in some applications, motion artifacts add a large interfering component to the voltage seen at the measurement electrodes.

Once the derived biosignal is formed through differential combination of the electrical activity from the electrodes, the signal is processed by analog electronics prior to digitizing. If not removed, dc offsets at skin-electrode interface an/or motion artifact will cause the electronics to saturate, resulting in loss of the signal-of-interest. Within the analog signal processing electronics, device 1/f is also within the band of interest, so the maximum input-referred noise must be designed to be less than a few μV_{pp}. Moreover, the largest electrical signal on/within the body is usually due to voltages from the power line at 50/60-Hz. The power line voltage is several volts, which is several orders of magnitude larger than the bio-potential signals. Since the power line interference is nearly the same at each site, bio-

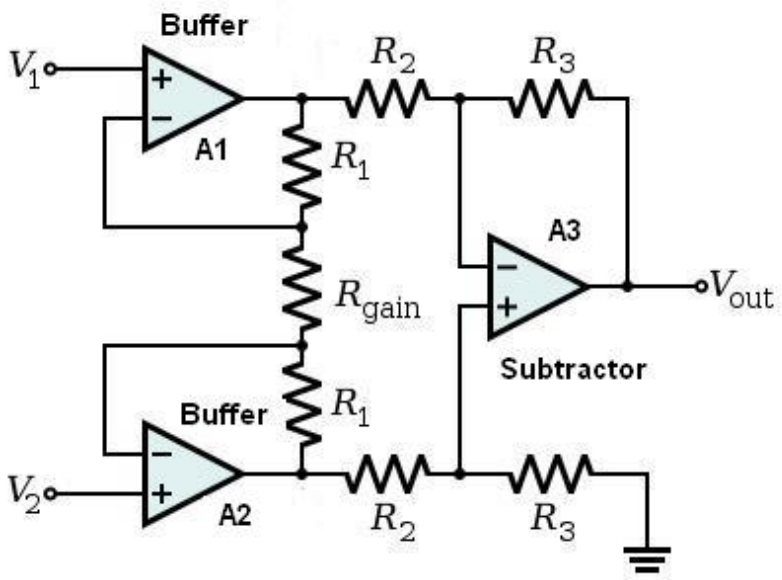

Figure 1.4: Typical Instrumentation amplifier with 3-op amp configuration.

potential signals tend to be acquired using a weighted, balanced electrode configuration. Then the common mode of electrical activity from two sites can be subtracted and the differential mode of these is amplified.

A summary of measurement source errors is shown in Figure 1.2. In order to achieve signal extraction under these circumstances, an acquisition system must be designed with high common-mode rejection ration (CMRR), low noise, and a high-pass filter (HPF) characteristics as shown in Figure 1.3.

1.3 Existing Work, as of 2006

In this section, several design alternatives are investigated for a bio-potential signal acquisition system. An instrumentation amplifier (IA) is used in many applications, from motor control to data acquisition to automotive. Figure 1.4 shows a typical 3-op amp IA configuration [2]. The input amplifiers A_1 and A_2 of the IA buffer the input voltage. A single resistor, R_{gain}, is connected between the summing nodes of the two input buffers.

The full differential input voltage will now appear across R_{gain}. Since the amplified input voltage appears differentially across the three resistors R_1 - R_{gain} - R_1, the differential gain can be varied by changing R_{gain}.The total gain of the circuit is

$$\frac{V_{out}}{V_{in}} = \left(1 + \frac{2R_1}{R_{gain}}\right)\frac{R_3}{R_2}. \tag{1.1}$$

Since the voltage across R_{gain} equals V_{in}, the current through R_{gain} will equal (V_{in}/R_{gain}). Amplifiers A_1 and A_2 will operate with gain and amplify the input signal. If a common-mode voltage is applied to the amplifier input, the voltages on each side of R_{gain} will be equal, and no current will flow through this resistor. Since no current flows through R_{gain}, amplifiers A_1 and A_2 will operate as unity-gain followers. Thus, common-mode signals will be passed through the input buffers at unity gain, but differential voltages will be amplified by the factor $(1 + 2R_1/R_{gain})$. Finally, the common-mode voltages are attenuated by the subtractor A_3 while the differential voltages are amplified by a factor of R_3/R_2. In order to process the weak bio-potential signals, the buffer amplifiers must be designed with low input referred noise. One of the R_3 resistors can be adjustable to maintain high common-mode rejection due to the mismatch between the two R_2 / R_3 resistor ratios.

The AD620 from Analog Devices, Inc. (ADI) is one alternative as an integrated solution for IA design [3]. A simplified schematic of the AD620 in Figure 1.5 shows it to be a modification the 3-op amp circuit. The current sources I_1, I_2 set the collector currents of transistors Q_1 and Q_2 as well as the voltages between the base and emitter (V_{be}) of Q_1 and Q_2. The two op-amps A_1 and A_2 force the collector voltages of Q_1 and Q_2 to be equal to V_B, so the V_{ce} of Q_1 and Q_2 are constant; this ensures linear processing of the input signals and good common mode rejection. The source degeneration resistor R_G provides a constant linear transconductance (g_{m1}, g_{m2}) for Q_1 and Q_2. The gain of the AD620 is

$$Gain = \frac{R_1 + R_2}{R_G} + 1. \tag{1.2}$$

Again, the common-mode signals at the output of A_1 and A_2 are subtracted by the unity gain subtractor A_3 while the differential signals are amplified. Note that the low frequency limit of the bandwidth extends to dc; this can lead to problems with amplifier saturation

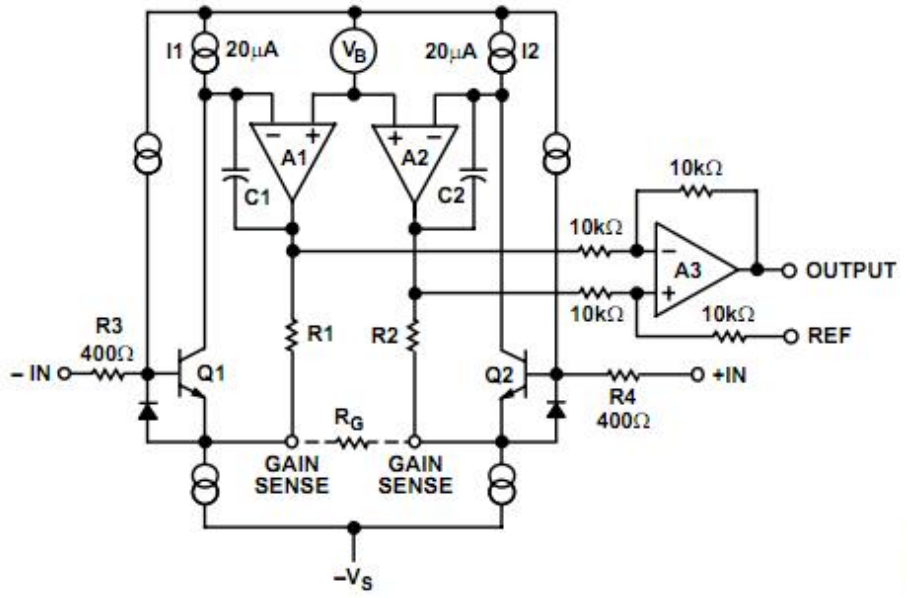

Figure 1.5: A simplified schematic of the AD620.

given the large dc errors indicated in Figure 1.2.

As of project initiation in 2006, recent work on bio-amplifier design [4–13] featured AC-coupled input circuitry with a MOS-Bipolar "pseudoresistor" to obtain a low-frequency cutoff that passes the signal of interest while rejecting large dc offsets. A MOS-Bipolar pseudoresistor can achieve an equivalent resistance r_{eq} of greater than $10^{10}\Omega$ [4]. A typical schematic of this bio-amplifier design approach is shown at the left of Figure 1.6. The midband gain A_M is set by C_1/C_2, and the bandwidth is $g_m/(A_M C_L)$, where C_1 and C_2 are the feedback network capacitors, and g_m is the transconductance of the operational transconductance amplifier (OTA). Two MOS-bipolar pseudoresistors are used in serial to reduce the distortion for large output signals, while any dc signals are rejected by the capacitor C_1. The low-frequency cutoff of the ac-coupled amplifier is $1/(2r_{eq}C_2)$. The measured amplifier transfer function from 0.004Hz to 50 kHz is shown at the right of Figure 1.6. The midband gain is approximately 40dB. The low-frequency cutoff is approximately 0.025 Hz. The input-referred noise of the bio-amplifier can be related to the (OTA) input-referred noise by

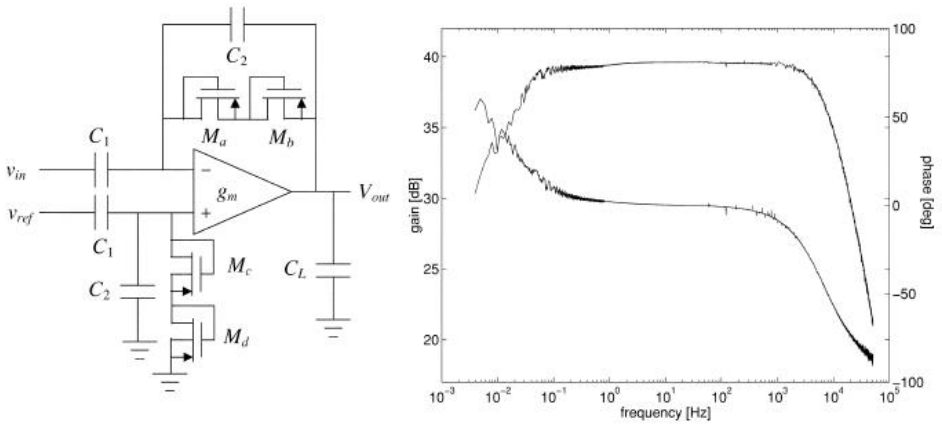

Figure 1.6: The schematic of bio-amplifier design at left. The transfer function of bio-amplifier design at right.

$$V_{ni,amp}^2 = \left(\frac{C_1 + C_2 + C_{in}}{C_1}\right)^2 V_{ni,OTA}^2. \tag{1.3}$$

where C_{in} is the parasitic capacitance at the input terminal of the OTA. All transistors of OTA are made as large as possible to minimize 1/f noise. The input referred noise is $21nV/\sqrt{Hz}$ with capacitor C_1=20 pF, C_2=200 fF, C_L=17 pF, and operating all transistors of the OTA in weak inversion region to minimize power dissipation.

In [5] and [6] a combination of ac-coupled and chopper stabilization techniques is proposed to remove dc offset and to reduce 1/f noise and motion artifact effects at low frequencies. The architecture of the bio-potential readout system in [5] is shown in Figure 1.7. It includes an ac-coupled chopped IA clocked at 4kHz, a switched capacitor (SC) spike filter (SF) stage, a constant gain stage, and a programmable gain stage. The dc offset and 1/f noise of the ac-coupled chopped IA is modulated by the output chopper modulator, while the electrode dc offset is rejected by the ac-coupled stage. The switched-capacitor spike filter mitigates the effect of possible spike coupling due to non-ideality of the chopping switches. The second gain stage is designed with a pseudoresistor in order to reject the dc offset or motion artifact at low frequencies. The third stage is designed to program the gain and to adjust the high frequency cutoff through bandwidth (BW) switches. The transfer function of the bio-amplifier is shown at the left of Figure 1.8. The input referred noise is

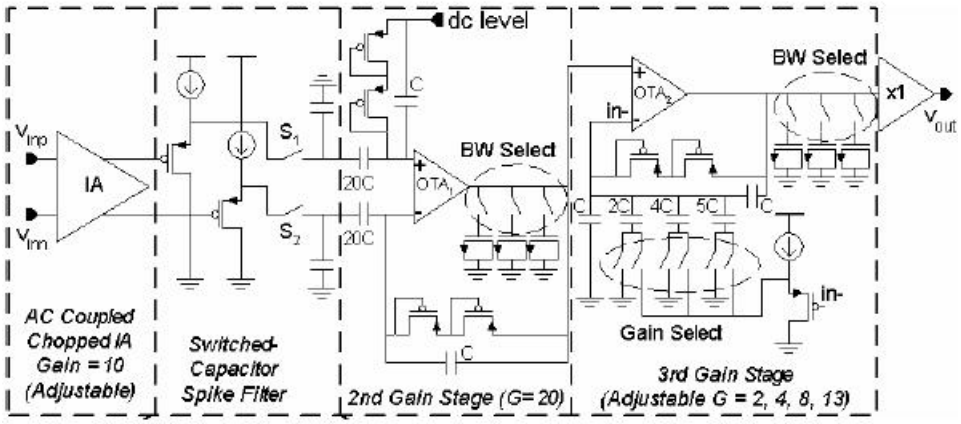

Figure 1.7: The schematic of bio-amplifier design.

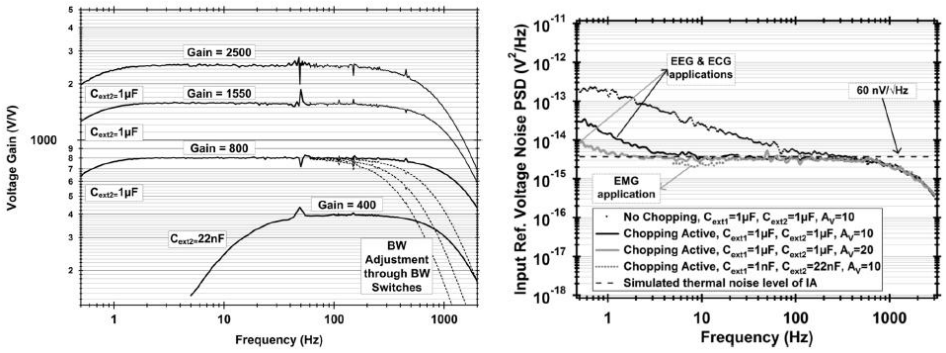

Figure 1.8: The transfer function of bio-amplifier design at the left. The noise results of bio-amplifier design at the right.

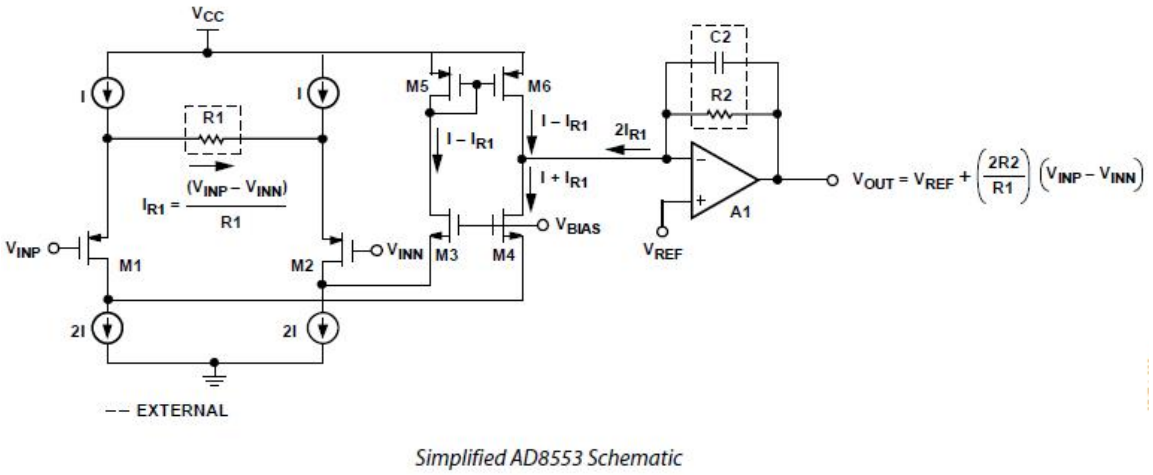

Figure 1.9: Simplified AD8553 schematic.

$56nV/\sqrt{Hz}$ and is shown at the right of Figure 1.8.

Following demonstration of single channel biomedical acquisition systems, multi-channel systems [8, 10–12] have been designed based on the AC-coupled with pseudoresistor technique, and also [11] using the chopping technique.

1.4 Existing Work as of 2010

As the work of this thesis was nearing completion in 2010, Analog Devices released the AD8553 product for single channel systems with gain set by two off-chip resistors R_1 and R_2 based on the fundamental concept of 3-op amp IA topology. White noise is defined by the off-chip resistors R_1 and R_2, and transconductances of transistors M_1 and M_2 as shown in Figure 1.9. 1/f noise is reduced by an autocorrelation shuffling technique.

As shown in Figure 1.9, the circuit consists of a voltage-to-current converter (M_1 to M_6), followed by a current-to-voltage amplifier (R_2 and A_1). When an input signal is applied, the differential-mode voltage is converted to a current in R_1. Transistors M_3 to M_6 form a folded cascode structure which provides twice this current to the input of the opamp A_1. Amplifier A_1 and resistor R_2 form a current-to-voltage converter to generate a output

voltage at V_{OUT}. Since common-mode input voltage does not contribute to current in R_1, the current I_R inherently rejects the input common-mode voltage so it is not seen by the voltage-to-current amplifier. The external capacitor C_2 aattenuates high frequency noise.

Also in 2010, Texas instruments (TI) released the ADS1298, an 8-channel product with programmable gain amplifier (PGA) and 24-bit $\Sigma\Delta$ ADC for biomedical applications. The functional block diagram of ADS1298 is shown in Figure 1.10 ($\Sigma\Delta$ ADC is not shown). Each channel contains an EMI filter, a flexible input multiplexer, a PGA, and a $\Sigma\Delta$ ADC. The EMI filter is designed with cutoff frequency at 3 MHz to filter out any electromagnetic interference that may have been coupled to/from signal or power lines. The PGA is designed with low-noise, gain programmable based on the traditional 3-op amp configuration. The right leg drive (RLD) circuity is used as a negative feedback loop to reduce the effect of common mode signal from the power line. Once the bio-potential signals are extracted, the $\Sigma\Delta$ ADC converts the analog signal to digital format. Thus, it can be digitally networked with many other of these ICs.

Both AD8553 and ADS1298 are good examples of single and multi-channel systems for biomedical applications, similar to the work to be described in this thesis. More detailed specifications for these products can be found in [14, 15].

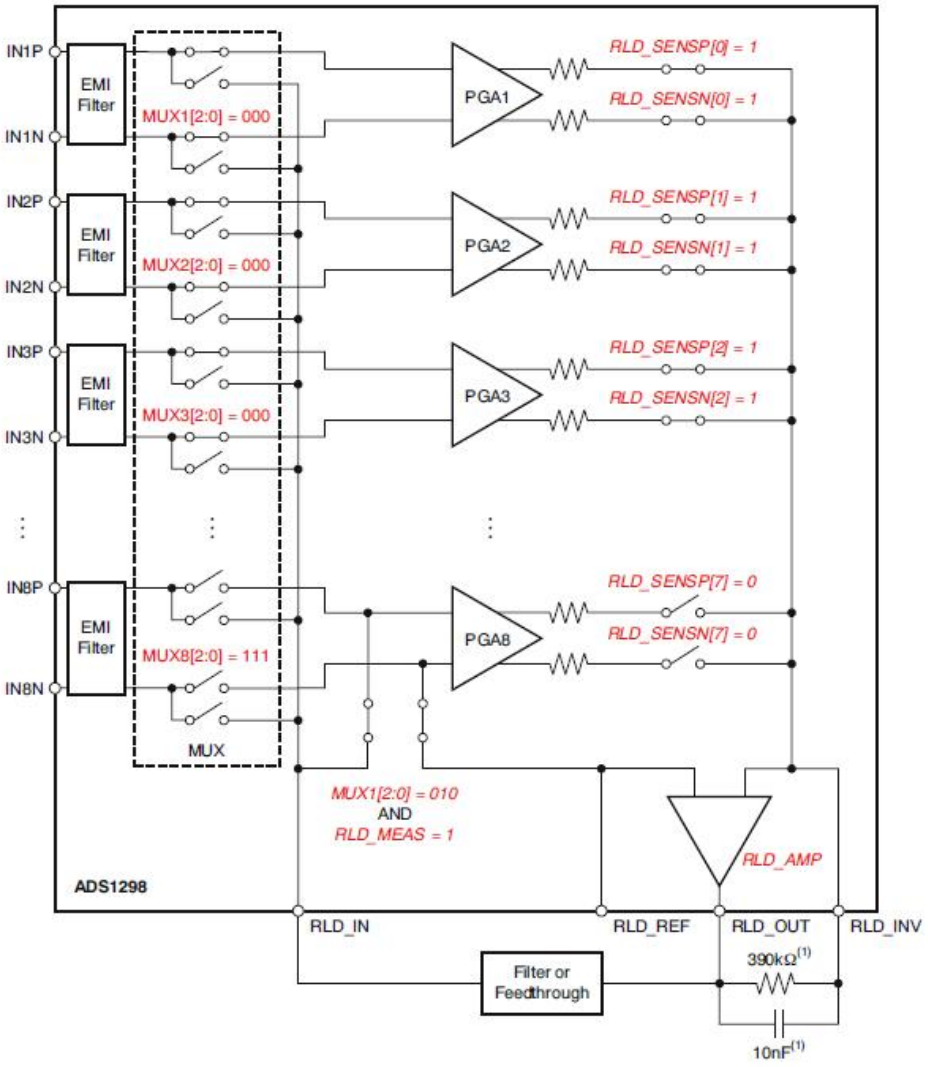

Figure 1.10: Functional block diagram of ADS1298.

Chapter 2

Analog Architecture Requirement

In this chapter, analog architecture requirements for biomedical acquisition system are introduced. Table 2.1 summaries the specifications for bio-potential signals. Section 2.1 introduces the bandwidth requirement for these signals. Section 2.2 states the noise from different sources. Section 2.3 and section 2.4 describes the CMRR and input common-mode range (ICMR) requirements for the system respectively.

2.1 Bandwidth

The bandwidth for bio-potential signals ranges from 0.05 Hz to 2000 Hz according to Table 2.1. A system with high-pass filter (HPF) and low-pass filter (LPF) characteristics is needed in order to meet the requirement. However, a HPF with 0.05 Hz cutoff frequency is not easy to achieve, as a large value resistor or capacitor is required in order to realize a low

Table 2.1: Specifications for Bio-potential Signals

	ECG	EEG	EMG
Amplitude (mV)	1	0.1	1
Frequency Range (Hz)	0.05-100	0.1-100	100-2000
Noise (uVrms)	$\leq$2.5	$\leq$2.5	$\leq$1.6
CMRR (dB)	$\geq$85		
ICMR (V)	$\pm$0.3		

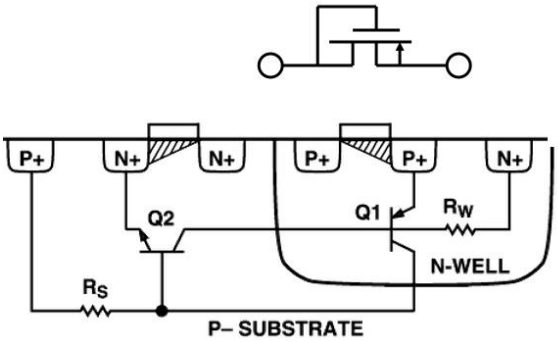

Figure 2.1: Cross-section of PMOS and NMOS devices, showing parasitic transistor Q1 and Q2

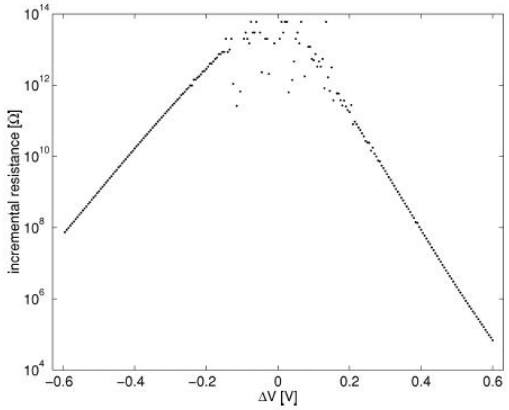

Figure 2.2: Equivalent resistance of single MOS-bipolar element. For low voltages, the resistance exceeds 10^{12} ohm.

cutoff frequency of order 0.05 Hz. For integrated circuit design, several techniques [4,16,17] are introduced with large value of equivalent resistance.

In [4, 17], the transistors acts as pseudoresistor as shown in Figure 2.1. The device functions as diode-connected PMOS transistor when V_{GS} is negative. With positive V_{GS}, the source-well-drain pnp bipolar junction transistor (BJT) is activated, and the device acts as a diode-connected BJT. Figure 2.2 is the plot for $|\Delta V|$ in x-axis and equivalent resistance in y-axis. The equivalent resistance r_{eq} is extremely high for a small voltages across the device. For $|\Delta V < 0.2V|$, the observed $dV/dI > 10^{11}$ ohm as shown in Figure 2.2. The low-frequency cutoff is $1/(r_{eq}C_2 2\pi) < 0.8Hz$ with $C_2 = 200fF$ as discussed in section 1.3.

In [16], a bias current is passed through a reference FET M_1, biased in the sub-threshold

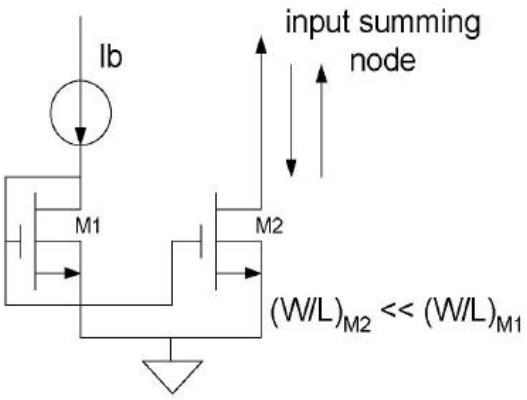

Figure 2.3: Long-FET biasing scheme for practical implementation of the monolithic $5G\Omega$ impedance.

region as shown in Figure 2.3. The gate voltage is then mirrored to a long-length FET M_2. Assuming symmetric drift currents, the small-signal impedance of M_2 to the reference voltage is modeled as

$$R_{eq} = \frac{W_1}{L_1}\frac{L_2}{W_2}\frac{kT}{qI_{bias}} \tag{2.1}$$

where k is Boltzmann constant, and T is temperature in Kelvin. This model demonstrates that synthesizing $5G\Omega$ is feasible using on-chip FETs. With an on-chip capacitor of 10 pF, the low-frequency cutoff can be achieved at 3.2 Hz.

The above methods are insufficient for ECG application, since the low-frequency cutoff for ECG is less than 0.05 Hz according to Table 2.1. In order to get a lower frequency cutoff while proving programmable feature, a new design for low-frequency cutoff is introduced in Chapter 3.

2.2 Noise

EEG, ECG, and EMG have amplitudes ranging from 100 μV to few mV [1], so the maximum input-referred noise of electronics must be designed to be less then few μV_{pp} as can be seen from Table 2.1. The input referred noise design goal is therefor 1 μVrms across

the widest frequency range of 0.05 Hz to 2 kHz for the different bio-potential signals in this project. When narrower frequency ranges are selected, then the SNR is always less than the specification. In this section, different noise sources are discussed and analyzed.

2.2.1 Quantization Noise

The quantization errors can be modeled as

$$V_Q = V_y - V_{in} \tag{2.2}$$

where the V_y is output from Digital-to-analog block, and V_{in} is the input signal as shown in Figure 2.4. The power of quantization noise can be found by deterministic or stochastic approach [18]. To deal with more general input case, the stochastic approach is discussed. We assume the quantization noise V_Q is a random variable uniformly distributed between $\pm V_{LSB}/2$, the probability density function for this signal, f_Q(x), will be a constant value as shown in Figure 2.5. The rms value of the quantization error is given by

$$V_{Q(rms)} = \left[\int_{-\infty}^{\infty} x^2 f_Q(x)\, dx\right]^{1/2} = \frac{1}{V_{LSB}}\left[\int_{-V_{LSB}/2}^{V_{LSB}/2} x^2 dx\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}}. \tag{2.3}$$

Signal-to-noise (SNR) is defined as the ratio of the signal power to the noise at the analog output. Thus, for a random signal uniformly distributed between zero and V_{ref}, the SNR is

$$SNR = 20log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20log\left(\frac{V_{ref}/\sqrt{12}}{V_{LSB}/\sqrt{12}}\right) = 20log(2^N) = 6.02NdB. \tag{2.4}$$

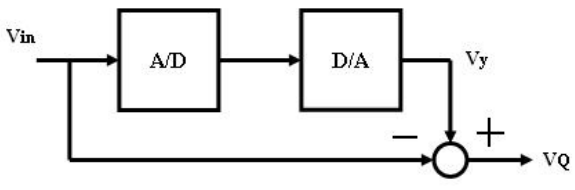

Figure 2.4: Quantization noise.

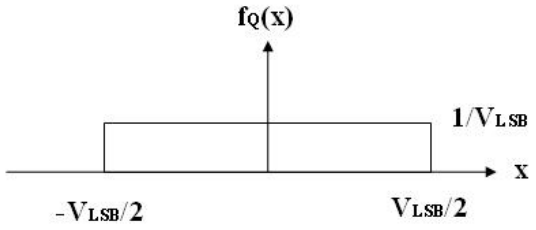

Figure 2.5: Probability density function for the quantization error.

where N is number of bit of analog-to digital converter (ADC). However, a input sinusoidal waveform between zero and V_{ref} is more commonly used in many applications. The SNR is then given by

$$SNR = 20log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20log\left(\frac{V_{ref}/2\sqrt{2}}{V_{LSB}/\sqrt{12}}\right) = 20log\left(\sqrt{\frac{3}{2}}2^N\right) = 6.02N + 1.76dB. \tag{2.5}$$

2.2.2 Thermal Noise

The random motion of electrons in a conductor introduces thermal noise. Thus, the thermal noise power is proportional to the absolute temperature. In a resistor R, thermal noise power can be modeled by a series voltage source V^2 or by a shunt current generator i^2 as shown in Figure 2.6. These representations are equivalent and

$$v^2 = 4kTR\Delta f \tag{2.6}$$

$$i^2 = 4kT\frac{1}{R}\Delta f \tag{2.7}$$

For MOS transistor, the resistive channel under gate is modulated by the gate-source voltage so that the drain current is controlled by the gate-source voltage. Since the channel material is resistive, it exhibits thermal noise. It can be proved [19] that for long-channel MOS devices operating in saturation region, the channel noise can be modeled by a current source connected between the drain and source terminals with a spectrum density:

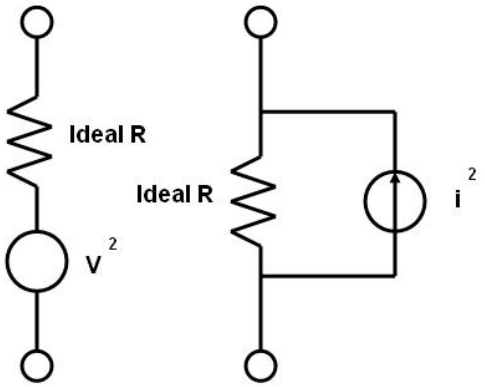

Figure 2.6: Alternative representations of thermal noise.

$$I_n^2 = 4kT\gamma/R_{ch} \tag{2.8}$$

where R_{ch} is channel resistance, and γ is equal to 2/3 for long-channel transistors and may vary with different technologies.

There has been some work on modeling thermal noise for short-channel trnasistors [20–22]. However, the thermal noise behavior of short-channel MOSFETs in the saturation region is not well understood and controversial. The theoretical determination of γ is still under research. Since this project is implemented with CMOS 0.18um technology, the γ is assumed to be equal 2/3 with hand analysis and then be verified by simulation. The R_{ch} in (2.8) is also equal to $1/g_m$, where g_m is transconductance of MOS transistor. A more general expression of thermal noise for MOSFETs is also given

$$V_n^2 = \frac{8}{3}kT\frac{1}{g_m} \tag{2.9}$$

2.2.3 1/f Noise

In the MOSFET, 1/f noise is caused mainly by the random trapping and detrapping process of charges in the oxide traps associated with contamination and crystal defects near the $Si-SiO_2$ interface. The charge fluctuation results in fluctuation of the surface potential

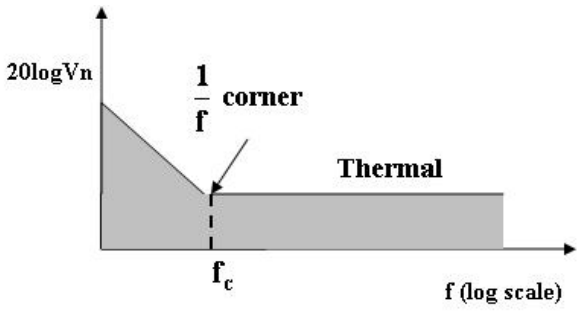

Figure 2.7: 1/f noise corner frequency.

and thus modulates the channel carrier density. Since the carrier lifetime in silicon is on the order of tens of microseconds, the resulting current fluctuations are concentrated at lower frequencies [23]. Typically PMOS transistors have less 1/f noise than NMOS transistors since their majority carriers (holes) are less likely to be trapped. The average power of 1/f noise cannot be predicted easily, it depends on the "cleanness" of the oxide-silicon interface. The 1/f noise can be modeled as a voltage source in series the gate and roughly given by

$$V_n^2 = \frac{K}{C_{ox}WL}\frac{1}{f} \tag{2.10}$$

where K is a process-dependent constant and depends on device characteristics, C_{ox} is gate oxide capacitance per unit area, and WL is the area for MOS transistor. An important point to note here is that the 1/f noise is inversely proportional to the transistor area, WL. In other words, larger devices results in less 1/f noise. 1/f noise is extremely important in biomedical applications, because it typically dominates at low frequencies. If we plot both thermal noise and 1/f noise on the same axes as shown in Figure 2.7, the intersection point between both noise sources is called 1/f noise corner frequency. The 1/f noise corner, f_C, can be found as

$$\frac{8}{3}kT\frac{1}{g_m} = \frac{K}{C_{ox}WL}\frac{1}{f_C}, \tag{2.11}$$

that is,

$$f_C = \frac{K}{C_{ox}WL}g_m\frac{3}{8kT}. \tag{2.12}$$

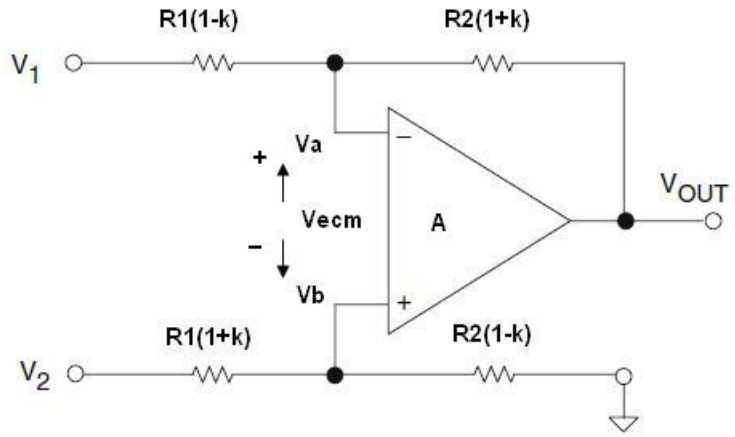

Figure 2.8: Schematic of Differential Amplifier.

This implies that f_C depends on the device dimensions WL and bias current through g_m. Thus, the tradoff between noise and power or die area are challenges for circuit design.

Chopping techniques for 1/f reduction is widely used in biomedical application [6, 7, 24, 25]. In this project, this technique is applied, and the detailed description is given in next chapter.

2.3 Common Mode Rejection Ratio

The common mode signal at 50/60 Hz from power line is another noise for bio-potential signal acquisition system. Thus, an IA is designed with high CMRR to reject any common mode signals from outside world. The CMRR is defined as [26]

$$CMRR = \frac{A_{DM}}{A_{CM}}. \tag{2.13}$$

where A_{DM} is differential gain, and A_{CM} is common mode gain. A good example of high CMRR design is the traditional 3-op IA as discussed in Chapter 1. A key point of this topology is the differential amplifier or subtractor for common-mode signal rejection and differential-mode signal amplification. The A_{CM} of differential amplifier is zero, if

$R_1(1-k) = R_1(1+k)$, and $R_2(1-k) = R_2(1+k)$ with k =0 as shown in Figure 2.8, where k is individual resistor tolerance in fractional form. If the resistors R_1 and R_2 are not matched well, and $V_1 = V_2 = V_{cm}$, the voltages V_a and V_b can be found by

$$V_a = \frac{R_2(1+k)}{R_1(1-k)+R_2(1+k)}V_{cm}. \tag{2.14}$$

$$V_b = \frac{R_2(1-k)}{R_1(1+k)+R_2(1-k)}V_{cm}. \tag{2.15}$$

since the error voltage V_{ecm} at the input terminals of amplifier is equal to $V_a - V_b$, the output voltage V_{ocm} due to V_{ecm} can be expressed as

$$\begin{aligned} V_{ocm} &= V_{ecm} \times \frac{R_1(1-k)+R_2(1+k)}{R_1(1-k)} \\ &= V_{cm}\left(\frac{R_2(1+k)}{R_1(1-k)+R_2(1+k)} - \frac{R_2(1-k)}{R_1(1+k)+R_2(1-k)}\right) \\ &\times \left(\frac{R_1(1-k)+R_2(1+k)}{R_1(1-k)}\right) \end{aligned} \tag{2.16}$$

Thus, the common gain A_{CM} is

$$\begin{aligned} A_{CM} &= \frac{V_{ocm}}{V_{cm}} \\ &= \left(\frac{R_2(1+k)}{R_1(1-k)+R_2(1+k)} - \frac{R_2(1-k)}{R_1(1+k)+R_2(1-k)}\right)\left(\frac{R_1(1-k)+R_2(1+k)}{R_1(1-k)}\right) \\ &= \frac{R_2}{R_1}\left(\frac{1+k}{1-k} - \frac{R_1(1-k)+R_2(1+k)}{R_1(1+k)+R_2(1-k)}\right) \\ &= \frac{R_2}{R_1}\left(\frac{(1+k)^2R_1-(1-k)^2R_1}{R_1(1+k)(1-k)+R_2(1-k)^2}\right) \\ &\cong \frac{R_2}{R_1}\frac{4kR_1}{R_1+R_2} \\ &\cong \frac{4kR_2}{R_1+R_2} \end{aligned} \tag{2.17}$$

Since the differential gain $A_{DM} = R_2/R_1$, the CMRR is

Table 2.2: CMRR for different mismatching error in resistors R_1 and R_2, and assuming $R_1 = R_2$

k	1%	0.1%	0.01%	0.001%
CMRR (dB)	34	54	74	94

$$\begin{aligned} CMRR &= \frac{A_{DM}}{A_{CM}} \\ &= \frac{R_2}{R_1}\frac{R_1+R_2}{4kR_2} \\ &= \left(1+\frac{R_2}{R_1}\right)\frac{1}{4k} \end{aligned} \tag{2.18}$$

With a mismatching error of k=1% in resistor ratios, the CMRR is 34 dB using (2.18), and assuming $R_1 = R_2$. Table 2.2 summaries the CMRR corresponding to the percentage error of k in resistor ratios. According to the table 2.2, the mismatching error k should be less than 0.01% in order to meet the specification. Due to mismatching between resistors, an error voltage V_{ir} at the input is generated and can be obtained by

$$V_{ir} = \frac{V_{IN}}{CMRR_r}. \tag{2.19}$$

Thus, the error voltage at the output V_{or} can be expressed by

$$\begin{aligned} V_{or} &= \frac{1}{\beta}(V_{IN} - V_{ir}) \\ &= \frac{1}{\beta}\left(1-\frac{1}{CMRR_r}\right)V_{IN} \end{aligned} \tag{2.20}$$

where β is $R_1/(R_1+R_2)$, and $CMRR_r$ is CMRR due to mismatching between resistors. If there is another offset voltage at the input due to the amplifier gain error, the total output voltage error is then given by

$$\begin{aligned} V_{or} &= \frac{1}{\beta}\left(1-\left(\frac{1}{CMRR_a}+\frac{1}{CMRR_r}\right)\right)V_{IN} \\ &= \frac{1}{\beta}\left(1-\frac{1}{CMRR_{Total}}\right)V_{IN} \end{aligned} \tag{2.21}$$

where $CMRR_a$ are CMRR for amplifier gain error, and $1/CMRR_{Total} = 1/CMRR_r + 1/CMRR_a$. Since most of IA design are differential topology, the mismatching between input stages should be carefully considered.

2.4 Input Common Mode Range

Due to electrochemical effects at the skin-electrode interface, dc offsets of ±0.3 V are common across differential recording electrodes [1]. An IA with wide input common mode range is needed in order to reject the common mode interference of ±0.3 V. Source degeneration is widely used to provide good linearity over wide input common range [27,28]. The schematic of a typical source degeneration design for bio-medical applications is shown at the left of Figure 2.9. The transconductance g_m is $2/R_{in}$ and is linear over a wide input common mode range. However, the noise at the input due to the extra resistor R_{in} is increased to $4kTR_{in}/2$.

Another technique to improve linearity is also presented in [29, 30]. The basic idea is to generate an offset voltage at the inputs by sizing the different transistors Q_1 and Q_3 as shown at the right of Figure 2.9. The output currents I_{C1} and I_{C3} are plotted at the top of Figure 2.10 when a differential input voltage is applied. The current I_{SUM} is the summation of I_{C1} and I_{C3}. The total transconductance g_m is derivative of I_{SUM} with respective to input voltage and is plotted at the bottom of Figure 2.10. As a result, the transconductance g_m is linear over an input range ±40 mV. However, the total noise is almost twice that of a single differential pair.

In this thesis, one major novel contribution is the design of a pre-amplifier, described in chapter 4, with wide input common mode range and high CMRR in order to meet the specifications based on the requirements of Table 2.1.

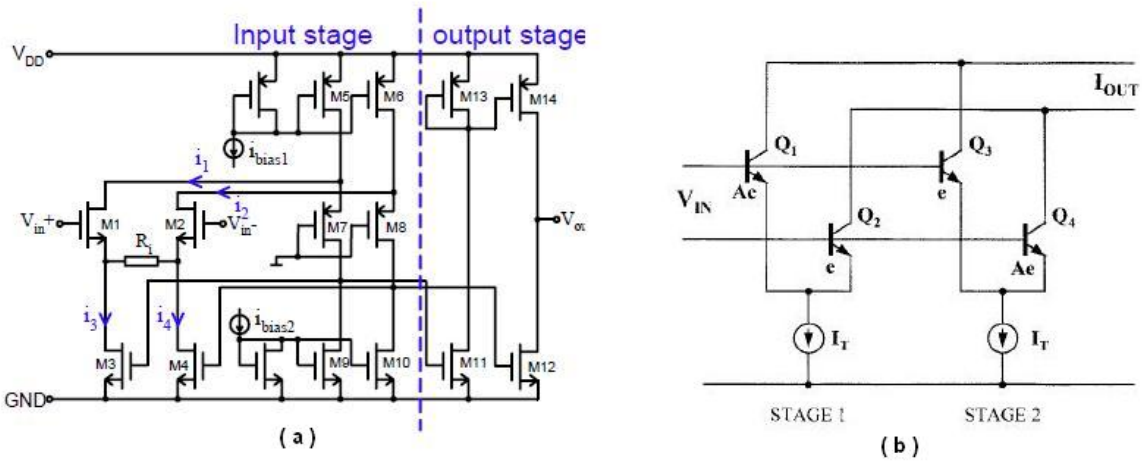

Figure 2.9: (a) Schematic of Source Degeneration. (b) Schematic of Offset Ttechnique.

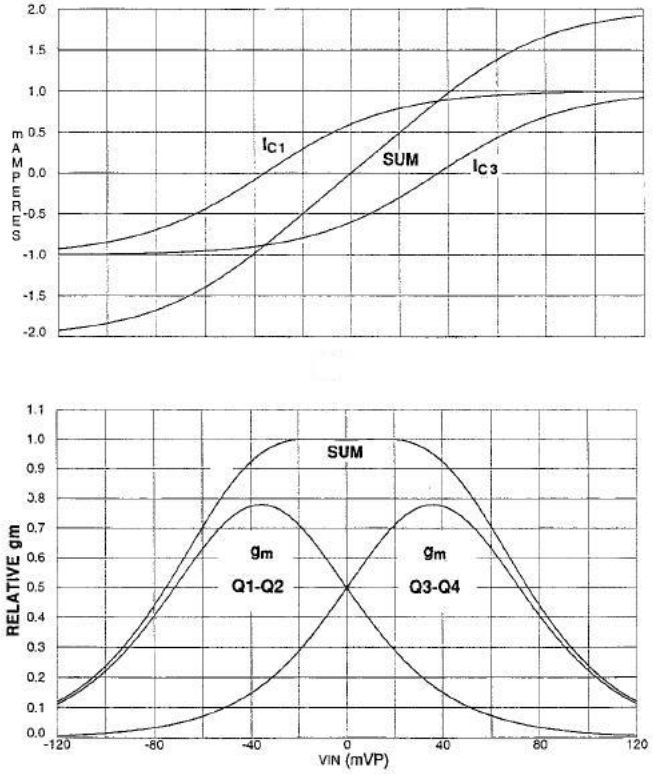

Figure 2.10: Currents plot offset Technique at the top. Transconductances plot at the bottom.

Chapter 3

Sigma-Delta ADC Architecture

Several topologies for bio-potential applications are investigated in Chapter .1. With traditional 3-op amp IA or AD620 IA design [2], the resistors mismatching is an issue for high CMRR as discussed in section 2.3. Lower mismatching resistors can be achieved by trimming technique, however, it increases the budget for the project. An ADC is also needed to digitize the analog signal to digital format, and to communicate over shared digital buses.

The AC-couple with pseudoresistor is also discussed in Chapter .1 [4]. The impedance of pseudoresistor is lack of control to provide the selection for different applications. Moreover, an ADC is required to convert the analog signal to digital format for sharing by other such ICs. Since the goal of this project is to design an IC for portable biomedical application, low power design should also be considered.

The AD8553 is presented in Chapter .1 [14]. Source degeneration technique is used based on the idea of 3-op amp IA configuration. The product is designed from 1.8V to 5.5V power supplies with total current of 4 uA and input referred noise of 0.7 uVp-p from 0.01Hz to 10Hz. Although an IA can be designed with 1.8V power supply in 0.18um CMOS technology by this topology, extra circuitry is needed to program the bandwidth selection for different biomedical applications. An ADC again is also needed to translate the analog signal to digital signal.

A conventional $\Sigma\Delta$ ADC has LPF characteristic for the signal transfer function, which can saturate the integrator to most positive supply rail and severely degrade dynamic range

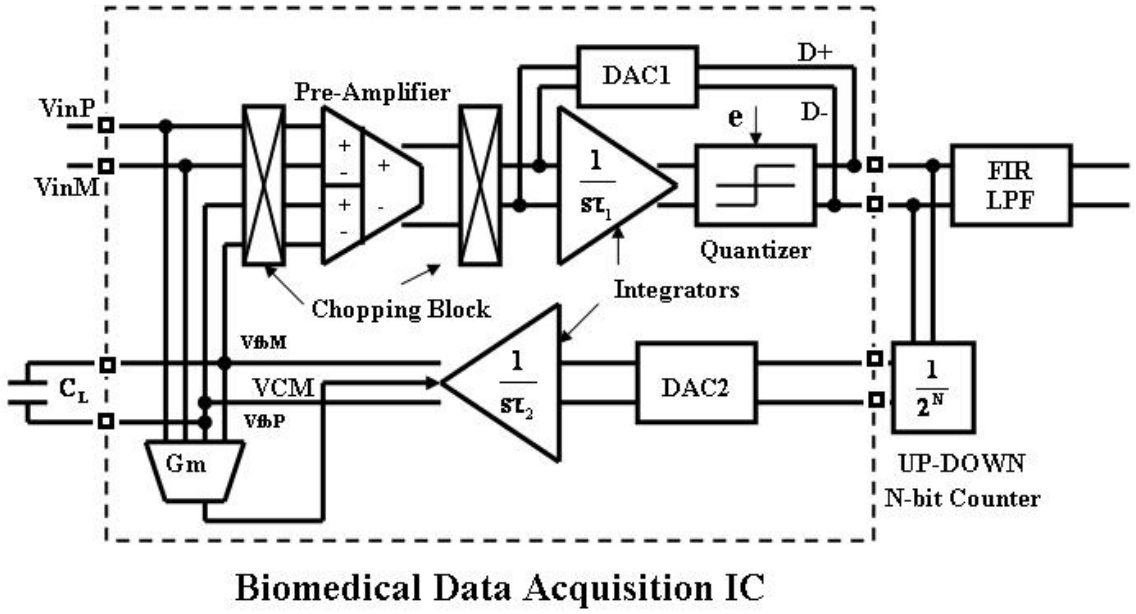

Figure 3.1: Overall System Block

due to the large offset generated at the skin-electrode interface. Thus, a 24-bit ΣΔ ADC for bio-potential acquisition system is not sufficient without an isolated buffer or HPF in the front-end. Therefore, a front-end with a buffer or HPF characteristic is needed to process very weak biomedical signals. Figure 3.1 shows the proposed ΣΔ ADC with inherent HPF signal conditioning stage. The overall system consists of an integrator and quantizer as in a conventional ΣΔ ADC, a differential difference pre-amplifier, and a feedback path with a controllable UP-DOWN counter, integrator, transconductance G_m stage, and FIR LPF.

The pre-amplifier is designed with low input referred noise 1 μVrms and high CMRR. The G_m stage provides cancellation of input common signals while alleviating the dc offsets due to electrochemical effects at the electrode-tissue interface. The first integrator, second integrator, a UP-DOWN digital counter, and a quantizer form the architecture of a second order ΣΔ ADC. The UP-DOWN counter acts as a programmable attenuator in the feedback path, since a total of 2^N digital counts must be accumulated before the feedback DAC2 bit is activated.

This chapter is organized as follows: Section 3.1 and section 3.2 state the reasons that ΣΔ ADC and chopping technique are selected for the overall system. Section 3.3 and section

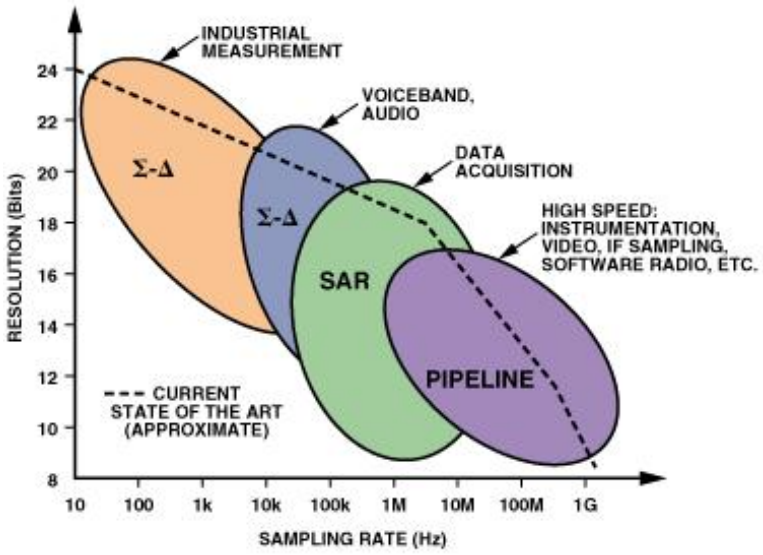

Figure 3.2: ADC architectures, applications, resolution, and sampling rates.

3.4 present the behavior of first order and second order ΣΔ ADC respectively. Final, a summary is given in Section 3.5

3.1 Motivation for Sigma-Delta ADC

ADCs can be categorized into two types based on the sampling frequency: Nyquist ADC and Oversampling ADC [31]. The Nyquist ADC requires that the sampling frequency be at least twice the highest frequency of signal. If the sampling frequency is less than twice the maximum signal frequency, the signal will be lost and the phenomena is called aliasing. The quantization noise of Nyquist ADC is evenly spread over the frequency and SNR can be obtained by (2.5). For Oversampling ADC, the samping frequency is much higher than Nyquist ADC, and its quantization noise is pushed into high frequencies with the noise shaping property of Oversampling ADC. Thus, the SNR is different from (2.5) and is analyzed in sections 3.3 and 3.4. As a result, the resolution of oversampling ADC is higher than Nyquist ADC.

The most popular ADC architectures today for Nyquist ADC are successive-approximation-register ADC (SAR), flash, pipelined ADC, and ΣΔ ADC for Oversampling ADC. All ADC

require one or more steps involving comparison of an input signal with a reference. Figure 3.2 shows how flash, pipelined, SAR, and ΣΔ architectures differ with respect to the resolution vs. frequency.

Flash ADCs is the fastest way to digitize an analog signal to a digital signal. They are suitable for applications requiring very large bandwidths. However, flash converters consume a lot of power, have relatively low resolution, and can be quite expensive. This limits them to high frequency applications such as radar processing, sampling oscilloscopes, and high-density disk drives.

The pipelined ADC has become more popular ADC architecture for sampling rates from a few mega-samples per second (MS/s) up to 100MS/s, with resolutions from 8 to 16 bits. They offer the resolution and sampling rate to cover a wide range of applications, including CCD imaging, digital video (HDTV), cable modem, and fast Ethernet.

The SAR ADCs are widely used for medium-to-high-resolution applications, typically with sample rates fewer than 5 mega-samples per second (Msps). SAR ADCs provide low power consumption resolution from 8 to 20 bits. This combination makes them ideal for a wide variety of applications, such as portable battery-powered instruments, pen digitizers, industrial controls, and data signal acquisition.

The architecture of ΣΔ ADC takes a fundamentally different approach from the Nyquist architectures. ΣΔ ADC has high resolution, high integration, and low cost, making them a good ADC choice for applications such as Audio designs, and instrumentation.

Based on the description above, it is important to select a converter for biomedical applications. For this project, ΣΔ ADC is chosen for the benefit of low frequency and high resolution. The most important reason that ΣΔ ADC is used in this project is the noise shaping property. The quantization noise is shaped by the modulator and pushed into the frequencies above the band of interest, a digital filter then can be applied to this shaped quantization noise as shown in Figure 3.3. The purpose of the digital filter is twofold. First, it must act as an anti-aliasing filter with respect to the final sampling rate, F_S. Second, it must filter out the higher frequency noise produced by the noise-shaping process of ΣΔ modulator. Thus, the band of interest contains no quantization noise with selection of lower cutoff frequency for the filter. The behavior of ΣΔ ADC and noise effects is presented in

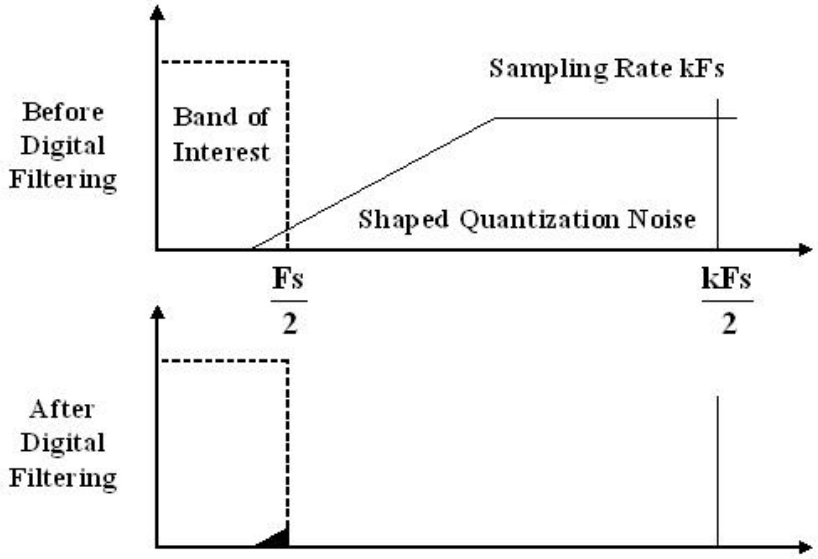

Figure 3.3: Effects of digital filtering on shaped quantization noise

section 3.3 and 3.4.

3.2 Motivation for Chopping

According the section 2.2.3, 1/f noise is inside the band of interest. Moreover, the DC offsets due to the input stage mismatching will degrade the performance of CMRR. Since bio-potential signals are located between 0.05-2000 Hz, the effects of 1/f noise and DC offsets are significant challenges to the circuit design. Autozeroing and chopping technique are widely used to reduce the noise at low frequency [24,32]. A clear distinction is made between autozeroing, which is sampling technique, and chopping, which is modulation technique. The comparison between these two techniques is shown in Figure 3.4. For autozeroing technique, the 1/f noise is reduced if the sampling frequency is much greater than 1/f corner frequency. However, the noise floor is increased due to aliasing of the wide band noise (thermal noise) inherent to the sampling precess. The total noise after autozeroing is

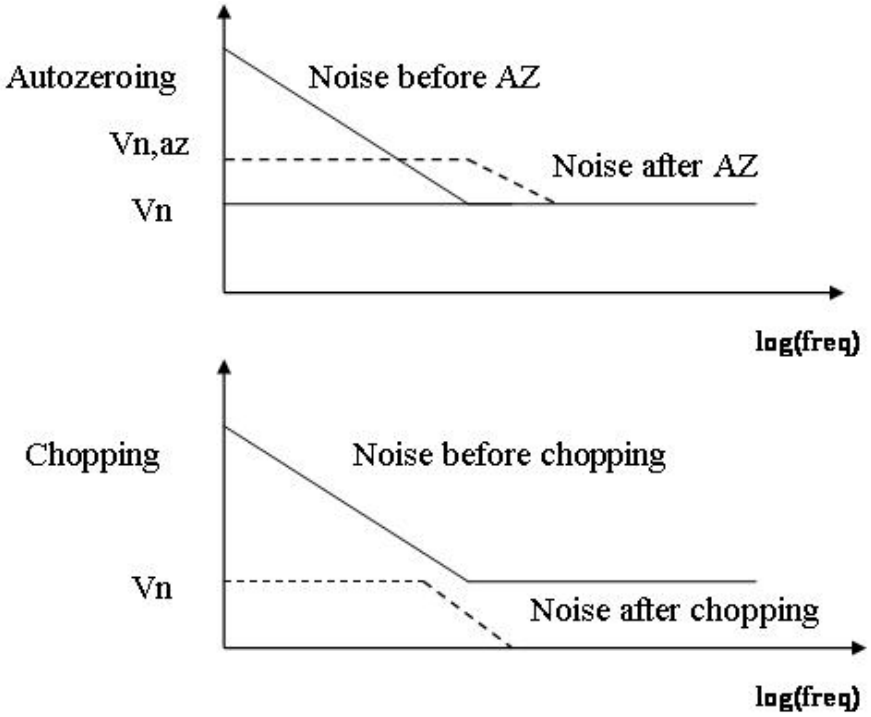

Figure 3.4: Comparison between autozeroing and chopping in the frequency domain

$$V_{n,az} = V_n\sqrt{2B/F_S}. \tag{3.1}$$

where V_n is the thermal noise, B is band of interest, and F_S is sampling frequency. The noise power increased by the under-sampling factor 2B/F_S.

For chopping technique, 1/f noise is completely removed if chopping frequency is greater than the 1/f corner frequency. the total noise after chopping is

$$V_{n,chop} \approx V_n. \tag{3.2}$$

Based on (3.1) and (3.2), chopping technique is selected for low-frequency biomedical application. The basic principle and effects of chopping technique are given in section 3.2.1 and section 3.2.2.

Another option to reduce 1/f noise is also discussed in section 2.2.3. From (2.10), large transistor area WL can reduce 1/f noise effect. A NMOS transistor with different WLs and

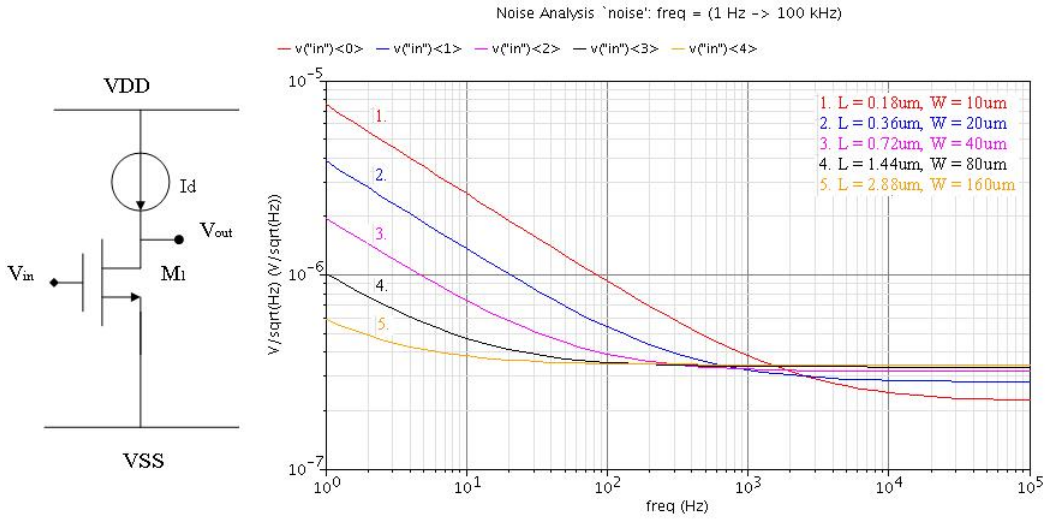

Figure 3.5: 1/f noise for different transistor WLs.

Table 3.1: Input referred noise for different WLs.

W/L (um)	10/0.18	20/0.36	40/0.72	80/1.44	160/2.88
Vrms(uV)	27.4	18.1	15.6	15.3	15

drain current of 20uA is simulated in CMOS 0.18um technology as shown in Figure 3.5. With increasing WL of trasistor M_1, the 1/f noise is reduced based on the (2.10). Table summaries the total input referred noise from 0-2kHz for different WLs of transistor M_1.

3.2.1 Basic Principle

The principle of the chopper amplifier is illustrated in Figure 3.6. An input spectrum and two stage amplifier are shown. There are two multipliers which are controlled by a chopping square wave with amplitude +1 and -1. For a periodic carrier with a period of T and 50% duty cycle, its Fourier representation is

$$m(t) = 2\sum_{k=1}^{\infty} \frac{sin(k\pi)}{\frac{k\pi}{2}} cos(2\pi f_{chop} kt). \tag{3.3}$$

Its k-th Fourier-coefficients, M_k, have the properties

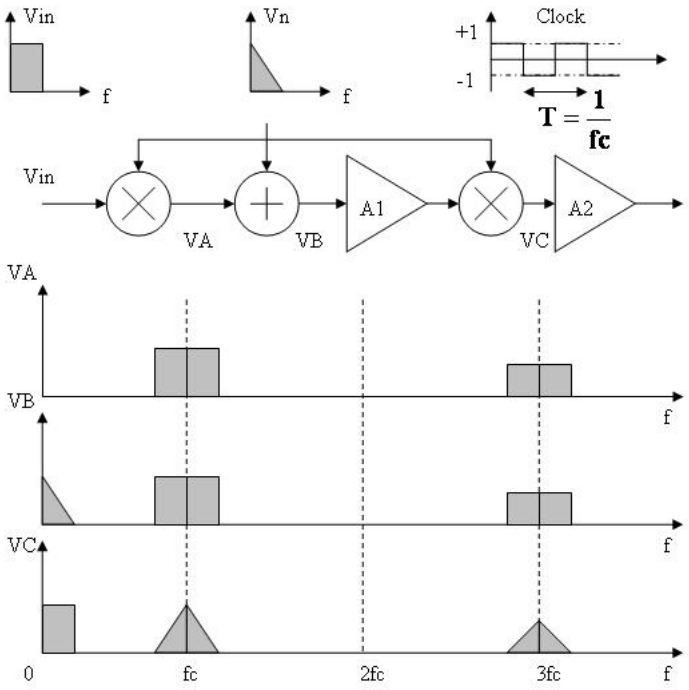

Figure 3.6: Illustration of the concept of chopper to remove the undesired signal, Vn from the desired signal, Vin.

$$m_k = \begin{cases} 0, & \text{if } k \text{ is even} \\ \frac{4}{\pi k}, & \text{if } k \text{ is odd} \end{cases} \tag{3.4}$$

After the first multiplier, VA, the signal is modulated and translated to the odd harmonic frequencies of the chopping square wave. At VB node, the undesired signal Vn, which represents sources of noise or DC offsets, is added the spectrum as shown in Figure 3.6. After the second multiplier, VC, the signal is demodulated back to the original one, and the undesired signal has been modulated as

$$S_{cs}(f) = \sum_{k=-\infty}^{\infty} |M_{2k+1}|^2 S_N(f - \frac{2k+1}{T}) = (\frac{2}{\pi})^2 \sum_{k=-\infty}^{\infty} \frac{1}{(2k+1)^2} S_N(f - \frac{2k+1}{T}). \tag{3.5}$$

where the $S_N(f)$ denotes the power spectrum density of noise and DC offsets and can be written in the following convenient form:

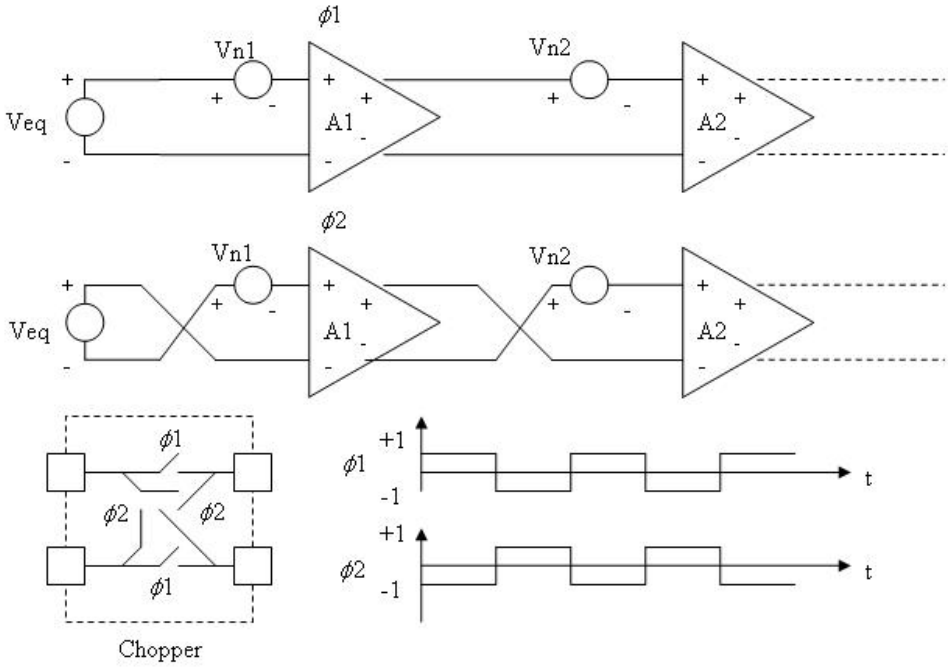

Figure 3.7: Circuit implementation for chopper technique in time domain.

$$S_N = S_0(1 + \frac{f_C}{f}). \tag{3.6}$$

where S_0 is the thermal in (2.9), and f_C is the 1/f noise corner frequency in (2.12). As a result, the spectrum of the undesired signal has been shifted to the odd harmonic frequencies of the chopping square wave. If the chopper frequency f_c is much greater than the signal bandwidth, the undesired signal will be greatly reduced. Since the undesired signal signal will contain 1/f noise and dc offsets of the amplifier, the influence of this source of undesired signal is mixed out of the desired range of operation.

Another way to interpret the principle of chopper technique in time domain is shown in Figure 3.7. The multipliers are implemented by two cross-coupled switches, which are controlled by two nonoverlapping clocks ϕ_1 and ϕ_2. During ϕ_1, the equivalent noise V_{eq} is equal to the input noise of the first stage plus that of the second divided by the gain of the first stage. Thus, the equivalent noise at the input is given

$$V_{eq}(\phi_1) = V_{n1} + \frac{V_{n2}}{A_1}. \tag{3.7}$$

During ϕ_2, the equivalent noise is equal to the negative of the previous value plus that of the second divided by the the gain of the first stage. The equivalent noise at the input is

$$V_{eq}(\phi_2) = -V_{n1} + \frac{V_{n2}}{A_1}. \tag{3.8}$$

According to (3.7) and (3.8), the average equivalent noise over the entire period is

$$V_{eq}(averag) = \frac{V_{eq}(\phi_1) + V_{eq}(\phi_2)}{2} = \frac{V_{n2}}{A_1}. \tag{3.9}$$

The input noise of the first stage, V_{n1}, is completely removed by the chopping technique while the input noise of second stage, V_{n2}, is reduced by the factor of gain A_1 of the first stage. If the gain of the first stage is high enough, the contribution of the noise from second stage become negligible.

3.2.2 Effects of Chopping

The effect of chopping on both thermal noise and 1/f noise is analyzed in this section. Assuming f_m is the cut-off frequency of the main amplifier A_1 in Figure 3.6. Typically, f_m equals five times the chopper frequency $f_{chop} = 1/\mathrm{T}$. In baseband ($|fT| \leq 0.5$), $S_{cs}(f)$ in (3.5) can be approximated by a thermal noise PSD

$$S_{cs-thermal}(f) \cong S_{cs-thermal}(f=0) = S_0(1 - \frac{tanh(\frac{\pi f_m T}{2})}{\frac{\pi f_m T}{2}}). \tag{3.10}$$

and for $f_m T \gg 1$, $S_{cs-thermal}$ can be further approximated by

$$S_{cs-thermal}(f) \cong S_0. \tag{3.11}$$

If $|fT| \leq 0.5$ and $f_m T \gg 1$. Therefore, the baseband PSD of the noise is nearly constant for large f_m of the main amplifier. For 1/f noise, the input PSD is given by

$$S_{N-1/f}(f) = S_0 \frac{f_C}{|f|}. \tag{3.12}$$

The 1/f noise pole has disappeared from the baseband since it has been transposed to $\pm 1/T$ and to the odd harmonic of the chopper frequency based on the (3.5). Reference [24] also shows that the chopped 1/f noise can be approximated by a thermal noise component

$$S_{N-1/f}(f) \cong 0.8525 S_0 f_C T. \tag{3.13}$$

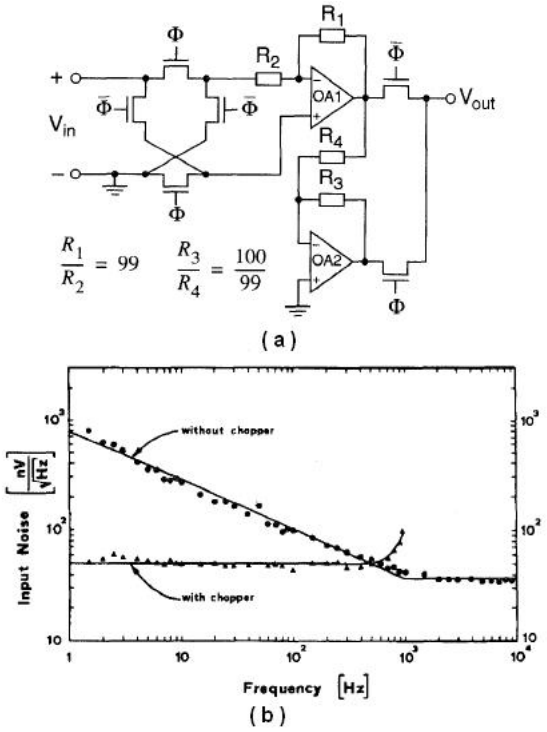

Figure 3.8: (a) Experimental chopper amplifier schematic. (OA1 and OA2 are CA3420 and uA741 respectively, and the switches are MC14016.) (b) Observed input referred PSD without and with chopper.

The total noise in the baseband can be obtained by adding (3.11) and (3.13), resulting in

$$S_{cs}(f) \cong S_0(1 + 0.8525 S_0 f_C T). \tag{3.14}$$

If the $fT \leq 0.5$ and $f_C T \gg 1$. This has been verified experimentally on a breadboard circuit with f_{chop}=f_C=1 KHz. The thermal noise without chopping was estimated to be 37 nV/$\sqrt{(Hz)}$, and the theoretical thermal noise with chopping from (3.14) was 50.4 nV/$\sqrt{(Hz)}$ which is very close to the observed result shown in Figure 3.8.

3.2.3 Effect on Residual Offset

If the modulators are realized with MOS switches, then unwanted charges are injected into the circuit when the transistors turn off. These non-idealities are charge injection and clock feedthrough and cause residual offset (or spikes) at the input of the main amplifier. This residual offset voltage will be amplified then demodulated by the output modulator. A

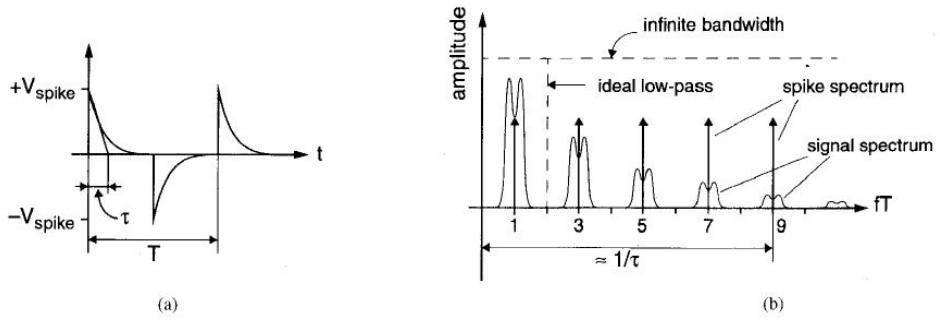

Figure 3.9: (a) Spike signal at the input signal and causing residual offset.(b) Spike signal and chopper-modulated spectra with amplifier bandwidth characteristics.

typical spike signal in time domain is shown in Figure 3.9. Figure 3.9(a) is the spike signal at the input of the amplifier, and Figure 3.9(b) is the spike signal and input signal spectrum in the frequency domain. τ is the time constant of parasitic spikes and T represents the period of chopping. Since the τ is generally much small than T/2, most of spike appears at frequencies higher than the chopping frequency. Assuming that the output modulator is ideal, the output offset is given by [33]

$$V_{offset,out} = -\sum_{n=-\infty}^{\infty} \frac{2}{j\pi n} j2\pi n \frac{t_0}{T} A(\frac{n}{T}) V_{spike}(\frac{n}{T}) \tag{3.15}$$

where t_0 is a possible delay between the input and output modulation signals to compensate for the phase shift introduced by the amplifier, n is odd based on (3.3), A is gain of amplifier and

$$V_{spike}(f) = -\sum_{n=-\infty}^{\infty} \delta(f - \frac{k}{T}) \frac{2\tau}{T} \frac{V_{spike}}{1 + j2\pi f\tau}. \tag{3.16}$$

is bilateral Fourier transform of the spike signal of Figure 3.9(a). The input referred offset can be obtained assuming that $\tau \ll T/1$ and (3.15) reduces to:

$$V_{os} \cong \frac{2\tau}{T} V_{spike}. \tag{3.17}$$

where V_{spike} is the amplitude of the spikes at the chopper amplifier input as shown in Figure 3.9(a). In the case of an ideal low-pass amplifier with gain A and a bandwidth

limited to $2f_{chop}$, the offset becomes

$$V_{os} \cong (\frac{2\tau}{T})^2 V_{spike}. \tag{3.18}$$

which is much smaller than that given by (3.17), since the τ has been assumed to be much smaller than T/2. Therefore, the offset can be reduced drastically by limiting the bandwidth of the amplifier to twice that chpooer frequency. Other techniques such as [25, 34–36] are introduced to reduce the effect of spikes. Since the input offset can be reduce by limiting the bandwidth of amplifier, the methods above are not used in this project. The non-idealities of modulators are discussed in next chapter.

3.3 First Order Sigma-Delta ADC

Although the ΣΔ modulator was first introduced in 1962 [37], it did not gain attraction until recent developments in digital VLSI technologies which provide the practical means to implement the large digital signal processing circuitry. The increasing use of digital techniques in communication and audio application has also contributed to the recent interest in cost effective high precision A/D converters. A requirement of analog-to-digital A/D interfaces is compatibility with VLSI technology, in order to provide for monolithic integration of both the analog and digital sections on a single die. In this section , the first order ΣΔ ADC in discrete and continuous time domains are reviewed respectively.

3.3.1 Discrete Time Implementation

Consider the first-order loop shown in Figure 3.10, the 1-bit quantizer is modeled as an additive noise source. The Vout can be expressed as

$$Vout(z) = z^{-1}Vout(z) + Vin(z) - z^{-1}D(z). \tag{3.19}$$

and can be solved D(z) as

$$D(z) = Vin(z) + (1 - z^{-1})e(z). \tag{3.20}$$

Based on the equation (3.20), the signal transfer function is

$$STF = 1. \tag{3.21}$$

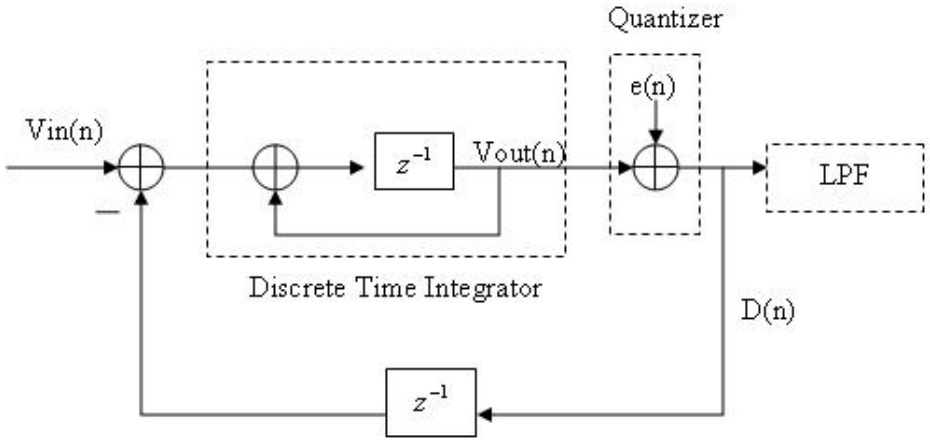

Figure 3.10: First order ΣΔ ADC in discrete time domain model

and noise transfer function is given by

$$NTF = (1 - z^{-1}). \tag{3.22}$$

By setting $z = e^{j2f\pi}$, the squared magnitude of NTF in the frequency is given by

$$|NTF(e^{j2f\pi})|^2 = |2sin(\pi f)|^2. \tag{3.23}$$

where f is normalized frequency f/F_S. For frequencies which satisfy $f \ll 1$, $|NTF|^2 \approx (2\pi f)^2$. Figure 3.11 illustrates the frequency response of the NTF. The quantization error has been pushed towards high frequencies due to the $(1 - z^{-1})$ factor. Therefore the analog input signal Vin(t) is oversampled, and the high-frequency quantization noise is removed by digital LPF without affecting the input signal characteristics in baseband.

Based on the discussion on sections 2.2.1 and 3.1, the goal of SNR is completely determined by the thermal noise. However, it is necessary to find out the SNR for ΣΔ ADC in order to meet the noise specification for overall system. The quantization noise power over frequency band from 0 to f_0 is given by

$$P_{noise} = \int_0^{f_0} V_{Q(rms)}^2 |NTF(f)|^2 \, df. \tag{3.24}$$

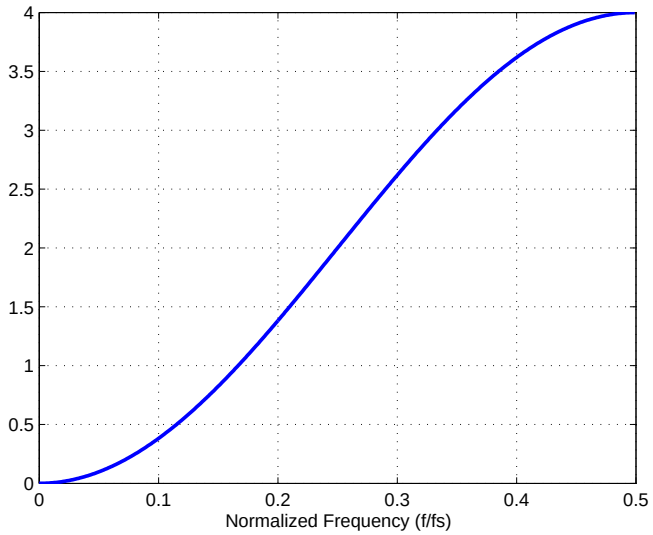

Figure 3.11: NTF plot for first order ΣΔ ADC

where the $V_{Q(rms)}$ is quantization error in (2.3), and the $|NTF(f)|^2$ is noise transfer function in (3.23). By making the approximation $f_0 \ll F_S$, we have

$$P_{noise} \cong (\frac{V_{LSB}}{12})(\frac{\pi^2}{3})(\frac{2f_0}{f_s}) = \frac{V_{LSB}^2\pi^2}{36}(\frac{1}{OSR})^3. \tag{3.25}$$

where the over sampling rate OSR $= F_S/2f_0$. Assuming the signal power for a given sinusoidal waveform with amplitude V_{ref} in (2.5) is $V_{ref}/2\sqrt{2}$, the SNR for this case is given by

$$SNR = 10\log(\frac{P_s}{P_{noise}}) = 10\log(\frac{3}{2}2^{2N}) + 10\log(\frac{3}{\pi^2}(OSR)^3). \tag{3.26}$$

or, equivalently,

$$SNR = 6.02N + 1.76 - 5.17 + 30\log(OSR). \tag{3.27}$$

Equation (3.27) shows that the SNR increases by 9 dB for each doubling of the OSR.

The waveforms of Vin(t) and D(n) for a first-order ΣΔ modulator are illustrated in Figure 3.12 when the input signal is a sinusoid with 0.5 V amplitude. In each clock cycle, the value of the output of the modulator is either logic high or logic low, according to the results of the 1-bit A/D conversion. When the sinusoidal input to the modulator is positive, the output is also positive during most clock cycles. A similar statement holds for the case

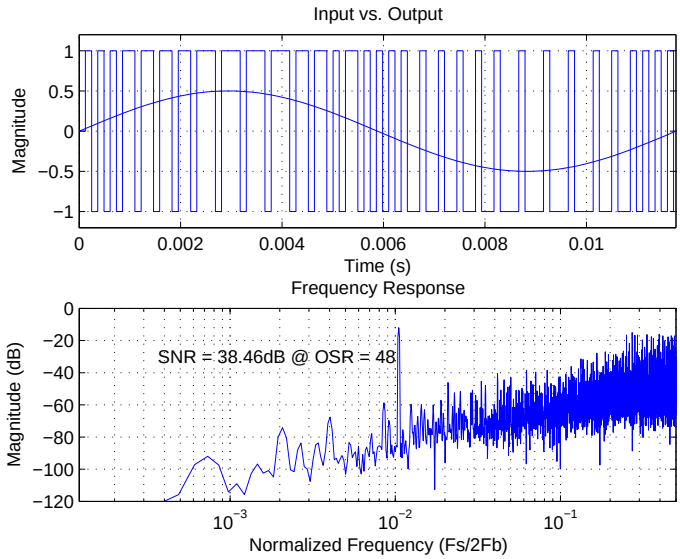

Figure 3.12: Input and Output of a First-Order ΣΔ ADC

when the sinusoid is negative. In both cases, the average of the modulator output tracks the analog input. When the input is near zero, the value of the modulator output varies rapidly between a plus and a minus values with approximately zero mean. The frequency response of output is shown at the bottom of Figure 3.12. The simulated SNR of 38 dB for step size of 2 and OSR of 48 is 2 dB less than the value of 40 dB predicted by (3.26) with amplitude of 0.5 V.

3.3.2 Continuous Time Implementation

The first order ΣΔ ADC can be also modeled as linear system in time domain as shown in Figure 3.13, where Vin is input signal, e is quantization error and D is digital output. From Figure 3.13, the digital output D can be expressed as

$$D(s) = \frac{1}{1+s\tau} Vin(s) + \frac{s}{1+s\tau} e. \tag{3.28}$$

where τ is time constant of integrator. Based on the equation (3.28), the signal transfer function is

$$STF = \frac{1}{1+s\tau}. \tag{3.29}$$

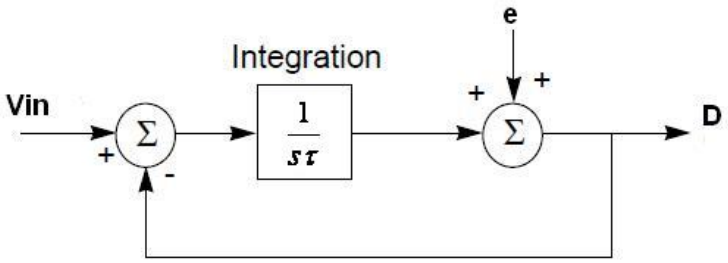

Figure 3.13: First order ΣΔ ADC in continuous time domain model

and noise transfer function is given by

$$NTF = \frac{s\tau}{1 + s\tau}. \tag{3.30}$$

Figure 3.14 is the plot for signal and noise transfer functions. Notice that the signal and noise transfer functions are LPF and HPF respectively. As we expected, the signal passes the ADC while the quantization noise is pushed into high frequencies.

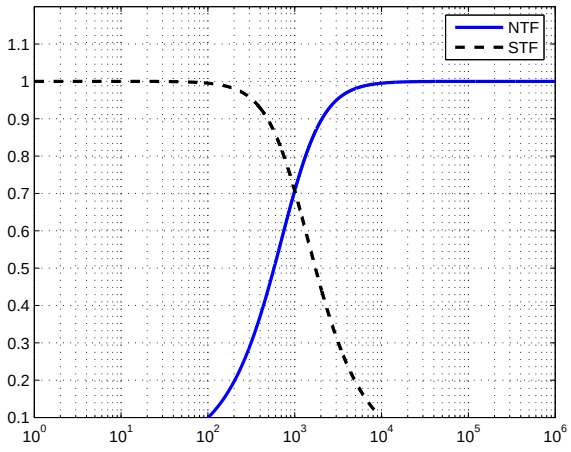

Figure 3.14: STF and NTF plot for first order ΣΔ ADC

Table 3.2: First order ΣΔ ADC operation for input signal = 1/3.

n	0	1	2	3	4	5	6
Vout(n)	1/3	-1/3	1	1/3	-1/3	1	1/3
D(n)	1	-1	1	1	-1	1	1

3.3.3 The Effects of Idle Tone

The periodic sequences generated by the DC inputs are introduced in this section. Consider the behavior of first order ΣΔ ADC in Figure 3.10. From the block diagram, Vout(n) is

$$Vout(n) = Vout(n-1) + Vin(n) - D(n-1). \tag{3.31}$$

and

$$D(n) = sgn(Vout(n)). \tag{3.32}$$

By combining the equations above,

$$Vout(n) = Vout(n-1) + Vin(n) - sgn(Vout(n)). \tag{3.33}$$

Now assume that the input signal Vin is 1/3, and also Vout(0) = 1/3. Then D(0) = 1, Vout(1) = 1/3+0-1=-2/3 and D(1)=-1. The results of Vout and D are summarized in Table 3.2 for n=0 to 6. The average value of digital output D for a full period is (-1+1+1)/3=1/3, which is identical to the input signal Vin. Thus, the output pattern is three cycles long and its power is located at dc and $F_S/3$.

Now consider applying a dc level of (1/3+1/9)=4/9 to the same modulator. For this case, the output sequence becomes

$$D(n) = 1, -1, 1, 1, 1, -1, 1, 1, -1, 1, 1, 1, -1, 1, 1, 1, -1, 1, 1, -1, 1, ... \tag{3.34}$$

The period of this output pattern is 16 cycles and has power at $F_S/16$. The periodic sequences generated by the dc input are sometimes called pattern noise, idle tones, or limit cycles [38]. This amplitude does not change with time and its frequency and it depends on the input. Based on the argument above, it is easy to find a tone at lower frequencies. If a tone say $F_S/250$ is inside band of interest, it could be a problem for next stage LPF

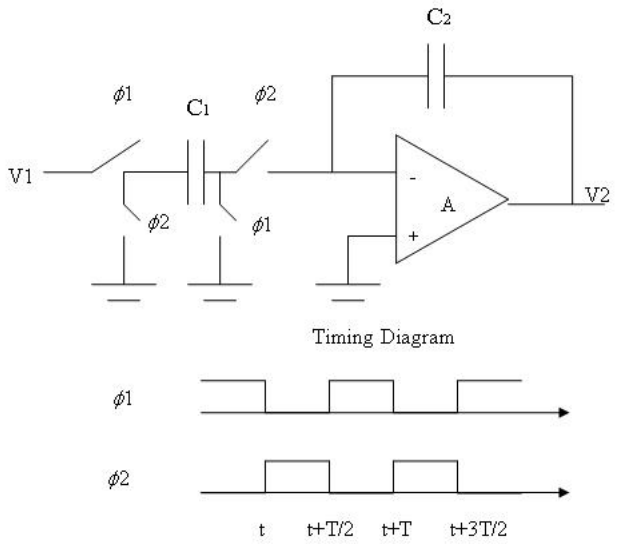

Figure 3.15: A swithed-capacitor implementation of first order ΣΔ ADC

to filtered it out. One way to reduce the effect of idle tone in the modulator is through the use of dithering. By adding the dithering signal just before the quantizer, the idle tone will break up so that they never occur. However, the noise power of the dithering signal is similar to the quantization noise power, the total noise power increases about 3 dB based on [18].

3.3.4 The Effects of Finite Op-Amp Gain

A switch-capacitor integrator with finite op-amp gain is shown in Figure 3.15. There are two non-overlapping clock waveform, ϕ_1 and ϕ_2. When t=t, the charges store in capacitors C_1 and C_2 are

$$q_1(t) = C_1 V_1(t) \tag{3.35}$$

$$q_2(t) = C_2(V_2(t) + V_2(t)\frac{1}{A}) \tag{3.36}$$

when t=t+T/2, the charges store in C_1 and C_2 are

$$q_1(t+\frac{T}{2}) = -C_1(-V_2(t+\frac{T}{2})\frac{1}{A}) \tag{3.37}$$

$$q_2(t+\frac{T}{2}) = C_2 V_2(t+\frac{T}{2})(1+\frac{1}{A}) \tag{3.38}$$

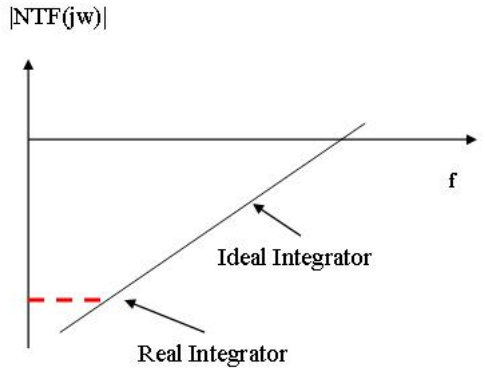

Figure 3.16: Finite Op-Amp gain effect for NTF

By charge conservation, the total charges at t=t+T/2 are equal to those at t=t. Thus, $q_2(t+T/2)+q_1(t+T/2) = q_1(t)+q_2(t)$, and $q_2(t+T) = q_2(t+T/2) \Longrightarrow V_2(t+T/2) = V_2(t)$. Rearranging the equations above gives

$$\begin{aligned} C_2V_2(t+T)(1+\frac{1}{A}) &= C_1V_1(t) + C_2V_2(t)(1+\frac{1}{A}) - C_1V_2(t+T)\frac{1}{A} \\ \Longrightarrow C_2V_2(z)z(1+\frac{1}{A}) &= C_1V_1(z) + C_2V_2(z)(1+\frac{1}{A}) - C_1V_2(z)z\frac{1}{A} \\ \Longrightarrow C_1V_1(z) &= V_2(z)(C_2z(1+\frac{1}{A}) - C_2(1+\frac{1}{A}) - C_1z\frac{1}{A}) \\ \Longrightarrow H(z) &= \frac{V_2(z)}{V_1(z)} \\ &= \frac{C_1}{C_2}\frac{1}{z - \frac{1}{1+\frac{C_1/C_2}{1+A}}}\frac{1}{1+(1+\frac{C_1}{C_2})\frac{1}{A}} \end{aligned} \tag{3.39}$$

As a result, the pole of the integrator moving to the left of z = 1 by an amount 1/A (If $C_1 \cong C_2$) as shown in Figure 3.16, and the gain is also changed according to (3.39). Thus, the quantization noise does not drop to zero at dc but instead levels off near dc. If the frequency band of interest, f_0 is greater than 1/A rad/sample, any further doubling of the oversampling ration will improve SNR. Finally, an approximation of minimum gian A is given

$$\frac{f_0}{F_S} > \frac{\frac{1}{A}}{2\pi}. \tag{3.40}$$

since $OSR = F_S/2f_0$, the equation 3.40 can be rewrite as

$$A > \frac{OSR}{\pi}. \tag{3.41}$$

According to [38], if the gain A is greater than OSR, the additional noise is less than 0.2 dB, and hence the effect is rarely serious.

3.3.5 The Effects of Timing Errors

Excess loop delay and clock jitter are two timing errors in ΣΔ modulators. These two timing errors will be discussed in this section.

Excess Loop Delay

Ideally DAC currents respond immediately to the quantizers clock edge, but the non-zero transistor switching time of the latched comparator (quantizer) and the DAC result in a finite delay between the comparator and the DAC [39, 40]. This delay is called Excess Loop Delay shown in Figure 3.17. Assume the system is single-bit system with clock 1 MHz, and every 100 cycles the comparator output is delayed by $t_d = 100ps$. The average power of equivalent error signal is

$$\frac{[2\frac{t_d}{T}]}{100} = 2 \times 10^{-6}. \tag{3.42}$$

which is 57 dB below the power of full-scale sine wave. Thus, the excess loop delay increases the noise floor for a given ΣΔ modulator. The excess loop delay also potentially increases the instability of the ΣΔ modulator by adding another order to the loop filter [41]. The solutions to the excess loop delay are by adding extra feedback DAC as well as an adjustment of the loop filter coefficients [38, 39].

Clock jitter

There are two clocks in a ΣΔ modulator and both can be affected by clock jitter. One of the clocks controls the decision instant of the quantizer while the other clock controls the DAC output. Since the quantization error is pushed into high frequencies, the impact

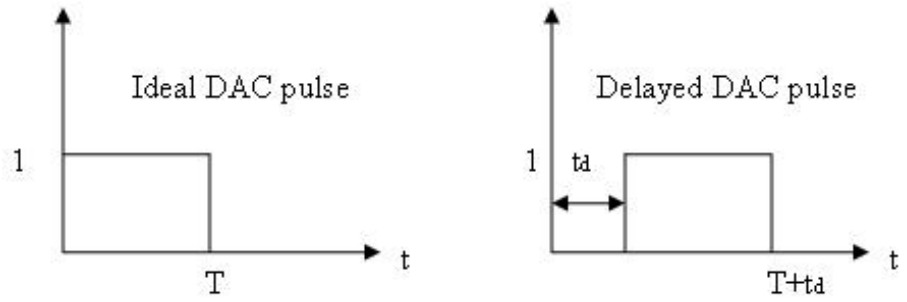

Figure 3.17: Excess Loop Delay

of this error will be relatively small. Conversely, the output of the DAC is located in band of interest, the impact of this error will affect the passband noise in the modulator. The clock jitter in the DAC manifests itself as white noise. This degrades the SNR of the $\Sigma\Delta$ modulator severely since the white noise spreads evenly across the band of interest. Therefore the clock jitter discussed will be the pulse-width clock jitter incurred in the DAC.

DT $\Sigma\Delta$ modulator is insensitive to clock jitter due to the sloping pulse form of the feedback. The clock jitter intruduces a relative small amount of error in charge lost ΔQ_D. The capacitor is discharged over a fairly steep slop as shown at the left of Figure 3.18 [42]. In constrast, CT $\Sigma\Delta$ modulator transfers charge at a constant rate over the clock period, and thus the charge loss ΔQ_c due to timing error is much greater than that of DT $\Sigma\Delta$

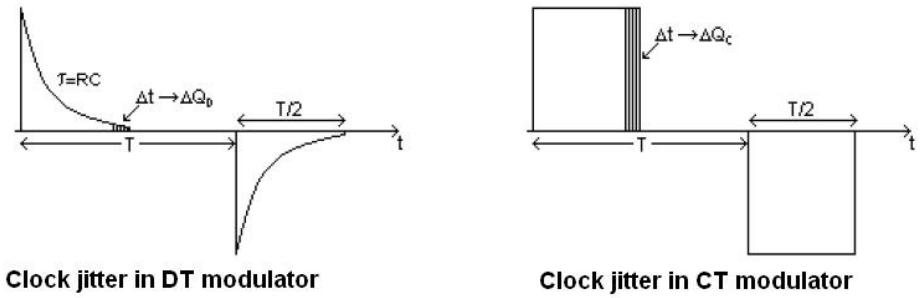

Figure 3.18: Clock jitter

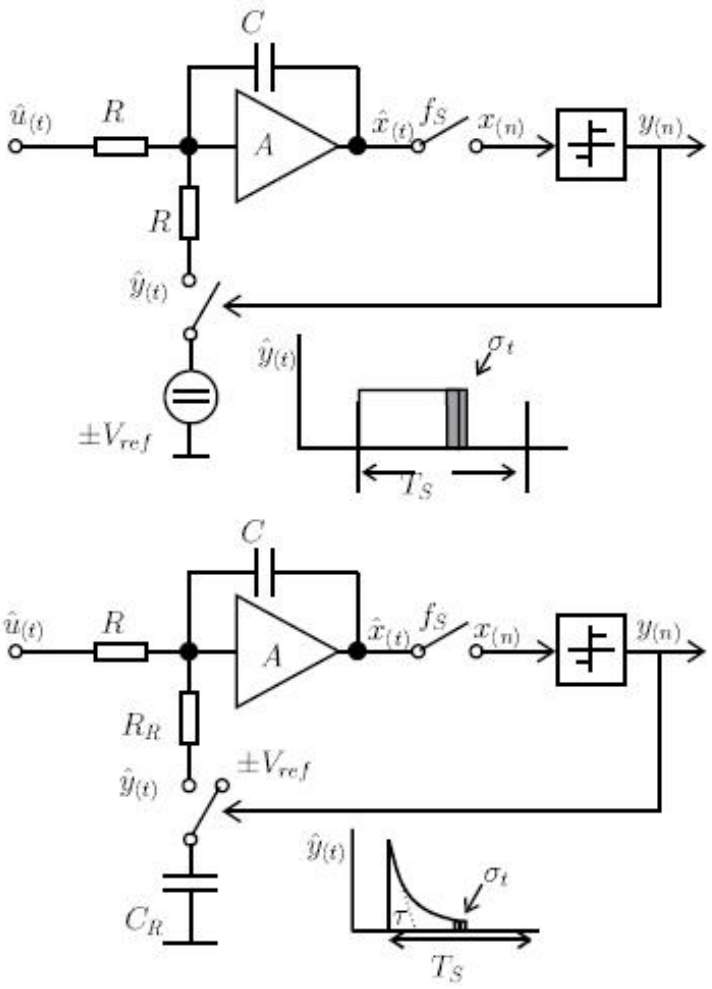

Figure 3.19: ΣΔ modulator with return to zero (RZ) and switched-capacitor-resistor (SRC) feedback

modulator shown at the right of Figure 3.18.

There are two solutions to reduce the effect of timing jitter in DAC. One of them is to increase the number of levels in feedback DAC. Another solution to the jitter problem is to change the feedback from a timing-dependent signal to a timing-insensitive signal.

ΣΔ modulator with return to zero (RZ) and switched-capacitor-resistor (SRC) feedback is shown in Figure 3.19. Due to the sloping pulse form of the SCR feedback the white noise power will be heavily reduced compared to the NRZ feedback [43]. The results for both feedbacks are shown in Figure 3.20. The PSD of output is insensitive to rms jitter of

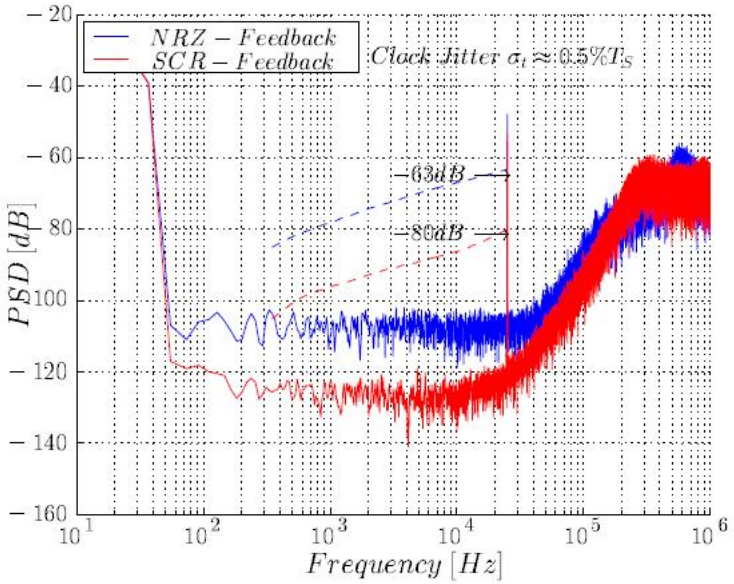

Figure 3.20: PSD for Non returen to zero (NRZ) and SRC

$\sigma_t \cong 0.5\%T$ clock jitter.

3.4 Second Order Sigma-Delta ADC

Although the second order $\Sigma\Delta$ is implemented in continuous time domain in this thesis, the overall system is first discussed in discrete time domain in section 3.4.1 and then continuous time domain in section 3.4.2.

3.4.1 Discrete Time Implementation

In this section, the second order $\Sigma\Delta$ ADC is discussed and analyzed in discrete time domain. The linear model in z domain is shown in Figure 3.21. From the figure,

$$Vfb = (\frac{1}{2^N}D)z^{-1} \tag{3.43}$$

$$Vout = (Vin - Vfb - bD + Vout)z^{-1} \tag{3.44}$$

$$D = Vout + e. \tag{3.45}$$

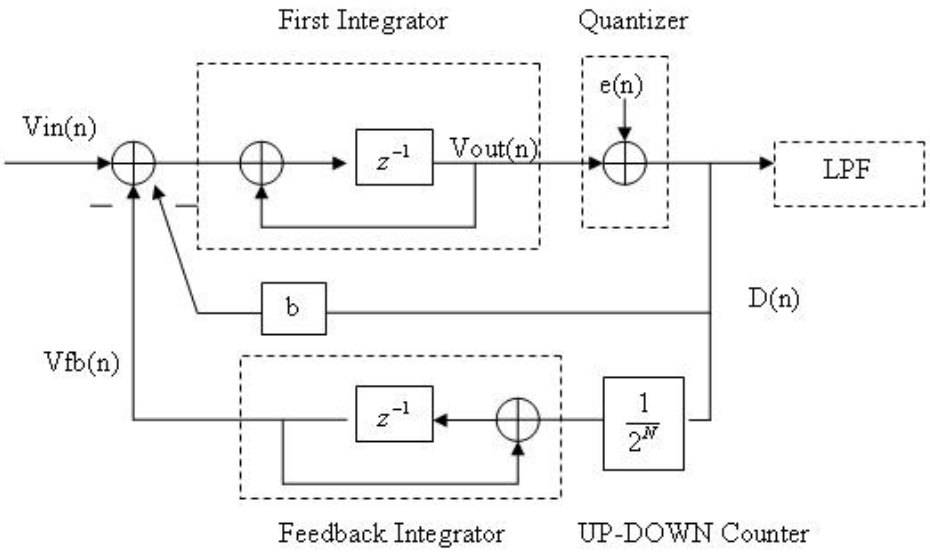

Figure 3.21: Linear model of second order ΣΔ ADC.

Rearranging the equations above gives

$$\begin{aligned} D - e &= Vinz^{-1} - \frac{z^{-1}}{1-z^{-1}}\frac{1}{2^N}D - bDz^{-1} + (D-e)z^{-1} \\ \Rightarrow D(1 + \frac{z^{-1}}{1-z^{-1}}\frac{1}{2^N} + bz^{-1} - z^{-1}) &= Vinz^{-1} + (1-z^{-1})e \\ \Rightarrow D(\frac{1-(2-b-\frac{1}{2^N}z^{-1}+(1-b+1/2^N)z^{-2})}{1-z^{-1}}) &= Vinz^{-1} + (1-z^{-1})e \\ \Rightarrow D = \frac{(1-z^{-1})z^{-1}}{1-(2-b-1/2^N)z^{-1}+(1-b+1/2^N)z^{-2}}&Vin \\ +\frac{(1-z^{-1})}{1-(2-b-1/2^N)z^{-1}+(1-b+1/2^N)z^{-2}}&e \end{aligned} \tag{3.46}$$

According to the (3.46), the STF is

$$STF = \frac{(1-z^{-1})z^{-1}}{1-(2-b-1/2^N)z^{-1}+(1-b+1/2^N)z^{-2}}. \tag{3.47}$$

and the NTF is given by

$$NTF = \frac{(1-z^{-1})}{1-(2-b-1/2^N)z^{-1}+(1-b+1/2^N)z^{-2}}. \tag{3.48}$$

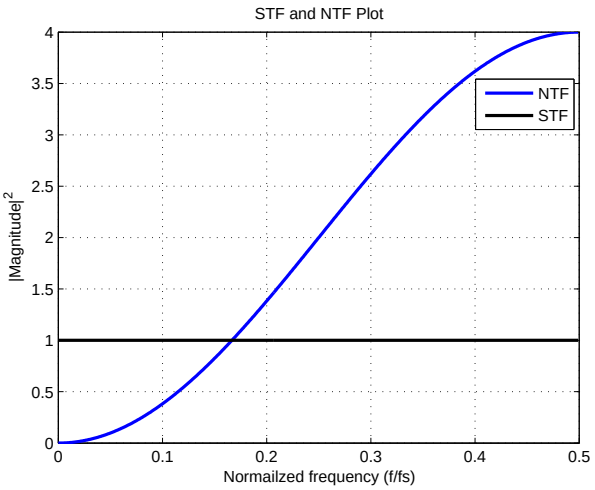

Figure 3.22: STF and NTF Plot.

If b is equal 1 and N is very large, then the term $1/2^N$ is close to zero. The STF becomes

$$STF = z^{-1}. \tag{3.49}$$

and the NTF is

$$NTF = (1 - z^{-1}). \tag{3.50}$$

The STF and NTF plots are shown in Figure 3.22. Notice that the STF is equal to one and the NTF is equal to the equation (3.22), which implies that the SNR is almost the same as first order $\Sigma\Delta$ ADC. The advantages of use of second order $\Sigma\Delta$ ADC are low-frequency cutoff control and common mode signal subtraction. With proper selection of OSR, gain, and high-frequency cutoff, the SNR of second order $\Sigma\Delta$ ADC is white noise limited for the overall system. The SNR is discussed more detailed in next section.

3.4.2 Continuous Time Implementation

Based on Figure 3.1, the second order $\Sigma\Delta$ ADC can be modeled as linear system as shown in Figure 3.23. τ_1 and τ_2 are time constants for the first and feedback integrators respectively. The UP-DOWN N-bit digital counter is modeled as $1/2^N$. The digital output is then

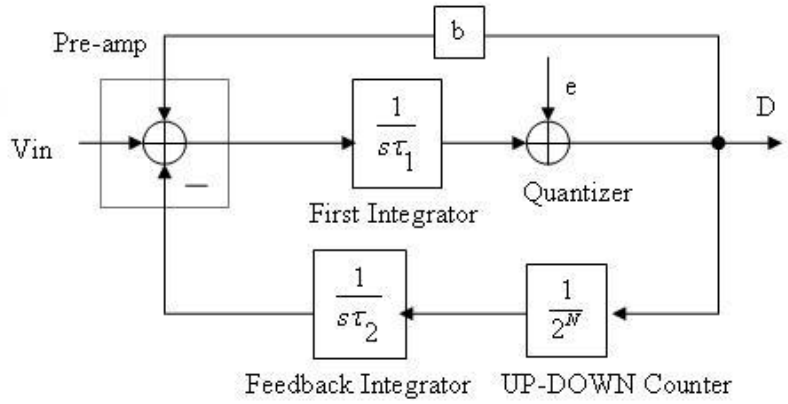

Figure 3.23: Linear model for second order ΣΔ ADC

$$\begin{aligned} Dout &= \frac{1}{s\tau_1}(Vin - Dout\frac{1}{s\tau_2 2^N} - bDout) + e \\ &= \frac{s\tau_2}{s^2\tau_1\tau_2 + bs\tau_2 + 2^{-N}}Vin + \frac{s^2\tau_1\tau_2}{s^2\tau_1\tau_2 + bs\tau_2 + 2^{-N}}e \end{aligned} \tag{3.51}$$

Based on the (3.51), the signal transfer function is

$$STF = \frac{s\tau_2}{s^2\tau_1\tau_2 + bs\tau_2 + 2^{-N}}. \tag{3.52}$$

and noise transfer function is given by

$$NTF = \frac{s^2\tau_1\tau_2}{s^2\tau_1\tau_2 + bs\tau_2 + 2^{-N}}. \tag{3.53}$$

where b is the resistive ratio between pre-amp and DAC1. According to (3.52), high-frequency pole P_H and low-frequency pole P_L are b/τ_1 and $1/(b2^N\tau_2)$ respectively. The definition of time constants τ_1 and τ_2, and the behavior of N-bit UP-DOWN counter are described in next chapter.

Figure 3.24 shows how control of the low-frequency cutoff for the proposed second order ΣΔ ADC is achieved by changing the number of bits N of the UP-DOWN counter. The

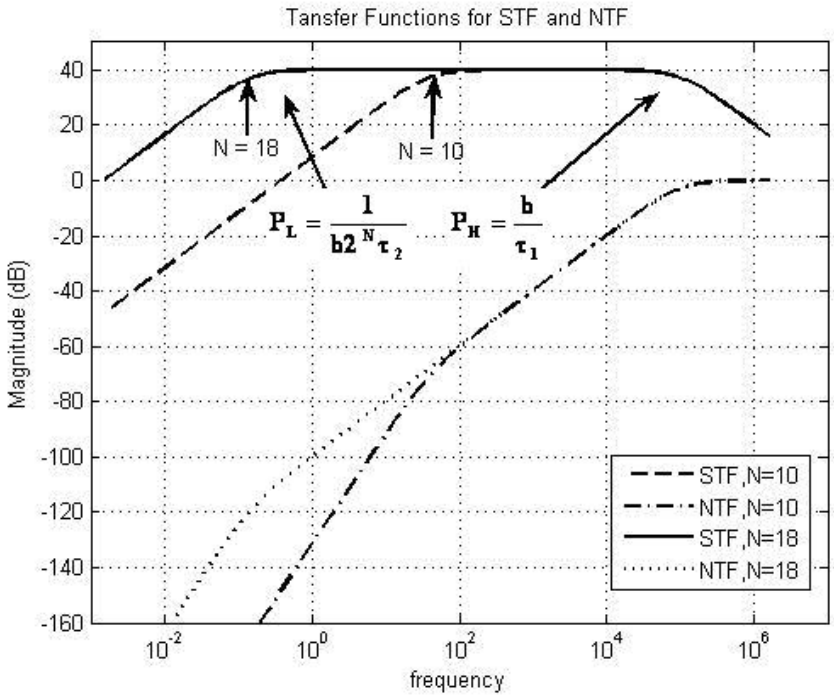

Figure 3.24: Comparison of N=10 and N=18 bits UP-DOWN digital counter.

signal and noise transfer functions are band-pass filter (BPF) and LPF respectively. The low-frequency cutoff for the signal transfer function is reduced to 0.02 Hz with $N = 18$ for the digital UP-DOWN counter.

Finally, a digital FIR LPF filter with cut-off frequency at 2 kHz is used in the digital domain to eliminate the high frequency quantization noise.

3.4.3 Noise Performance

This section analyzes contributions to the system SNR from device noise and the effect of the ΣΔ ADC. First, the total input referred noise in Figure 3.25 is given by

$$V^2_{thermal,n} = V^2_{in,n(Preamp)} + V^2_{out,n(Fbopamp)} \tag{3.54}$$

where $V^2_{in,n(Preamp)}$ is the input referred noise of pre-amplifier and $V^2_{out,n(Fbopamp)}$ is the output referred noise of the feedback op-amp. The input referred noise for each devices is introduced in next chapter.

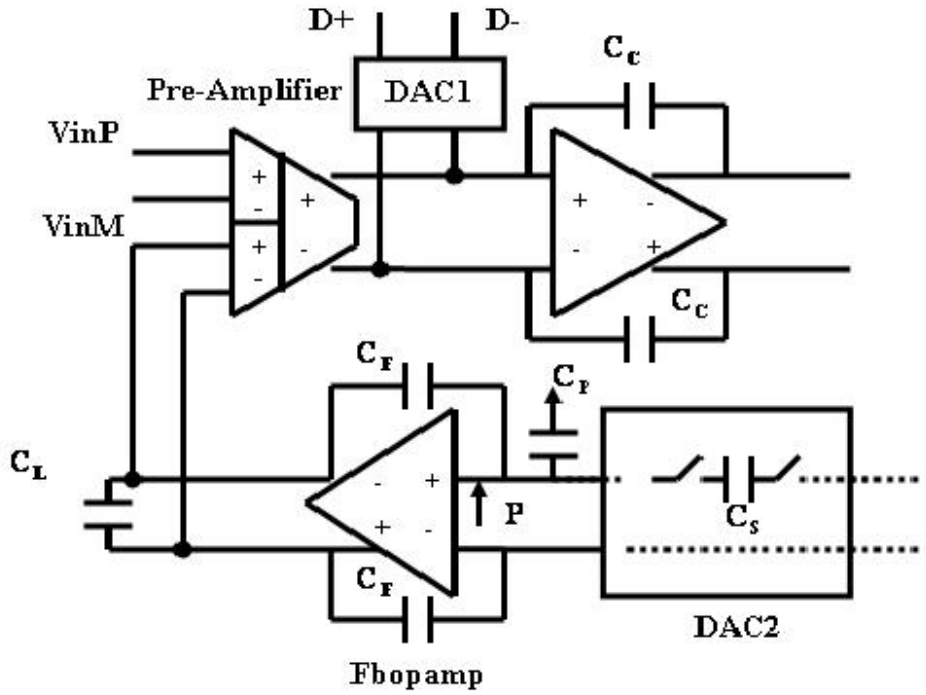

Figure 3.25: Schematic of pre-amplifier and feedback opamp.

Second, according to the (2.3), the quantization noise is

$$V_{q,n}^2 = \frac{\triangle^2}{12 f_S} \tag{3.55}$$

where $\triangle$ is the step size of the quantizer, and f_S is the sampling frequency for $\Sigma\Delta$ ADC.

The final noise source is 1/f noise and is expressed as follow:

$$V_{1/f,n}^2 = \frac{K}{f}\left(\frac{1}{C_{ox}WL_{Preamp}} + \frac{1}{CoxWL_{Fbopamp}}\right) \tag{3.56}$$

where K is process-dependent constant for the pre-amplifier and feedback op-amp devices, and C_{ox} is gate oxide capacitance per unit area. The inverse dependence of (3.56) on WL suggests that to decrease 1/f noise, the device area should be increased, which was done in the feedback op-amp. For the input stage, the chopping technique described earlier in section 3.2 has the additional benefit of reducing the 1/f noise and DC offsets of the pre-amplifier.

Since the quantization noise is pushed into high frequencies by NTF, the 1/f noise and

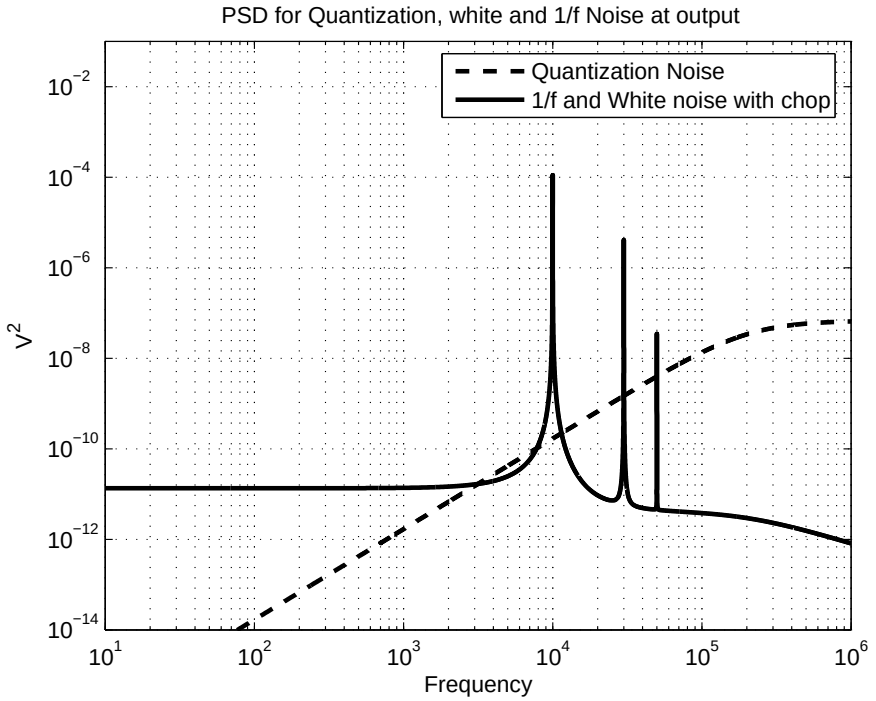

Figure 3.26: Power spectrum density for output noise.

thermal noise should also be determined in order to find the noise at the output. Assuming the Vin $= V_{1/f,n} = 0$, then the digital output D in Figure 3.23 is

$$\begin{aligned} D &= \frac{1}{s\tau_1}(V_{thermal,n} - D\frac{1}{s\tau_2 2^N} - bD) \\ \Rightarrow V_{thermal,n}\frac{1}{s\tau_1} &= D(1 + \frac{1}{s^2\tau_1\tau_2 2^N} + \frac{b}{s\tau_1}) \\ \Rightarrow D &= \frac{s\tau_2}{s^2\tau_1\tau_2 + bs\tau_2 + 2^{-N}}V_{thermal,n}. \end{aligned} \tag{3.57}$$

The same method can be applied in order to find the output noise for $V_{1/f,n}$ by assuming Vin $= V_{thermal,n} = 0$. The output D is then given

$$D = \frac{s\tau_2}{s^2\tau_1\tau_2 + bs\tau_2 + 2^{-N}}V_{1/f,n}. \tag{3.58}$$

Thus, the total thermal noise and 1/f noise see the STF from (3.57) and (3.58).

Based on the analysis of different noise sources at the output, the output noise power spectral density (PSD) of overall system can be determined [24]. Since the 1/f noise and

DC offsets at the input are only modulated by the output chopper, the output PSD in (3.5) can be expressed by

$$S_{out,thernal}(f) = (\frac{2}{\pi})^2 \sum_{n=-\infty}^{\infty} \frac{1}{n^2} S_{in,w}(f - nf_{chop})|STF(f)|^2 \tag{3.59}$$

where n is an odd number, f_{chop} is chopping frequency, and S_{in} is $V^2_{thermal,n}$ in (3.54). The output PSD for quantization noise is given by

$$S_{out,q} = V_{q,n}|NTF(f)|^2 \tag{3.60}$$

Figure 3.26 shows the total output PSD for each noise source with chopping frequency at 10 kHz with total thermal noise 1uVrms, and OSR = 250. Notice that the 1/f noise has been removed by chopping technique. The intersection between PSD for quantization noise and white noise is above 2 kHz. This implies that SNR is white noise limited, and the SNR will not improve with higher order $\Sigma\Delta$ ADC design. Achieving higher SNR would require lower white noise and an associated increase in power dissipation.

3.4.4 Common Mode Subtraction

With differential pairs in the front-end, the input common mode range to preserve adequate linearity is only a few millivolts. Several techniques are used in order to improve linearity [29,30,44,45]. However, the increased noise from adding extra devices in the front-end is an issue. In Figure 3.1, the complementary G_m stage provides a wide input common mode range such that the common mode DC offsets due to skin-electrode interface can be subtracted by the pre-amplifier. The circuit implementation of G_m is described in next chapter.

3.4.5 Frequency Control

A $\Sigma\Delta$ ADC is used to digitize the analog signal. Thus, it can be digitally networked with other ICs. According to (3.52), the $\Sigma\Delta$ ADC has not only LPF but also HPF characteristics for the signal transfer function. These characteristics are described as follow:

High Frequency Cutoff

Assuming the transconductance of pre-amplifier is $gm_{n,p}$, the time constant for τ_1 is defined by $C_C/gm_{n,p}$, the P_H then can be expressed from (3.52) as

$$P_H = \frac{bgm_{n,p}}{C_C} \tag{3.61}$$

where C_C is feedback capacitor for first integrator in Figure 3.25. Although the noise at high frequency is integrated by the integrator, these signals are then rejected by the FIR LPF.

Low Frequency Cutoff

The low-frequency pole P_L defines the low-frequency cutoff for the overall system based on (3.52). The time constant τ_2 is equal to C_F/gm_{eff}, where gm_{eff} is $f_S C_S$ shown in Figure 3.25. Therefore, by replacing gm_{eff} with $C_S f_S$ and τ_2 with C_F/gm_{eff}, P_L is given by

$$P_L = \frac{f_S}{b}\frac{C_S}{2^N C_F} \tag{3.62}$$

Without the N-bit UP-DOWN counter, achieving a low frequency cutoff $< 0.1Hz$ would require an unrealistically large ratio between C_S and C_F. With the counter, the effective ratio is between C_S and $2^N C_F$, which is not only physically realizable but also can be easily controlled by programming the N of the UP-DOWN counter. The output of UP-DOWN counter will go high or low depending on accumulated comparator states. A signal or noise at high frequency will present an approximately equal density of logic high or low values. Since the output of the UP-DOWN counter does not activate the feedback integrator until 2^N counts are accumulated, the behavior of the UP-DOWN counter is analogous to

a lowpass characteristic in the feedback path. The input subtracts the lowpass feedback, resulting in a highpass characteristic for the overall system transfer function.

3.5 Summary for Overall System

A novel second order ΣΔ ADC with feedback integrator from the ΣΔ output is presented. With feedback integrator and UP-DOWN counter, the low-frequency cutoff can be programmed. In addition, the Gm stage enables the wide input common mode while the common mode signal at the input is subtracted by the pre-amplifier. The SNR is dominated by the thermal noise as discussed in section 3.4.3. In next chapter, the circuit implementation for each block is described and discussed.

Chapter 4

Circuit Implementation of Sigma-Delta ADC

The second order ΣΔ ADC outlined in Chapter 3 is implemented in Jazz Semiconductor 0.18 um CMOS technology . In section 4.1, a detailed description of pre-amplifier, op-amp, DAC_1, and chopping block are discussed. In section 4.2, the implementation of op-amp for second integrator is presented. The design of UP-DOWN counter, DAC_2, and GM stage are also described. In section 4.3, the quantizer are presented, followed by a simulation results of the actual chip layout in section 4.4.

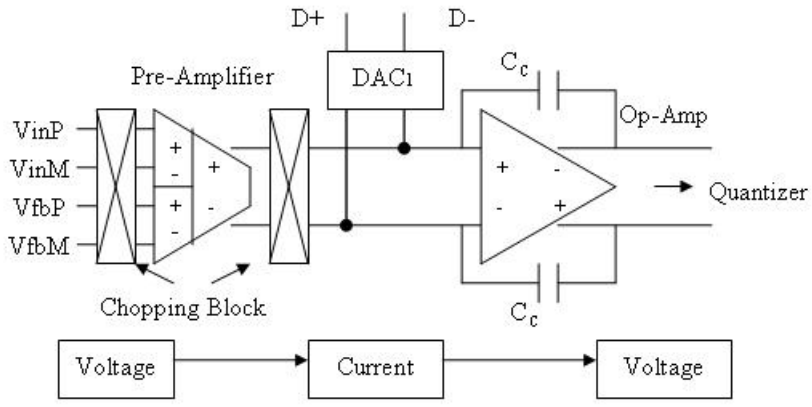

Figure 4.1: First integrator.

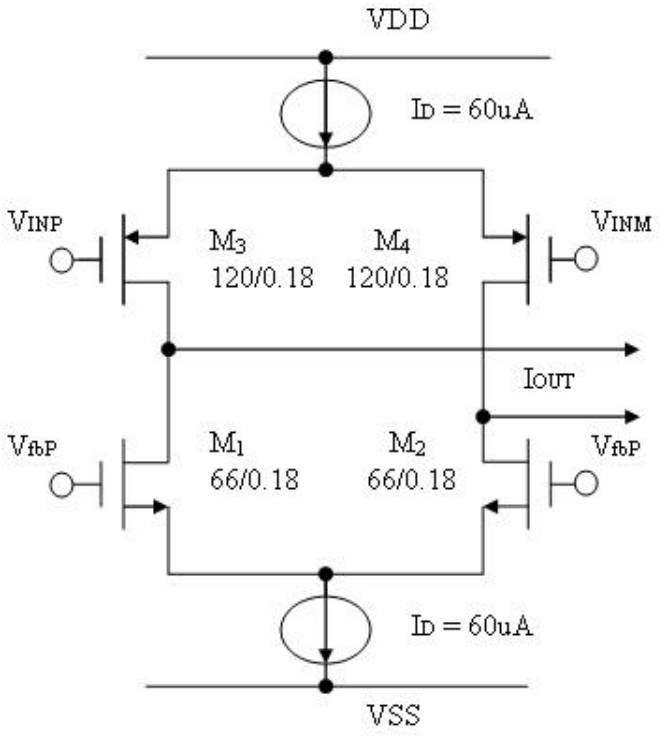

Figure 4.2: Circuit implementation of pre-amplifier.

4.1 First Integrator

The first order integrator of overall system is in Figure 4.1. The circuit implementation of pre-amplifier, chopping block, op-amp, and DAC_1 are discussed in this section.

4.1.1 Pre-Amplifier

Figure 4.2 shows the pre-amplifier, which is designed with complementary NMOS-PMOS differential pairs. The input differential voltages are converted to a current as

$$I_{out} = gm_p(V_{inP} - V_{inM}) - gm_n(V_{fbP} - V_{fbM}) \tag{4.1}$$

where V_{inP},V_{inM} and V_{fbP}, V_{fbM} are input signals from electrodes and signals from feedback integrator respectively, and gm_n and gm_p are transconductance of NMOS and PMOS

differential pairs. The current I_{out} is then integrated in continuous time by the first integrator.

Mismatch between NMOS and PMOS differential pairs would cause linearity errors for the differential signal. Also, the pre-amplifier must provide equal and opposite gains in each path to implement subtraction of the common interference (4.1). As shown in Figure 4.1, chopping technique is used to modulate the effects of these mismatch errors to high frequency where they can be removed by the FIR LPF. For low noise pre-amplifier design [4], the drain current and sizing of each transistor are implemented with transconductance $gm_{n,p}$ of $630\mu A/V$ as shown in Figure 4.2.

Although the circuit topology is a standard design suitable for driving capacitive loads, the sizing of transistors is critical for achieving low noise at low current levels. The bias current is set to 60 uA, giving devices M1 to M4 drain currents of 30 uA. At this current level, each transistor may operate in weak, moderate, or strong inversion depending on its W/L ratio. For low noise pre-amplifier design, each transistor is operated in moderate region and its moderate inversion characteristic current I_S [19] is given by

$$I_S = \frac{2uC_{ox}V_T^2}{\kappa}\frac{W}{L} \tag{4.2}$$

where V_T is the thermal voltage kT/q, and κ is the subthreshold gate coupling coefficient. Note that κ has typical value of 0.7.

The inversion coefficient (i) is

$$i = \frac{I_D}{I_S} \tag{4.3}$$

For large currents (i>10), the transistor operates in strong inversion. For very small currents (i<0.1), the transistor is in the weak inversion. The region between (0.1<i<10) is called the moderate inversion region as shown in Figure 4.3. It provides a smooth transition between two regions. Figure 4.3 also shows the relationship between the over drive voltage $V_{GS} - V_{th}$ of MOS transistor and its inversion coefficient i. The EKV model [19] is used in order to calculate transconductance gm, the gm is given by

$$gm_{1-4} = \frac{\kappa I_D}{V_T}\frac{2}{1+\sqrt{1+4i}} \tag{4.4}$$

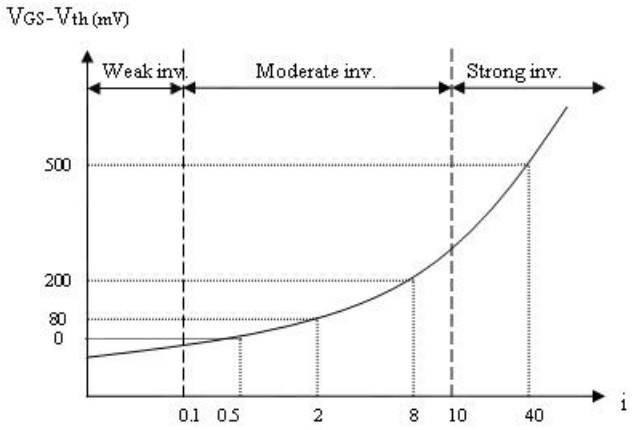

Figure 4.3: Relation between $V_{GS} - V_{th}$ and inversion coefficients i.

Table 4.1: Operating Point of Pre-Amplifier

Devices	$I_D(uA)$	gm/$I_D(V^{-1})$	$V_{gs} - V_{th}(mV)$
M_1,M_2	30	21	42
M_3,M_4	30	21	46

Table 4.1 summaries the operating conditions of each transistor. Based on Figure 4.3, the $V_{GS} - V_{th}$ for both NMOS and PMOS differential pairs are closed to 50 mV which are located inside the moderate region.

Input referred noise

According to Figure 4.2, the total input referred noise can be found by

$$V^2_{in,n(total)} = \frac{8}{3}\frac{kT}{gm_{1-4}} + \frac{K}{f}(\frac{1}{C_{ox}WL_{M_{1-4}}}) \tag{4.5}$$

where the first term is thermal noise, and last term is 1/f noise. Since the 1/f noise is modulated into high frequencies by the output modulator, the total input referred noise is then dominated by the thermal noise. The total thermal noise is $8.4nV/\sqrt{Hz}$ based on gm of $630uA/V$.

In order to compare the noise specification with other works, a noise efficiency factor is introduced by [46]

$$NEF = V_{in,rms}\sqrt{\frac{2I_{total}}{\pi V_T 4kTBW}}. \tag{4.6}$$

where the $V_{in,rms}$ is input referred noise rms noise voltage, I_{total} is the total current of pre-amplifier, and BW is bandwidth of pre-amplifier in hertz. An amplifier using a BJT transistor has

$$\begin{aligned} NEF &= \sqrt{\frac{2kT}{gm}\frac{\pi}{2}BW\frac{2I_{total}}{\pi V_T 4kTBW}} \\ &= \sqrt{\frac{1}{2}} \\ &= 0.707. \end{aligned} \tag{4.7}$$

Any practical circuits have higher value of NEF. Integrating the expression (4.5) over bandwidth BW and substituting into (4.6), the noise efficiency factor is

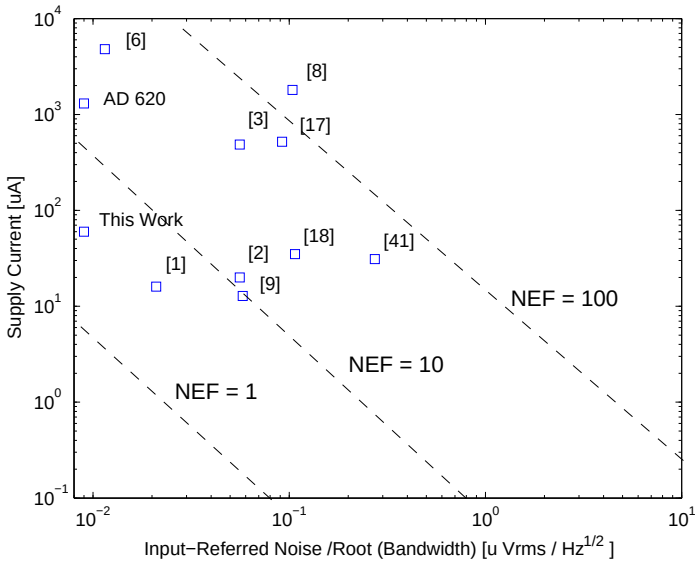

Figure 4.4: Supply Current versus normalized noise for amplifiers. Dash lines indicate constant NEF contours.

$$
\begin{aligned}
NEF &= \sqrt{\frac{8kT}{3gm_{1-4}} 4\frac{\pi}{2} BW \frac{2I_{total}}{\pi V_T 4kTBW}} \\
&= \sqrt{\frac{8I_{total}}{3V_T gm_{1-4}}} \\
&= \sqrt{\frac{16I_{D1}}{3V_T gm_{1-4}}}
\end{aligned}
\tag{4.8}
$$

Based on Table 4.1, the NEF is equal to 3.1.

Figure 4.4 shows the power-noise performance of pre-amplifier compared with estimated NEF values based on equation (4.6) from previous published bio-amplifiers. The pre-amplifier has better NEF than existing designs.

4.1.2 Chopping Block

The Chopping technique is used to modulated the dc offsets and 1/f noise of amplifier stage to the odd harmonic frequencies of the chopping square signal F_C. The implementation of chopping block is shown in Figure 3.7. However, the MOS switch nonidealities include a nonzero and nonlinear on-resistor as discussed in section 3.2.3. The factors affecting residual offset are as follow:

- clock feedthrough;
- charge injection;
- sampled noise;
- leakage current.

The nonlinear effects of MOS transistor can be reduced by circuit techniques. The techniques are

- complementary switches;
- dummy transistor;

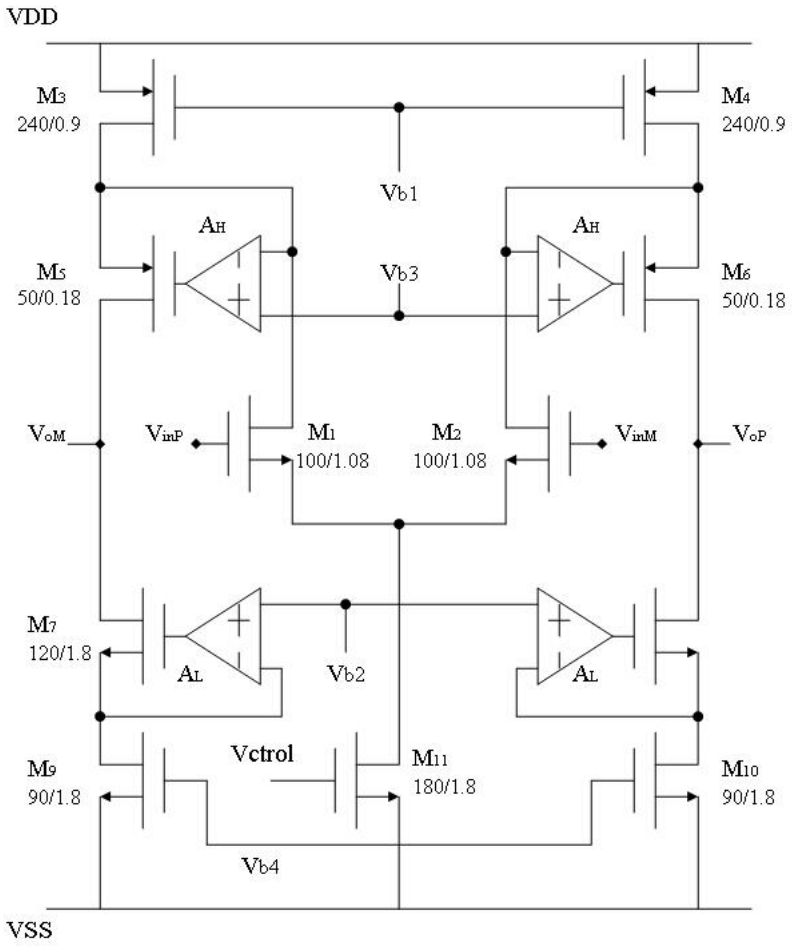

Figure 4.5: Folded cascode op amp with gain boosting.

- fully differential structure;
- bottom plate technique.

In this thesis, the dummy transistors are used for the chopping block while the fully differential structure and bottom plate technique are used for the first integrator.

4.1.3 Op-Amp for First Integrator

Figure 4.5 is a fully differential folded cascode with gain boosting amplifier for the first integrator [47–52]. The Figure shown is a differential input differential output design. All

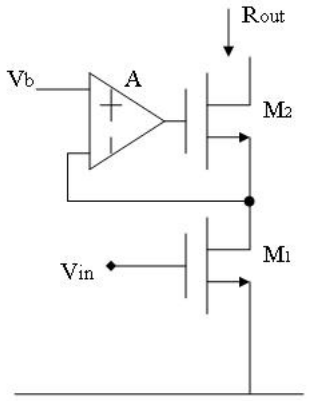

Figure 4.6: Gain boosting.

current mirrors in the circuit result in high input impedance. Thereby maximizing the dc gain of opamp. The gain boosting technique is introduced first for high impedance design. As shown in Figure 4.6, the idea is to drive the gate of transistor M_2 by an amplifier A that forces the voltage V_b to be equal to the source voltage of transistor M_2 with negative feedback loop. Therefore, the variation at the drain of transistor M_2 has much less effect on the source of transistor of M_2, because amplifier A regulates this voltage. This topology is usually called regulated cascode or active cascode. With the smaller variation of the source of M_2 due to the change of output voltage, the output current becomes less sensitive to the voltage variation at output compared with conventional cascode structure. Thus, the output impedance can be found by

$$\begin{aligned} R_{out} &= r_{o1} + r_{o2} + [gm_2(A+1) + g_{mb2}]r_{o1}r_{o2} \\ &\cong Agm_2r_{o1}r_{o2}. \end{aligned} \tag{4.9}$$

The increasing output impedance R_{out} is several order of improvement without the boosting technique. Another advantage of gain boosting is no cascode devices needed on top of transistor M_2.

Using half circuit of folded cascode op amp model of Figure 4.7, the total gain of folded cascode with gain boosting amplifier $|A_V|$ is equal to $G_M R_{out}$. By shorting the output to ground, the G_M is approximately to gm_1. According to (4.9), the output impedance R_{out}

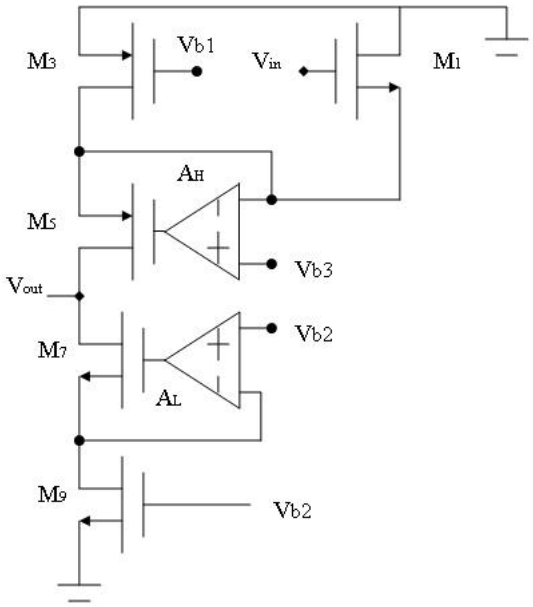

Figure 4.7: Half Circuit of folded cascode op amp.

is $[A_H gm_5(r_{o1}||r_{o3})r_{05}]|||[A_L gm_7 r_{o7} r_{o9}]$. Thus, the gain is

$$|A_V| = gm_1[A_H gm_5(r_{o1}||r_{o3})r_{05}]|||[A_L gm_7 r_{o7} r_{o9}]. \tag{4.10}$$

Since the amplifier is symmetrical design for low dc offsets due to mismatching and high CMRR, transistor sizing is done by equalizing the currents for each branch of the amplifier. The drain current I_{D5} is equal to the drain current I_{D1}, the summation of I_{D1} and I_{D5} is equal to the drain current I_{D3}. Thus, the current I_{D3} is equal to the tail current I_{D11} of input differential pair M_1 and M_2. Since the current I_{D3} is twice as large as the current I_{D1}, the transistor M_3 must be wide enough to carry the large current. However, the large area of transistor results in substantial capacitor at drain of transistor M_3. Therefore, the large overdrive voltage can be made to minimize effect of frequency response due to the large value of parasitic capacitor.

In order to increase the gain of amplifier, additional gain stages A_H and A_L are used. Assuming $A_H = A_L = A$, $gm_5(r_{o1}||r_{o3})r_{05} = gm_7 r_{o7} r_{o9} = R_T$, then the total gain is $Agm_1 R_T$ based on (4.10). The total gain is increased by a factor of gain A. Since the output impedance R_T is quit high, the additional gain A is designed with relative low gain in order

to save the power and die area. Figures 4.8 and 4.9 are additional gain stages A_H and A_L to boost the output impedance of PMOS and NMOS current sources respectively. The A_H and A_L consist of one differential pair and three current mirrors. The input differential pairs M_{1-2} are loaded with two equal current mirrors M_{3-4}, which provide a current gain B to the output. The current gain B can be found by the ratio between W_5/W_3. The total

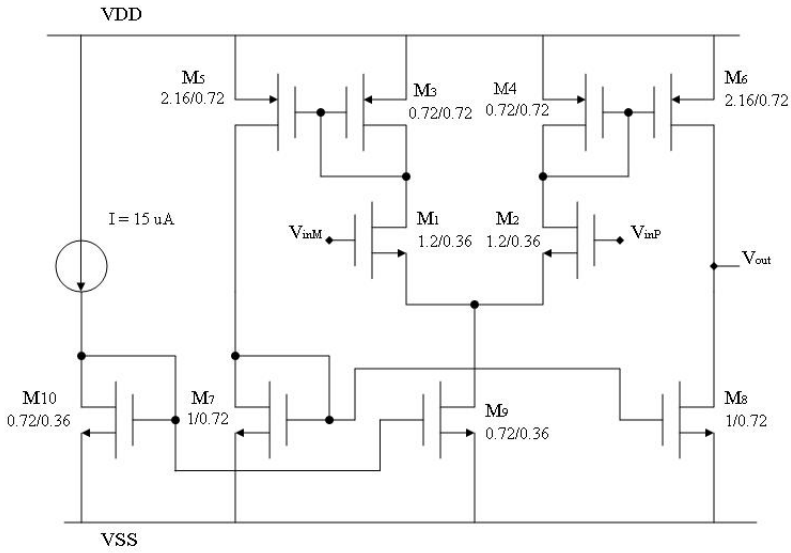

Figure 4.8: Additional Gian stage for boosting output impedance of PMOS current sources.

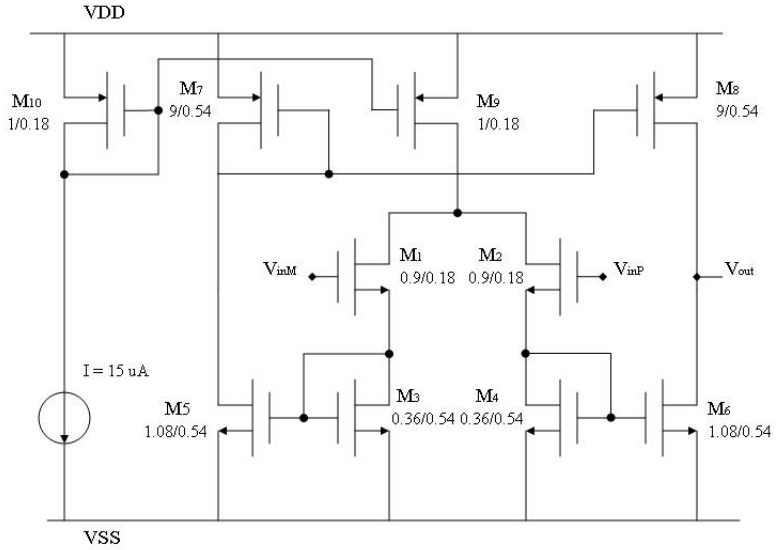

Figure 4.9: Additional Gian stage for boosting output impedance of NMOS current sources.

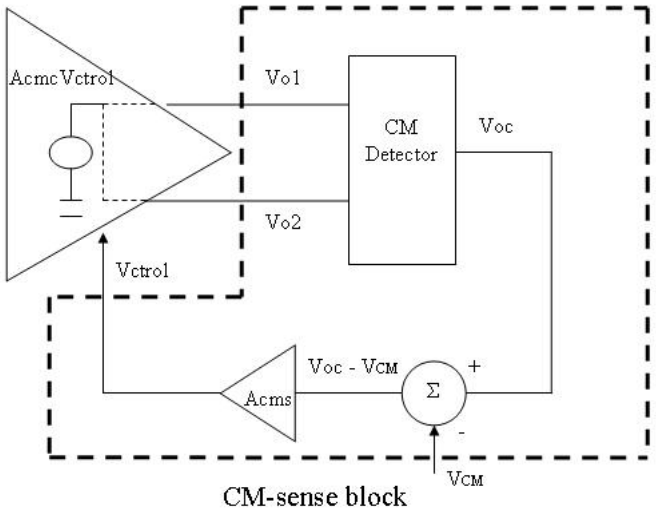

Figure 4.10: A conceptual block diagram of the CMFB loop.

gain of A_H and A_L are then determined by the ratio $Bg_{m1,2}/g_{m3,4}$.

Common Mode Feed Back (CMFB) circuit for OP-Amp

Since the amplifier is designed with fully differential topology, the output voltages are not well defined compare to the single-end amplifier. Therefore, the common mode feedback (CMFB) circuitry is needed in order to set the common mode output voltage correctly as shown in Figure 4.10 [53]. The purpose of CMFB is to sense the common mode voltage, V_{oc}, by the CM detector then to compare with a reference voltage, V_{CM}. If the V_{oc} is higher than the V_{CM}, the bias current I_{D11} is increased in order to bring the V_{oc} down until both of V_{CM} and V_{oc} agree. A similar statement holds for the case when the V_{oc} is lower than the V_{CM}.

The small-signal model can be also analyzed based on Figure 4.10. The CMFB loop uses negative feedback to make $V_{oc} \cong V_{CM}$, the V_{oc} can be expressed as

$$V_{oc} = A_{cms}A_{cmc}(V_{oc} - V_{CM}). \tag{4.11}$$

Thus, the ratio V_{oc}/V_{CM} is the closed-loop small-signal gain of the CMFB, which is

$$\begin{aligned} A_{CMFB} &= \frac{\Delta V_{oc}}{\Delta V_{CM}} \\ &= \frac{V_{oc}}{V_{CM}} \\ &= \frac{A_{cms}(-A_{cmc})}{1 + A_{cms}(-A_{cmc})}. \end{aligned} \tag{4.12}$$

where the A_{cms} the gain of CMFB, and the A_{cmc} is the gain from V_{ctrol} to V_{oc}. The gain of A_{cmc} can be obtained by applying the input to the gate of transistor M_{11}, and is given by

$$|A_{cmc}| = gm_{11H}[A_H gm_5(gm_1 r_{o1} r_{o11} || r_{o3}) r_{05}] || [A_L gm_7 r_{o7} r_{o9}]. \tag{4.13}$$

where gm_{11H} is equal to $gm_{11}/2$ in CM half-circuit. Since $A_{cms}(-A_{cmc})$ is much greater than one, $A_{CMFB} \approx 1$ and $\Delta V_{oc} \simeq \Delta V_{CM}$. If the V_{CM} changes by a small amount, V_{oc} should change by an equal amount so that V_{oc} tracks V_{CM}.

Since the CMFB loop is a negative feedback loop, it is important to check the loop is stable or not. The dominant pole P_{cp} in the CMFB is set by the load capacitance C_L and the output impedance in the CM half-circuit. The $A_{cmc}(s)$ is

$$A_{cmc}(s) = -\frac{gm_{11H}[A_H gm_5(gm_1 r_{o1} r_{o11} || r_{o3}) r_{05}] || [A_L gm_7 r_{o7} r_{o9}]}{1 + s(A_H gm_5(gm_1 r_{o1} r_{o11} || r_{o3}) r_{05}) C_L}. \tag{4.14}$$

At high frequency $w \gg P_{cp}$, (4.14) reduces to

$$A_{cmc}(s) = -\frac{gm_{11H}}{sC_L}. \tag{4.15}$$

The unity frequency of CMFB is gm_{11H}/C_L. For stability issue, the adequate phase margin for CMFB can be designed by splitting the transistor M_{11} into two identical devices. Thus, $gm_{11H} = gm_{11}/2$ decreases gain of A_{cmc} and therefore increases the phase margin of CMFB loop. For high speed application, the gain-bandwidth-product (GBW) of common mode is designed to be higher than the differential GBW gm_1/C_L. Therefore, the fast common-mode feedback would not take much time to restore the biasing in the input stage. In this case, the tradeoffs between power and speed are challenges for circuit design.

Figure 4.11 is a CMFB circuitry in continuous time domain. The source-coupled pairs M_{1-2} and M_{3-4} together sense the common mode output voltages and generate an output

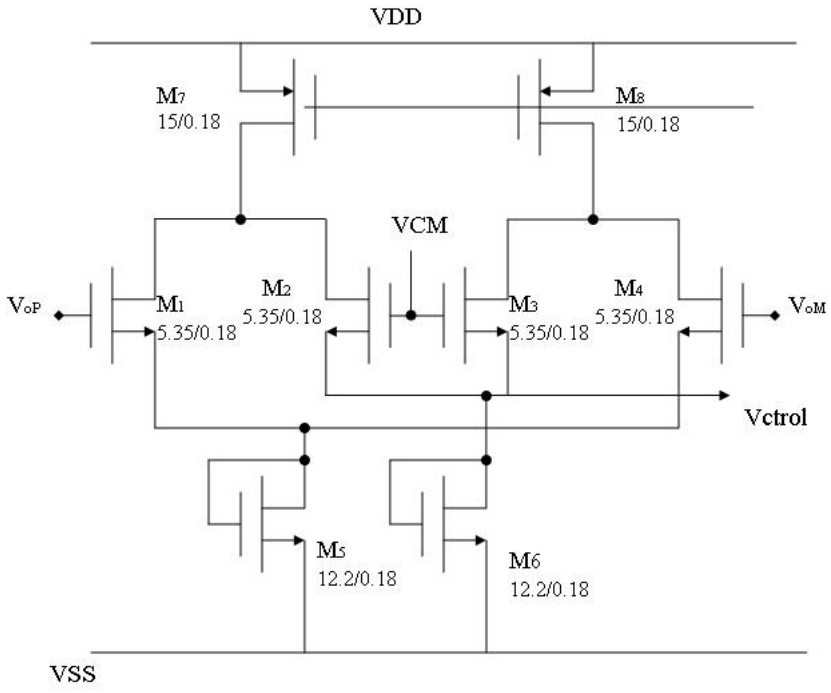

Figure 4.11: A continuous-time CMFB circuit.

that is proportional to the difference between V_{oc} and V_{CM}. Assume $V_{OP} - V_{CM}$ and $V_{OM} - V_{CM}$ are small, drain currents of transistor M_7 and M_8 are equal to I, and the common mode gain of CMFB is zero. Under these assumptions, the drain currents in M_2 and M_3 are

$$I_{d2} = -\frac{I}{2} - gm_2\frac{V_{OP} - V_{CM}}{2}. \tag{4.16}$$

$$I_{d3} = -\frac{I}{2} - gm_3\frac{V_{OM} - V_{CM}}{2}. \tag{4.17}$$

The two currents are summed in diode-connected transistor M_6 to give the common mode output current

$$\begin{aligned} I_{d6} &= -I_{d2} - I_{d3} \\ &= I + gm_2(\frac{V_{OP} + V_{OM}}{2} - V_{CM}) \\ &= I + gm_2(V_{oc} - V_{CM}). \end{aligned} \tag{4.18}$$

where $gm_2 = gm_3$ is assumed. This shows that the current includes a dc term I and a term

that is proportional to $V_{oc} - V_{CM}$. The current I_{d6} is mirrored by M_{11} in Figure 4.5 to produce the tail current in the amplifier, which controls the common mode output voltage.

A modified version of the CMFB can be made by splitting the transistor M_6 into two equal size transistors. One of these transistors is diode-connected and tie the gate to V_{ctrol}, and the other one is biased at a constant current which is equal to I. This changes effectively doubles the common mode gain of the circuit with very good linearity [54].

Noise Analysis

The noise performance of op amp is analyzed in this section. Since the noise of active cascode devices is negligible at low frequency, the total output noise is contributed by transistors M_{1-2}, M_{3-4}, and M_{9-10}. To determine the input-referred thermal noise, the noise sources of M_{3-4} are referred to the output:

$$V_{n,out} = 2(4kT\frac{2}{3gm_{3,4}}gm_{3,4}^2R_{out}^2). \tag{4.19}$$

where the factor 2 accounts for noise of M_3 and M_4, and R_{out} is the open-loop output impedance of the op amp. Similarly, for transistors M_9 and M_{10}

$$V_{n,out} = 2(4kT\frac{2}{3gm_{9,10}}gm_{9,10}^2R_{out}^2). \tag{4.20}$$

Dividing (4.19) and (4.20) by $gm_{1,2}^2R_{out}^2$ and adding the contribution of M_{1-2}, the total input referred noise is

$$V_{n,in} = 8kT(\frac{2}{3gm_{1,2}} + \frac{2}{3}\frac{gm_{3,4}}{gm_{1,2}^2} + \frac{2}{3}\frac{gm_{9,10}}{gm_{1,2}^2}). \tag{4.21}$$

According the equation above, the $gm_{1,2}$ can be made larger in order to reduce the noise at the input. However, the noise contribution from transistors $M_{3,4}$ have effect on the noise performance because the currents $I_{d3,d4}$ are twice as large as current I_{d1}. The simulation result of total input referred noise is shown in the end of this chapter.

Frequency and Transient Response

The settling time is an important parameter of amplifier for use in applications such as A/D and D/A. The settling time consists of two distinct periods. The first portion is

slew-rate (SR) limit, and it acts nonlinear fashion. The time of slew-rate is determined by the current to charge the amplifier compensation capacitor. With a load or compensation capacitor C_L, the slew-rate may limit by a fixed biasing current. Thus, the linear settling time will be affected by the slew-rate in this case. Increasing biasing current is one way to avoid the slew-rate limiting. However, the power consumption is increased with fast settling time. Another way to improve the SR is to reduce the transconductance of $gm_{1,2}$ while keeping the bias current constant. It will lower the dc gain and increase the noise [53].

The second portion of settling time is due to the finite unity-gain frequency (w_t) of the amplifier and it acts in a linear fashion. Several work have been shown that this period is significantly affected by the presence of pole-zero pairs in the amplifier with gain boosting design [48, 55, 56]. A solution is provided to avoid the effect of pole-zero doublet by the additional gain stage in this section.

A model which represents the behavior for slewing of input differential pair of amplifier and transient response is shown in Figure 4.12. The differential input stage is modeled as shown with maximum current I_O and voltage V_x is limited by I_o/gm. For the voltage $|V_x| > I_o/gm$, the input stage is limited by a current I_o. This is nonlinearity behavior in the transient response. A pole-zero doublet is also modeled between the input stage and single-pole stage. The settling time behavior between slewing and pole-zero effects are discussed next.

Settling Time and Slew Rate (SR) Limit

For settling time requirement, If the amplifier needs to settle within 1/2 LSB at the 16 bit level in 24 nsec. With feedback $\beta \cong 1$, we can obtain,

$$\begin{aligned} \frac{1}{2^{17}} &= e^{\frac{-24ns}{\tau}} \\ \Rightarrow \tau &\cong 2ns. \end{aligned} \tag{4.22}$$

Since $\tau = 1/\beta w_t$, w_t is equal to 87.5 MHz. From $w_t = g_m/C_L$, the g_m is $1.6mA/V$. The bias current I_{D11} is 164 uA by using the square-law relationship $g_m = 2I_D/V_{eff}$. Where the effective over dirve voltage is assumed to be $0.2V$. Based on the bias current I_{D11}, the

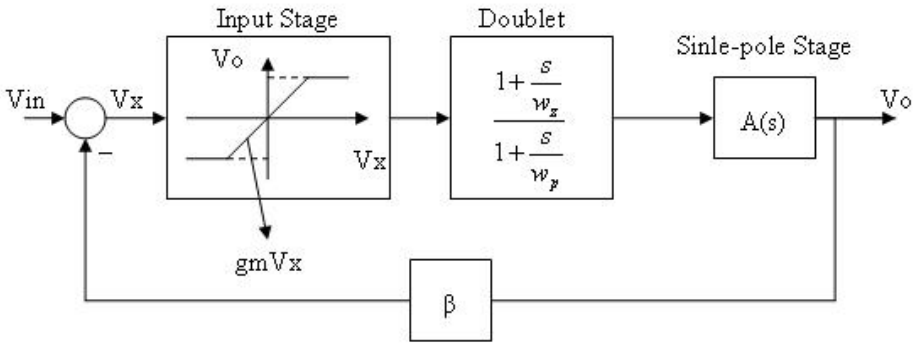

Figure 4.12: A model for slewing behavior and transient response.

SR is $54.7V/uS$ by I_D/C_L.(Assuming the load capacitor C_L is 3 pf in order to achieve dynamic range 80 dB)

The SR can be also defined as $SR = V_o/\tau$ by assuming a single-pole system with output voltage $V_o = V_o(1 - e^{-t/\tau})$. If the maximum output swing is 1V, the SR is equal to $200V/uS$. Thus, to settle within 1/2 LSB in 16-bit levels accuracy, the bias currents $I = 2 \times 200V/us \times C_L = 1.2mA$ for the input differential pair which is larger than the one we calculated above.

According to [55], the optimized bias current can be found with a given settling time. Assuming to settle within accuracy of 1/A, the settling time with slewing is

$$t_{settle} = (\frac{V_o C_L}{I} - \tau) - \tau \cdot ln\frac{V_o}{I}\frac{C_L}{\tau} + \tau \cdot lnA. \tag{4.23}$$

By using the square-law model, the time constant is

$$\begin{aligned} \tau &= \frac{V_{eff}}{2\beta V_o}\frac{V_o C_L}{I} \\ &= \frac{V_{eff} C_L}{2\beta I}. \end{aligned} \tag{4.24}$$

Based on (4.23), the minimum biasing current is

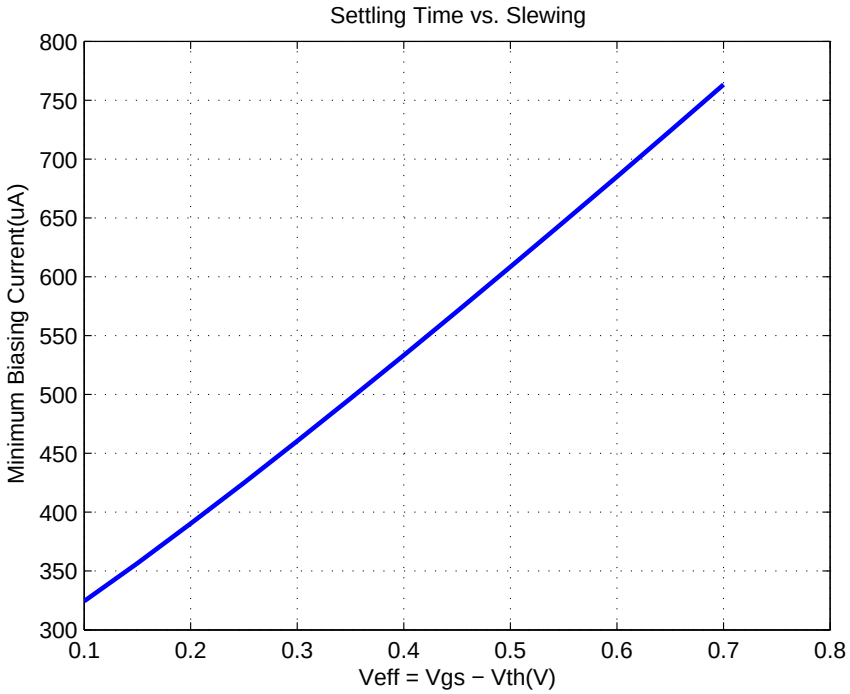

Figure 4.13: Settling Time vs. Slewing.

$$\begin{aligned} t_{settle} &= \frac{V_o C_L}{I_{min}} - \frac{C_L V_{eff}}{2I\beta} - \frac{C_L V_{eff}}{2I\beta} \cdot ln\frac{V_o}{I}\frac{C_L 2I\beta}{C_L V_{eff}} + \frac{C_L V_{eff}}{2I\beta} \cdot lnA. \\ &= \frac{V_o C_L}{I_{min}}(1 - \frac{V_{eff}}{2I\beta} - \frac{V_{eff}}{2V_o\beta} \cdot ln\frac{2\beta V_o}{V_{eff}} + \frac{V_{eff}}{2V_o\beta} \cdot lnA) \\ \Rightarrow I_{min} &= \frac{V_o C_L}{t_{settle}}(1 - \frac{V_{eff}}{2I\beta} - \frac{V_{eff}}{2V_o\beta} \cdot ln\frac{2\beta V_o}{V_{eff}} + \frac{V_{eff}}{2V_o\beta} \cdot lnA). \end{aligned} \quad (4.25)$$

Figure 4.13 is the simulation result for minimum biasing current corresponding with over drive voltage V_{eff} with settling time $t_{settle} = 24ns$. Notice that, the transistors of input differential pair will operate in weak inversion if V_{eff} is too low.

Settling Time and Pole-Zero Doublet

The transient response of a single pole amplifier shows a single time constant exponential settling behavior without overshoot or ringing. Settling accuracy within a specified time is therefore easily determined. The gain-boosting technique can achieve extremely large DC

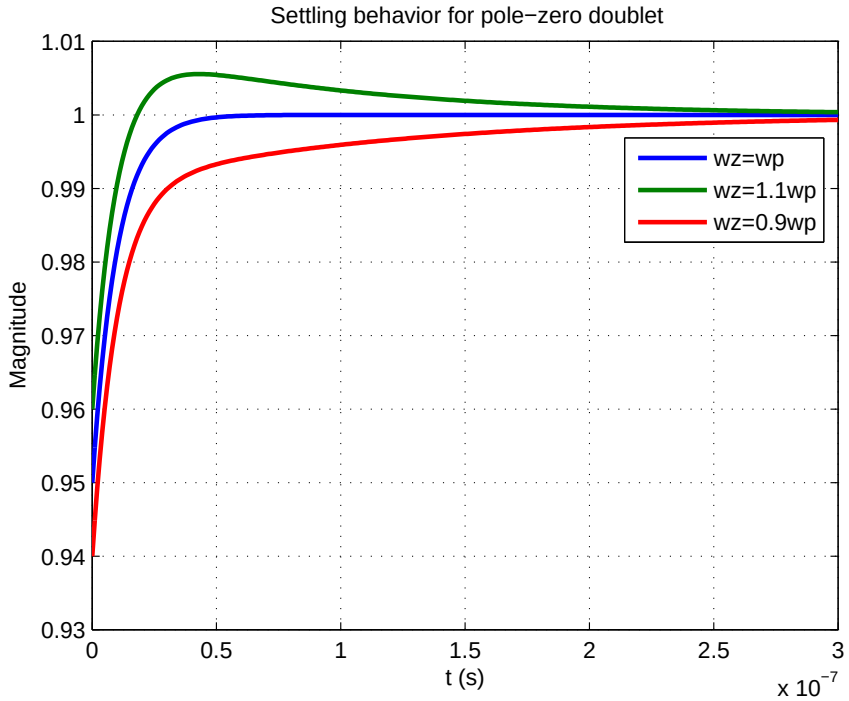

Figure 4.14: Settling Behavior vs. pole-zero doublet.

gain, however it comes with slow settling behavior due to pole-zero doublet [48, 56].

According to Figure 4.12, the step response of output $V_{out}(t)$ can be expressed as [56],

$$V_{out}(t) = V(1 - k_1 exp[-w_t t] + k_2 exp[-(\frac{t}{\tau_2})]). \tag{4.26}$$

for $t > T_s$, where $k_2 \cong (w_z - w_p)/w_t$, V is input amplitude, $\tau_2 \cong 1/w_z$, T_s is slewing period, w_z is doublet zero frequency, w_p is doublet pole frequency, and w_t is unity-gain frequency of amplifier. The last term of equation (4.26) represents the slow settling component and is the term of interest. Three examples for $w_z = w_p = 10^6(rad/s)$, $w_z = 1.1 \times w_p = 1.1 \times 10^6(rad/s)$, and $w_z = 0.9 \times w_p = 9 \times 10^6(rad/s)$ are compared with input amplitude 1V and $w_t = 10^8(rad/s)$ as shown in Figure 4.14 . When the ratio between w_z and w_p are relative large, output voltage has fast transient response with overshoot. Conversely, the output has slow time response with no overshoot. According to [48], the settling behavior can be optimized by

$$\beta w_t < w_{add} < w_{p2}. \tag{4.27}$$

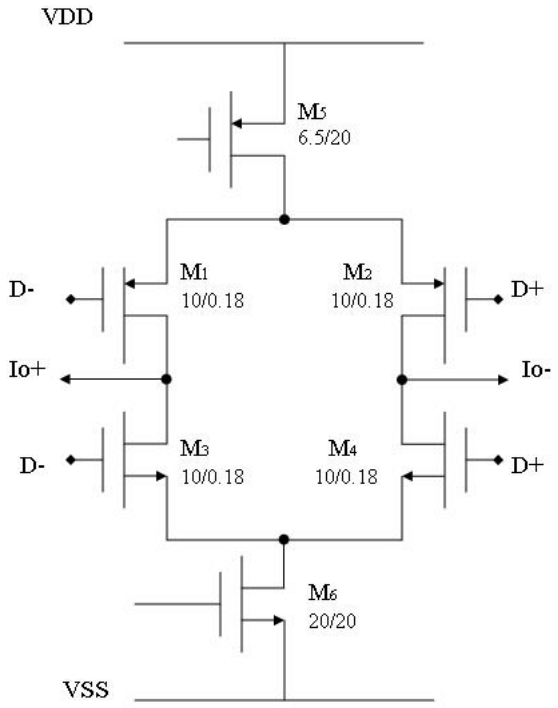

Figure 4.15: Implementation of DAC_1.

where βw_t is the closed-loop dominant pole frequency, w_t is the open-loop unity-gain frequency, w_{add} is the unity-gain frequency of the boosting amplifier and w_{p2} is the 2nd pole frequency of the main amplifier. A small capacitor C_C can be placed at the output of the gain booster to tune the frequency w_{add} between βw_t and w_{p2}. The second pole is higher than w_t and can be expressed as $w_{p2} = gm_{5,6}/C_P$, where C_P is parasitic capacitor at the source of transistor $M_{5,6}$ in Figure 4.5.

4.1.4 DAC_1 for First Integrator

The DAC_1 is designed with complementary NMOS-PMOS current sources as shown in Figure 4.15. The transistors M_5 and M_6 are designed large in order to minimize the 1/f noise. With DAC current 1uA, the current density at the output of DAC_1 is $0.56pA/\sqrt{Hz}$, which translates to input referred noise of $0.8nV\sqrt{Hz}$. The noise at the input is therefor negligible.

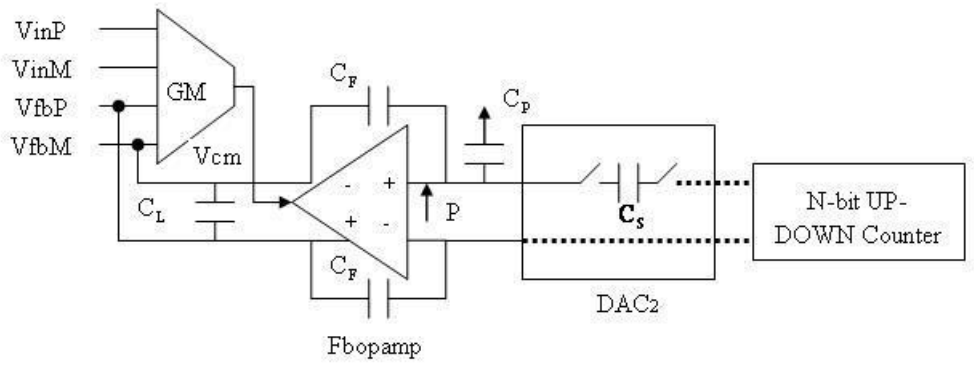

Figure 4.16: Feedback integrator.

4.2 Feedback Integrator

The feedback integrator of overall system is in Figure 4.16. The circuit implementation of op-amp, GM stage, and DAC_2 are discussed in this section.

4.2.1 Op-Amp for Second Integrator

In order to enable wide ICMR for pre-amplifier, a two-stage amplifier is used based on its wide output swings property as shown in Figure 4.17 . Since the speed of feedback path is relative low, the low power design can be achieved by using small current.

The gain of first and second stages are $gm_{1,2}/gm_{3,4}$ and $B \times gm_{3,4} \times r_{O5,O6}||r_{O7,O8}$ respectively. Thus, the total gain of amplifier is

$$\begin{aligned} A_V &= \frac{gm_{1,2}}{gm_{3,4}} \times B \times gm_{3,4} \times r_{O5,O6}||r_{O7,O8} \\ &= B \times gm_{1,2} \times r_{O5,O6}||r_{O7,O8}. \end{aligned} \tag{4.28}$$

where B is the factor of drain current $I_{d1,d2}$. The gain of the amplifier can be made large by increasing the factor B. The operating points for each device are summarized in Table 4.2

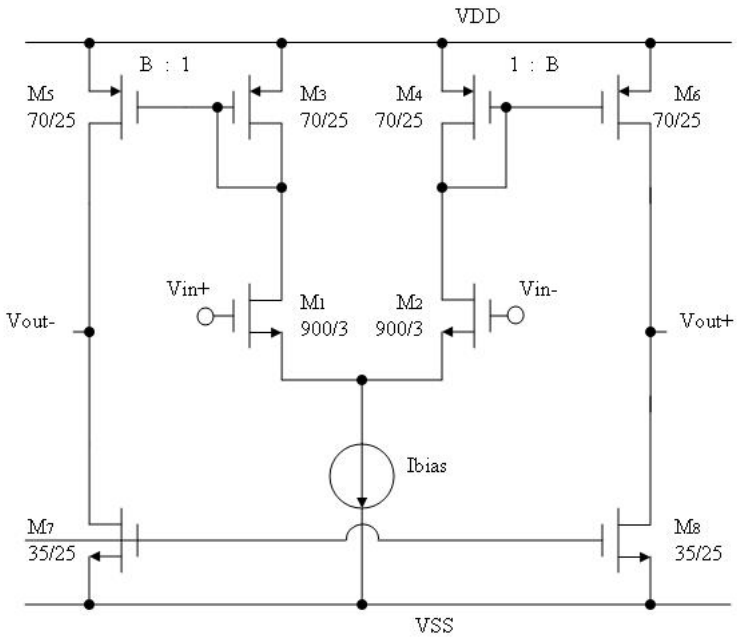

Figure 4.17: Op-amp for feedback integrator.

Table 4.2: Operating point for each transistor of op-amp.

Devices	$I_D(uA)$	V_{GS}-V_{th} (mV)	gm (uA/V)
M_1,M_2	6.5	4	171
M_3, M_4	6.5	282	41
M_5, M_6	6.5	282	41
M_7, M_8	6.5	190	61

Noise Analysis

In section 3.4.3, the total input referred noise is shown in equation (3.54). The input referred noise is analyzed first in order to find the noise at output. The noise of M_5 and M_7 referred to the gate of M_5 is equal to $4kT(2/3)(B \times gm_3 + gm_7)/(B \times gm_3)^2$, which is divided by ${gm_1/gm_3}^2$ when referred to the main input. Transistors M_1 and M_3 produce an input-referred noise of $(8kT/3)(gm_3 + gm_1)/gm_1^2$. Thus, the total input-referred noise equals

$$\begin{aligned} V_{in,n}^2 &= \frac{8}{3}kT(\frac{B \times gm_3 + {gm_7}^2}{B \times gm_3}) + \frac{8}{3}kT\frac{1}{gm_1^2}(gm_1 + gm_3) \\ &= \frac{8}{3}kT\frac{1}{gm_1^2}[\frac{gm_3}{B} + \frac{gm_7}{B^2} + gm_1 + gm_3]. \end{aligned} \tag{4.29}$$

If gm_1 is larger than gm_3 and B is greater than one, the input referred noise is determined by the first stage and can be approximated by

$$V_{in,n}^2 \cong \frac{8}{3}kT\frac{1}{gm_1}. \tag{4.30}$$

Based on Figure 4.16, the noise at the output is limited by the off-chip capacitor C_L and is expressed as

$$\begin{aligned} V_{out,n}^2 &= \frac{8}{3}kT\frac{1}{gm_1}\frac{1}{\beta^2}\frac{gm_1}{C_L 2\pi}\frac{\pi}{2} \\ &= \frac{1}{\beta^2}\frac{2kT}{3C_L}. \end{aligned} \tag{4.31}$$

where $\beta = (C_F + C_P)/C_F$. Thus, the noise at the output is limited by the capacitor C_L and has no effect on gm_1. Since the capacitor C_L is off-chip and can be made very large, the total input referred noise is then dominated by the input noise of pre-amplifier according to equation (3.54). Also, the devices of op-amp are made large, 1/f noise is negligible based on (2.10).

4.2.2 GM stage circuit for feedback integrator

The CMFB of feedback op-amp is the GM stage to enable wide ICMR for the pre-amplifier as shown in Figure 3.1. The GM stage has not only no noise effect at the input but also no extra power consumption for the overall system. The GM stage is designed based on the concept of CMFB in section 4.1.3. The source degeneration is applied in order to improve linearity for wide ICMR. The implementation of GM stage is shown in Figure 4.18.

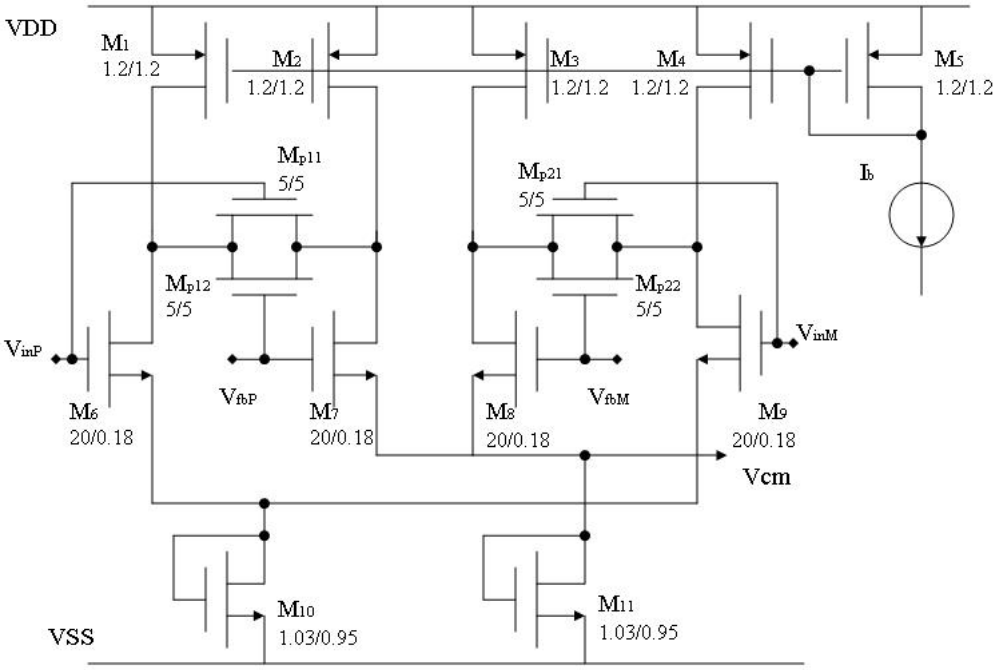

Figure 4.18: CMFB as GM stage for Overall System.

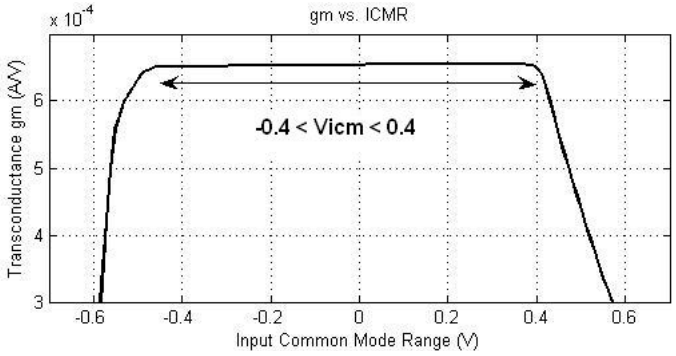

Figure 4.19: Transconductance vs. ICMR.

The simulation result for GM stage is shown in Figure 4.19. The transconductance of pre-amplifier is linear between $\pm 0.3V$ ICMR. The common mode signal or noise will be subtracted by the pre-amplifier at the input.

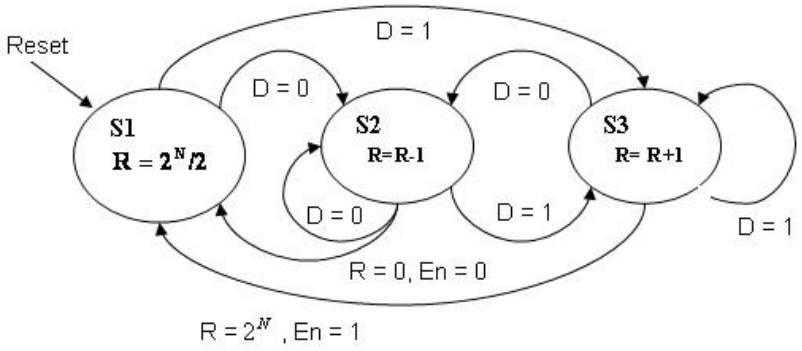

Figure 4.20: State Machine for UP-DOWN Counter.

4.2.3 UP-DOWN Counter

Figure 4.20 shows the state machine for the behavior of UP-DOWN digital counter. The description of behavior is as follow: When the reset is high, R is equal to $2^N/2$. During state S_1, a digital output of quantizer D is detected, if the D is logic low, state S_1 goes to state S_2, and R is subtracted by one, and vice versa. In state S_2 or S_3, if R is equal to 0 or 2^N, its value is reset and goes back to state S_1 while producing an output signal En logic high or low depending on the R is equal to 2^N or 0. With digital feedback from $\Sigma\Delta$ output, quantization noise in high frequency domain also goes through the UP-DOWN counter. Therefore, the UP-DOWN counter must be designed with low-pass filter characteristic in order to reject quantization noise in high frequency domain. With ideal $\Sigma\Delta$ ADC operation, if the input is higher than the reference voltage, more high logics will present at the output. In the other hand, more low logics will present at the output when the input is lower than the reference voltage. A signal or noise at high frequency will present logic high or logic low in a short period of time at the digital output. Therefore, increasing the number of bit of UP-DOWN counter will make the output of the counter never go high or low according to the operation of $\Sigma\Delta$ ADC in time domain. Thus, the feedback integrator is not activated by the UP-DOWN counter, the behavior of UP-DOWN counter is analogous to LPF.

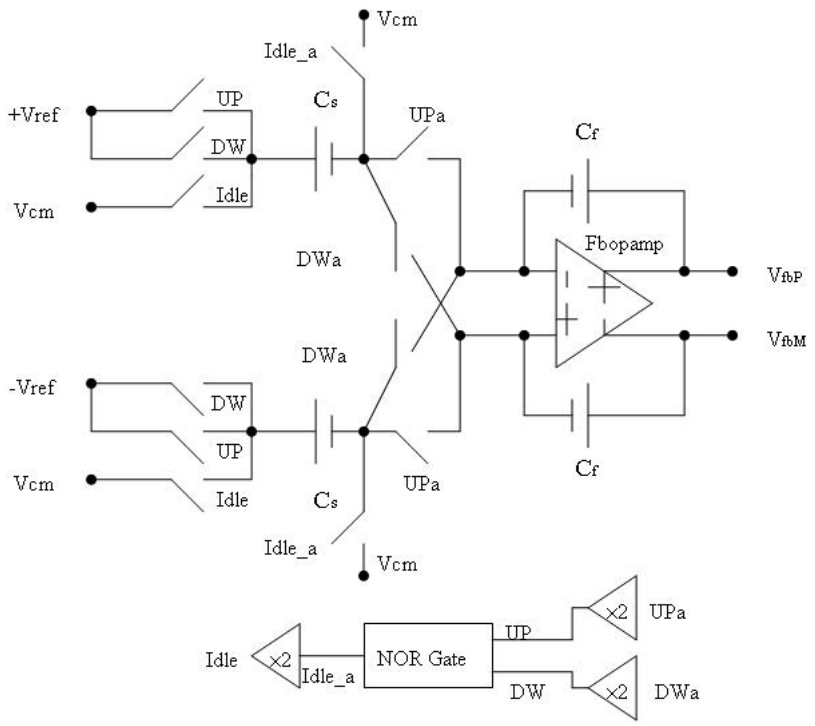

Figure 4.21: Implementation of Feedback DAC_2.

4.2.4 DAC_2 for Feedback Integrator

The circuit implementation of feedback DAC_2 is shown in Figure 4.21. The UPa and DWa signals are the outputs of UP-DOWN digital counter, and the UP and DW signals are delay signals of UPa and DWa in order to make charge-injection signal independent. The step size is the ratio between C_F and C_S, and low-frequency cutoff is determined by (3.62). The outputs V_{fbP} and V_{fbM} are then fed back to input of pre-amplifier.

4.3 Quantizer

The circuit implementation of quantizer is shown in Figure 4.22. This component contains of a regenerative latch and two D flip flops (DFF). The latch has two back to back inverters whose outputs are tied together with PMOS transistors. When the PMOS transistors M_7 and M_8 are on, the outputs of the inverters are held together and the latch is in tracking mode. After a short of period, both currents of inverters are equal by turning

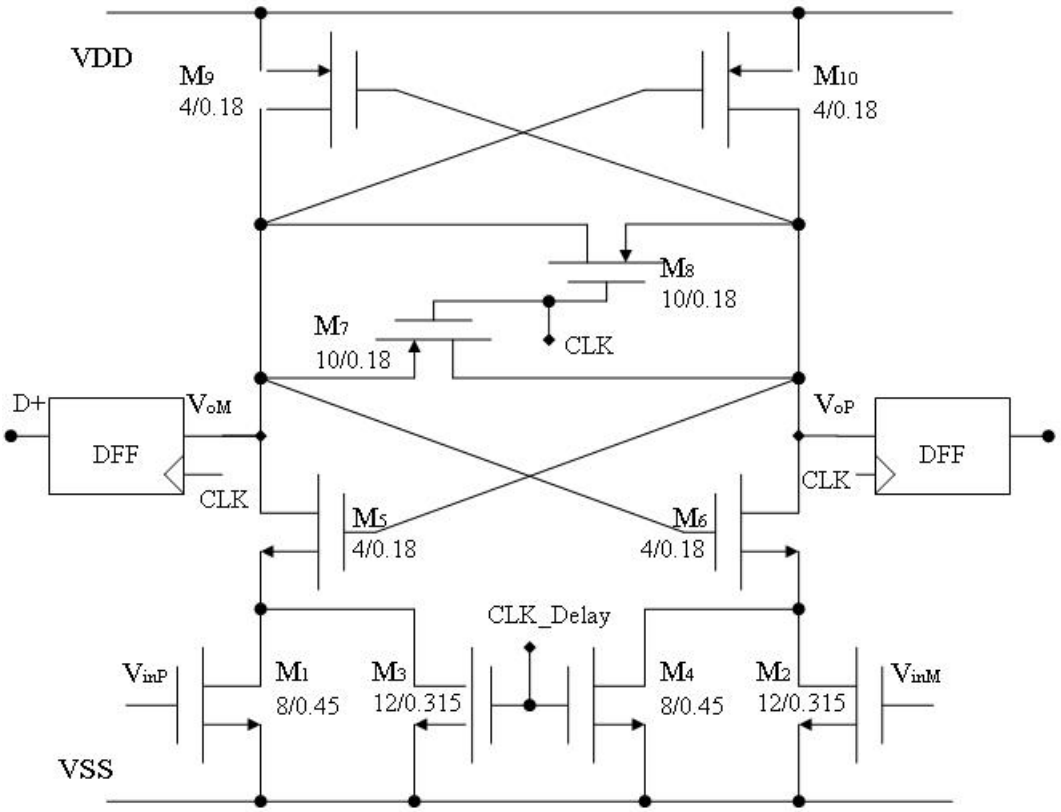

Figure 4.22: Implementation of Quantizer.

on the transistors M_3 and M_4. When a differential input signal is applied at the inputs to gate of transistors M_1 and M_2, the imbalance currents due to the differential voltages at the input result in one of inverters output goes high and the other goes low. This logic decisions are then fed to DFFs with a sampling frequency F_S. The outputs of DFFs are the digital output of overall system. The noise and unwanted signal at high frequency of digital output is then rejected by a LPF with cutoff frequency at 2 kHz.

4.4 Simulation Results

The IC is designed and implemented in Jazz semiconductor CMOS 0.18μm technology with power consumption 5.8 mW. The total input referred noise for overall system is 1

Table 4.3: Input Noise Summary for EEG, ECG, and EMG.

	ECG	EEG	EMG	Total Input Referred Noise
Frequency (Hz)	0.05-100	0.1-100	20-2000	0-2000
Noise (uVrms)	0.54	0.51	0.72	1

$uVrms$ as shown in Figure 4.23. The input referred noise for EEG, ECG, and EMG are also summarized in Table 4.3.

The CMRR is 102 dB as shown at the top of Figure 4.24. An input signal with amplitude

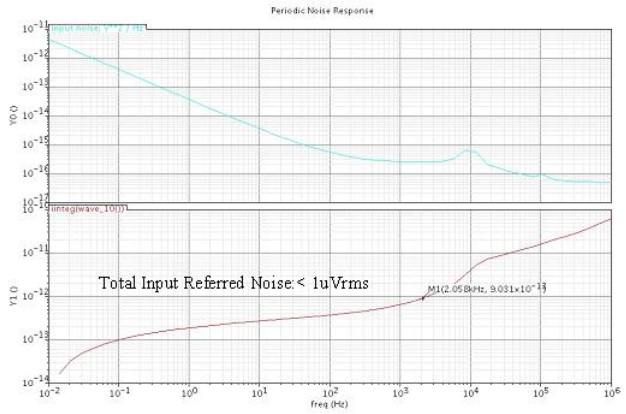

Figure 4.23: Total input referred noise.

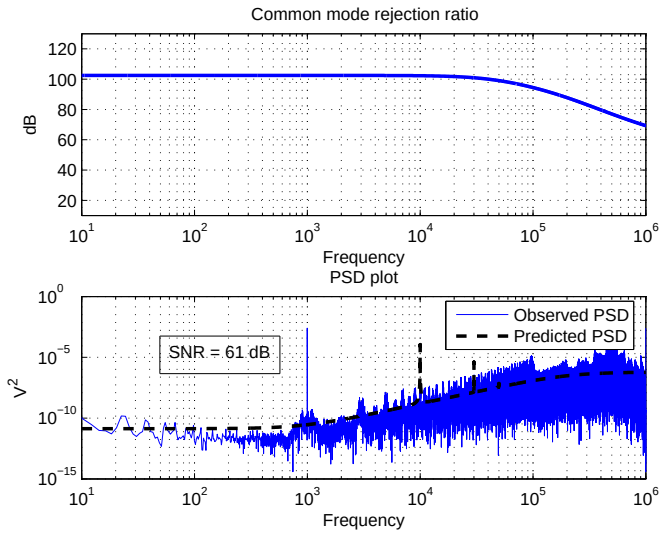

Figure 4.24: CMRR on the top and predicted and observed PSD on the bottom.

Table 4.4: Performance Summary

Parameter	Simulation
Supply Voltage (V)	±0.9
Supply Current (mA)	3.2
Gain (dB)	40
Low-Frequency cutoff	Via UP-DOWN counter
Input-referred noise (uVrms)	1
CMRR (dB)	102
Input Common-mode range (V)	±0.3

1 mV at frequency 1 kHz is also used to test the overall system; the SNR is 61 dB for observed PSD as shown at the bottom of Figure 4.24. The predicted PSD of noise is also similar to the observed PSD, but has a corner frequency that is higher than that of the observed PSD. This is due to the signal-dependent quantizer gain [38]. Table 5.4 summaries the performance for overall system.

From the table, the proposed design offers input referred noise of 1 $uVrms$, CMRR of 102 dB, and programmable low-frequency cutoff via UP-DOWN counter.

Chapter 5

Test Chip Results

5.1 Signal Reconstruction

The off-chip LPF is used to reject the quantization noise at high frequencies as shown in Figure 3.1. It also acts as anti-aliasing filter to limit the bandwidth of signal of interest. The signal reconstruction can be done by the process of averaging filter function and a rate reduction function. This process is also known as decimation [57].

Since the output signal of system is a single-bit data stream, a high-order linear-phase finite-impulse-response (FIR) LPF is used. The output of FIR LPF can be expressed

$$Y(k) = a_0X(k) + a_1X(k-1) + \ldots + a_nX(k-n). \tag{5.1}$$

where X(k) is the input sequence, n is the order, and a_i the filter coefficients. The advantage of FIR LPF is nonrecursive property based on (5.1). Although FIR filter takes more time to perform the decimation filtering process than infinite-impulse-response (IIR) filter for the same passband and out-of-band frequency characteristics, FIR filter can be designed to have a linear-phase response which is required for instrumentation applications. A 10000 order FIR LPF is designed with cutoff frequency at 2 kHz as shown in Figure 5.1. The phase response is linear over frequency 0-2 kHz. An input signal with amplitude $1mV$ at 1 kHz is used to test the system, the digital outputs are compared at the top of Figure 5.2. The input signal is reconstructed and shown at the bottom of Figure 5.2.

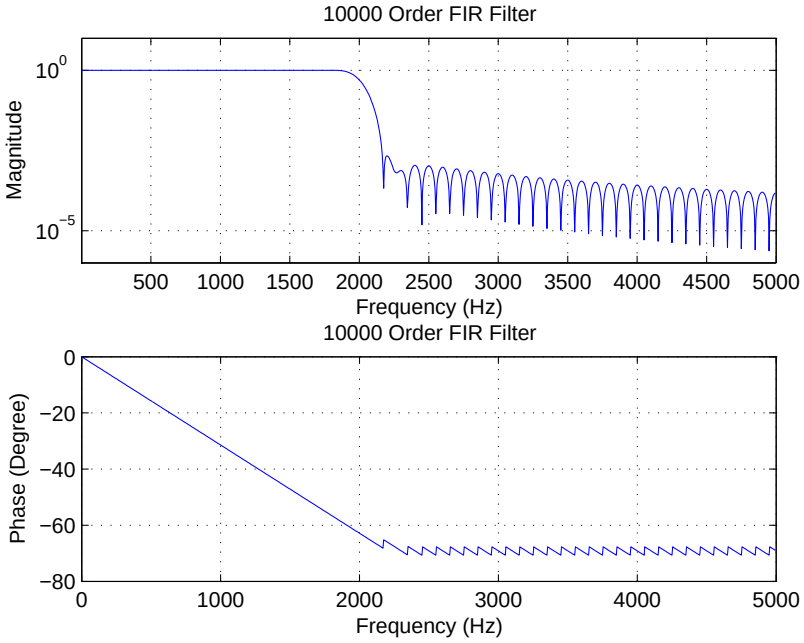

Figure 5.1: Frequency Response for FIR LPF with cutoff frequency at 2000 Hz.

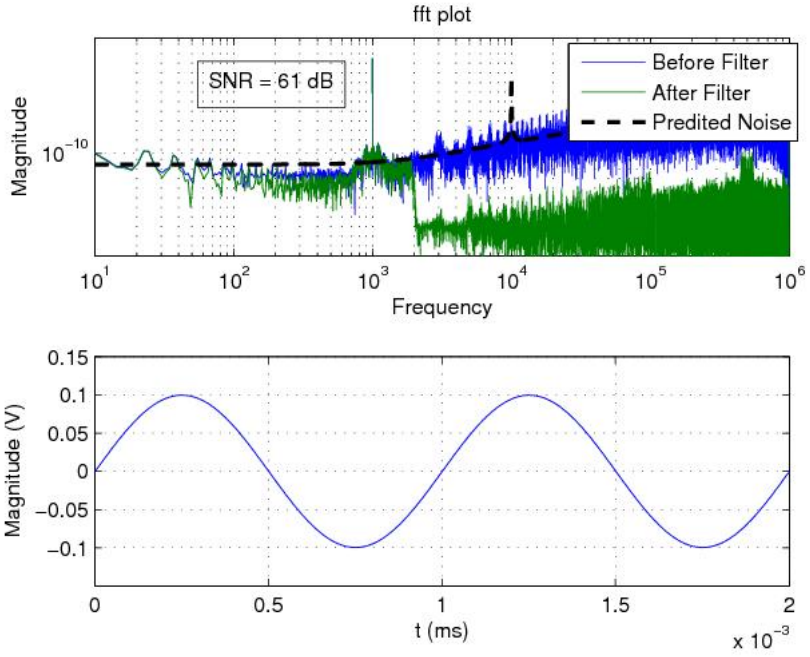

Figure 5.2: Output signal before and after FIR LPF and Signal Reconstruction.

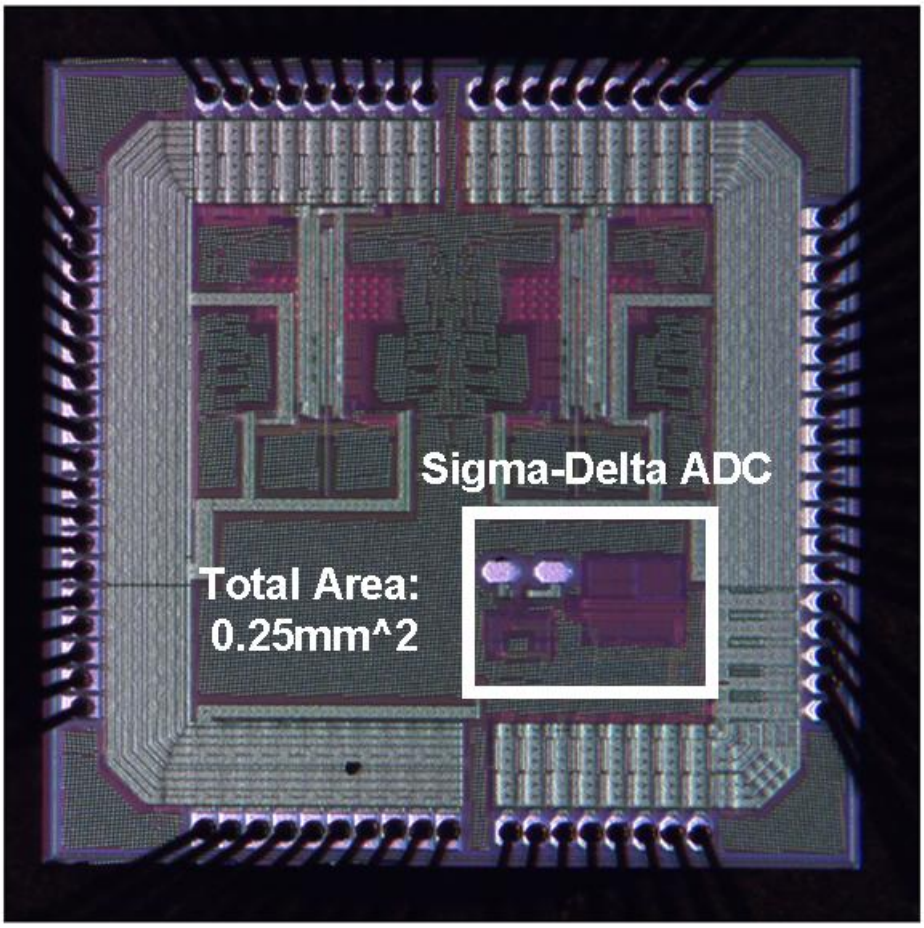

Figure 5.3: Die photo for Biomedical IC

5.2 Chip Evaluation

The overall system is fabricated on a chip with total area 0.25 mm^2. The photo die of circuitry is shown in Figure 5.3. The power supplies, reference voltages, timing signals , and input attenuator are required in order to test the biomedical IC. The implementation of circuits are discussed in this section.

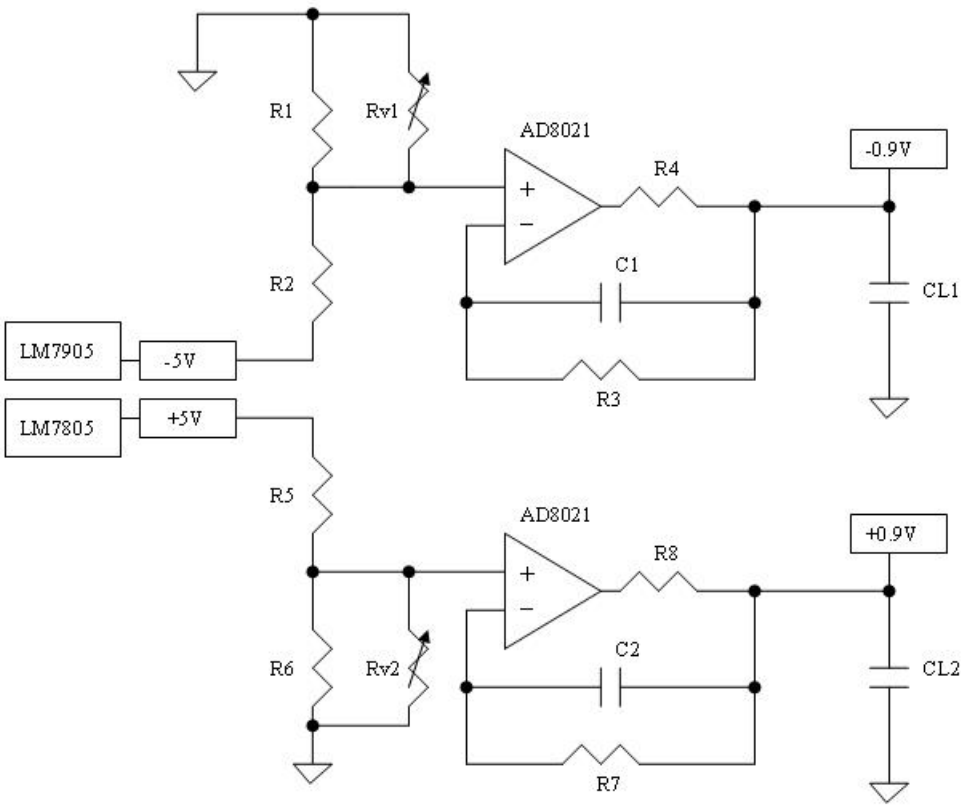

Figure 5.4: Positive 0.9V and negative 0.9V for IC

5.2.1 PCB Design

Power Rails and Reference Voltages

LM7805 and LM7905 regulators are used to generate positive 5 volts and negative 5 volts respectively. Its output currents are 100 mA which are sufficient to support overall components on the board. The TI TPS76301 regulator is chosen to supply 3.3 volts for digital pad ring of the chip. The positive 0.9 volts and negative 0.9 volts are generated as shown in Figure 5.4. Resistor R_1 and R_2 are used to divide the negative 5 volts generated by LM7905 to negative 0.9V. Resistor R_{V1} is used to fine tune the negative voltage 0.9V. The voltage at positive input of AD8021 is buffered in an non-inverting configuration to generate negative 0.9V power. Resistor R_4 at the output of op-amp stabilizes the op-amp, which has to drive the large bypass capacitor C_{L1}. The $C_1 - R_3$ network provides compensation.

Table 5.1: Components for 0.9V and -09V.

Components	-0.9V	Components	+0.9V
R_1	200 ohm	R_5	820 ohm
R_2	820 ohm	R_6	200 ohm
R_3	1 kohm	R_7	1 kohm
R_4	1 ohm	R_8	1 ohm
C_1	0.1 uF	C_5	0.1 uF
C_{L1}	1 uF	C_{L2}	1 uF

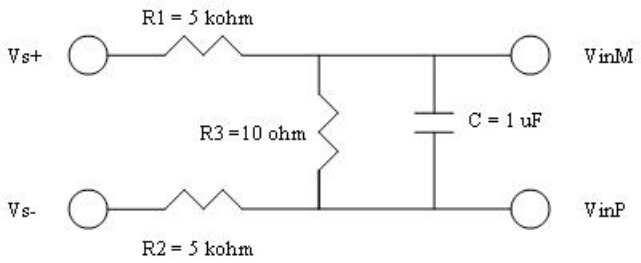

Figure 5.5: Input Attenuator

The same idea is applied to generate the positive 0.9V power, -Vref, and +Vref for DAC_2. Table 5.1 summaries the components for 0.9V and -0.9V.

Input Attenuator

In order to test the IC, an input signal with 1mV amplitude and low noise is required. An input attenuator is deigned with low noise as shown in Figure 5.5. Resistors R_1 and R_2 are voltage attenuator to divide 1 V input signal from function generator to 1 mV. Capacitor C is used to limit the bandwidth while keeping the noise of $kT/2C$.

Timing Signals

The sampling frequency F_S and chopping signals F_C are generated from crystal oscillator. The Spartan-3 Starter board is used with VHDL code to generate the sampling

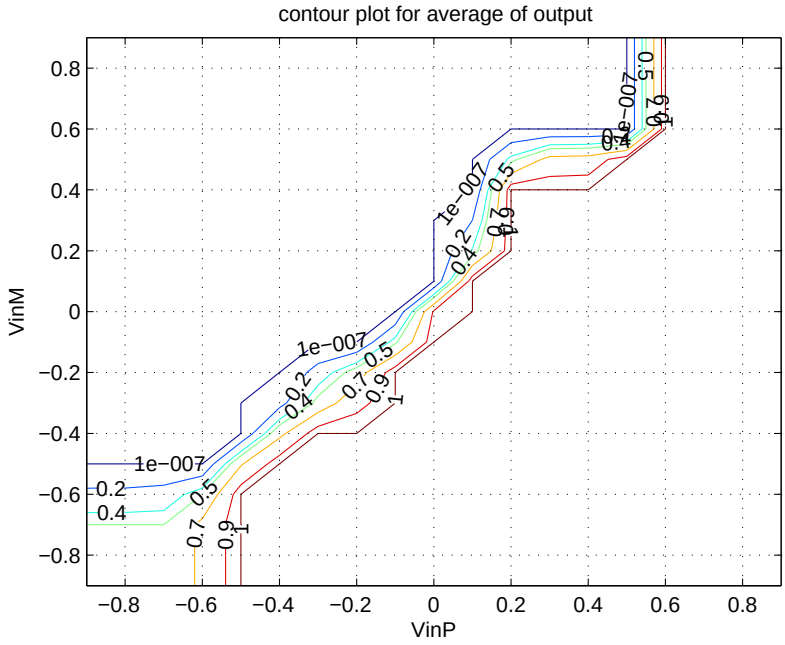

Figure 5.6: Averaging output.

frequency F_S at 1 MHz and chopping frequency F_C at 10 KHz.

Digital Output Acquisition

The National Instrument PCI-6533 (DIO-32HS) digital I/O board and Labview are used for data acquisition. This board has 32 digital I/O lines, at 5 V TTL/CMOS, and with a 2.5 MHz maximum input rate for an 8-bit word which is sufficient to handle the sampling frequency of 1 MHz.

5.2.2 Experimental Results

Digital Output Averaging

A DC test is performed first to determine the input output characteristic. According to section 3.3, the average of the modulator output will track the analog input without taking noise at high frequencies into account. A 19 sets of 100000 samples are acquired with $VinP = -0.9V$ and sweeping $VinM$ from -0.9V to 0.9V. Similarly, the $VinP$ is increased

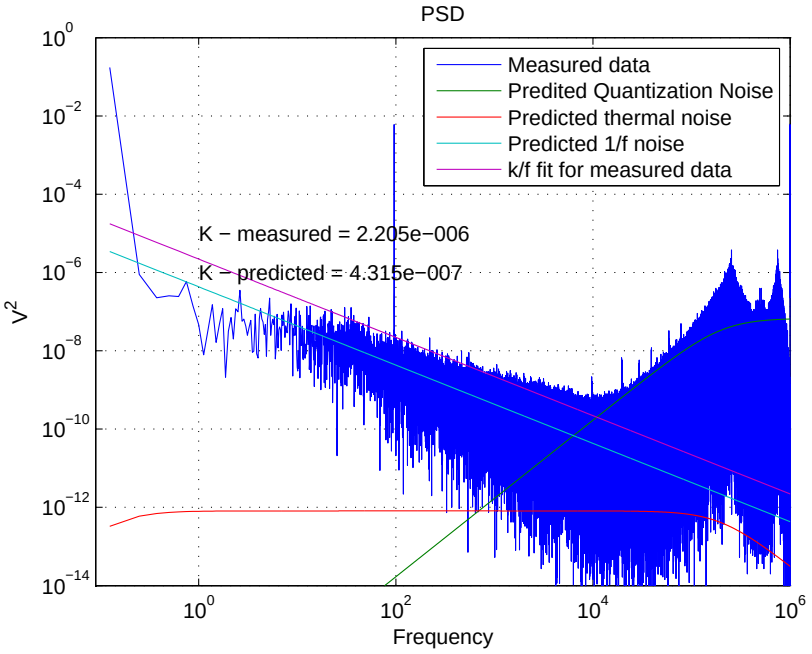

Figure 5.7: fft plot without chopping.

per 0.1V with sweeping of $VinM$ for 19×19 matrix data sets. The results are shown in Figure 5.6, where x-axis is voltages sweeping from -0.9V to 0.9V for $VinP$, and y-axis is voltage sweeping from -0.9V to 0.9V for $VinM$. The average digital output is scaled to 0.5 for $VinP = 0$ and $VinM = 0$ in this case. The contour plot shows the average of output tracks the analog input with pretty good linear ICMR, and large gain for differential input. Since the digital outputs contain the noise at high frequencies, the averaging output gives a good sign for ac testing in next step.

No Chopping

A total of 8000000 samples of data are collected with no chopping, sampling frequency F_S at 1 MHz, and an input with 1 mV amplitude at 100 Hz. The result is transformed into frequency domain by using an FFT algorithm in Matlab. This plot is shown in Figure 5.7. The 1/f noise is dominated at low frequencies while the quantization is presented at high frequencies for both predicted and measured PSD. The measured PSD is around 7 dB higher than predicted PSD. These effects are most likely the measured differential gain is

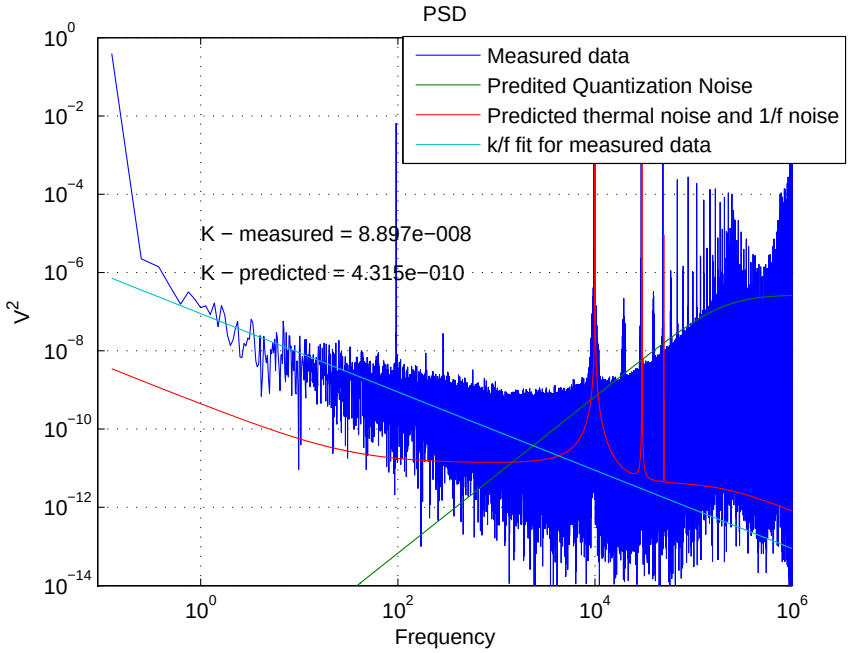

Figure 5.8: fft plot with chopping with input 1 mV amplitude at 100 Hz .

higher than the predicted one. In addition, the K constants for 1/f noise are $2.2e-6V^2 \cdot f$ and $4.3e-7V^2 \cdot f$ for measured and predicted data respectively. The measured data of K constant is 5 times larger than the predicted data from Cadence simulation. The PSD between measured and predicted data are acceptable for no chopping test. Notice that, SNR is determined by 1/f noise since the chopping blocks are not enable in this case.

With Chopping

A total of 8000000 samples of data are again acquired with sampling frequency F_S at 1 MHz, chopping frequency F_C at 10 KHz, and an input with 1 mV amplitude at 100 HZ. The PSD for predicted and measured data are shown in Figure 5.8. The 1/f noise of pre-amplifier is modulated and translated to the odd harmonic chopping frequencies in this case. However, the even harmonic chopping signals are still presented at high frequencies due to the duty cycle of chopping signals are not exactly 50 percent. There is another 1/f noise source due to first integrator amplifier at low frequencies as shown in Figure 5.8. The corner frequency between 1/f noise and thermal noise are less than 100 Hz and over

Table 5.2: Signal and Noise powers summary.

CASE	A	B	C	D	E	
[ϕ_1,ϕ_2]	[1,0]	[0,1]	[F_C,0]	[0,F_C]	[F_C,F_C]	unit
Signal Power	0.0049	0.0059	0.0012	0.0014	0.0054	v^2
Noise Power	2.37e-5	2.6e-5	9.82e-6	1.08e-5	8.45e-6	v^2
SNR	23.1	23.58	20.9	21.33	28.07	dB

1 KHz for predicted PSD and measured PSD respectively. The K constants of 1/f noise for predicted and measured data are $4.3e-10v^2 \cdot f$ and $8.9e-8v^2 \cdot f$, resulting in 23 dB difference. With integral PSD over frequency 0.25-2 kHz, the SNR is 28dB which is lower than the one we predicted in Chapter 3.

Table 5.2 summaries the signal and noise powers for different cases. The SNR is 23 dB without chopping for cases A and B. For cases C and D, one of chopping signals connects to F_C at 10 KHz and the other connects to negative rail, the signal power is reduce to 1/4 compare with cases A and B. When the chopping is applied for case E, the signal power is $0.0054V^2$ which is almost equal to no chopping cases A and B. The SNR is improved 5dB with chopping technique based on Table 5.2.

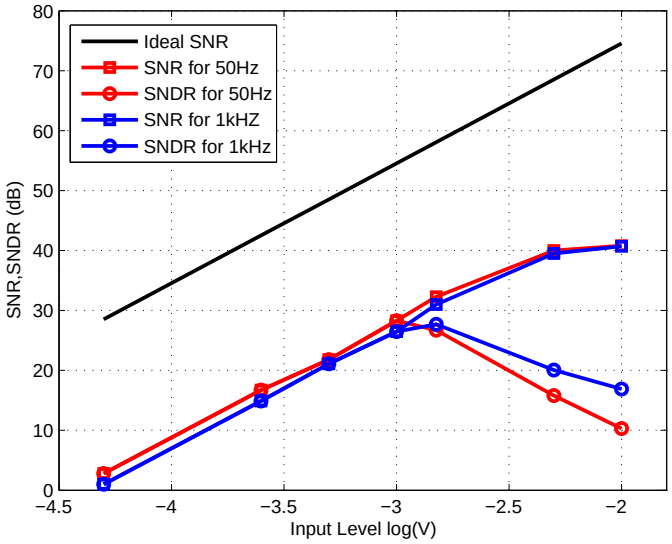

Figure 5.9: SNR and SNDR vs. Input Amplitude.

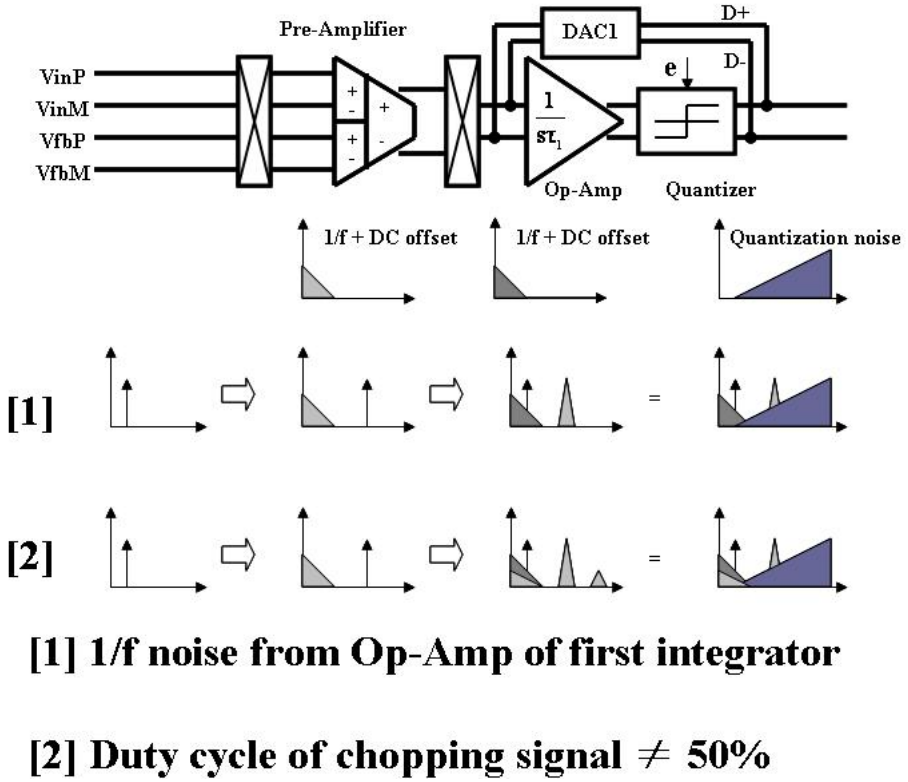

Figure 5.10: Problems for 1/f noise.

Figure 5.9 shows the relationship between input amplitude and SNR. The black line represents the ideal case while the red and blue lines are input signals at 50 Hz and 1 kHz respectively. From the Figure, the observed SNR is 20 dB lower than the predicted one due to the 1/f noise of first integrator amplifier. Also, the SNR is proportional to input amplitude and reaches peak value at amplitude of 100 mV. This is caused by the decrease of the gain of quantizer as the amplitude is increased. The decrease in gain of quantizer changes the shape of noise transfer function, causing the noise to move inside the band of interest [38,58]. For SNDR, it reaches the peak value at amplitude 1mV and decreases with increasing amplitude. This is due to the non-linear effects of pre-amplifier and quantizer. Figure 5.9 also shows the SNR and SNDR is frequency independent.

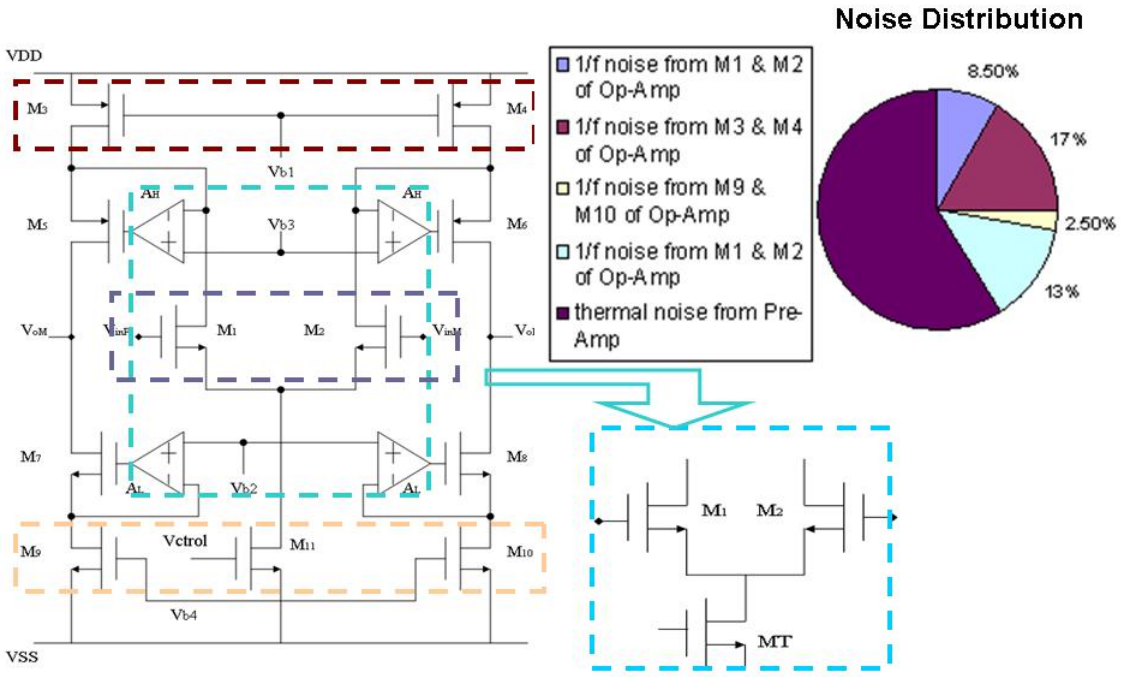

Figure 5.11: Noise Distribution.

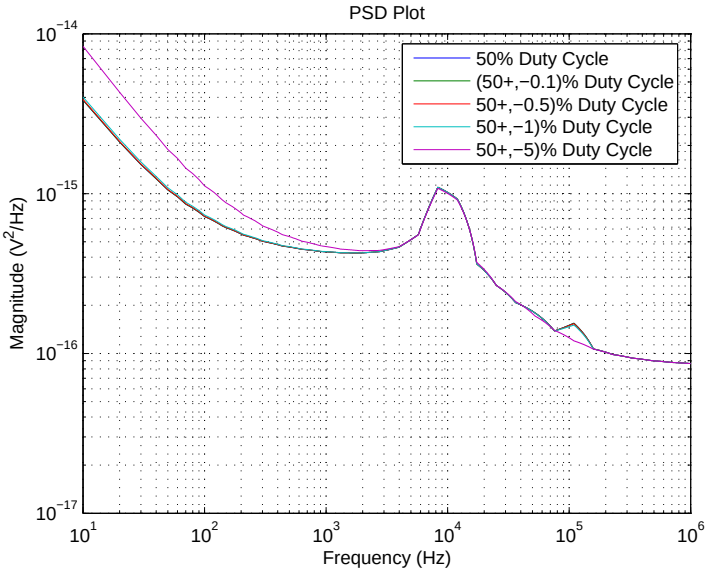

Figure 5.12: Noise analysis for different duty cycle.

Problems for 1/f noise

Two possible problems for 1/f noise at low frequencies are investigated as shown in Figure 5.10. The light and dark grays represent the dc offsets and 1/f noise for pre-amplifier and

Table 5.3: Total input referred noise for different duty cycles.

Duty Cycle	Total input referred noise (uVrms)	$(\frac{Real-Ideal}{Ideal})\times 100\%$ error
50%	1.07	0
$50 \pm 0.1\%$	1.13	6
$50 \pm 0.5\%$	1.14	6.5
$50 \pm 1\%$	1.162	9
$50 \pm 5\%$	1.48	38

Op-Amp of first integrator respectively. First, the 1/f noise of Op-Amp is too high and will present at the output. Second, the even harmonic chopping signals do not cancel out due to duty cycle is not equal to 50%. Thus, the 1/f noise of pre-amplifier is presented at low frequencies when the second chopper modulated the signals back to original. The noise behavior of overall system is verified again by Cadence. First, the noise analysis is simulated and verified as shown in Figure 5.11. About 40% of total input referred noise is from 1/f noise of Op-Amp of first integrator. If the measured 1/f noise is much higher than the spice model predicted, the SNR will decrease due to this effect.

Second, the different duty cycles of chopping signal are tested and plotted in Figure 5.12. Table 5.3 summaries the percentage error for different duty cycles. The error of total input referred noise is less than 10% if the duty cycle is less than 1%. Since the chopping signals are generated off chip, the error for total input referred noise is definitely less than 10%. To conclude, the 1/f noise is dominated by the 1/f noise of Op-Amp.

The performance parameters for measured data are summaried in Table 5.4 . The improvements for 1/f noise reduction are discussed next.

5.3 Improvements

After the $\Sigma\Delta$ ADC is experimentally characterized, two improvements can be made in order to reduce the 1/f noise effect at the input. These are described first for the large devices, then for auto-zero technique.

Table 5.4: Performance Summary.

Parameter	Measurement
Supply Voltage (mV)	±0.9
Supply Current (mA)	3.2
Peak SNDR (dB)	30
Input-referred noise (uVmrs)	27.9
CMRR (dB)	> 55
ICMR (V)	±0.3
Die Area (mm^2)	0.25

5.3.1 Large device area for first integrator op-amp

Equation (2.10) suggests that to decrease 1/f noise, the device area should be increased. However, increasing the devices area of transistors M_3 and M_4 of main amplifier will increase the capacitance at the drain of transistors M_3 and M_4. Since the nodes at the drain of transistors M_3 and M_4 are low impedance, the pole should still higher than the unity gain frequency of main amplifier. Therefore, the stability of amplifier will not affect by large devices of M_3 and M_4. Also, increasing devices area of transistors M_1 and M_2 of additional gain stages A_L and A_H will not affect the stability of amplifier.

5.3.2 Auto-zero technique

Another way to reduce the 1/f noise effect is auto-zero technique as discussed in Chapter.3. Since the first order $\Sigma\Delta$ is designed in continuous time domain, a feedforward technique for auto-zero should be applied for this application [24]. Although the total white noise is increased due to aliasing of the wide band noise (thermal noise) inherent to the sampling precess, the noise refer to the input is negligible. Other effects such as residual offset due to non-ideality of MOSFET switch and stability are given by [24].

Chapter 6

Conclusion and Future Work

6.1 Conclusion

A bio-potential acquisition system is presented in this thesis. The background of bio-potential signals and existing work are introduced in Chapter 1. The specifications and analog requirements for extracting bio-potential signals are discussed in Chapter 2. A novel second order $\Sigma\Delta$ ADC with feedback integrator to program the low frequency cutoff is introduced in Chapter 3. In order to improve wide ICMR, the CMFB circuit of feedback integrator is used as GM stage to provide wide ICMR to subtract the CM signals at the input by the pre-amplifier. The noise issues and bandwidth selection also are analyzed. In Chapter 4, the circuit implementation of each block is designed and discussed. The simulation results of overall system are met the specifications with input referred noise 1 uVmrs, the control of low frequency cutoff via N-bit counter, CMRR of 102 dB, and ICMR $\pm$ 0.3V.

In Chapter 5, the system is fabricated in 0.18 um CMOS technology with total die area $0.25mm^2$. The measured SNR is around 20 dB lower then the predicted one. The 1/f noise of pre-amplifier is translated to high frequencies by the chopping technique. However, the 1/f noise of Op-Amp of first integrator is amplified and presented at the outputs. This effect results in decreasing the SNR for the system.

6.2 Future Work

Two ways to improve the 1/f noise are discussed in 5.3. First, the large size of transistors can be made to reduce the 1/f noise effect. Since the parasitic capacitance is proportional to the total area of transistor, the second pole at the low impedance node will move to lower frequency. The stability problem should be considered if the second pole is less than three times of dominant pole.

Second, if the auto-zero technique is used in the future. It is best to apply for both Pre-Amplifier and Op-Amp of first integrator. Although the white noise will increase as discussed in Chapter. 3, it provides very large input impedance to buffer the input voltages from the electrodes. With improvement of circuitry in the future, the IC presented in this thesis can be used as one of multi-channel bio-medical applications.

Appendix A

Sigma-Delta ADC Matlab Code

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Idealized Signal Transfer Function and Noise transfer Function  %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all;clc;format long;

% Sampling Frequency
Fs = 1e6;

% Number of points
N = 8e6;

% to1 = C/gm , where C = 10pF and gm of 630e-6 uA/V is
% transconductance of Pre-Amplifier
to1 = 10e-12/630e-6;

% to2 = CF / CS / Fs, where CF is 20pF and CS = 50fF.
to2 = 20e-12/50e-15/Fs;
```

```
% b is gain of STF and set by the ratio of DAC1 and DAC2
b= .01;

f = Fs/N:Fs/N:Fs;
s = i*f*2*pi;

% Nb is number of bit for UP-DW counter.
Nb = 18;

% Signal Transfer Function (STF)
num = [0 to2 0];
den = [to1*to2 b*to2 2^(-Nb)];
h = polyval(num,s)./polyval(den,s);

% Noise Transfer Function (NTF)
numn = [to1*to2 0 0];
denn = [to1*to2 b*to2 2^(-Nb)];
hn = polyval(numn,s)./polyval(denn,s);

% Compare STF and NTF
% figure(1)
% loglog(f,abs(h),f,abs(hn));grid;
% xlabel('Frequency');ylabel('Magnitude');title('NTF & STF');
% axis tight

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%  Models for 1/f, white, and quantization Noise                  %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
%%%%%%%%%%%%%%%%%%%%%%
% Quantization noise %
%%%%%%%%%%%%%%%%%%%%%%

% step size for 1-bit quantizer is 1.8V.

VLsb = 1.8/sqrt(12);

% Quantization noise at the input
Vq = VLsb*ones(1,N)/sqrt(Fs);

% Quantization noise at the output.
VVq = (Vq.*abs(hn)).^2;

%%%%%%%%%%%%%%%%%%%%%%
% White noise        %
%%%%%%%%%%%%%%%%%%%%%%

% the total thermal noise is 9nV/sqrt(Hz) based on cadence simulation
whitenoise = 9e-9;

% thermal or white noise at the input
Vw = whitenoise*ones(1,N);

% white noise at the output
VVw = (Vw.*abs(h)).^2;

%%%%%%%%%%%%%%%%%%%%%%
%  1/f  noise        %
%%%%%%%%%%%%%%%%%%%%%%
```

```
% K constants for 1/f noise, the Ks are found by cadence simulation
% where K_cadeno and K_cadeni are K fit for output and input respectively

K_cadeno = 4.315451793498000e-007

K_cadeni = 1.368851885114884e-004;

% 1/f noise at the input
Vf = K_cadeni ./ f;

% 1/f noise at the output
VVf = K_cadeno ./ f;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%  find fk                                                            %
%%%                                                                     %
% f_k = f(1:1001);                                                      %
% k_caden = f_k.*maout(1:1001);                                         %
% K_caden = mean(k_caden);                                              %
% flick_fit = K_caden./f;                                               %
%%%                                                                     %
%%%                                                                     %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


% Chopping model for n = 1, 3 ,5 harmonics only.
% where Fchop = 10 KHz.

Fchop1 = 10e3;
```

```
Fchop3 = 30e3;
Fchop5 = 50e3;
FC1 = round(Fchop1*N/Fs);
FC3 = round(Fchop3*N/Fs);
FC5 = round(Fchop5*N/Fs);
maoutn = (Vf./b).^2 + (Vw./b).^2;
maout_rot = rot90(maoutn,2);
maout_t = [maout_rot(1:end-1) maoutn];
right1 = [zeros(1,FC1) maout_t(1:length(maout_t)-FC1)];
left1 = [maout_t(FC1+1:end) zeros(1,FC1)];
right3 = [zeros(1,FC3) maout_t(1:length(maout_t)-FC3)];
left3 = [maout_t(FC3+1:end) zeros(1,FC3)];
right5 = [zeros(1,FC5) maout_t(1:length(maout_t)-FC5)];
left5 = [maout_t(FC5+1:end) zeros(1,FC5)];
maout_T = (pi/2)^2*(right1 + left1 + 1/3^3*(right3 + left3)
+ 1/5^5*(right5 + left5));
maout_Tp = maout_T(N:length(maout_T));

% 1/f noise at the output
maout_Tm = maout_Tp.*abs(h)*b;

% Comparison for no chopping and with Chopping
% figure(2)
% loglog(f,VVf.*abs(h).*b,f,maout_Tm);grid
% xlabel('Frequency');ylabel('V^2');title('compare 1/f')
% legend('no chopping','with chopping')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Total plot for Vn(1/f), Vn(white), Vq noise  %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
% figure(3)
% loglog(f,Vq,f,Vw,f,Vf);grid
% xlabel('Frequency');ylabel('V/sqrt(Hz)');title('PSD for
Quantization, white and 1/f Noise at input')
% legend('Quantization Noise','White noise','1/f noise');

% figure(4)
% loglog(f,VVq,f,maout_Tm + VVw);grid
% axis([10^1 10^6 10^-12 10^-1])
% xlabel('Frequency');ylabel('V^2');title('PSD for Quantization,
white and 1/f Noise at output')
% legend('Quantization Noise','1/f and White noise with chop');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%    1mvp-p signal @ 100Hz  test     %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% fin = 100;
% t= 0:1/Fs:100e-3;
% x = .5e-3*sin(2*pi*fin*t);
% xf = abs(fft(x))/length(t);
% xff = (xf.*abs(h)).^2;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Total plot for  Vin @ 100Hz Vn(1/f), Vn(white), Wq noise  %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% figure(5)
% loglog(f,VVq,f,VV_fw,f,xff);grid
```

```
% axis([10^1 10^6 10^-12 10^-1])
% xlabel('Frequency');ylabel('V^2');title('PSD for Quantization,
white and 1/f Noise at output')
% legend('Quantization Noise','1/f and White noise','input test signal');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%          Measured data             %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Read measured data
B = csvread('input.csv',1);
Nd = length(B);
fd = Fs/Nd:Fs/Nd:Fs;
D1 = fft(B)/Nd;
PP = D1.*conj(D1);

% PSD plot for measured data
% figure(6)
% loglog(fd,PP)
% xlabel('Frequency');ylabel('V^2');title('PSD');grid
% axis([10^1 10^6 10^-12 10^-1])

% PSD plots for measured data, quantization noise, 1/f noise,
% and white noise at output
% figure(7)
% loglog(fd,PP,f,VVq,f,maout_Tm,f,VVw);grid
% xlabel('Frequency');ylabel('V^2');title('PSD')
% legend('Measured data','Quantization Noise','1/f and White noise');
% axis([10^1 10^6 10^-12 10^-1])
```

```
% PSD plots for measured data and total noise at output
% figure(8)
totalnoise = VVq + maout_Tm + VVw;
% loglog(fd,PP,f,totalnoise);grid
% hold on
% xlabel('Frequency');ylabel('V^2');title('PSD')
% axis([1e-1 10^6 10^-12 10^-1])



% SNR for predicted and measured data
% where vinf is input signal at 96 Hz from function generator.
vinf = 96;
sig = round(Nd / Fs * vinf);

% Select the signal for plus and minus 20 bins
S_bin = sig + [-20:20];

% Select the bandwidth from 0.25 Hz to 2 kHz
FL = .25; FH = 2000;
in_band = round(FL*Nd/Fs:Nd/Fs*FH);
noise_bin = setdiff(in_band,S_bin);

% Noise power for measured data
NP_m = sum(PP(int32(noise_bin)))

% signal power for measured data
Sig_P = sum(PP(int32(S_bin)))

% SNR for measured date
SNR = 10*log10(Sig_P/NP_m)
```

```
% noise power for predicted data
NP_p = sum(totalnoise(int32(in_band)))

% s = sprintf( 'Noise Power - measured = %0.4g',NP_m);
% s1 = sprintf( 'Noise Power - predicted = %0.4g',NP_p);
% text(1.2e2,1e-6,s)
% text(1.2e2,1e-8,s1)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        Comparison of K constants for predicted and measured data
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% K fit from 1 Hz to 90 Hz for measured data
fl = 1;fh = 90;
f_in = round(fl*Nd/Fs:fh*Nd/Fs);
f_k = f(f_in);

% k for measured data
k_measu = f_k.*PP(f_in)';
K_measu = mean(k_measu)
PP_fit = K_measu./fd;

% K constant with chopping at output.
% its value is verified by Cadence.
K_chop = 4.315451793498000e-10;
Kout_caden = K_chop./f;

figure(9)
loglog(fd,PP, f, VVq, f , VVw + maout_Tm , f, Kout_caden,fd,PP_fit);grid
```

```
xlabel('Frequency');ylabel('V^2');title('PSD')
legend('Measured data','Predited Quantization Noise','Predicted
 thermal noise and 1/f noise','Predicted K/f','k/f fit for measured data');
axis([0.9e-1 10^6 10^-14 10^0])
s = sprintf( 'K - measured = %0.4g',K_measu);
s1 = sprintf( 'K - predicted = %0.4g',K_chop);
text(1e0,1e-5,s)
text(1e0,1e-6,s1)
```

Appendix B

VHDL Code for Timing Signals and UP-DW Counter

```
-----------------------------------
-----------------------------------
----  Timing Signals ----------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity signaltest is
    Port ( reset,Din : in  STD_LOGIC;
           clk_50M : in  STD_LOGIC;
           clk_1M : out  STD_LOGIC;
           Frin1 : out  STD_LOGIC;
           Frin2 : out  STD_LOGIC;
           Fchop1 : out  STD_LOGIC;
           Fchop2 : out  STD_LOGIC;
  reset1,DAC_UP,DAC_DN : out STD_LOGIC);
```

```
end signaltest;

architecture Behavioral of signaltest is

    component timing is
           port ( clk : in  STD_LOGIC;
                  reset : in  STD_LOGIC;
                  Frin1, Frin2, Fchop1, Fchop2 : out  STD_LOGIC);
 end component;

 component counter is
            Port ( clk : in std_logic;
                   reset : in std_logic;
                Din : in std_logic;
                Dout1, Dout2 : out std_logic);
 end component;

   signal cstate,cstate1: std_logic;

begin
    -- Make copy of timing component
    timing1: timing port map (clk => cstate1, reset => reset,
    Frin1 => Frin1, Frin2 => Frin2, Fchop1 => Fchop1, Fchop2 => Fchop2);

 -- Make copy of 4 bit counter component

    counter8b1: counter port map (clk => cstate, reset => reset
     ,Din => Din, Dout1 => DAC_UP, Dout2 => DAC_DN);

 -- Generate 1M clock
```

```
  process(clk_50M,reset)
  variable count : integer range 0 to 25;
  begin

   if reset='1' then

   count:=0;
cstate <='0';
elsif clk_50M'EVENT and clk_50M = '1' then
count:=count+1;
if count=25 then
count:=1;
cstate <= not cstate;
  end if;
 end if;
end process;
clk_1M <= cstate;
      reset1 <= reset;


  process(clk_50M,reset)
  variable count : integer range 0 to 50;
  begin

   if reset='1' then

   count:=0;
cstate1 <='0';
elsif clk_50M'EVENT and clk_50M = '1' then
count:=count+1;
```

```
  if count = 50 then
  count:=1;
  cstate1 <= not cstate1;
    end if;
   end if;
  end process;
--  clk_1M <= cstate1;
        reset1 <= reset;

end Behavioral;




-- Additional Comments:
-- 4 bit counter
-- can be extended to 18 bit with signal n(17 downto 0)
----------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity counter is
  Port ( clk : in std_logic;
         reset : in std_logic;
 Din : in std_logic;
 Dout1, Dout2 : out std_logic);
-- Idle : out std_logic);
end counter;
```

```
architecture Behavioral of counter is
  signal n : std_logic_vector(3 downto 0);
begin
  process(reset, clk)
  begin
    if reset='1' then
      n <= "1000";
--    idle <= '1';
Dout1 <= '0';
Dout2 <= '0';
    elsif clk'event and clk='1' then
      if n="1111" then
  Dout1<='1';
--  Idle<='0';
  if Din='1' then
    n<="1001";
  else
    n<="0111";
  end if;
elsif n="0001" then
  Dout2<='1';
--  Idle<='0';
  if Din='1' then
    n<="1001";
  else
    n<="0111";
  end if;
else
  Dout1<='0';
```

```
  Dout2<='0';
--  Idle<='1';
  if Din='1' then
          n<=n+"0001";
        else
          n<=n-"0001";
        end if;
end if;
    end if;
  end process;
end Behavioral;
```

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