Settling Time Measurement Techniques Achieving High Precision at High Speeds

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Abstract

Settling time is very important for data acquisition systems because it is the primary factor that defines the data rate for a given error level. Therefore settling time measurement is a crucial test. The goal of the project was to design, test and compare different measurement techniques. Three methods were tested to the accuracies of 0.1% and 0.01%. Also simulations were conducted to explain the parameters that affect the settling behavior. Additionally bench measurements were correlated to simulation results. This report is intended as a guide for settling time measurements.

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Table of Contents

List of Figures and Tables

Executive Summary

Operational amplifiers are used in many applications such as control systems, filters, instrumentation, waveform generation, and data acquisition. With today's standards, high speed *and* high precision are amplifiers' main characteristics. With high precision comes the issue of settling behavior of an amplifier. Settling time is important especially in data acquisition systems, since it is the primary factor that defines the data transfer rate for a given accuracy.

Settling time is defined as the duration from an ideal step input until the output of the amplifier enters – and remains – within a specified error band related to the amplitude of the pulse and the expected final settling value. It can be separated into three parts: The delay, the slew, and recovery and linear settling. The delay is the dead time and purely due to propagation delay within the amplifier. The slew period is when the amplifier is trying to reach the final value. The recovery and linear settling is the duration when the amplifier recovers from slewing settles within the error band.

The goal of the project was to design test and compare different measurement methods that could determine settling time to the accuracies of 0.1% and 0.01%. Another goal was to explain settling behavior through simulations and correlate the simulation results to the bench results. The measurement of settling time is not as easy as it seems from its definition. Since very small amounts of voltages are being measured within few nanoseconds, it is a very challenging task.

The primary goal was accomplished by testing three different methods. One of the methods relies totally on the oscilloscope performance. On this technique, first the input signal is measured, then the output. Then the output signal is subtracted from the input signal by using the scope's math function in order to eliminate any input imperfections. However, it was proved that using this technique it is really hard to obtain any reliable results, especially with low-resolution scopes.

Another technique uses the amplifier in the inverting configuration. A bridge type of network is created with two additional resistors (other than the gain and the feedback resistors). The output of the bridge replicates the signal at the summing node of the amplifier. Therefore it is also referred as the 'false summing node'. Also, clamping this

node to prevent voltage excursions improves on more effective use of the oscilloscope resolution.

The last method tries to improve over the false summing node circuit. A current switch is added to amplifier's summing node and it is controlled by an input pulse. This way any interference from the input pulse characteristics to the amplifier is prevented. Therefore a very clean and a fast pulse response can be obtained. Another feature is the output switch. This switch is used to further limit the voltage swing in order to improve even more on the effectiveness of the scope resolution.

Three amplifiers were tested; two of them were current feedback amplifiers (AD8000 and AD8007), and the other was a voltage feedback amplifier (AD8045). Their 0.1% settling times, as given by the datasheet, are 8ns, 18ns, and 7.5ns respectively. Using the first method yielded the longest settling times, which did not correlate with the datasheet. The main problem with this method was the parastics in the circuit. The second and the third methods yielded similar results to each other and correlated to the datasheet.

Using method #2, the measurement is fairly easy. However input imperfections can cause problems. There were reflections – due to improper termination – observed on the waveforms, which did not interfere with the results. However, it could have been a lot worse and this reflects the vulnerability of the second method. Third method is the longest measurement, even though the results are reliable. A lot of time is spent on adjusting the bridge trims in order to minimize switching transients on the output. On the other hand, due to the input current switch, the pulse response of the amplifier was very clean.

After the tests were completed, it was concluded that the best method would be to use the advantages of Method #2 and #3. This means adding the current switch to the false summing node circuit. This way a very clean pulse is obtained with the additional advantages of the second technique. With the modern Schottky diodes and high-resolution modern oscilloscopes, 0.3V of voltage excursion would not cause any problems.

Two printed circuit boards were designed and manufactured. The first board included only the circuit of the third method. Although it worked very well, there was a short ringing on the amplifier's output. First, simulations were used to prove that this was

caused by parasitics, rather than building a second board right away. On the second board this ringing was completely eliminated. Nonetheless, this time there was an oscillation on the output switch. Through experiments and simulations the cause of this was linked to trace inductance. However a third was not built due to time constraints.

Simulations were not only used for parasitic investigations but also to understand the effects of various parameters on settling time. Effects of Pole-Zero pairs in the frequency response were examined. As the separation of the doublets increased, settling behavior extended. Also, the effect of frequency of the doublets was looked into. Stability is an important issue on settling time. It was seen that under-compensation resulted in a fast rise time but also in longer settling due to ringing. Over-compensation, on the other hand, resulted in long lasting tails, which extended the settling time as well. Therefore an optimal stability point must be found for best settling results. Also with the knowledge gained from these simulations, a correlation simulation of AD8007 was conducted where the simulation results came very close to the measurement results.

Settling time measurement is one of the hardest time domain tests. But with the guidance of this project the degree of difficulty can be lessened and reliable results can be obtained with relative ease.

1 Introduction

The use of the operational amplifiers has grown exceedingly in system design since their first introduction. They are used in many applications such as control systems, filters, instrumentation, waveform generation, and data acquisition. With the advances in technology, these applications require wideband amplifiers. However, sheer speed by itself is not enough. Precision is another important factor in amplifier design. Today the amplifiers are optimized for high speed *and* high precision.

When high speed and high precision are considered, settling time of the amplifier becomes important. Very briefly, settling time can be defined as the measure of how fast an amplifier can deliver a large, high speed input within a given error level. This measurement becomes more challenging with increasing settling speeds. Non-idealities of the components become more apparent and interfere with the measurement results. Thus the tests fail to provide reliable data.

Although the detailed frequency response of an amplifier might be an excellent tool to explain its behavior, time-response characterization is a must. Settling time is especially important in data acquisition. It is the primary factor that defines the fastest data rate for an intended accuracy. In other words, it will specify the error for a given transfer speed. For example, if an amplifier is to be used as a buffer in a sample-and-hold circuit, the customer would want to see the experimental results in time domain and not just some mathematical formulas and results that are derived from the frequency response of the component.

The goal of this project was to find a technique to accurately measure settling time to at least 10-bit accuracy (~0.1%) of today's high speed amplifier. Of course, higher accuracies were intended to achieve. 10-bit accuracy was a reasonable level of difficulty for the beginning of the project. A high speed amplifier means a 10-bit settling time of less than 10ns, which is another challenge by itself.

The aim was to realize the primary goal using different test techniques and work on the circuit to improve on the accuracy. The secondary goal was to explain the settling behavior in theory by using simulations. Although the simulations do not improve on testing methods, it is important to understand what is happening in reality for design purposes.

The purpose of this chapter was to explain the goals and the motivation of the project as well as to introduce the report outline. Next chapter provides the background information on settling time. Fundamentals such as the definition, the theory behind, and affecting parameters are provided. *Chapters 3* and *4* explain different circuit design and discuss the measurement results. *Chapter 5* provides the simulation results. *Chapter 6* is the conclusion section that discusses the accomplishments of the project with further remarks and recommendations.

2 Background Review

2.1 Settling Time Definition

Settling time was briefly explained in previous chapter. More specifically, settling time is the duration from an ideal step input until the output of the amplifier enters – and remains – within a specified error level related to the final value [18]. As shown on *Figure 2-1* there are three distinctive regions in settling time of an amplifier: Propagation delay, slewing of the amplifier (non-linear), and recovery and linear settling – or ringing (quasi-linear).
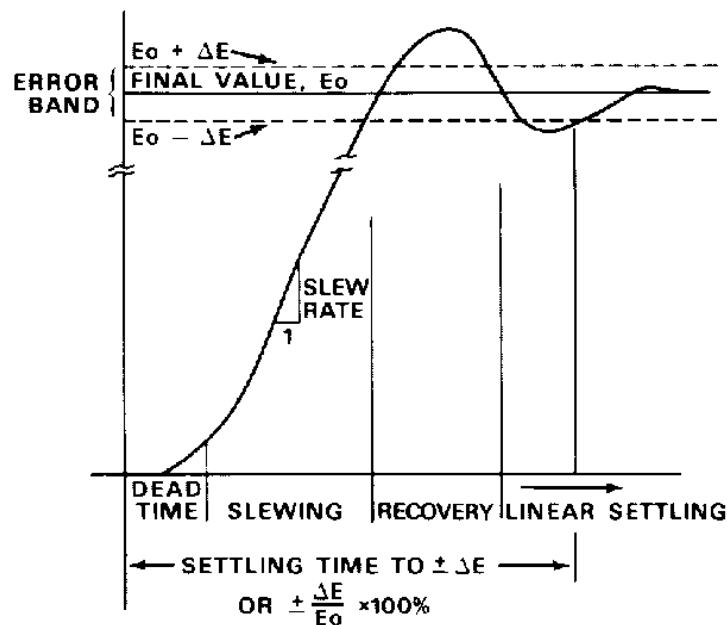
Figure 2-1: Definition of Settling Time [18]

The initial delay (dead time) is usually a short term [11]. Slewing period is a non-linear phenomenon. The length of this period is usually determined by the maximum available input stage current to charge/discharge the compensation capacitor (as well as parasitic capacitances). After slew limiting, amplifier settles towards the final value in a quasi-linear way [5][17]. In high speed amplifiers the slewing period is really short (only few nanoseconds). If the amplifier is poorly compensated and/or there is an imprecise pole-zero cancellation, then the recovery time might be the dominant factor in settling. There are number of parameters that affect the settling duration and these are examined in the next section.

The error band is defined as a percentage of the amplitude of the output step. Once the ringing is confined within that percentage near the final value, the amplifier is assumed settled for a specific error level. Assuming an output step from –2.5V to 2.5V, this results in a 0.1% settling band of ±5mV. Therefore 0.1% settling is not complete until the waveform is bounded between 2.505V and 2.495V.

Although it may look easy to measure settling time by looking at the description, it is a difficult task especially when higher precisions are considered. Measurements of these fine voltage levels are a difficult task at any speed. Also it is difficult to isolate any testing method from affecting the performance of an amplifier.

2.2 Design Parameters Affecting Settling Duration

2.2.1 Slew Rate

Slew rate limiting is one of the major disadvantages of the amplifiers. Basically it is a limitation on the maximum rate of change of the output voltage of the amplifier [16]. The main cause of this limitation is the non-linear behavior of the input stage. *Figure 2-2* models a simple op-amp model.
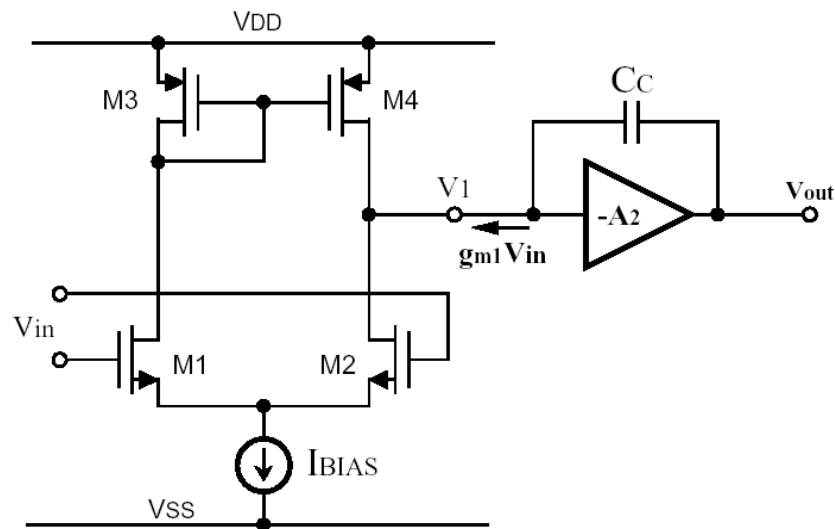
Figure 2-2: Dominant Pole Op-Amp Model [9]

The first stage is a differential input stage and a second gain stage is connected to it. There is a compensation capacitor added across the second gain stage in order to increase the phase margin at unity gain (to make the op-amp more stable) [4], [9]. Assuming all ideal components (i.e. no parasitics) and infinite bias current, one would expect the

output voltage rise linearly (in this case exponentially) for an instantaneous input voltage. Since there is a limited current to charge/discharge the compensation capacitor, the output voltage is actually a non-linear function of the input voltage [4], [8], [9]. This is illustrated on *Figure 2-3*.
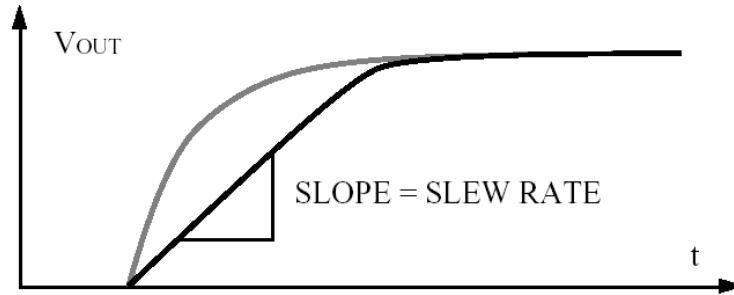
Figure 2-3: Slewing of the Output Voltage [9]

The gray line indicates the expected output voltage rise [9]. If a dominant pole op-amp model is assumed and without any current limitations, for an ideal input step the output voltage would rise exponentially (i.e. $v_{OUT} = v_{IN} \cdot \left[1 - e^{-\tau} \right]$). But looking at the *Figure 2-2* again, it is apparent that the maximum current available to charge C_C is I_{BIAS}. Therefore:

$$C_C \cdot \frac{dv_{OUT}}{dt} = I_{BIAS} \qquad \Rightarrow SR = \frac{dv_{OUT}}{dt} = \frac{I_{BIAS}}{C_C}$$

Since both terms on the right hand side of the equation are constants, the output is expected to ramp up, instead of rising exponentially. Even though increasing the input stage bias current seems as a logical option, excessive currents would, then, degrade the AC accuracy and drift specifications [18]. Thus (everything else remaining constant), this would increase the settling period instead of shortening it.

The compensation capacitor is not the only component that affects the slew rate. There are parasitic capacitances inherent to the silicon, stray capacitances due to the external circuitry, and as well as capacitive loads [16]. All of these would slow down the output voltage increase rate.

2.2.2 Pole-Zero Matching

Recovery and linear settling is the most crucial part of the settling. This portion is particularly sensitive to the detailed shape of the open loop frequency response

(magnitude *and* phase) of the amplifier. The impact of pole-zero pairs on settling time is significant [17]. These doublets could be caused by couple of reasons.

For example, an added feed-forward compensation capacitor across a pnp transistor, in order to broadband the level shift, will introduce a zero [2]. This zero does not exactly cancel the pole introduced by the pnp transistor. Another reason that creates a doublet is bypassing one side of an active load [17]. There are number of other reasons that create pole-zero pairs, which - in theory - can be perfectly matched. A perfect match is nominal for best settling performance. Although there are techniques for doublet compression, components variations in IC production can cause up to $\pm30\%$ mismatch in pole-zero locations [2].

Figure 2-4 illustrates an open loop response of an amplifier with different mismatch conditions. With a perfect match $m = 1$, which means that the pole and the zero are at the same frequency [18]. If $m < 1$, then the zero frequency is higher than the pole frequency. Opposite is true if $m > 1$. Corresponding step responses are also illustrated in the graph.
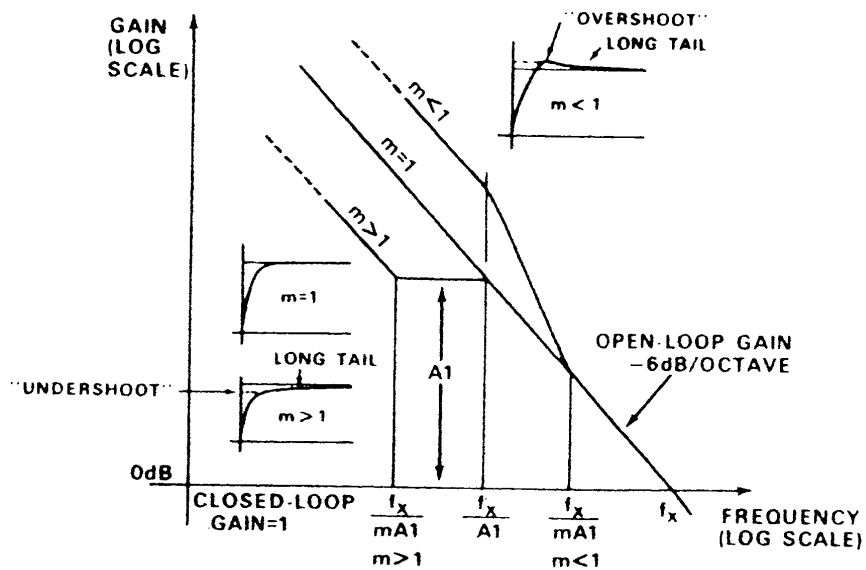
Figure 2-4: Pole-Zero Matching Illustration [18]

The effect of the doublets depends on their frequency and their separation as well as the input step amplitude [5], [18]. A larger separation will result in a slower settling component, thus it will extend the settling time. Also a low frequency doublet means that the step response has a smaller overshoot but a longer tail. In the other hand, a high

frequency doublet has a bigger overshoot with faster decaying tail. A simulation of this behavior presented on *Figure 2-5*.
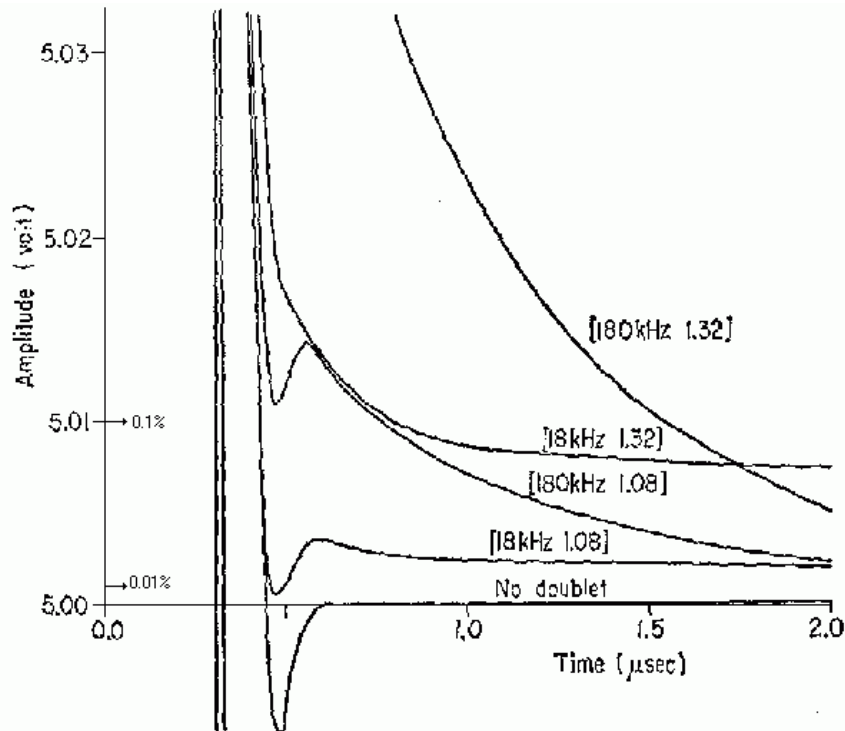
Figure 2-5: Low vs. High Frequency Doublet (with specific doublet separation) [5]

This graph is an output of a unity gain amplifier with a step input of $10V_{P-P}$. The simulation had been accomplished with two different doublet frequencies. For each frequency, two different separation values (ω_Z/ω_P) were experimented [5]. The case of perfect matching ("no doublet") is presented on the graph. Also it should be noted that since $\omega_Z > \omega_P$, the response overshoots.

One might ask the question "Which one, then, is the faster settling; high frequency or low frequency doublet?" It depends on the particular situation. Since the doublet with lower frequency has a smaller overshoot, it might as well be within the 0.1% band even though its tail is still decaying [5]. On the other hand the high frequency doublet has a bigger overshoot but because of its faster decaying tail it might get in the 0.01% band faster than the lower frequency doublet. This situation can be observed in *Figure 2-5*, additionally, *Figure 2-6* shows a clearer picture of this incident.
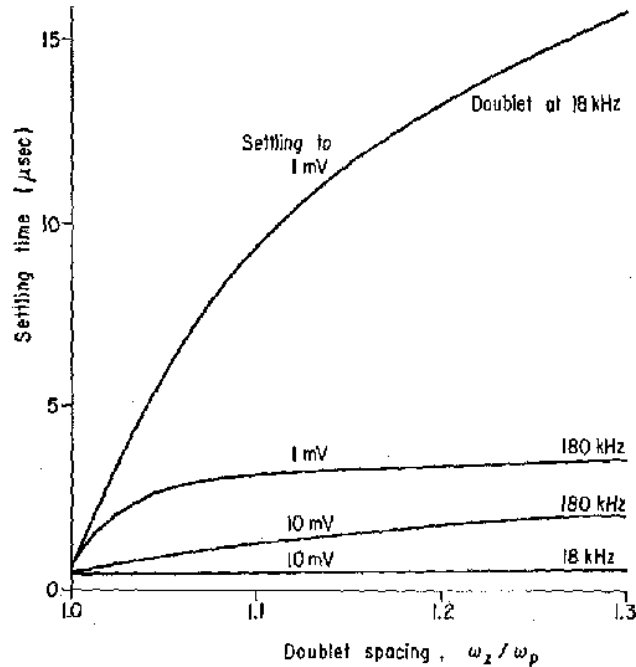
Figure 2-6: Doublet Spacing vs. Settling Time [5]

It is clear from the graph that for 0.1% case lower frequency doublet is faster settling due to its smaller overshoot. Higher frequency doublet wins the race for 0.01% case as a result of its shorter tail. The graph also shows that an increased separation causes the settling time to extend.

Pole-Zero pairs play a big role in settling time [2], [5] [17], [18]. Even though they may not greatly affect the frequency response of the amplifier, they can severely degrade settling performance. A fast slew rate by itself does not necessarily mean a faster settling amplifier. A clean shape of the open loop response will give the best results. Test circuit should be carefully designed to prevent parasitics. Stray capacitance, wiring, external compensation, etc. will alter the open loop (thus the closed loop) performance. Therefore, for a precise settling time measurement result, layout of the circuit, load conditions, closed loop configurations, and input signal properties must be provided.

2.2.3 Phase Margin & Compensation

It was previously discussed that the duration of the slewing period and the quasi-linear settling period is inversely proportional to the unity gain bandwidth of the amplifier. Consequently an op-amp is designed for high crossover frequency and for optimal phase margin. In theory an amplifier must not be worse than critically damped in

8

order to prevent any oscillation or ringing [7]. If overshooting is acceptable to a level, then damping ratio could be lowered.

A dominant pole must be provided in order to achieve an acceptable phase margin ($\sim\geq45°$) at unity gain [7], [9], [14]. It is introduced by a compensation capacitor. Since there is a trade-off between high speed and stability, this capacitor should be chosen for desired time domain response. A larger capacitor will decrease the slew rate due to the previously discussed reasons. It is one of the disadvantages of adding a compensation capacitor. In the other hand the quasi-linear region might or might not extend; it depends of the chosen damping ratio (phase margin).

Poorly damped systems will have longer (if not sustained or increasing) ringing [5], [7], [14]. This will clearly extend the settling time of the amplifier. The other extreme case is over-damped systems. In that case, the amplifier will suffer from a long tail due to the exponential rise with a long time constant [5]. The rule of thumb is that best results are achieved with a phase margin of about 60 degrees (or damping ratio, $\zeta\cong0.6$) [7]. *Figure 2-7* is a simulation of step response for a specific compensation capacitor (thus a specific damping ratio).

Curve	C_C(pF)	$\omega_1/2\pi$(Hz)	$\omega_2/2\pi$(Hz)	ξ
1	1.0	601	3.53×10^6	0 53
2	2.0	302	3.83×10^6	0.78
3	3.0	201	3.94×10^6	0.97
4	4.5	135	4.03×10^8	1.19
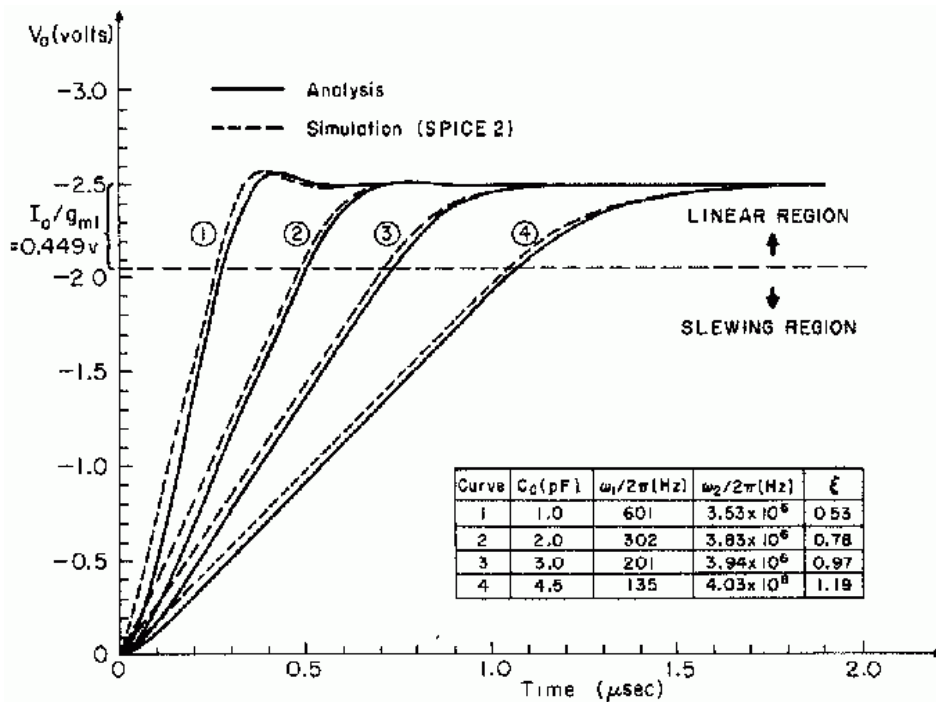
Figure 2-7: Compensation vs. Fast Settling Trade Off [5]

In this graph, 1st system has the least damping while 4th system has the highest damping. Since 2nd system has more damping, its slew rate is lower than the 1st, as expected. But looking at the settling duration, there is not much difference (it is more clear in *Figure 2-8*). This is a consequence of overshoot/slew rate trade off. Noticeably 3rd and 4th systems are over-damped and neither improves on the slew rate nor on the settling time [5].
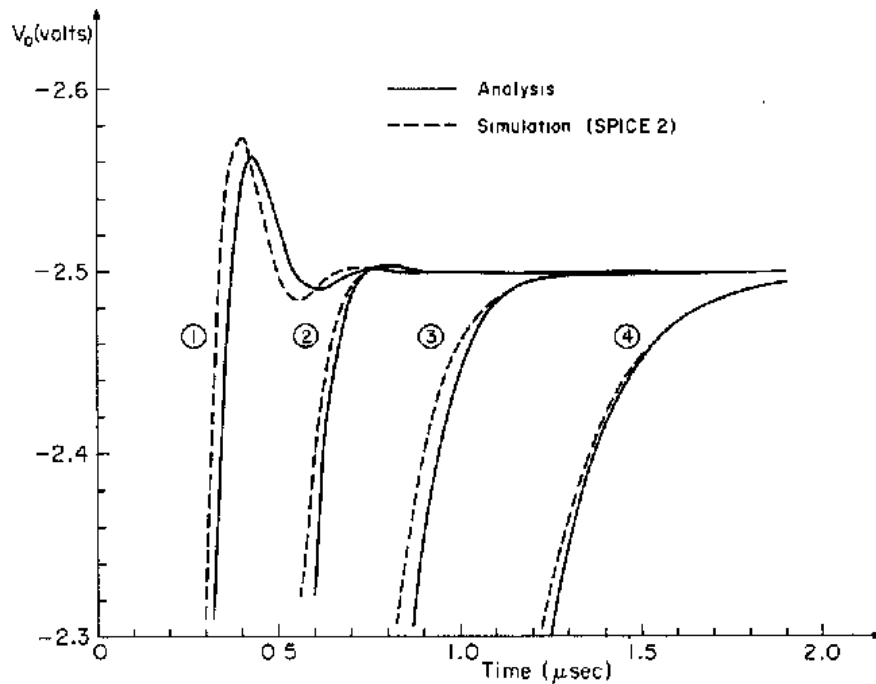
Figure 2-8: Compensation vs. Fast Settling Trade Off (expanded in y-axis) [5]

As a summary, three important factors of the settling time were briefly discussed in this section. None, however, by itself is a determining factor on the settling time. Altering with anyone of them, will affect the others. Therefore if designing for best settling performance, one needs to think in *multiple dimensions*. A smaller compensation capacitor might increase the slew rate but it will also increase the amount of overshoot. A bigger capacitor means a lower crossover frequency. This results in lower slew rate as well as decreased doublet gain at a given frequency, which in turn causes slower decaying tails. A fast slew rate will not improve settling by itself, if care is not taken in the design to decrease the doublet separation. Better settling results can be achieved by analyzing these tradeoffs and by optimizing each parameter for the best performance.

2.3 Definition of Noise and Related Issues

While it is relatively easy to design an amplifier with extreme gains, the more challenging task is to maximize the limit on the smallest magnitude of an input signal (i.e. optimize for the maximum available gain) [10]. The minimum input signal magnitude is restricted by the *background signals*, which create the noise floor. The output signal of the amplifier must be distinct from the output noise.

The noise in the amplifier is created by the physical mechanisms within the components that were used to design the amplifier [10]. Even though an ammeter might indicate a continuous flow of current, it is - in reality - a discrete movement. The magnitude of the current depends on the amount of charge (or, number of electrons) that flows in a given time. Also, the flow of current is unpredictable. For example, there is no way of knowing that when an electron will pass through a forward biased PN junction. Since, now, statistics must be used to explain this random behavior, the description of the noise voltages and noise currents become probabilistic. Therefore two different AC noise sources are assumed totally random and uncorrelated with each other. This means that there is simply no way to cancel an AC noise source with another AC noise source (unlike DC errors of the amplifier). In addition to being non-deterministic, AC noise sources are frequency dependent. Therefore the bandwidth of the circuit is important. A larger bandwidth will cause a greater output noise. Therefore the bandwidth should be kept as small as possible (i.e. large enough to transmit the required signal information).

The random behavior brings up another issue: the addition of the AC noise sources. Since the sources are uncorrelated, the algebraic addition does not apply (i.e. there is "+" or "−"). RMS addition must be used [10]. Also, ambient temperature (in °K) is another parameter that affects the noise. The erratic movement of the charges is made even more complex by the thermal energy that they have. The noise caused by the thermal motion is called the Johnson noise. The thermal noise is best characterized by the noise power or by the average value of square of the noise voltage. If noise voltage is e_n, then:

$$\left\langle e_n^2 \right\rangle = 4kT \cdot R \cdot BW \quad [V^2/Hz]$$

and   k is the Boltzmann's Constant

T is the temperature in °K

R is the resistance in Ω

BW is the noise bandwidth in Hz

Any conductor with a temperature above absolute zero is a noise source by itself, as thermal motion exists for temperatures above $0°K$ [10]. Johnson noise is frequency independent and has a uniform spectral density. Since it exists at all frequencies, it is also referred as white noise (analogous to white light).

While it may be easy to calculate the AC noise voltage of a resistor, it could be quite complex to do so for the op-amps [10]. The input noise of the op-amp depends on the design. Also, usually, op-amps with large input DC currents have low AC noise voltage.

Additional to AC noise voltage source, there is AC noise current source, which is due to the DC current flow [10]. This noise is also known as the shot noise. It is also a *white* noise and represented by mean-square current. Even though the op-amps have high input impedance, it is not infinite; meaning that there is a DC current flow at each input (e.g. base current, I_B, of BJTs). An idea could be to design an amplifier that internally generates the anticipated value of I_B. While these currents could be trimmed to match in order make the apparent current flow to be zero, since the noise sources are uncorrelated, the overall AC current noise increases. If the source resistance is low, using BJTs might give better overall noise performance. In the other hand, if the source resistance is high, FETs should be considered for their extremely low gate currents (in the order of pA). The AC noise sources of an op-amp are illustrated in *Figure 2-9*. The noise sources are drawn outside and the op-amp is considered noiseless.
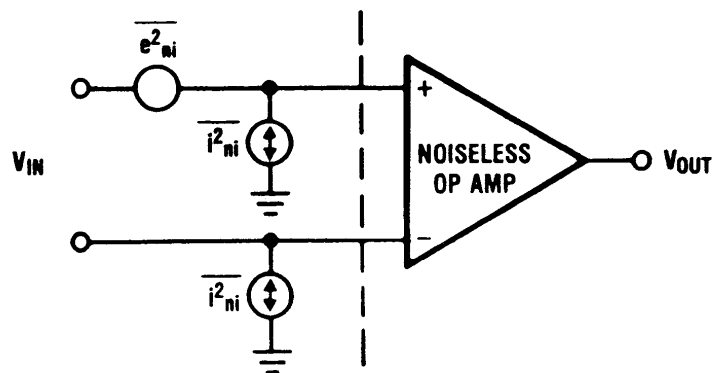
Figure 2-9: AC Noise Model of an Amplifier [10]

An amplifier is most likely to be used in the closed loop configuration [10]. There are noise sources due to the external elements in addition to the noise sources inherent to the amplifier. It is worthy to calculate the expected noise at the output of the amplifier. The result will give an idea on how small the output signal could be without being lost in the noise. A brief example is demonstrated using the previously presented noise model. The amplifier configuration is redrawn on *Figure 2-10*.
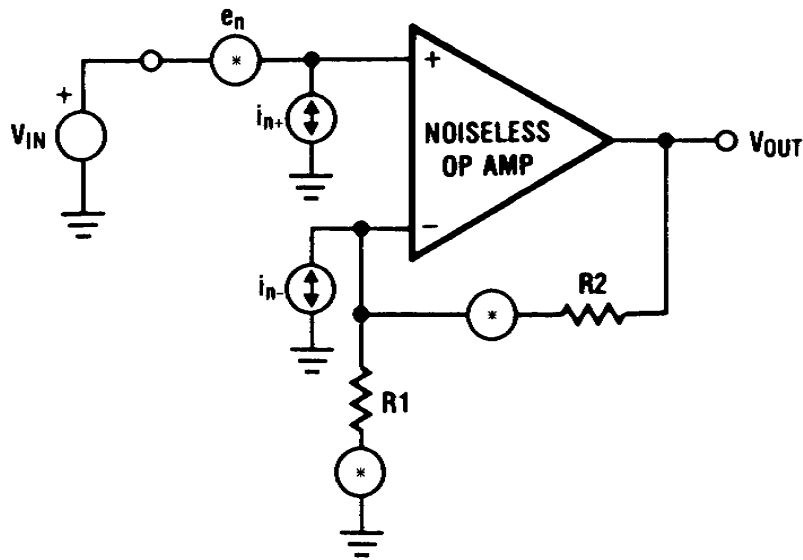
Figure 2-10: Calculation of Expected Output Noise on Non-Inverting Configuration [10]

The reference point for the noise analysis is the output. Before starting the analysis the all the sources should be suppressed (in this case V_{IN} is shorted). It is assumed white noise for all the noise sources. Next thing to do is to find the transfer function of each noise source to the reference point – the output.

Using superposition, e_n has a gain of R_2/R_1+1. i_{n+} does not affect the output (assuming infinite input impedance) and has a gain of zero. i_{n-} flows only through R_2 to the output, therefore its gain is R_2. This is because the inverting input is a signal ground therefore no AC signal is accumulated at that node. Noise due to R_2 appears directly at the output, which means a gain of 1. Noise due to R_1 has a gain of R_2/R_1. The noise densities of e_n, i_{n+}, and i_{n-} depend on the internal design of the amplifier. The noise due to the resistive network can be calculated using the white noise equation. The resulting output noise of the each source is summarized on *Table 2-1*.

13

Noise Source	Value	Gain	Output Noise $[V/\sqrt{Hz}]$
e_n	e_n	R_2/R_1+1	$e_n \times [R_2/R_1 + 1]$
i_{n+}	i_{n+}	0	0
i_{n-}	i_{n-}	R_2	$i_{n-} \times R_2$
R_1	$\sqrt{4kT \cdot R_1}$	R_2/R_1	$\sqrt{4kT \cdot R_1} \times R_2/R_1$
R_2	$\sqrt{4kT \cdot R_2}$	1	$\sqrt{4kT \cdot R_2}$

Table 2-1: Overall Noise Sources

The total noise density is found using RMS addition. The total RMS noise is the integration of the noise density over the noise bandwidth (roughly $f_T \cdot \pi/2$ for a first order system) [10]. The last task would be to find the peak-to-peak noise voltage. Although it is easy to read the value from an oscilloscope, it is not deterministic to calculate it due to the statistical nature of the noise. A general approach is that the noise amplitude is 5 times of the RMS value with 1.2% probability of having larger amplitude.

Until now the focus was on the white noise. There is also *Flicker (1/f) Noise* that exists at lower frequencies [10]. As the frequency increases, the energy content of this type of noise decreases. Therefore at low frequencies flicker noise might be dominant. However with increasing frequency white noise becomes more of a problem as shown on *Figure 2-11*. Also at very low frequencies 1/f noise becomes inseparable from DC drift effects.

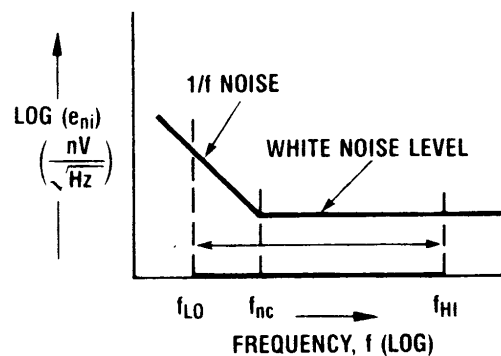**Figure 2-11: Illustration of White Noise Region vs. Flicker Noise Region [10]**

Since the settling time involves the measurement of signals with very small amplitudes, noise is a factor that cannot be ignored. If the output noise of the amplifier is

greater than the error band defined for settling, the settling time cannot be measured [18]. The external components added to the test circuit might increase the noise levels. This might require the filtering of the signal. While cleaning out the noise might help the measurement, extensive filtering might attenuate the signal as well, thus creating erroneous results. The method used above is a useful tool to predict the noise level at the output. Hence, it would help to determine reasonable amount of filtering. Other than the amplifier and the external components, there might also be interference noise due to the environment. Some of the sources for the interference noise could be due to the power supply noise, the input signal, unintentional ground loops, and even from radiations from transmitters. As a result the test circuitry might require shielding [1]. The test board should be designed to minimize the noise in the circuit.

2.4 Oscilloscope Overdrive

While analyzing a waveform on an oscilloscope, it is often required to observe the details of the waveform rather than just large signal characteristics. These details could include an overshoot, a ripple, or other kinds of small aberrations. For example, measuring 0.1% settling time of a 5V step means a resolution of 5mV or even less.

One of the techniques to increase the resolution to display only a small part of the waveform is to offset the signal (or to change the vertical position using the vertical positioning) and increase the vertical sensitivity of the oscilloscope [15], [19]. This would effectively increase the resolution in the screen in order to make the measurement. On the other hand, now a big portion of the signal is driven out of the screen and out of the oscilloscope's dynamic range. This is a major drawback, since the accuracy of the measurement is in question.

The reason for the inaccurate measurement is that when the dynamic range is exceeded, the input amplifier of the scope is saturated causing distortions on the waveform [19]. Now the vertical system must recover from overdrive before showing any meaningful data. Thus the measurement is limited by the overdrive recovery of the oscilloscope. This situation is illustrated on *Figure 2-12*. The dynamic range of the oscilloscopes is always specified. Whereas the overdrive recovery time may not be given or may be vaguely specified as "90% recovery in 10ns".
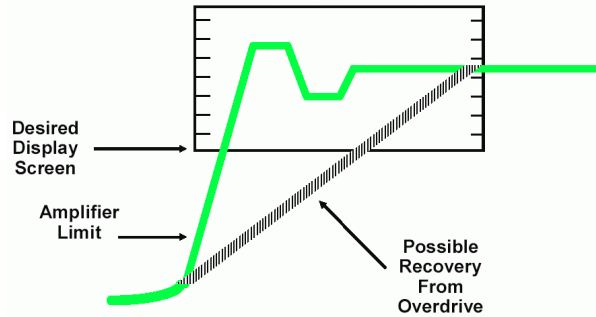
Figure 2-12: Illustration of Oscilloscope Overdrive [19]

An effective way to eliminate the overdrive problems is to use a digital storage oscilloscope (DSO) with waveform averaging [15]. The input signal should still remain within the dynamic range of the scope. After adequate number of averages is taken (i.e. no perceptible changes in the waveform), it is best to freeze the screen (i.e. to stop the data acquisition). Using the math function in the oscilloscope, now the waveform can be *digitally* magnified. The math function manipulates the saved data points of the input signal using software. Clearly the analog input circuitry of the oscilloscope is not affected by using this method; therefore, there are no signal distortions due to the scope. The main limitation on this technique though, is the vertical accuracy of the scope. But there are scopes available with 14 bits of vertical resolution (~60μV resolution for 1V$_{P-P}$). The experiment results comparing both techniques are presented on *Figure 2-13*.
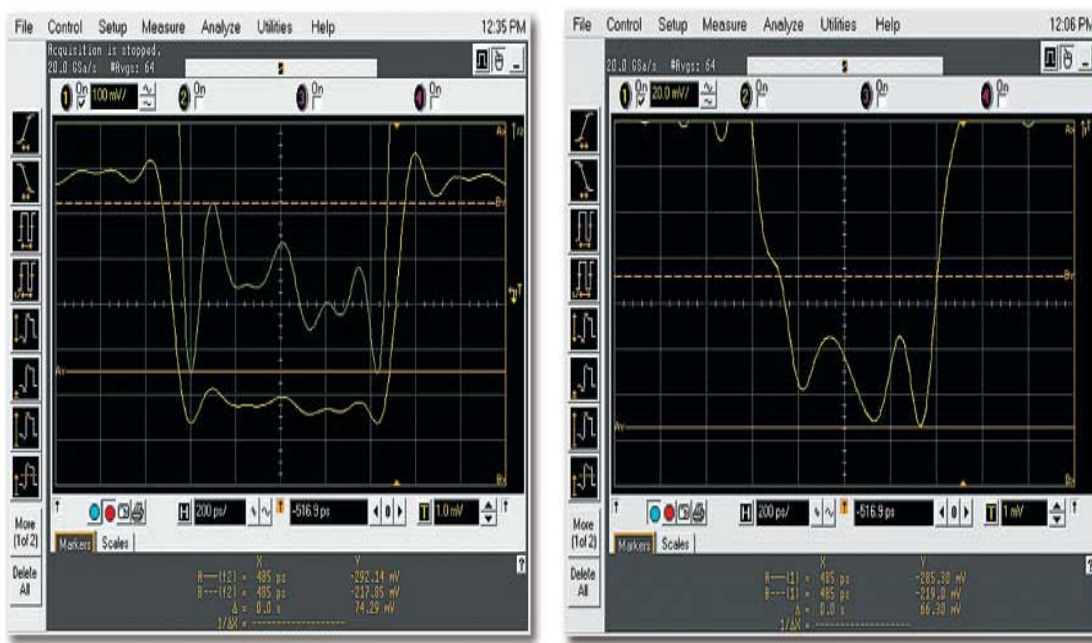
Figure 2-13: Preventing Oscilloscope Overdrive [15]

The picture on the left shows no distortion on the zoomed-in signal [15]. The input is well within the scope's dynamic range and math function is used to *amplify* the signal. On the picture to the right, the signal is clearly distorted. The waveform is driven out of the screen and the input stage of the scope is saturated. While the scope is recovering from the overdrive, it gives erroneous results.

If a DSO is not accessible, overdrive recovery performance of the available scope(s) should be determined before making ay measurements. This is to make sure that the results will not be affected by the recovery time of the scope. If it is likely to affect the measurements, then, circuits that eliminate the overdrive should be considered (such as using clamping diodes and/or switches – more on this is presented on *Chapter 3*).

3   Design Review

3.1 Introduction

In the course of this project, three different settling time measurement circuits were tested. The purpose of this chapter is to provide a detailed design analysis for each of these measurement methods. It is crucial to understand how a circuit works before making any kind of testing. After each design analysis simulation results for the corresponding circuit is provided. Explanations are helpful; however providing the simulation results facilitates the visual understanding. Therefore one would know what kind of waveform to expect during the testing.

The first technique presented is a method that heavily relies on the oscilloscope. Another method, simple and reliable, is introduced secondly. A third method, which tries to improve over the second, is presented at last. Also the printed circuit board (PCB) layouts that were fabricated are shown in order to explain a few PCB design issues.

3.2 Method #1: Depending On Oscilloscope

3.2.1 Design Analysis

The first method is a very common technique to measure settling time. Although it is not a complicated method, it has its cons. The circuit used is very simple. The amplifier on *Figure 3*-1 is usually set to gain of two. While configuring the amplifier at gain of one results in higher bandwidth, it would also decrease the stability. Therefore, any gain made from an higher bandwidth for fast settling, would have been eliminated by a less stable system.
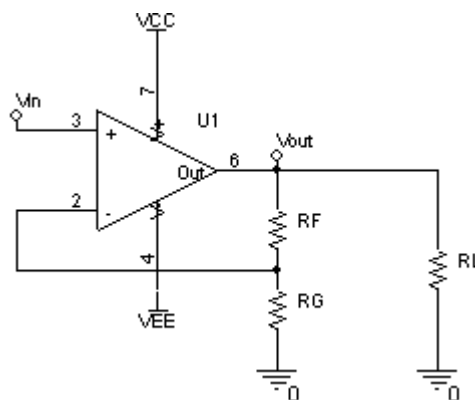

Figure 3-1: The Circuit for Method #1

To measure the settling time, first the input signal is measured, then the output. Subsequently, in order to eliminate any input imperfections, the difference between the two signals is taken; of course the input signal should be multiplied by the proper gain of the amplifier. This is usually done using the math function of the scope or by importing the signals into Excel, MATLab, etc.

The resulting signal is called the error signal, which is also referred as the settling waveform. Ideally, this waveform would start from zero volts, jump up/down during the delay and the slew period of the amplifier, and then settle back to zero volts. Afterwards the settling time is found by looking at the time when the waveform is confined within the specified error band near zero volts.

Although it seems as a very logical and simple way to measure the settling time, there are some flaws. First of all, the real world is far from ideal. The input signal will have a finite amount of slew rate. For proper measurements, its slew rate must be faster the slew rate of the amplifier. It will have it own settling characteristics. For sure, the pulse generator will not produce perfectly flat pulses. Additional to the amplifier's noise, there will be noise on the input signal, which will further limit the precision of settling.

These non-idealities can be lowered by using various ways. For example, he layout of the board is very important [1], [11]. The traces and the way the components are placed should be very compact to minimize the stray capacitances and inductances. Bypass capacitors must be placed carefully. Also using the averaging feature of oscilloscope, if available, is very helpful to get rid of some of the noise and allows a cleaner settling waveform.

Assuming all these non-idealities are taken care of, there is still one other issue that remains: The precision of settling. The settling time is measured using a large output step (preferably five volts, sometimes two volts). To prevent overdriving the scope, this large step must be confined within the screen. Therefore all the resolution of the scope is wasted on a five-volt step, even though only few milivolts of the output voltage is of interest [12], [13], [15]. With higher resolution – such as 14Bits – oscilloscopes this problem could be avoided. Even then, the resolution for a five volts step would be around 0.3mV, which is near 0.01%. Therefore it would raise a question mark on the results for that precision. Also 14Bit oscilloscopes may not be readily available everyone.

As a summary, ideally *Method #1* is a very simple and effective way to measure the settling time. In reality it has various shortcomings that would interfere with the measurement and thus result in unreliable data. Also to avoid overdriving, oscilloscope resolution is sacrificed. With this method, obtaining dependable results requires careful routing and soldering, very clean input signals, and a high performance oscilloscope.

3.2.2 Simulation Results

Spice simulations were conducted to express the design analysis visually. The circuit of *Figure 3-1* was simulated. The amplifier model used was of AD8007. The simulation results were imported to MATLab and they are shown on *Figure 3-2*. The recommended value for the feedback resistor for AD8007 is 499Ω. Therefore R_F and R_G were chosen as 499Ω. The input trace is a 2.5V step. This creates an output step of 5V. The difference between two signals is also shown on the same graph. The graph right below it is the zoomed in version of the settling waveform. Voltage excursion during the delay and the slew period should be noted.
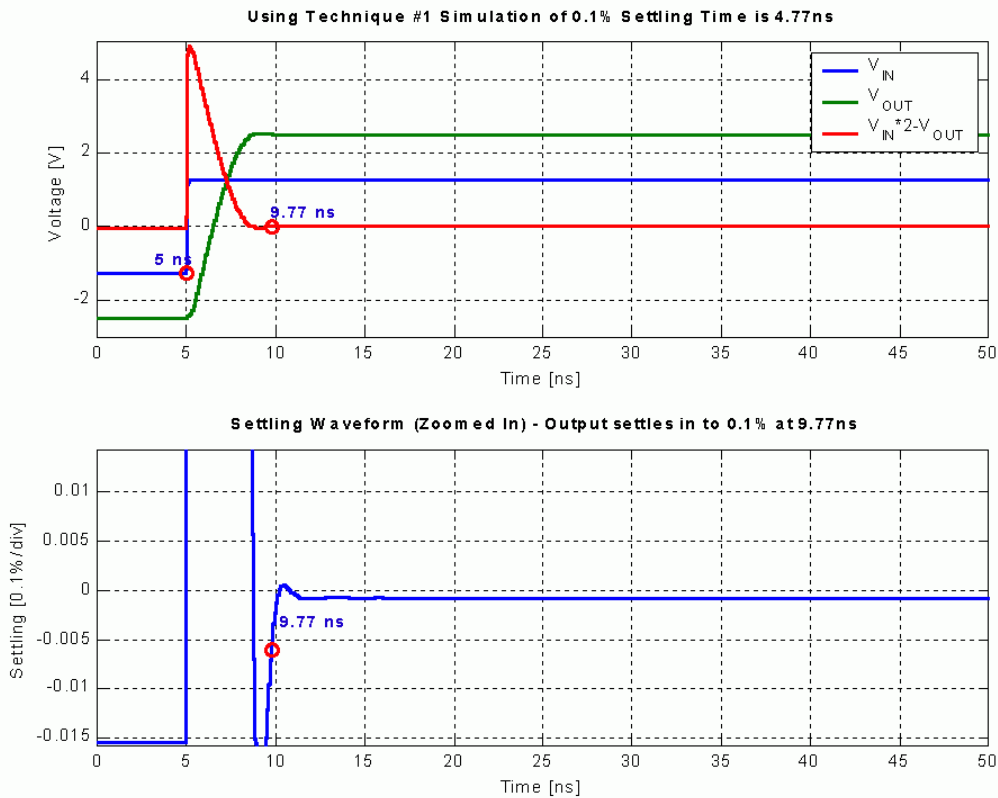

Figure 3-2: Simulation Results for the First Method

The simulation shows 0.1% settling time of 4.77ns. Of course this is an unrealistically fast settling for AD8007 but it is used to compare different measurement techniques in (near) ideal conditions. The slight offset between pre and post settling voltage indicates that the gain of the circuit was not exactly two.

3.3 Method #2: "False" Summing Node

3.3.1 Design Analysis

Observing the full dynamic range of the amplifier is essential to make sure that it is not slew rate limited by the input and that it behaves as expected. However, for settling time measurements only a very small portion of the output signal is important. Therefore any voltage excursion that occurs during delay and slewing is unwanted.

One of the ways to eliminate this is to use diodes (preferably Schottky) to clip the settling waveform [3], [6], [13]. This would not completely eliminate the problem but the voltage swing can be improved from a 5V step, down to few hundreds of milivolts. Thus the effectiveness of the scope resolution would be increased.

The second method, called the False Summing Node, incorporates a few nice features; clamping diodes is one of them. The circuit is presented on *Figure 3*-3. Now the amplifier is set to gain of −1 ($R_F = R_G$). Since it has about the same bandwidth as gain of 2, one does not settle faster than the other. One noticeable feature is that the output is referred to the input. Unlike the first method where the input and the output was measured at different times, then subtracted, now they are constantly being compared. This results in a more efficient way to eliminate the input imperfections.

The main feature of this method is the settle node created by the voltage divider created by R_1 and R_2. This node is also referred as the false summing node since it replicates the "error" at the summing (inverting) node of the amplifier owing to the bridge type of network [1], [8], [13]. This error signal is crucial for settling time measurement. It directly relates to the output signal. The measurement is made on the settle node. However due to the voltage divider, the signal on this node is the half of the signal of interest. Therefore the attenuation factor should be compensated for.
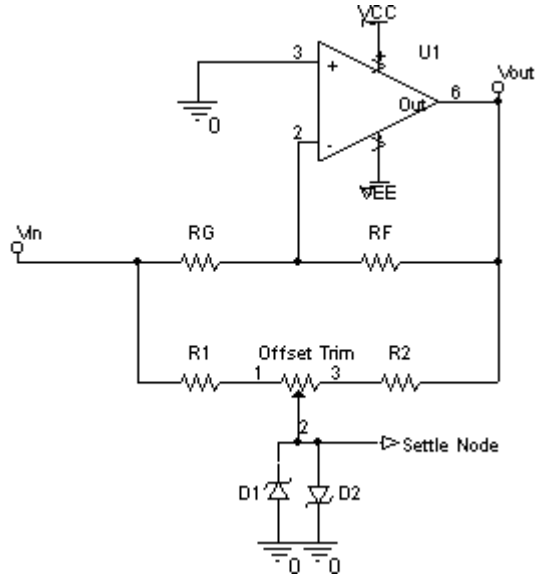
Figure 3-3: Method #2 - False Summing Node

For the most reliable results, again, pre and post settling voltages should be same. A potentiometer is added to the settling node in order to trim off any offset that there might be. As previously discussed, clamping diodes are used on the settling node in order to prevent any unwanted voltage excursions. This is a great advantage as it increases effectiveness of the scope resolution, and thus more precise measurements can be made. The downside of using these diodes is that extra capacitance is added to this crucial node. This may cause some delay and extend the settling time. Modern schottky diodes minimize this problem with very low junction capacitances (such as 0.2pF). Therefore they might as well be considered as a PCB layout parasitics.

The second technique is a definitive improvement over the first. Now the input and the output are constantly compared. Settling measurement is taken from the false summing node, however attenuation due to the voltage divider should not be forgotten. Addition of clamping diodes improves over the extreme voltage swing; attention should be paid when choosing the diodes. With the addition of the tricks that were explained on *Section 3.2.1*, very accurate and fast settling time measurement is possible using this method.

3.3.2 Simulation Results

Simulation for 0.1% was accomplished using Spice and, again, the results are analyzed in MATLab. The graph on *Figure 3-4* shows the measurement results.

Using Technique #2 Simulation of 0.1% Settling Time is 4.98ns

V_{IN}
V_{OUT}
Settle Node*2

9.98 ns

5 ns

Voltage [V]

Time [ns]

Settle Node x 2 (Zoomed In) - Output settles in to 0.1% at 9.98ns

9.98 ns

Settling [0.1%/div]

Time [ns]
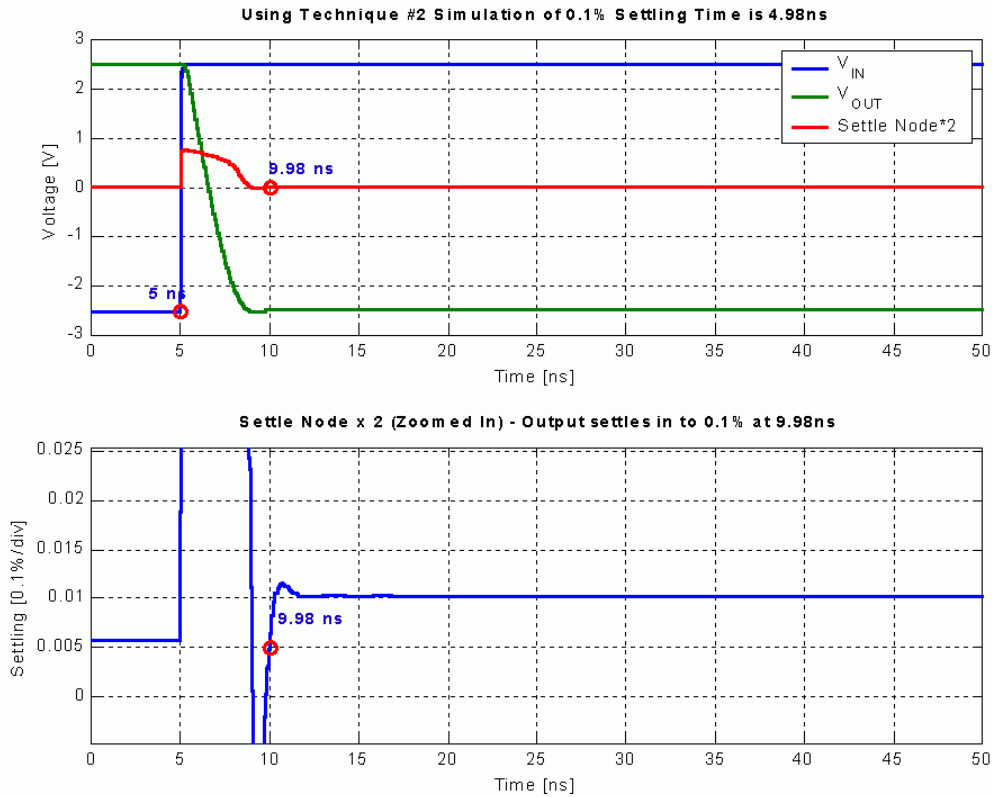
Figure 3-4: Simulation Results for the "False Summing Node" Method

A very fast input pulse is applied and the output drops at its maximum slew rate. During this period maximum voltage excursion is 0.4V at the settle node. In the graph the attenuation factor was compensated for accurate measurement results.

The graph right below the one that shows the full dynamic range is the zoomed in version of the settling signal. The amplifier settles within 0.1% at 9.98ns. Since the input pulse is applied at 5ns, this gives 0.1% settling time of 4.98ns, which is 210ps slower than the previous method. This was expected due to the reasons that were described previously.

3.4 Method #3: Input and Output Switching

3.4.1 Block Diagram of the Design

The last technique, although it seems complicated, it tries to improve over the false summing node circuit. The design includes various stages and it is best to show a block diagram before delving into any details. The block diagram is shown on *Figure 3-*

5. The circuit was designed by Jim Williams. A design similar to this was first appeared on *Linear Technology Application Note #10* on 1985. Then that design was revised and this one was included in *Linear Technology Application Note #79* on September of 1999. A month later this method was published in *EDN Magazine* as a Design Feature.
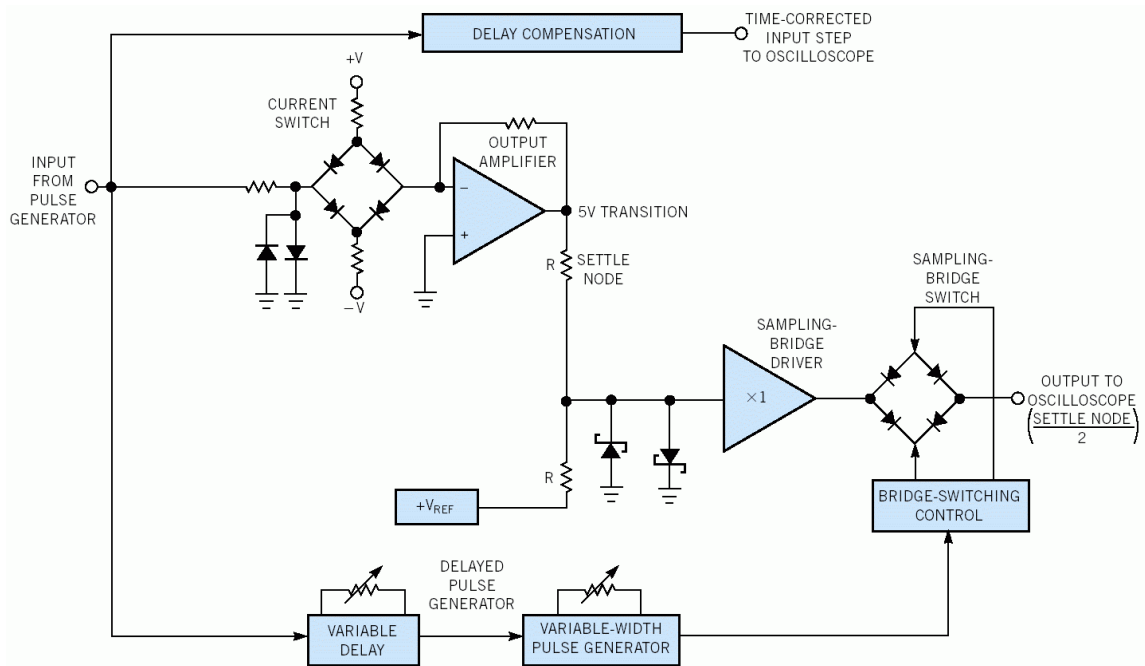
Figure 3-5: Block Diagram of Method #3: Input/Output Switching [12]

The false summing node circuit is clearly visible in the middle of the diagram. However, now the input pulse is not directly fed to the inverting input of the DUT. Rather, the input pulse is connected to a diode bridge, which controls the current flow to the inverting node of the amplifier. The amount of the current flow is adjusted such that a 5V step is obtained in the output of the DUT. This first improvement is a very efficient way to create an output pulse as it greatly improves the independence on the input pulse characteristics. Current switching allows a very fast and clean output signal.

Of course since now the output and the input are not related, output of the DUT cannot be referenced to the input signal. Rather, it is referenced to V_{REF}, which is chosen such that when the output settles, the settle node is actually at 0V. Also, settling node is clamped with Schottky diodes.

A second improvement is the added output switch. It was previously mentioned that when using the second method, the voltage excursion is improved to few hundreds of miliviolts from a 5V step. Now with the use of an output switch this voltage excursion

can be further limited in order to allow even smaller amounts of voltage to be displayed. This becomes important especially for low-resolution and analog scopes. The bridge switching control pulse is conditioned such that the output switch does not turn on until the amplifier settles within the desired voltage. Technically speaking it could be few tens of milivolts.

Unfortunately there is a downside of adding an output switch to the circuit: Switching transients. Parasitic bridge outputs can be greatly improved by using monolithic bridge diodes first of all. This way the capacitive imbalance of the diodes is minimized. Also the drift can nearly be eliminated. To further improve the switching transients, or if the monolithic bridge diodes are not available (hard to find nowadays), the circuit, which is presented on *Figure 3-6*, can be added to the design.
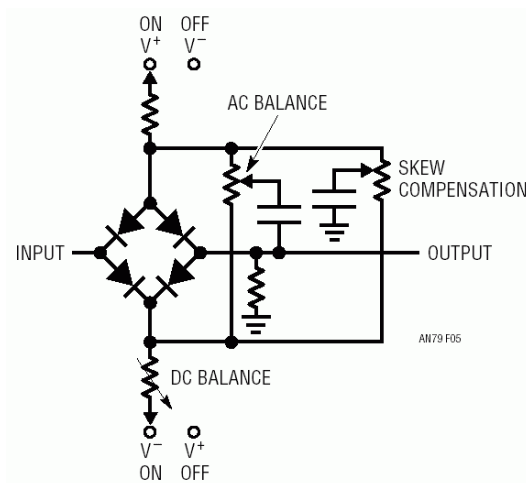
Figure 3-6: Minimizing Switching Transients [13]

DC balance is necessary to eliminate any pre and post switching offset in the output. AC balance is added to lower capacitive imbalances. Finally skew compensation takes care off any timing asymmetry in the bridge drive circuitry. Also, looking back at *Figure 3-5* there is one added precaution between the settle node and the output switch: A buffer. Removing this buffer is out of question because it prevents any interference from the output switch to the settle node. This buffer should be the same model as the DUT. Since the input signal to the second DUT is very small, its settling characteristics does not interfere much with the measurement results. Although a slight extension of settling is inevitable.

The last block to be discussed is the delay compensation. Additional to the delay caused by the DUT, which should be included in the settling time, there are other components that introduce further delay. If the measurement is made directly from the start of the input pulse, without compensating these extra delays, the results will be faulty. These delays are as follows:

- Input Step to DUT Input
- DUT output to Settle Node
- Settle Node to Buffer Output
- Buffer Output to Bridge Output

Delay compensation block is adjusted to create a time-corrected input step, which includes all extra delays added by the test circuit, in order to obtain meaningful results.

In the next sections a more detailed circuit that closely follows the block diagram is explained. The circuit is divided into two parts, each focusing on the improvements over the second technique.

3.4.2 Improved False Summing Node

This block by itself could be used to measure settling time. However, the efficiencies of the second technique were already proven. Therefore whole design was built for an investigation of another method. *Figure 3-7* shows a detailed circuit for the new false summing node.
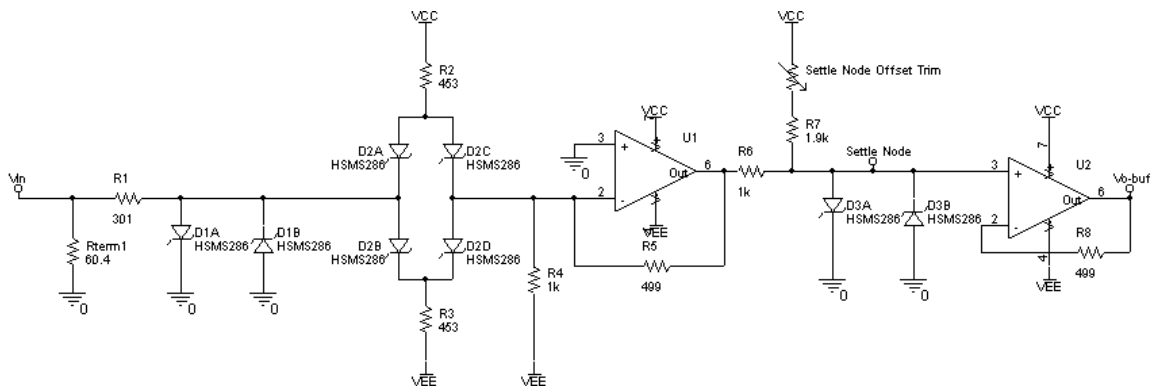

Figure 3-7: The New False Summing Node Circuit

This circuit is very similar to that of *Figure 3-3* with the addition of input diode bridge and the V_{REF} is set to V_{CC}. Rails are set to ±5V. Without any input pulse the bridge is balanced and there is about 10mA of bias current flowing through it. For now D_{1A} and

D_{1B} are off since the bridge input is at 0V. The bridge output is held at *virtual ground* by the amplifier. R_4 constantly pulls 5mA from the inverting node of the amplifier. This means that the output of the amplifier is held at 2.5V when the input is low.

When the input pulse goes high, input of the diode bridge is clamped and the bridge balance is disturbed. Since the input voltage increases, D_{2A} shuts off and D_{2B} takes all the input current and dumps it off through R_3. Now the top of R_3 rises and this phenomenon shuts off D_{2D}, since the output of the bridge is still *virtually grounded*. There remains one diode, D_{2C}, which is still on. Therefore all the bias current flowing through R_2 is carried to the summing node by D_{2C}^*. R_4 is still pulling 5mA. That leaves 5mA, which flows through the feedback resistor, R_5, to pull the output down to –2.5V. This creates a nice and clean output pulse. The input pulse acts as a trigger voltage rather than an imperfect input voltage to be followed. Thus the dependence on the input signal characteristics is eliminated.

The next goal is to set the settle node to 0V when the DUT transitions to –2.5V. One thing to do could be to make V_{REF} = 2.5V and use $R_6 = R_7$ just as before. But this would require a voltage regulator. Instead of that, the reference voltage is set to V_{CC}, which is readily available, and the resistor ratio of R_7 / R_6 is changed to 2. Another advantage of doing this is that now the attenuation of the circuit is decreased to 3/2 = 1.5 from of 2. Settle node is again clamped by Schottky diodes and connected to the output switch by the buffer. The diodes used throughout the design are HSMS286s, which have low forward voltage drop ($V_R \approx 0.35V$) and have a zero bias junction capacitance of C_{jo} = 0.2pF.

3.4.3 Output Switching

3.4.3.1 Simplified Schematic

To avoid confusion, a simplified schematic of the output switch is shown on *Figure 3-8*. Next section introduces a detailed version of this schematic.

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* The reason the diodes are named D_{2ABCD} is because although they are not monolithic, they are contained in one package.
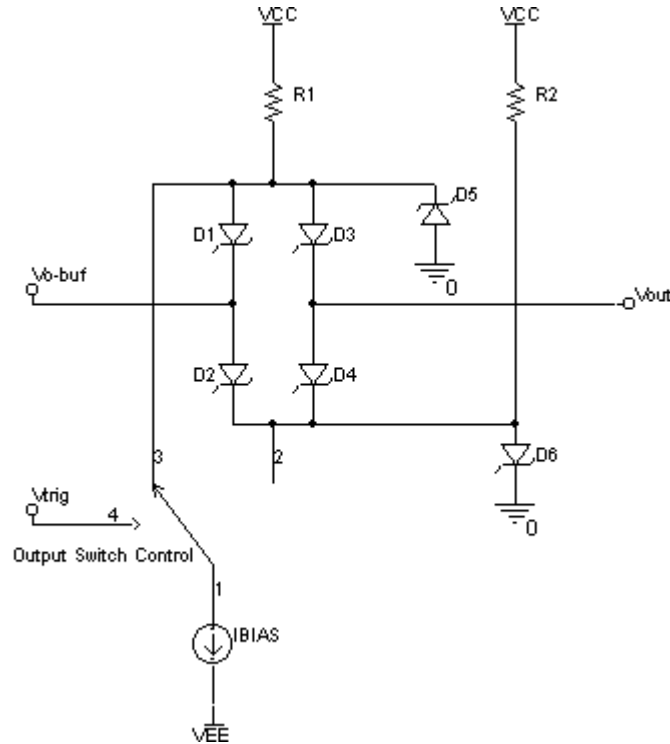
Figure 3-8: Simplified Output Switching Circuitry

The same diode bridge of *Figure 3-7* is used at the output. Now, however, it functions differently. When V_{Trig} is high, the output switch control is at its current position. Bias current flows through R_1, and pulls the voltage at the top of the bridge below 0V to keep D_1 and D_3 off. This node is clamped by D_5 to prevent any extreme reverse bias voltages in order to attain a faster bridge response. With no current flow through D_2 and D_4 bottom of the bridge is clamped to a voltage above 0V by forward biased D_6. The top of the bridge being at $-V_F$ and the bottom at $+V_F$, the diodes are off, hence the switch is off and the output is disconnected from the input.

On the other hand, when V_{Trig} goes low, the output switch control changes its position. This forces the bias current to pulled first through R_2, reducing the voltage at the bottom of R_2. This reverse biases D_6 and the voltage continues to fall down until D_2 and D_4 are forward biased and the node is clamped. Meanwhile, since the current through R_1 is reduced (it is shared with R_2), the voltage at the top of the bridge increases until D_1 and D_3 are forward biased and D_5 is turned off. Now that all the diodes are on, the switch is on and the bridge is balanced (meaning that with 0V input voltage $V_{out} = 0V$). Since the

output of the bridge is floating in this condition (i.e. it is not held constant by anything), any input disturbance will be reflected to the output.

3.4.3.2 Detailed Schematic

Since the functioning of the output switch is now clear, a more detailed version of the switching circuitry is shown on *Figure 3-9*. The top half of the schematic is the diode bridge that was explained above. Bottom half of the circuit is used to create the bias current and the control step, V_{Trig}.

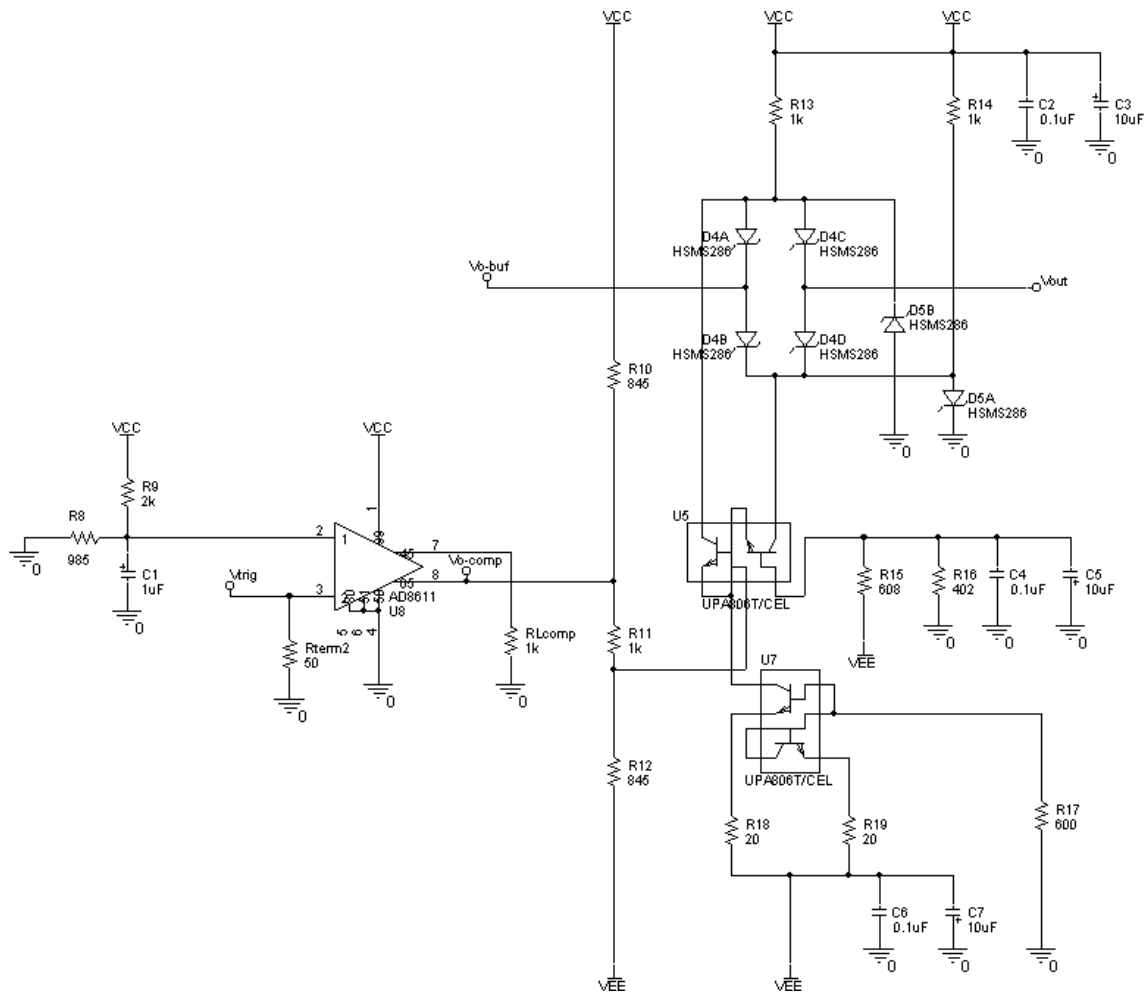**Figure 3-9: Full Schematic of the Output Switch**

The transistors of U_5 form a differential pair. This pair is used as a differential switch, which means that only one of them is on at any given time. The transistors that were used are UPA806Ts. These are RF transistors and have an f_T of 12GHz, which is highest at I_C = 10mA. Therefore the current mirror created by another package of

UPA806Ts is biased such that it creates a bias current of 10mA, which ultimately resulted in $R_{13} = R_{14} = 1k\Omega$ for proper bridge biasing. Of course to prevent any offset voltage between pre and post switching, this bias current had to be trimmable. R_{17} is actually a resistor in series with a potentiometer. This allows trimming of the bridge DC offset.

The *Variable Delay* and the *Variable Width Pulse Generator* on *Figure 3-5* was first implemented on the first PCB design. These were basically two comparators. One of them was connected to the output of a low pass filter in order to create delay by changing f_C of the filter, and thus the rise time of input pulse. The output of that comparator was connected to a high pass filter (with variable f_C) in order to adjust the sample window width. The output of the high pass filter was connected to the second comparator, which ultimately created the differential switch control pulse. However, the pulse generator used for the task (HP3133A) had a second output (independent of the first one) with adjustable pulse width and delay. Therefore on the second PCB design this unnecessary portion was replaced with a single comparator. Even though the comparator's rise time (~4ns) was slower than that of the generator, it was used because it greatly facilitated routing of the PCB.

The comparator used is an AD8611. It has an output voltage swing from 0.5V to 3.4V. Although it may not be a large step, it is more than enough to enable differential switching. These swing values set the values for $R_{10,11,12,15,16}$ for proper bias point of the differential switch. $R_{10,11,12}$ were set such that the symmetrical operation of the output stage of the comparator was obtained (i.e. sink/source same amount of current) in order to achieve the maximum output swing.

3.4.4 Simulation Results

It is now clear how the circuit functions. Therefore the simulations can be better understood. The circuits on *Figures 3-7* and *3-9* were joined together to conduct the simulations. The results are provided on *Figure 3-10*. The graph on the top shows the waveforms at important nodes of the circuit. These are the DUT output, the output switch trigger, the buffer output, and the bridge output. The graph on the bottom is the amplified bridge output by the attenuation factor of 1.5.

Delay factors that were presented on *Section 3.4.1* were eliminated using a different method instead of creating a time corrected input step. The measurement starts right before the DUT output transitions. This eliminates the delay from Input Step to DUT Input and the delay of the DUT, which actually should not be eliminated. Since the buffer used on the circuit is the same model as the DUT, it has the same amount of delay. Therefore it is perfectly legitimate to start the measurement right before the output transitions.

That leaves two more delay routes. Once the output bridge is on, it has practically no effect on delay because the voltage change and the diode capacitances are very small. Spice reports a delay of 7ps, which is not a practical value to measure. Also any measurement result would be unreliable for a timing amount of this small, since, once the probe is placed on the circuit, the circuit does not behave the same way anymore due to the added parasitics by the probe.

The last delay is from DUT output to the settle node. The reasons for this delay were discussed in *Section 3.3.1*. It is also a small amount of delay (few hundreds of picoseconds maximum with the diodes used in this design) and therefore it can be left in the measurement path. *However*, the tester *should* check this delay while making the measurement to *make sure* that it is not greatly affecting the measurement. If it is then it should be compensated for.

Other than the delay issue, there is also the attenuation of the false summing node. The top graph on *Figure 3-10* shows that the bridge output settles within 0.1% in 9.98ns – 5.22ns = 4.76ns. However this number is not correct since the attenuation factor is not added. The graph on the bottom is the amplitude corrected signal. It shows a 0.1% settling time of 11.5ns – 5.22ns = 6.28ns.
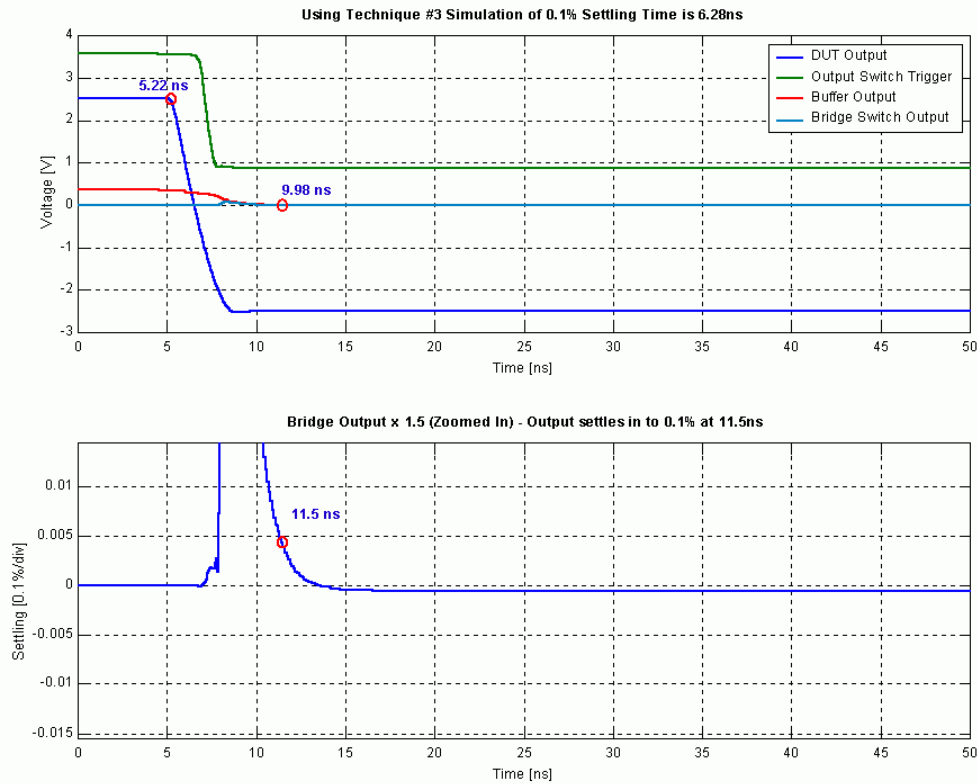
Figure 3-10: Simulation Results for the 3rd Method

With ideal input conditions, the last method shows an extension of 0.1% settling time of 1.3ns over the second method. As anticipated in *Section 3.4.1*, this is primarily due to the added buffer. Although the signal it sees is very small compared the real DUT, its settling characteristics are not completely eliminated. This might look like a disadvantage but at least the tester will know the amplifier can actually settle a nanosecond or two faster than the measurement result. It gives a margin for error. It is better to be safe than telling the customer that amplifier can settle in certain amount of time and later finding out that the actual settling time is a nanosecond or two slower.

3.5 Printed Circuit Board Layout

3.5.1 1st Design

It was proven that the PCB design plays a crucial role on settling time measurement on two of the PCBs that were built. The first board is presented on *Figures 3-11* and *3-12*, which are the top and the bottom layers respectively.
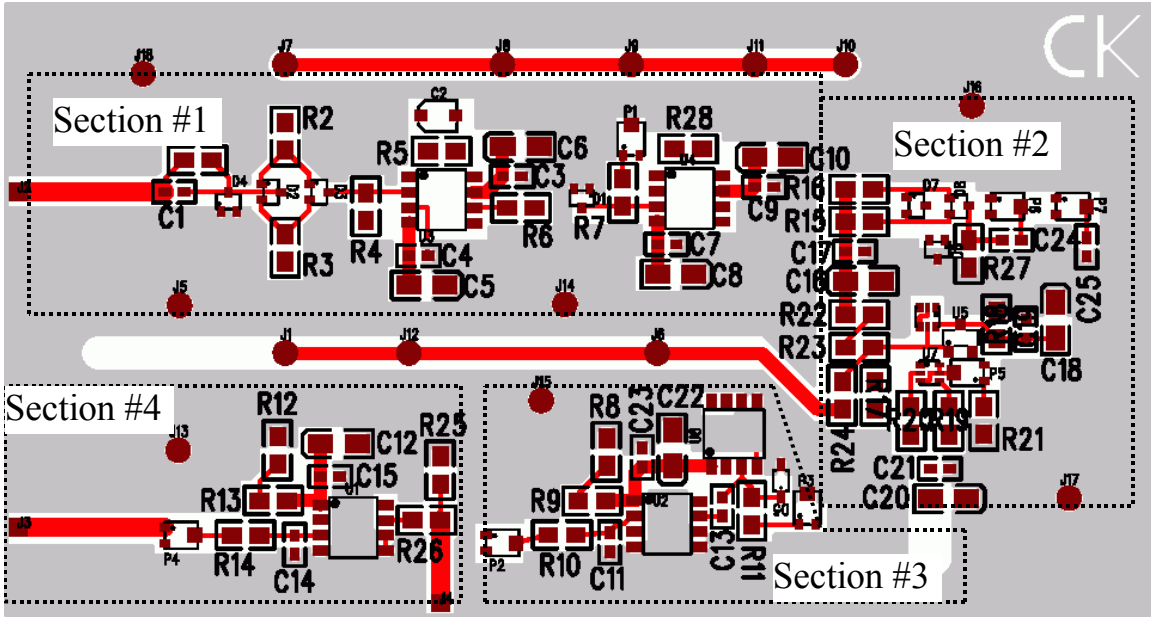
Figure 3-11: First PCB Layout (Top Layer)
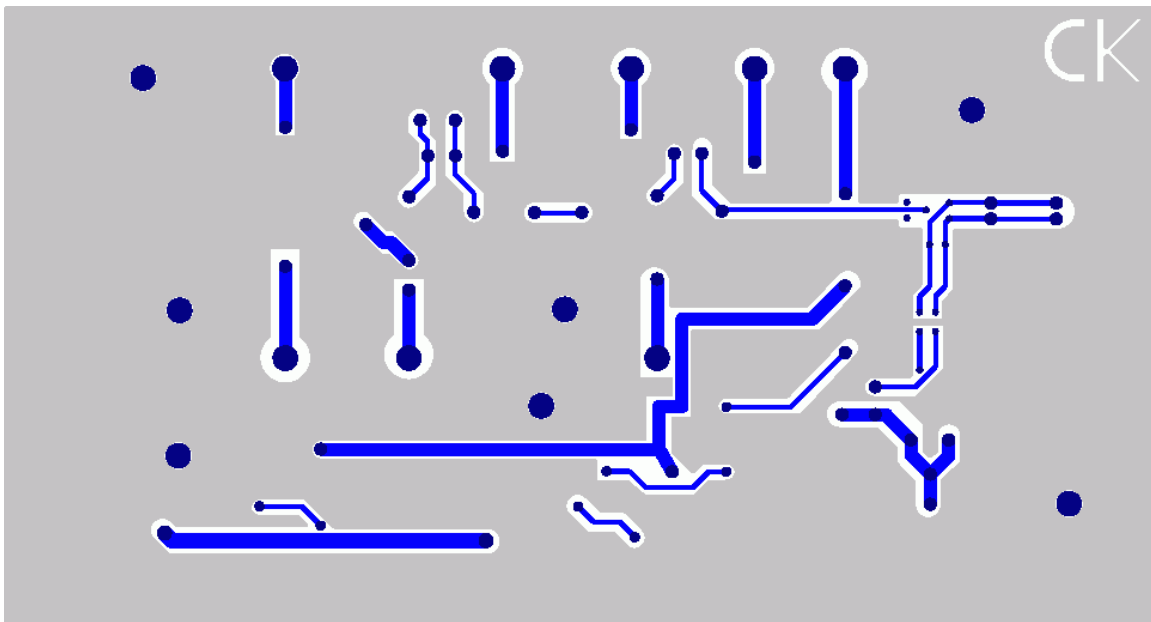
Figure 3-12: First PCB Layout (Bottom Layer)

The board is 4"×2"×0.62". It has all blocks that are on *Figure 3-5*. The top layer is divided into four different sections. Section #1 is the improved false summing node. Section #2 is the output switch. Section #3 is the delay and the variable pulse width generator. Finally Section #4 is the circuit to create the time corrected input step.

The board does not have a middle ground layer because by doing so the production time and cost were greatly reduced. However, the routing on the bottom layer

was minimized so that it behaves as a pure ground plane. Also to avoid any parasitics to board was built as compact as possible. The ground plane was kept as clean as possible to minimize noise problems. Therefore the trigger circuitry and the settling measurement circuits were separated as much as possible. Also positioning of the bypass capacitors was important.

This PCB worked very well and allowed measurement accuracies of 0.1% and 0.01%. However there was a very short ringing at DUT output. Although it did not extend the settling time of the amplifier, the cause for it was investigated and linked to board parasitics. Therefore a second board was built with a more compact design.

3.5.2 2nd Design

The layout of the second design is shown on *Figures 3-13* and *3-14*.
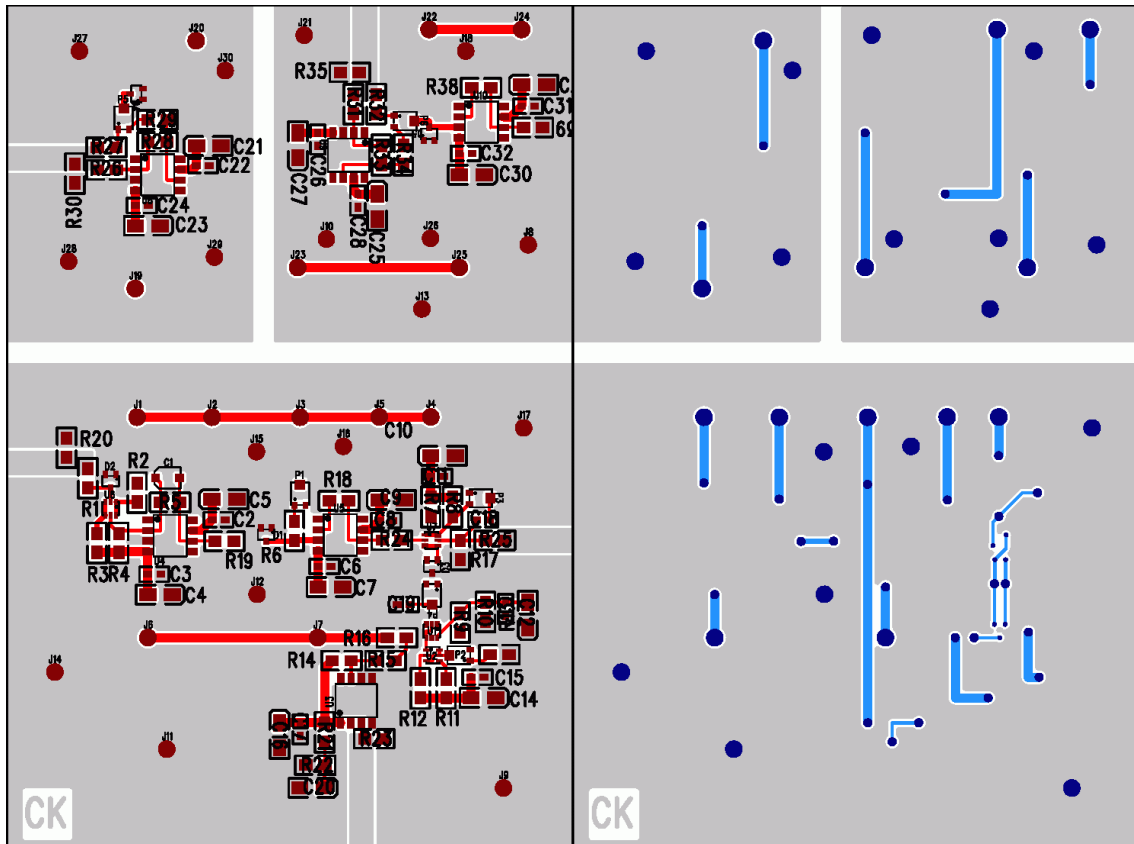

Figure 3-13: Second PCB Layout (Top Layer)   **Figure 3-14: Second PCB Layout (Bottom Layer)**

The size of the board is 2.5"×4"×0.62". Although it is larger than the first board, it has three separated test circuits on it. The top left corner is the second method. Right next to it is the second method with a buffer added to the settle node. Nevertheless this

buffer proved to be unnecessary and the circuit was not used. The circuit below these two is the third method with an even more compact input stage.

The circuit for the second method is very compact and has a ground plane underneath. This compact design resulted in very clean settling waveforms. Of course with better dielectric, parasitics can be further reduced. For the third method, the routing on the bottom layer of the second board was further reduced to achieve a larger ground area. Furthermore the delay and the variable pulse width generator and the time corrected input step generator was removed from the layout.

Creating a more compact input stage removed all the parasitic induced ringing from the output of the DUT. Changes made to the layout on Sections #1, #3, and #4 forced a change on the layout of the output switch. During the testing, it was seen that there was an oscillation on the output whenever the output switch was turned on. Investigations of this phenomenon related the cause to trace inductances on the differential current switching path. These parasitics investigations, although they took time, showed how vulnerable the circuit was to the slightest amount of non-idealities on the board, especially at high speeds. Due to the time constraints a third board was not built.

Once again, PCB layout is very crucial. The design should be as compact as possible. Grounding is very important. Bypass capacitors should be placed very carefully. Current return paths on the ground should be considered. Using shielding over the board could make the measurements more complicated than already are but it will add a degree of improvement on the way to a clearer measurement.

4 Measurement Results

4.1 Introduction

After comparing all three designs in near ideal conditions (i.e. simulations), next task was to start bench measurements. PCBs were ordered, along with the required components. Next, three amplifier models were chosen. These were AD8000, AD8007, and AD8045. AD8000 and AD8007 are current feedback op-amps. AD8045 is a voltage feedback. Their bandwidths are 1.5GHz, 650MHz, and 1GHz respectively. The reason AD8007 was chosen is because it is a low-noise, ultralow-distortion op-amp and its 0.01% settling time was specified in the datasheet. Therefore it was suitable for 0.01% settling time measurements. It has a slew rate of 1V/ns. According to the datasheet its 0.1% and 0.01% settling times are 18ns and 35ns respectively.

AD8000 is the newest high speed op-amp that Analog Devices, Inc has designed. It has a very high slew rate (4.1V/ns) and a 0.1% settling time of 12ns[*]. This amplifier was chosen due to its high speed settling feature and it is a new amplifier. AD8045 was also tested primarily because it is a voltage feedback op-amp. It also has high bandwidth and very fast settling characteristics (7.5ns to 0.1%). Its slew rate is 1.3V/ns. Both, AD8000 and AD8045, are not specified to 0.01% settling.

Lab equipment is also important for reliable results. The pulse generator used was a HP3133A. It is a 3GHz generator with a 50% rise time of ~60ps. It has two independent channels with complementary outputs on each channel. This proved to be very useful especially for the third method. The oscilloscope was a Tektronix TDS8000, which is a high performance scope with 14Bit resolution and 20GHz bandwidth. Since the connection to oscilloscope using long coax cables was out of question, active probes were used to take the measurements. They had an impedance of 1MΩ and a capacitance less than 1pF. The downside of using active probes, however, is the 10X attenuation.

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[*] First it was measured as 8ns by Andy Wheeler, later on, it was specified as 12ns in the datasheet in order to add a safety margin.

4.2 Results for Method #1

In simulations, the first method proved to be the fastest and the easiest method with no *extra* components added to the circuit, which is ideal. This is hardly the case when it comes down to the bench. Due to parasitics and non-ideal input pulse, it is really hard to obtain proper measurement results. It is certainly not impossible, although routing, component placement, bypass scheme, probe grounding, etc. are really important and it takes time to find the optimal configuration.

The measurement results are shown for each of the amplifiers on *Figures 4-1*, *4-2*, and *4-3*. Since AD8007 has a 0.01% specification, the measurement results for that precision are shown on *Figure 4-4*.
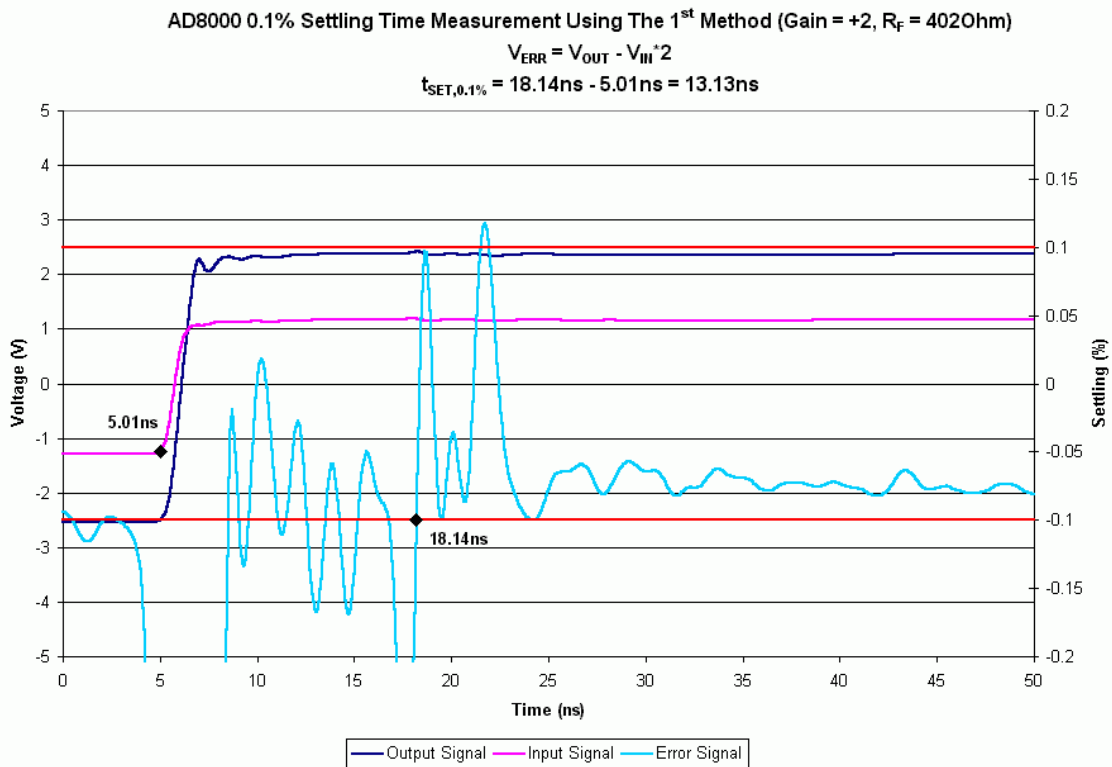

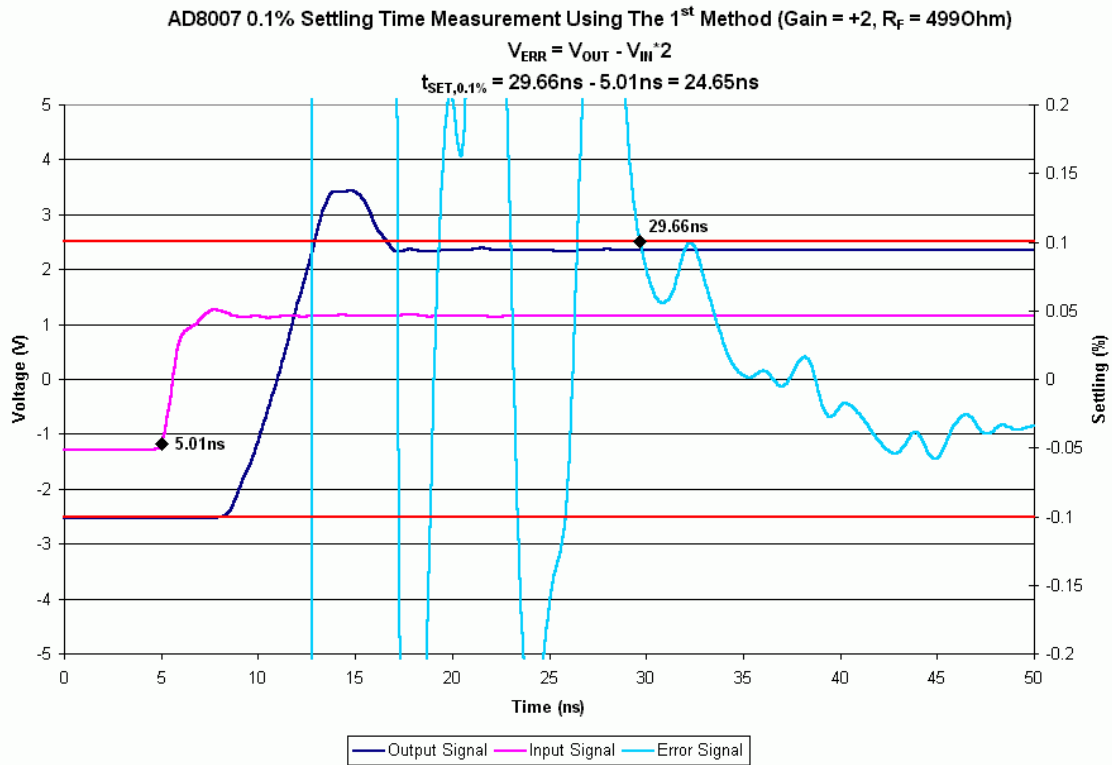**Figure 4-1: AD8000 0.1% Settling Measurement Using The First Method**

Figure 4-2: AD8007 0.1% Settling Measurement Using The First Method
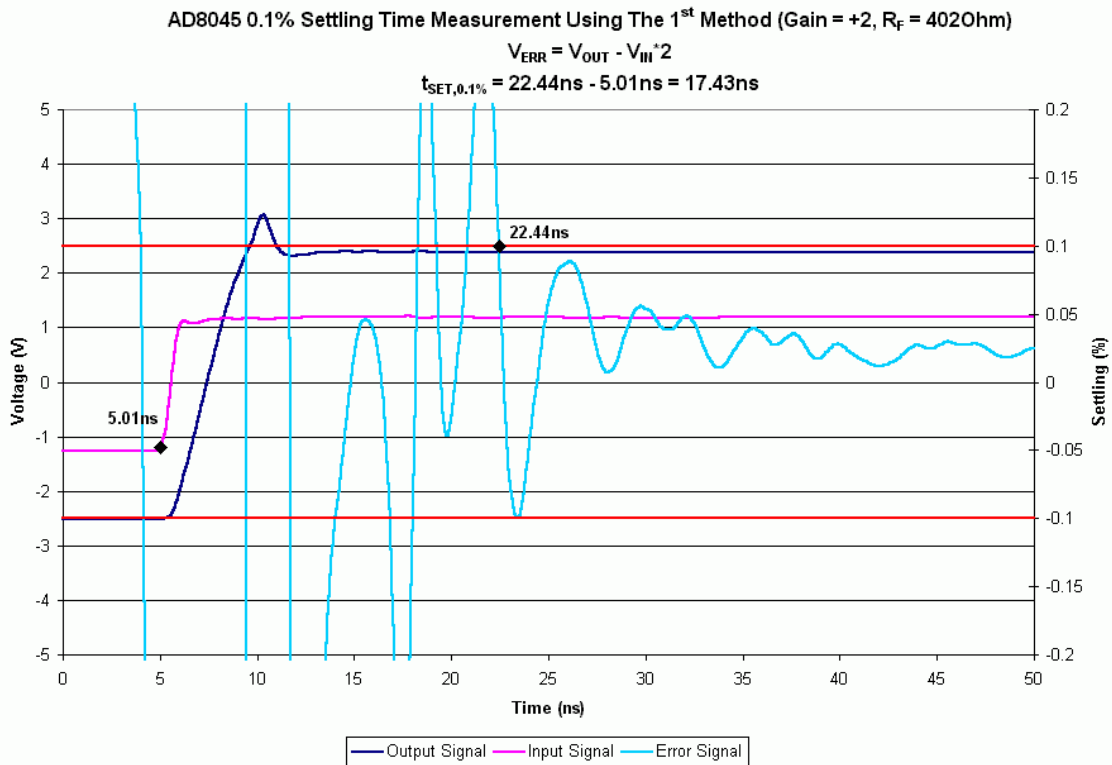

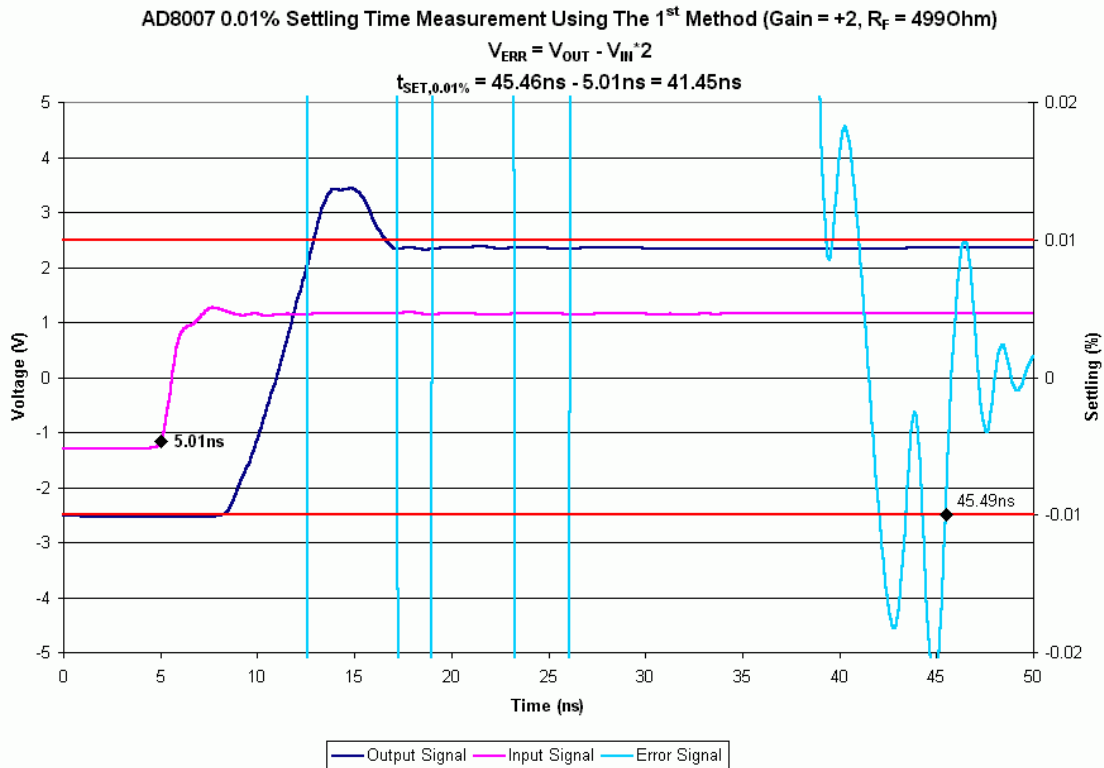**Figure 4-3: AD8045 0.1% Settling Measurement Using The First Method**

Figure 4-4: AD8007 0.01% Settling Measurement Using The First Method

The board, which was used to do these measurements, was an AD8000 test board. AD8045 also has the same pinout configuration; therefore this board suited it very well. On the other hand AD8007 had a slightly different configuration. Therefore the board had to be altered, which is hardly ideal while doing settling time measurements – especially for this method. Also the severe reflection on the board should be noted (2 spikes near 20ns), which definitely extended the settling.

All the measurement results did not correlate to the datasheet. They are off the pace by few seconds. It is possible to obtain better results; however, the goal was to prove that how easy it would be to obtain faulty results using this technique. For reliable results, a lot of time must be spent on improving the board setup.

4.3 Results for Method #2

The circuit for the second method was custom built. It was made as compact as possible to minimize parasitics, particularly near the settle node. This resulted in very clean settling waveforms, although some small reflections were still present on the board. The results for each amplifier are presented on *Figures 4-5*, *4-6*, *4-7,* and *4-8*.
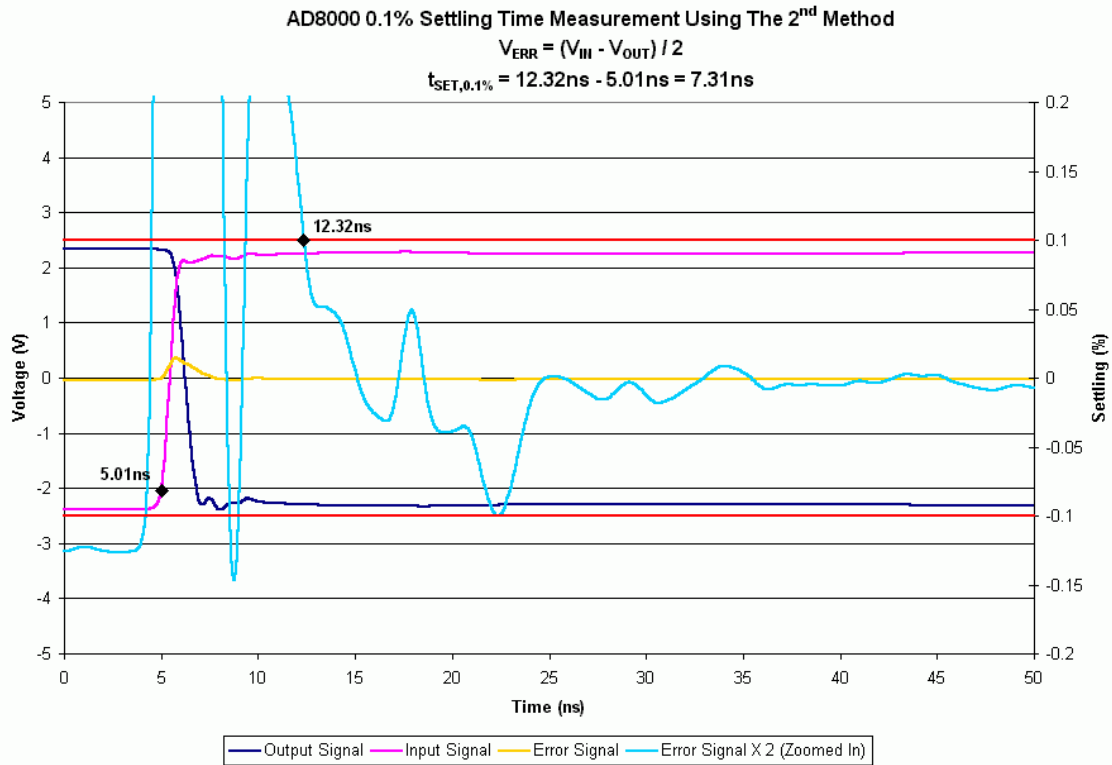
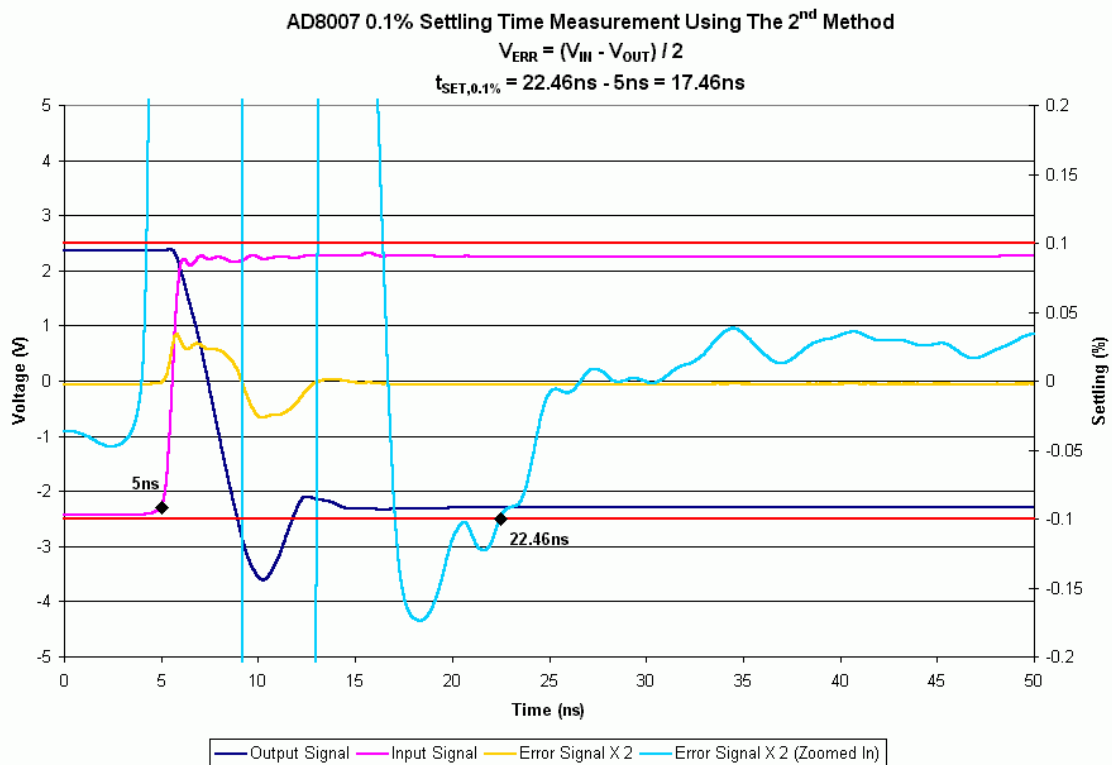**Figure 4-5: AD8000 0.1% Settling Measurement Using The Second Method**

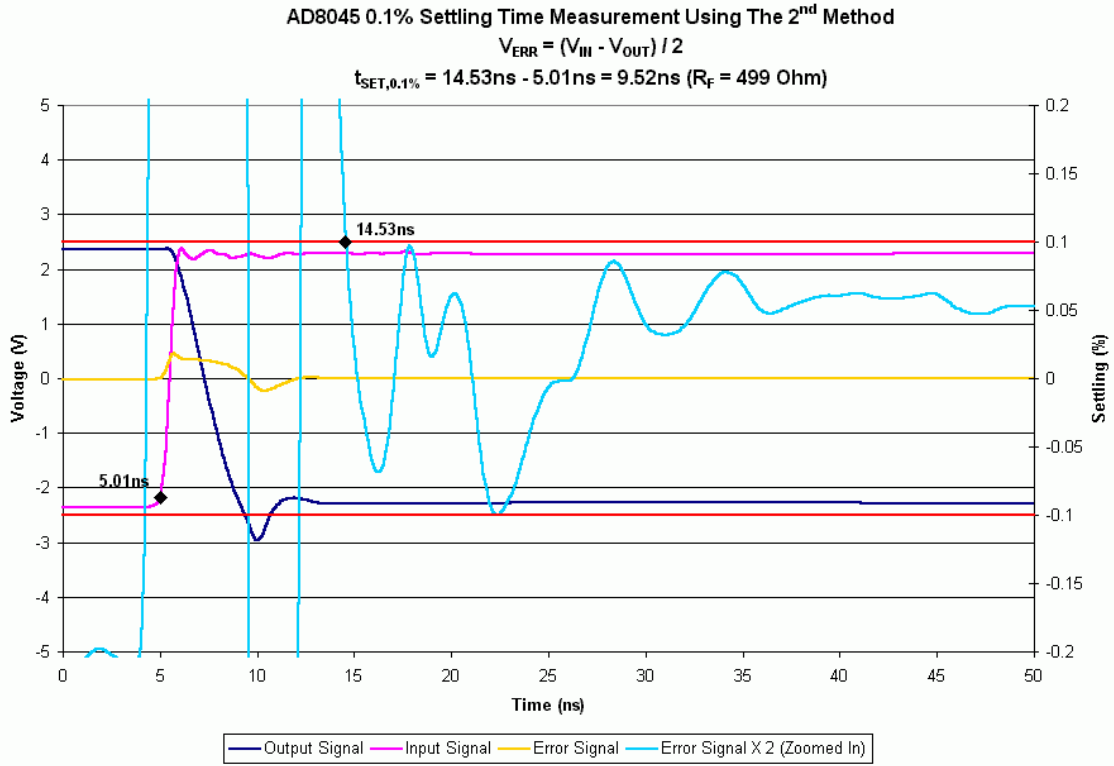**Figure 4-6: AD8007 0.1% Settling Measurement Using The Second Method**

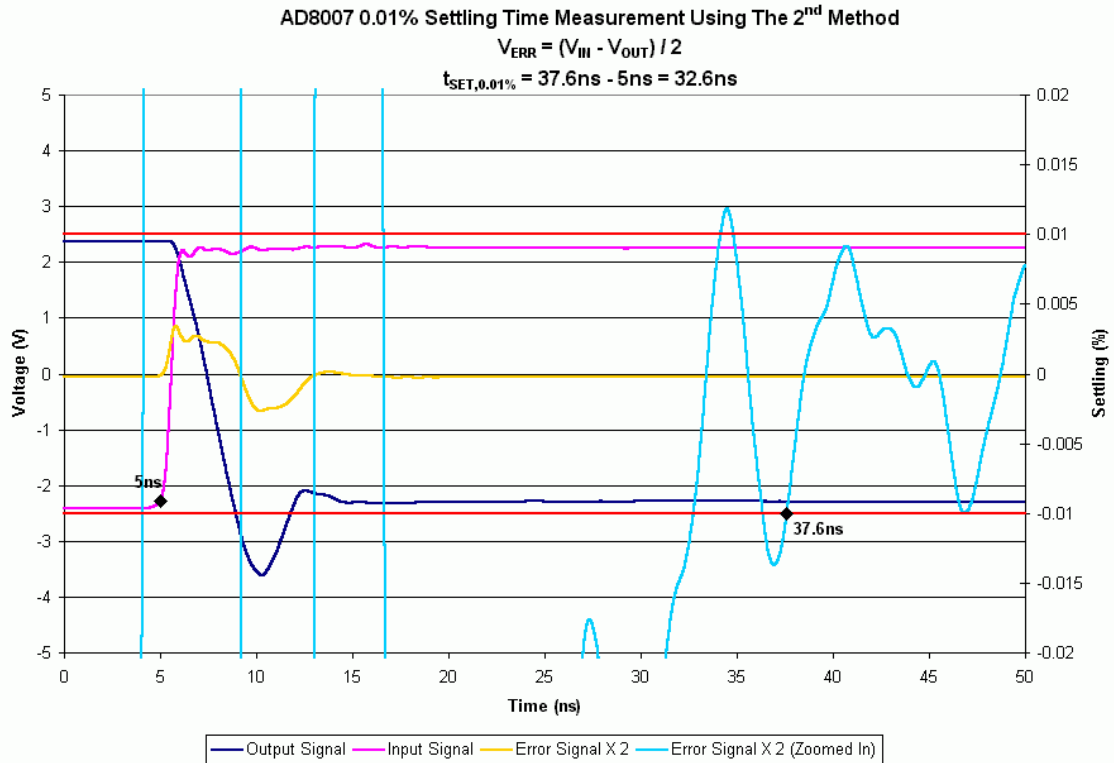**Figure 4-7: AD8045 0.1% Settling Measurement Using The Second Method**

Figure 4-8: AD8007 0.01% Settling Measurement Using The Second Method

On the second technique the results improved a lot and correlated with the datasheet. Note that AD8045 0.1% settling is shown as 9.5ns, whereas the datasheet indicates it is 7.5ns. The reason for this, when the measurement was made, the feedback resistor was chosen as 499Ω. In the datasheet, the optimal value for this resistor is given as 100Ω. Using a 5× higher feedback resistor value decreases the bandwidth of an already stable system. Therefore an extension of settling time is expected. In this case it is 2ns, which is an acceptable extension and can be improved with lower feedback resistor.

4.4 Results for Method #3

The PCB layout of this circuit is complicated. It is a very challenging task to minimize parasitics when the routing gets very confusing. This caused a number of problems during the testing. The first layout had few problems, fixing those resulted in others. These are discussed on the next section. These issues forced the testing of the third technique to be limited to AD8007 only, due to its lower bandwidth. Fortunately the first board allowed 0.1% and 0.01% measurements for AD8007. The results are shown on *Figures 4-9* and *4-10*. They correlate to the datasheet and to the previous technique.
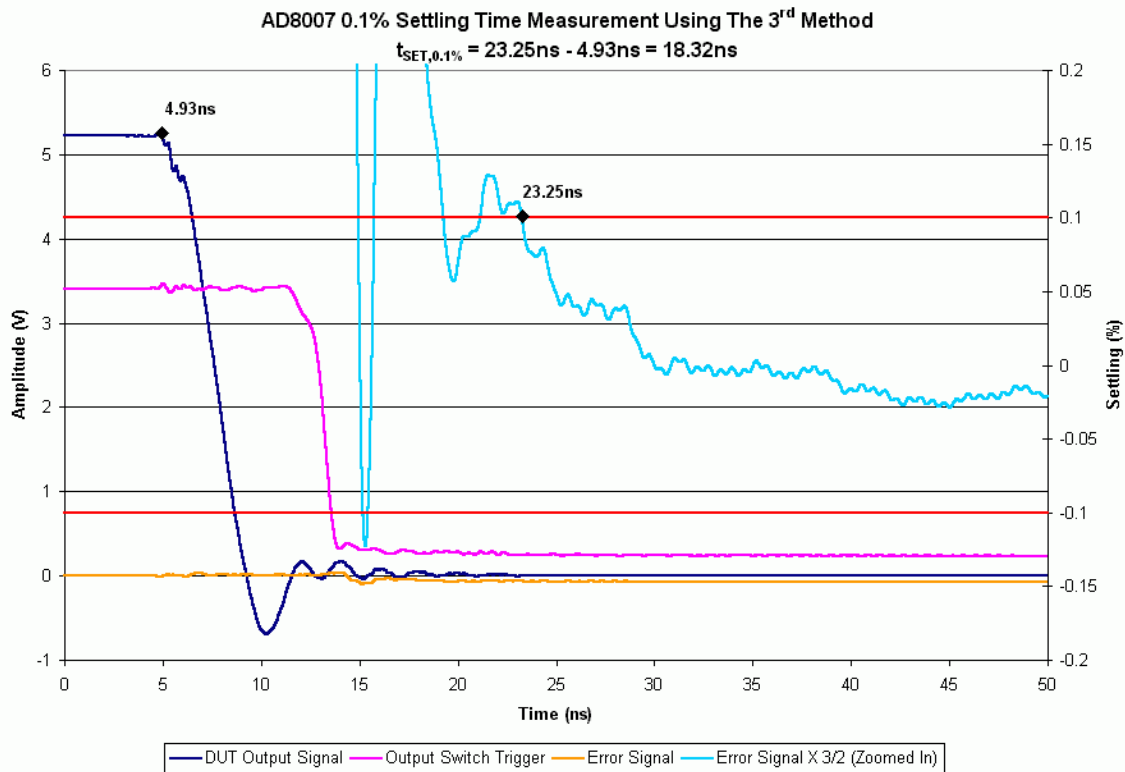
Figure 4-9: AD8007 0.1% Settling Measurement Using The Third Method
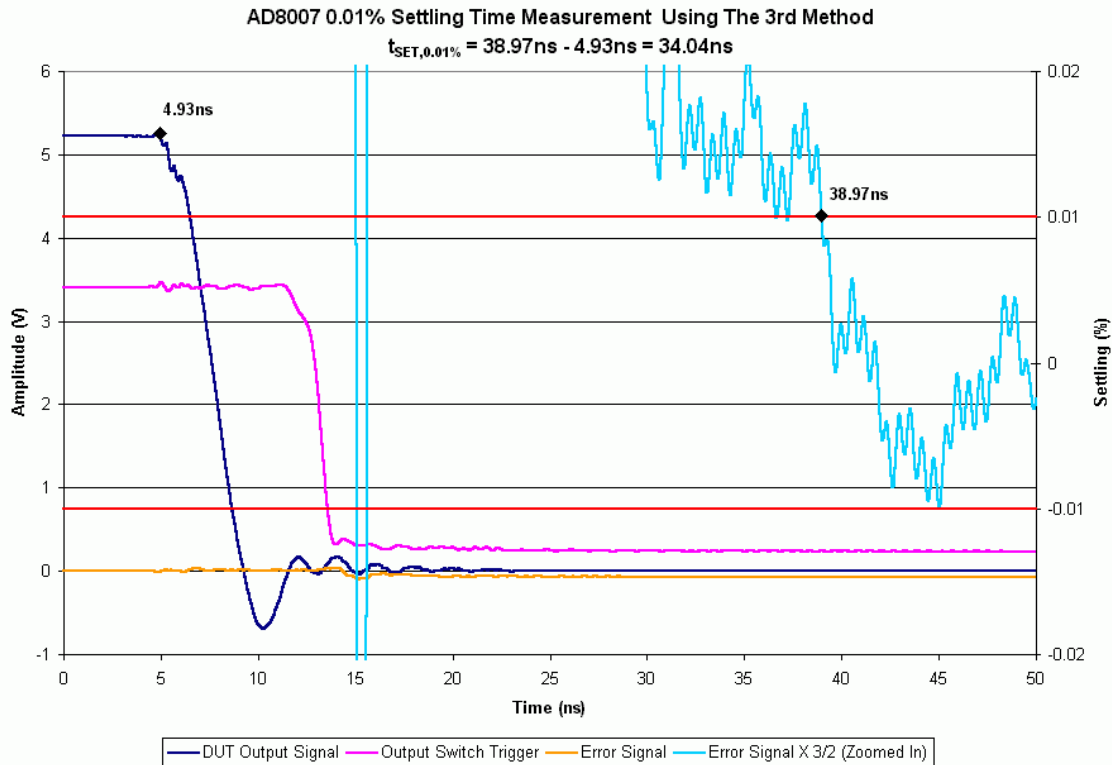
Figure 4-10: AD8007 0.01% Settling Measurement Using The Third Method

4.5 Unwanted Behavior

4.5.1 DUT Output Ringing

First layout of the third method worked well for AD8007 except for one condition. When the input pulse was applied and the DUT transitioned from +2.5V to –2.5V, there was a short ringing. As shown on *Figure 4-11*, the ringing was short and decayed before the amplifier settled. Therefore it was ignored at first.

The same amplifier was tested on an AD8000 test board. Due to different pin configuration of the amplifiers (AD8000 and AD8007), the board had to be rerouted using wires. Even then, there was no ringing at the output. This raised a question mark about the parasitics of the first PCB layout.

Figure 4-11: 3rd Method – 1st Layout: DUT Output Ringing (AD8007)

Before pointing the finger at the parasitics and designing a new board, a few experiments were conducted through simulations. This is because third technique uses a different method to create a pulse and this behavior might have been an issue related to this switching method. Nonetheless, it was found out that the cause of this ringing was related to parasitics; therefore 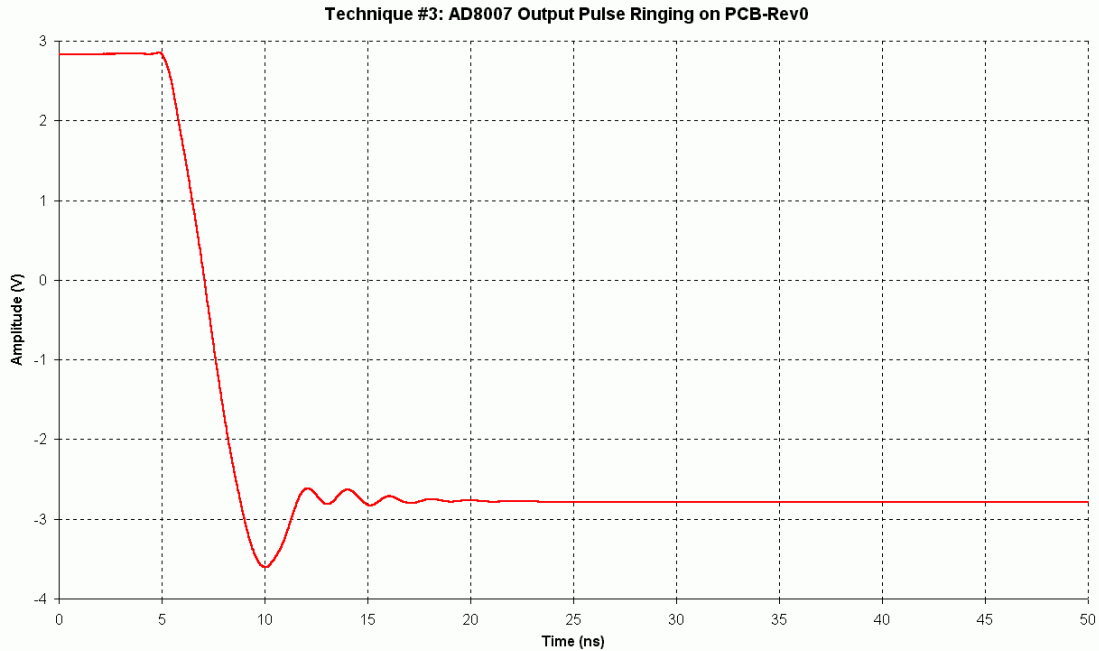a second layout was designed. Through more careful routing this behavior was completely eliminated on the second PCB. The result is shown on *Figure 4-13* (The red line is the DUT output when the switch is never triggered).

4.5.2 Oscillation Problem

The oscillation problem became very clear on the second board. With the switch remained closed, the DUT output was very clean, free of ringing. Trouble became apparent when the switch turned on. *Figure 4-12* shows the oscillation at a frequency of 3.2GHz. The red line is the DUT output (no ringing is left), the blue line is the switch trigger and the purple line is the bridge output. Since AD8007 has a bandwidth of 650MHz its amplitude is not too large but big enough to prevent settling. After this behavior was observed the results of the first board was rechecked. It was realized that there was a hint of this oscillation on the first board too. As can be observed from the *Figures 4-9* and *4-10* there is a very small oscillation, which was first thought to be

related to noise. Since its frequency was higher, its amplitude was not as high as the one on *Figure 4-12*.
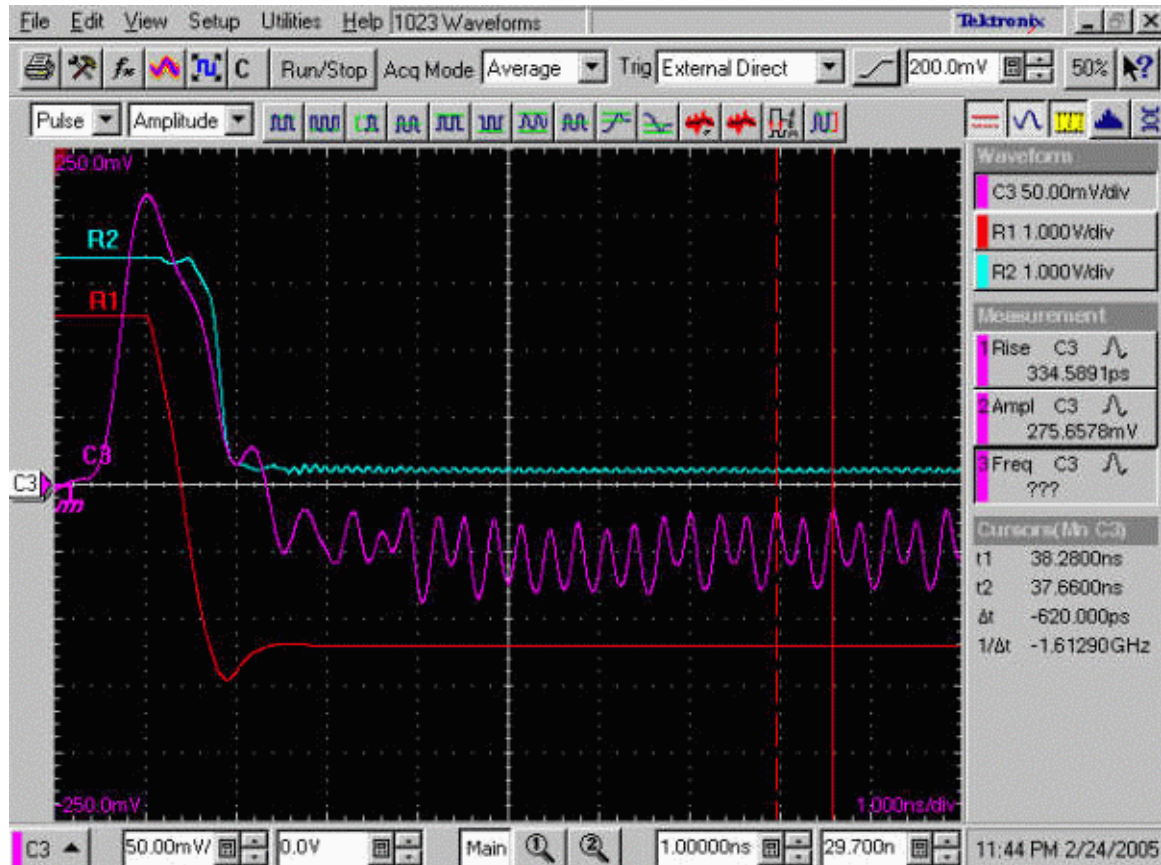
Figure 4-12: 3ʳᵈ Method – 2ⁿᵈ Layout: Oscillation when the Output Switch is on

It became clear that settling could not be measured using the second board. To continue with the measurements AD8000 was tested on the first board. With its massive bandwidth of 1.5GHz, the barely noticeable oscillation on *Figure 4-10* became a lot more obvious. The oscillation was confined in the 0.2% band. After this experience it was accepted that 3ʳᵈ technique was to be tested using only AD8007. Not only there was an oscillation at the output but also this oscillation was carried to DUT output through other parasitics. Two waveforms are shown on *Figure 4-13*, the DUT output when the switch is triggered and when no switching is used. A small amount of oscillation is noticeable on the picture.

Settling measurements were clearly over and an investigation was started to find out the source of this oscillation. Among the things, which were attempted, was using a coax connection to the scope. The thought behind this was that probe's small capacitance

was interacting with circuit parasitics. Therefore placing the probe on the circuit might have been causing this behavior. It was not the case. Another thought was that the bridge capacitance was affecting the buffer output and this was causing a problem. Snub resistors were added to the input and the output of the bridge. By doing this, the oscillation was not even attenuated. While running out of ideas one last thing was tried.
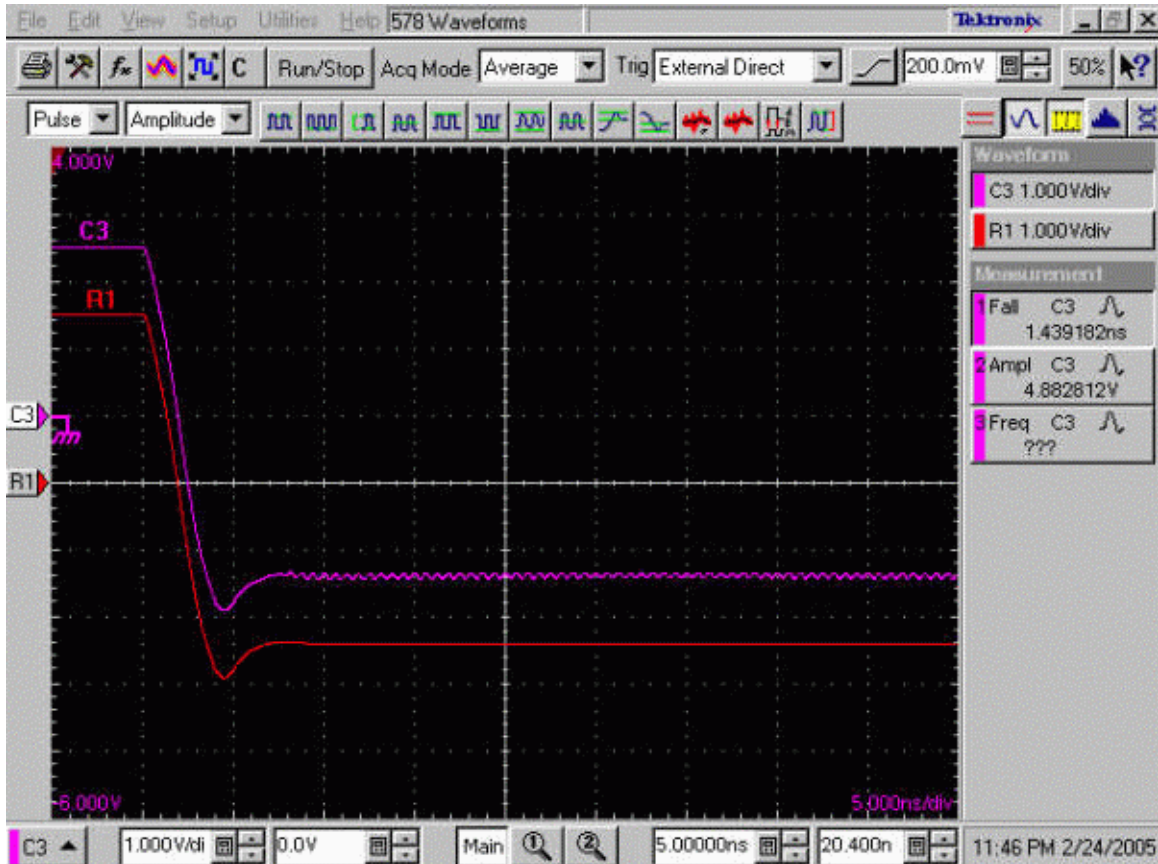
Figure 4-13: Oscillation carried to the DUT Output (AD8007)

From the PCB layout, it is noticeable that the differential switching traces are very thin and long (*Figure 3-14*, thin parallel traces on the right side of the board). To check if this was an inductive problem, something had to be done to those traces. Hacking on these traces and adding a resistor was not preferred because there were only two available test boards. Another thing to do would be to add some solder to change the thickness of the traces, and thus the inductance. When this was done, the board was retested. The results were satisfying (although very ugly), since now the oscillation frequency dropped down to 666MHz from 3.2GHz. This meant that now the oscillation was well within the bandwidth of AD8007; therefore the oscillation amplitude was increased. To further

check that the oscillation was coming from those traces – and not from the amplifier – AD8007 was replaced with AD8000. As a result, oscillation frequency *did not change* but now its amplitude reached 700mV. These results are shown on *Figures 4-14* (AD8007) and *4-15* (AD8000).

Later on, spice experiments were conducted to further prove that the reason of the oscillation was caused by the inductance on the described traces.
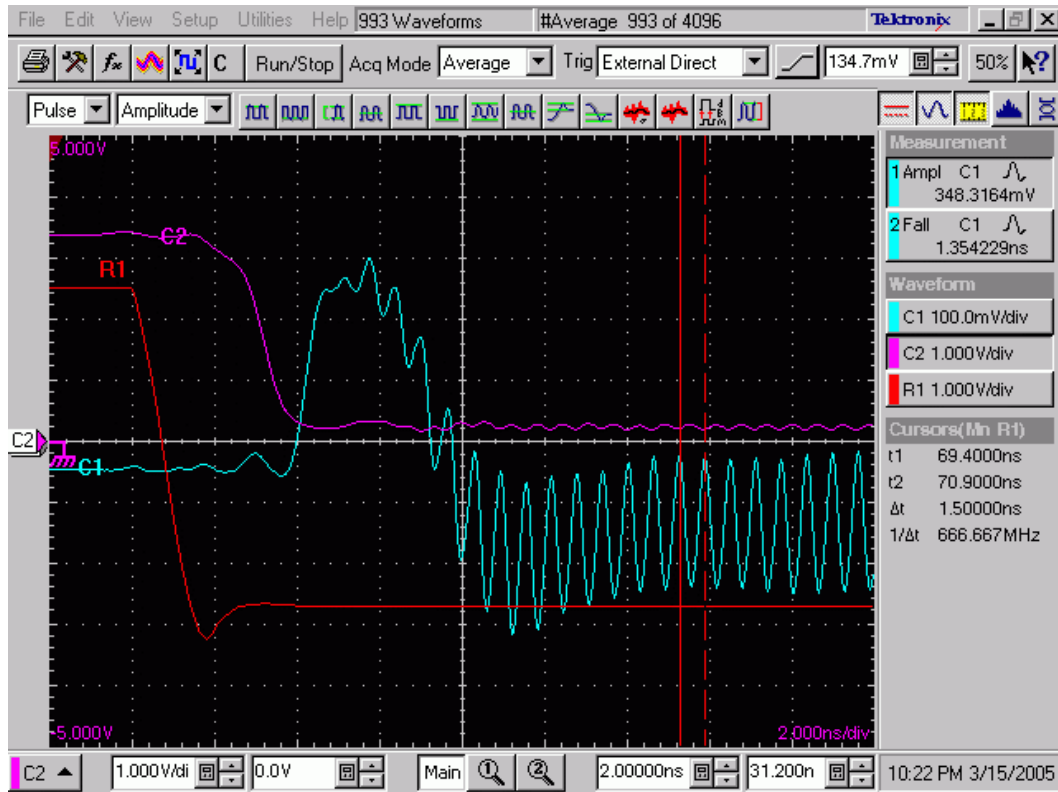

Figure 4-14: Switching Oscillation: Lower Frequency, Higher Amplitude (AD8007)
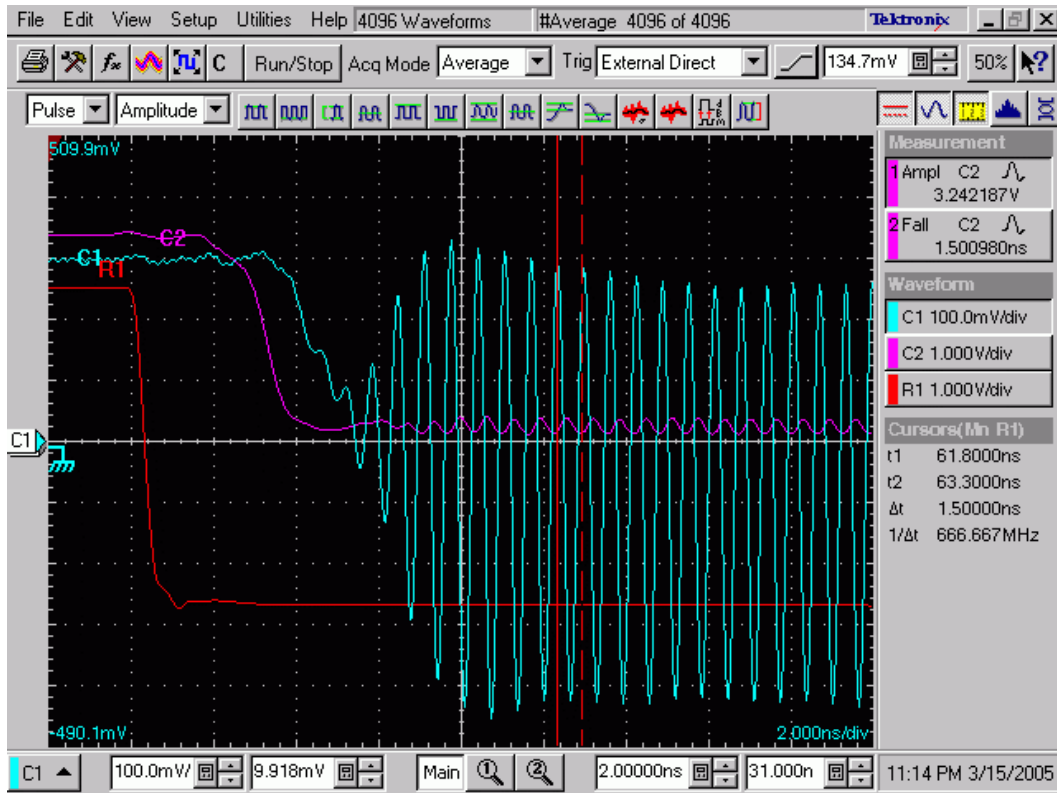
Figure 4-15: Switching Oscillation: Increased Amplitude due to Higher BW AD8000

4.6 Summary of Results

The purpose of this section is to gather all the collected data together. Comments are also made on results and different features of the circuits. The results of the measurements are summarized on *Table 4-1*.

Amplifier	Settling Band	Datasheet	Method #1	Method #2	Method #3
AD8000	0.1%	12ns	13.1ns	7.3ns	
AD8007	0.1%	18ns	24.6ns	17.5ns	18.3ns
	0.01%	35ns	41.4ns	32.6ns	34.0ns
AD8045	0.1%	7.5ns	17.4ns	9.5ns	

Table 4-1: Summary of Results

Even though Method #1 is the simplest circuit, it is hard to achieve reliable results using this technique. The method is the most vulnerable measurement to input imperfections. Results of this technique are the longest ones. These could have been improved through better soldering but the goal was to make the reader to acknowledge the fact that it is possible to obtain false results that may look like dependable numbers.

Method #2 is a lot more reliable, since now the actual error signal that the amplifier sees is replicated at the false summing node. Also clamping this node improves the oscilloscope resolution efficiency. Input imperfections are minimized since the output is referred to the input. The results obtained from this method correlate to the datasheet. As explained before, in case of AD8045, the 2ns extension is due to the larger feedback resistor used on the circuit. The layout of the circuit is very simple and easy to build. With proper PCB design and careful soldering highly accurate and fast settling results can be obtained. The only necessary trim on the circuit is the pre and post settling DC offset, which can be accomplished through a trimmable resistor. The measurement is fairly quick and reliable.

The nicest feature of Method #3 is the input current switch. This way the dependence on input pulse characteristics is eliminated. This kind of switching creates a very clean pulse with a very fast fall time (slew rate of AD8007 was improved to 1.8V/ns). The bridge circuit driver (i.e. buffer) prevents any bridge transients from affecting the settle node. The downside is that it might extend the settling due to its own characteristics. The output switch is another feature of the circuit. It is useful if a low-resolution or an analog oscilloscope is used for the measurement. It is not completely necessary if a high-resolution scope is used to make narrow band measurements. This is primarily due to the very low forward voltage drop on the modern schottky diodes.

The circuit of Method #3 is complicated, which even more complicates the PCB layout. As shown on *Section 4.5*, a small mistake on the board can cause big problems on the circuit performance. With the output switch comes three more trimming. These take *a lot* of time and very high patience is required. It should not be expected that the measurement would be done within an hour. Having said that, *if* the trims are properly made highly accurate settling times can be measured.

The results obtained from the third method are slightly slower than the second method, which is not a big issue. This is primarily due to the buffer and also two delay routes, which were explained in the previous chapter. The delay on the bridge output could not be measured; it was too small. The delay to the settle node was only few picohundred seconds. Since the probe could have interfered with such a small measurements, they were not compensated for.

There were few unwanted phenomenon on the circuits. On the second circuit there were two small bumps due to non-perfect termination. These reflections did not interfere with the 0.1% measurement results of AD8000 and AD8045 but for their 0.01% settling performances, it would have yielded unreliable results. Since by the time AD8007 settled these reflections were already dissipated, its settling performance was not affected.

Two other unwanted behaviors were found on the third method. The DUT output ringing was linked to parasitics; and through more careful routing, on the second revision of the PCB, this ringing was eliminated. The oscillation on the second board was explained through various experiments and the cause was linked to parasitic inductance. Simulation results, which investigated these two phenomenons, are presented on the next chapter.

5 Simulations

5.1 Doublet Effects on Settling Time

5.1.1 Pole-Zero Separation

The effects of pole-zero matching were previously explained on *Chapter 2*. These can be better understood through hands-on experiments. Therefore few simulations were conducted using MATLab. The first simulation is the Pole-Zero Separation, where the effects of separation factor and the position of poles and zeros relative to each other are explained. The simulation block diagram is presented on *Figure 5-1*.
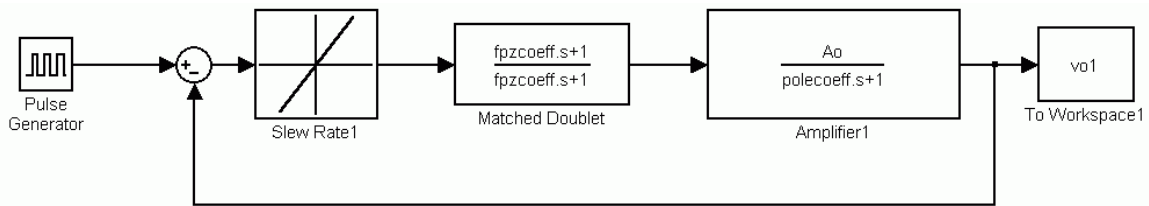
Figure 5-1: Block Diagram for Investigation of Doublet Effects

For simplicity a single pole op-amp model was used. A doublet at 1MHz was introduced after the slew rate stage. The separation factor is chosen to be 2. This is a severe mismatch (50% relative to center frequency) but for demonstration purposes it is acceptable. As this factor gets closer to one, matching gets more ideal. The ideal condition would be a perfect matching, which is practically near impossible. *Figure 5-2* shows the bode plots for three different conditions: Perfect matching, pole frequency is greater than zero frequency, and vice versa. The shifts on the frequency response and the phase response should be noted.

Figure 5-2: Bode Plots of Different Separation Conditions

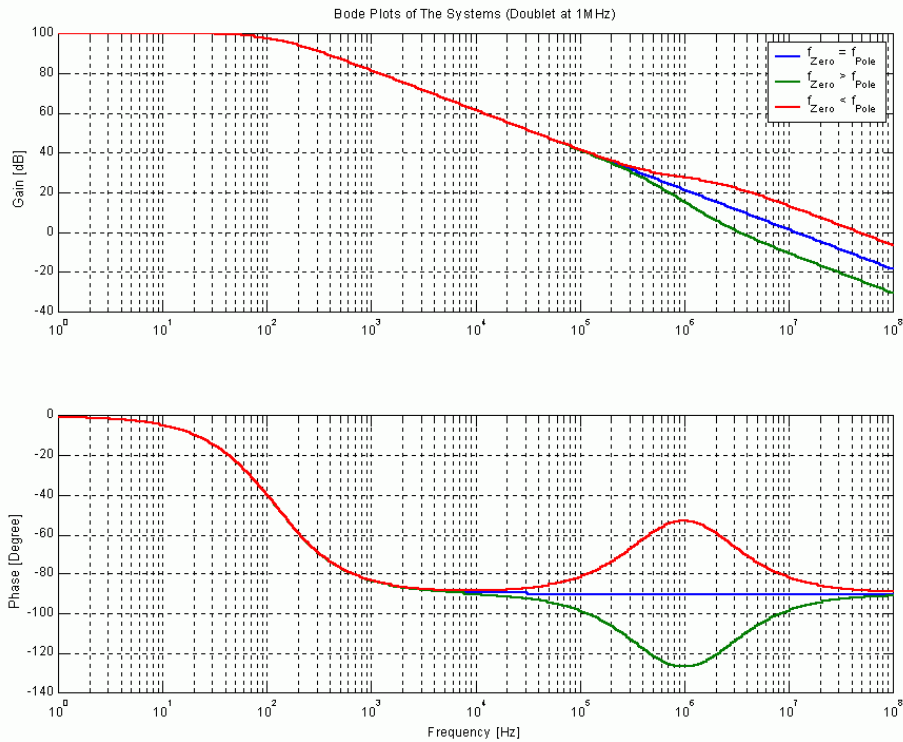On *Figure 5-3,* pulse response of each condition is presented. Upper graph shows the full step, and the lower graph focuses on the settling time. The ideal case, the blue line, is not the fastest rising pulse, nor it is the slowest. However it is the fastest settling signal. If the zero frequency is lower then the pole frequency, this *artificially* decreases the phase margin; therefore the waveform overshoots (the green line). Then it slowly decays to its final value. The red line, on the other hand, is overcompensated ($\phi_M > 90°$) and it has a long lasting tail.

The graph right below shows the 0.1% settling times. The ideal case settles in 90ns and the other two takes a lot longer to settle (0.6µs and 1.1µs). Next section compares the doublets at different frequencies. MATLab codes of these simulations are given on Appendices.
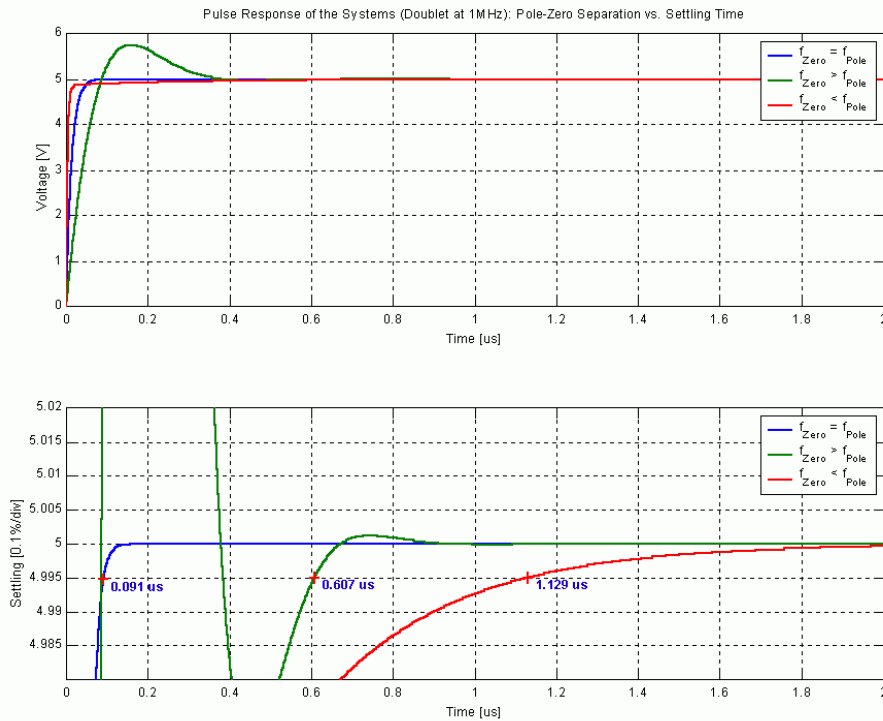
Figure 5-3: Pulse Response of Different Matching Conditions

5.1.2 Doublet Frequency

The block diagram on *Figure 5-1* is used to simulate the effects of doublet frequency. The results are shown on *Figure 5-4*. In this simulation pole frequency is lower than the zero frequency. Therefore there is a dip in the frequency response (similar to the green line on *Figure 5-2*). Changing the doublet frequency changes the location of this dip. Moving this dip closer to the crossover point lowers the phase margin of the system. Therefore higher peaking is expected for higher frequency doublets.

As expected, *Figure 5-4* shows higher peaking for the doublet at 1MHz. The lower frequency doublet does not overshoot as much but it has a slowly decaying tail because it is better (over) compensated. The conditions resulted for 0.1% settling times of 0.6μs for 1MHz doublet and 1.5μs for 250kHz doublet.
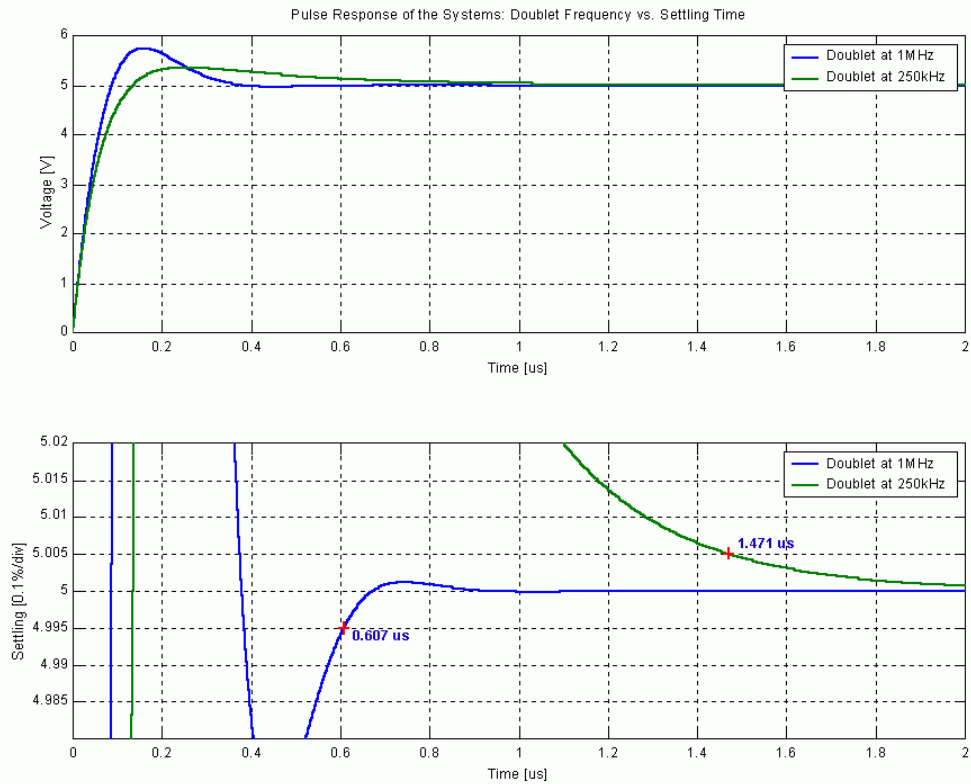
Figure 5-4: Low vs. High Frequency Doublets

It would be wrong to generalize as high frequency doublets result in faster settling times. There might be a condition where the doublet frequency is high enough and the separation is big enough that it creates an under-compensated system, which could even result in oscillations, thus a never settling waveform.

Once again just by looking at a parameter, nothing can be generalized because changing one changes others. Therefore the next simulation investigates stability vs. settling time.

5.2 Stability and Settling Time

Stability of the system affects the rise time and the ringing of the pulse. Therefore compensation is another important parameter for settling time. For this simulation a simple op-amp model, *CK0001, was* designed. It is shown on *Figure 5-5*. Spice was chosen over MATLab because it is more intuitive to show how the stability changes by adjusting the compensation capacitor, C_{Comp}.

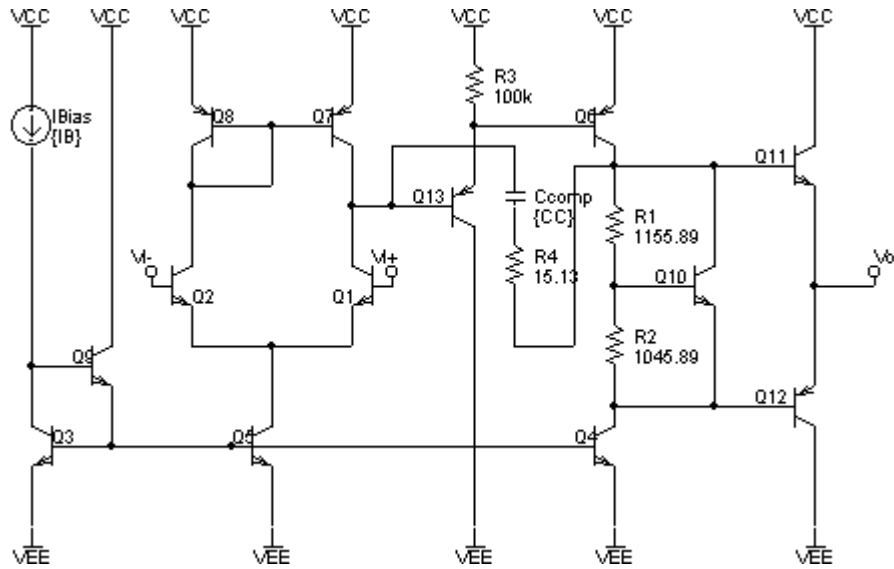**Figure 5-5: Op-Amp Model (CK0001) used for Stability vs. Settling Investigation**

A brief design overview is as follows. Q_1 and Q_2 is the input differential pair. There are actively loaded by Q_8 and Q_7. Q_{13} was added to buffer the two stages in order to keep the impedance (thus the gain) at that node high. A Beta Helper could be added to the current mirror created by the Q_8 in order to improve the performance of the input stage and to keep the bias voltage of both legs at the same point. This was not done because Spice denied functioning properly when an extra transistor was added at that node. The buffer output is connected to the (second) gain stage, which is a common-emitter amplifier with active load. The output buffer is consisted of a push-pull pair. These transistors are biased with the V_{BE} multiplier created by Q_{10}, R_1 and R_2. The values of these resistors are adjusted such that there is 2mA quiescent current flowing through buffer transistors and the amplifier can source/sink 50mA ($\pm$5V into 100Ω) if needed. Even though it is not needed with just three transistors in the bias rail, Q_9 was added as a Beta Helper in order to prevent part of I_{Bias} to flow into the base of these three transistors. The value of I_{Bias} was adjusted such that 0VDC was obtained at the output.

The compensation capacitor was connected between the collector of Q_6 and the base of Q_{13} rather than the base of Q_6. Adding the buffer transistor, Q_{13}, introduced a doublet in the frequency response (previously mentioned in *Section 2.2.2*). In order to bypass this doublet this compensation scheme was used (rather than removing the buffer and sacrificing gain). It might be considered as cheating but for the purposes of this

simulation it was an effective and a simple way to solve the problem. R_4 was used to push the zero created by the addition of the compensation capacitor to infinity. Setting its value equal to $1/g_{m6}$ enables that.

A parametric simulation was conducted using three different values for the compensation capacitor, 150pF, 500pF, and 1.5nF. The bode plot and the pulse response is shown on *Figures 5-6* and *5-7* respectively. Each value of the capacitor resulted in a different crossover frequency, thus a different rise time, a different phase margin, and ultimately a different settling time. These results are summarized on *Table 5-1*.
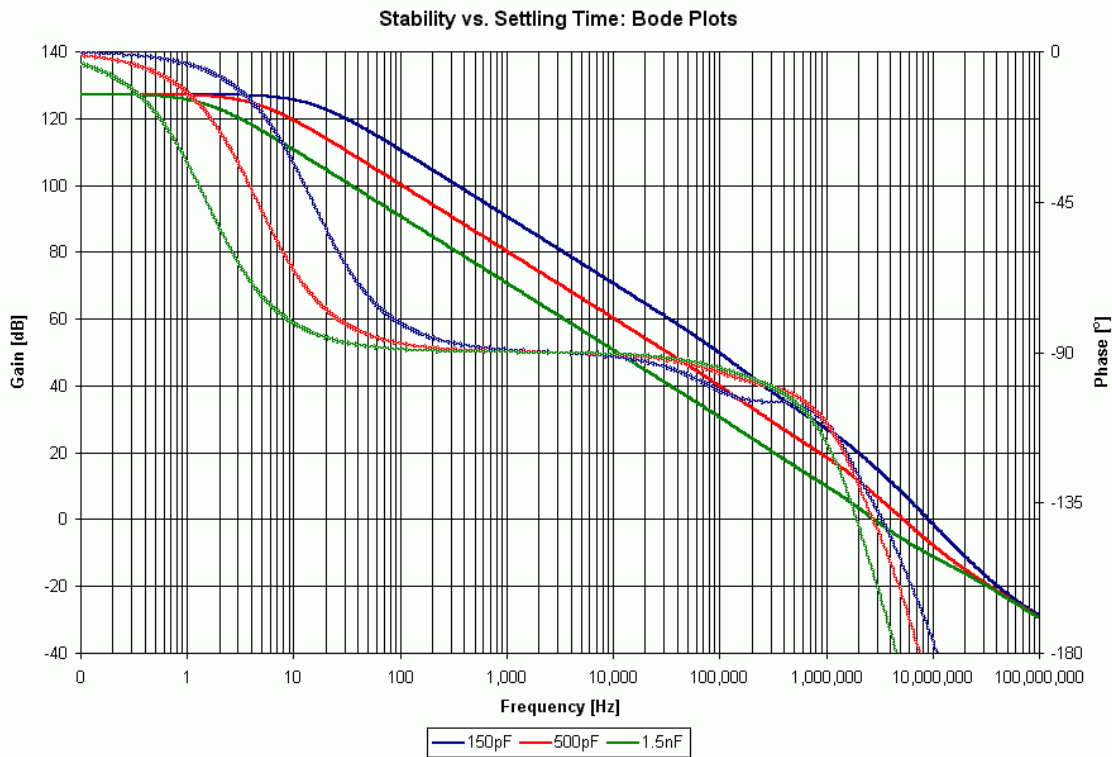
Figure 5-6: Bode Plot of CK0001

C_{Comp}	ϕ_M	Slew Rate	Rise Time	0.1% Sett	0.01% Sett
150pF	7°	**11.46V/μs**	**0.157μs**	2.13μs	3.67μs
500pF	15°	3.44V/μs	0.524μs	**1.52μs**	**2.08μs**
1.5nF	**23°**	1.15V/μs	1.57μs	2.73μs	3.38μs

$*I_{TAIL-DIFF\ PAIR}$ = 1.719mA

Table 5-1: Summary of CK0001 Simulation

The highest value of compensation resulted in the largest phase margin. The smallest compensation resulted in the highest slew rate. The optimal compensation had

mediocre phase margin and rise time. However it was the fastest settling system. It should also be noted that overcompensated system settles faster to 0.01% than the under-compensated system. This simple simulation emphasizes the importance of the stability. Low stability causes longer ringing. Over-stable systems extend the settling time. The optimal point of compensation should be found for best settling results.
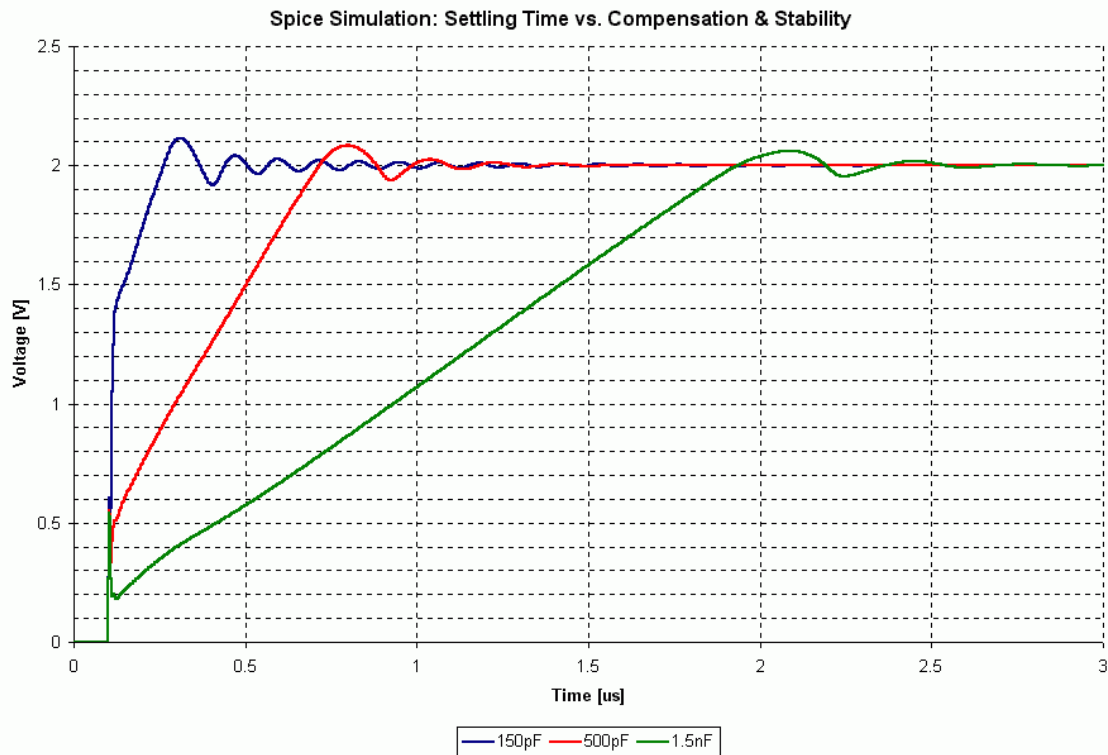

Figure 5-7: Pulse Response of CK0001

5.3 AD8007 Correlation: Simulation vs. Bench

One of the goals of the project was to understand the settling behavior of AD8007. This meant the matching the simulation results with the bench measurements. For this task, first simulations were performed through Spice. The model for AD8007 was extracted from the datasheet and the part was created in Spice. The settling behavior did not match at all by just using the op-amp model. Various parasitics were added to the model. The parasitics were approximated by the trace width and length on the PCB. Unfortunately, this as well did not improved matching.

Then a simple current feedback op-amp was designed. Although the speed of the design model was similar to AD8007, the pulse characteristics were completely different.

After these experiments, it was decided to use Simulink/MATLab to do the simulations. The thought behind this was a non-ideality that could be affecting the transfer function of AD8007.

The block diagram used for the simulation is shown on *Figure 5-8*. The slew rate was set to 1.4V/ns. The transfer function of AD8007 was extracted from the spice model. Two pole-zero pairs were added to the overall transfer function in order to find out if a few doublets were giving the characteristic shape of the pulse. The results are shown on *Figure 5-9*.
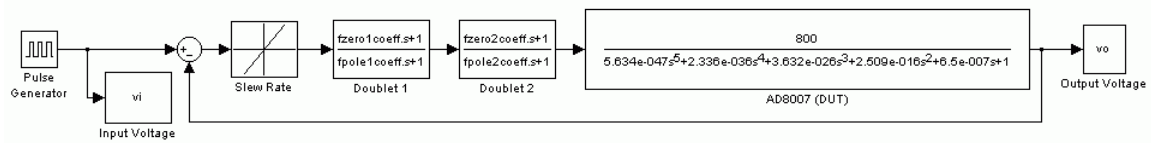

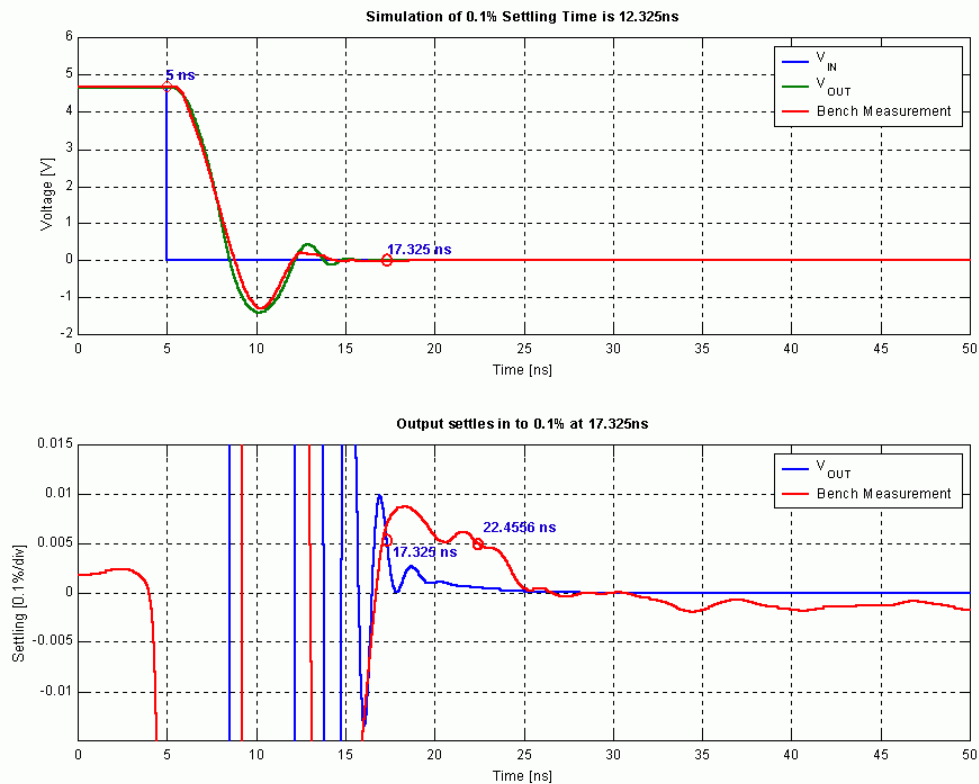**Figure 5-8: Block Diagram used for the Correlation Simulations**

Figure 5-9: AD8007 Correlation Results

For the matching, the settling waveform of *Figure 4-6* was used. The full swing is shown on the top graph, and the amplitude corrected settle node is shown on the bottom graph. While the simulations did not perfectly match the bench, which was not expected anyway, the waveforms looked very similar, especially the slew portion, and the dip after slewing (something that Spice did not show). Additionally, the two little bumps on the simulation were also observed on the measurement (The graph on the bottom).

The simulation showed a settling time of 12.3ns compared to 17.5ns of the bench. The results are, evidently, are not perfect but satisfactory.

5.4 Parasitics

5.4.1 DUT Output Ringing

On *Section 4.4*, a few unwanted behavior was mentioned. It was important that the source of these problems were found. It was not too hard to understand the first problem. Two different boards, resulted in two different pulse responses. This made it obvious that the output ringing of the DUT on the third method was created by the board parasitics. However, before attempting to spend the resources, especially time, on a second board, more proof was gathered through simulations.

The circuit used in the simulation is shown on *Figure 5-10*. The AD8007 model is used in the circuit. The input bridge circuit was replaced by a current pulse generator to simplify things. All the circuit was drawn until the buffer input. Then the PCB Rev0 was analyzed. By looking at the trace width and length in this portion of the circuit the parasitics were approximated. The appropriate parasitic was placed to the appropriate section on the circuit with its estimated value.

The results were really satisfying and allowed the finger to be pointed to the board parasitics directly. The simulation is compared to the bench measurement on *Figure 5-11*. The ringing had the similar amplitude and frequency; it also decayed at about the same time. Obviously the board had to be revised in order to better the pulse response of the amplifier. Consequently a second board was designed and the ringing was completely eliminated.
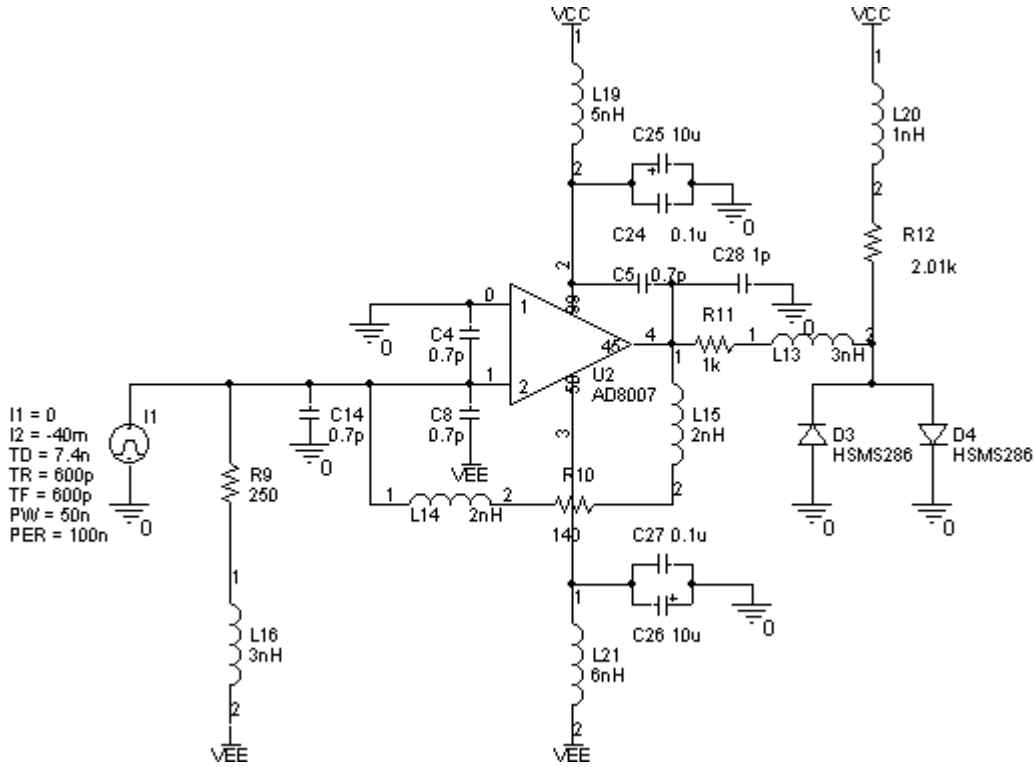
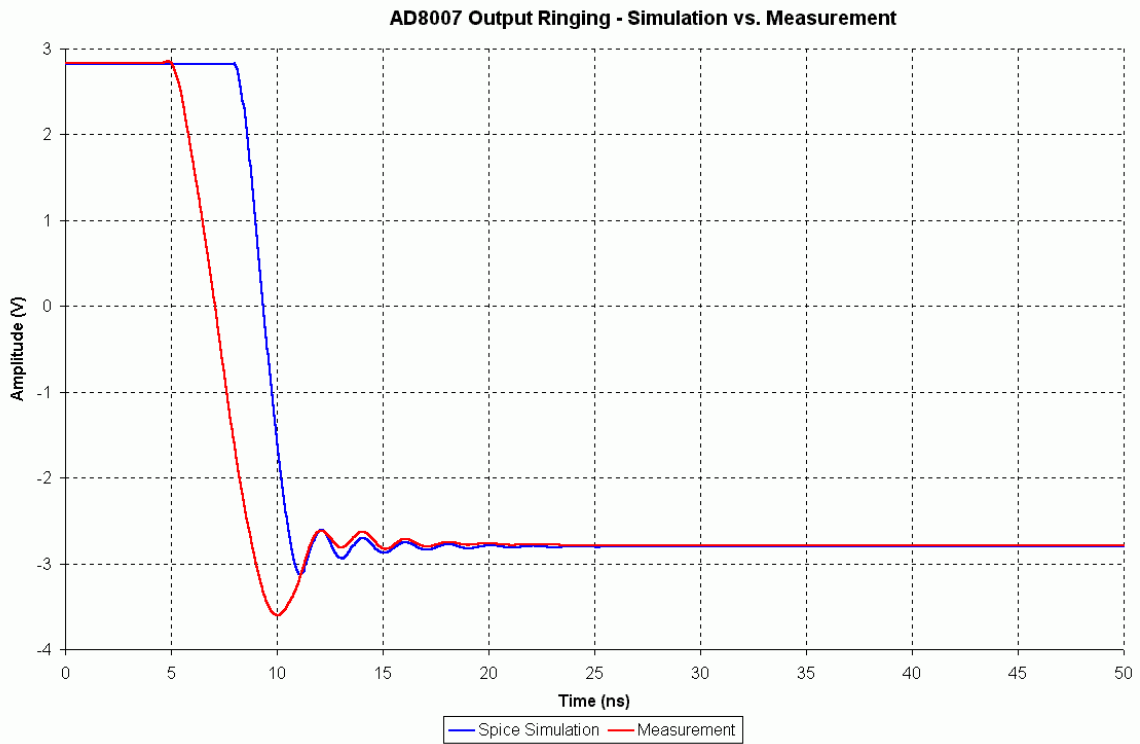**Figure 5-10: Schematic for DUT Output Ringing Simulation**

Figure 5-11: DUT Output Ringing on the 3rd Method: Simulation vs. Bench

5.4.2 Bridge Circuit Oscillation

On the second board, some of the previously existed portions were removed and some new ones were added. Especially the input circuitry was made as compact as possible. These changes affected the whole board, and the layout of the circuit was re-designed. This generated a new problem, a bigger one and hard to spot. An oscillation arose whenever the output switch was turned on.

Through experiments, which were explained on *Section 4.5.2*, the cause of this oscillation was linked to the trace inductance on the differential current switching path. Due to time constraints designing a third board was out of question. Again, to further prove this theory, Spice simulations were used. The circuit that was simulated is presented on *Figure 5-12*. This time parasitic extraction was less tedious since the troubled trace was known.
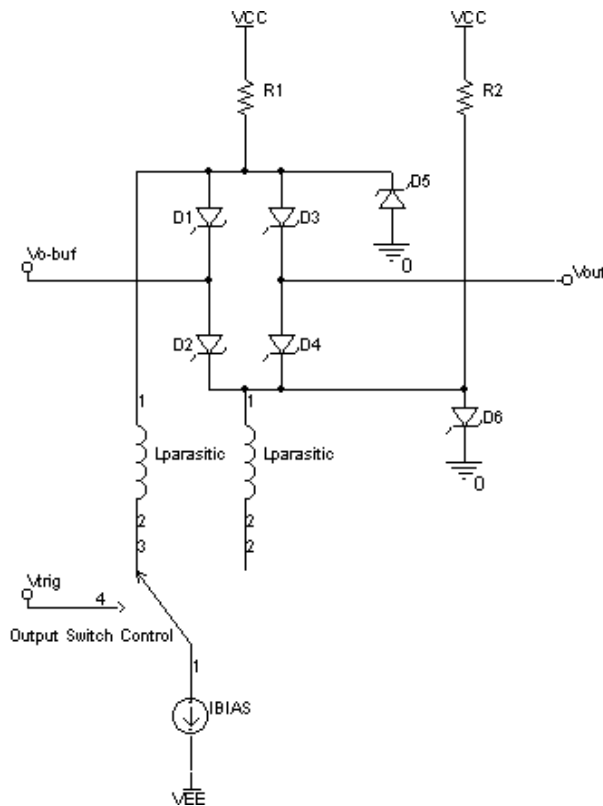
Figure 5-12: Simplified Output Bridge Circuitry with added Parasitic Inductances

Two inductors were added to the switching traces, which are connected to the top and the bottom of the bridge. Then the simulation was started. Exact same phenomenon was observed as the bench. If the switch was not triggered anytime, there were no

oscillations. On the other hand, whenever the switch was turned on, there was a clear oscillation on the circuit, as shown on *Figure 5-13*, which proved the theory of *Section 4.5.2*. Also a small capacitance was added to between the inputs of the buffer in order to simulate the package parasitics. Although it is not observable on the graph (its amplitude is only few hundreds of microvolts), this carried the oscillation to the output of the DUT.

Figure 5-13: Simulation Results for Output Bridge Oscillation

6 Conclusions and Recommendations

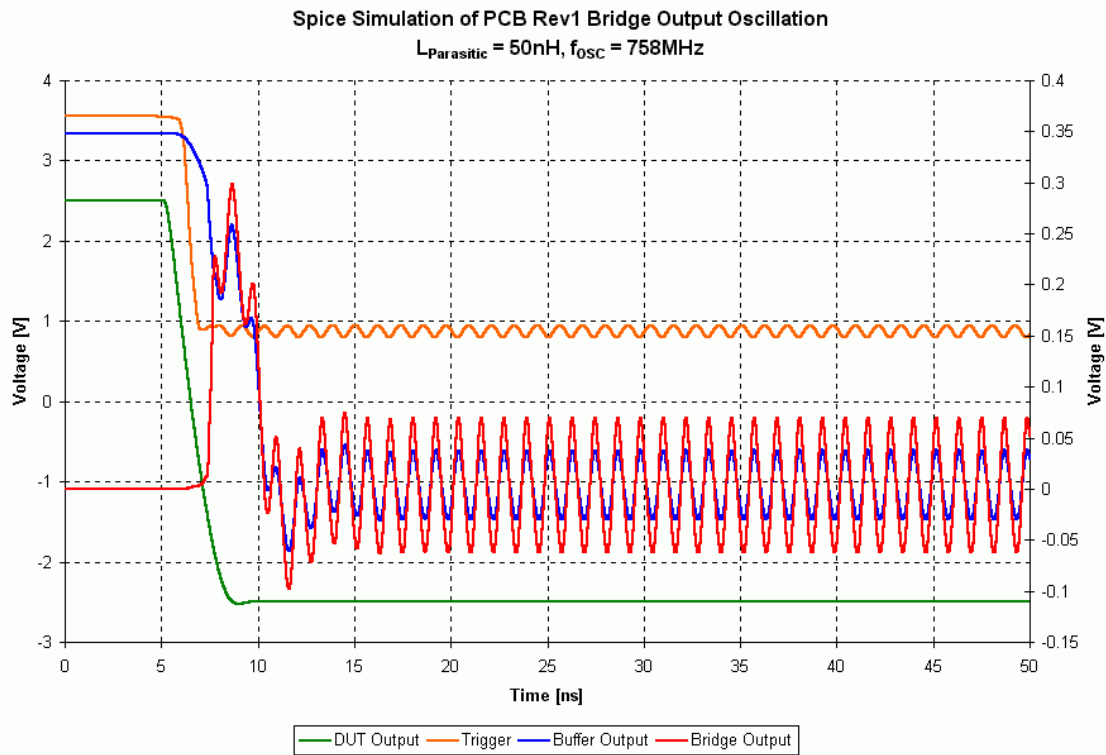Measuring settling time is a very challenging task. When the amounts of voltages and the speed involved are considered, the challenge becomes more evident. At the same time, as challenging it is, this parameter plays a crucial role on data acquisition. It is the primary factor that defines the fastest data rate for an intended accuracy. In other words, it will specify the error for a given transfer speed. The accurate measurement of settling time, therefore, is very important.

There are number of ways in the literature to accomplish this measurement. Three that seemed most promising were chosen to complete project goals. Each of these techniques was explained in detail in the *Design Analysis* (*Chapter 3*). Along with the explanations, simulations of these methods were provided in order prepare the reader for the real measurements chapter and to give an idea of what kind of waveforms to expect.

As can be derived from the results, each method has its own advantages and disadvantages. Method #1, for example, ideally would be the fastest method of all, since it is simplistic and has no extra blocks added. It was shown on *Section 4* that this was hardly the case. Although it is not impossible to make accurate measurements using this method, board layout and component placement must be optimized. Another downside of this measurement is resolution of the oscilloscope is wasted on the full dynamic range of the output signal.

Method #2, as the results showed, turned out to be a reliable and quick technique. With the addition of two extra resistors, along with the feedback and the gain resistors, a bridge type of network is created. This enables the circuit to replicate the signal at the summing node of the amplifier, on a different node called the 'false summing node', or the settle node. Clamping this node using Schottky diodes prevents unnecessary voltage excursion, since only few milivolts – or even less – of the voltage at this node is actually important. This increases the effectiveness of the scope resolution.

The results obtained from the second technique were truly satisfying. High speed probes combined with high speed Schottky diodes create minimal disturbance to the circuit. Therefore the results are very reliable. Having said this, there is still one issue with the circuit. The input imperfections are still not totally eliminated. How could the input be provided with a flattop pulse, with something *does not* exist in reality?

The answer is embedded on Method #3, where the input pulse is rather used as a trigger to improve the already well-functioning false summing node. This trigger controls a current switch. This switch controls the current flow into the summing node of the amplifier. This way, as it was previously demonstrated, very clean and fast pulses can be obtained at the output of the amplifier. This output transition is compared to a reference voltage in order to obtain a settling near 0VDC. Of course the clamping diodes are also extremely useful here.

This is not all that the third technique has to offer. The settle node is connected to an output switch through a buffer. This is recommended as an optional feature especially for low-resolution or analog oscilloscopes. This switch is controlled such that it is ON for only a short period of time, just to see last few percent of settling. The goal is to minimize voltage swing for maximum resolution effectiveness without overdriving the scope.

In the other hand, with these nice features come the cons. The buffer used to safeguard the settle node from the output switch does extend the settling time, by a very small amount, however, as shown on *Section 4.6*. Additionally, there are number of delay routes that must be accounted for. *Section 3.4* explains a trick to bypass these delays embedded to the test circuit. Finally, the most crucial sector of the circuit, which is more likely to cause problems more than anything, is the output switch. When it is turned on there are all kinds of switching transients. For proper measurements the diode bridge, which is used as a switch, must be calibrated. This task is not as easy as it sounds; and takes the most of the time and the effort used to measure settling time; very high patience is required. Using this method, tester should *not* expect to be done with the measurement in an hour or two.

An interesting question arises: "If the input of the 'False Summing Node' circuit can be improved to create near perfect pulses, and a high-resolution scope is accessible, then, why use a buffer and an output switch to complicate things?" Therefore it is recommended that the best features of two methods, #2 and #3, be combined. This way, the circuit, thus the layout of the PCB, becomes a lot simpler and very efficient, accurate, and reliable settling measurements can be made.

Speaking of PCB layout, routing is extremely crucial to the measurement. At the time of design of the test boards, first of the two PBCs was thought to be compact with

minimal parasitics. Later on, this was proved to be wrong with a ringing at the output of the DUT. The second board, which was even more compact, completely eliminated this ringing. On the other hand, changes made to the layout, now, caused an oscillation on the bridge circuit. As proved by hands-on experiments and by simulations, this oscillation was due to parasitic trace inductance.

Throughout the report the importance of the PCB design is emphasized many times. The two problems that were encountered prove this importance. This is why it is dwelled on this subject. The circuit should be as tight as possible; grounding scheme is very important as well as bypassing. The ground plane near important nodes must be kept clean. If there is a part of the circuit that creates a lot of noise on, its grounding should be separated as much as possible. Having a plain ground plane is preferred. If this is not possible, the amount of traces on the non-component side should be minimized. Furthermore, although not completely necessary (at least for the accuracies down to 0.01%), it is recommended that shielding be used.

The project did not only involve bench testing. There were also few simulations conducted to better understand the parameters that affect the settling behavior. Pole-Zero pair simulations, especially, was important to visualize the theory behind it. Also effects of compensation were demonstrated. From the knowledge gained from these simulations, bench and simulation correlation was carried out for AD8007. Although the results were not perfect, the settling characteristics of AD8007 were very similar to the simulation results.

Settling time measurement is important and even more challenging, especially because it integrates very small amounts of voltages with high speed. It is one of the hardest time-domain tests. If the methods, tricks, warnings, and recommendations in this report are used as guidance, the degree of difficulty can be lessened and reliable results can be obtained with relative ease.

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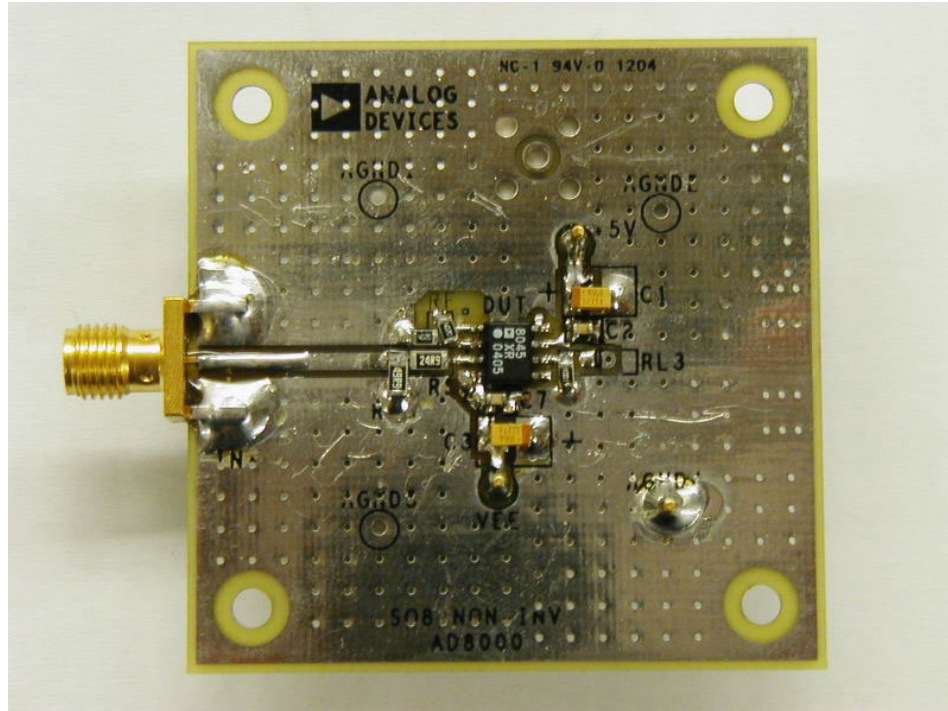
Appendices

A1. Pictures of the PCBs
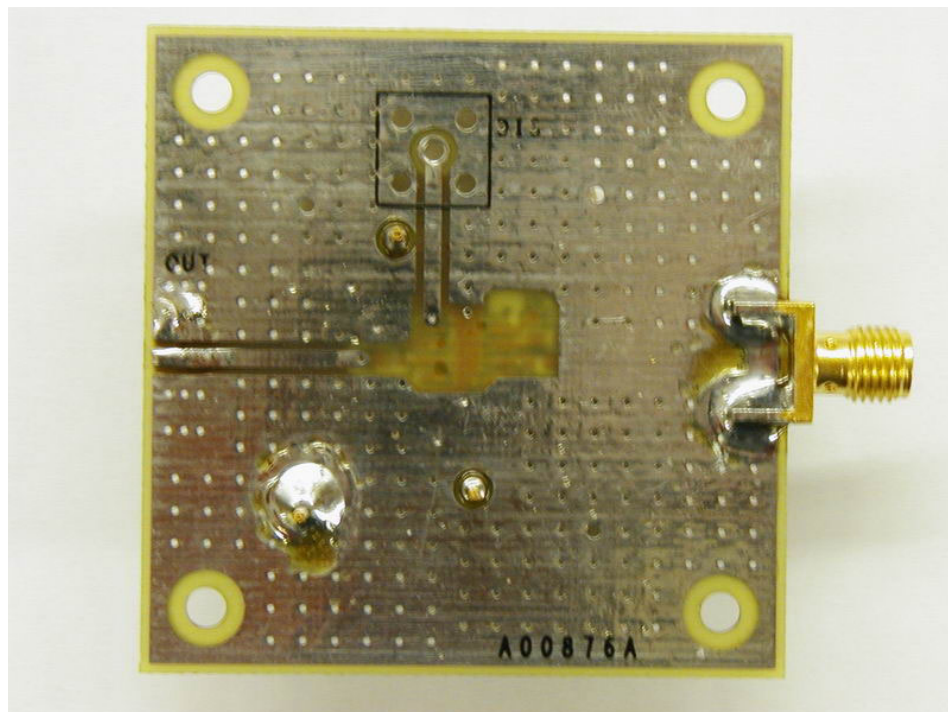

Figure A-1: AD8000 Test Board (Top)
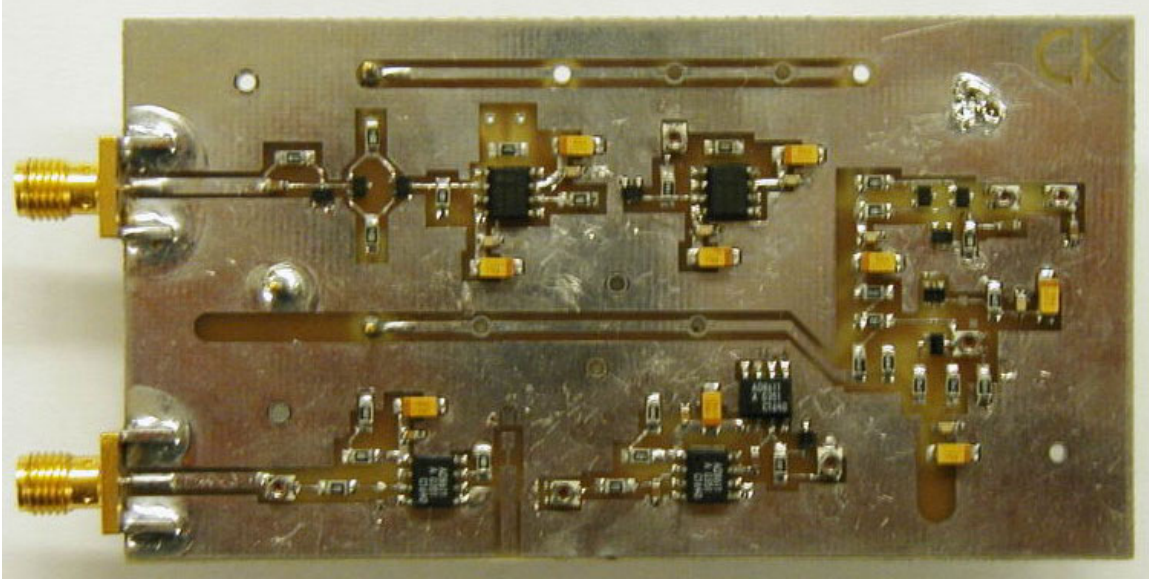

Figure A-2: AD8000 Test Board (Bottom)

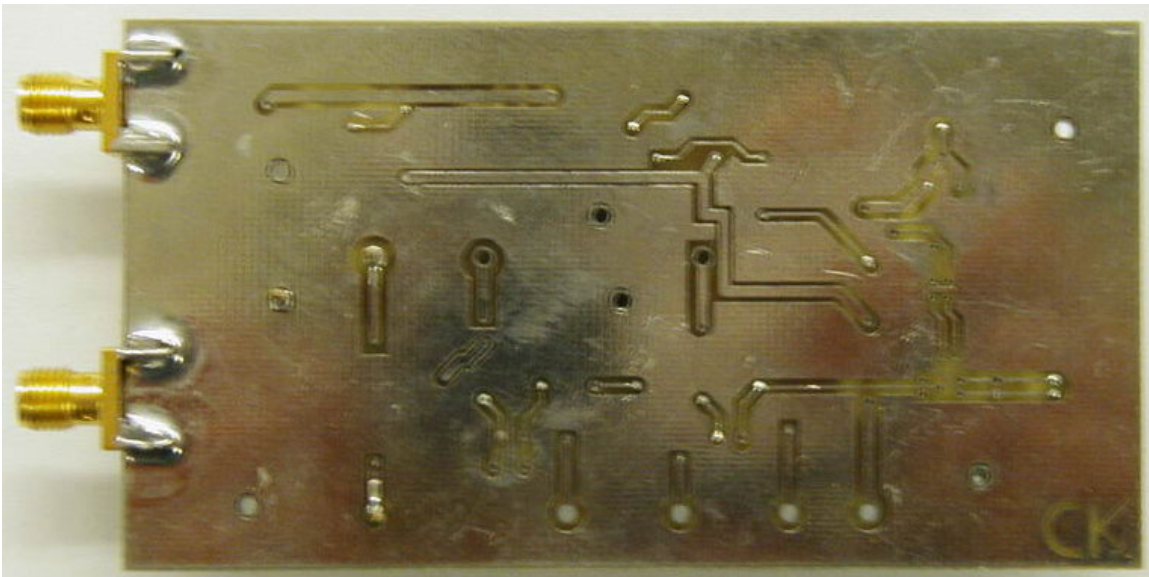**Figure A-3: PCB Rev0 (Top)**

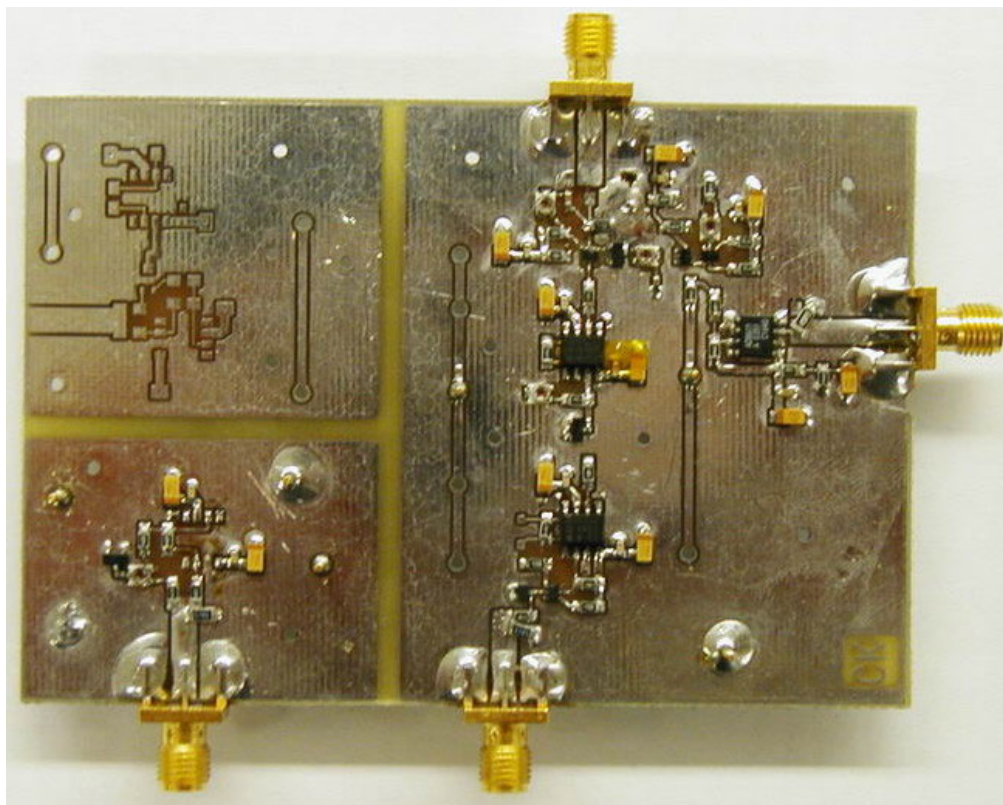**Figure A-4: PCB Rev0 (Bottom)**

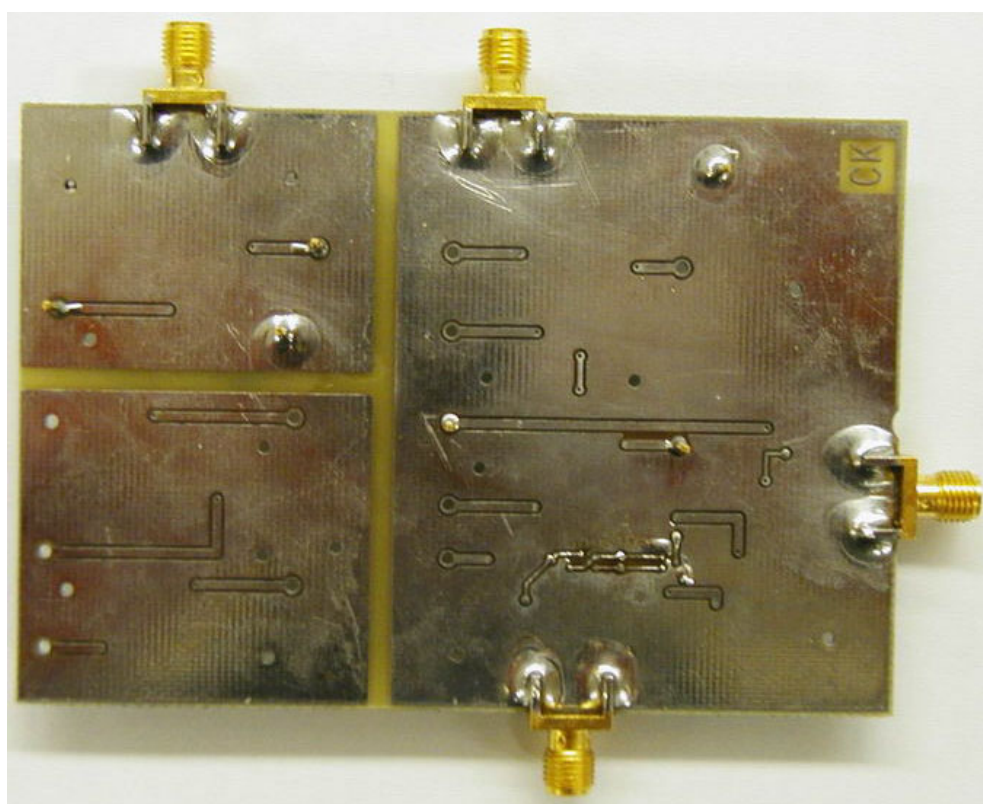**Figure A-5: PCB Rev1 (Top)**

Figure A-6: PCB Rev1 (Bottom)

A2. MATLab Codes for Simulations

A2.1 Section 5.1

```
clear all;
close all;
f = logspace(0,8,3000);

%Single (Dominant) Pole Op-Amp
Ao = 1e5;
fT = 12e6;
tr = 0.35/fT;
SR = 4/tr;
fpole = fT*10^(-log10(Ao));
polecoeff = 1/(2*pi*fpole);
hs = Ao./(1+j*f/fpole);
hsmag = 20*log10(abs(hs));

%Doublet at 1MHz
%Mismatch Factor = 2
fdb = 1e6;
mf = 2;
%Case #1:
%Matched Pair
fpzcoeff = 1/(2*pi*fdb);
dbm = (1+j*f/fdb)./(1+j*f/fdb);
%Case #2:
%Freq Zero > Freq Pole
fpole1 = fdb/mf;
fzero1 = fdb*mf;
fp1coeff = 1/(2*pi*fpole1);
fz1coeff = 1/(2*pi*fzero1);
dbzp = (1+j*f/(fdb*mf))./(1+j*f/(fdb/mf));
%Case #3:
%Freq Pole > Freq Zero
fpole2 = fdb*mf;
fzero2 = fdb/mf;
fp2coeff = 1/(2*pi*fpole2);
fz2coeff = 1/(2*pi*fzero2);
dbpz = (1+j*f/(fdb/mf))./(1+j*f/(fdb*mf));
%Doublet at 250kHz
%Mismatch Factor = 2
fdb1 = 250e3;
fpole3 = fdb1/mf;
fzero3 = fdb1*mf;
fp3coeff = 1/(2*pi*fpole3);
fz3coeff = 1/(2*pi*fzero3);
%Doublet at 1MHz
%Mismatch Factor = 1.5
%Freq Zero > Freq Pole
mflo = 1.5;
fpole4 = fdb/mflo;
fzero4 = fdb*mflo;
fp4coeff = 1/(2*pi*fpole4);
fz4coeff = 1/(2*pi*fzero4);
```

```matlab
sim('simu1')

l = length(vi);
for i = 0:l-1
    if abs(vo1(l-i)-5) >= 0.005
        tsett1 = tout(l-i)*1e6;
        vsett1 = vo1(l-i);
        break
    end
end

for i = 0:l-1
    if abs(vo2(l-i)-5) >= 0.005
        tsett2 = tout(l-i)*1e6;
        vsett2 = vo2(l-i);
        break
    end
end

for i = 0:l-1
    if abs(vo3(l-i)-5) >= 0.005
        tsett3 = tout(l-i)*1e6;
        vsett3 = vo3(l-i);
        break
    end
end

for i = 0:l-1
    if abs(vo4(l-i)-5) >= 0.005
        tsett4 = tout(l-i)*1e6;
        vsett4 = vo4(l-i);
        break
    end
end

for i = 0:l-1
    if abs(vo5(l-i)-5) >= 0.005
        tsett5 = tout(l-i)*1e6;
        vsett5 = vo5(l-i);
        break
    end
end

figure(1)
subplot(2,1,1)
semilogx(f,20*log10(abs(hs.*dbm)),f,20*log10(abs(hs.*dbzp)),f,20*log10(
    abs(hs.*dbpz)))
ylabel('Gain [dB]')
grid on
legend('f_Z_e_r_o = f_P_o_l_e','f_Z_e_r_o > f_P_o_l_e','f_Z_e_r_o <
    f_P_o_l_e')
title('Bode Plots of The Systems (Doublet at 1MHz)');
subplot(2,1,2)
semilogx(f,angle(hs.*dbm)*180/pi,f,angle(hs.*dbzp)*180/pi,f,angle(hs.*d
    bpz)*180/pi)
ylabel('Phase [Degree]')
xlabel('Frequency [Hz]')
```

```
grid on

figure(2)
subplot(2,1,1)
plot(tout*1e6,vo1,tout*1e6,vo2,tout*1e6,vo3)
legend('f_Z_e_r_o = f_P_o_l_e','f_Z_e_r_o > f_P_o_l_e','f_Z_e_r_o <
    f_P_o_l_e')
title('Pulse Response of the Systems (Doublet at 1MHz): Pole-Zero
    Separation vs. Settling Time');
axis([0 2 0 6])
xlabel('Time [us]')
grid on;
subplot(2,1,2)
plot(tout*1e6,vo1,tout*1e6,vo2,tout*1e6,vo3,tsett1,vsett1,'r+',tsett2,v
    sett2,'r+',tsett3,vsett3,'r+')
tset1=strcat('{\bf',sprintf('%g',tsett1),' us}');
text(tsett1+0.02,vsett1-0.00125,tset1,'color',[0.1 0 0.8]);
tset2=strcat('{\bf',sprintf('%g',tsett2),' us}');
text(tsett2+0.02,vsett2-0.00125,tset2,'color',[0.1 0 0.8]);
tset3=strcat('{\bf',sprintf('%g',tsett3),' us}');
text(tsett3+0.02,vsett3-0.00125,tset3,'color',[0.1 0 0.8]);
legend('f_Z_e_r_o = f_P_o_l_e','f_Z_e_r_o > f_P_o_l_e','f_Z_e_r_o <
    f_P_o_l_e')
axis([0 2 4.98 5.02])
xlabel('Time [us]')
grid on;

figure(3)
subplot(2,1,1)
plot(tout*1e6,vo2,tout*1e6,vo4)
legend('Doublet at 1MHz','Doublet at 250kHz')
title('Pulse Response of the Systems: Doublet Frequency vs. Settling
    Time');
axis([0 2 0 6])
xlabel('Time [us]')
grid on;
subplot(2,1,2)
plot(tout*1e6,vo2,tout*1e6,vo4,tsett2,vsett2,'r+',tsett4,vsett4,'r+')
text(tsett2+0.02,vsett2-0.00125,tset2,'color',[0.1 0 0.8]);
tset4=strcat('{\bf',sprintf('%g',tsett4),' us}');
text(tsett4+0.02,vsett4+0.00125,tset4,'color',[0.1 0 0.8]);
legend('Doublet at 1MHz','Doublet at 250kHz')
axis([0 2 4.98 5.02])
xlabel('Time [us]')
grid on;

figure(4)
subplot(2,1,1)
plot(tout*1e6,vo5,tout*1e6,vo2)
legend('Separation Factor of 1.5','Separation Factor of 2')
title('Pulse Response of the Systems: Doublet Separation Factor vs.
    Settling Time');
axis([0 2 0 6])
xlabel('Time [us]')
grid on;
subplot(2,1,2)
plot(tout*1e6,vo5,tout*1e6,vo2,tsett5,vsett5,'r+',tsett2,vsett2,'r+')
```

```
text(tsett2+0.02,vsett2-0.00125,tset2,'color',[0.1 0 0.8]);
tset5=strcat('{\bf',sprintf('%g',tsett5),' us}');
text(tsett5+0.02,vsett5+0.00125,tset5,'color',[0.1 0 0.8]);
legend('Separation Factor of 1.5','Separation Factor of 2')
axis([0 2 4.98 5.02])
xlabel('Time [us]')
grid on;
```

A2.2 Section 5.3

```matlab
clear all;
close all;

%s = tf('s');
%
%f1 = 245000;
%f2 = 1.6e9;
%f3 = f2;
%f4 = 1.7e9;
%f5 = f4;
%ad8007 =
    800/((1+s/(2*pi*f1))*(1+s/(2*pi*f2))*(1+s/(2*pi*f3))*(1+s/(2*pi*f4))
    *(1+s/(2*pi*f5)));

fdoublet1 = 150e6;
m1=1/1.3;
fpole1 = fdoublet1/m1;
fzero1 = fdoublet1*m1;
fpole1coeff = 1/(2*pi*fpole1);
fzero1coeff = 1/(2*pi*fzero1);
%doublet1_tf = (1+s/(2*pi*fzero1))/(1+s/(2*pi*fpole1));

fdoublet2 = 80e6;
m2=1/1.2;
fpole2 = fdoublet2/m2;
fzero2 = fdoublet2*m2;
fpole2coeff = 1/(2*pi*fpole2);
fzero2coeff = 1/(2*pi*fzero2);
%doublet2_tf = (1+s/(2*pi*fzero2))/(1+s/(2*pi*fpole2));

sim('simu2');
time = load('meas1.csv');
meas = load('meas2a.csv');
meassett = -0.05*load('meas3a.csv');

l = length(vo);
vsettle = vo(l);
for i = 0:l-1
   if abs(vo(l-i)-vsettle) >= 0.005
      tsettle = tout(l-i)*1e9;
      break
   end
end

for j = 0:l-1
   if vi(l-j) >= 4.6712
      tstart = tout(l-j)*1e9;
      break
   end
end

l1 = length(meassett);
for k = 0:l1-1
   if abs(meassett(l1-k)) >= 0.005
```

```matlab
        tsettbench = time(l1-k);
        break
    end
end

subplot(2,1,1);
plot(tout*1e9-145,vi,tout*1e9-145,vo,time,meas-meas(l1),tstart-
    145,vi(l-j),'ro',tsettle-145,vo(l-i),'ro');
xlabel('Time [ns]');
ylabel('Voltage [V]');
legend('V_I_N','V_O_U_T','Bench Measurement');
graphtitle=strcat('{\bf','{Simulation of 0.1% Settling Time is
    }',sprintf('%g',tsettle-tstart),'ns}');
title(graphtitle);
tsrt=strcat('{\bf',sprintf('%g',tstart-145),' ns}');
text(tstart-145,vi(l-j)+0.25,tsrt,'color',[0.1 0 0.8]);
tset=strcat('{\bf',sprintf('%g',tsettle-145),' ns}');
text(tsettle-145,vo(l-i)+0.25,tset,'color',[0.1 0 0.8]);
axis([tout(l)*1e9-145-50 tout(l)*1e9-145 -2 6]);
grid on;

subplot(2,1,2);
plot(tout*1e9-145,vo,time,meassett,'r',tsettle-145,vo(l-
    i),'ro',tsettbench,meassett(l1-k),'ro');
xlabel('Time [ns]');
ylabel('Settling [0.1%/div]');
legend('V_O_U_T','Bench Measurement');
graphtitle2=strcat('{\bf','{Output settles in to 0.1% at
    }',sprintf('%g',tsettle-145),'ns}');
title(graphtitle2);
tset2=strcat('{\bf',sprintf('%g',tsettle-145),' ns}');
text(tsettle-145,vo(l-i)+0.0025,tset2,'color',[0.1 0 0.8]);
tsetbench=strcat('{\bf',sprintf('%g',tsettbench),' ns}');
text(tsettbench,meassett(l1-k)+0.0025,tsetbench,'color',[0.1 0 0.8]);
axis([tout(l)*1e9-145-50 tout(l)*1e9-145 vsettle-0.005*3
    vsettle+0.005*3 ]);
grid on;
```