Variable Planar Inductor
Major Qualifying Project

A Major Qualifying Project Report submitted to the faculty of the Electrical and Computer Engineering Department at Worcester Polytechnic Institute in partial fulfillment of the requirements for the Degree of Bachelor of Science

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Executive Summary

The Variable Planar Inductor Major Qualifying Project set out to design and test a variable planar inductor that operates in a similar fashion to a potentiometer.

Planar inductors are constructed by overlaying copper windings onto printed circuit board (PCB), which can be stacked as many times as desired. It is then surrounded by a core made of a ferrous material. The team decided to model a planar inductor because a planar type can be sized down to take up less space. Additionally, it can be rated for the same current with a better inductance value compared to a coil inductor. The planar type also allowed the team to vary inductance by changing the core's airgap length. This inductor can be used in common circuit applications such as filters and DC-DC power converters.

To begin, a one-layer planar inductor with three turns was first modeled with Ansys Maxwell. After this model was created, with the same physical specifications as the ferrite cores the team would later use, the team ran a series of simulation tests. This simulation modeled the top half of the ferrite core moving up from 0µm (flush with the bottom half of the core), to 100µm. The core was moved in increments of 5µm, and the program measured the inductance value at each airgap length. After understanding what behavior is expected, the team then modeled a multi-layer planar inductor. This model consisted of five layers with three turns each, equivalent to a fifteen-turn inductor. The same simulation parameters were implemented where the top half of the ferrite core was moved up from 0µm to 100µm in increments 5µm. After successfully running and analyzing data from both tests, the team translated the simulation design to a physical prototype. The team used Altium Designer to design both the one-layer and the multi-layer planar inductors on PCB. The multi-layer planar inductor was unable to be fabricated with the five layers were already combined due to price and time constraints. Instead, the team designed five separate layers and then manually soldered them together once delivered.

After receiving and assembling both styles of planar inductors from the manufacturer, physical testing was implemented. Two procedures were created to determine if a variable planar inductor could produce viable or usable data. The first procedure measured the inductance generated as the airgap length between the top and bottom half of the core is increased. The test measured every 10µm from 0µm to 100µm. This test was performed for the one-layer and multi-layer planar inductors as done in simulation. The second procedure implemented the multi-layer planar inductor into a lowpass filter, a highpass filter. This test increased the airgap until the cutoff

frequency, f3dB, was reached, and recorded frequency pushed into the circuit. The inductor was also implemented in a boost converter to test if it would be viable for power applications.

Both procedures confirmed that a multi-layer variable planar inductor operates as expected, with a margin of error. Results show the data from the physical model matched the simulated and mathematical data with slight variations. These variations were attributed to potential sources of error in operating the airgap variation rig, soldering, chipped ferrite cores with large tolerance variations for dimensions and permeability measurements.

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Abstract

The purpose of this Major Qualifying Project was to understand the relationship between core airgap length and inductance. This knowledge was used to create a tunable inductor that operates similarly to a potentiometer. This inductor could be integrated into real world applications, such as filters and DC-DC power converters. It allows the capability to adjust inductance values without replacing the inductor. The team modeled and built a five-layer tunable planar inductor to test this concept. The process started with research into planar inductors and their applications. The team then modeled and simulated 3-D single and multi-layer inductors using Ansys Maxwell. Finally, the team designed and fabricated multiple printed circuit board (PCB) planar inductors and tested them through multiple procedures in a lab setting.

1.0 Introduction

Inductors are important components that have numerous uses in electronics. They are utilized in applications such as machinery that involves motors, transformers, and any other appliance that deals with ferro-magnetic influences [15]. A challenge that designers and manufacturers can face is that once an inductor is made, the inductance value is set and cannot be changed unless it were to be replaced with an entirely new inductor. Additionally, in many applications, circuits could require different inductance values for different loads [9]. Having a variable inductor could be beneficial in applications such as filters and DC-DC power converters.

Having to account for the possibility of replacing an inductor can waste time, money, and resources. Currently, there are no applications that can accommodate the ability to change inductance values on demand [10]. A potential solution is to take advantage of the relationship between inductance values and the length of the airgap. This can be achieved by considering how a planar inductor is designed. The following image shows how planar inductors are typically constructed. Observe spiral copper traces on non-permeable FR4 encased in a ferrite core in the figure below.

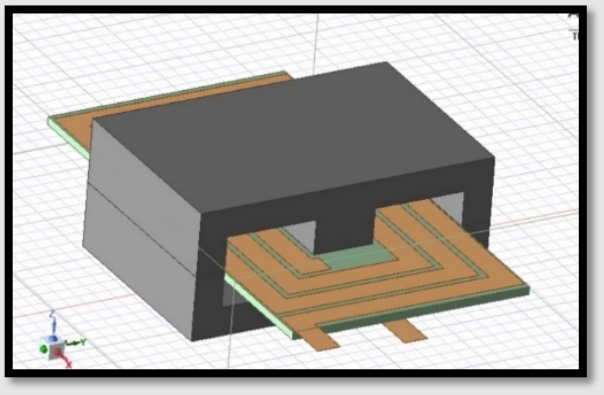

Figure 1: Planar Inductor.

Over the 2023 to 2024 academic year, the team developed a planar inductor model and then produced and evaluated it to determine its effectiveness. The benefits of creating an inductor model that has similar functionality to a potentiometer are that resources such as time and money could be conserved, the design process could take less time, and it would be easier for both engineers and whomever is using the design to application to change the use or purpose of the overall design.

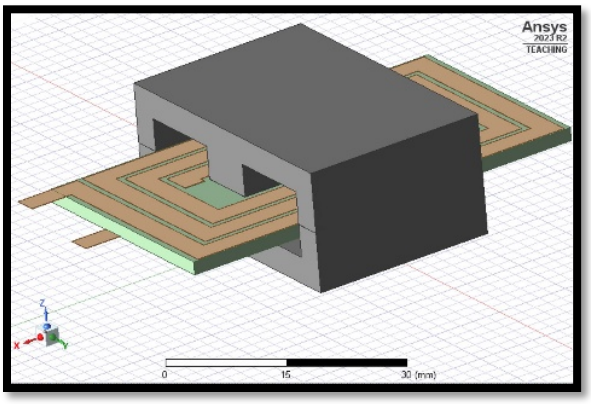

Figure 2: Planar Inductor.

The team decided to take this project on because of the lack of research on variable inductors, unlike the prolific use of potentiometers. The team saw a great amount of potential for the usefulness of the design and its applications. There was also an interest in seeing if the completed design could be useful for professional designers and others who rely on inductors as integral components in their devices or machines.

2.0 Background

2.1 Introduction to Inductors

An inductor is a passive machine or component used in electrical circuits and other electrical applications. Inductors store magnetic energy as current passes through a circuit and releases this energy when the current flow has stopped.

$$V = L \cdot \left(\frac{dI}{dt}\right)$$

Equation 1: Inductance, L, relates the voltage, V, to the changing current, I, over time [4].

Magnetic energy within a circuit is important because it dictates the strength and direction of the flow of magnetic flux within a ferromagnetic core of an inductor, or any device that employs the use of one, such as a motor [13]. The most common type is called a coil inductor and is constructed by winding wire around an iron core, which creates an electro-magnetic field (Figure 3). The number of windings in the coil can influence how inductive this component is, along with other environmental factors [15]. Because of its ability to store and discharge magnetic energy and flux when a circuit is not attached to a power source, inductors are often used in the design of DC-DC power converters.

$$L = N\frac{\Phi}{I}$$

Equation 2: Equation for Inductance, L, based on N turns, change in flux, Φ, and change in current, I.

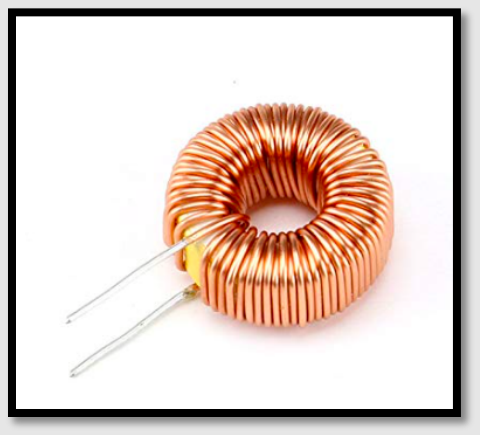

Figure 3: Coil Inductor.

2.2 Planar Inductors

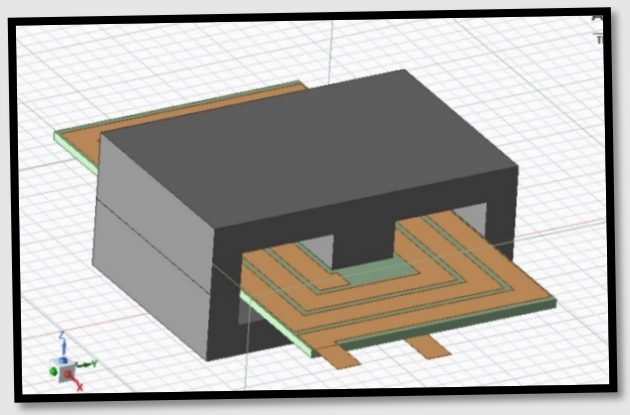

Figure 4: Planar Inductor.

Planar inductors follow the same concepts as coil inductors, as outlined in the last section, but with different design configurations. Rather than helical windings found on coil inductors, windings on planar inductors are found on flat surfaces [3]. Core shapes are also different on planar inductors compared to coil inductors (Figure 4). Planar inductors can be used in applications where geometric constraints limit the available design volume. Planar magnetic components are also used in applications where high frequencies are expected to occur, and when high density power is expected to be generated such as in military, aviation, and industrial applications. Planar magnetic inductors are often used because unlike traditional power source components, they have power losses that typically amount to less than 30%. These can be used in machines such as a Boost-Buck integrated LLC converter [11].

A big difference between coil and planar inductors is the amount of space they can take up. While each type can be scaled up or down depending on the application or the size of the machine it would be integrated into, planar inductors could be built on a flat plane. This is advantageous for many applications because building and testing the inductor will be a much less time-consuming, and less expensive task. Unlike coil inductors, the airgap between the core halves in a planar inductor can be varied. Additionally, planar inductors have excellent repeatability as the planar windings on flat surfaces eliminate variation from wire winding that can be found in coil inductors [3].

2.2.1 Core

Inductors are designed with cores that tend to be composed of magnetic material with high magnetic permeability, μ. An effective magnetic core permeability is much greater than the permeability of free space, μ_0. Two common core materials are steel and iron.

$$\mu_0 = 4\pi * 10^{-7} \text{ [H/m]}$$

Equation 3: Permeability of free space.

A core is of uniform cross section and is excited by N turns of windings that carry a current, I. These windings produce a magnetic field in the core. Because the cross-sectional area is uniform, the flux density, B, is essentially uniform as well.

Magnetic cores for planar inductors have different shapes than cores found in conventional coil inductors with helical windings. Cores tend to have a reduced height and greater surface area [2]. The team considered two common core configurations used in PCB applications of trace windings EE and EI cores.

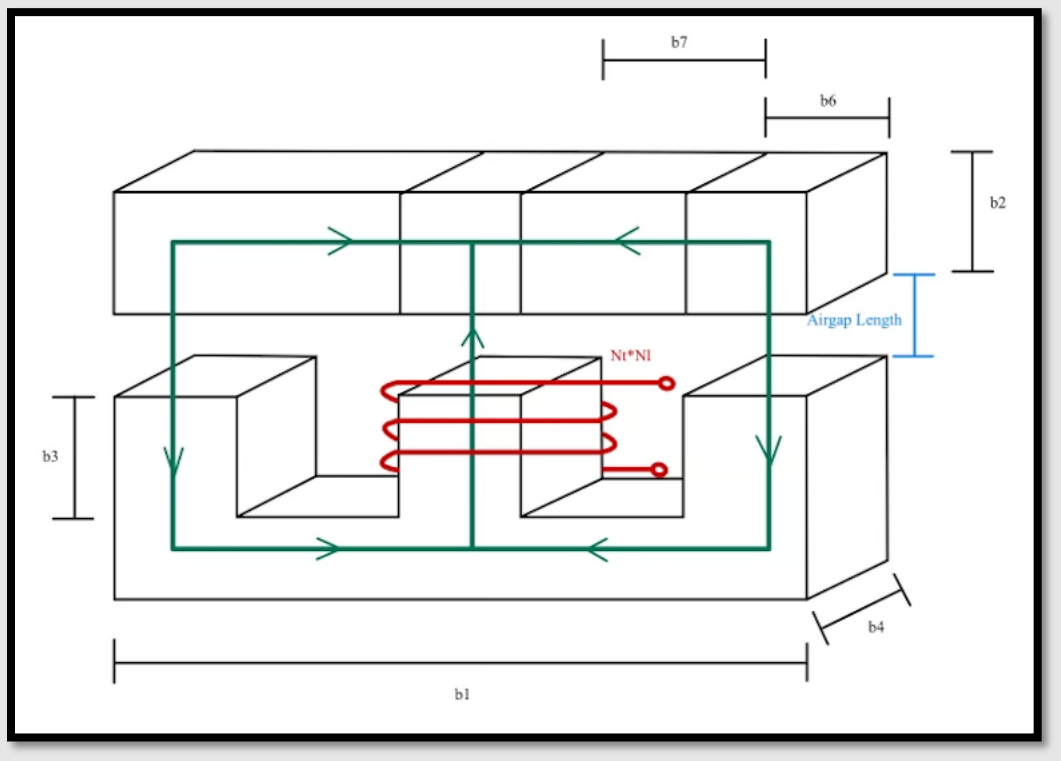

Figure 5: EI Core Configuration.

EI cores, shown as one 'E' and one 'I' shaped core stacked in Figure 5, are configured with PCB windings encased between the two cores. See Table 2 for measurement values. The two cores are not bound together, rather the team is evaluating the inductor with various airgap lengths. Thus,

where the two cores meet, the airgap between the two cores can be increased or decreased in simulation and in experimentation with a rig that can clamp to the core and vary the gap length at a precise value. This makes the EI core a viable configuration for this project.

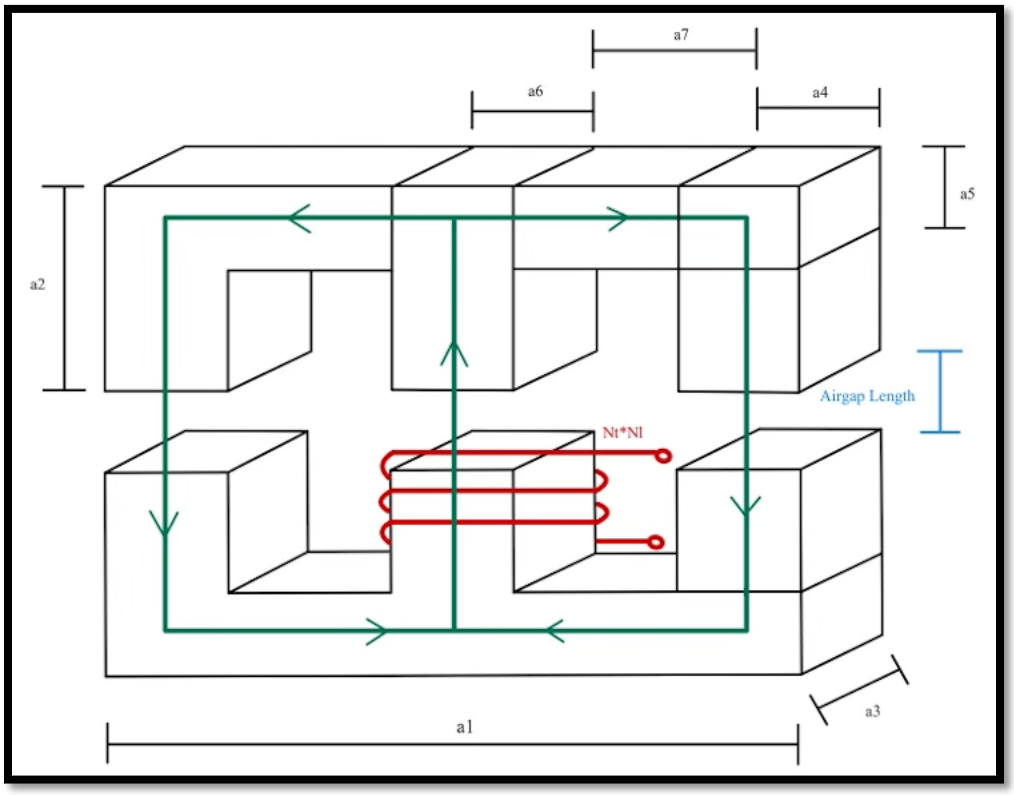

Figure 6: EE Core Configuration.

EE cores, shown as two ‘E’ shaped cores stacked in Figure 6 are configured with PCB windings encased between the two cores. See Table 1 for measurement values. Like the EI configuration, the two cores are not bound together, rather the team is assessing the inductor with various airgap lengths. Thus, where the two cores meet, the airgap between the two cores can be increased or decreased in simulation and experimentation with a rig that can clamp to the core and vary the gap length at a precise value. This also makes the EE core a viable configuration for this project.

Both configurations can be used to design an effective planar inductor, however one configuration may prove to be more beneficial. This will be based on simulation results of the two core configurations and ultimately the teams’ decision on final design.

2.2.2 Windings

Planar inductors are often constructed on PCB with copper traces as windings and FR4 as an insulator between winding traces. Different to traditional inductors, planar inductor windings are in the Z direction in a PCB, opposed to the helical windings in the X-Y direction in coil inductors (compare Figure 3 and Figure 4). The inductance value of a planar inductor fabricated on a PCB depends on number of turns, N, trace width, trace separation, and inner and outer winding diameter. After the core configuration and desired inductance are determined, copper traces of calculated width and separation can determine the number of turns required in the inductor. Trace windings can be laid out in different types (Figure 7) [8].

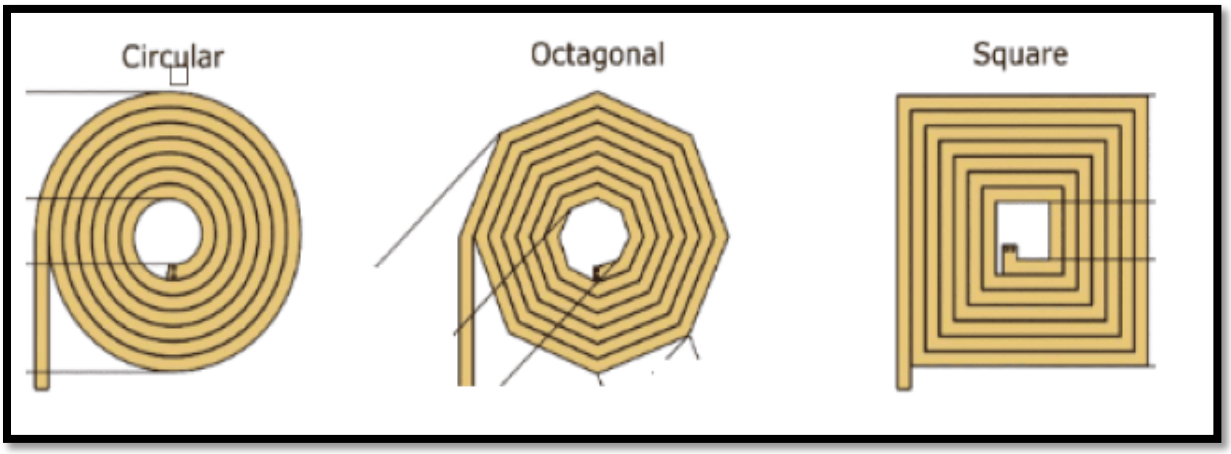

Figure 7: Types of PCB Windings.

Windings of multiple turns can be modeled on PCB as multiple layers connected by vias. Vias are used to transition signals between layers. One type of via is called a through-hole via. These vias are drilled in the PCB connected by pads on each layer where a connection is made to the trace. Buried vias are placed in between multilayer PCB. Figure 8 shows the different types of vias that can be used in multilayer PCB [8].

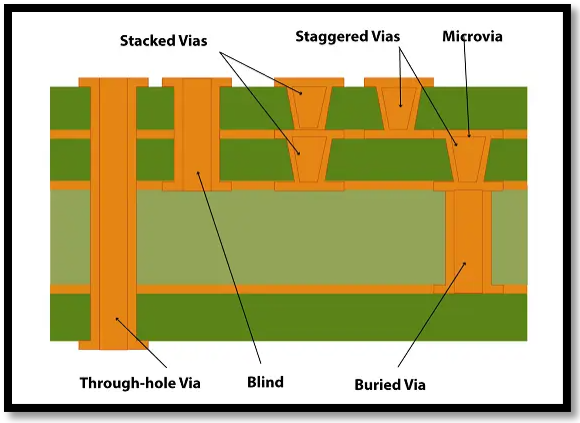

Figure 8: Vias.

Determining the type of via depends on the cost and availability, as many PCB manufacturers either do not offer services for blind and buried vias or have large price requirements [7].

2.2.3 Magnetic Circuits

Using trace windings encased in a highly permeable core results in the structure of a magnetic circuit. The presence of this core allows magnetic flux, ϕ, to be mostly confined to the paths within the core structure [14]. This is like how currents are confined to conductors of an electric circuit. Continuing with the assumption that the cross-sectional area, A, of the core is uniform, which is true in an ideal core scenario, the flux density, B, is essentially unform as well [14].

$$\phi = B * A \text{ [Wb]}$$

Equation 4: Flux Equation.

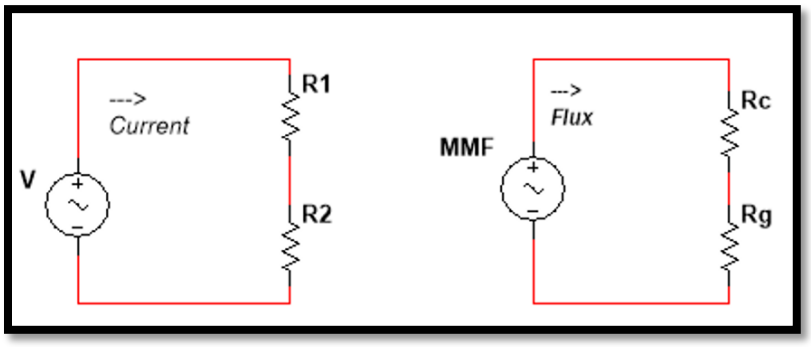

Figure 9: Circuit.

In electrical circuits, voltage sources drive currents through resistance. Analogously, in magnetic circuits the magnetomotive force, $\mathcal{F}$, drives a flux through reluctances of the core [14].

This can be seen in Figure 9. The magnetomotive force, or shortened as MMF, is found in terms of flux and reluctance like Ohm's Law in electrical circuits [14].

$$V = IR_{total}$$
$$\mathcal{F} = \phi(\mathcal{R}_{core} + \mathcal{R}_{gap})$$

Equation 4 and 5: Voltage and Magnetomotive Force.

Reluctance in the core is determined using the mean path length, l_c, the permeability of the core, μ_{core}, and the cross-sectional area of the core, A_{core}. The mean flux path length, l_c, is the length of travel of the flux from the center of the core [14]. This length of travel also assumes an ideal core.

$$\mathcal{R}_{core} = \frac{l_c}{\mu_{core} * A_{core}}$$
$$\mu_{core} = \mu_0 * \mu_r$$

Equation 6 and 7: Reluctance and Permeability.

The MMF can also be found in terms of winding, N, and current, I. It can also be determined in terms of the magnitude of the magnetic field intensity, H, in the core and airgap and the mean flux path length, l_c and airgap length [14].

$$\mathcal{F} = Ni \text{ [A*Turns]}$$

Equation 8: Magnetomotive Force.

The magnetic field intensity can be determined through the right-hand rule, figuratively using the right hand to 'grasp' the coil [14]. The thumb indicates the direction of the magnetic field. The relationship between the magnetic field intensity, H, and the magnetic flux density, B is a property of the material in which the field exists [14].

$$B = \frac{\phi}{A_c} = \mu_{core} H$$
$$\mu_{core} = \mu_0 * \mu_r$$

Equation 9 and 10: Magnetic Flux Density and Permeability.

According to Faraday's Law, the line integral of the electric field intensity, E, around a closed contour, C, is equal to the time rate of change of the magnetic flux linking that contour [14].

$$\oint_c E \cdot dl = -\int_{-\infty}^{\infty} \left(\frac{\partial B}{\partial t}\right) \cdot ds$$

Equation 11: Faraday's Law.

In magnetic structures with windings of high electrical conductivity, as in a planar inductor, the E field in the wire is small and negligible. The left side of the equation is reduced to the

electromotive force (emf), e, at the winding terminals [14]. The instantaneous value of a time-varying flux is denoted as φ and the flux linkage of the winding as λ. Flux linkage is the flux, ϕ, multiplied by the number of turns, N. Thus, Faraday's Law is reduced to:

$$\mathrm{e} = N\frac{d\varphi}{dt} = \frac{d\lambda}{dt}$$

Equation 12: Faraday's Law.

In a magnetic circuit composed of magnetic material of constant magnetic permeability, or which includes an airgap, the relationship between flux linkage, λ and current is linear. Inductance, L, is defined below [14].

$$L = \frac{\lambda}{i} = \frac{N^2}{\mathcal{R}_{total}}\,[\mathrm{H}]$$

Equation 13: Inductance.

2.2.4 Magnetic Circuits with Airgaps

This project focuses on varying the airgap length of the inductor cores. When an airgap length, g, is smaller than the dimensions of the adjacent core faces, the flux in the core, ϕ, will follow the path defined by the core and the airgap using the techniques outlined in the Magnetic Circuits section (Section 2.2.3) [14]. If the airgap becomes too large the flux will 'leak' out of the sides of the airgap, causing field fringing [14].

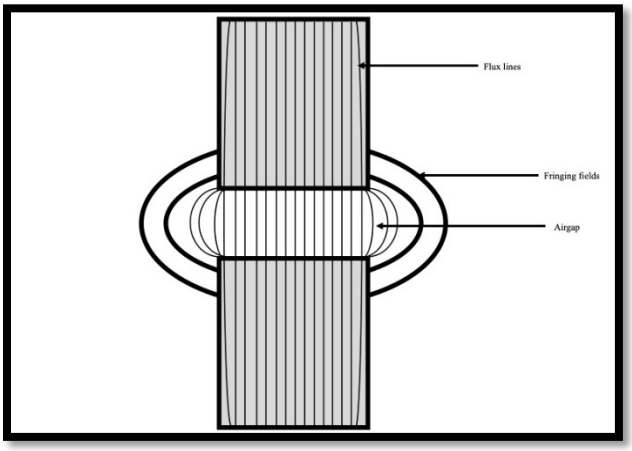

Figure 10: Fringing.

Figure 10 indicates the fringing effect across an airgap in a magnetic circuit. Flux lines bow outward from the airgap which makes the effective area of the gap larger than the area of the core. Fringing is accounted for, mathematically, with airgaps by adding the length of the gap to each dimension of cross-sectional area [14].

$$A_{gap} = \left(length + \ l_{gap}\right) * (width + l_{gap})$$

Equation 14: Area of Airgap with Fringing.

The reluctance of the airgap, $\mathcal{R}_{gap}$, is determined with the length of the airgap, g, the permeability of the gap, μ_{gap}, and the area if the gap with fringing accounted for, A_{gap}. The permeability of the gap is free space, μ_0 [14].

$$\mathcal{R}_{gap} = \frac{g}{\mu_{gap} * \ A_{gap}}$$

$$\mathcal{R}_{gap} = \frac{g}{\mu_0 * A_{gap}} \text{ [A*Turns/ Wb]}$$

Equation 15 and 16: Reluctance of Airgap.

Under the assumption that the permeability of free space, μ_0 is far smaller than the permeability of the core, the reluctance of the core can be considered negligible as compared to the airgap, g, the inductance of the winding is:

$$L = \frac{N^2 \mu_0 A_{gap}}{g} \text{ [H]}$$

Equation 17: Inductance.

2.3 Planar Inductor Design

When designing a planar inductor, there are constraints that must be considered. These include the size of the PCB board and its thermal limits, the required inductance values and the time and cost of production. The size cannot exceed the constraints of the PCB board. If the design goes beyond the constraints, it could affect the cost and the production time of the inductor.

The inductor must be sized appropriately so that they are both functionally efficient. This will also influence the budget and production time. It's also important to consider the thermal limits of the design. If the build exceeds the thermal limit of the PCB material, there is risk destroying the device. It's also possible to exceed the thermal limit for the materials that make up the inductor. In this case, the production time and costs would increase greatly.

2.3.1 Thermal Considerations

Thermal management focuses on effectively managing and removing heat to control the temperature of a device [20]. Regarding a high-power, high current planar inductor, effective thermal management strategies lead to 2.5 to 3 times higher peak power in comparison to standard

solutions [21]. Improving thermal management is important during the design process to enable size reduction and increase performance [21].

Planar inductors at low current and voltage have an advantage regarding thermal management due to their high surface-area-to-volume ratio [21]. However, in high-power planar inductors, where current is higher, thermal management can prove to be a challenge. Potential solutions are the introduction of direct thermal interfaces in-between windings and heat sink, or to directly print windings onto a cold plate [6]. Each solution comes with a disadvantage as effective thermal management for high-power planar inductors has not been created [21].

For a PCB, the copper trace width has a thermal impact. Trace thickness must provide a low impedance path for the current to reduce heat generation. Heat reduction for copper traces on a PCB can be implemented with vias. Vias help dissipate heat in the board. In the case of smaller boards, a thick board with a proportionally larger surface area can allow heat to dissipate quickly [6].

2.3.2 Losses

Winding loss can occur within inductors. These losses encompass resistive losses of the wire, typically made of copper, and the losses that occur in the airgap(s) within the physical structure. Winding losses are mainly due to excess flux creating electro-magnetic fields outside of the machine or circuit that draw flux away from its intended path through the core. This can typically be fixed by increasing the number of windings so that the flux loss is negated. Increasing the windings, however, can sometimes increase the overall inductance which would then have to be fixed by adding more resistive components to balance out the system [12].

2.4 Planar Inductor Applications

2.4.1 DC-DC Converters

A boost converter is a DC-to-DC converter that performs a step-up conversion on the input voltage. The purpose is to take an input volage and obtain a greater output voltage per the requirement of the load and to regulate the output [5]. Boost converters have a variety of applications where the load requires a step-up conversion from the input voltage. A specific example of a planar inductor application is that they have been used as an energy storage element in a very small DC-DC converter [7]. Boost converters are common in photovoltaic applications

since input voltage from solar panels can change due to varying weather conditions and solar energy [19]. Boost converters also have applications in automotives, battery power and consumer electronics [17].

A boost converter must be sized appropriately so that they are both functionally efficient. This will also influence the budget and production time. It's also important to consider the thermal limits of the design. If the build exceeds the thermal limit of the PCB material, there is risk destroying the device. It's also possible to exceed the thermal limit for the materials that make up the boost converter. In either of these cases, the production time and costs would increase greatly.

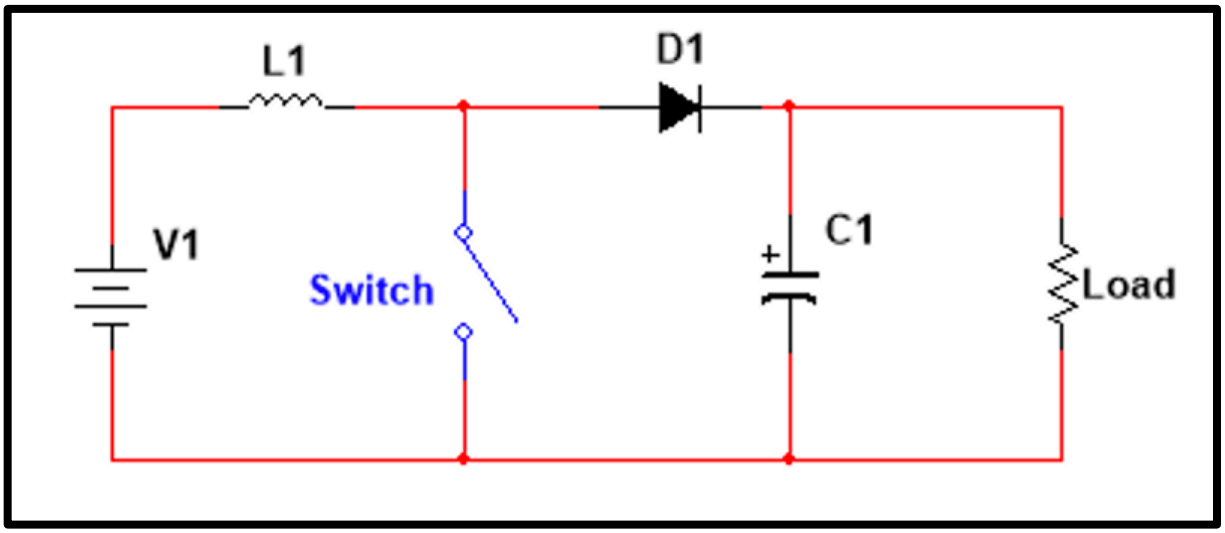

Figure 11: Boost Converter.

A buck converter is a DC-to-DC converter that performs a step-down conversion on the input voltage. The purpose is to take an input volage and obtain a lower output voltage per the requirement of the load and to regulate the output. Buck converters are used in applications where voltage needs to decrease very quickly and drastically, or where input voltage needs to be precise and efficient. Buck converters are used in sophisticated electrical equipment, like controls systems found in aircrafts, because it is primarily used to ensure voltages from the DC power source, such as a battery or other independent source, are consistent [18].

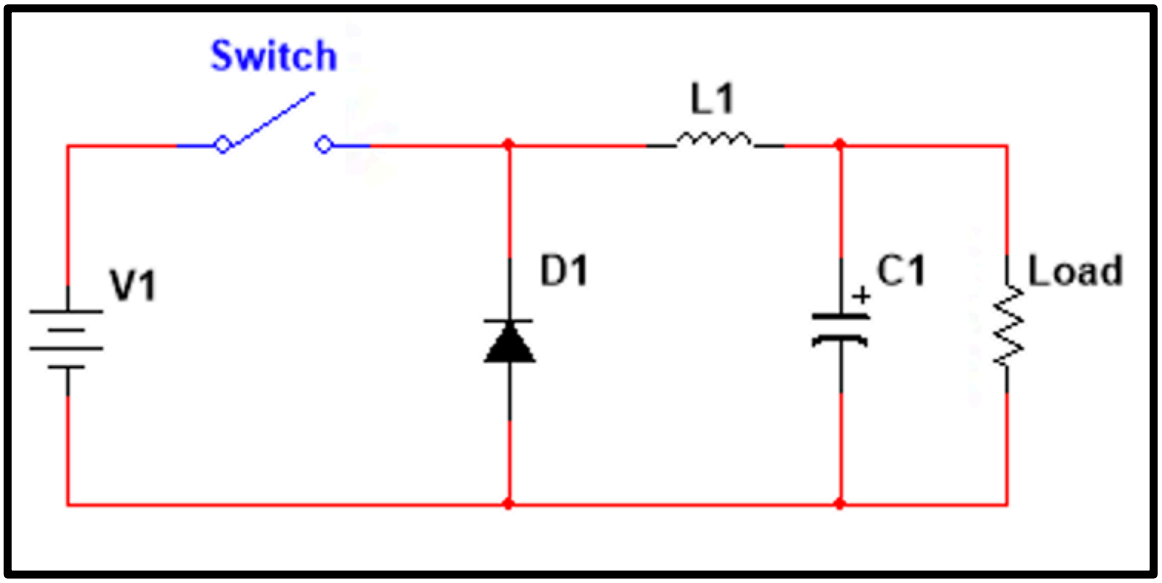

Figure 12: Buck Converter.

2.4.2 Filters

Lowpass and highpass filters generate a frequency response based on a 3dB frequency, also known as a cutoff frequency, and the desired output. Lowpass filters allow frequencies below the 3dB frequency to pass through the circuit and be included in the output response. Highpass filters do the opposite. A lowpass RL filter can be configured such that the current will pass through the inductor first, and then the resistor (Figure 13). The opposite is true for a highpass filter, where the circuit is configured such that the current flows through the resistor first and the inductor second (Figure 15).

2.4.2.1 Lowpass Filters

Lowpass filters operate such that they will only allow low frequencies to pass through to the remainder of the circuit. They are generally useful for systems that operate on lower frequencies that want to prevent noise, or excess or unnecessary signal data, from interfering with the output data [15].

The team will use a lowpass filter in one testing scenario to understand how the behavior of the filter is affected by a variable planar inductor. In this test, the team will understand how changing airgap and inductance values will affect the filters cut off frequency.

Figure 13 shows what a lowpass filter looks like when it is configured with an inductor and a resistor. The next figure, Figure 14, shows an AC sweep of a simulated filter and the resulting

graphs. In both graphs, one can see how both the magnitude of the resulting output and the phase changes as the frequency increases from 0Hz to 10GHz.

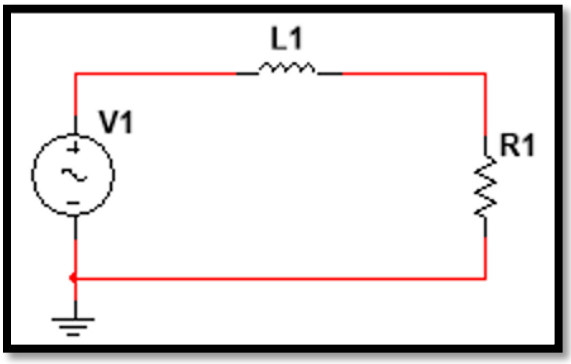

Figure 13: An RL (resistor and indictor) lowpass circuit.

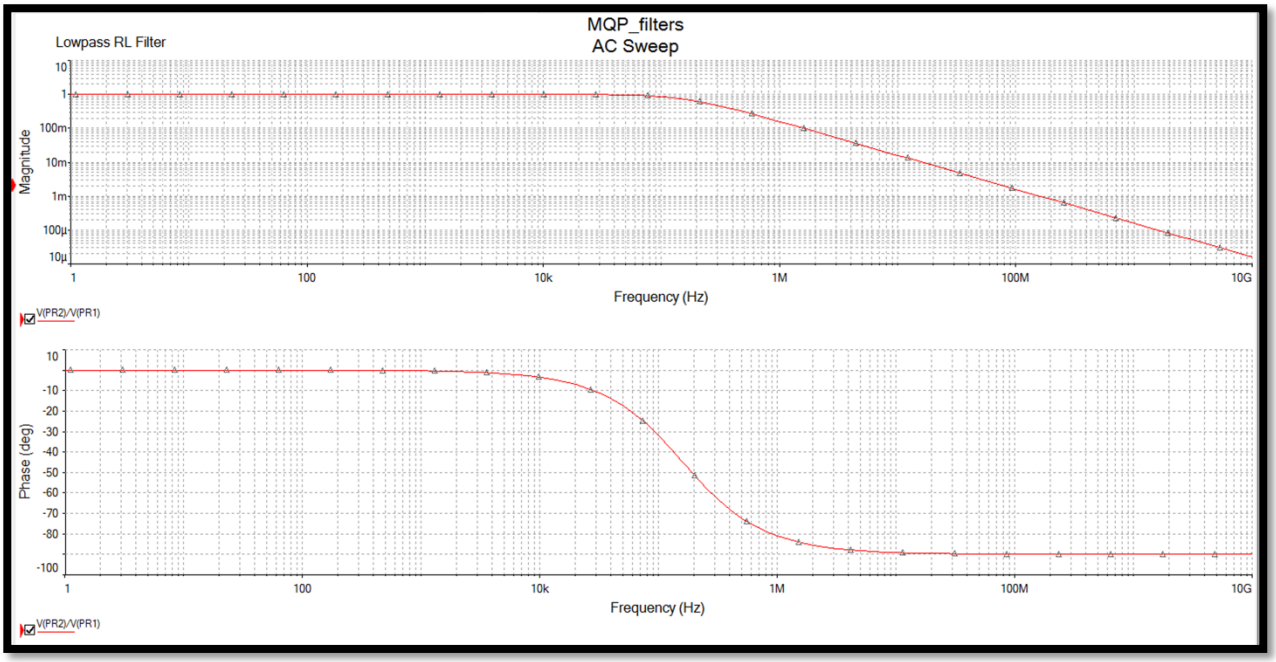

Figure 14: Magnitude and Phase frequency response of a lowpass filter.

2.4.2.2 High pass Filters

Conversely, highpass filters operate in a fashion that permits higher frequencies to pass through to the remainder of the circuit. They are used in systems where larger signal frequencies are acceptable to be processed, and where any frequency lower than the cut-off, or 3dB frequency, is noise [15].

Similarly, to the purpose of testing the team's inductor with a lowpass filter, the purpose of performing experiments with a highpass filter is to understand how airgap length and inductance affect the cut off frequency of the filter.

The figure below, Figure 15, depicts the circuit configuration of a highpass filter with a resistor and an inductor. Comparing this figure to the one above, Figure 13, the resistor and inductor are in opposite places. Figure 16 shows the magnitude and phase response to how frequency changes from 0Hz to 10GHz.

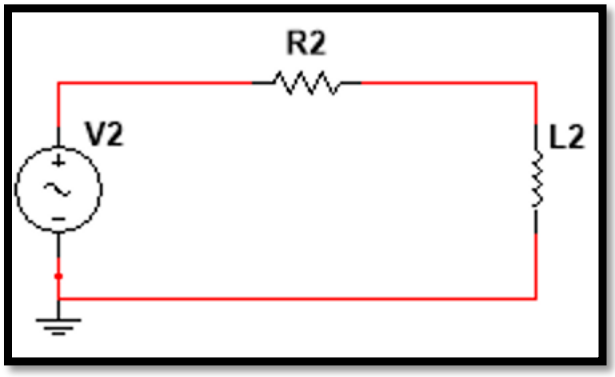

Figure 15: An RL (resistor and inductor) highpass circuit.

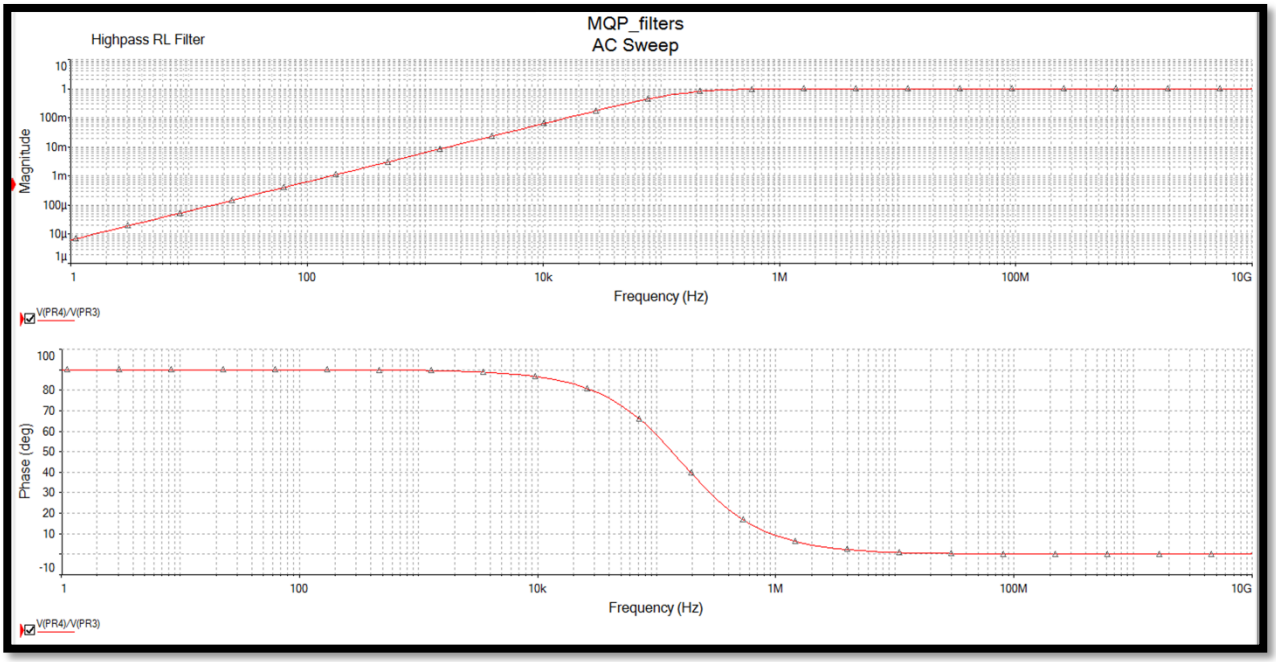

Figure 16: Magnitude and Phase frequency response of a highpass filter.

2.5 Simulation Software

The software chosen to simulate the planar inductor throughout the design process was Ansys Maxwell. Ansys Maxwell is an electromagnetic field solver providing 2D and 3D

simulation analysis for electromagnetic and electromechanical devices [16]. Maxwell focuses on low frequency electromagnetic simulation. This software provided the simulation tools and capabilities needed to simulate the inductor design.

2.6 Problem Statement

The team wants to better understand the relationship between airgap lengths of core and inductance. Additionally, the team will implement the multi-layer planar inductor in different applications of planar inductors.

3.0 Methodology

3.1 Modeling of a One Layer Planar Inductor

To begin the modeling and design process, the team decided to start by creating a one-layer planar inductor. In doing so, the team gained knowledge and experience with using the software Ansys Maxwell (See Section 1.2). The team analyzed the typical behaviors of an inductor in preparation for the prototype testing process (See Section 3).

Additionally, the team used Ansys Maxwell to vary the airgap length of the inductor core. In collecting this data, the team predicted the behavior of the multi-layer planar inductor with varied airgap (See Section 2).

Through the modeling and simulation process, the team gained a better understanding of the parameters that affect the inductance of the multi-layer planar inductor. Through using Ansys Maxwell simulation tools and MATLAB calculations, the team modeled two one-layer planar inductors with two different core configurations with different dimensions, an EE-core, and an EI-core (See Section 1.2).

3.1.1 EE Core Mathematical Modeling

As the first step to creating a magnetic circuit for the planar inductor, the team modeled the planar inductor as a N-turn coil wrapped around a magnetic core. The team assumed that a planar inductor with N turns (N_T) and N layers (N_L) can be modeled as a coil with $N_T \cdot N_L$ turns wrapped around the core with a current I (Figure 17).

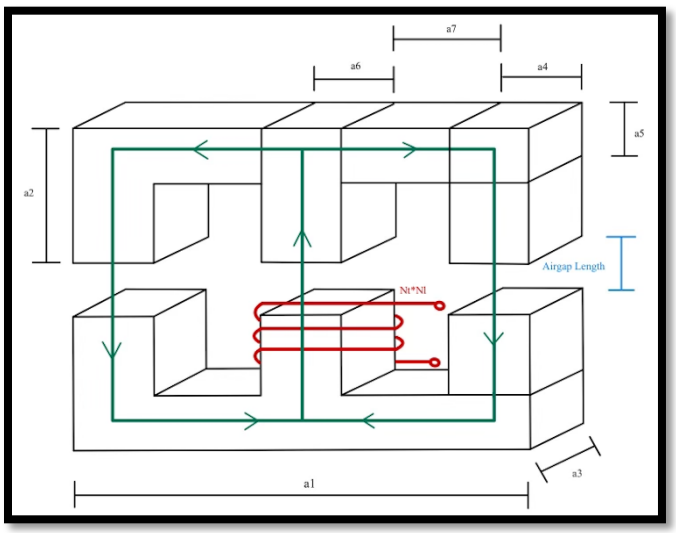

Figure 17: Planar Inductor Coil Model.

From this the team created an equivalent magnetic circuit representing each section of the core as a reluctance and the coil as a source.

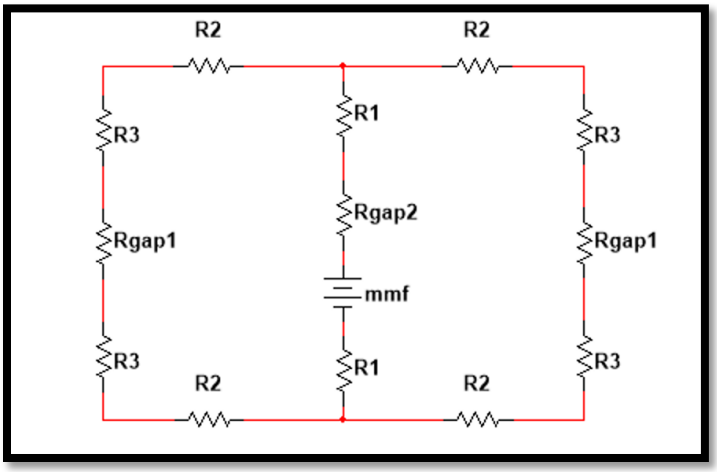

Figure 18: Planar Inductor Equivalent Circuit.

Using the model above, the team calculated the reluctance values using the following dimensions in Table 1 for the EE-core configuration (Figure 17).

Side	EE-38/8/25 (mm)
a1	38.5
a2	16.4
a3	25.5
a4	3.7
a5	3.7
a6	7.7
a7	11.7

Table 1: EE-Core dimension used in Calculations [1].

From these dimensions, the team determined equations for each reluctance value in the circuit. Using the relative magnetic permittivity of the 3C95 ferrite to be 3000.

$$\mathcal{R}_1 = \frac{\frac{a_2}{2} - \frac{a_3}{2}}{\mu_r \mu_0 (a_6 * a_3)}$$

$$\mathcal{R}_2 = \frac{\frac{a_1}{2} - \frac{a_4}{2}}{\mu_r \mu_0 (a_5 * a_3)}$$

$$\mathcal{R}_3 = \frac{\frac{a_2}{2} - a_5}{\mu_r \mu_0 (a_4 * a_3)}$$

Equations 18-20: Reluctance.

To find the reluctance of the airgap, the team accounted for the fringing effect by adding the gap length to each dimension for the cross-sectional area. Thus, the team modeled the gap reluctances of the gap.

$$\mathcal{R}_{gap1} = \frac{l_{gap}}{\mu_0 (a_4 + l_{gap}) * (a_3 + l_{gap})}$$

$$\mathcal{R}_{gap2} = \frac{l_{gap}}{\mu_0 (a_6 + l_{gap}) * (a_3 + l_{gap})}$$

Equation 21 and 22: Reluctance.

The circuit model can be further simplified by combining the series resistances. From this the team calculated the total reluctance.

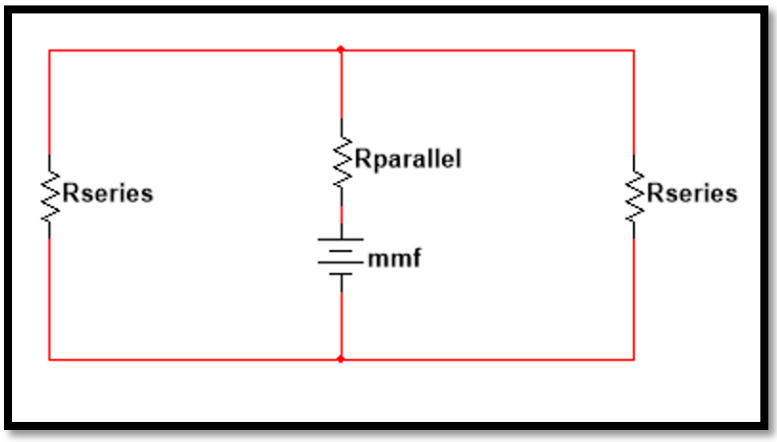

Figure 19: Simplified Circuit.

Using the equivalent series and parallel reluctances, the total reluctance from this circuit can be found using the following equations below.

$$\mathcal{R}_{series} = 2\mathcal{R}_2 + 2\mathcal{R}_3 + \mathcal{R}_{gap1}$$

$$\mathcal{R}_{parallel} = 2\mathcal{R}_1 + \mathcal{R}_{gap2}$$

$$\mathcal{R}_{total} = \mathcal{R}_{parallel} + \frac{\mathcal{R}_{series}}{2}$$

Equations 23-25: Reluctance.

Using this total reluctance value, the team then calculated the inductance of this magnetic circuit using the following equation.

$$L = \frac{(N_T * N_L)^2}{\mathcal{R}_{total}}$$

Equation 26: Inductance.

From these equations, the team predicted the inductance of the planar inductor with considerations to how the airgap affects the total inductance. Then, using MATLAB, shown in the appendix, the team calculated the predicted inductance values. See Appendix D for all MATLAB code. The graph shown below shows the relationship between airgap length and inductance value.

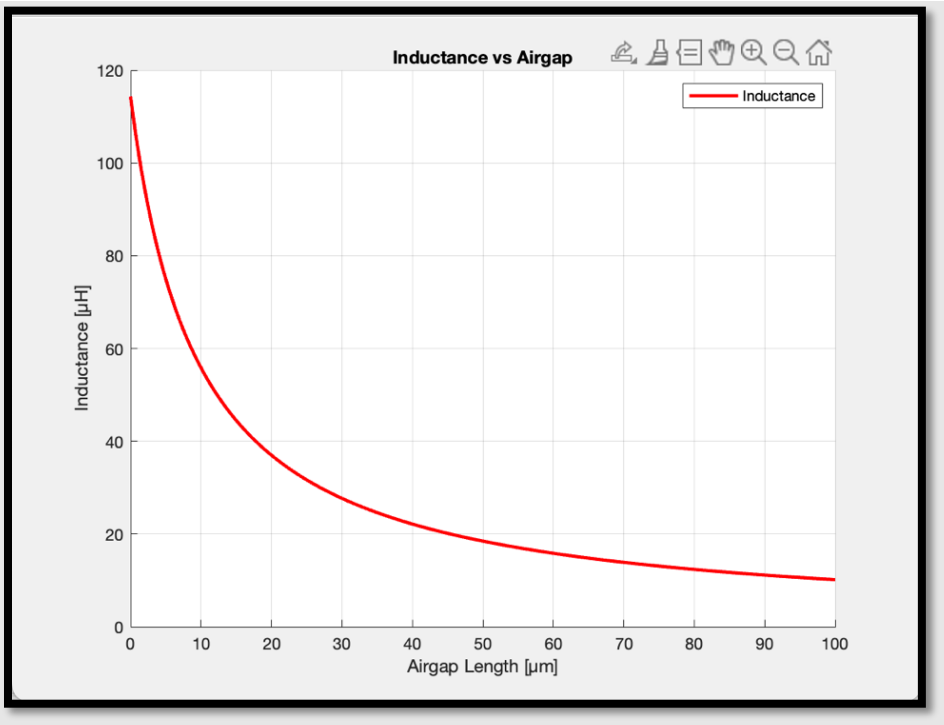

Figure 20: Inductance vs Airgap of EE core.

3.1.2 EI Core Mathematical Modeling

The team mathematically modeled the planar inductor as a N-turn coil wrapped around a magnetic core. It was assumed that a planar inductor with N turns (N_T) and N layers (N_L) can be modeled as a coil with $N_T \cdot N_L$ turns wrapped around the core with a current I (Figure 21).

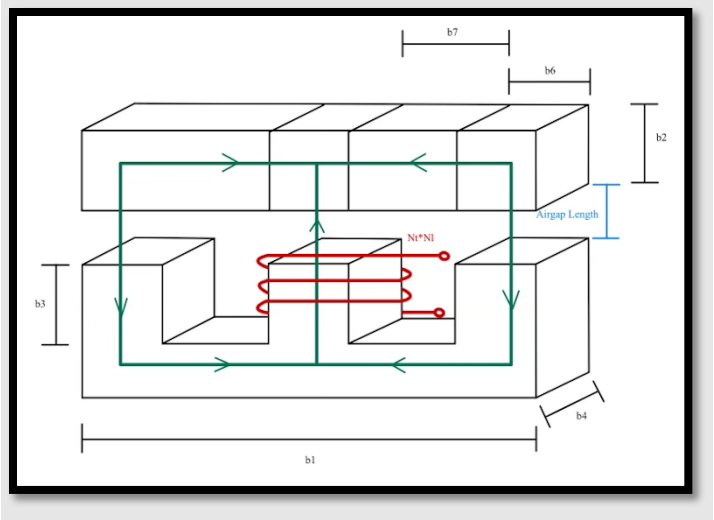

Figure 21: Planar Inductor Coil Model.

From this the team created an equivalent magnetic circuit representing each section of the core as a reluctance and the coil as a source.

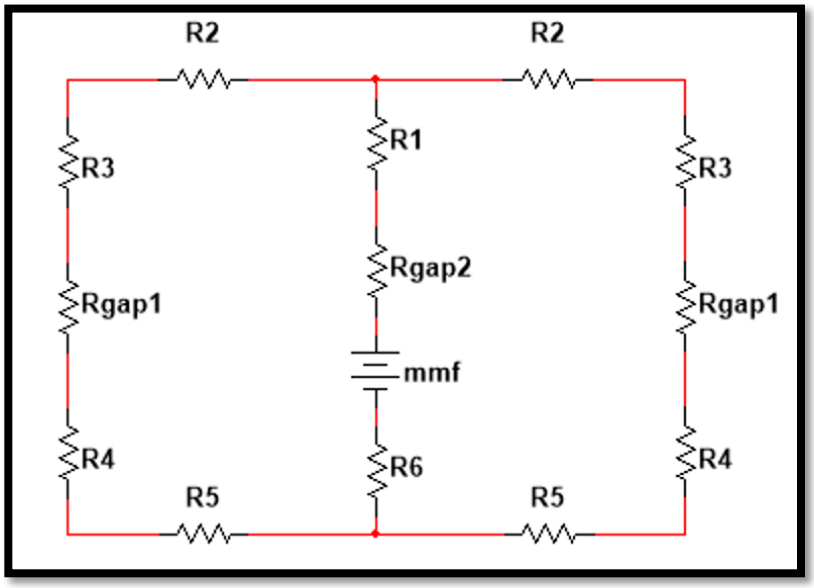

Figure 22: Planar Inductor Equivalent Circuit.

Using the model in Figure 21, the team calculated the reluctance values using the following dimensions in Table 2 for the EI-core configuration.

Side	EI-43/10/28 (mm)
b1	43.3
b2	4.1

b3	9.5
b4	28
b5	5.5
b6	3.8
b7	13.8
b8	8.1

Table 2: EI Core Dimension used [1].

From these dimensions, the team determined equations for each reluctance value in the circuit. Using the relative magnetic permittivity of the 3C95 ferrite to be 3000.

$$\mathcal{R}_1 = \frac{\frac{b_2}{2}}{\mu_r \mu_0 (b_8 * b_4)}$$

$$\mathcal{R}_2 = \frac{b_7 + \frac{b_8}{2} + \frac{b_6}{2}}{\mu_r \mu_0 (b_2 * b_4)}$$

$$\mathcal{R}_3 = \frac{\frac{b_2}{2}}{\mu_r \mu_0 (b_6 * b_4)}$$

$$\mathcal{R}_4 = \frac{b_5 + \frac{b_3 - b_5}{2}}{\mu_r \mu_0 (b_6 * b_4)}$$

$$\mathcal{R}_5 = \frac{b_7 + \frac{b_8}{2} + \frac{b_6}{2}}{\mu_r \mu_0 (b_3 - b_5) * b_4)}$$

$$\mathcal{R}_6 = \frac{b_5 + \frac{b_3 - b_5}{2}}{\mu_r \mu_0 (b_8 * b_4)}$$

Equation 27-32: Reluctance.

To find the reluctance of the airgap, the team accounted for the fringing effect by adding the gap length to each dimension for the cross-sectional area. Thus, the team modeled the gap reluctances of the gap.

$$\mathcal{R}_{gap1} = \frac{l_{gap}}{\mu_0 (b_6 + l_{gap}) * (b_4 + l_{gap})}$$

$$\mathcal{R}_{gap2} = \frac{l_{gap}}{\mu_0(b_8 + l_{gap}) * (b_4 + l_{gap})}$$

Equation 33 and 34: Reluctance.

The circuit model can be further simplified by combining the series resistances. From this the team calculated the total reluctance (Figure 23).

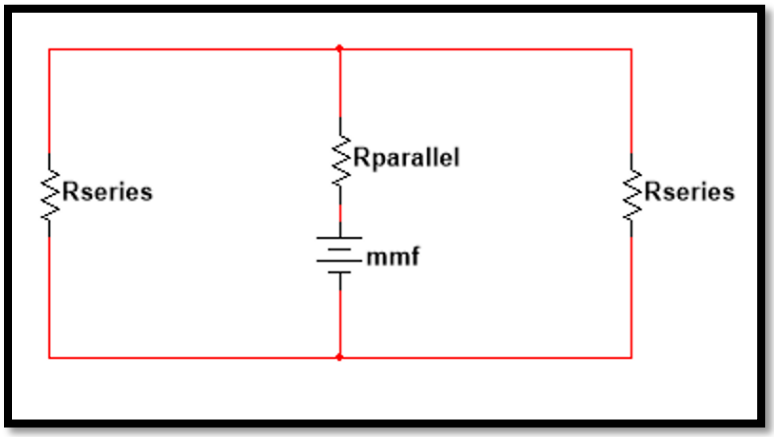

Figure 23: Simplified Circuit.

Using the equivalent series and parallel reluctances, the total reluctance from this circuit can be found using the following equations below.

$$\mathcal{R}_{series} = \mathcal{R}_2 + \mathcal{R}_3 + \mathcal{R}_{gap1} + R_4 + R_5$$

$$\mathcal{R}_{parallel} = \mathcal{R}_1 + \mathcal{R}_{gap2} + R_6$$

$$\mathcal{R}_{total} = \mathcal{R}_{parallel} + \frac{\mathcal{R}_{series}}{2}$$

Equation 35-37: Reluctance.

Using this total reluctance value, the team then calculated the inductance of this magnetic circuit using the following equation.

$$L = \frac{(N_T * N_L)^2}{\mathcal{R}_{total}}$$

Equation 38: Inductance.

From these equations, the team predicted the inductance of the planar inductor with considerations to how the airgap affects the total inductance. Then, using MATLAB, the team calculated the predicted inductance values. The graph shown below shows the relationship between airgap length and inductance value.

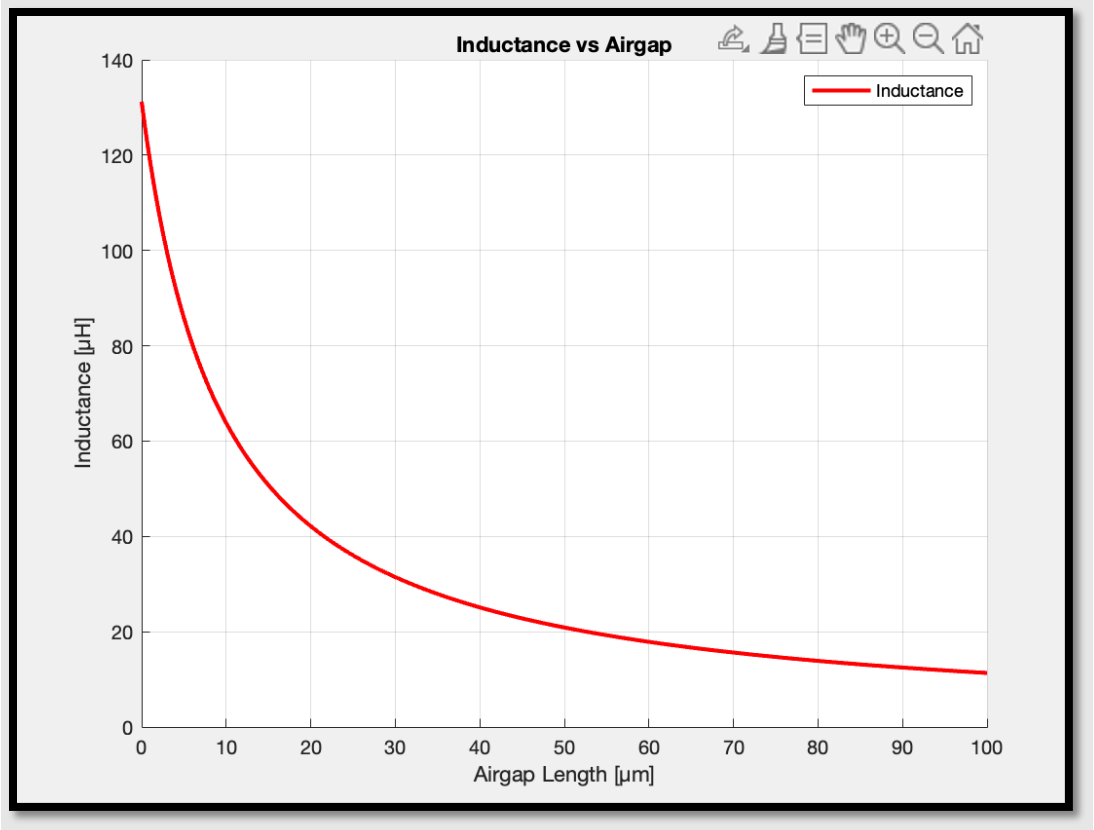

Figure 24: Inductance vs Airgap of EI core.

3.2 Modeling in Ansys Maxwell

3.2.1 No Core Planar Inductor Simulation

Before modeling the other configurations, the team modeled a one layer, three turn planar inductor with no core. The team ran a simulation with 30 adaptive passes with a 0.001 percent error and recorded the inductance for each adaptive pass. Outlined in Figure 25, the teams' preliminary inductor is comprised of one layer with three turns of copper trace overlaying a dielectric material called FR-4.

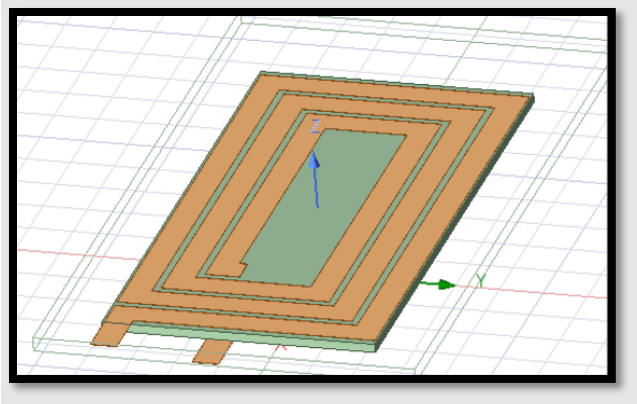

Figure 25: Planar Inductor with No Core.

Pass	L (nH)
1	1765.496485
2	1026.169455
3	439.766693
4	294.627863
5	193.072958
6	135.913041
7	102.570715
8	79.523712
9	65.929044
10	52.783627
11	45.43995
12	40.281946
13	37.083662
14	34.995292
15	33.75829
16	32.94915
17	32.44947
18	32.119902
19	31.913714
20	31.783773
21	31.682106
22	31.610572
23	31.569196
24	31.539341
25	31.520444
26	31.506207
27	31.496571
28	31.489215
29	31.483904
30	31.48042

Table 3: Inductance values in nH for 30 Adaptive Passes of a Coreless One-Layer Inductor.

As expected, the team determined that the inductor without a core had a low value of inductance. Also, the team documented the precision of each adaptive pass of the simulation software. After about 25 adaptive passes, the value of inductance converged sufficiently for the teams' purposes. The team determined this when considering the time it took to run 30 adaptive passes compared to 25 adaptive passes. Also, the difference between the inductance values determined in 35 passes and 25 is only 0.04nH. This was an acceptable difference for the teams' purposes, and the time to run the simulation significantly lessened when using 25 passes. Therefore, for the rest of the simulations the team used 25 adaptive passes with a 0.001 percent error.

3.2.2 EE Core Simulation Model

The team simulated the single-layer planar inductor model encased within an EE-core in Ansys Maxwell (Figure 26). The team used the EE core dimensions in Table 1 and assigned a relative permeability of 3000 per the specifications of 3C95 ferrite. The copper traces were 3mm wide and 35µm thick. They were spaced apart by 0.8mm and arranged in a spiral pattern on a 1.8mm thick piece of FR4. For the simulation, the traces were excited with a current of 5 A. The simulation was set up to have 25 adaptive passes with a 0.001% error. Using this setup, the team ran a parametric simulation varying the gap length from 0µm to 100µm in steps of 5µm. The results of this simulation will be compared to the mathematical model for the EE core discussed above.

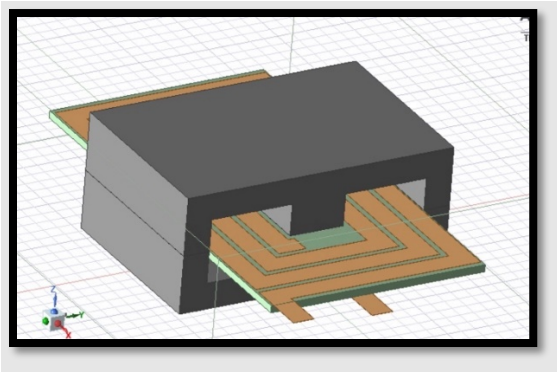

Figure 26: EE Core Inductor Model.

3.2.3 EI Core Simulation Model

Using similar procedures as the EE core, the team created a single-layer inductor model with an EI-core in Ansys Maxwell (Figure 27). The team used the EE core dimensions in Table 2 and assigned a relative permeability of 3000 per the specifications of 3C95 ferrite. The copper traces were 3mm wide and 35µm thick. They were spaced apart by 0.8mm and arranged in a spiral

pattern on a 1.8mm thick piece of FR4. For the simulation, the traces were excited with a current of 5 A. The simulation was set up to have 25 adaptive passes with a 0.001% error. Using this setup, the team ran a parametric simulation varying the gap length from 0µm to 100µm in steps of 5µm. The results of this simulation will be compared to the mathematical model for the EI core discussed in 3.1.2.

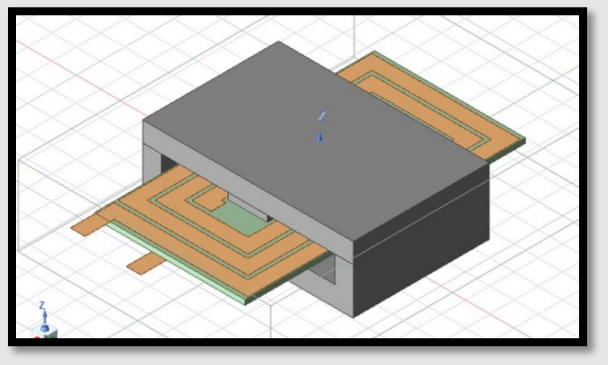

Figure 27: EI Core Inductor Model.

3.3 Design and Modeling of a Multilayer Planar Inductor

Through comparison of the EI and EE cores, the team determined that the inductor was better in the EE core due to the structure of the configurations. The EE core showed better simulation results for fringing effects than EI. Through MATLAB calculations, the team determined the final design to be a five-layer planar inductor with three turns on each layer.

The five-layer inductor was fabricated using the same dimensions as the EE one layer design. This means the team was able to use the same calculations for total reluctance as calculated in 3.1.1. The team replaced the 3 turns in Equation 26 with 15 turns to predict the 5-layer inductor's behavior when the gap length is varied.

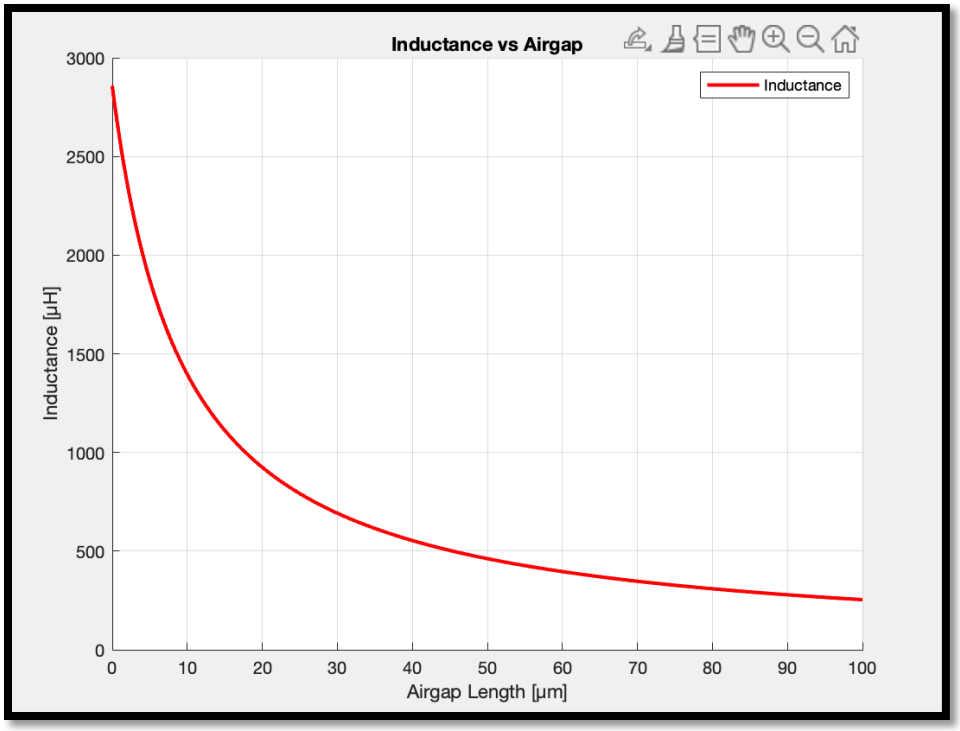

Figure 28: Inductance vs Airgap Length for 5 Layer Inductor.

Practically, the copper traces would be placed on an FR-4 dielectric with three turns for one layer, then connected to the next layer using blind and buried vias. This allows for each layer to be connected to one another to accommodate the flow of current. The resulting circuit element has five layers, each with three turns for a total of fifteen turns (Figure 1). To obtain these parameters, the team designed the inductor to meet the specifications of the tested circuits.

3.3.1 Test Circuits: Boost Converter

In performing tests with the final inductor design, the team chose three different circuits to implement. The first is a low-pass circuit, the second is a high-pass circuit, and the third is a boost-converter. These three circuits were chosen as the team wanted to evaluate the inductor in practical applications where the team can see the result of the variable inductor concept.

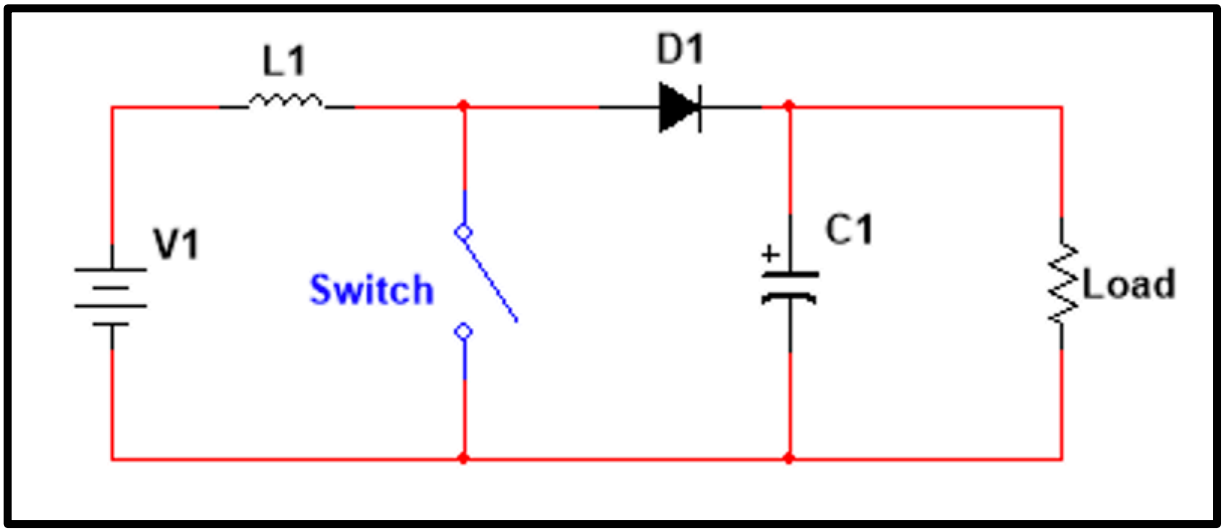

Figure 29: Boost Converter.

Expanding upon the configuration of boost converters outlined in the background, the team designed a simple boost converter with a 12V input those doubles to 24V in the output (Figure 11). To smooth out the voltage ripple, the team implemented a 100µF capacitor. Using this rig the team tested the practicality of implementing the variable inductor design in a DC-DC converter. To build this converter the team would need to know what range of inductance values could be used to stay in continuous conduction. The inductance to keep continuous conduction is with the following equation.

$$L_{min} = \frac{D(1-D)^2 R}{2f}$$

Equation 39: Minimum inductance to keep continuous conduction.

f – Frequency
D – Duty cycle
R – Load Resistance

Using a duty cycle of 50%, a frequency of 125kHz and a load resistance of 500Ω we get a minimum inductance value of 250µH. Based on the previous calculations, a 15-turn planar inductor would have an inductance around 254µH at a gap length of 100µm. This means that a planar inductor with 15 turns will be able to keep the boost converter in continuous conduction mode through the desired 0µm-100µm change in gap length. The team came up with an inductor design that would be 5 layers with 3 turns per layer, like the one-layer design. To better understand the range of ripple current this inductor would allow for, the team used the following equation.

$$I_{ripple} = \frac{V_{in}}{L * T * D}$$

Equation 40: Ripple Current.

L à Inductance
T à Period
D à Duty cycle

The range was found to be from about 0.1A to 1A and the team determined the inductance values from both extremes. Using the max inductance value when the inductor gap length is 1µm, and the minimum inductance value when the gap length is 100µm.

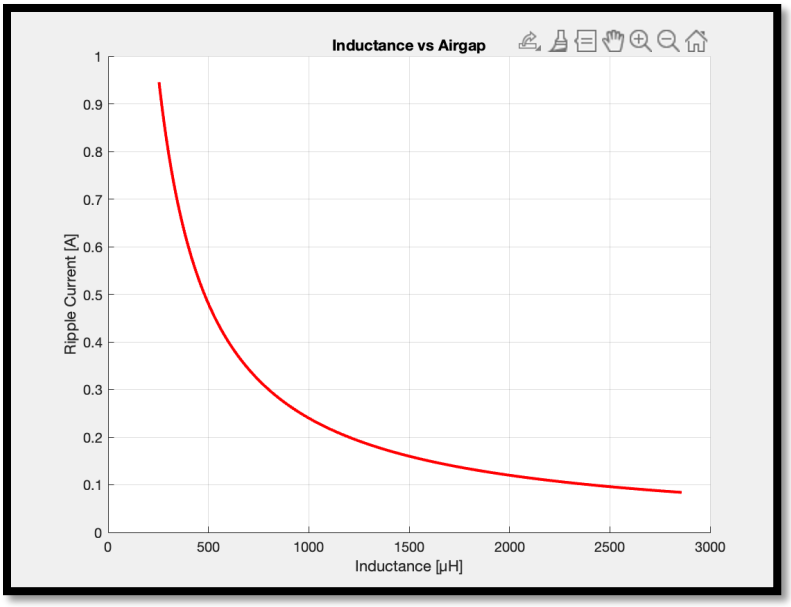

Figure 30: Inductance vs Ripple Current for 15 Turn Design.

Using the design methodology from the one-layer inductor, the relationship between ripple current and airgap length was predicted (Figure 31).

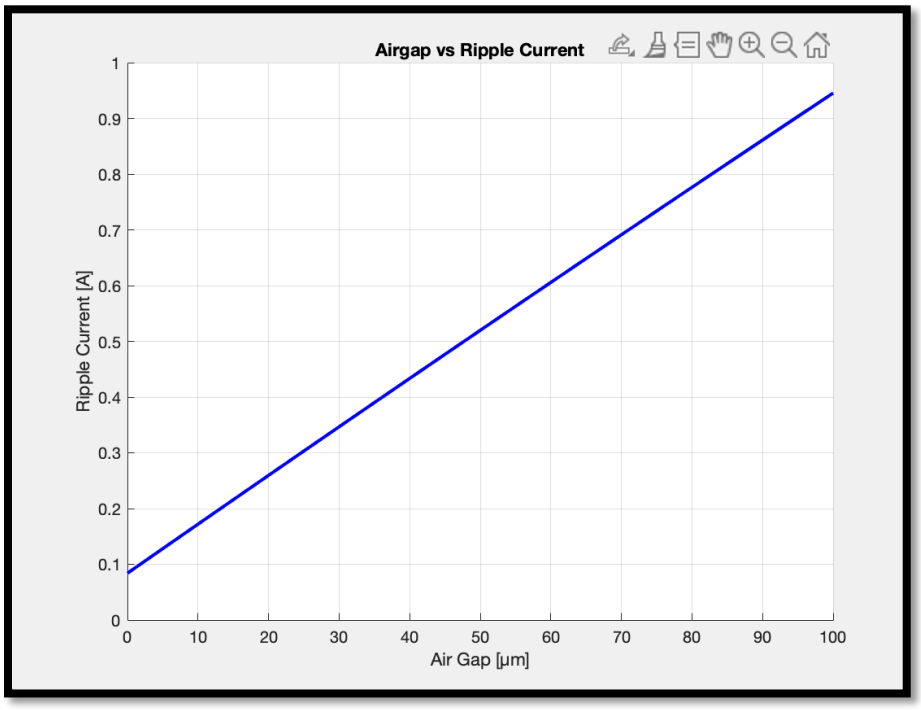

Figure 31: Airgap vs Ripple Current for 15 Turn Design.

This boost converter circuit was created in National Instruments' Multisim, then designed on a PCB using 282834-2 connectors which have a max of 10amps to make the circuit modular. Different versions of the inductor can be plugged in, as well as using a DC power supply to make sure the input is constant. Also, a waveform generator to make sure the duty cycle is accurate.

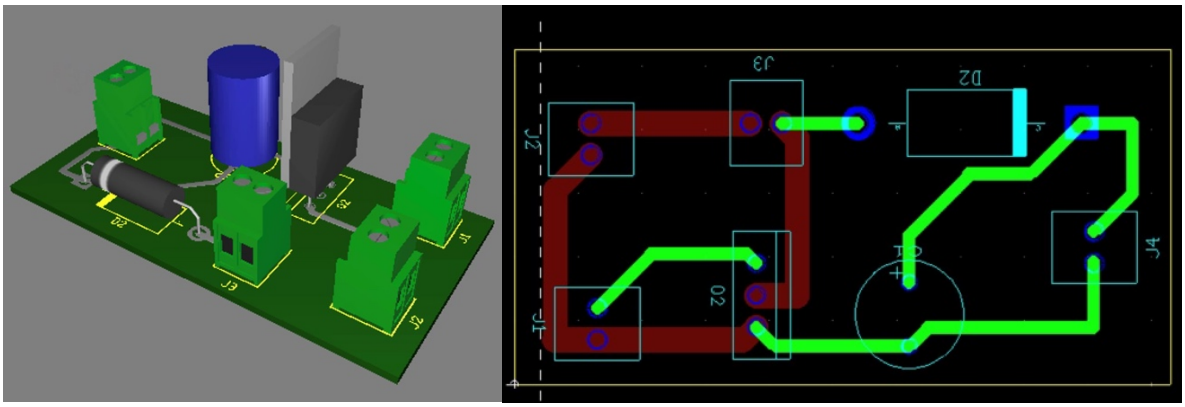

Figure 32: Boost Converter PCB Design.

The team will connect the variable planar inductor to this circuit and observe any changes to the output voltage and currents. The load resistances will also be varied to see how the inductor handles high currents. The goal is to make sure that as the inductance value changes the circuit

still behaves predictably. Also, to make sure that the team's inductor design is suitable to applications that could involve higher currents.

3.3.2 Test Circuits: Filters

To thoroughly understand the potential behaviors that the team's inductor design could display, it is important to find an avenue where the inductor could be applicable. Two scenarios where this inductor could be implemented are a lowpass and a highpass filter.

One common filter application is a lowpass RL filter. A lowpass filter passes through frequency values lower than 3dB frequency. A lowpass RL filter consists of a resistor and an inductor.

Highpass filters have predicable behavior, except that it will allow higher frequency values to pass through to the remainder of the circuit. Nothing below the 3dB frequency value will pass in this case.

The team would like to observe how a changing inductance and airgap value affects the anticipated filter behavior. Specifically, how the 3dB cutoff frequency changes as it relates as a function of inductance.

$$F_{3dB} = \frac{R}{2\pi L}$$

Equation 41: RL Cutoff Frequency Equation.

Using Equation 41 with a 1kΩ resistor, Figure 33 shows the relationship between the inductance values of our design and the predicted 3dB frequency. This is used to create a graph for the relationship between gap length and 3dB frequency (Figure 34).

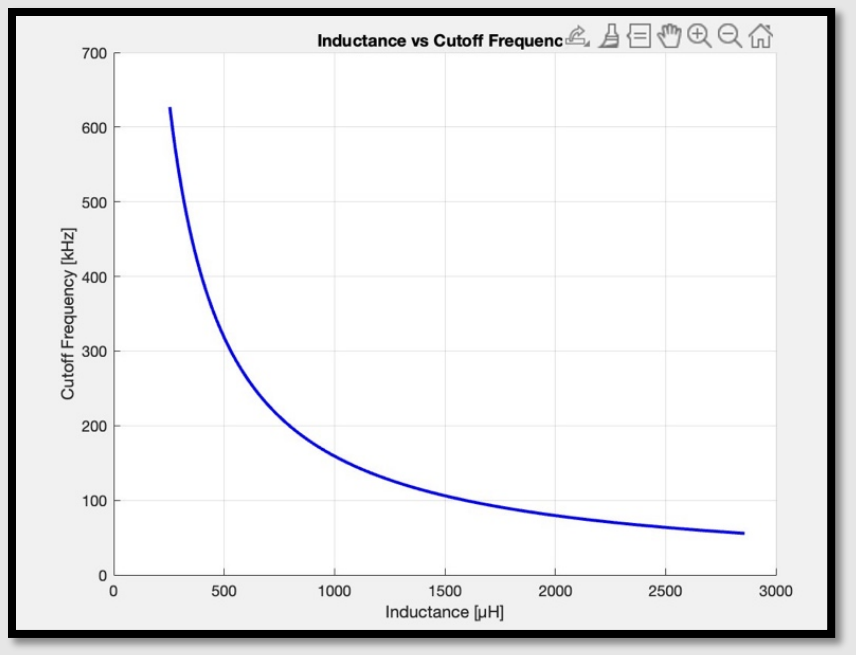

Figure 33: Inductance vs 3dB Frequency.

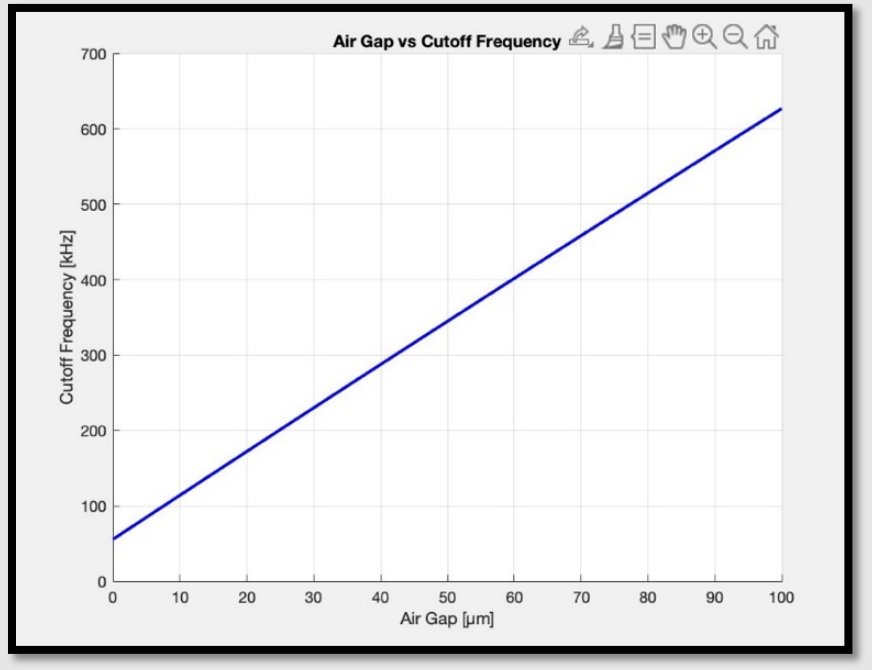

Figure 34: Airgap vs 3dB Frequency.

3.3.3 Modeling in Ansys Maxwell

Using the software Ansys Maxwell provided by WPI's licensure, the team designed a 5-layer inductor to model, shown below. The team performed simulations to have data to refer to during the physical testing phase. The team wanted to ensure that the data collected with a

fabricated 5-layer inductor was reasonable, and to prove that the initial math and theory understanding was correct (Figure 35).

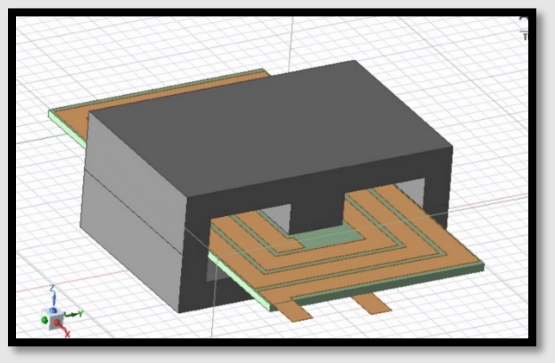

Figure 35: Multilayer inductor in Ansys Maxwell

The same dimensions from Table 1 for the EE cores were used and the core was given a relative permeability of 3000 per the specifications of the 3C95 ferrite. The copper traces were 3mm wide and 35µm thick. They were spaced apart by 0.8mm and arranged in a spiral pattern on a 1.8mm thick piece of FR4, then connected to the next layer using blind and buried vias. For the simulation, the traces were excited with 5amps of current. The simulation was set up to have 25 adaptive passes with a .001% error. Using this setup, the team ran a parametric simulation varying the gap length from 0µm to 100µm in steps of 5µm. The results of this simulation will be compared to the mathematical model for the 5-layer EE core.

3.4 Designing PCB in Altium Designer

The team designed the PCB using the software, Altium Designer, using the WPI Student License. The following procedure outlines the steps the team took to create the one layer and 5-layer PCB.

3.4.1 Designing the One Layer PCB

Creating a new project, the team used the ‘Place Line’ feature to create a box with the required size requirements of the PCB. Highlighting the box and selecting ‘Define Board Shape from Selected Objects’ removes all exterior space from the board (Figure 36).

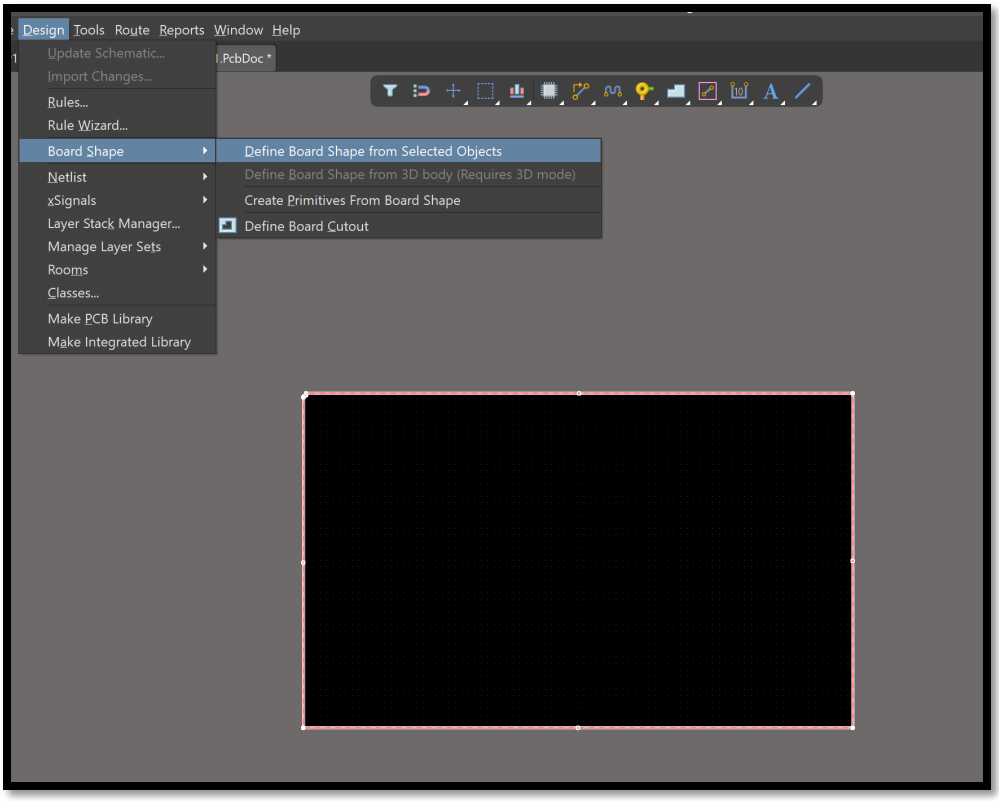

Figure 36: Defining Board Shape of PCB in Altium Designer.

Selecting ‘Place’, ‘Fill’, the team laid out the spiral configuration of the copper traces. The dimensions were determined via the core specs to assure that the PCB could sit enclosed in both cores.

Figure 37 outlines the steps to define the board cutout in the center of the PCB. The dimensions of this were determined by measuring the core dimensions.

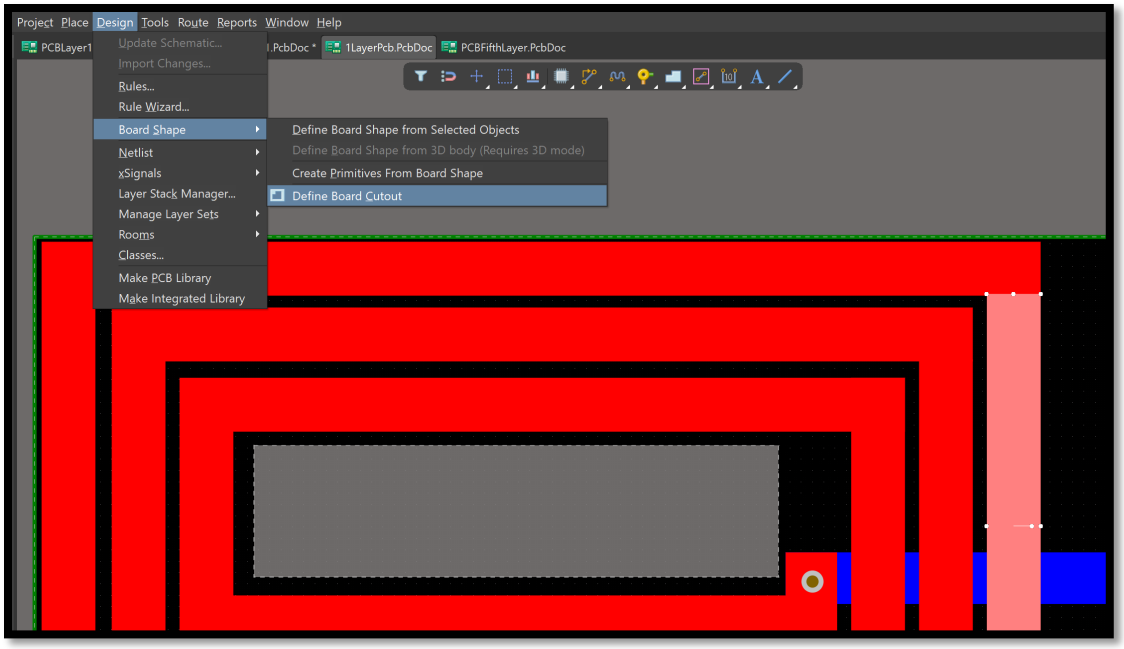

Figure 37: Defining Board Cutout.

The team's one-layer PCB had "two layers" of traces with a through-hole via connecting them. The traces in red were assigned to 'Top Layer' and the trace in blue was assigned to 'Bottom Layer'. This bottom layer was created in order to attach device leads in physical testing. Selecting 'Place' 'Via' on top of the overlapping traces creates a through via down.

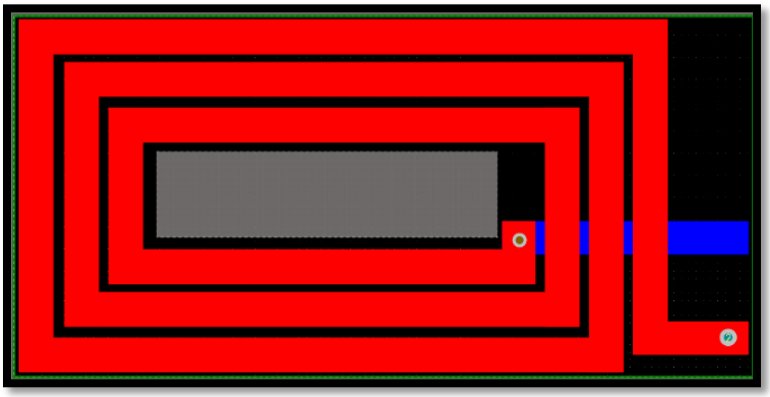

Figure 38: Finalized One-Layer PCB on Altium Designer.

3.4.2 Designing the Five Layer PCB

The team designed two methods of creating the five-layer PCB. Starting with the one-layer design, the team created five separate one-layer boards. These five separate layers stacked together, connected with manual solder through vias, create the five-layer design. The bottom layer was removed for layers 1-4 as they didn't need any connections to device leads. The soldering was

done by the team in the lab after the manufacturing of the five separate layers. The transition from each layer results in a continuous spiral winding. The “six” layer, shown in blue, is the bottom trace used to connect the leads to testing equipment. Using through vias allowed the team to effectively solder the layers together.

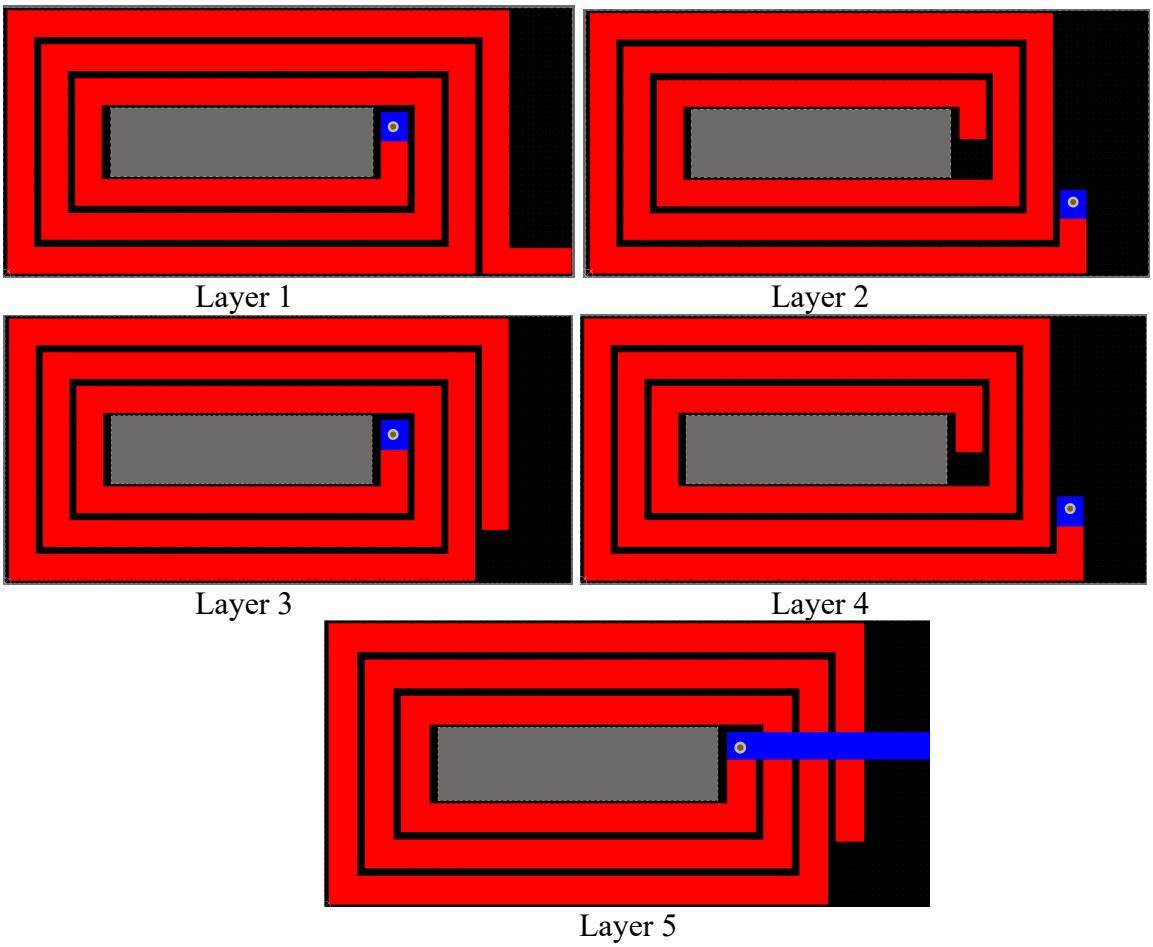

Figure 39: Individual PCB paths for multi-layer planar inductor and final combined design.

The team also designed the five-layer PCB using bling and buried vias in between layers of traces. Starting with the one-layer design, the team stacked the layer windings and separated the traces using the ‘Layer Stack Manager’. Layer one in red, layer two in yellow, layer 3 in light blue, layer 4 in green, layer 5 in purple. The “sixth” layer is the bottom trace used to connect the leads to the testing equipment (Figure 41).

#	Name	Material	Type	Weight	Thickness	Dk	Df
1	Top Layer	CF-004	Signal	1oz	0.035mm		
	Dielectric 2	PP-006	Prepreg		0.07112mm	4.1	0.02
2	Layer 2	CF-004	Signal	1oz	0.035mm		
	Dielectric 4	PP-006	Prepreg		0.07112mm	4.1	0.02
3	Layer 3	CF-004	Signal	1oz	0.035mm		
	Dielectric 1	FR-4	Dielectric		0.32004mm	4.8	
4	Layer 4	CF-004	Signal	1oz	0.035mm		
	Dielectric 5	PP-006	Prepreg		0.07112mm	4.1	0.02
5	Layer 5	CF-004	Signal	1oz	0.035mm		
	Dielectric 3	PP-006	Prepreg		0.07112mm	4.1	0.02
6	Bottom Layer	CF-004	Signal	1oz	0.035mm		

Figure 40: Layer Stack Manager of 5-Layer PCB.

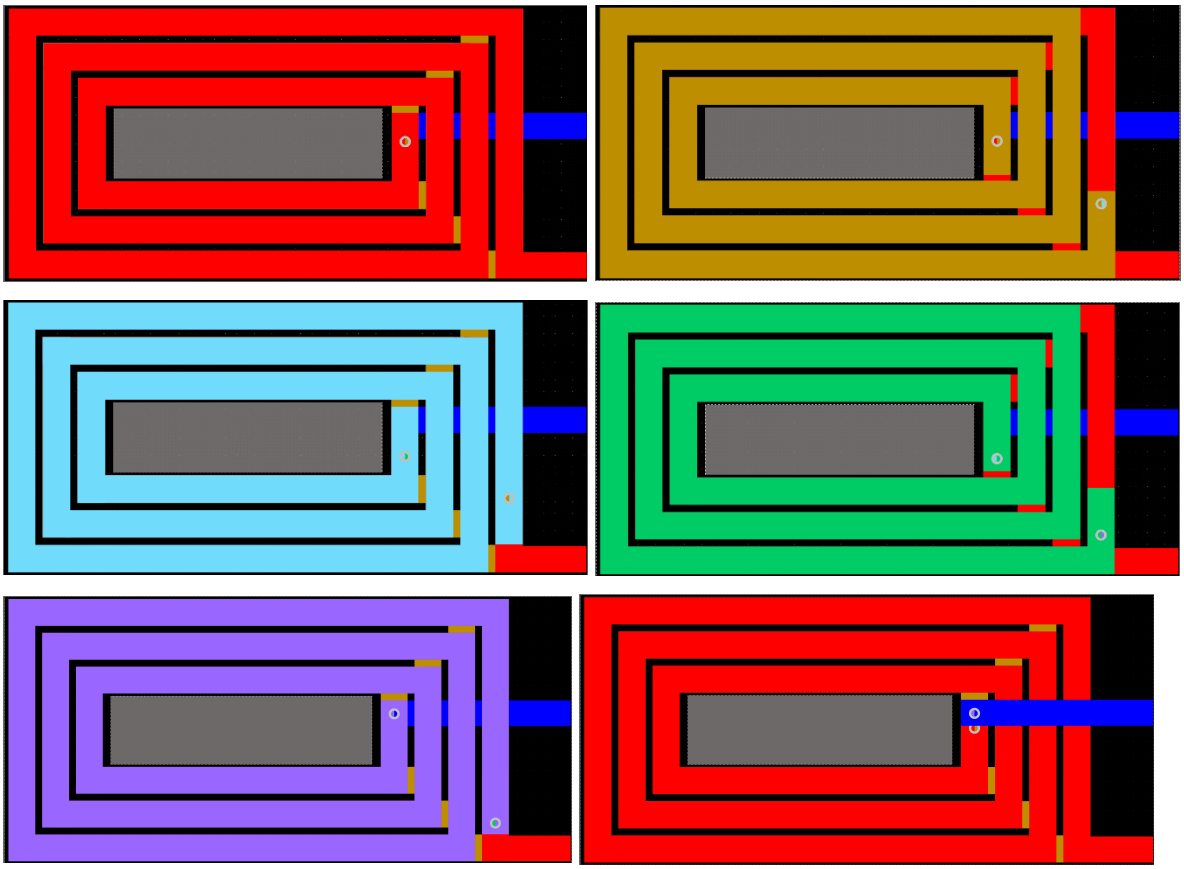

Figure 41: 5 layer PCB.

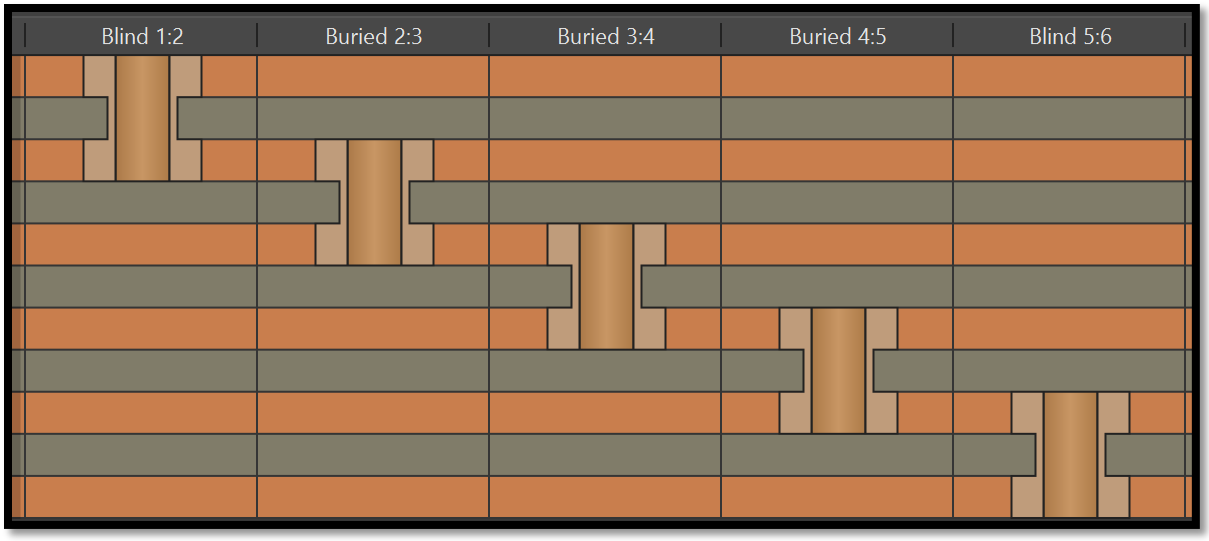

Figure 42: 5-layer Via Configuration.

When determining the best manufacturers to use for the PCB production, the team determined that the stacked five-layer design would be far more affordable than the five-layer design with blind and buried vias. This is due to the high manufacturing costs of the vias. As a result of the budget for this project, the team proceeded with the stacked PCB design. Final PCB shown below.

3.5 Designing the Test Rig

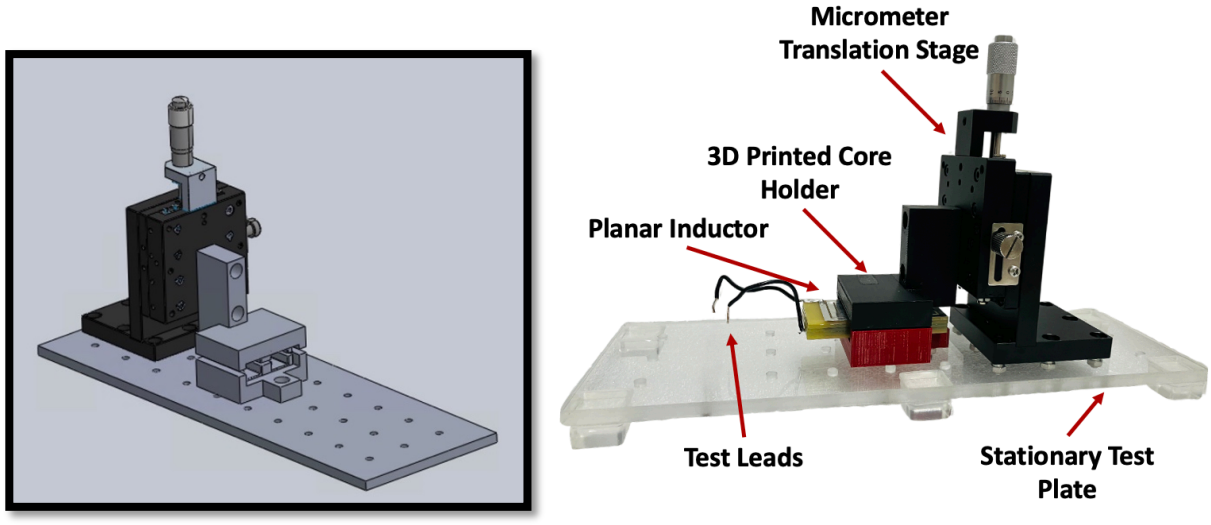

Figure 43: Test Rig.

The test rig was set up on a stationary test plate with rubber feet on the bottom to provide stability. The team laser printed holes though the test plate to secure the micrometer translation stage. The micrometer translation stage has a precision of 10 micrometers and was chosen due to its cost.

Attached to the micrometer translation stage is a 3D printed CAD holder used to hold the core in place to keep it level and precise as possible. The core is superglued to the holder to allow the micrometer translation stage to move the two pieces of the core apart to vary the gap length. In-between the core sits the PCB inductor with two test leads connected to the windings. Final rig shown below.

3.6 Practical Testing of Planar Inductor Circuits

The following sections describe the testing procedures the team used to understand how the inductor behaves.

3.6.1 Procedure 1

The first procedure was to have the planar inductor in both 1-layer and 5-layer EE core configurations connected to an LCR. The team observed the changing inductance and recorded the results as that airgap changes. The team observed the effect of airgap length on the overall inductance value and compared it to both the mathematical and simulated models. In addition, the team hypothesized practical applications for a variable inductor.

3.6.2 Procedure 2

For this experiment, the team built three circuits to see how the 5-layer inductor would perform in a more practical setting. The first two are a RL low pass circuit and a RL high pass-circuit using a 1kΩ resistor. Following this, the team decided to incorporate the inductor into a boost converter.

Like Procedure #1, the team wanted to observe and evaluate the effects of varying the airgap on the inductance. However, for this experiment, the team observed how the varying inductance due to the gap length affected the filter's 3dB cutoff frequency. This information was then compared to the team's predictions from the mathematical and simulated models.

In addition, the team will be implementing the inductor design in a boost converter circuit. The output will be monitored to observe if the changing inductance affects the output voltage and

currents in any significant or unpredictable ways. The purpose of this test is to find any potential problems with the variable inductor design when implemented in practical circuits.

The goal of this procedure is also to evaluate the viability of the variable inductor's design. The team needed to assess the practicality of these proposed use cases, so understanding the efficiency, stability and predictability of the circuits is important.

4.0 Results

This section presents the data that the team collected throughout this MQP. The data is the result of the steps and procedures described in the methodology.

4.1 Simulation results

Using the simulation setups described in the methodology, the team ran multiple different simulations on Ansys Maxwell on single layer PCB with EE cores and EI cores. The team also ran simulations of the multilayer inductor design. Data presented below reflects the most recent and accurate simulations performed by the team.

The simulation results support the accuracy of the team's mathematical calculations for modeling planar coils as magnetic circuits represented in the methodology. Through analyzing the data from the multilayer simulation, the team confirmed the practicality of using a variable inductor design in the test circuits described in the Methodology.

4.1.1 EE core Inductor Simulation

Using the EE core Ansys model, outlined in the methodology, the team ran a parametric simulation varying the gap length between the two core halves. The table below reflects the inductance of the model as the gap varies from 0µm to 100µm in steps of 5µm.

Gap Length (µm)	L (µH)
0	130.167027
5	81.909481
10	59.935507
15	47.360795
20	39.219393

25	33.512866
30	29.288268
35	26.037862
40	23.456656
45	21.357899
50	19.616854
55	18.15469
60	16.90088
65	15.817354
70	14.870725
75	14.037419
80	13.297638
85	12.636539
90	12.041898
95	11.504585
100	11.016726

Table 4: Simulated Inductance vs Gap Length for EE core Inductor

The simulation results are close to those predicted by the mathematical modeling calculated in the methodology. To better represent this similarity, both data sets were plotted on an Inductance vs Airgap graph for comparison shown in Figure 44.

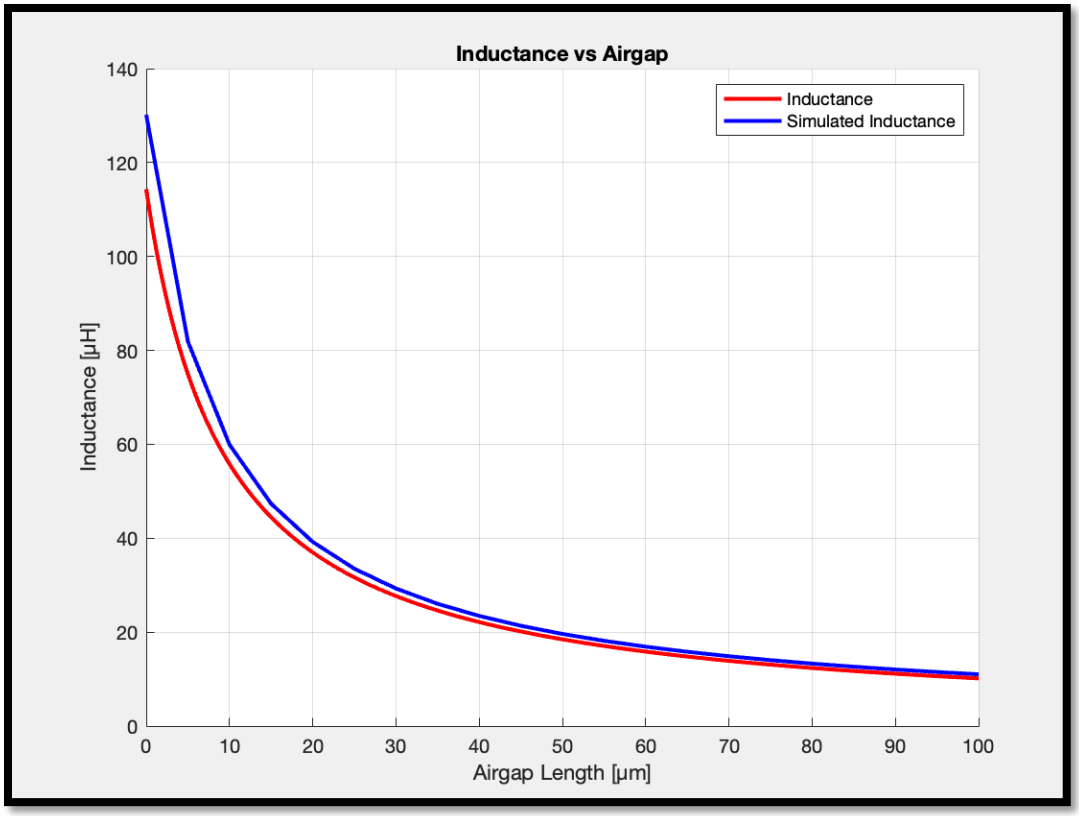

Figure 44: Graph comparing Inductance vs Airgap for the mathematical and simulated models of the EE core inductor.

While both curves are close to each other, the values of inductance are higher on the simulated curve (shown in blue). The greatest difference is when the gap length is 0µm. The simulated inductance is 130.167µH and the calculated inductance is 114.319µH. This is only a 12.17% error, and the curves converge as the gap length increases. This data, with minor error, validates the calculations done in the methodology and shows they are accurate enough to predict the inductance of the team's EE core model.

4.1.2 EI core Inductor Simulation

Using the EI core ANSYS model outlined in the methodology, the team ran a parametric simulation varying the gap length between the two core halves. The table below reflects the inductance of the model as the gap varies from 0µm to 100µm in steps of 5µm.

Gap Length (µm)	L (µH)
0	162.443742
5	98.339747
10	71.075568
15	55.866169

20	46.092014
25	39.271223
30	34.281341
35	30.454027
40	27.442288
45	24.981866
50	22.946379
55	21.232482
60	19.771622
65	18.508348
70	17.408098
75	16.438553
80	15.571703
85	14.804001
90	14.119585
95	13.490168
100	12.923496

Table 5: Simulated Inductance vs Gap Length for EI core Inductor.

The results from the simulation are close to those predicted by the mathematical modeling shown in the Methodology. To better represent this similarity, both data sets were plotted on an Inductance vs Airgap graph for comparison shown in Figure 45.

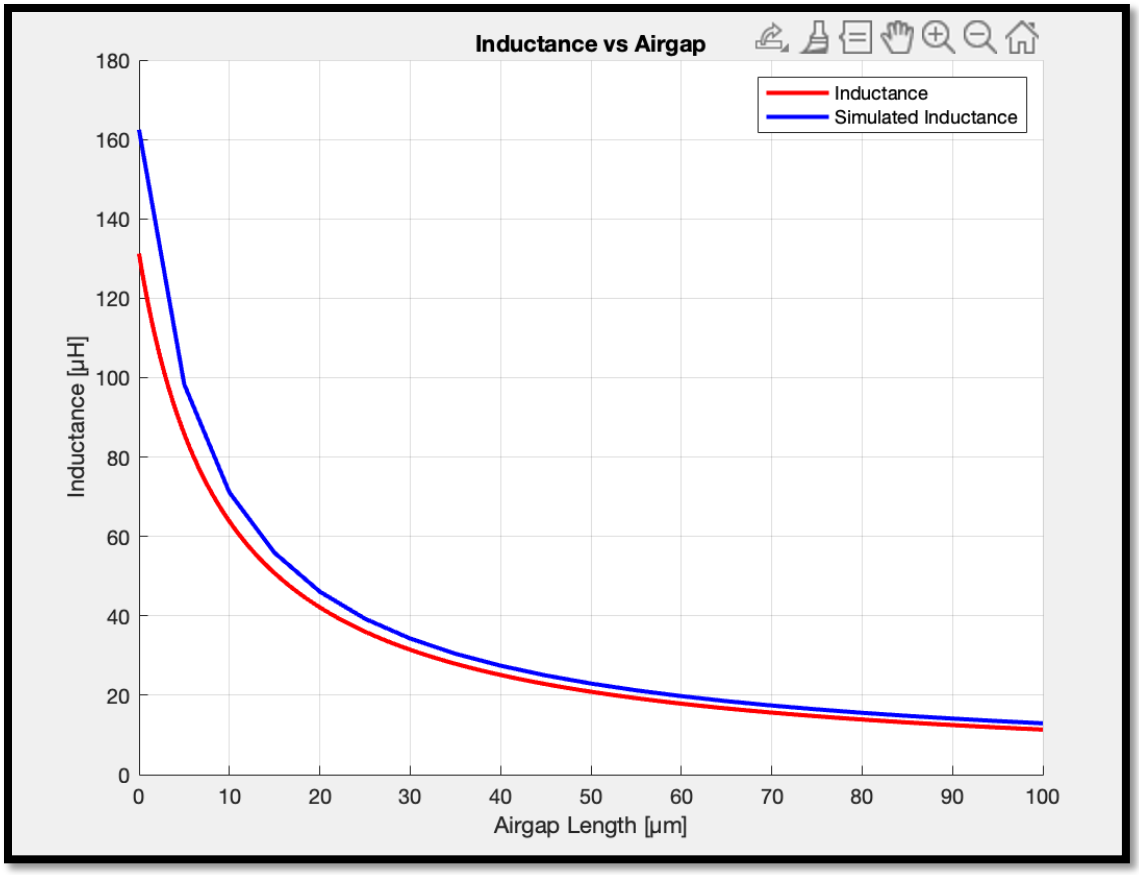

Figure 45: Graph comparing Inductance vs Airgap for the mathematical and simulated models of the EI core inductor.

While both curves are close to each other, the values of inductance tend to be higher on the simulated curve (shown in blue). The greatest difference is when the gap length is 0µm. The simulated inductance is 162.444µH and the calculated inductance is 131.219µH. This is a 19.22% error, while the curves do converge as the gap length increases, the simulation does seem to have significantly higher inductance values compared to the calculations. This can be due to inaccuracies in the assumptions made in the mathematical calculations. The team's approach of adding the gap length to each dimension of the area does not appear to work with this core configuration. This could be because the core is not uniform at the intersection like the EE configuration, allowing for greater fringing. This difference between the calculation and simulation and the need for additional materials is why the team modeled the multilayer inductor with the EE core configuration.

4.1.2 Multilayer Inductor Simulations

Using the multilayer (3 turns 5 layers) Ansys model outlined in the methodology, the team ran a parametric simulation varying the gap length between the two core halves. The table below reflects the inductance of the model as the gap varies from 0µm to 100µm in steps of 5µm.

Gap Length (µm)	L (µH)
0	3252.307611
5	2044.318873
10	1495.283011
15	1181.365949
20	978.079007
25	835.659659
30	730.270752
35	649.12791
40	584.713537
50	488.871806
55	452.24373
60	420.947711
65	393.894024
70	370.279836
75	349.471402
80	331.001067
85	314.494719
90	299.654522
95	286.237655
100	274.049532

Table 5: Simulated Inductance vs Gap Length for the Multilayer Inductor.

The results from the simulation are close to those predicted by the mathematical modeling. To better represent this similarity both data sets were plotted on an Inductance vs Airgap graph for comparison shown in Figure 46.

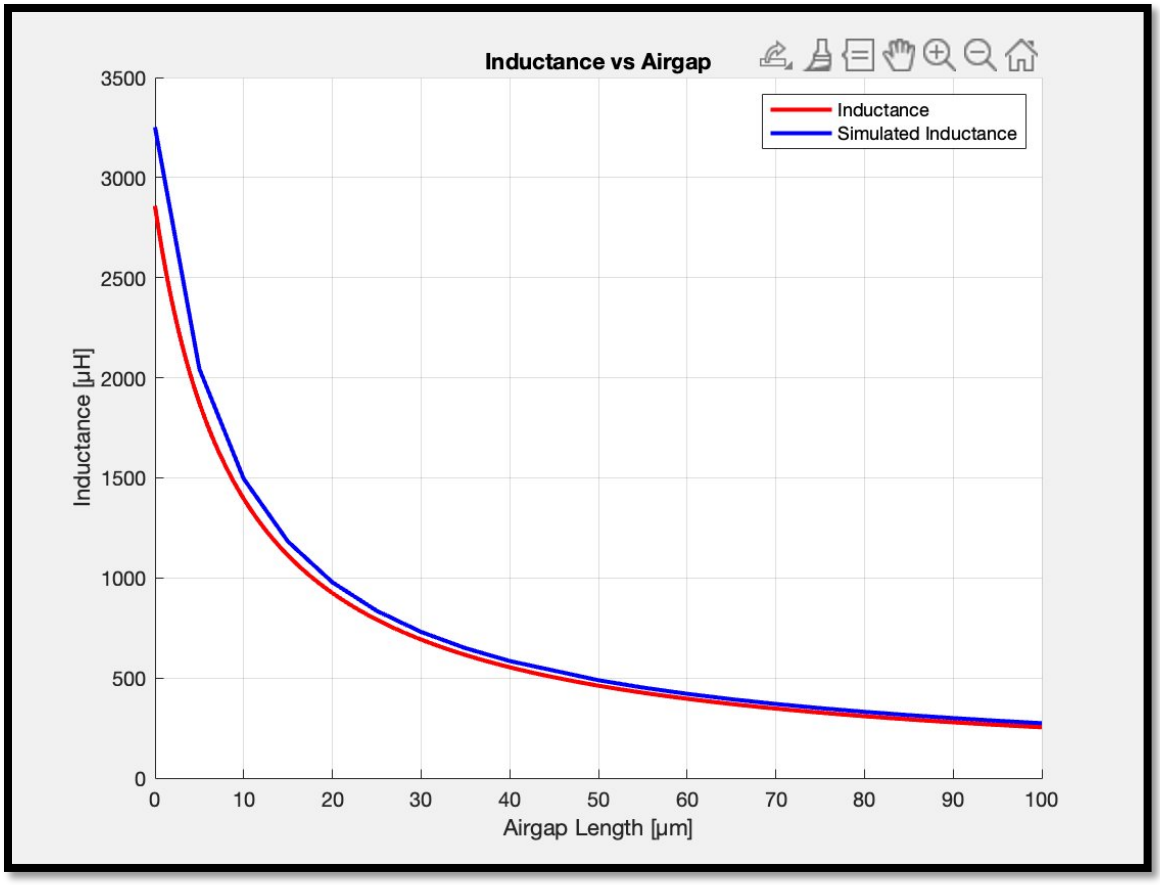

Figure 46: Graph comparing Inductance vs Airgap for the mathematical and simulated models of the multilayer inductor.

Using this data, the team assessed the practicality of using a variable inductor design in an RL filter and a boost converter. The cutoff frequency vs gap length (Figure 39) and ripple current vs gap length (Figure 40) can be reassessed using the simulated inductance data. If values match the team's previous graphs, with a small margin calculated error, then the prediction will be validated, and the team can confirm that the test circuits should perform as expected.

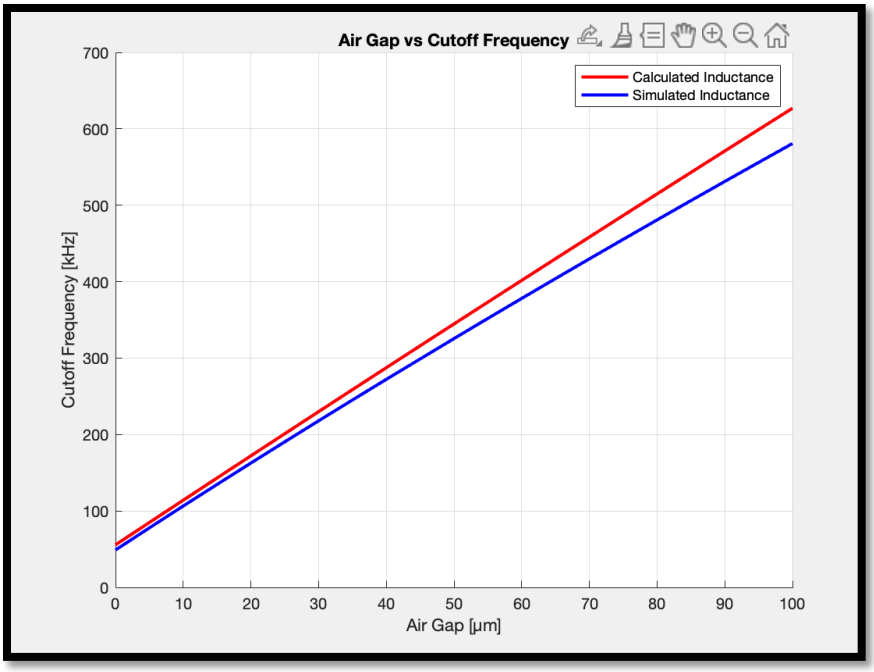

Figure 47: Graph comparing Airgap vs Cutoff frequency for the mathematical and simulated models of the multilayer inductor.

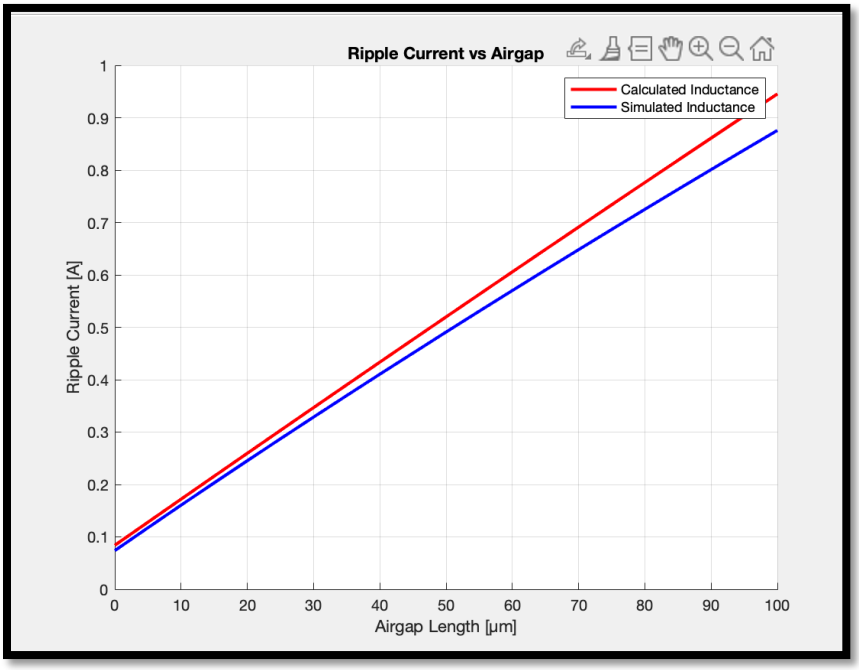

Figure 48: Graph comparing Airgap vs Ripple current for the mathematical and simulated models of the multilayer inductor.

Figure 47 and Figure 48 show that the simulated results vary little from the original in each test circuit. This confirms the validity of the use cases for each circuit described in the methodology. A variable inductor should be able to significantly adjust the cutoff frequency of a

filter and the ripple current of a boost converter at will. The linearity of each also shows that this variation will be predictable with respect to the gap length.

4.2 Physical PCB Testing Results

The following sections will expand upon the results of two different procedures and their findings. In each procedure, which can be found in Appendix A, two tests were performed. Before beginning to collect data, the team first looked at the simulated results so that expectations on what data we should have been. Keeping this in mind, testing proceeded as planned. Further discussion on why differences or data variations may have occurred are in Section 5.1.

4.2.1 Procedure 1

One-Layer Planar Inductor

The data table below shows the results of each test performed comparing the airgap length versus the recorded inductance value in a one-layer planar inductor in an EE ferrite core. Of the tests performed, there were numerous outliers and other inconsistencies within the testing rig due to uncontrollable factors, which are further discussed in Section 5.1. The team decided to use the eleven data points that were the most consistent among the data set.

One-Layer													
GapL (μm)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	Avg (μH)	SD
0	84.59	83.81	85.62	76.8	80.37	80.33	85.05	85.25	83.67	84.76	84.27	83.13818	2.77036
10	52.31	51.47	50.32	53.76	53.63	52.45	53.17	52.38	51.48	51.21	51.3	52.13455	1.08881
20	37.53	38.04	38.76	51.72	52.39	47.09	44.69	45.06	43.21	46.01	42.57	44.27909	5.01827
30	28.17	27.92	27.47	40.33	42.38	32.18	38.78	38.55	37.37	40.57	37.17	35.53545	5.56228
40	22.57	22.55	21.85	32.71	31.18	24.04	34.32	33.99	33.25	36.86	32.85	29.65182	5.66023
50	18.51	18.52	18.08	27.72	22.49	19.27	25.63	27.41	28.66	32.25	27.51	24.18636	4.99709
60	16.16	15.99	15.92	23.26	18.53	16.39	20.75	21.24	21.93	27.93	22.65	20.06818	3.85971
70	14	14.36	14.03	20.36	15.87	14.91	18.02	18.78	17.79	22.28	18.19	17.14455	2.74996
80	12.64	12.65	12.68	18.65	14.35	13.04	15.52	15.7	15.7	18.31	15.66	14.99091	2.16107
90	11.55	11.69	11.57	16.58	12.77	11.61	13.71	13.88	13.69	15.78	14.05	13.35273	1.72864
100	10.69	10.82	10.65	15.21	11.59	10.83	12.48	12.31	12.31	14.07	12.56	12.13818	1.46912

Table 6: Airgap length versus Inductance value for a one-layer planar inductor.

The following graph compares the data collected compared to the simulated and calculated data. This shows the team any differences in data, and where the deviations, if any, occurred.

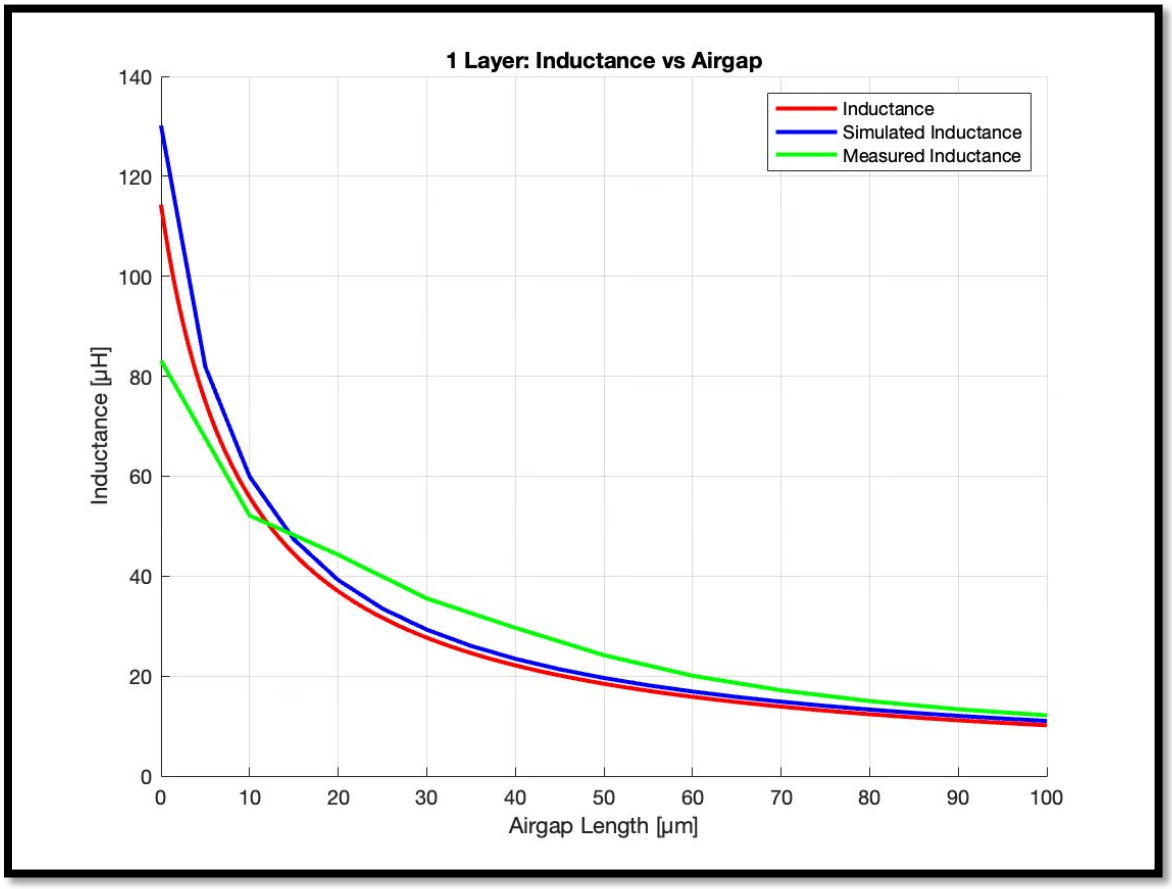

Figure 49: Inductance versus Airgap for the mathematical, simulated, and physical test results of the one-layer EE core inductor.

As shown above, the data collected from the physical testing of the one-layer planar inductor have both differences and similarities. The measured data (green) follows the general expected shape (red). From approximately 70µm to 100µm, the measured inductance follows the expected inductance (red) and the simulated inductance value (blue).

The largest difference occurs from approximately 20µm to 50µm. For each of these values and those between, they are roughly 9.6% to 21.4% greater than the expected values (red). These variations are generally acceptable because they are within a 20% +/- predicted values range. Overall, it can be said that the teams' result for this test displays that the behavior of a one-layer planar inductor is comparable to other types of inductors when airgap length is increased.

Multi-Layer Planar Inductor

The data table below shows the results of each test performed comparing the airgap length versus the recorded inductance value in a multi-layer planar inductor in an EE ferrite core.

Five-Layer													
GapL (μm)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	L (μH)	Avg (μH)	SD
0	2190.5	2159.4	2027.4	2178	2132.8	2159	2202.6	2227.7	2262	2277.1	2272.8	2189.936	76.7088
10	1334.5	1398.9	1184.8	1291.9	1314.3	1363.7	1381.2	1507.3	1475.2	1438.9	1348.1	1367.164	89.899
20	984.02	1043.9	961.16	953.2	1261.3	1252.8	1165.4	1173.2	1094.8	1050.8	1125.7	1096.935	109.285
30	711.85	804.61	692.85	865.98	1054.2	1036	998.38	863.71	830.55	804.17	856.4	865.3364	120.22
40	576.53	634.12	573.48	731.24	826.05	803.3	768.38	734.75	676.97	634.87	720.65	698.2127	86.1247
50	479.46	513.35	497.85	584.72	661.62	647.2	593.73	556.03	513.22	504.06	586.36	557.9636	61.796
60	419.61	436.23	432.28	523.23	568.83	578.25	504.62	457.26	437.9	419.39	438.42	474.1836	59.3116
70	365.92	394.03	388.17	444.33	489.4	471.22	434.02	380.05	383.69	357.84	417.23	411.4455	43.3838
80	327.46	352.42	346.03	353.89	397.18	376.12	379.45	332.11	334.9	316.56	370.2	353.3018	25.0494
90	296.77	318.43	306.24	310.04	341.34	326.4	333.85	300.23	300.31	290.48	313.96	312.55	16.1082
100	270.17	284.33	282.41	282.19	291.81	290.96	290.69	270.37	275.57	263.77	278.53	280.0727	9.36874

Table 7: Airgap length versus Inductance value for a multi-layer planar inductor.

The following graph compares the data collected compared to the simulated data. This shows the team any differences in data, and where the deviations, if any, occurred.

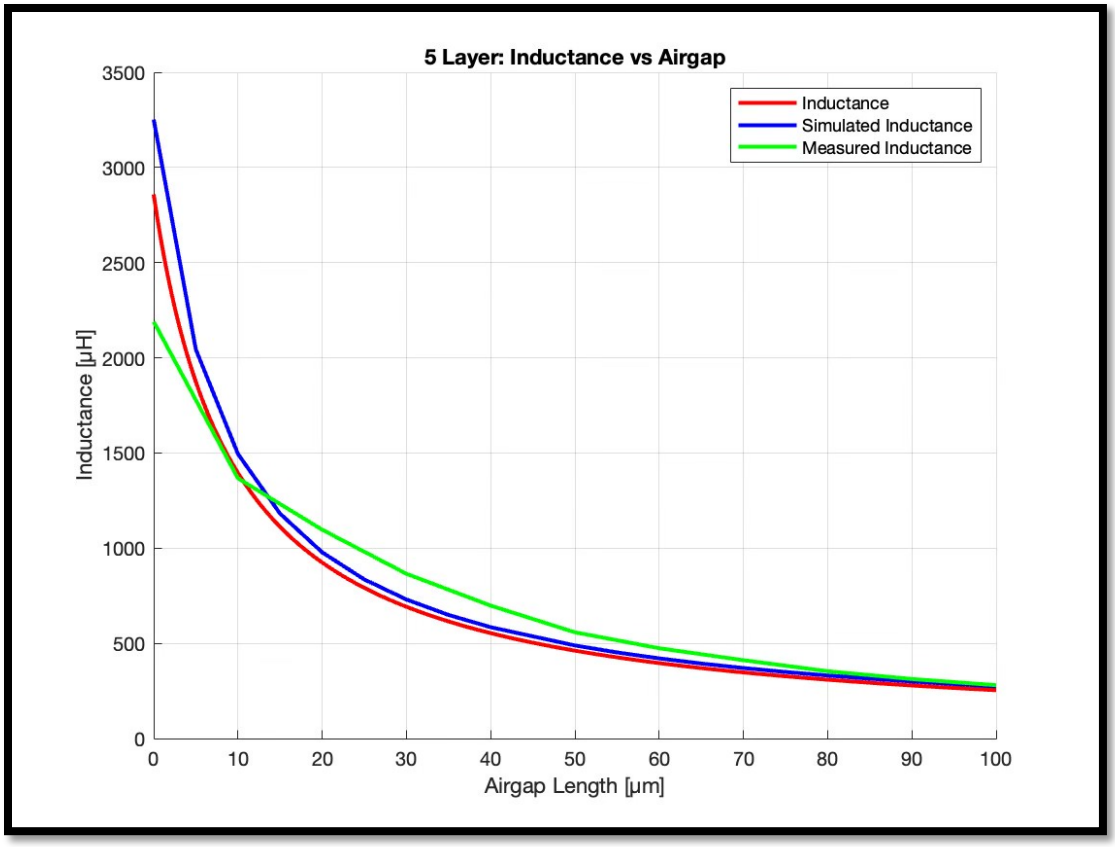

Figure 50: Inductance versus Airgap for the mathematical, simulated, and physical test results of the multi-layer EE core inductor.

As shown above, the data collected from the physical testing of the multi-layer planar inductor are very similar to the simulated and calculated data. There are some variations in the measured inductance (green) from approximately 20µm to 50µm, but otherwise fits the theoretical (red) and simulated (blue) data lines nicely. Additionally, there is a very small deviation from roughly 0µm to slightly less than 10µm.

At 0µm from the measured data versus the theoretical data (red), there is approximately a 17.4% difference in expected inductance values. For the differences between 20µm and 50µm, there is approximately 12.2% to 13.4% difference in the measured inductance value (green), and the theoretical (red). Overall, the teams' results for this procedure are acceptable and prove that a multi-layer planar inductor can behave similarly to other types of inductors when the airgap length is changed.

4.2.2 Procedure 2

Lowpass Filter

The data table below shows the results of each test performed comparing the airgap length to the recorded frequency value when the f3dB frequency is approximately -3.02535Hz. These tests were performed using the teams' multi-layer inductor in a lowpass circuit (see Figure 13). Of the tests performed, there were outliers and inconsistencies within the testing rig due to uncontrollable factors, which are further discussed in Section 5.1. The team decided to use the eleven data points that were the most consistent among the data set.

Low Pass Filter					
Gap length (µm)	Test 1 (kHz)	Test 2 (kHz)	Test 3 (kHz)	Average (kHz)	Standard Deviation
0	80	90	89	86.33333	5.507571
10	115	128	122	121.6667	6.506407
20	135	139	135	136.3333	2.309401
30	185	152	153	163.3333	18.77054
40	240	169	186	198.3333	37.072
50	305	199	255	253	53.02829
60	385	269	323	325.6667	58.04596
70	440	345	389	391.3333	47.54296
80	520	401	445	455.3333	60.16921
90	565	469	512	515.3333	48.08673
100	575	527	569	557	26.15339

Table 8: Airgap Length versus Frequency value for a multi-layer inductor in a lowpass circuit.

The following graph compares the data collected compared to the simulated data. This shows the team any differences in data, and where the deviations, if any, occurred.

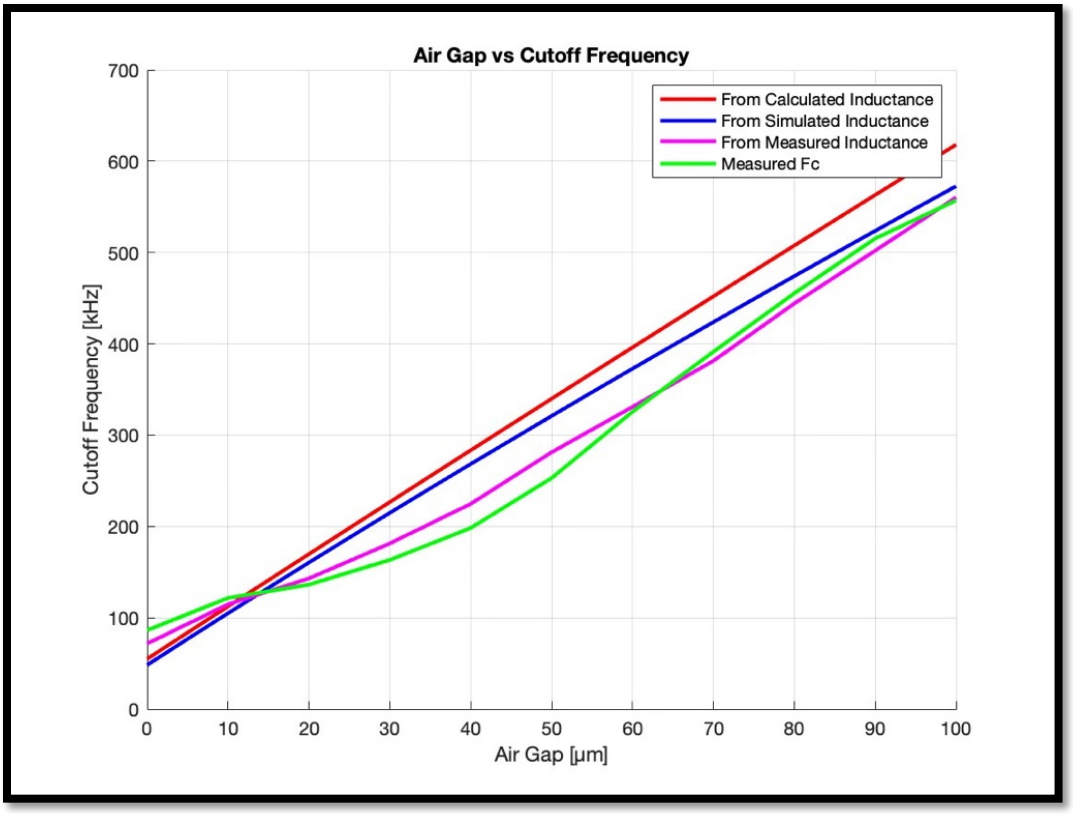

Figure 51: Frequency value to Airgap Length for the mathematical, simulated, and physical test results for a multi-layer inductor in a lowpass filter.

The data displayed above shows that the measured cutoff frequency (green), behaves similarly to the simulated data (blue), but is not a perfect match. It is, however, behaving in a comparable manner to the measured cutoff frequency (pink), and deviates only slightly. Overall, the data for the lowpass filter using a multi-layer variable planar inductor behaves in a manner that is expected and acceptable.

Highpass Filter

The data table below shows the results of each test performed comparing the airgap length to the recorded frequency value when the f3dB frequency is approximately -3.02535Hz. These tests were performed using the teams' multi-layer inductor in a highpass circuit (see Figure 15).

High Pass					
Gap L (µm)	Test 1 (KHz)	Test 2 (KHz)	Test 3 (KHz)	Average	SD
0	82	82	82	82	0
10	113	113	109	111.6667	2.309401
20	125	129	114	122.6667	7.767453
30	136	143	130	136.3333	6.506407
40	153	158	153	154.6667	2.886751
50	176	187	191	184.6667	7.767453
60	197	239	233	223	22.71563
70	243	274	270	262.3333	16.86219
80	289	314	306	303	12.76715
90	340	349	344	344.3333	4.50925
100	389	388	385	387.3333	2.081666

Table 9: Airgap Length versus Frequency value for a multi-layer inductor in a highpass circuit.

The following graph compares the data collected compared to the simulated data. This shows the team any differences in data, and where the deviations, if any, occurred.

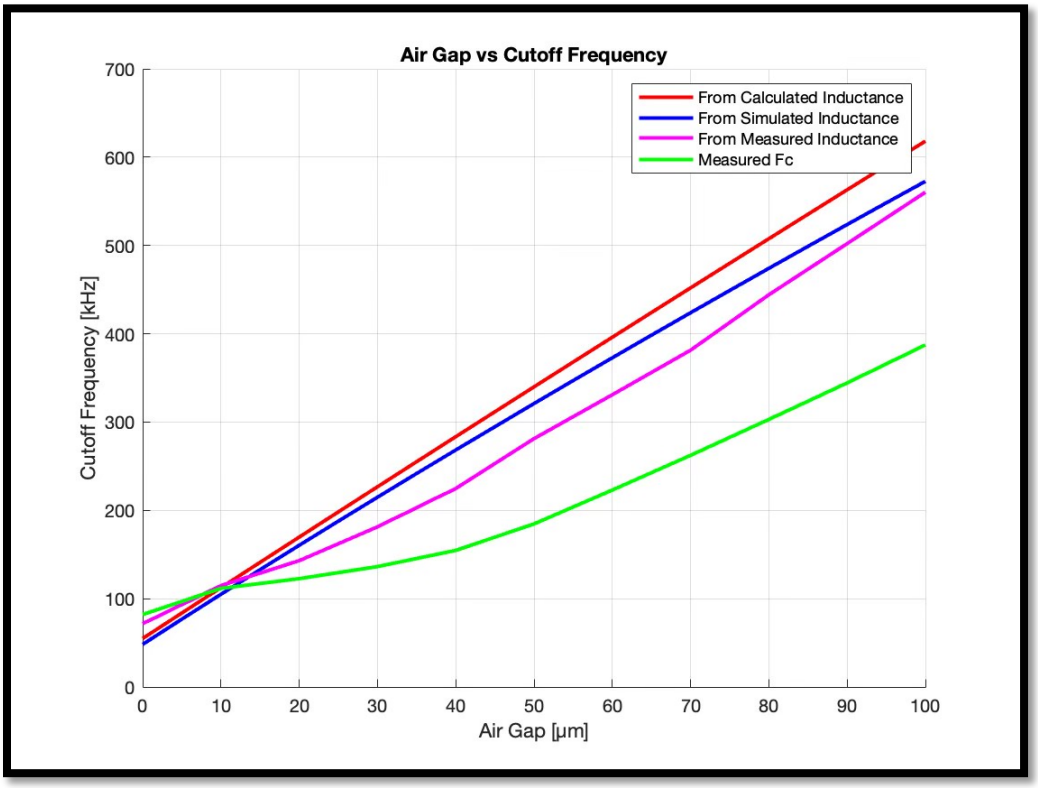

Figure 52: Frequency value to Airgap Length for the mathematical, simulated, and physical test results for a multi-layer inductor in a highpass filter.

The measured cutoff frequency for the highpass filter (green) using a multi-layer variable planar inductor does not behave in a way that was expected. It entirely deviates from the simulated

values (blue) and is approximately 31.8% below the measured cutoff frequency (pink). The team discusses potential sources of error in Section 5, but overall, there is little explanation for why these results occurred.

Overall Results

Cutoff, or f3dB frequencies, will be the same for a low pass or a high pass filter given that the parameters, such as resistance value, also stay the same. That means that the results for the low pass and high pass filter should look the same. The graph below shows the results of both filters averaged together.

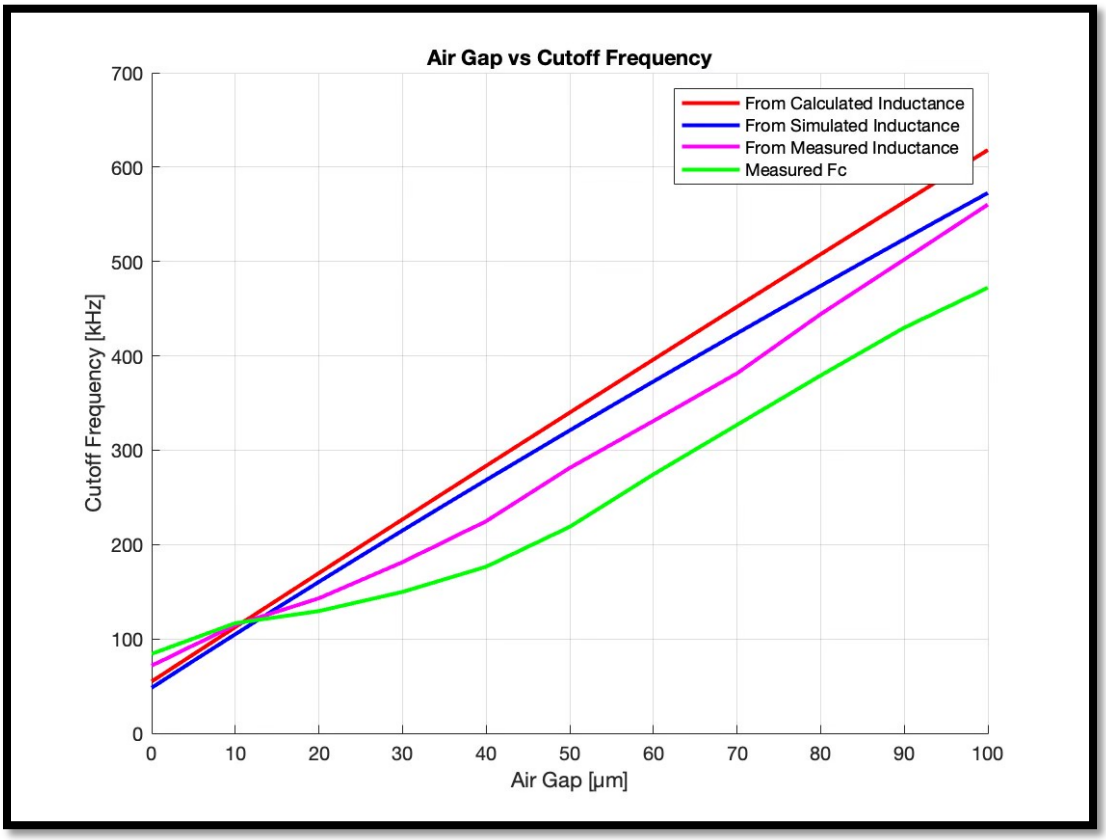

Figure 53: Combined data for lowpass and highpass filter cutoff frequencies versus calculated, simulated, and measured inductance.

The red line represents the calculated cutoff frequency using calculated inductance values, and the blue line represents the calculated cutoff frequency using simulated inductance values. Additionally, the pink line is the calculated cutoff frequency using the average measured inductance values from the testing rig, and the green line is simply the measured cutoff frequency.

As seen in the graph above, the measured cutoff frequency for the combined lowpass and highpass filter (green) data is quite different than the other measurements. From about 0µm to 10µm, it is approximately 47.4% greater than the simulated cutoff frequency (blue). As seen in the generalized shape of the simulated cutoff frequency, the data collected is supposed to be linear. The slope of the simulated cutoff frequency is 5. However, the measured cutoff frequency does not have a linear relationship. It is not possible to determine a slope from a non-linear data set, but it can be said that the measured cutoff frequency is approximately 26.3% lower than what it is expected to be. This could be due to a multitude of reasons including human error in operating the micrometer, which is discussed further in Section 5.1.3.

Boost Converter

When implementing the planar inductor into a boost converter the team did not notice any unexpected behavior from the circuit using a 470Ω load. There was some slight variation in voltage output and current as the gap length was increased. However, given the tools used that variation could be error. The output was relatively steady around 24V. The circuit behaved as expected up until the point where the inductance went beyond continuous conduction. The team was unable to get an accurate reading for how the ripple current changed with the inductance.

The team then used a load with a lower resistance of 200Ω, this allowed for more current to flow in the circuit. When this happened the two halves of the core seemed to stick together magnetically. This was an unexpected result and has some implications for the variable planar inductor design at higher power. If larger currents can cause the cores to magnetize, operation of the variable inductor needs to be done more carefully. To prevent magnetization the operator would need to completely stop current flow to make precise adjustments to the gap length. So, at higher power the variation of the inductance values would not be as smooth or convenient as predicted. If a gap length is set before the current is turned back on it is also not guaranteed that the gap length will remain constant if the two parts of the core start to be pulled together.

5. Discussion

5.1 Potential Errors

The following section will discuss any errors that may have occurred while performing lab testing, and how those errors may have affected the results.

5.1.1 Ferrite EE Core

The ferrite cores received in a shipment for testing may have contributed to testing errors and unexpected data variation. The core used in the Ansys Maxwell simulation, as well as the assumed permeability in mathematical or MATLAB simulations, were modeled as 'perfect'. This means that the form is completely uniform, with no imperceptible physical variations.

However, the team visually observed that many of the shipped cores had dents, chips, or other noticeable imperfections. This may have affected the team's test results because any physical imperfections would have altered the flow of flux throughout the core, the mean pathway would be shortened and would force the numerical value for flux to be smaller, which in turn lowers the flux density. The cores that arrived were also of varying sizes. Almost none of the cores had an exact matching pair, as there were tolerances on the dimensions. This error would have altered results for the one-layer and multi-layer inductor in Procedure 1.

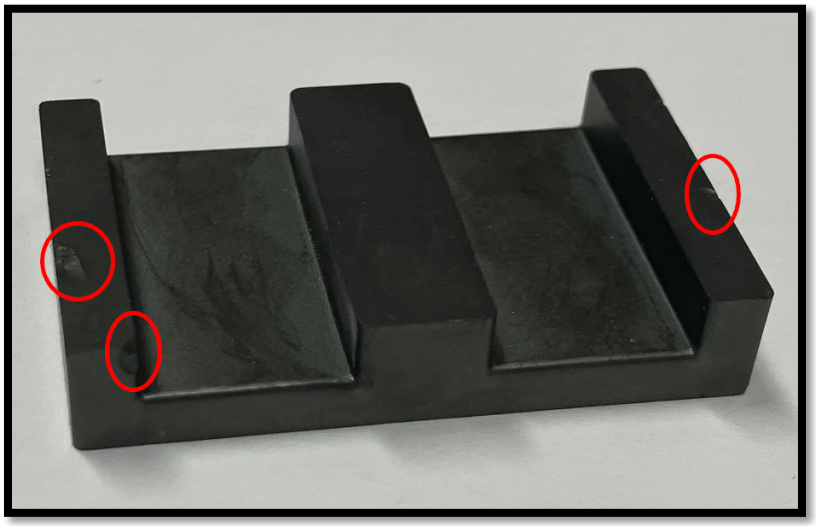

Figure 54: Photo of core highlighting the chips and dents.

Additionally, the permeability of the core can contribute to any errors. When looking at the manufacturer's data sheet, which can be found in Appendix C, the manufacturer was unable to guarantee an exact value for relative permeability (μr). They provided a range saying that the given

value of 3000 had a 20% tolerance. Given the available resources and time the team was unable to get an accurate measurement for the relative permeability so 3000 was used in both simulation and calculation.

5.1.2 PCB for Multi-Layer Planar Inductor

As outlined in the Methodology, the team had two PCB designs for the five-layer. Due to the cost and unavailability of PCBs with blind and buried vias, the team proceeded with the stacked five-layer PCB. Though it was the correct decision to make due to cost and timing of the project, the team found that the stacked configuration left room for error.

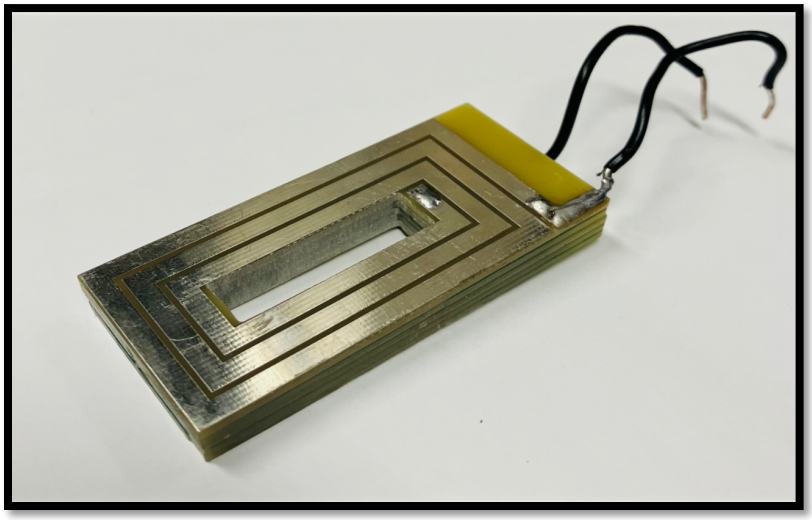

Figure 55: Final stacked 5-layer PCB.

To connect each layer, the team soldered down to the layer beneath through the vias. Though the team had designed a CAD holder to help keep the inductor flush, the team struggled to solder a five layer that was perfectly aligned. This made the PCB sit tighter in the core and there were times that the core would get caught on one of the ridges of the stacked PCB. The layers were also not perfectly flush and level. There were sizable differences in height due to the solder accumulating between the layers pushing up parts of the board.

5.1.3 Airgap Length Testing Rig

The design for the airgap rip, shown in the Methodology, was fine tuned to ensure that the inductor was as flush and stable as possible. The CAD holders for the core were designed with as low tolerance as possible and glued to the core. The clear stage was laser cut to be as close as possible to the screws used to attach the 10µ translation stage. Though the team attempted to be as

precise as possible, the cores were never perfectly aligned, and repeated tests had inconsistent data based on how the translation stage was turned.

5.2 Recommendations

The team recommends repeating testing procedures with more precise tools. Regarding the micrometer translation stage, the stage was accurate to 10 micrometers, meaning the gap length was varied by 10 micrometers for each datapoint. It could not be assumed that the micrometer translation stage would linearly increase or decrease between each 10-micrometer increment, therefore no datapoints could be taken in-between each 10-micrometer value. This resulted in large slope differences between points as shown in graphs in the Results section, such as Figure 41. A more precise, and thus a more expensive, tool to replace the micrometer stage would help show more data.

Additionally, the 10μ translation stage did not have a precise "zero" value for the team to determine as no airgap. "Zero" values represented in the Results are a result of a team member firmly pressing the cores together when measuring. A more precise translation stage could prevent the need to force a zero value for airgap.

The team also recommends finding different production companies for the cores and the PCB multilayer inductor. The EE cores came chipped from shipping and had a large tolerance of +/-20%. The team shipped ten cores, and each core had noticeable differences from each other. Additionally, the material was very delicate and often chipped if handled at too much pressure as outlined in the Potential Error section.

As for the PCB, the company that printed the inductor was unable to accommodate the 5-layer design with buried vias. Many other manufacturers either did not offer buried vias as a service or offered it at a steep price. Given more budget, the team would have ordered the buried via design over the stacked PCB design presented in the project. Because the team ordered each layer individually, the team ended up soldering each layer together resulting in possible errors in connections.

The overall rig to vary airgap was designed with a combination of designed and order parts. For this variable planar inductor to be viable by industry standards, the team recommends designing a smaller rig that would make a variable inductor as viable as a potentiometer.

5.3 Conclusion

This MQP showed proof of concept of a variable planar inductor as outlined in the problem statement. The team implemented the variable planar inductor in lowpass and highpass filters, and a DC-DC boost converter. The team was successful, bearing error discussed in section 5.1, in implementing the planar inductor in the lowpass and highpass filters and the DC-DC boost converter. With more time and money, this project could be improved to a more condensed and precise rig.

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7. Appendix

Appendix A: Physical Testing Procedures

Procedure #1:

Varying the Airgap Length vs. Inductance Values

Introduction: For this experiment, two circuits will be tested. A one-layer planar inductor attached to an LCR meter, and a multi-layer planar inductor attached to an LCR meter. We will vary the airgap in our planar inductor to observe the results as that airgap changes.

Purpose:

1. To understand what happens to the measured inductance value as the airgap length of an EE-core planar inductor increases.
2. Compare simulated/calculated results to measured results to see if the data matches and if the testing methodology is viable and repeatable in the 2023-24 Variable Planar Inductor Major Qualifying Project (MQP).

Materials:

- EE-core planar inductor,
- Airgap varying rig,
- LCR device,
- Test leads,

Part I: One-Layer Planar Inductor

Steps:

1. Begin by inserting a one-layer planar inductor into an airgap varying rig.
2. Once secure, attach the LCR meter leads to the beginning and the end of PCB trace. Ensure that PCB does not move or shift.
3. Measure an ideal zero.
    a. To do this, move the micrometer as close to zero as possible.
    b. Then, push down on the top half of the airgap rig until the LCR meter reaches the desired expected value for when the gap length is meant to be at 0µm.
4. From there, raise the micrometer until the LCR meter shows a large jump in inductance this will represent the 10µm point.

5. Raise the micrometer by 10µm until 100µm is reached.
6. Repeat 5-10 times to get range of data. Then take the average of that data as the results.

Gap Length (µm)	Inductance Value (µH)
0	
10	
20	
30	
40	
50	
60	
70	
80	
90	
100	

Table A.1: Procedure 1, Part I Testing Results

Part II: Multi-Layer Planar Inductor

Steps:

1. Begin by inserting a multi-layer planar inductor into an airgap varying rig.
2. Once secure, attach the LCR meter leads to the beginning and the end of PCB trace. Ensure Measure an ideal zero.
    a. To do this, move the micrometer as close to zero as possible.
    b. Then, push down on the top half of the airgap rig until the LCR meter reaches the desired expected value for when the gap length is meant to be at 0µm.
3. Raise the micrometer by 10µm until 100µm is reached.
4. From there, raise the micrometer until the LCR meter shows a large jump in inductance this will represent the 10µm point.
5. Repeat 5-10 times to get range of data. Then take the average of that data as the results.

Gap Length (µm)	Inductance Value (µH)
0	
10	
20	
30	
40	
50	
60	
70	
80	
90	
100	

Table A.2: Procedure 1, Part II Testing Results

Procedure #2:

Varying the Airgap Length vs. Cutoff Frequency Values

Introduction: For this experiment, we will build three circuits. A lowpass circuit, highpass circuit and boost converter. We will vary the airgap in our planar inductor to observe the results as the inductance changes.

Purpose:

1. To understand the relationship between airgap length and cutoff frequency as the length increases.
2. Compare simulated/calculated results to measured results to see if the data matches and if the testing methodology is viable and repeatable in the 2023-24 Variable Planar Inductor Major Qualifying Project (MQP).
3. **Materials:**
    - 1kΩ resistor,
    - EE-core planar inductor,
    - Airgap varying rig,
    - Power supply,
    - LCR device,
    - Alligator clips,
    - Oscilloscope,
    - Jumper wires.

Part I: Lowpass Filter

Steps:

1. Begin by creating a lowpass filter, pictured below.

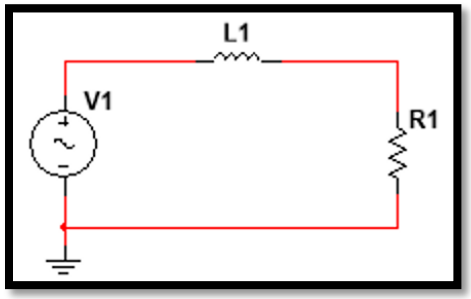


Figure A.1: A Resistor-Inductor Lowpass Circuit

2. Attach oscilloscope to either side of the resistor.
3. Set the oscilloscope power generator to 10V peak-to-peak, the frequency to 10kHz, and the impedance to high.
4. Measure an ideal zero.
    a. To do this, move the micrometer as close to zero as possible.
    b. Then, push down on the top half of the airgap rig until the LCR meter reaches the desired expected value for when the gap length is meant to be at 0µm.
5. From there, raise the micrometer until the LCR meter shows a large jump in inductance this will represent the 10µm point.
6. Adjust the frequency until an output voltage of 7.07V peak-to-peak is measured every time.
7. Raise the micrometer by 10µm and take another data point.
8. Repeat until 100µm is reached.

Input Voltage (V)	Airgap Length (µm)	Output Voltage (V)	Frequency (Hz)
10	0	7.7	
10	10	7.7	
10	20	7.7	
10	30	7.7	
10	40	7.7	
10	50	7.7	
10	60	7.7	
10	70	7.7	
10	80	7.7	
10	90	7.7	
10	100	7.7	

Table A.3: Procedure 2, Part I Testing Results

Part II: Highpass Filter

Steps:

1. Begin by creating a highpass filter, pictured below.

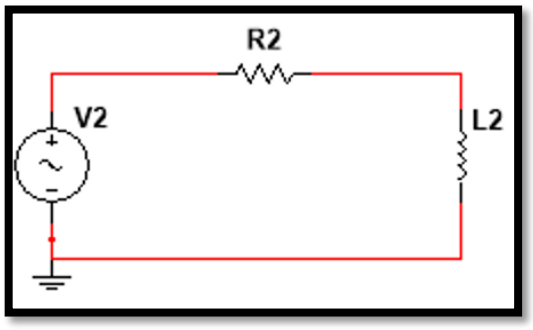


Figure A.2: A Resistor-Inductor Highpass Circuit

2. Attach oscilloscope to either side of the inductor.
3. Set the oscilloscope power generator to 10V peak-to-peak, the frequency to 10kHz, and the impedance to high.
4. Measure an ideal zero.
    a. To do this, move the micrometer as close to zero as possible.
    b. Then, push down on the top half of the airgap rig until the LCR meter reaches the desired expected value for when the gap length is meant to be at 0µm.
5. From there, raise the micrometer until the LCR meter shows a large jump in inductance this will represent the 10µm point.
6. Adjust the frequency until an output voltage of 7.07V peak-to-peak is measured every time.
7. Raise the micrometer by 10µm and take another data point.
8. Repeat until 100µm is reached.

Input Voltage (V)	Airgap Length (µm)	Output Voltage (V)	Frequency (Hz)
10	0	7.7	
10	10	7.7	
10	20	7.7	
10	30	7.7	
10	40	7.7	
10	50	7.7	
10	60	7.7	
10	70	7.7	

10	80	7.7	
10	90	7.7	
10	100	7.7	

Table A.4: Procedure 2, Part II Testing Results

Part III: Boost converter:

For this section of the procedure, we will implement the inductor in a boost converter and observe the changes in the output voltages and currents as the inductance changes.

1. Begin by creating a boost converter circuit like below.

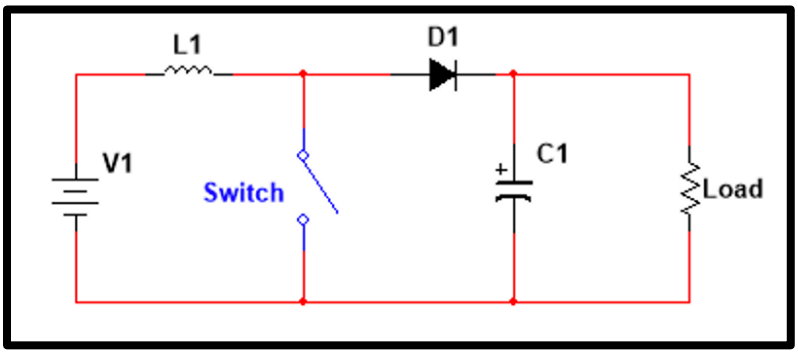


Figure A.3: Boost converter

2. Hook up a DC voltage source and control the switch with a square wave using a function generator.
3. Attach an oscilloscope and DMM to measure output voltage.
4. Measure an ideal zero.
    a. To do this, move the micrometer as close to zero as possible.
    b. Then, push down on the top half of the airgap rig until the LCR meter reaches the desired expected value for when the gap length is meant to be at 0µm.
5. From there, raise the micrometer until the LCR meter shows a large jump in inductance this will represent the 10µm point.
6. Observe the output voltage and the current running through it.
7. Raise the micrometer by 10µm and take another data point.
8. Repeat until 100µm is reached.

Appendix B: Bill of Materials

Item	Qty.	Link
Inductor		
E38/8/25-3C95 Ferrite Core	10	https://www.digikey.com/en/products/detail/ferroxcube/E38-8-25-3C95/7041492
Boost Converter		
1000 µF 50 V Aluminum Electrolytic Capacitors Radial UVR1H102 MHD	10	https://www.digikey.com/short/d47djdqw
IRF540PBF N Channel Mosfet	10	https://www.digikey.com/en/products/detail/vishay-siliconix/IRF540PBF/812042
SB550 Diode	10	https://www.digikey.com/en/products/detail/vishay-general-semiconductor-diodes-division/SB550-E3-54/754861
Misc.		
Micrometer Manual Precision Linear Translation Stage Platform Z Axis	1	https://www.amazon.com/gp/product/B07TTJ492P/ref=ewc_pr_img_1?smid=AN3QLT9N21E5P&psc=1
M4 10mm screw	lot	https://www.amazon.com/gp/product/B09VV59VSR/ref=ewc_pr_img_3?smid=ADEBTV7I8FDCW&th=1
M4 12mm screw	lot	https://www.amazon.com/gp/product/B09VV9MKGQ/ref=ewc_pr_img_1?smid=ADEBTV7I8FDCW&th=1
Eunenete 304 Stainless Steel C Clamp,1 1/2 Inch Tiger Clamp	lot	https://www.amazon.com/gp/product/B0CC4WXYXY/ref=ewc_pr_img_2?smid=AQZVZAJU5COEB&th=1

BOJACK 300 Pcs 30 Values Resistor Kit 1 Ohm - 1M Ohm with 1% 2W Metal Film Resistors Assortment	kit	https://www.amazon.com/gp/product/B09MS545M3/ref=ewc_pr_img_4?smid=A2RFXKS6GNXFWP&th=1
18 awg Solid Wire kit Electrical Wire Cable	lot	https://a.co/d/1eouxg7
282834-2 Connector	10	https://www.digikey.com/short/821rmrnw
300 Pcs M4 Screw Assortment Button Head Socket Cap	kit	https://www.amazon.com/gp/product/B0BZ6Y8KRD/ref=ox_sc_act_title_2?smid=A23XVIPJ96UME3&psc=1
Clear Rubber Stoppers Bumpers Self Adhesive	kit	https://www.amazon.com/gp/product/B09WRFDMKY/ref=ox_sc_act_title_1?smid=A16FUM8J3D9097&psc=1
Proster LCR Meter Digital LCR Multimeter Capacitance Resistance Inductance Measuring Meter with LCD Over-Range Display	kit	https://a.co/d/e7UabZ5

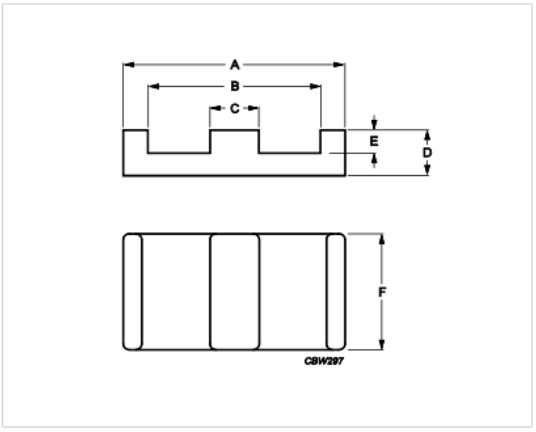
Appendix C: Specification Sheets

Ferrite Core

Product specifications

FERROXCUBE
A YAGEO COMPANY

Core **E38/8/25**



Effective parameters			
	Parameter	**Value**	**Unit**
Σ(I/A)	*core factor (C1)*	0.272	mm^{-1}
Ve	*effective volume*	10200	mm^3
Le	*effective length*	52.4	mm
Ae	*effective area*	194	mm^2
Amin	*minimum area*	194	mm^2
m	*E38/8/25*	≈ 25	g/pcs

Dimensions for product: E38/8/25						
	Nom	**Tol +**	**Tol -**	**Max**	**Min**	**Unit**
A	38.10	0.76	0.76	38.86	37.34	mm
B					30.23	mm
C	7.60	0.20	0.20	7.80	7.40	mm
D	8.26	0.13	0.13	8.39	8.13	mm
E	4.45	0.13	0.13	4.58	4.32	mm
F	25.40	0.51	0.51	25.91	24.89	mm

Inductance factor				
Material	**Value**	**Tol +**	**Tol -**	**Unit**
3C92	6100	25%	25%	$nH/turns^2$
3C95	9600	25%	25%	$nH/turns^2$
3C96	7140	25%	25%	$nH/turns^2$
3C97	9600	25%	25%	$nH/turns^2$
3F36	5100	25%	25%	$nH/turns^2$
3F4	3880	25%	25%	$nH/turns^2$

Power loss: 3C92				
Measuring conditions			**Max**	**Unit**
100 kHz	200 mT	100 °C	5.100	W/set
Power loss: 3C95				
Measuring conditions			**Max**	**Unit**
100 kHz	200 mT	100 °C	4.900	W/set
100 kHz	200 mT	25 °C	5.300	W/set

2016

Core **E38/8/25**

Power loss: 3C96				
Measuring conditions			Max	Unit
100 kHz	200 mT	100 °C	4.600	W/set
400 kHz	50 mT	100 °C	1.800	W/set
Power loss: 3C97				
Measuring conditions			Max	Unit
100 kHz	200 mT	60 °C	5.100	W/set
100 kHz	200 mT	120 °C	4.900	W/set
100 kHz	200 mT	140 °C	6.100	W/set
Power loss: 3F36				
Measuring conditions			Max	Unit
500 kHz	50 mT	100 °C	1.500	W/set
500 kHz	100 mT	100 °C	12.000	W/set
Power loss: 3F4				
Measuring conditions			Max	Unit
1000 kHz	30 mT	100 °C	3.100	W/set
3000 kHz	10 mT	100 °C	5.100	W/set

Bsat					
Measuring conditions			Material	Min	Unit
25 kHz	250 A/m	100 °C	3C92	370	mT
25 kHz	250 A/m	100 °C	3C95	330	mT
25 kHz	250 A/m	100 °C	3C96	340	mT
25 kHz	250 A/m	100 °C	3C97	330	mT
25 kHz	250 A/m	100 °C	3F36	340	mT
25 kHz	250 A/m	100 °C	3F4	330	mT

Figure C.1: Data sheet for Core E38/8/25.

ALUMINUM ELECTROLYTIC CAPACITORS

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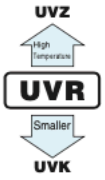
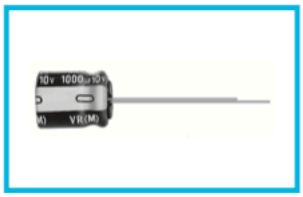
Miniature Sized

- Standard series for entertainment electronics.
- Compliant to the RoHS directive (2011/65/EU,(EU)2015/863).





■Specifications

Item	Performance Characteristics
Category Temperature Range	−40 to +85˚C (6.3V to 400V), −25 to +85˚C (450V)
Rated Voltage Range	6.3 to 450V
Rated Capacitance Range	1 to 22000μF
Capacitance Tolerance	±20% at 120Hz, 20˚C
Leakage Current ※	Rated voltage (V) | 6.3 to 100V: After 1 minute's application of rated voltage at 20˚C, leakage current is not more than 0.03CV(μA). After 2 minutes' application of rated voltage at 20˚C, leakage current is not more than 0.01CV(μA). | 160 to 450V: After 1 minute's application of rated voltage at 20˚C, CV ≦ 1000 : I = 0.1CV+40μA or less; CV > 1000 : I = 0.04CV+100 (μA) or less
Tangent of loss angle (tan δ)	For capacitance of more than 1000μF, add 0.02 for every increase of 1000μF. Measurement frequency : 120Hz at 20˚C

Rated voltage (V)	6.3	10	16	25	35	50	63	100	160 to 315	350 to 450
tan δ (max.)	0.28	0.24	0.20	0.16	0.14	0.12	0.10	0.08	0.20	0.25

Stability at Low Temperature — Measurement frequency : 120Hz

Rated voltage (V)		6.3	10	16	25	35	50	63	100	160 to 200	250 to 350	400	450
Impedance ratio (max.)	Z(−25˚C) / Z(+20˚C)	5	4	3	2	2	2	2	2	3	4	6	15
	Z(−40˚C) / Z(+20˚C)	12	10	8	5	4	3	3	3	4	8	10	—

Endurance — The specifications listed at right shall be met when the capacitors are restored to 20°C after the rated voltage is applied for 2000 hours at 85°C.

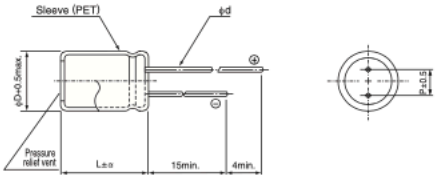
Capacitance change	Within ±20% of the initial capacitance value
tan δ	200% or less than the initial specified value
Leakage current	Less than or equal to the initial specified value

Shelf Life — After storing the capacitors under no load at 85˚C for 1000 hours and then performing voltage treatment based on JIS C 5101-4 clause 4.1 at 20°C, they shall meet the specified values for the endurance characteristics listed above.

Marking — Printed with white color letter on black sleeve.

※ I : Leakage Current (μA), C : Rated Capacitance (μF), V : Rated Voltage (V)

■Radial Lead Type



(mm)

φD	8	10	12.5	16	18
P	3.5	5.0	5.0	7.5	7.5
φd	0.6	0.6	0.6	0.8	0.8

α	
	(L<20) 1.5
	(L≧20) 2.0

- Please refer to the Guidelines for Aluminum Electrolytic Capacitors for end seal configuration information.

Type numbering system (Example : 10V 3300μF)

1	2	3	4	5	6	7	8	9	10	11	12
U	V	R	1	A	3	3	2	M	H	D	

Size code
Configuration※
Capacitance tolerance (±20%)
Rated capacitance (3300μF)
Rated voltage (10V)
Series name
Type

※ Configuration

φ D	Pb-free leadwire Pb-free PET sleeve
8 · 10	PD
12.5 to 18	HD

● Frequency coefficient of rated ripple current

V	Cap.(μF) \ Frequency	50Hz	120Hz	300Hz	1 kHz	10kHz or more
6.3 to 100	33 to 47	0.75	1.00	1.35	1.57	2.00
	100 to 470	0.80	1.00	1.23	1.34	1.50
	1000 to 22000	0.85	1.00	1.10	1.13	1.15
160 to 450	1 to 220	0.80	1.00	1.25	1.40	1.60
	330	0.90	1.00	1.10	1.13	1.15

●Dimension table in next page.

CAT.8100M

UVR

■ Dimensions

Rated Voltage (V) (code)	Rated Capacitance (μF)	Case Size φD×L (mm)	tan δ	Leakage Current (μA) at 20℃ after 1 minute	Leakage Current (μA) at 20℃ after 2 minutes	Rated Ripple (mArms) (85℃/120Hz)	Part Number
6.3 (0J)	1000	8×11.5	0.28	189	63	540	UVR0J102MPD
	2200	10×20	0.30	415.8	138.6	1000	UVR0J222MPD
	3300	10×20	0.32	623.7	207.9	1190	UVR0J332MPD
	4700	12.5×20	0.34	888.3	296.1	1550	UVR0J472MHD
	6800	12.5×25	0.38	1285.2	428.4	1920	UVR0J682MHD
	10000	16×25	0.46	1890	630	2350	UVR0J103MHD
	15000	16×35.5	0.56	2835	945	2850	UVR0J153MHD
	22000	18×40	0.70	4158	1386	3350	UVR0J223MHD
10 (1A)	1000	10×12.5	0.24	300	100	650	UVR1A102MPD
	2200	10×20	0.26	660	220	1100	UVR1A222MPD
	3300	12.5×20	0.28	990	330	1450	UVR1A332MHD
	4700	12.5×25	0.30	1410	470	1800	UVR1A472MHD
	6800	16×25	0.34	2040	680	2250	UVR1A682MHD
	10000	16×35.5	0.42	3000	1000	2700	UVR1A103MHD
	15000	18×35.5	0.52	4500	1500	3100	UVR1A153MHD
16 (1C)	330	8×11.5	0.20	158.4	52.8	370	UVR1C331MPD
	470	8×11.5	0.20	225.6	75.2	440	UVR1C471MPD
	1000	10×16	0.20	480	160	790	UVR1C102MPD
	2200	12.5×20	0.22	1056	352	1300	UVR1C222MHD
	3300	12.5×25	0.24	1584	528	1700	UVR1C332MHD
	4700	16×25	0.26	2256	752	2100	UVR1C472MHD
	6800	16×35.5	0.30	3264	1088	2650	UVR1C682MHD
	10000	18×35.5	0.38	4800	1600	2950	UVR1C103MHD
25 (1E)	220	8×11.5	0.16	165	55	330	UVR1E221MPD
	330	10×12.5	0.16	247.5	82.5	440	UVR1E331MPD
	470	10×12.5	0.16	352.5	117.5	550	UVR1E471MPD
	1000	10×20	0.16	750	250	960	UVR1E102MPD
	2200	12.5×25	0.18	1650	550	1550	UVR1E222MHD
	3300	16×25	0.20	2475	825	1980	UVR1E332MHD
	4700	16×30.5	0.22	3525	1175	2450	UVR1E472MHD
	6800	18×35.5	0.26	5100	1700	2900	UVR1E682MHD
35 (1V)	220	10×12.5	0.14	231	77	385	UVR1V221MPD
	330	10×12.5	0.14	346.5	115.5	490	UVR1V331MPD
	470	10×16	0.14	493.5	164.5	650	UVR1V471MPD
	1000	12.5×20	0.14	1050	350	1150	UVR1V102MHD
	2200	16×25	0.16	2310	770	1800	UVR1V222MHD
	3300	16×35.5	0.18	3465	1155	2280	UVR1V332MHD
	4700	18×35.5	0.20	4935	1645	2700	UVR1V472MHD

For cut leads, formed leads or taped parts, please add the appropriate code after the size code (12th digit).
If there is no size code in the part number, please add size code "1" and then add the appropriate code.

UVR

■ Dimensions

Rated Voltage (V) (code)	Rated Capacitance (μF)	Case Size φD×L (mm)	tan δ	Leakage Current (μA) at 20℃ after 1 minute	Leakage Current (μA) at 20℃ after 2 minutes	Rated Ripple (mArms) (85℃/120Hz)	Part Number
50 (1H)	100	8×11.5	0.12	150	50	260	UVR1H101MPD
	220	10×12.5	0.12	330	110	430	UVR1H221MPD
	330	10×16	0.12	495	165	590	UVR1H331MPD
	470	12.5×20	0.12	705	235	760	UVR1H471MHD
	1000	12.5×25	0.12	1500	500	1350	UVR1H102MHD
	2200	16×35.5	0.14	3300	1100	2100	UVR1H222MHD
	3300	18×35.5	0.16	4950	1650	2500	UVR1H332MHD
63 (1J)	100	10×12.5	0.10	189	63	300	UVR1J101MPD
	220	10×16	0.10	415.8	138.6	490	UVR1J221MPD
	330	10×20	0.10	623.7	207.9	710	UVR1J331MPD
	470	12.5×20	0.10	888.3	296.1	900	UVR1J471MHD
	1000	16×25	0.10	1890	630	1300	UVR1J102MHD
	2200	18×35.5	0.12	4158	1386	2300	UVR1J222MHD
100 (2A)	33	8×11.5	0.08	99	33	180	UVR2A330MPD
	47	10×12.5	0.08	141	47	230	UVR2A470MPD
	100	10×20	0.08	300	100	370	UVR2A101MPD
	220	12.5×25	0.08	660	220	620	UVR2A221MHD
	330	12.5×25	0.08	990	330	760	UVR2A331MHD
	470	16×25	0.08	1410	470	1000	UVR2A471MHD
	1000	18×40	0.08	3000	1000	1380	UVR2A102MHD
160 (2C)	10	8×11.5	0.20	164	—	80	UVR2C100MPD
	22	10×16	0.20	240.8	—	155	UVR2C220MPD
	33	10×20	0.20	311.2	—	205	UVR2C330MPD
	47	12.5×20	0.20	400.8	—	270	UVR2C470MHD
	100	12.5×25	0.20	740	—	430	UVR2C101MHD
	220	16×35.5	0.20	1508	—	800	UVR2C221MHD
	330	18×40	0.20	2212	—	940	UVR2C331MHD
200 (2D)	4.7	8×11.5	0.20	134	—	55	UVR2D4R7MPD
	10	10×12.5	0.20	180	—	95	UVR2D100MPD
	22	10×20	0.20	276	—	170	UVR2D220MPD
	33	12.5×20	0.20	364	—	230	UVR2D330MHD
	47	12.5×20	0.20	476	—	270	UVR2D470MHD
	100	16×30.5	0.20	900	—	530	UVR2D101MHD
	220	18×35.5	0.20	1860	—	810	UVR2D221MHD
250 (2E)	3.3	8×11.5	0.20	122.5	—	46	UVR2E3R3MPD
	4.7	8×11.5	0.20	147	—	55	UVR2E4R7MPD
	10	10×16	0.20	200	—	105	UVR2E100MPD
	22	12.5×20	0.20	320	—	190	UVR2E220MHD
	33	12.5×20	0.20	430	—	230	UVR2E330MHD
	47	12.5×25	0.20	570	—	300	UVR2E470MHD
	100	16×30.5	0.20	1100	—	520	UVR2E101MHD

For cut leads, formed leads or taped parts, please add the appropriate code after the size code (12th digit).
If there is no size code in the part number, please add size code "1" and then add the appropriate code.

CAT.8100M

ALUMINUM ELECTROLYTIC CAPACITORS

nichicon

UVR

■ Dimensions

Rated Voltage (V) (code)	Rated Capacitance (μF)	Case Size φD×L (mm)	tan δ	Leakage Current (μA) at 20℃ after 1 minute	Leakage Current (μA) at 20℃ after 2 minutes	Rated Ripple (mArms) (85℃/120Hz)	Part Number
315 (2F)	2.2	8×11.5	0.20	109.3	—	33	UVR2F2R2MPD
	3.3	10×12.5	0.20	141.58	—	55	UVR2F3R3MPD
	4.7	10×12.5	0.20	159.22	—	65	UVR2F4R7MPD
	10	10×20	0.20	226	—	115	UVR2F100MPD
	22	12.5×20	0.20	377.2	—	190	UVR2F220MHD
	33	16×25	0.20	515.8	—	275	UVR2F330MHD
	47	16×25	0.20	692.2	—	340	UVR2F470MHD
	100	18×35.5	0.20	1360	—	560	UVR2F101MHD
350 (2V)	2.2	8×11.5	0.25	117	—	38	UVR2V2R2MPD
	3.3	10×12.5	0.25	146.2	—	55	UVR2V3R3MPD
	4.7	10×12.5	0.25	165.8	—	65	UVR2V4R7MPD
	10	10×20	0.25	240	—	115	UVR2V100MPD
	22	12.5×25	0.25	408	—	200	UVR2V220MHD
	33	16×25	0.25	562	—	275	UVR2V330MHD
	47	16×35.5	0.25	758	—	380	UVR2V470MHD
	100	18×40	0.25	1500	—	590	UVR2V101MHD
400 (2G)	1	8×11.5	0.25	80	—	25	UVR2G010MPD
	2.2	10×12.5	0.25	128	—	45	UVR2G2R2MPD
	3.3	10×12.5	0.25	152.8	—	55	UVR2G3R3MPD
	4.7	10×16	0.25	175.2	—	70	UVR2G4R7MPD
	10	12.5×20	0.25	260	—	130	UVR2G100MHD
	22	16×25	0.25	452	—	240	UVR2G220MHD
	33	16×30.5	0.25	628	—	300	UVR2G330MHD
	47	16×35.5	0.25	852	—	370	UVR2G470MHD
450 (2W)	1	8×11.5	0.25	85	—	23	UVR2W010MPD
	2.2	10×12.5	0.25	139	—	35	UVR2W2R2MPD
	3.3	10×16	0.25	159.4	—	45	UVR2W3R3MPD
	4.7	10×20	0.25	184.6	—	55	UVR2W4R7MPD
	10	12.5×20	0.25	280	—	90	UVR2W100MHD
	22	16×25	0.25	496	—	165	UVR2W220MHD
	33	16×35.5	0.25	694	—	230	UVR2W330MHD
	47	18×40	0.25	946	—	300	UVR2W470MHD

For cut leads, formed leads or taped parts, please add the appropriate code after the size code (12th digit).
If there is no size code in the part number, please add size code "1" and then add the appropriate code.

• For formed lead or taped product specifications and minimum order quantity, please refer to the Guidelines for Aluminum Electrolytic Capacitors.

CAT.8100M

Figure C.2: Datasheet for Aluminum Electrolytic Capacitors.

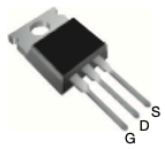
VISHAY
www.vishay.com

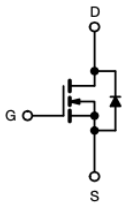
IRF540

Vishay Siliconix

Power MOSFET

TO-220AB





N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Available
RoHS* Available
HALOGEN FREE Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY		
V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.077
Q_g max. (nC)	72	
Q_{gs} (nC)	11	
Q_{gd} (nC)	32	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF540PbF
Lead (Pb)-free and halogen-free	IRF540PbF-BE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	100	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	28	A
		T_C = 100 °C		20	
Pulsed drain current [a]			I_{DM}	110	
Linear derating factor				1.0	W/°C
Single pulse avalanche energy [b]			E_{AS}	230	mJ
Repetitive avalanche current [a]			I_{AR}	28	A
Repetitive avalanche energy [a]			E_{AR}	15	mJ
Maximum power dissipation	T_C = 25 °C		P_D	150	W
Peak diode recovery dV/dt [c]			dV/dt	5.5	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d]	For 10 s			300	
Mounting torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 440 µH, R_g = 25 Ω, I_{AS} = 28 A (see fig. 12)
c. I_{SD} ≤ 28 A, dI/dt ≤ 170 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C
d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	100	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.13	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 17 A [b]	-	-	0.077	Ω
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 17 A [b]	8.7	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	1700	-	pF
Output capacitance	C_{oss}		-	560	-	
Reverse transfer capacitance	C_{rss}		-	120	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 17 A, V_{DS} = 80 V, see fig. 6 and 13 [b]	-	-	72	nC
Gate-source charge	Q_{gs}		-	-	11	
Gate-drain charge	Q_{gd}		-	-	32	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 17 A, R_g = 9.1 Ω, R_D = 2.9 Ω, see fig. 10 [b]	-	11	-	ns
Rise time	t_r		-	44	-	
Turn-off delay time	$t_{d(off)}$		-	53	-	
Fall time	t_f		-	43	-	
Gate input resistance	R_g	f = 1 MHz, open drain	0.5	-	3.6	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	28	A
Pulsed diode forward current [a]	I_{SM}		-	-	110	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 28 A, V_{GS} = 0 V [b]	-	-	2.5	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = 17 A, dI/dt = 100 A/µs [b]	-	180	360	ns
Body diode reverse recovery charge	Q_{rr}		-	1.3	2.8	µC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

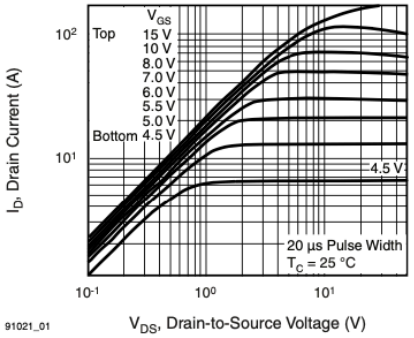


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

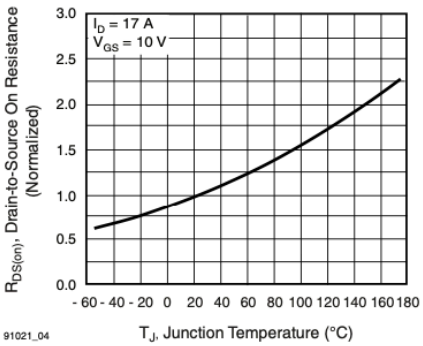


Fig. 4 - Normalized On-Resistance vs. Temperature

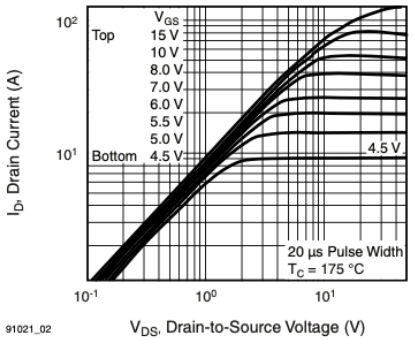


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

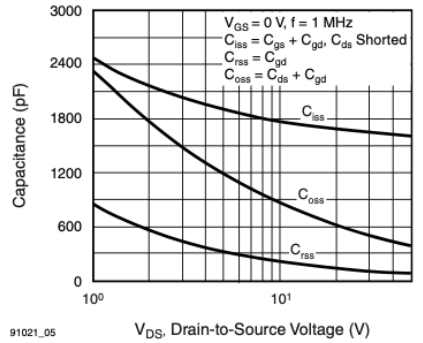


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

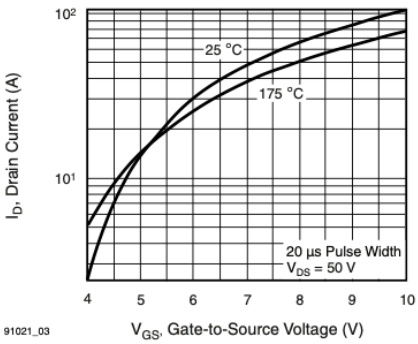


Fig. 3 - Typical Transfer Characteristics

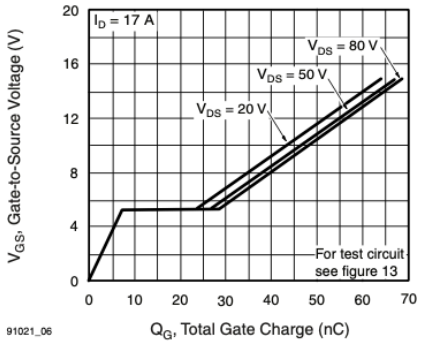


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

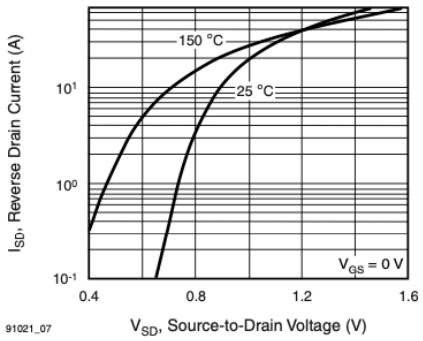


Fig. 7 - Typical Source-Drain Diode Forward Voltage

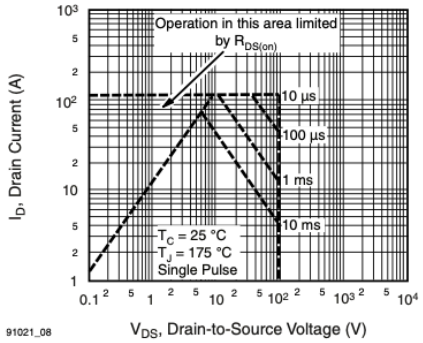


Fig. 8 - Maximum Safe Operating Area

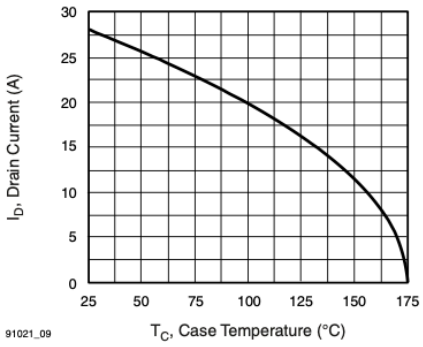


Fig. 9 - Maximum Drain Current vs. Case Temperature

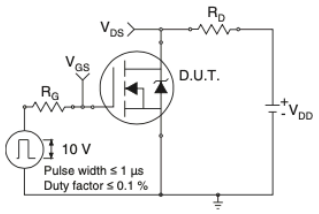


Fig. 10a - Switching Time Test Circuit

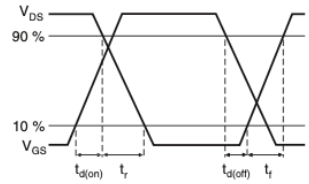


Fig. 10b - Switching Time Waveforms

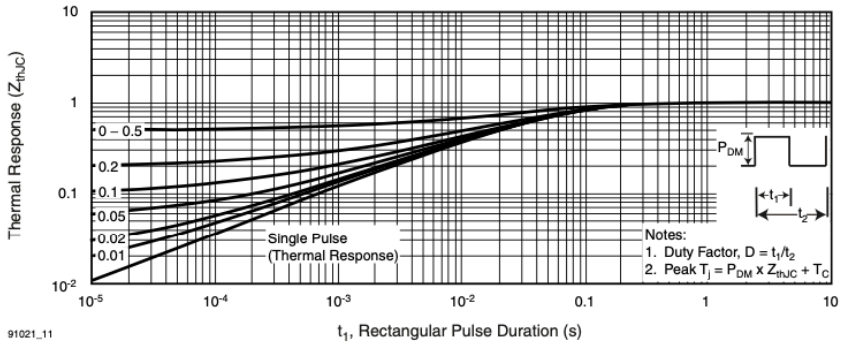


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

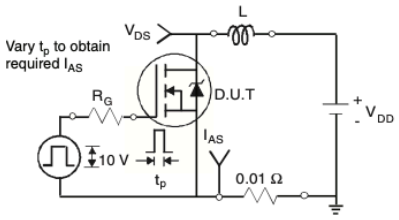


Fig. 12a - Unclamped Inductive Test Circuit

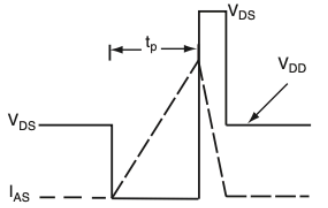


Fig. 12b - Unclamped Inductive Waveforms

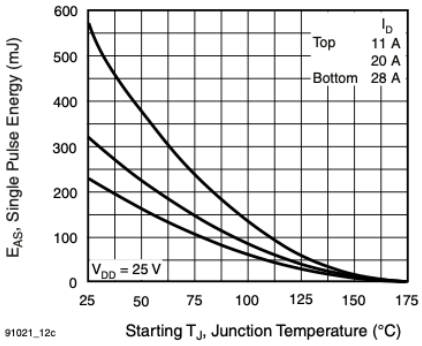


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

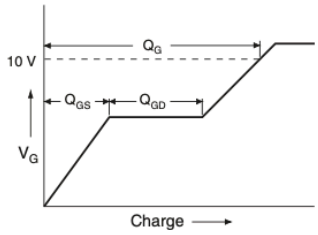


Fig. 13a - Basic Gate Charge Waveform

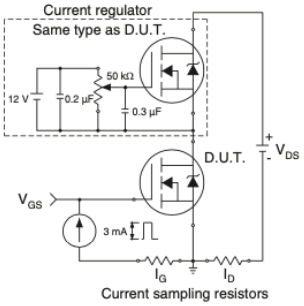


Fig. 13b - Gate Charge Test Circuit

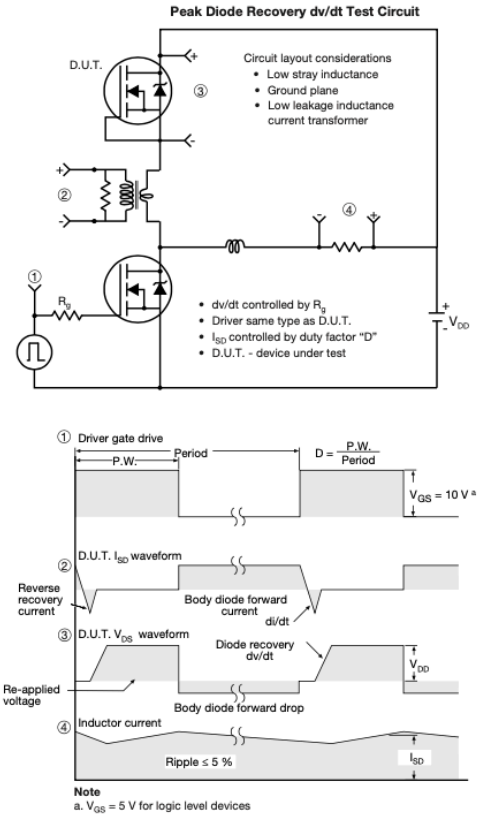


Fig. 14 - For N-Channel

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Figure C.3: Datasheet for Power MOSFET IRF540.

SB520 thru SB560

Vishay General Semiconductor

Schottky Barrier Rectifier

DO-201AD

FEATURES

- Guardring for overvoltage protection
- Extremely fast switching
- Low forward voltage drop
- High forward surge capability
- High frequency operation
- Solder dip 275 °C max. 10 s, per JESD 22-B106
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC

RoHS COMPLIANT

TYPICAL APPLICATIONS

For use in low voltage high frequency inverters, freewheeling, dc-to-dc converters, and polarity protection applications.

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	5.0 A
V_{RRM}	20 V to 60 V
I_{FSM}	220 A
V_F	0.48 V, 0.65 V
T_J max.	150 °C

MECHANICAL DATA

Case: DO-201AD
Molding compound meets UL 94 V-0 flammability rating
Base P/N-E3 - RoHS compliant, commercial grade

Terminals: Matte tin plated leads, solderable per J-STD-002 and JESD 22-B102
E3 suffix meets JESD 201 class 1A whisker test

Polarity: Color band denotes the cathode end

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAMETER	SYMBOL	SB520	SB530	SB540	SB550	SB560	UNIT
Maximum repetitive peak reverse voltage	V_{RRM}	20	30	40	50	60	V
Maximum RMS voltage	V_{RMS}	14	21	28	35	42	V
Maximum DC blocking voltage	V_{DC}	20	30	40	50	60	V
Maximum average forward rectified current at 0.375" (9.5 mm) lead length (fig. 1)	$I_{F(AV)}$	5.0					A
Peak forward surge current, 8.3 ms single half sine-wave superimposed on rated load	I_{FSM}	220					A
Operating junction temperature range	T_J	- 65 to + 150					°C
Storage temperature range	T_{STG}	- 65 to + 150					°C

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

PARAMETER	TEST CONDITIONS		SYMBOL	SB520	SB530	SB540	SB550	SB560	UNIT
Maximum instantaneous forward voltage	5.0 A		V_F (1)	0.48			0.65		V
Maximum instantaneous reverse current at rated DC blocking voltage		T_A = 25 °C	I_R (1)	0.5					mA
		T_A = 100 °C		50			25		

Note
(1) Pulse test: 300 µs pulse width, 1 % duty cycle

THERMAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)							
PARAMETER	SYMBOL	SB520	SB530	SB540	SB550	SB560	UNIT
Typical thermal resistance	$R_{\theta JA}$ (1)	25					°C/W
	$R_{\theta JL}$ (1)	8					

Note

(1) Thermal resistance from junction to lead vertical P.C.B. mounting, 0.375" (9.5 mm) lead length

ORDERING INFORMATION (Example)				
PREFERRED P/N	UNIT WEIGHT (g)	PREFERRED PACKAGE CODE	BASE QUANTITY	DELIVERY MODE
SB540-E3/54	1.09	54	1400	13" diameter paper tape and reel
SB540-E3/73	1.09	73	1000	Ammo pack packaging

RATINGS AND CHARACTERISTICS CURVES

(T_A = 25 °C unless otherwise noted)

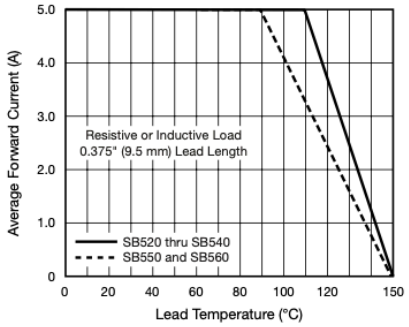

Fig. 1 - Forward Current Derating Curve

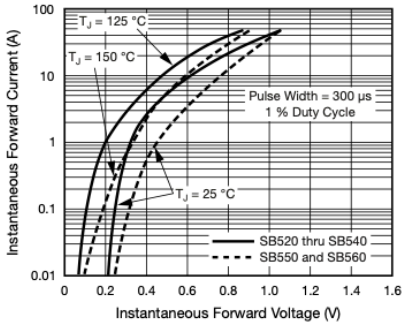

Fig. 3 - Typical Instantaneous Forward Characteristics

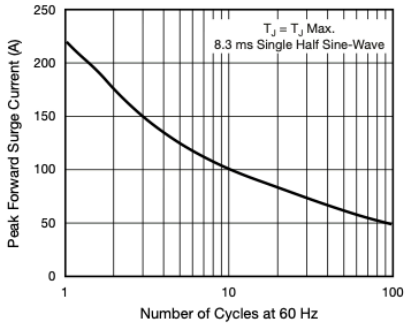

Fig. 2 - Maximum Non-Repetitive Peak Forward Surge Current

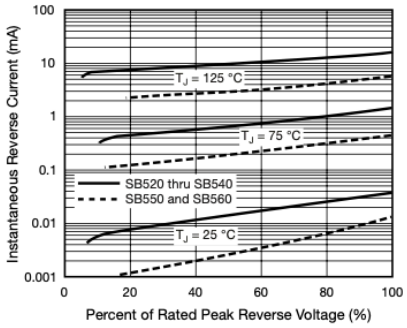

Fig. 4 - Typical Reverse Characteristics

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Figure C.4: Datasheet for Schottky Barrier Rectifier SB520 thru SB560.

Specification

Condition	100% Brand New
Item Type	Linear Stages
Model	SEMZL60-ACR
Table Size	Approx. 60 * 60mm / 2.4 * 2.4in
Centimeter Card Accuracy	0.01mm
Load Resistance	19.6N
Stroke	±6.5mm
True Straightness	3μm

Horizontal Deflection	25"
Vertical Deflection	15"
Moving Distance Adjustment	Micrometer Differential Head
Material	Aluminum Alloy (Black Anodized)
Sliding Track	Linear Guide
Rail Type	Cross Roller Type
Package List	1 * Linear Stage

Figure C.5: Datasheet for SEMZL60-ACR Z Linear Stage.

M4 10mm Screw

Product information

Material	Carbon Steel
Drive System	Phillips
Head Style	Pan
Item Dimensions LxWxH	6.5 x 3.75 x 0.5 inches
Exterior Finish	Black Oxide
Thread Size	M4
Point Style	Flat Point
Brand	ReplacementScrews
Color	Black
Head Type	Pan
Item Weight	0.32 Ounces
Thread Type	Machine
Thread Coverage	Fully Threaded
Fastener Type	Standard
Thread Style	Right Hand
Fastener Size	M4
Size	10mm
Number of Pieces	4
Product Dimensions	6.5 x 3.75 x 0.5 inches
Item Weight	0.32 ounces
ASIN	B09VV59VSR
Item model number	RSAZN2361911
Customer Reviews	★★★★½ 150 4.6 out of 5 stars
Best Sellers Rank	#9,718 in Electronics (See Top 100 in Electronics) #254 in TV Wall & Ceiling Mounts
Date First Available	March 17, 2022
Manufacturer	ReplacementScrews

Figure C.6: Datasheet for VESA Compatible M4 10mm TV/Monitor Wall Mount Screws.

M4 12mm Screw

Product information

Material	Carbon Steel
Drive System	Phillips
Head Style	Pan
Item Dimensions LxWxH	6.5 x 3.75 x 0.5 inches
Exterior Finish	Black Oxide
Thread Size	M4
Point Style	Flat Point
Brand	ReplacementScrews
Color	Black
Head Type	Pan
Item Weight	0.34 Ounces
Thread Type	Machine
Thread Coverage	Fully Threaded
Fastener Type	Standard
Thread Style	Right Hand
Fastener Size	M4
Size	12mm
Number of Pieces	4
Product Dimensions	6.5 x 3.75 x 0.5 inches
Item Weight	0.34 ounces
ASIN	B09VV9MKGQ
Item model number	RSAZN2358841
Customer Reviews	★★★★½ 150 4.6 out of 5 stars
Best Sellers Rank	#108,565 in Electronics (See Top 100 in Electronics) #1,365 in TV Wall & Ceiling Mounts
Date First Available	March 26, 2022
Manufacturer	ReplacementScrews

Figure C.7: Datasheet for VESA Compatible M4 12mm TV/Monitor Wall Mount Screws.

C Clamp

Product information

Technical Details

Manufacturer	Eunenete
Item Weight	15.8 ounces
Package Dimensions	5.28 x 2.68 x 1.85 inches
Country of Origin	China
Item model number	C02
Size	45mm-2 Pcs
Color	304 Stainless Steel
Material	Stainless Steel
Shape	45mm-2 Pcs
Power Source	hand_powered
Included Components	With wrench
Batteries Included?	No
Batteries Required?	No

Additional Information

ASIN	B0CC4WXYXY
Customer Reviews	74 4.6 out of 5 stars
Best Sellers Rank	#49,165 in Tools & Home Improvement (See Top 100 in Tools & Home Improvement) #27 in C-Clamps
Date First Available	July 18, 2023

Warranty & Support

Amazon.com Return Policy: **Amazon.com Voluntary 30-Day Return Guarantee:** You can return many items you have purchased within 30 days following delivery of the item to you. Our Voluntary 30-Day Return Guarantee does not affect your legal right of withdrawal in any way. You can find out more about the exceptions and conditions here.

Product Warranty: For warranty information about this product, please click here

Feedback

Would you like to **tell us about a lower price?**

Figure C.8: Datasheet for 304 Stainless Steel C Clamp.

18 AWG Wire

Product Description

Total 7 Colors: Black、Red、Yellow、Green、Blue、White、Brown
Length：each color 16.5 feet(5 Meters)

Nominal Voltage: 300V
Testing Voltage:3kV
Temperature Range:-20 °C to 80 °C
Conductor: Tinned Copper
OD Tolerance: ±0.1mm
Insulator: PVC

Conductor：
(1) Gauge:18AWG(0.8mm²)
(2) Copper Number/Wire Diameter:1/1.02mm
(3) Diameter: ∮1.02mm

Insulator:
(1) Jacket Thick:0.38mm
(2) Over Diameter:1.8mm

Bear Current: 8.0A

Marking Content: E300956 AWM 1007 18AWG 80°C 300V VW—1 GUANGDONG HAERKN NEW ENERGY CO.,LTD c AWM 18AWG 80°C 300V I A FT1 ROHS

Figure C.9: Datasheet for 18 awg Solid Wire kit Electrical Wire Cable.

Terminal Block

282834-2 ✔ ACTIVE

Buchanan

TE Internal #: 282834-2

PCB Terminal Blocks, Header, Wire-to-Board, 2 Position, .1 in [2.54 mm] Centerline, 1 Row, 90° Wire Entry Angle, 30 – 16 AWG Wire Size

View on TE.com >

Connectors > Terminal Blocks & Strips > PCB Terminal Blocks

Terminal Block Connector Type: **Header**

Connector System: **Wire-to-Board**

Number of Positions: **2**

Centerline (Pitch): **2.54 mm [.1 in]**

Number of Rows: **1**

Features

Product Type Features

Wire Protection	With
Terminal Block Connector Type	Header
Connector System	Wire-to-Board
Connector & Contact Terminates To	Printed Circuit Board

Configuration Features

Stacked Levels	Without
Wire Entry Location	Side
Stacking Configuration	Side Stackable
Number of Positions	2
Number of Rows	1
Wire Entry Angle	90°

Electrical Characteristics

Operating Voltage	150 VAC

Body Features

Primary Product Color	Green
Product Orientation	Vertical

Contact Features

Contact Mating Area Plating Material	Tin
Contact Base Material	Brass
Contact Current Rating (Max)	10 A

Termination Features

Termination Post & Tail Length	3.4 mm[.133 in]
Termination Method to Printed Circuit Board	Through Hole - Solder

Mechanical Attachment

Screw Plating Material	Nickel
Screw Material	Brass
Thread Size	M1.6
Connector Mounting Type	Board Mount

Housing Features

Housing Material	PA 66
Centerline (Pitch)	2.54 mm[.1 in]

Dimensions

Wire Size	.05 – 1.3 mm²

Usage Conditions

Operating Temperature Range	-40 – 110 °C[-40 – 230 °F]

Operation/Application

Circuit Application	Power & Signal

Packaging Features

Packaging Quantity	300

Product Compliance

For compliance documentation, visit the product page on TE.com>

EU RoHS Directive 2011/65/EU	Compliant with Exemptions
EU ELV Directive 2000/53/EC	Compliant with Exemptions
China RoHS 2 Directive MIIT Order No 32, 2016	Restricted Materials Above Threshold

EU REACH Regulation (EC) No. 1907/2006	Current ECHA Candidate List: JAN 2024 (240) Candidate List Declared Against: JAN 2024 (240) SVHC > Threshold: Pb (2% in Component Part) **Article Safe Usage Statements:** Do not eat, drink or smoke when using this product. Wash thoroughly after handling. Recycle if possible and dispose of the article by following all applicable governmental regulations relevant to your geographic location.
Halogen Content	Low Halogen - Br, Cl, F, I < 900 ppm per homogenous material. Also BFR/CFR/PVC Free
Solder Process Capability	Wave solder capable to 265°C

Product Compliance Disclaimer

This information is provided based on reasonable inquiry of our suppliers and represents our current actual knowledge based on the information they provided. This information is subject to change. The part numbers that TE has identified as EU RoHS compliant have a maximum concentration of 0.1% by weight in homogenous materials for lead, hexavalent chromium, mercury, PBB, PBDE, DBP, BBP, DEHP, DIBP, and 0.01% for cadmium, or qualify for an exemption to these limits as defined in the Annexes of Directive 2011/65/EU (RoHS2). Finished electrical and electronic equipment products will be CE marked as required by Directive 2011/65/EU. Components may not be CE marked. Additionally, the part numbers that TE has identified as EU ELV compliant have a maximum concentration of 0.1% by weight in homogenous materials for lead, hexavalent chromium, and mercury, and 0.01% for cadmium, or qualify for an exemption to these limits as defined in the Annexes of Directive 2000/53/EC (ELV). Regarding the REACH Regulation, the information TE provides on SVHC in articles for this part number is based on the latest European Chemicals Agency (ECHA) 'Guidance on requirements for substances in articles' posted at this URL: https://echa.europa.eu/guidance-documents/guidance-on-reach

Compatible Parts

TE Part # 1546215-2
TERMI-BLOK PCB MOUNT, 90 2P.

Customers Also Bought

TE Part #282834-5
TERMI-BLOK PCB MOUNT, 90 5P.

TE Part #282834-6
TERMI-BLOK PCB MOUNT, 90 6P.

TE Part #282834-8
TERMI-BLOK PCB MOUNT, 90 8P.

TE Part #1-282834-2
TERMI-BLOK PCB MOUNT, 90 12P.

TE Part #282834-7
TERMI-BLOK PCB MOUNT, 90 7P.

TE Part #2342838-1
AVP16M H. FLAT AIO NL 500MM/2X3

TE Part #9-1614350-1
RN 0603 11R 0.1% 10PPM 1K RL

TE Part #5-1614958-1
CPF 0805 3R24 0.1% 25ppm 1K RL

TE Part #8-2176361-5
RQ 0402 34K8 0.1% 10PPM 1K RL

Documents

Product Drawings

TERMI-BLOK PCB MOUNT, 90 2P.

English

CAD Files

3D PDF

3D

Customer View Model
ENG_CVM_CVM_282834-2_C.2d_dxf.zip

English

Customer View Model
ENG_CVM_CVM_282834-2_C.3d_igs.zip

English

Customer View Model
ENG_CVM_CVM_282834-2_C.3d_stp.zip

English

Datasheets & Catalog Pages

Eurostyle Terminal Blocks Focus Product Stock List

English

BUCHANAN TERMINAL BLOCKS CATALOG - EUROSTYLE TERMINAL BLOCKS

English

1-1773458-1_EURO_STYLE_TERMINAL_BLOCKS_QRG

English

Product Specifications

282834-2

PCB Terminal Blocks, Header, Wire-to-Board, 2 Position, .1 in [2.54 mm] Centerline, 1 Row, 90° Wire Entry Angle, 30 – 16 AWG Wire Size

Application Specification

English

Agency Approvals

UL

English

Figure C.10: Datasheet for 282834-2 Connector Terminal Block.

M4 Assorted Screws

Product Description

About us: Kadrick is a company with 25 years of fastener production experience.
Our fasteners are widely used in aerospace, high-speed railway, ships,
automobiles, computers, furniture and other fields.

Specifications:

Pitch:The distances between adjacent threads of these metric M4 screws is 0.7MM
Material: 304 Stainless steel
Screw Type: Hex socket button head cap screw
Package Included: M4 X 6 mm 20pcs
M4 X 8 mm 20pcs
M4 X 10 mm 15pcs
M4 X 12 mm 15pcs
M4 X 16 mm 15pcs
M4 X 20 mm 15pcs
M4 Nuts 100pcs
M4 Washers 100pcs
Total:300 pcs M4 304 Stainless Steel Hex Socket Head Cap Screws and Nuts Whit Hex Wrench

Features:
Commonly used 304 stainless steel screws and nuts washers, suitable for small DIY projects
such as 3D printing.

High quality:304 stainless steel with superior rust resistance ensures long lasting results,
corrosion resistance, anti-aging, good toughness.

Well packed: We use a plastic box with clear classification to place these small screws.
To prevent screw confusion, we also prepare another outer packaging to ensure that the products
are not damaged during transportation.
Note: Small Parts, Keep Away From Children Under 5 Years Old.

Figure C.11: Datasheet for 300 Pcs M4 Screw Assortment Button Head Socket Cap.

Rubber Stoppers

Product information

Product Dimensions	0.5"L x 0.5"W x 0.14"Th
Number of Items	100
Number of Pieces	100
Grip Material	Silicone,Rubber
Item Weight	1.76 ounces
Manufacturer	monochef
ASIN	B09WRFDMKY
Item model number	RS30
Customer Reviews	★★★★½ 769 4.6 out of 5 stars
Best Sellers Rank	#1,668 in Tools & Home Improvement (See Top 100 in Tools & Home Improvement) #20 in Furniture Pads
Date First Available	March 29, 2022

Figure C.12: Datasheet for 100pcs Cabinet Door Bumpers Clear Rubber Stoppers Bumpers Self Adhesive.

Portable LCR Meter

Function	Measuring Range	Resolution	Accuracy
Capacitance	200pF	0.1pF	±(2.5%+5)
	2nF	1pF	
	20nF	10pF	
	200nF	100pF	
	2uF	1nF	
	20uF	10nF	
	200uF	100nF	
	2000uF	1uF	±(5%+5)
Inductance	200uH	0.1uH	±(3%+5)
	2mH	1uH	
	20mH	10uH	±(2%+5)
	200mH	100uH	
	2H	1mH	
	20H	10mH	±(5%+5)
Resistance	200Ω	0.1Ω	±(0.8%+2)
	2KΩ	1Ω	
	20KΩ	10Ω	
	200KΩ	100Ω	
	20MΩ	10KΩ	±(1.5%+5)

Product details

Is Discontinued By Manufacturer : No

Package Dimensions : 8.55 x 6.34 x 2.4 inches; 1.3 Pounds

Batteries : 1 Lithium Ion batteries required.

Date First Available : July 17, 2017

Manufacturer : Proster Trading Limited

ASIN : B071WNNYQT

Best Sellers Rank: #45,251 in Tools & Home Improvement (See Top 100 in Tools & Home Improvement)
#93 in Multi Testers

Customer Reviews:
4.5 1,385

Figure C.13: Datasheet for Proster LCR Meter Digital LCR Multimeter Capacitance Resistance Inductance Measuring Meter with LCD Over-Range Display.

Appendix D: MATLAB Code

Five- Layer Inductance versus Airgap

```
clc;
clear;
close all;


Induct15=[3252.31, 2044.32, 1495.28, 1181.37, 978.08, 835.66, 730.27, 649.13,
584.71, 488.87, 452.24, 420.95, 393.89, 370.28, 349.47, 331.00, 314.49,
299.65, 286.24, 274.05];
GapL15 = [0, 5, 10,15,20,25,30,35,40,50,55,60,65,70,75,80,85,90,95,100];

LMeasured =
[2189.936,1367.164,1096.935,865.3364,698.2127,557.9636,474.1836,411.4455,353.3
018,312.55,280.0727];
GapLTest = 0:10:100;



Nturns=3;
Nlayers=5;
N=Nturns*Nlayers;
I=5;
mmf=N*I;
a1=.0385;
a2=.0164;
a3=.0255;
a4=.0037;
a5=.0037;
a6=.0077;
a7=.0117;
Mr=3000;
M0=4*pi*10^-7;
lgap=0:.0000001:.0001;
R1=(a2/2-a5/2)/(Mr*M0*a6*a3);
R2=(a1/2-a4/2)/(Mr*M0*a5*a3);
R3=(a2/2-a5)/(Mr*M0*a4*a3);
Rgap1=lgap./(M0.*(a4+lgap).*(a3+lgap));
Rgap2=lgap./(M0.*(a6+lgap).*(a3+lgap));
Rseries=2.*R2+2.*R3+Rgap1;
Rparrallel=2.*R1+Rgap2;
Rtotal=Rparrallel+Rseries./2;
Flux=mmf./Rtotal;

L=N^2./Rtotal;

hold on;
grid on;


plot(lgap.*10^6,L.*10^6,'red','LineWidth',2)
plot(GapL15,Induct15,'blue','LineWidth',2)
plot(GapLTest,LMeasured, 'green','LineWidth',2)
```

```
title('5 Layer: Inductance vs Airgap')
xlabel('Airgap Length [μm]')
ylabel('Inductance [μH]')
legend('Inductance','Simulated Inductance','Measured Inductance')
```

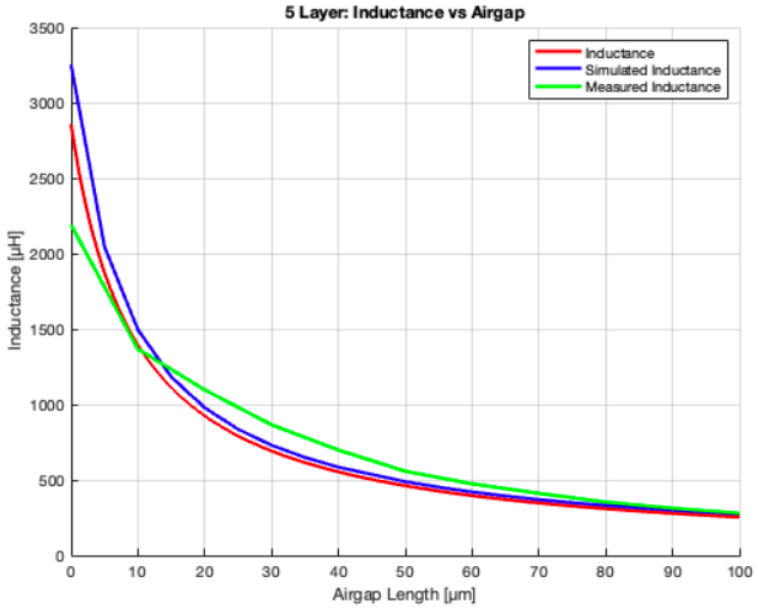

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Figure D.1: MATLAB Code for the Five-Layer Inductance versus Airgap graph.

Filter Cutoff Frequency versus Airgap

```
clc;
clear;
close all;

Induct15=[3252.31, 2044.32, 1495.28, 1181.37, 978.08, 835.66, 730.27, 649.13,
584.71, 488.87, 452.24, 420.95, 393.89, 370.28, 349.47, 331.00, 314.49,
299.65, 286.24, 274.05];
GapL15 = [0, 5, 10,15,20,25,30,35,40,50,55,60,65,70,75,80,85,90,95,100];

LMeasured =
[2189.936,1367.164,1096.935,865.3364,698.2127,557.9636,474.1836,411.4455,353.3
018,312.55,280.0727];
GapLTest = [0,10,20,30,40,50,60,70,80,90,100];

FCMeasured =
[84.1666667,116.666667,129.5,149.833333,176.5,218.833333,274.333333,326.833333
,379.166667,429.833333,472.166667];



Nturns=3;
Nlayers=5;
N=Nturns*Nlayers;
I=5;
mmf=N*I;
a1=.0385;
a2=.0164;
a3=.0255;
a4=.0037;
a5=.0037;
a6=.0077;
a7=.0117;
Mr=3000;
M0=4*pi*10^-7;
lgap=0:.0000001:.0001;
R1=(a2/2-a5/2)/(Mr*M0*a6*a3);
R2=(a1/2-a4/2)/(Mr*M0*a5*a3);
R3=(a2/2-a5)/(Mr*M0*a4*a3);
Rgap1=lgap./(M0.*(a4+lgap).*(a3+lgap));
Rgap2=lgap./(M0.*(a6+lgap).*(a3+lgap));
Rseries=2.*R2+2.*R3+Rgap1;
Rparrallel=2.*R1+Rgap2;
Rtotal=Rparrallel+Rseries./2;
Flux=mmf./Rtotal;

L=N^2./Rtotal;

hold on;
grid on;

R = 986;
```

```
Fcsim = R./(2.*pi.*Induct15);
FcLMeasured = R./(2.*pi.*LMeasured);
Fc=R./(2.*pi.*L);


plot(lgap*10^6,Fc*10^-3,'red','LineWidth',2)
plot(GapL15,Fcsim*10^3,'blue','LineWidth',2)
plot(GapLTest,FcLMeasured*10^3,'magenta','LineWidth',2)
plot(GapLTest,FCMeasured,'green','LineWidth',2)

title(['Air Gap vs Cutoff Frequency'])
ylabel('Cutoff Frequency [kHz]')
xlabel(['Air Gap [μm]'])
legend('From Calculated Inductance','From Simulated Inductance','From
Measured Inductance','Measured Fc')
```

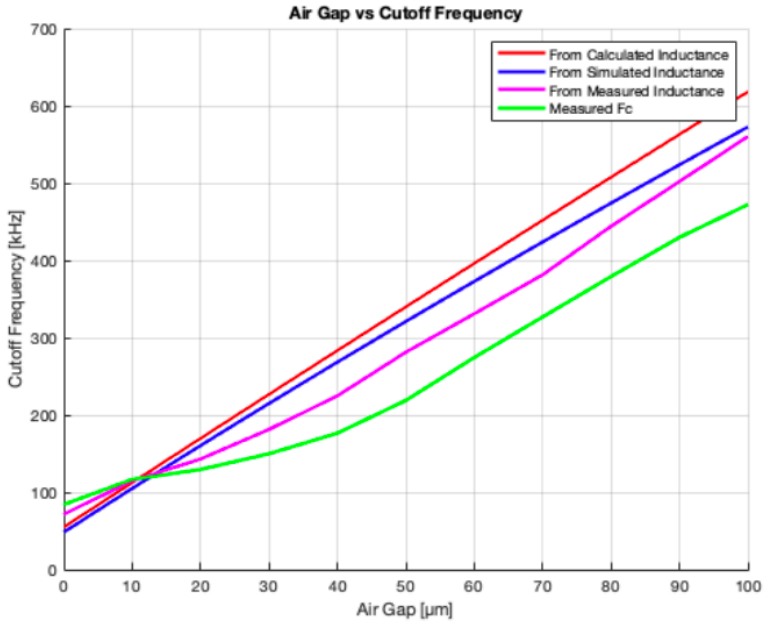

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Figure D.2: MATLAB Code for the Filter Cutoff Frequency versus Airgap graph.

EE Core One-Layer Inductance versus Airgap

```
clc;
clear;
close all;

GapL = [0, 5, 10,15,20,25,30,35,40,45,50,55,60,65,70,75,80,85,90,95,100];
GapLTest = [0,10,20,30,40,50,60,70,80,90,100];
InductanceSIM = [130.167, 81.909, 59.935, 47.361, 39.219, 33.513, 29.288,
26.038, 23.456, 21.358, 19.617, 18.155, 16.901, 15.817, 14.871, 14.037,
13.298, 12.637, 12.042, 11.505, 11.017];
LMeasured =
[83.13818,52.13455,44.27909,35.53545,29.65182,24.18636,20.06818,17.14455,14.99
091,13.35273,12.13818];

Nturns=3;
Nlayers=1;
N=Nturns*Nlayers;
I=5;
mmf=N*I;
a1=.0385;
a2=.0164;
a3=.0255;
a4=.0037;
a5=.0037;
a6=.0077;
a7=.0117;
Mr=3000;
M0=4*pi*10^-7;
lgap=0:.0000001:.0001;
R1=(a2/2-a5/2)/(Mr*M0*a6*a3);
R2=(a1/2-a4/2)/(Mr*M0*a5*a3);
R3=(a2/2-a5)/(Mr*M0*a4*a3);
Rgap1=lgap./(M0.*(a4+lgap).*(a3+lgap));
Rgap2=lgap./(M0.*(a6+lgap).*(a3+lgap));
Rseries=2.*R2+2.*R3+Rgap1;
Rparrallel=2.*R1+Rgap2;
Rtotal=Rparrallel+Rseries./2;
Flux=mmf./Rtotal;

L=N^2./Rtotal;

hold on;
grid on;

plot(lgap.*10^6,L.*10^6,'red','LineWidth',2)
plot(GapL,InductanceSIM,'blue','LineWidth',2)
plot(GapLTest,LMeasured, 'green','LineWidth',2)

title('1 Layer: Inductance vs Airgap')
xlabel('Airgap Length [μm]')
ylabel('Inductance [μH]')
legend('Inductance','Simulated Inductance','Measured Inductance')
```

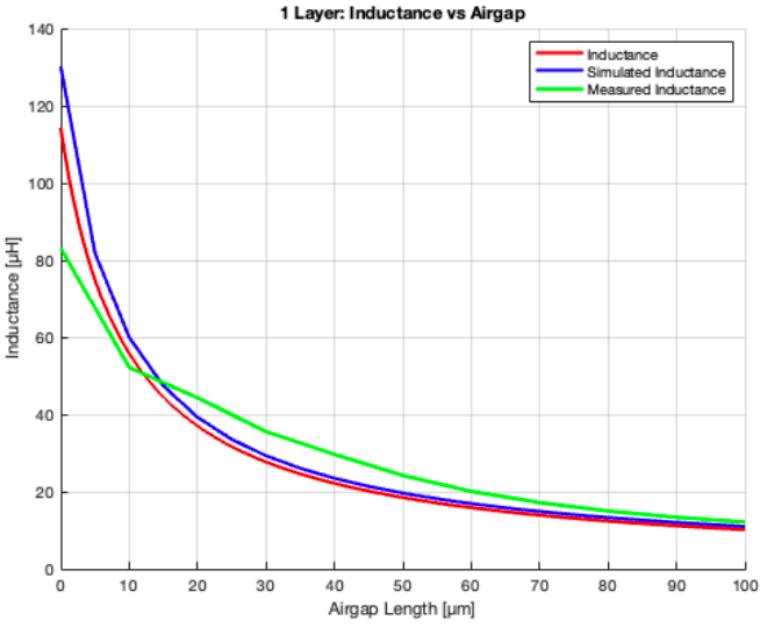

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Figure D.3: MATLAB Code for the EE Core One-Layer Inductance versus Airgap graph.

EI Core One-Layer Inductance versus Airgap

```
clc;
clear;
close all;

GapL = [0, 5, 10,15,20,25,30,35,40,45,50,55,60,65,70,75,80,85,90,95,100];
InductanceSIM = [162.444, 98.339, 71.076, 55.866, 46.092, 39.271, 34.281,
30.454, 27.442, 24.982, 22.946, 21.232, 19.772, 18.508, 17.408, 16.439,
15.572, 14.804, 14.119, 13.49, 12.923];

Nturns=3;
Nlayers=1;
N=Nturns*Nlayers;
I=5;
mmf=N*I;
b1=43.3*10^-3;
b2=4.1*10^-3;
b3=9.5*10^-3;
b4=28*10^-3;
b5=5.4*10^-3;
b6=3.8*10^-3;
b7=13.8*10^-3;
b8=8.1*10^-3;
Mr=3000;
M0=4*pi*10^-7;
lgap=0:.0000001:.0001;

R1= (b2/2)/(Mr*M0*(b8*b4));
R2= (b7+b8/2+b6/2)/(Mr*M0*(b2*b4));
R3= (b2/2)/(Mr*M0*(b6*b4));
Rgap1= (lgap)./(M0.*((b6).*(b4)));
R4= (b5+(b3-b5)/2)/(Mr*M0*(b6*b4));
R5= (b7+b8/2+b6/2)/(Mr*M0*((b3-b5)*b4));
R6= (b5+(b3-b5)/2)/(Mr*M0*(b8*b4));
Rgap2= lgap./(M0.*((b8).*(b4)));

Rseries= R6+Rgap2+R1;
Rparrallel=R2+R3+Rgap1+R4+R5;
Rtotal= Rparrallel./2+Rseries;
Flux=mmf./Rtotal;

L=N^2./Rtotal;

hold on;
grid on;

plot(lgap.*10^6,L.*10^6,'red','LineWidth',2)
plot(GapL,InductanceSIM,'blue','LineWidth',2)


title('Inductance vs Airgap')
xlabel('Airgap Length [μm]')
```

```
ylabel('Inductance [μH]')
legend('Inductance','Simulated Inductance')
```

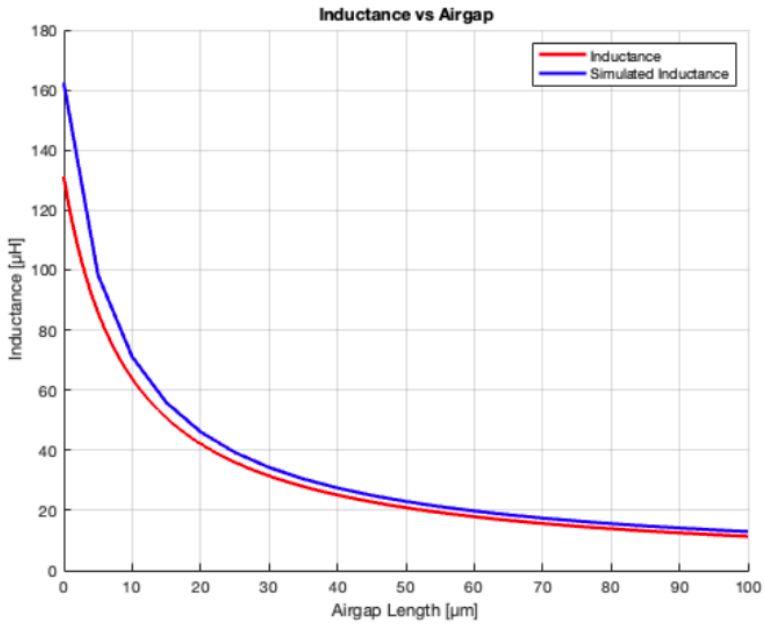

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Figure D.4: MATLAB Code for the EI Core One-Layer Inductance versus Airgap graph.