

HIGH-GAIN DIFFERENTIAL TRANSIMPEDANCE AMPLIFIER
WITH DC PHOTODIODE CURRENT REJECTION

by

Halil I. Ozbas

A Thesis

Submitted to the Faculty

of the

WORCESTER POLYTECHNIC INSTITUTE

in partial fulfillment of the requirements for the

Degree of Master of Science

in

Electrical Engineering

May 2005

APPROVED:

Prof. Brian M. King, Thesis Advisor

Prof John A. McNeill
Thesis Committee

Prof. Shela J. Aboud
Thesis Committee

Abstract

This master's thesis addresses the design of a high-gain transimpedance amplifier using a differential architecture and utilizing a DC photodiode current cancellation loop, bilinear gain, and common mode feedback. This amplifier is targeted towards optical sensing applications with the final goal of being used in an optical coherence tomography device which requires accurate measurements on the peak optical power of an amplitude modulated sinusoidal waveform that is produced by an interferometer.

Transimpedance amplifiers used in fiber optic data transmission handle random data with little or no interference from outside conditions such as ambient light. It is not desirable to use these amplifiers in optical coherence tomography applications because most of these amplifiers are optimized for high bandwidth applications and have insufficient gain. Moreover, automatic gain control (AGC) schemes that are used in most of these amplifiers make it impossible to make proportional measurements. The amplifier designed for this project senses the amplitude of a continuous sine wave biased on top of a fairly large DC current that is much larger than the amplitude of the interference by the use of DC current cancellation. In addition, it is able to drive a 50Ω load with a high transimpedance gain of $22,000\ \Omega$ that is stable through a range of DC input currents produced by total reflected light from the interferometer. It incorporates a bilinear switching AGC scheme to improve dynamic range and gain linearity. The following report describes the process of designing this amplifier starting with an overview of modern fabrication processes and current to voltage conversion and continuing with a detailed explanation of the sub-systems including the core transimpedance amplifier, common mode feedback, DC current cancellation loop, output buffer, automatic gain control utilizing the bilinear gain profile and the current reference circuit. Layout considerations and simulation results conclude this thesis.

Acknowledgements

I would like to thank the following people for helping me along the way.

Prof. Brian M. King for being my thesis advisor and guiding me through this project. His expertise on optical transmission and noise analysis was invaluable to the outcome of this thesis.

Prof. John McNeill and Prof. Shela Aboud for their help and for being in my thesis committee.

Chengxin Liu for his expert advice on the Cadence Virtuoso design suite.

Robert Brown for his continued support on WPI virtual private network and wireless networking issues.

My family and fiancée for their love and support throughout my graduate studies.

Table of Contents

ABSTRACT	I
ACKNOWLEDGEMENTS	II
TABLE OF CONTENTS	III
LIST OF FIGURES.....	V
LIST OF TABLES.....	VII
LIST OF TABLES.....	VII
1 INTRODUCTION.....	1
2 DESIGN OVERVIEW.....	4
3 MODERN SEMICONDUCTOR PROCESSES.....	8
3.1 SiGe HBT TECHNOLOGY	8
3.2 GaAs PHEMT TECHNOLOGY	9
3.3 CMOS TECHNOLOGY	11
4 CURRENT TO VOLTAGE CONVERSION	13
5 DESIGNING FOR LOW NOISE	16
5.1 TYPES OF NOISE	16
5.1.1 Thermal Noise.....	18
5.1.2 Shot-Noise.....	19
5.1.3 Flicker (1/f) Noise.....	19
5.2 METHODOLOGY	20
5.3 RESULTS	22
6 TRANSIMPEDANCE AMPLIFIER STAGE	26
7 COMMON MODE FEEDBACK.....	31
8 DC CANCELLATION	38
9 OUTPUT BUFFER.....	46
10 AUTOMATIC GAIN CONTROL.....	48
11 CURRENT REFERENCE CIRCUIT	53
11.1 SELF BIASING (BOOTSTRAPPED) REFERENCE.....	53

11.2	V_{BE} REFERENCED CURRENT SOURCE	55
11.3	V_T REFERENCED CURRENT SOURCE.....	55
11.4	BAND GAP REFERENCE	56
12	LAYOUT CONSIDERATIONS	60
12.1	TRANSIMPEDANCE STAGE	60
12.2	OUTPUT BUFFER	60
12.3	INVERTER.....	60
12.4	CURRENT REFERENCE	61
12.5	ESD PROTECTION	62
12.6	TRACES	62
13	SIMULATION RESULTS	64
13.1	SYSTEM PERFORMANCE	64
13.2	PACKAGE PARASITICS.....	64
13.3	DC CURRENT CANCELLATION LOOP AND CMFB LOOP.....	68
14	CONCLUSIONS	69
APPENDICES		72
	APPENDIX 1	73
	APPENDIX 2.....	81
LITERATURE REVIEW		87
	DC PHOTODIODE CURRENT REJECTION	87
	CMOS DESIGN TECHNIQUES.....	87
	COMMON MODE FEEDBACK CIRCUITS	88
	BILINEAR GAIN CONCEPT.....	88
BIBLIOGRAPHY		90

List of Figures

FIGURE 1 INTERFEROMETER BASED OPTICAL COHESION TOMOGRAPHY DEVICE	2
FIGURE 2 DIFFERENTIAL TRANSIMPEDANCE AMPLIFIER INCLUDING THE COMMON-MODE FEEDBACK, DC CURRENT CANCELLATION, AND THE BILINEAR AUTOMATIC GAIN CONTROL LOOPS	5
FIGURE 3 TRANSCONDUCTANCE VS. DRAIN CURRENT [33]	10
FIGURE 4 CUTOFF FREQUENCY VS. DRAIN CURRENT [33]	11
FIGURE 6 - A) MOTION OF ELECTRONS WHEN NO ELECTRIC FIELD IS APPLIED - B) MOTION OF ELECTRONS IN THE PRESENCE OF AND EXTERNALLY APPLIED ELECTRIC FIELD.....	17
FIGURE 7 INPUT REFERRED NOISE CURRENT VS. DC PHOTODIODE CURRENT (0 – 500UA) CALCULATED BY ORCAD PSPICE	24
FIGURE 8 RMS INPUT NOISE CURRENT CALCULATED BY THE CADENCE SPECTRE SIMULATOR	25
FIGURE 9 OPEN LOOP FREQUENCY RESPONSE OF THE TIA.....	28
FIGURE 10 CLOSED LOOP FREQUENCY RESPONSE OF THE UNLOADED TIA	29
FIGURE 11 CLOSED LOOP FREQUENCY RESPONSE OF THE LOADED TIA.....	30
FIGURE 12 COMMON MODE FEEDBACK CIRCUIT (SEE APPENDICES FOR THE ACTUAL CIRCUIT DIAGRAM)	31
FIGURE 13 FREQUENCY RESPONSE OF THE CMFB LOOP FOR THE SINGLE RESISTOR FEEDBACK TIA.....	33
FIGURE 14 FREQUENCY RESPONSE OF THE CMFB LOOP FOR THE DUAL RESISTOR FEEDBACK TIA	34
FIGURE 15 OPEN LOOP COMMON-MODE STEP RESPONSE OF CMFB LOOP FOR THE SINGLE RESISTOR FEEDBACK TIA (PLOTS REFLECT THE OUTPUT VOLTAGES OF THE TIA AT THE POINT WHERE THE LOOP IS BROKEN).....	35
FIGURE 16 OPEN LOOP COMMON-MODE STEP RESPONSE OF CMFB LOOP FOR THE DUAL RESISTOR FEEDBACK TIA	36
FIGURE 17 CLOSED LOOP STEP RESPONSE OF THE CMFB FOR THE SINGLE RESISTOR FEEDBACK TIA	37
FIGURE 18 FREQUENCY RESPONSE OF THE ERROR AMPLIFIER WITH LOW-PASS FILTERING (10 KHZ BANDWIDTH).39	
FIGURE 19 DC CURRENT CANCELLATION LOOP FREQUENCY RESPONSE WITH CHANGING DC CURRENT INPUTS....	40
FIGURE 20 OVERALL SYSTEM FREQUENCY RESPONSE WITH DC CANCELLATION LOOP	41
FIGURE 21 DC CANCELLATION LOOP STEP RESPONSE VS. INPUT DC PHOTODIODE CURRENT	43
FIGURE 22 FREQUENCY SPREAD Δf_1 DUE TO DC CURRENT AT 0 Ω DEGENERATION (65kHz).....	44
FIGURE 23 FREQUENCY SPREAD Δf_2 DUE TO DC CURRENT AT 200 Ω DEGENERATION (56kHz).....	44
FIGURE 24 FREQUENCY SPREAD Δf_3 DUE TO DC CURRENT AT 500 Ω DEGENERATION (45kHz).....	45
FIGURE 25 FT DOUBLER CONFIGURATION	46
FIGURE 26 SCHMITT TRIGGER.....	48
FIGURE 27 SCHMITT TRIGGER CIRCUIT IMPLEMENTATION WITH TWO GAIN STAGES AND INVERTER OUTPUT STAGE	49

FIGURE 28 GAIN OF THE TRANSIMPEDANCE AMPLIFIER VS. INPUT CURRENT AMPLITUDE WITH AND WITHOUT THE AUTOMATIC GAIN CONTROL. NOTE THAT THE AGC RESULTS IN INCREASED LINEARITY OVER A WIDE RANGE OF INPUTS (THE SWITCH POINT CORRESPONDS TO THE HIGH THRESHOLD).....	50
FIGURE 29 OUTPUT VOLTAGE SWING VS. INPUT CURRENT SWING WITH AND WITHOUT THE AUTOMATIC GAIN CONTROL. IT CAN BE SEEN THAT AT THE SWITCHING POINT, THE OUTPUT DROPS OFF SHARPLY. BECAUSE THE OUTPUT OF THE AMPLIFIER DOES NOT INCREASE CONTINUOUSLY, HYSTERESIS IS ESSENTIAL TO PREVENT OSCILLATION AROUND THE SWITCHING POINT	51
FIGURE 30 SELF-BIASING REFERENCE	54
FIGURE 31 BAND-GAP CURRENT REFERENCE; A) START-UP CIRCUIT, B) V_T REFERENCED CURRENT SOURCE PROVIDING PTAT TEMPERATURE DEPENDENCE, AND C) V_{BE} REFERENCED CURRENT SOURCE WITH A NEGATIVE TEMPERATURE COEFFICIENT. THE VOLTAGE AT NODE X COMBINES THESE TEMPERATURE DEPENDENCES [22]	57
FIGURE 32 TEMPERATURE CHARACTERISTIC OF THE BAND-GAP REFERENCE. TEMPERATURE DEPENDENCE IS MINIMIZED AROUND 25 DEGREES CELSIUS.....	58
FIGURE 33 START-UP TRANSIENT AND DC SWEEP OF THE BAND-GAP REFERENCE.....	59
FIGURE 34 CURRENT DISTRIBUTION IN A SYSTEM. IF THE TARGET DEVICE IS FAR AWAY FROM THE REFERENCE, THE DESIGNER SHOULD DO THE CURRENT MIRRORING LOCALLY TO AVOID VOLTAGE DROP OVER LONG TRACES.	62
FIGURE 35 BANDWIDTH VS. ALL BONDING PAD PARASITIC CAPACITANCES, ALL BOND WIRE PARASITIC INDUCTANCES AND INPUT BONDING PAD PARASITIC CAPACITANCE	66
FIGURE 36 EFFECT OF PARASITIC PHOTODIODE CAPACITANCE ON THE REALISTIC SYSTEM	67
FIGURE 37 SYSTEM SCHEMATIC	73
FIGURE 38 TRANSIMPEDANCE STAGE	74
FIGURE 39 COMMON MODE FEEDBACK STAGE	75
FIGURE 40 DC CANCELLATION CIRCUIT (ERROR AMPLIFIER).....	76
FIGURE 41 OUTPUT BUFFER	77
FIGURE 42 BAND-GAP CURRENT REFERENCE	78
FIGURE 43 INVERTER	79
FIGURE 44 SCHMITT TRIGGER	80
FIGURE 45 TIA CHIP.....	81
FIGURE 46 TRANSIMPEDANCE STAGE	82
FIGURE 47 OUTPUT BUFFER STAGE	82
FIGURE 48 COMMON MODE FEEDBACK STAGE	83
FIGURE 49 SCHMITT TRIGGER	84
FIGURE 50 ERROR AMPLIFIER.....	85
FIGURE 51 INVERTER	86

List of Tables

TABLE 1 CORE AMPLIFIER NOISE RESULTS	22
TABLE 2 EFFECT OF THE DC CANCELLATION MOSFET ON NOISE	23
TABLE 3 GAIN BEHAVIOR AT 100 MHZ WITH DIFFERENT DEGENERATION RESISTOR VALUES	45
TABLE 4 COMPARISON OF SIMULATION RESULTS	64
TABLE 5 COMBINED EFFECT OF PARASITIC BONDING PAD CAPACITANCES AND BOND WIRE INDUCTANCES ON SYSTEM PERFORMANCE.....	65
TABLE 6 EFFECT OF THE ISOLATED PARASITIC INPUT PAD CAPACITANCE ON THE FREQUENCY RESPONSE	66
TABLE 7 EFFECT OF PARASITIC PHOTODIODE CAPACITANCE ON THE REALISTIC SYSTEM.....	67
TABLE 8 STEP RESPONSE SETTTLING TIME VALUES FOR THE DCCC AND CMFB LOOPS	68

1 Introduction

It is prudent to give a little background about the optical coherence tomography (OCT) system to fully understand the requirements that set the goals for this design. OCT is an imaging modality where light from a low coherence source illuminates a specimen to be imaged and the backscatter from the specimen is measured. It is analogous to ultrasound where sound waves are transmitted and the reflected sound is captured by a transducer. The heart of the OCT device is a setup called an interferometer (Figure 1). The setup includes a beam splitter, a reference mirror and a low coherence light source, typically a superluminescent light emitting diode (SLED). The beam splitter reflects part of the beam coming from the source to a reference mirror that is perpendicular to the path of the incident light. The transmitted light from the beam splitter is sent to the sample to be imaged. The reflected light from the reference mirror and the sample return into the beam splitter once again and are combined. The combined beam is transmitted to a photodetector. The reference mirror is movable and can be adjusted to change the path length between itself and the beam splitter. The key operating principle of the interferometer is that if the path length of the reference mirror and the path length from the sample to the beam splitter is within the coherence length of the source, the reflected light from the sample and the reference mirror create a sinusoidal interference which rides on top of the average power created by all other reflections from the sample. The interference occurs only if the path lengths are within this small margin which correlates the position of the reference mirror to the exact depth that is being scanned within the specimen. Furthermore, the amplitude of the interference is proportional to the amount of light reflected from that particular depth. Using this information we can determine how much reflectivity exists at any depth of the sample by changing the path length of the reference mirror.

The interference signal is usually small compared to the average power created by the total reflections from the sample and any ambient light that may come into the system. This behavior presents itself at the output of the photodetector as an amplitude modulated AC current with a large DC component. This DC component is the undesired portion of the

signal and must be rejected by the receiver circuit that converts this current to a measurable voltage signal. The means of achieving this will be discussed in the following report.

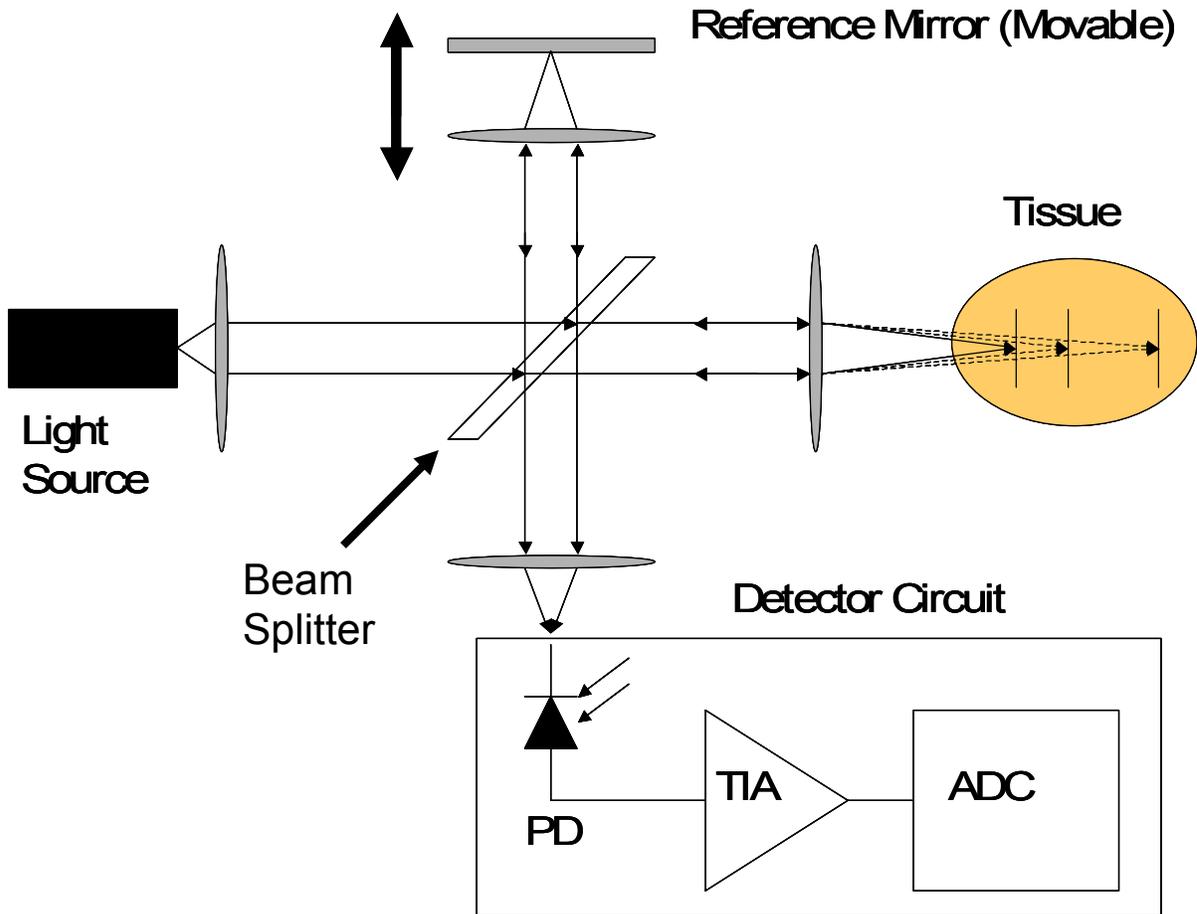


Figure 1 Interferometer based Optical Coherence Tomography device

The photodetector used in the OCT device is a semiconductor photodiode. Photodiodes convert the energy in light that is incident on the p-n junction to a linearly proportional current. When a photon hits the p-n junction, it transfers its energy to an electron in the valence band and may cause it to jump into the conduction band creating an electron-hole pair [3]. Photodiodes are operated under a reverse bias as opposed to regular diodes to achieve a large depletion region where the generation of electron-hole pairs can take place. To further facilitate the creation of a large depletion region, photodiodes are fabricated with an intrinsic region between the p and n doped regions forming what is referred to as a pin diode. The efficiency of a photodiode is referred to as the responsivity in

units of amperes per watt. This tells the user how much current is produced in proportion to the incident power. Responsivity of a pin diode can fall between 0.5 to 1 Amps/Watt depending on the area of the active region (the region where the photons are absorbed). There exists a tradeoff between responsivity and the parasitic capacitance a photodiode has. This capacitance which will be mentioned later in the report is an important factor in the bandwidth of the receiver circuit connected to the photodiode.

The focus of this thesis is the design of the portion of the receiver, which converts the current from a photodiode that receives the interference signal, to a proportional voltage so the processing circuitry can use this voltage to determine the amount of reflection from a sample under test. This information is ultimately used to produce a high resolution image of the sample.

2 Design Overview

This chapter is intended to familiarize the reader with the design and summarizes the important features of this thesis before they are discussed in greater detail in the following chapters. One of the key features of this project is that a differential architecture is used throughout the design in order to reject common mode noise such as the noise coupled from the power supply and ground which is important for maximizing the sensitivity of the amplifier in the presence of supply noise. Even though differential stages have $\sqrt{2}$ times the input referred noise compared to the single-ended structures the benefits outweigh the disadvantages [3].

The use of active loading is important in the design of high gain amplifiers especially in CMOS processes. The core amplifier (transimpedance amplifier) utilizes active loading which significantly reduces the required die area because the low transconductance of MOSFETs demand large load resistors in order to achieve decent gain and polysilicon resistors occupy a large amount of silicon area. Another disadvantage of using resistive loads is the inflexibility in adjusting the bias levels while obtaining the desired gain. Large resistors require very small currents in order to keep the output common mode level at a suitable voltage (at mid-swing) which decreases the transconductance of the input devices. Active loads can provide higher gain while using up less space and giving the designer the flexibility to determine the bias current of the devices. However, polysilicon resistors were utilized in certain places in the design where accuracy was essential such as the resistors used in the band-gap current reference and the feedback resistor of the transimpedance stage because the poly resistors are less susceptible to variations in the process parameters. Also, the use of poly resistors in the buffer stage was necessary to obtain low output impedance.

During the course of this project, various semiconductor processes were considered as possible candidates for implementation. These processes include CMOS, BiCMOS, SiGe HBT and GaAs HEMT. Although latter processes have advantages over silicon CMOS which is explained in the next chapter, CMOS processes are cheaper and more mature. CMOS was chosen for this application given that the frequency requirement of the project was relatively low and the Spice models were more readily available. The Taiwan

Semiconductor Manufacturing Company (TSMC) 0.18 μm process was ultimately used for this design based on a survey of previous projects done at WPI. This process supports 1.8V and 3.3V power supply voltages with the latter using a thicker gate oxide to handle the higher voltage. 1.8V was not sufficient for this application since both high gain and a fairly large signal swing was desired therefore the design was realized to utilize a 3.3 V power supply. The tradeoff for the thicker oxide devices was that the minimum device length could only be .35 μm for the NMOS and .30 μm PMOS devices (the minimum length for the 1.8V devices are .22 μm and .18 μm respectively). This restriction increased the overall size of the devices by restricting the minimum gate length and as a result increased the parasitic capacitances.

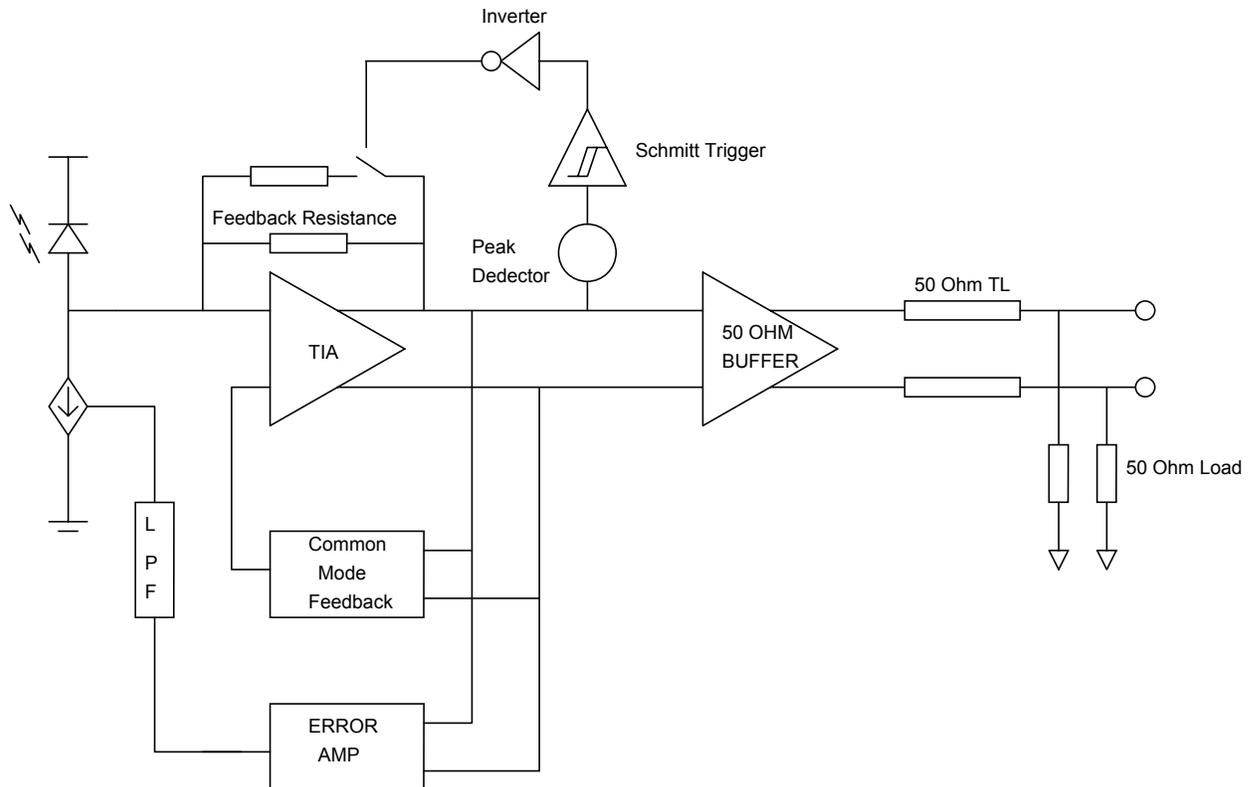


Figure 2 Differential transimpedance amplifier including the common-mode feedback, DC current cancellation, and the bilinear automatic gain control loops

One of the biggest design challenges in this project was the rejection of DC current that originates from the total reflected power returning from the measured sample. If this DC current is allowed to enter the transimpedance amplifier (TIA) it severely degrades the swing

and the gain of the amplifier because the increasing DC current at the input manifests itself as diverging DC levels of the differential outputs. A DC photodiode current cancellation technique similar to the method used in [7,8] is implemented in this amplifier where the differential outputs are sensed by an error amplifier (Figure 2). The output of the error amplifier is averaged by a low-pass filter which produces a control voltage that is proportional to the difference between the DC levels of the transimpedance amplifier's outputs and this voltage controls an NMOS device which is connected to the anode of the photodiode by modulating its gate voltage. As the DC level increases, the diverging DC levels causes the output of the error amplifier to rise, turning the MOSFET on and drawing the DC current away from the TIA. This feedback system holds the DC level of the outputs at the same voltage (which is set by a common mode feedback loop) which maximizes the swing and gain of the TIA. The "common mode feedback loop" is fully independent of the DC cancellation loop and keeps the common mode level of the transimpedance amplifier outputs at 1.2 volts.

A "bilinear" gain profile is implemented in this design so that the gain switches to half its original value at a predetermined input signal magnitude, increasing the dynamic range of the amplifier. This compressive gain profile is used instead of a logarithmic profile because the point at which the gain changes is well defined unlike the smooth gain curve of a log amplifier, making the post processing of the signal easier. Peak voltage at the output of the TIA is sensed by a peak detector and the output of the peak detector goes into Schmitt trigger with externally adjusted thresholds. The Schmitt trigger then drives the automatic gain control (AGC) through an inverter output stage.

The transimpedance amplifier utilizes a single resistor feedback from the inverting output to the input. The use of one feedback path instead of two increases the bandwidth of the TIA considerably by achieving the same gain as a dual feedback system which requires resistor values twice as large. Also, automatic gain control becomes less complex with a single feedback resistor since only one feedback loop needs to be managed.

Furthermore, the TIA has an output buffer which can be AC or DC coupled to a 50Ω load depending on the application. Being able to drive low input impedance stages increases the flexibility of the design by making it compatible with both high and low input impedance

circuits. The output of this buffer is also compatible with low-voltage positive-emitter-coupled-logic (LVPECL) bias levels which is a common termination scheme in high-speed differential signaling. This property makes it easy to use readily available differential amplifiers to be cascaded to further increase the gain if needed.

3 Modern Semiconductor Processes

This section gives an explanation of three semiconductor processes used in optoelectronic applications. The properties of SiGe and GaAs technologies are discussed and an overview of silicon CMOS process is given. SiGe and GaAs are compound semiconductors which have superior characteristics compared to silicon including better speed and low noise whereas CMOS, being a more mature process has the advantage of low fabrication costs and high level of integration. Section 3.1 explains the heterojunction bipolar transistor in the SiGe process. Section 3.2 gives an explanation of the GaAs high electron mobility transistors (HEMT) and the final section 3.3 describes the CMOS process which was used in the design of this project.

3.1 SiGe HBT Technology

The practice of bandgap engineering began with the advent of compound semiconductors in the early 1980's. This led to the design of transistors with qualities such as speed and noise figure that are better than silicon transistors. These transistors (called heterojunction transistors) were engineered to contain different compound semiconductors in different regions. An example is "a bipolar transistor that has a GaAs base and collector region, but also has an AlGaAs emitter" [29]. Bandgap engineers were also able to produce graded regions within the transistor to increase performance. The high performance of the compound semiconductors such as GaAs however came at a high cost.

Silicon (Si) technology on the other hand is mature, has a low cost and is reliable but lacks the performance of compound semiconductors. SiGe combines performance with the low cost of silicon manufacturing. It is possible to form an alloy from Si and Ge because they are "chemically compatible" [29] provided that certain conditions are fulfilled. These conditions under which the SiGe lattice is thermodynamically stable are determined by the thickness of the film and the effective strain of the lattice. Typically the thickness of the film has to be under 100nm. This makes SiGe an ideal material to be used in the base region of bipolar transistors which have to be thin to reduce transit times. SiGe has a lower bandgap than silicon which increases the carrier mobility. The Ge content of a region can also be

graded to produce electric fields that can for example boost the carriers in the base region of a transistor.

“The silicon-germanium heterojunction bipolar transistor (SiGe HBT) is the first practical bandgap-engineered device to be realized in silicon” [34]. In terms of performance, the reduction in the bandgap in the base emitter junction of the HBT results in a reduction of the potential barrier. This increases the collector current density which in turn increases the current gain of the transistor. Also as explained before, the base region of the HBT can have a grading in Ge doping which results in different conduction band locations in different portions of the base. This creates a potential difference in the base region that “accelerates the injected electrons”, reduces the carrier transit time and thus improves the frequency response. A SiGe HBT has a cutoff frequency that is about 1.7 times that of a Si BJT with similar doping densities. Cutoff frequencies that are more than 100GHz can also be reached with SiGe. In fact [30] shows a SiGe HBT with an emitter area of $0.2 \times 2 \mu\text{m}$ that has a cutoff frequency of 122GHz and a current gain (β) of 1400. The grading in the base region creates a more Ge rich area towards the collector. This makes it harder to deplete the base side of the junction which reduces base width modulation. A higher early voltage is thus achieved [29], which also results in a higher output impedance. This is desirable in an amplifier design requiring high gain. SiGe HBTs have other advantages such as low noise comparable to GaAs MESFETs and easy integration with Si CMOS technology. These qualities combined with the cost-effectiveness makes SiGe HBT technology a good choice for high-speed optical-fiber communication (ie. 40 Gb/s) [30].

3.2 GaAs pHEMT TECHNOLOGY

Compared to other compound semiconductor transistors, HEMT and pHEMT are recent additions. The primary advantages of the HEMT over other technologies is its very low noise figure (0.3dB at 2GHz is achieved) and high cutoff frequency compared to FETs. The pHEMT is an even higher performance variant of the HEMT with “applications up to 220GHz” [31]. Before the invention of the HEMT the primary GaAs device was the MESFET which has a worse frequency response and noise figure. The structure of the HEMT is formed by an undoped GaAs substrate topped with a silicon doped n type AlGaAs

layer. Because the undoped GaAs layer has higher electron affinity, the free electrons on the n-type AlGaAs layer pass to the substrate and form a two-dimensional high-mobility electron gas at the junction [32]. The AlGaAs layer is made very thin so that without an externally applied voltage this 2-D electron gas (2-DEG) layer cannot form. Once a positive external voltage greater than the threshold voltage is applied to the AlGaAs layer, the 2-D electron gas layer is formed at the junction, and the electron concentration can be controlled by the magnitude of the gate voltage [32]. The relatively new pseudomorphic AlGaAs/InGaAs/GaAs HEMTs are superior to AlGaAs/GaAs devices because of the higher electron velocity and the extra InGaAs channel which is used to confine the carriers. The In mole concentration in this channel affects the cutoff frequency and the g_m (transconductance) of the device. Both the cutoff frequency and the g_m of the amplifier increase with the mole concentration of In [33]. The drain current also affects these parameters. Figure 3 and Figure 4 show this relationship. The GaAs pHEMTs are used in a variety of applications such as low noise amplifiers, RF power amplifiers and transimpedance amplifiers for optical communications.

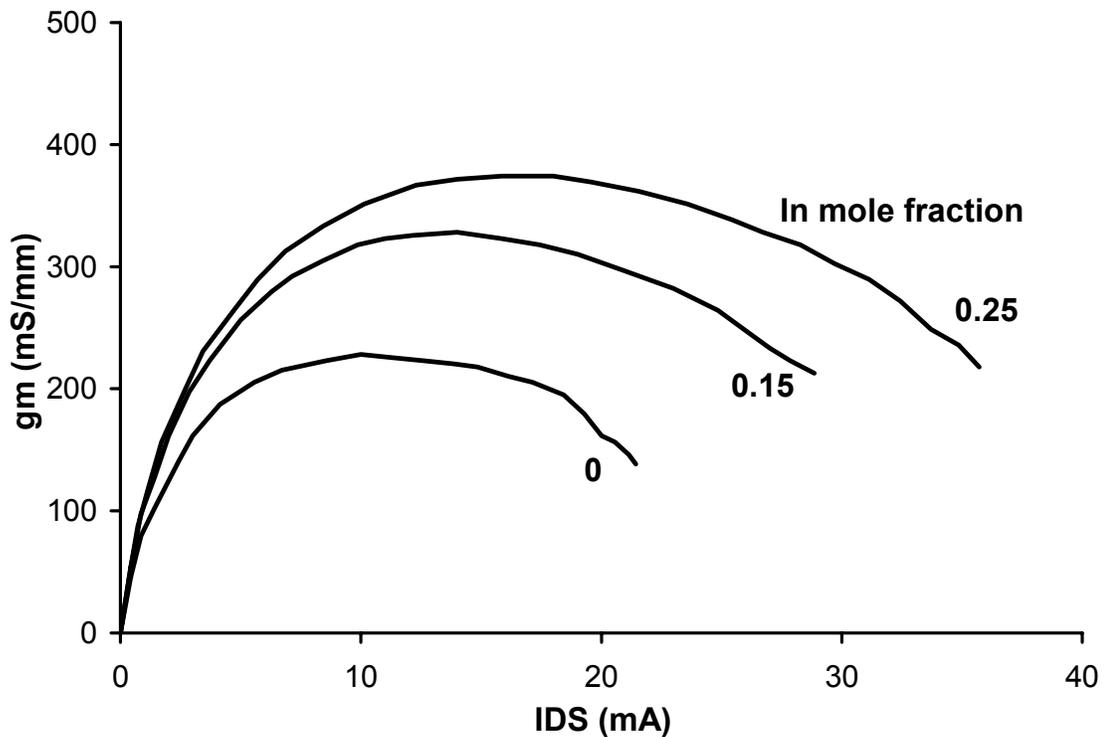


Figure 3 Transconductance Vs. drain current [33]

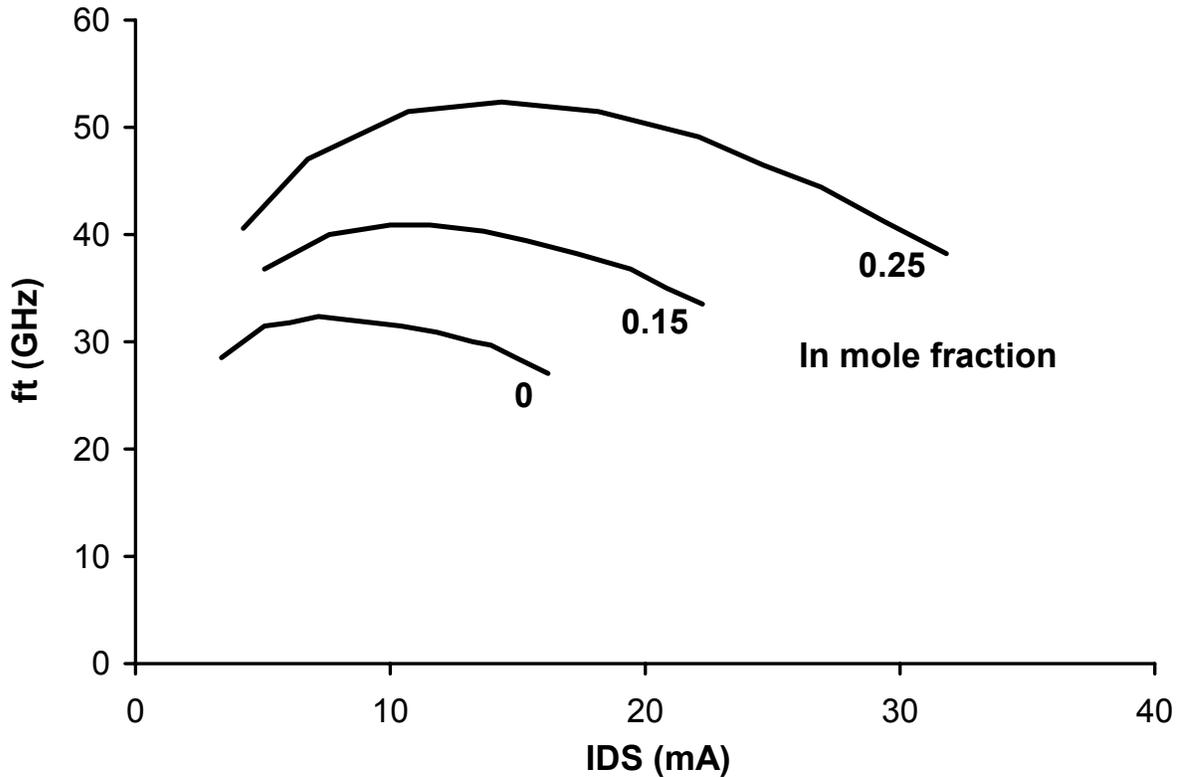


Figure 4 Cutoff Frequency Vs. drain current [33]

3.3 CMOS TECHNOLOGY

CMOS remains one of the more mature and cheaper processes in the world. CMOS processes have improved in speed due to scaling in the past 30 years and achieved gain-bandwidth products of 62 GHz allowing the use of this technology in high-speed optoelectronic circuits. This trend pushed the CMOS technology closer to the performance region of GaAs devices. Modern CMOS processes provide designers with many tools including a variety of active devices such as MOS varactors and passive components including spiral inductors, transmission lines and microstrip lines that were made feasible by the utilization of multiple metal layers which made the design of RF circuits possible.

Scaling of CMOS processes also caused the power supply voltages to be lowered which decreased the power dissipation of CMOS circuits considerably. Moreover the increased density of integration combined with the reduced costs of manufacturing have

made the CMOS process very popular in the design of large scale integrated circuits [35].

CMOS processes utilize MOSFET (Metal-Oxide-Semiconductor-Field-Effect-Transistor) transistors. Unlike bipolar transistors which rely on minority carrier transmission to operate and require constant biasing of the base, MOS devices use an isolated gate to form a channel by inversion between two doped terminals (n doping for NMOS and p doping for PMOS). Charge transfer is established between these terminals when a potential is applied between them. CMOS or complementary MOS uses both NMOS and PMOS devices, the latter obtained by “negating all the doping types” [2]. MOSFETs do not require a gate current to remain on which results in low power dissipation.

The process chosen for this project is the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm Mixed-Signal process. This process provides a power supply voltage of 1.8 V or 3.3 V with the latter achieved using a thicker oxide layer to handle the increased potential.

The reason for the CMOS process to be chosen for this design was the goal of designing a low cost, low noise amplifier in a proven technology.

4 Current to Voltage Conversion

In optical communications the optical signal that arrives at the receiver has to be converted into an electrical signal for further processing. This process is accomplished by photodiodes that produce a current that is proportional to the power of the incident optical signal. The current produced however is usually very small (most photodiodes have responsivity around 0.5 to 1 Amps/Watt at wavelengths of interest) and it has to be converted into a voltage signal that is large enough to be detected by devices such as sample and hold circuits and analog to digital converters (ADC) which do the post processing of the signal. In an optical receiver, the first stage that comes after the photodiode converts the photocurrent into a proportional voltage while also adding gain. This first stage may also need to convert the single-ended signal coming from the photodiode to a differential signal depending on the architecture of the following stages. In some TIAs used in data communication, one gain stage may not be enough and further amplification by a linear amplifier may be necessary in order to get a signal that has a swing that is detectable by the processing circuitry for very low power inputs. The components of a typical receiver are the current to voltage converter (typically a TIA), an optional linear amplifier (for data communications), an optional low-pass filter (to reduce inter-symbol interference “ISI” in data transmission) and the clock and data recovery circuit (if the receiver is to be used for data transmission; or other post decision making circuitry) [6].

According to the researched reference material, there are three main types of amplifier topologies used in optical receivers. These are high input impedance amplifiers, low input impedance amplifiers and transimpedance amplifiers [5, 6]. High input impedance and low input impedance amplifiers have a shunt resistor at the input to convert the input current to a voltage. In the “high input impedance amplifier” the sensitivity is increased due to the small input noise current, however the large input resistor along with the combined parasitic capacitance of the amplifier, the package and the photodiode results in a low bandwidth. Input referred noise current is low in this configuration due to the high input impedance since RMS noise current is defined as $\sqrt{\frac{4kT}{R}}$ [1] where T is the temperature in

kelvins, k is the Boltzmann's constant and R is the resistance. The low input impedance amplifier has the same configuration but the input impedance is very small so the bandwidth is increased at the expense of gain. Input noise current in this configuration is worse due to the reduced impedance. In both of these configurations, the dominant pole is formed by the input impedance and the capacitance, therefore a large gain bandwidth tradeoff exists. Transimpedance amplifiers (in the closed loop configuration) are more widely used because of their relatively higher bandwidth for the same gain compared to the high impedance topology. Also in a first order shunt-shunt feedback transimpedance amplifier, the dynamic range is better than the high input impedance case because of the negative feedback [14]. Disadvantages of the transimpedance amplifier are possible stability issues with the feedback

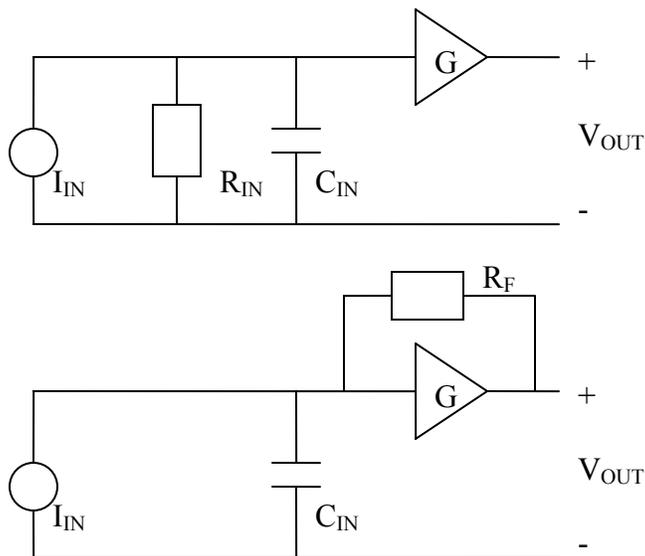


Figure 5 Current to voltage conversion amplifiers

loop [16] and higher input referred noise as compared to the high impedance amplifier. However the transimpedance amplifier requires no additional equalizing circuit at its output [6]. The higher bandwidth is obtained because of the Miller effect. The Miller effect reduces the input impedance and the output impedance of the amplifier by a factor approximately equal to the loop gain which is the product of the open loop gain of the transimpedance amplifier and the feedback resistor [1]. The calculation of the transfer function is explained both in [1] and [5]. The dominant pole of a transimpedance amplifier is created by the input impedance of the feedback amplifier and the total capacitance at the input therefore the reduction in input impedance by decreasing the feedback resistance (increases noise current) and possible measures to decrease the input capacitance (a better strategy) or increase the open loop gain of the core amplifier are alternatives in increasing the bandwidth [15]. Photodiodes with smaller active areas present less capacitance to the input

loop [16] and higher input referred noise as compared to the high impedance amplifier. However the transimpedance amplifier requires no additional equalizing circuit at its output [6]. The higher bandwidth is obtained because of the Miller effect. The Miller effect reduces the input impedance and the output impedance of the amplifier by a factor approximately equal to the loop gain which is the product of the open loop gain of

of the TIA, however decreasing the active area also decreases the responsivity of the photodiode which decreases the overall gain of the receiver. A better approach is to use packages which have smaller parasitic capacitances. Also keeping the trace lengths from the photodiode anode to the input of the TIA at a minimum length is essential. Figure 5 shows the high input impedance and low input impedance amplifier topologies on the top, and the transimpedance amplifier topology on the bottom [6]. C_{IN} is the input capacitance which includes the total parasitic capacitance of the amplifier, the package and the photodiode.

Noise analysis for a transimpedance amplifier is described in [1] and [2]. Constructing a noise model for the amplifier is difficult since all transistors contribute to shot noise and the resistive elements in the amplifier and transistors each contribute to the thermal noise. For the particular amplifier designed for this project, $1/f$ noise was not taken into account since the operating frequency is relatively high. After the noise model is generated, the equivalent noise at the input is derived as described in [1] in the following sections. The equivalent noise model consists of a noise voltage and noise current generator at the input of the amplifier which includes the effects of all the devices in the system. The effects of shunt-shunt feedback on input noise in a transimpedance amplifier are shown in [1] and will be discussed in the next section.

5 Designing For Low Noise

Noise is an important factor that limits the performance of electronic circuits. This chapter gives an overview of the various sources of noise as well as the effects of different types of noise in circuits and describes the techniques used in the design of this amplifier to minimize these effects. In section 5.3, noise analysis results obtained from simulations are presented.

5.1 *Types of Noise*

Noise in circuits is created by various physical phenomena and is due to the random motion of charge-carrying particles (electrons and holes). Noise exists because the flow of charge (current) through a conducting or semiconducting material is not continuous. Since electrons are particles, the flow of charge through a cross sectional area in the material is discrete [1]. Electrons are not stationary and move randomly through the lattice of the material and even in the presence of an electric field, the motion of electrons is not a straight line. At any moment in time the amount of charge that flows through a cross section in the material can be inhomogeneous. Figure 6 illustrates the movement of electrons in a piece of conducting (or semiconducting) material.

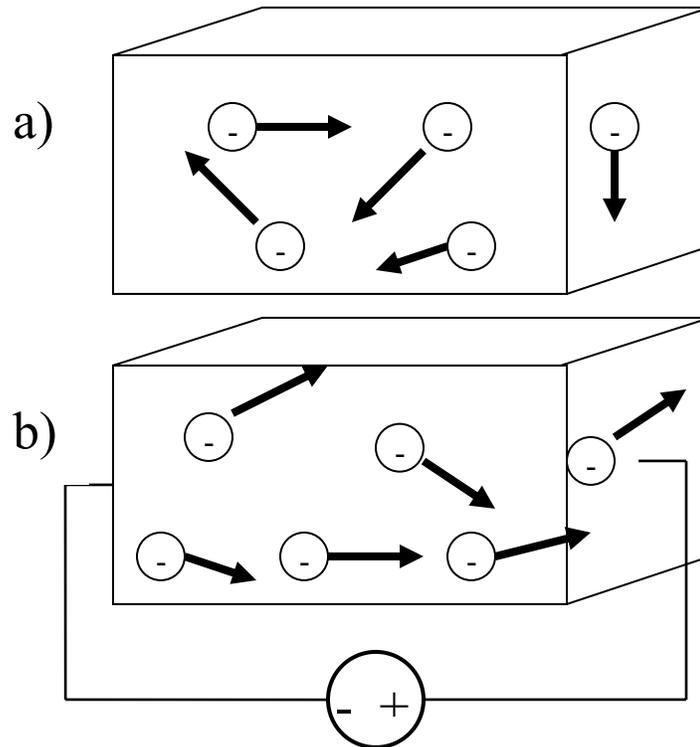


Figure 6 - a) Motion of electrons when no electric field is applied - b) Motion of electrons in the presence of and externally applied electric field

Noise in circuits is classified in relation to the mechanism of how it is created. The types of noise include thermal noise, shot noise and flicker noise. Thermal noise is the random motion of electrons due to thermal energy. Shot noise is created at junctions between two materials where an electric field exists and it is due to the discrete nature of the transportation of charge. Flicker noise is due to imperfections in the material itself where the charge carriers may get trapped or slowed down. These noise types are explained in more detail in the following sections.

Noise can not be represented by a fixed amplitude since the amplitude varies randomly over time. The probability density function (pdf) of a random process describes the probability of the occurrence of each amplitude in a random process. Most noise sources have a Gaussian probability distribution where the amplitude is within $\pm \sigma$ of the mean value 68% of the time. σ is defined as the standard deviation and σ^2 is the variance of a random process [1].

Sources of noise can also be represented by their average power in the frequency domain instead of their amplitude distribution. The average noise power is:

$$P_{AV} = E[x^2(t)] \quad (1)$$

P_{AV} is the expected value of $x^2(t)$ where $x(t)$ is the noise signal. In noise analysis the noise power is usually represented by its power spectral density (PSD) which is equal to the average power of a noise source per 1 Hz bandwidth calculated around a center frequency, for all possible frequencies of interest. In circuit analysis where the noise at one particular frequency is desired, the center frequency is usually taken as the frequency at which the device operates such as the fundamental frequency of a data signal. The PSD can be calculated over the range of the devices pass-band to determine the signal-to-noise ratio. PSD is represented by the unit V^2/Hz , however, it is sometimes more intuitive to show noise as currents and voltages during calculations. In those cases, the square root of the PSD is used with the units of $V/(\text{Hz})^{1/2}$ or $A/(\text{Hz})^{1/2}$ which are the root-mean-square (RMS) noise voltage and the noise current respectively. The root-mean-square noise current (voltage) is also equal to the standard deviation of the noise amplitude (σ).

5.1.1 Thermal Noise

Thermal noise is created when carriers inside a conductor are “thermally agitated” [13] and the random motion creates a random current and potential across the conductor. It is also referred to as Johnson noise or Nyquist noise. The amplitude of the noise voltage across the conductor has a Gaussian distribution and the PSD of thermal noise is constant over all frequencies. We can define the mean-square noise voltage and current of a resistor as:

$$\overline{V_n^2} = 4kTR\Delta f \quad \overline{I_n^2} = \frac{4kT}{R}\Delta f \quad (2)$$

Or in RMS form as:

$$v_n = \sqrt{4kTR\Delta f} \quad i_n = \sqrt{\frac{4kT}{R}\Delta f} \quad (3)$$

where k is the Boltzmann’s constant, T is the temperature in Kelvins, R is the resistance and Δf is a small bandwidth the noise is calculated over. As mentioned before this bandwidth is chosen as 1 Hz in circuit analysis therefore the Δf term is not used in the analysis from this

point on. It is clear that the noise power is proportional to temperature in both equations which is consistent with the idea that increasing temperature increases the energy of the carriers and thus increases the random motion. In MOSFETs thermal noise is created in the channel due to random thermal motion of carriers in the channel. This noise is also capacitively coupled to the gate which is called gate noise. The drain RMS noise current and the gate RMS noise voltage are represented as:

$$v_n = \sqrt{4kT\delta r_g} \quad i_n = \sqrt{4kT\gamma g_{d0}} \quad (4)$$

where γ , δ are process dependent constants, r_g is the gate resistance (resistance of the polysilicon gate) and g_{d0} is the conductance of the channel. γ can be taken as 2/3 when the device is at saturation (active) and δ is taken to be twice γ [13].

5.1.2 Shot-Noise

Shot noise results from the individual charges passing a potential barrier [13]. In optical systems (where it is also called quantum noise) shot noise can also be created in the photodiode because of the “random arrival rates of photons” at the detector [23, 24]. Shot noise of a PIN diode has the power spectral density:

$$\overline{i_n^2} = 2qI_{PD} \quad (5)$$

where I_{PD} is the mean photodiode current. Shot noise increases with increasing diode current.

Because of its nature, shot noise can form in P-N junctions where electric fields form potential differences across depletion regions. In MOS devices a potential exists between the gate and the channel of the device. The main source of shot noise in a MOSFET is the leakage current from the gate to the channel and this current is usually very small. For this reason we can usually neglect shot noise during noise analysis.

5.1.3 Flicker (1/f) Noise

Flicker noise in MOSFETs occur because of imperfections in the channel [13]. The charge carriers get trapped by these imperfections making the current fluctuate. The spectral density of flicker noise decreases with increasing frequency at a rate of 1/f and is greatest at DC thus higher DC bias levels lead to a higher flicker noise component. Also [13] states that

flicker noise is less in larger devices because the larger gate capacitance helps in absorbing the “fluctuations in the channel charge.” The RMS noise current of the flicker noise can be described as:

$$i_n = \sqrt{\frac{K \cdot g_m^2}{f \cdot C_{OX}^2 \cdot A}} \quad (6)$$

where K is a constant, A is the area of the gate, C_{OX} is the gate capacitance, g_m is the transconductance and f is the frequency at which the charge carriers get trapped and released [2]. As can be seen from the equation a thinner oxide layer at the gate leads to less 1/f noise as does a larger gate area.

5.2 Methodology

In a differential amplifier with source follower outputs, a significant source of noise are the source followers since the noise at the output is referred directly to the input with a gain of 1 or more (forward gain of a CMOS source follower is usually much less than one). If the gain of the differential stage is low, the input referred noise from the source follower can be significant. This is why care must be taken to design this stage for low noise. In this analysis, shot noise and 1/f noise will not be taken into account. It is shown in [2] that the input referred RMS thermal noise voltage of the source follower is:

$$v_{n,in} = \sqrt{4kT \frac{2}{3} \left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2} \right)} \quad (7)$$

If $(W/L)_1 \gg (W/L)_2$ then this equation reduces to:

$$v_{n,in} = \sqrt{\frac{8kT}{3g_{m1}}} \quad (8)$$

The input referred RMS noise current of the source follower can be calculated by noting that:

$$i_{n,in} = \omega C_{gs} \overline{v_{n,in}} \quad (9)$$

The gate source capacitance of the MOSFET is [2]:

$$C_{GS} = \frac{2}{3} WL C_{OX} + WC_{OV} \quad (10)$$

where C_{OX} and C_{OV} are process related capacitances, and g_{m1} and g_{m2} are related to M1 and M2 respectively where M1 is the input transistor and M2 is the current source. From this

equation it can be seen that g_{m1} must be large while g_{m2} must be minimized. This can be done by making $(W/L)_1$ large and $(W/L)_2$ small. Since the square term dominates the equation the drain current can be increased to decrease the noise. This however poses some challenges since the voltage drop across M1 increases with increasing current. So if a decent swing at the output is desired, the drain current cannot be made arbitrarily large.

The input referred RMS voltage noise of the differential amplifier with current source loads is given by the equation [2]:

$$v_{n,in} = \sqrt{8kT \left(\frac{2}{3g_{m1}} + \frac{2g_{m3}}{3g_{m1}^2} \right) + \frac{2K_N}{C_{ox}(WL)_1 f} + \frac{2K_P}{C_{ox}(WL)_3 f} \frac{g_{m3}^2}{g_{m1}^2}} \quad (11)$$

The first term in this equation corresponds to the thermal noise and the second and third terms are flicker (1/f) noise components. The factor K_N and K_P are called the flicker noise coefficients and are on the order of 10^{-25} in CMOS processes. If the flicker noise is ignored it can be observed that the thermal noise component is twice the input referred noise voltage of the former. This is because there are two inputs with two paths to the output and with one input connected to AC ground the total noise voltage is referenced to one input in this design. The input noise current however is not doubled. This equation suggests that in order to reduce noise, transconductance of the current mirror load devices have to be minimized and the transconductance of the input devices must be large. This however brings another tradeoff. The input devices cannot be made arbitrarily wide because this increases the total capacitance at the input which lowers the frequency of the dominant pole degrading speed. It can also be seen that designing for low noise puts a constraint on the bias current at the source follower devices which is the dominant parameter that determines the voltage level shift through those devices which in turn affect the amount of signal swing available. Also the current mirror devices have to be narrower in size which increases the voltage drop across the devices, reducing the upper limit for the signal swing.

When the two stages are brought together, the noise at the input of the source followers have to be referred to the input of the differential pair. The noise voltage at the source follower is reduced by the voltage gain of the differential pair. The noise current of the source follower can be treated as the drain current of the differential pair. The following relation is used to calculate the current gain of the differential pair.

$$\frac{i_{n,out}}{i_{n,in}} = \frac{g_{m1}}{\omega C_{gs}} \quad (12)$$

The noise current and voltage that is referred back from the source follower can then be added to the input noise of the differential pair in RMS fashion.

5.3 Results

The current design which incorporates a single-ended to differential input stage followed by a source follower has the following parameters for input referred noise. The total noise includes the noise current contributes by the feedback resistor which is the dominant source of noise in a feedback TIA with CMOS inputs. The inherent low noise current characteristic of the CMOS process is seen in the results. As explained in [1] shunt-shunt feedback does not affect the noise voltage of the core amplifier.

	SOURCE FOLLOWER	DIFF. PAIR	TOTAL
RMS Noise Current	Neglected	2.965 fA / Hz ^{1/2}	1.018 pA / Hz ^{1/2}
RMS Noise Voltage	3.773 nV / Hz ^{1/2}	2.066 nV / Hz ^{1/2}	2.072 nV / Hz ^{1/2}

Table 1 Core amplifier noise results

High gain and g_m of the differential input stage is important to shield the input from the noise of the subsequent stages. It is also verified in [2] that a shunt-shunt feedback does not change the noise voltage of the amplifier however the noise current of the feedback resistor directly adds to the input noise current of the amplifier.

Further analysis including the DC cancellation network shows that the MOSFET at the anode of the photodiode is a large contributor of noise. In fact the drain noise current increases with the amount of current that is sunk by the MOSFET. The equations below [2] show this relationship.

$$i_n = \sqrt{4kT\gamma g_m} \quad (13)$$

where γ is 2/3 for a MOSFET in saturation.

$$v_n = i_n r_O \quad (14)$$

where v_n is the RMS noise voltage at the drain and r_o in this case is the impedance formed by the parallel combination of the output impedance of the MOSFET and the input impedance of the transimpedance amplifier. Because r_o is a large impedance, the RMS noise voltage at the output of the MOSFET is significant, and it dominates the total input RMS noise voltage of the system. It can also be seen that increasing the gain of the TIA increases the total impedance seen by the MOSFET and the noise voltage increases proportionally so in this application with the DC canceling MOSFET, if further gain is needed, it should be provided by a second gain stage after the TIA.

The total input referred noise values at the input of the amplifier, including the DC cancellation MOSFET is shown below. The results are based on a 500uA drain current at the current sinking MOS device. Since the noise increases with the g_m of the device and g_m is proportional to drain current, the resulting value reflects the worst case scenario.

	DC CANC. MOS.	TIA	TOTAL
RMS Noise Current	2.803 pA / Hz ^{1/2}	1.018 pA / Hz ^{1/2}	2.982 pA / Hz ^{1/2}
RMS Noise Voltage	39.86 nV / Hz ^{1/2}	2.072 nV / Hz ^{1/2}	39.914 nV / Hz ^{1/2}

Table 2 Effect of the DC cancellation MOSFET on noise

Other sources of noise in the system are the error amplifier, the low-pass filter, the common mode feedback circuit and the buffer. The buffer couples noise to the input through two paths. One is through the TIA where the high transimpedance gain of the amplifier makes the contribution of the buffer insignificant. The other path is through the error amplifier, low-pass filter and the DC cancellation MOSFET. The total gain through this path can also be considered a transimpedance gain since any disturbance at the input of the error amplifier changes the total current at the input. Compared to the reverse gain of the TIA, this gain is much larger so the input referred noise current through this path is not insignificant. However because of the low-pass filter with a bandwidth much lower than the system, the noise coupled through the DC cancellation loop only exists in lower frequencies and does not affect the pass-band region. Figure 7 shows the RMS input referred noise current plot for different values of DC photodiode current. It can be observed from the plots that the total

noise current when the DC cancellation circuit is active increases with increasing DC photodiode current and then decreases when the DC current passes 350uA. This is because the gain of the error amplifier is not linear over the whole range due to the fact that the amplifier operates in open loop configuration and thus the noise referred from the other parts of the circuit through the error amplifier changes.

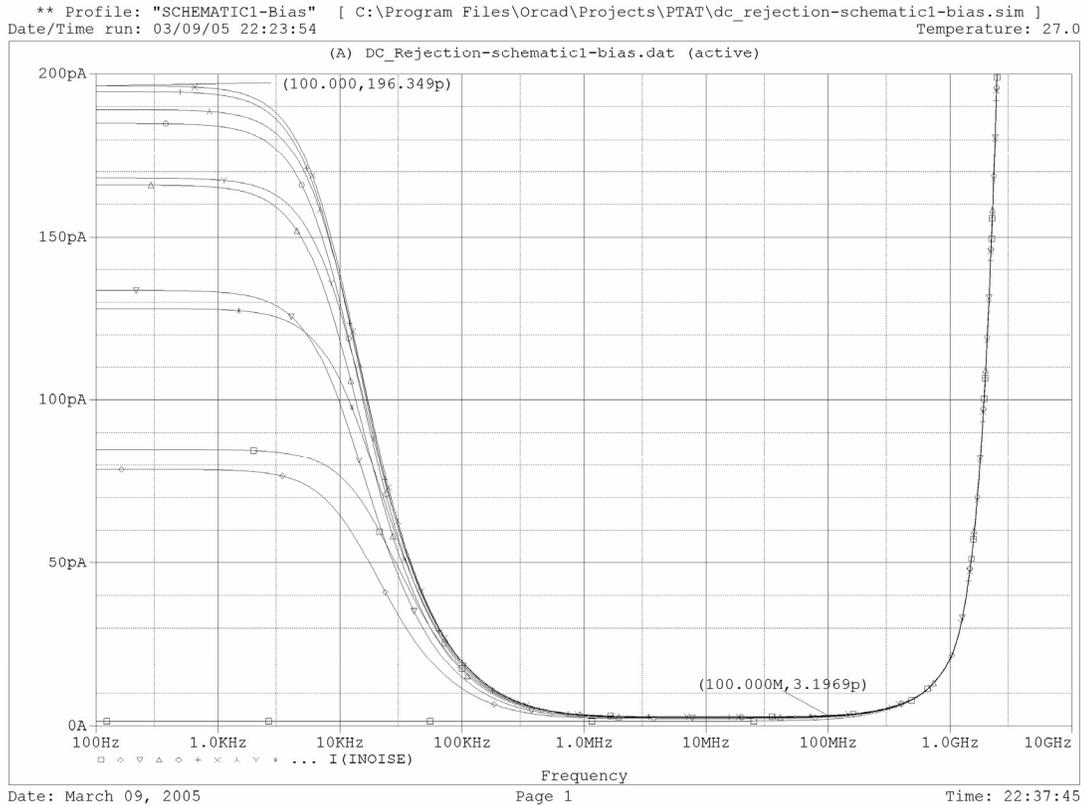


Figure 7 Input referred noise current vs. DC photodiode current (0 – 500uA) calculated by Orcad Pspice

Figure 7 shows the input referred noise current of the amplifier in the presence of DC current that is being sunk by the DC cancellation circuit. The X axis shows the center frequency of noise while the Y axis shows the input referred RMS noise current in pA/Hz^{1/2}. Each of the plots corresponds to the input noise current calculated for different DC current values from 0 to 500 uA. The changing gain of the DC cancellation loop changes the amount of noise referred to the input at frequencies below the pass-band of the system. It can be seen

that the Pspice calculated RMS input noise current ($3.197 \text{ pA/Hz}^{1/2}$) in the pass-band is very close to the result of $2.982 \text{ pA/Hz}^{1/2}$ obtained by hand calculations.

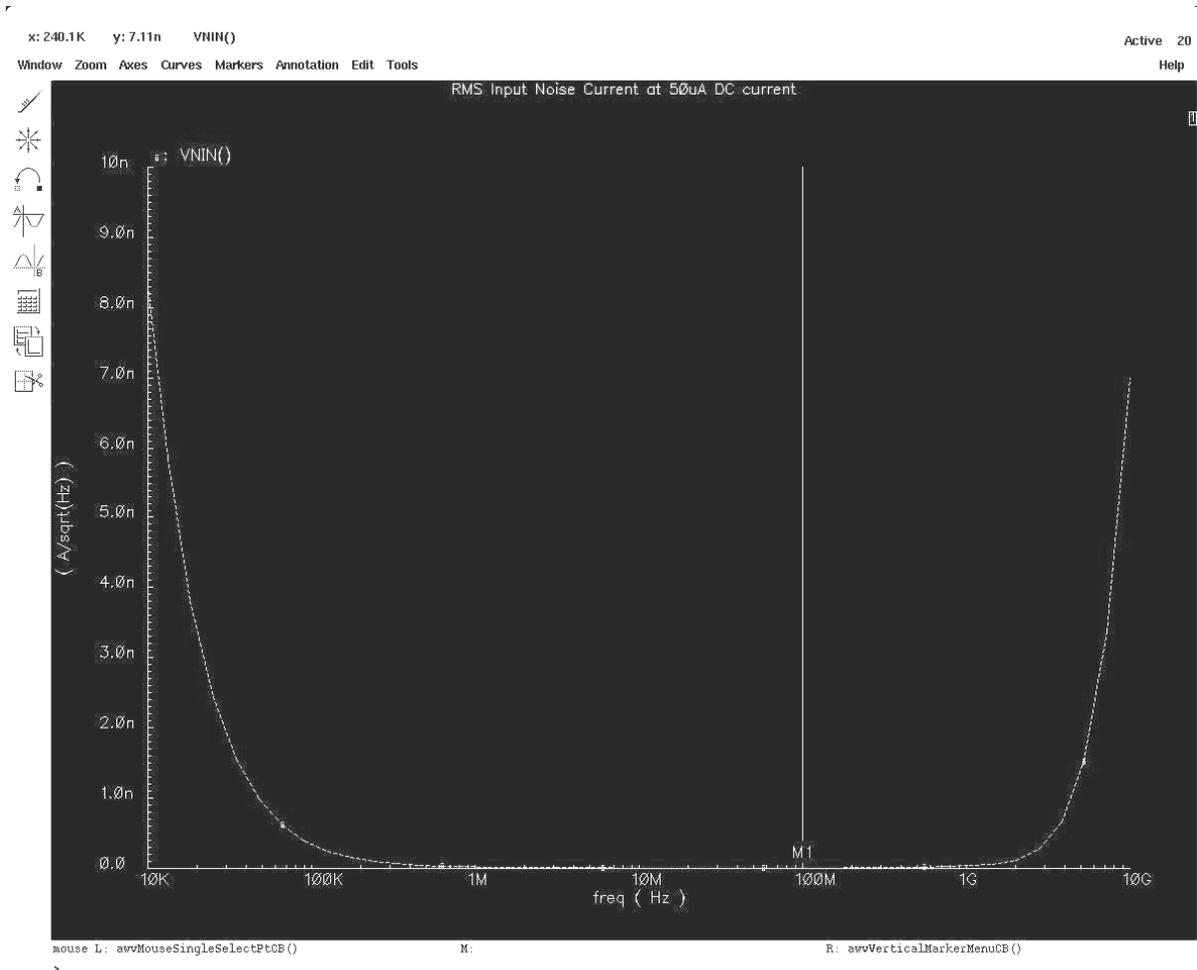


Figure 8 RMS input noise current calculated by the Cadence Spectre simulator

Figure 8 shows the RMS input current calculated by Cadence. The noise current at 100 MHz is $4.834 \text{ pA}/\sqrt{\text{Hz}}$ which is slightly more than the hand calculations and Orcad Pspice results. This might be due to the fact that various parts of the circuit including the current reference was not modeled in the Orcad simulation and Mosis model parameters provided for the Spectre simulator are much more accurate than the Orcad Pspice parameters. It is therefore safe to say that the circuit exhibits a worst case noise current of $4.834 \text{ pA}/\sqrt{\text{Hz}}$.

6 Transimpedance Amplifier Stage

Various topographies can be used for building a transimpedance amplifier. One can use a single-ended or differential structure that has a common-gate [28] or a common-source input. In addition, a common-gate and common-source cascade structure is presented in [3] in which the common-gate stage acts as a current buffer and isolates the parasitic capacitance of the photodiode from the input impedance of the common-source stage. Single-ended amplifiers are simple to design but do not have the power supply rejection and the common mode noise rejection of their differential counterparts. In both single-ended and differential devices, the load resistances in amplifiers can be implemented using passive resistors or MOS devices. Active loading is used in applications where the required voltage gain of the amplifier is large. This is especially true in CMOS processes where the transistors do not have a large transconductance. Active loads make use of the output impedance of the MOS devices which is higher than a poly resistor of the same dimensions. This maximizes the output impedance hence the voltage gain of the amplifier using less silicon area than polysilicon resistors. Also, in resistively loaded amplifiers, the designer can not set the operating current, gain and the common mode level independently from one another. In active loading it is possible to set the load impedance and current independently through physical device dimensions and the common mode is determined by an external feedback loop. This adds flexibility to the design process.

There are however disadvantages to the use of active loading. In fully differential amplifiers it is usually necessary to use a common mode feedback loop which adds more complexity and other sources of noise to the circuit. The common mode feedback loop is needed in actively loaded differential amplifiers because the common mode of the output signal cannot be determined as easily as in the case with the passive resistors since the common mode depends on the current mismatch of the tail current source and the active load transistors. The large open loop gain of the actively loaded amplifier makes the common mode very sensitive to process variations which is another reason for using a feedback loop. In this design, the high close-loop gain requirement with the low transconductance of the MOSFET devices in TSMC 0.18 μ m process rendered the use of active loading in the TIA stage

essential. Other techniques such as cascoding are suggested in literature in order to increase the gain bandwidth product by eliminating the Miller multiplication of the gate-drain capacitance however cascoding consumes swing headroom and thus was not used in this project [1, 2]. Furthermore, the use of shunt inductive peaking is suggested in [17-20] as a method of improving bandwidth without sacrificing gain, however this technique is not possible due to the utilization of active loads in this design.

There are various active loading schemes which display the tradeoffs between gain, and output swing. These schemes include diode connected loads, current source loads and depletion device loads [1, 2]. Diode connected loads present a reduced voltage swing at the amplifier output because the output can only swing within $V_{CC} - V_{TH}$. In comparison the current source loads can allow a swing within $V_{CC} - V_{OV}$ where V_{OV} is the overdrive voltage of the load device. The overdrive voltage is not defined by the process parameters but rather by the designer by means of device geometry and drain current and is usually smaller than the threshold voltage. The depletion device behaves like a current source in the active region and can have a large output impedance [1] but presents a large capacitance to the drain of the input device hence slowing down the frequency response of the circuit.

This design incorporates an actively loaded differential common-source stage using current source loads followed by a source follower stage to prevent the feedback resistor from loading the differential common-source input stage. The gain bandwidth product of the amplifier is in the order of 5 GHz (Figure 9 shows the frequency response of both differential outputs). In transimpedance amplifiers, the closed loop bandwidth depends on the open loop gain with the following relation [3].

$$f_{CL} = \frac{A_{OL}}{2\pi C_T R_F} \quad (15)$$

This is a first order relation where A_{OL} is the open loop gain at the desired closed loop bandwidth, C_T is the total capacitance the amplifier sees and R_F is the feedback resistor. However the TIA is really a second order system because of the pole created by the amplifier itself. The relationship for a second order system is given by:

$$f_{CL} = \frac{\sqrt{2}A_{OL}}{2\pi C_T R_F} \quad (16)$$

Using the first relation for a conservative approach, and defining the gain A_{OL} at 100 MHz which is the desired bandwidth for the closed loop system, we get a calculated bandwidth of 264 MHz for a closed loop gain of 16000 Ω . The differential TIA designed for this project achieves a 212 MHz bandwidth and 15500 Ω (83.8 dB) single-ended gain (Figure 10 shows the frequency response of each differential output in dB versus frequency in Hz) for the unloaded case. When the TIA is loaded with the DC cancellation circuit the buffer stage and the common mode feedback circuit, this bandwidth increases to 254 MHz which is actually higher than the unloaded case (Figure 11). This might be due to peaking in the frequency response due to the capacitive load that is caused by the aforementioned circuits.

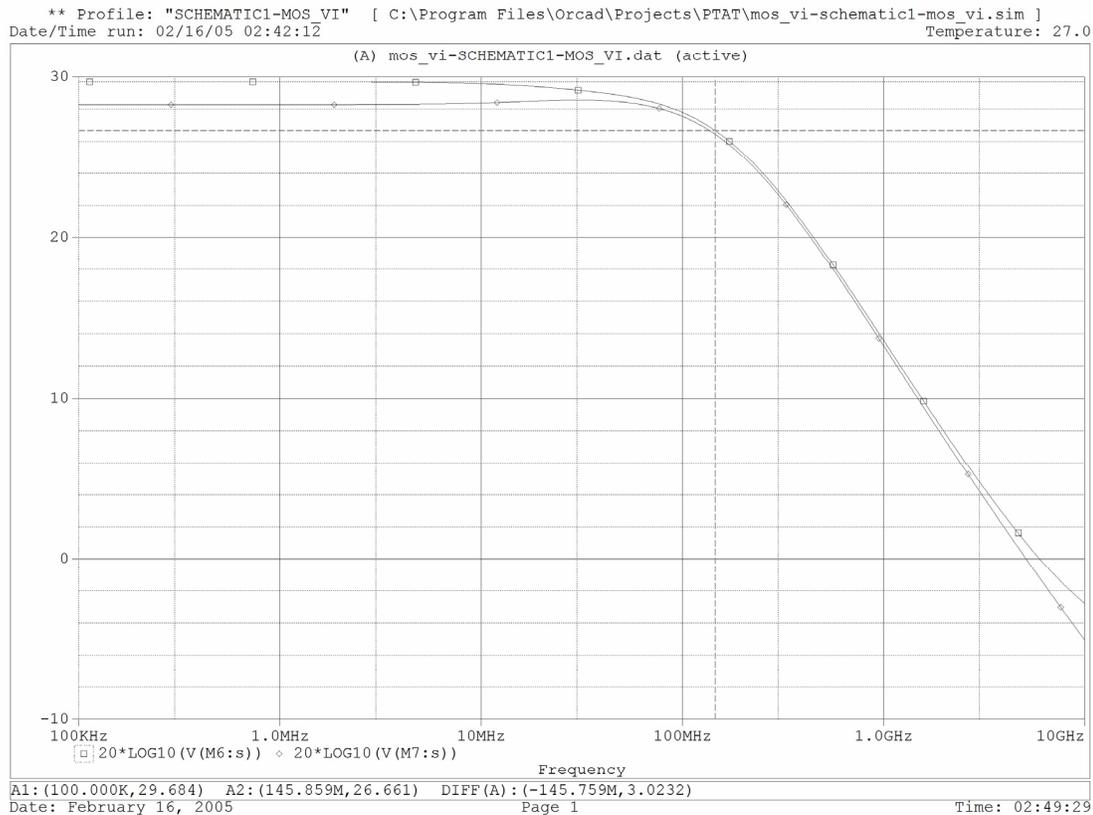


Figure 9 Open loop frequency response of the TIA

This design uses only one feedback resistor from the positive input to the negative output. The other input is biased at the local common mode voltage of 1.2 V. Compared to

most other applications that use two feedback resistors (one for each leg of the differential amplifier) the gain of the amplifier is doubled because the effective feedback is halved. Thus with a feedback resistor of 16 kΩ in the transimpedance stage, the individual gains of the differential legs are 16 kΩ and the differential gain is 32 kΩ. This performance can be matched using two feedback resistors of twice the value which reduces the bandwidth of the amplifier significantly. The only drawback of using a single feedback path is the resulting mismatch in the common mode response of the outputs which will be discussed in Chapter 7.

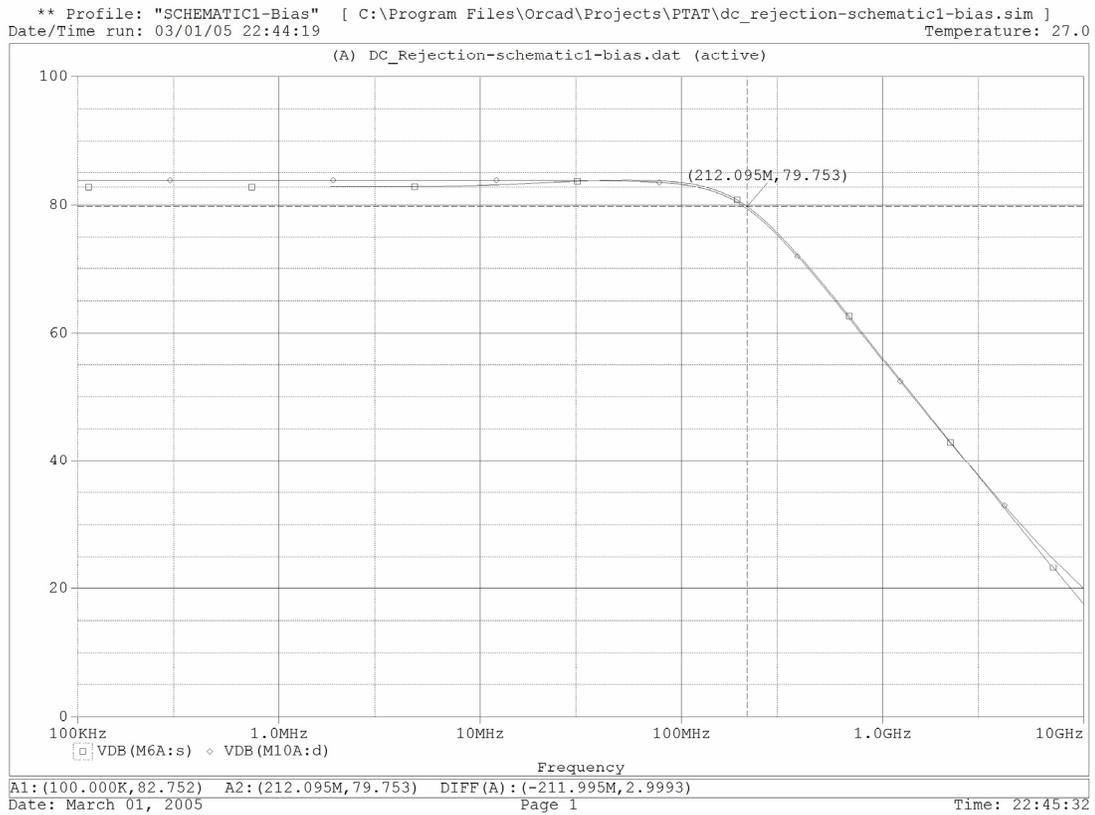


Figure 10 Closed loop frequency response of the unloaded TIA

Device sizing for the transimpedance amplifier brings a tradeoff between noise performance and gain. As explained in the previous chapter the transconductance of the input devices have to be larger than the transconductance of the current-source load devices for a satisfactory noise performance. For this reason the input devices were sized to have a

width of 60 μm and a drawn length of 350 nm. The short gate length keeps the input capacitance low while the high width to length ratio results in a high g_m . The current-source load devices have a width of 42 μm and a length of 1 μm . The increased length of these devices increase the total output impedance thus increasing the gain while possessing a lower g_m to satisfy noise performance.

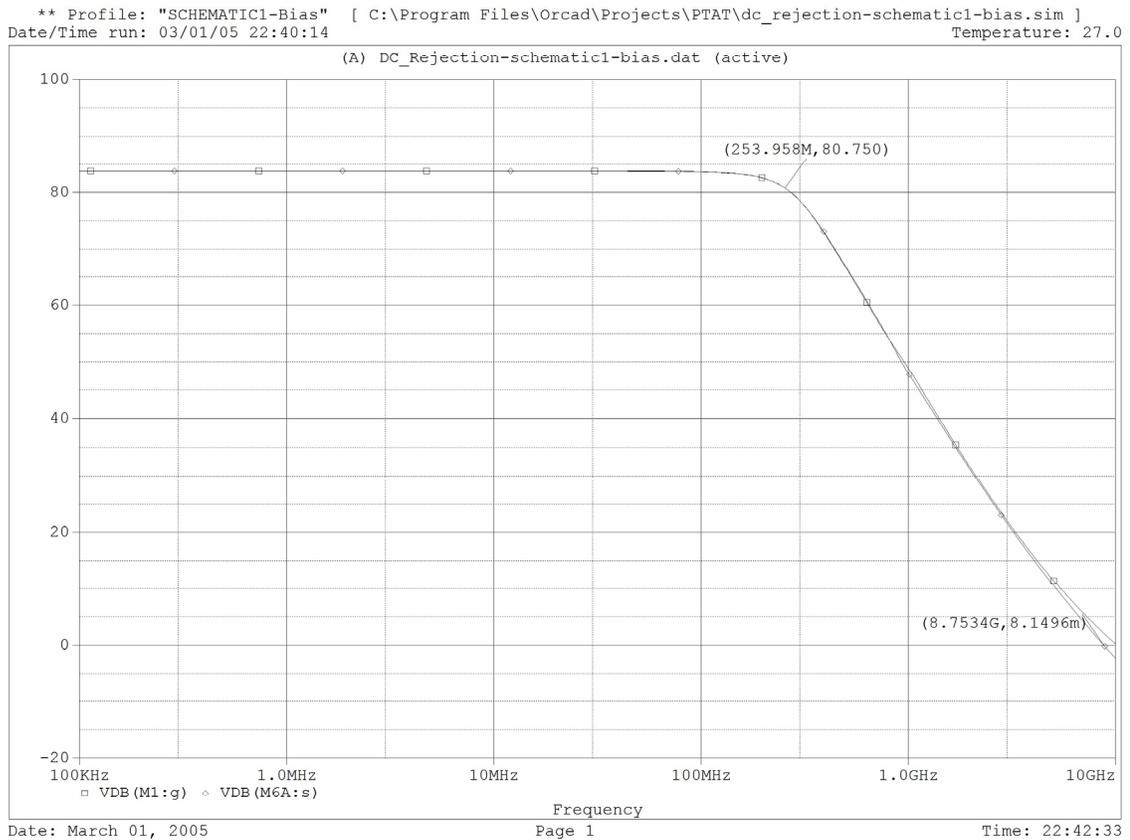


Figure 11 Closed loop frequency response of the loaded TIA

In this circuit, VIN1 and VIN2 are connected to the outputs of the differential amplifier. V_{CM} is the reference voltage that is set to the desired common mode voltage. V_{BIAS} is connected to the gate of the current mirror loads in the differential amplifier. V_{CMC} is the control voltage generated and it is connected to the gate of the tail current source of the differential amplifier. The operation of the circuit is summarized as follows. If the common mode voltage of the amplifier goes below V_{CM} , then current is steered away from Q2 and Q3. This reduces the current passing through Q7 decreasing its gate-source voltage. Since the gate of Q7 and the gate of the tail current source of the differential TIA are connected together forming a simple current mirror, the current through the TIA tail current source also decreases. This in turn causes the output common mode of the amplifier to increase towards V_{CM} . An increase in the common mode voltage causes the opposite reaction. However, if one of the output voltages (VIN1) increases while the other (VIN2) decreases by the same amount (differential stimulus), the current through Q2 decreases and current through Q3 increases by the same amount, thus the current through Q7 does not change keeping the common mode voltage constant. In this design, transistors Q5 and Q6 are sized to have twice the width of the load transistors so that the current through Q7 and the TIA tail current source are the same. The input transistors of the common mode feedback circuit are sized so that they satisfy differential mode swing specifications. The differential swing at the output of the TIA is specified as 600mV. It is explained in [1] that in order to accommodate a differential swing of magnitude V , the overdrive voltage V_{ov} has to satisfy:

$$\sqrt{2}V_{ov} \geq V \quad (17)$$

$$V_{ov} = \sqrt{\frac{2I_D}{k' \left(\frac{W}{L}\right)}} \quad \text{and} \quad k' = \mu_n C_{OX} = \frac{\mu_0}{2} C_{OX} \quad (18)$$

To be conservative the overdrive voltage for the differential pairs was chosen to be twice the minimum value. This led to a width to length ratio of 50 with the length equal to 180 nm which is the minimum allowed length for PMOS devices in the TSMC 0.18 μm process.

The CMFB circuit rejects differential signals perfectly as long as the differential swing does not exceed the input swing capability of the CMFB input devices. In addition to

this, the feedback circuit does not interfere with the operation of the DC cancellation circuit either since the changes induced by a change in the input DC photodiode current manifests itself as a divergence in the output DC levels (also a differential change which is rejected by the CMFB circuit).

The bandwidth and the gain of the CMFB circuit is also important for successful rejection of CM signals since not all common mode disturbances will be low frequency. In the event of common mode noise, the higher bandwidth of the CMFB circuit is an advantage. It is desirable to have the bandwidth of the common mode feedback loop equal to the bandwidth of the differential amplifier but it is not an easy task [1]. As mentioned before the transimpedance amplifier used in this design has only one feedback from the inverting output to the input. The non-inverting output does not have a feedback resistor that is connected to the inverting input. For this reason, the common mode response of the two legs are different.

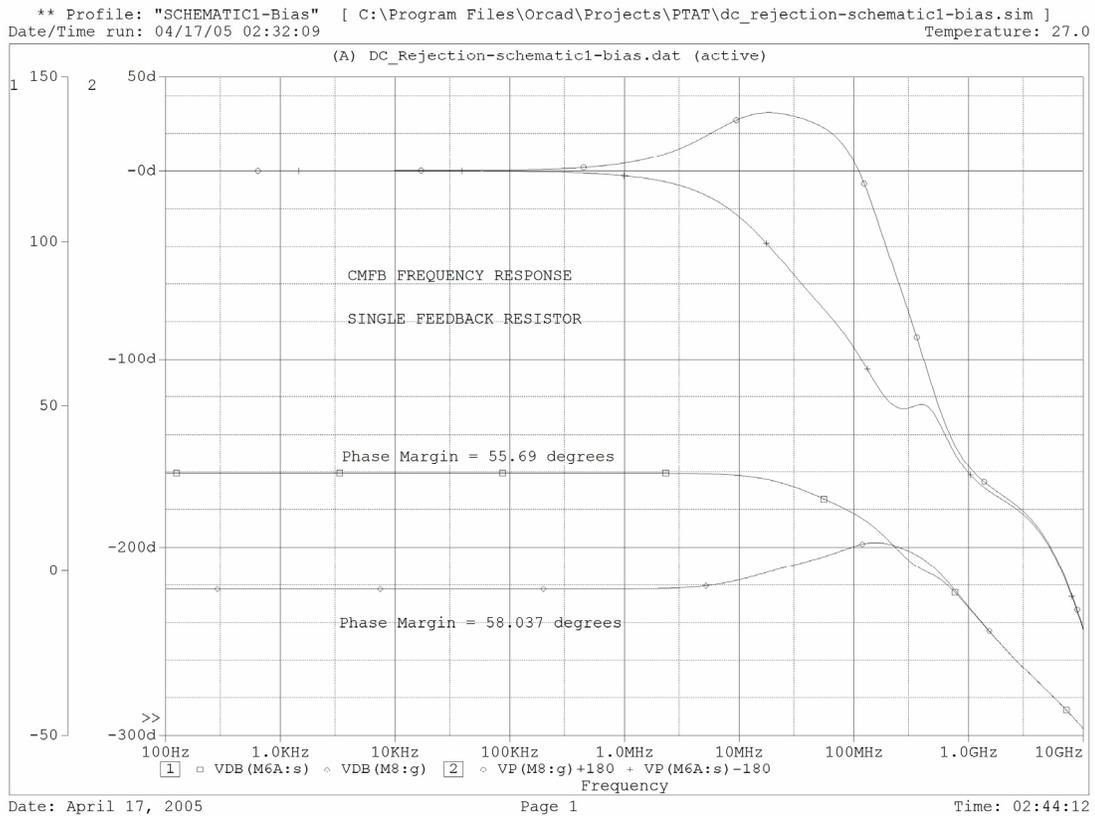


Figure 13 Frequency response of the CMFB loop for the single resistor feedback TIA

Figure 13 shows the open loop frequency response of the common mode feedback circuit for the single feedback resistor design. The top two plots show the phase in degrees for the two outputs of the TIA and the bottom two plots show the gain response of the CMFB loop for the two outputs. Although the phase margin of the two legs are adequate, one of the legs exhibit a very low loop gain at lower frequencies compared to the other leg. This causes the outputs to react with different rates to a disturbance so the CMFB loop creates a differential response. This response however is countered by the DC current cancellation loop which senses the differential change and corrects the problem.

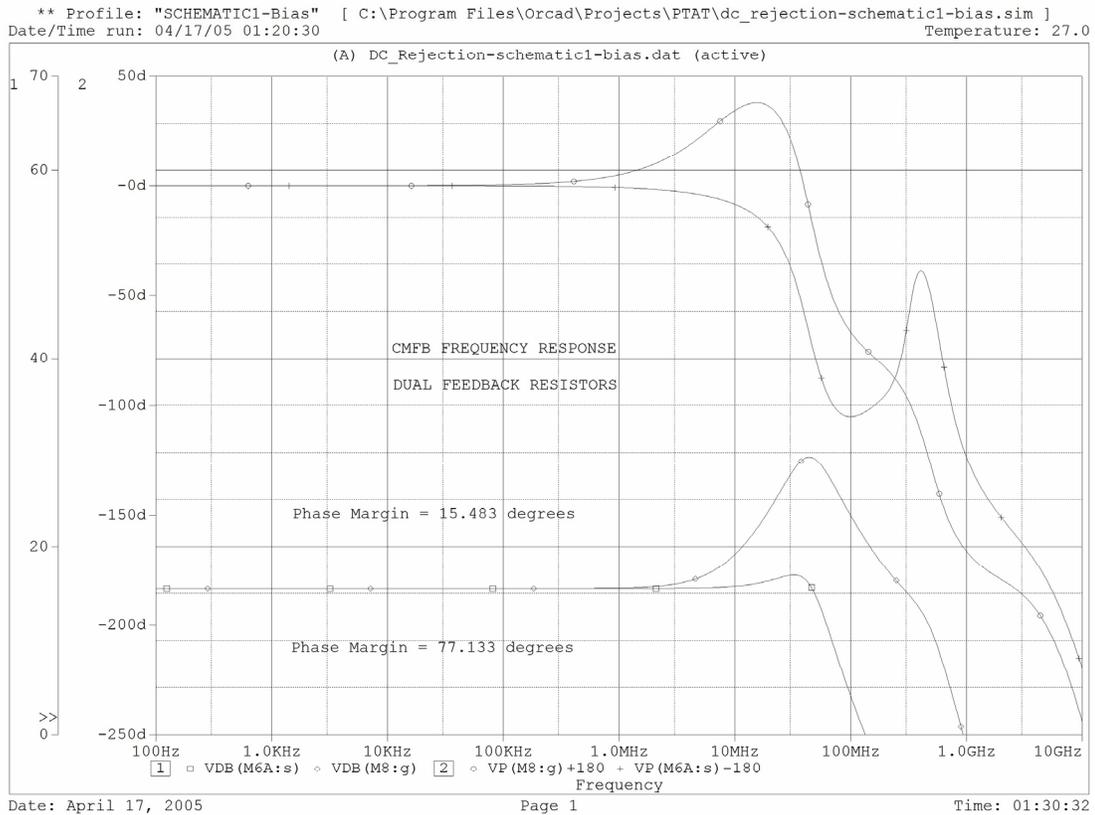


Figure 14 Frequency response of the CMFB loop for the dual resistor feedback TIA

The dual feedback resistor TIA does not have the problem mentioned above and as can be seen from Figure 14. The loop gain of both legs is consistent over most of the pass band which results in a balanced common mode response of the differential outputs. This

advantage however comes at a greater cost of overall system bandwidth and thus was not used in the final design.

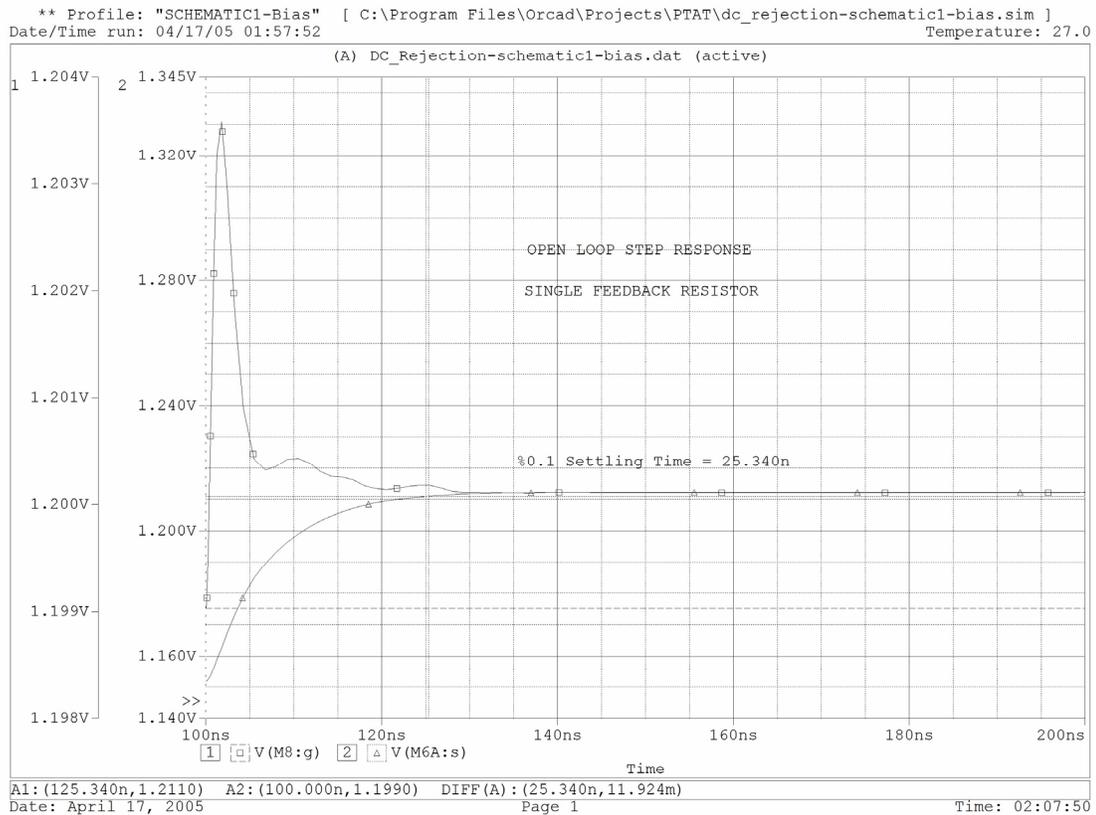


Figure 15 Open Loop common-mode step response of CMFB loop for the single resistor feedback TIA (Plots reflect the output voltages of the TIA at the point where the loop is broken)

Figure 15 shows the open loop step response of the CMFB loop for the single resistive feedback case where one can see the difference in the response of both outputs (note that the scales of the two y axes are different for illustrative purposes). The settling time is 25.34 ns which corresponds to the slower leg. The open loop step response on both cases is calculated by opening the loop at the outputs of the TIA, injecting the disturbance voltage to the inputs of the CMFB circuit and observing the output response of the TIA.

The open loop step response for the dual resistive feedback case is shown in Figure 16 where one can see that the responses of the two outputs are much similar except for the

increased overshoot of one of the outputs which is reflected in the frequency response (Figure 14) as a higher peak at around 30 MHz and lower phase margin.

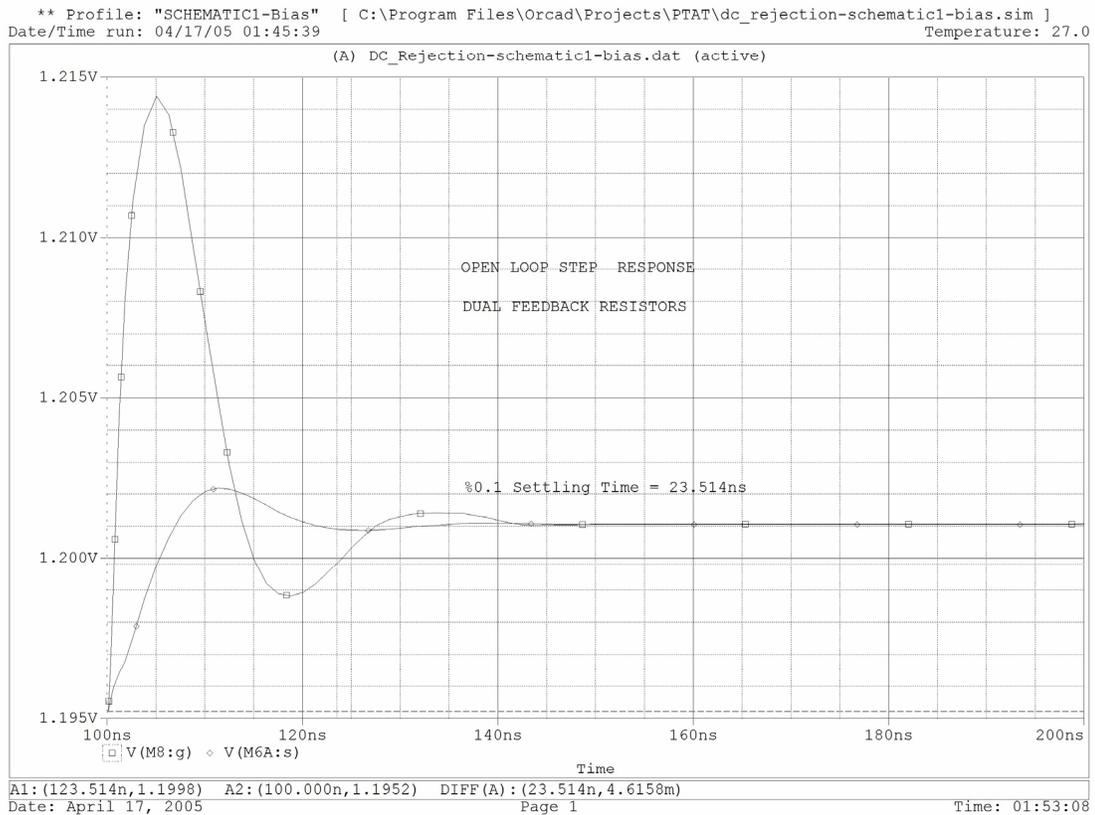


Figure 16 Open loop common-mode step response of CMFB loop for the dual resistor feedback TIA

The settling time of this case is close to the single resistor feedback TIA at 23.514 ns.

It is more important to observe the step response of the common mode feedback amplifier in the closed loop configuration because ultimately, this will be how the circuit will function. Therefore simulations were performed where the disturbance voltage source is connected in series with the common mode control net which controls the tail current source gate voltage of the transimpedance amplifier. Figure 17 shows the closed loop step response of the CMFB loop in the single feedback resistor case to a 1 mV disturbance voltage. The reader should note that the DC current cancellation loop is not helping the CMFB loop in this

case because the bandwidth of the DC cancellation loop is not high enough to respond fast enough.

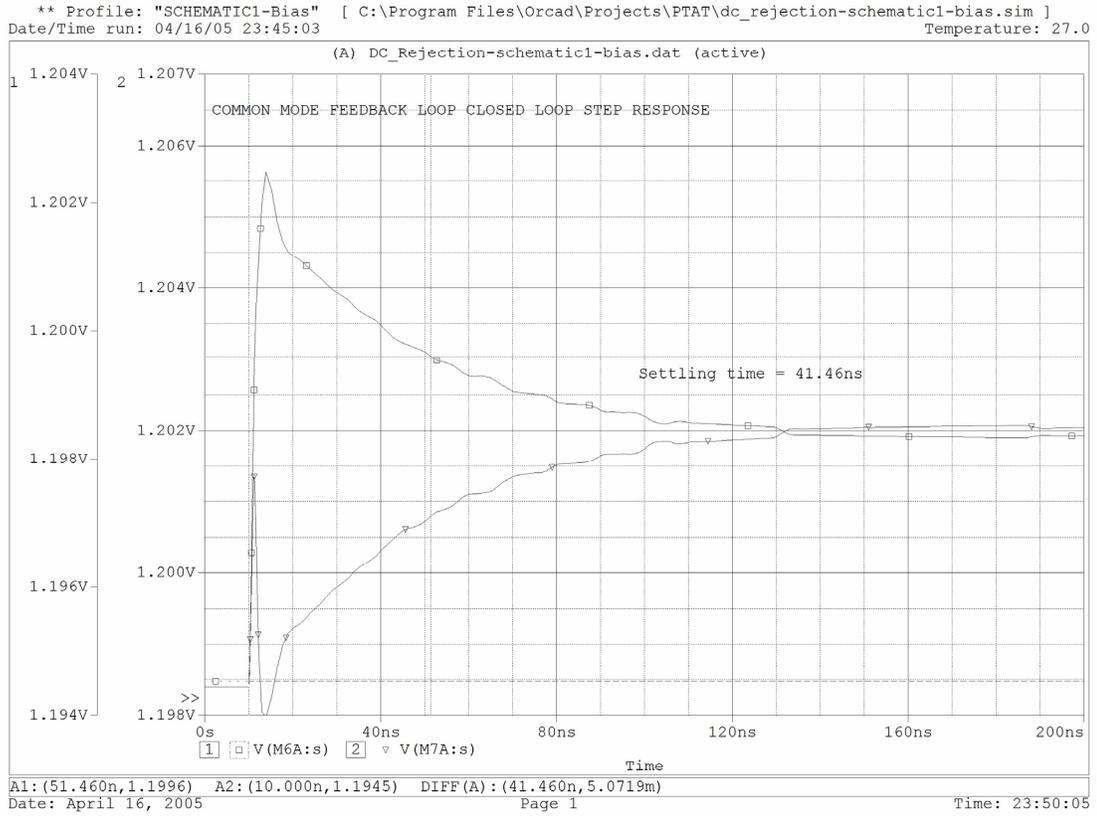


Figure 17 Closed loop step response of the CMFB for the single resistor feedback TIA

8 DC Cancellation

The most important aspect of this design is the ability to function with large DC photodiode currents. The DC current is the result of the total reflected light from the sample that is imaged by the OCT device. As mentioned before if this DC current is allowed to enter the amplifier, the gain would be greatly reduced because of the diverging DC levels at the output. Two DC cancellation techniques were considered which included a circuit described in [7] where the outputs of the TIA are fed into an error amplifier which produces a proportional control voltage that drives a MOSFET that sinks the DC photodiode current. The circuit described in [8] uses a negative and a positive peak detector to sense the DC levels of the outputs instead of using averaging. This technique requires more active devices that contribute additional noise to the system and does not have a clear advantage over the averaging technique. The error amplifier in [7] is implemented in this project with a single stage differential to single-ended amplifier used open loop with a single pole low-pass filter at its output. The low-pass filter determines the bandwidth of the DC current rejection loop since the error amplifier and the TIA have much larger bandwidths (Figure 18). The filtered output is directly tied to the gate of the NMOS that sinks the DC current from the photodiode. The size of the NMOS device that sinks the current is a critical design parameter. If the width is made too small then the MOSFET can not sink large currents. However it can not be made arbitrarily large because the device is a significant source of noise at the input of the TIA. A W/L ratio of 3 was chosen for this design and this allows currents up to 700 μA to be sunk.

The DC cancellation circuit adds a zero and a pole to the closed loop system. The zero is at a much lower frequency than the pole [7] which gives the overall TIA response a band-pass characteristic. The zero and the pole correspond to the dominant pole of the DC cancellation loop that is set by the low-pass filter, and the pole which marks the low cutoff frequency in the system response is the gain-bandwidth product of the open loop frequency response of the DC cancellation loop. This is explained in [7] with the following equations. The open loop gain of the DC cancellation loop is given by:

$$A(s) = g_m R_f A_{COMP}(s) = \sqrt{2\mu_n C_{OX} \frac{W}{L} I_D R_f} A_{COMP}(s) \quad (19)$$

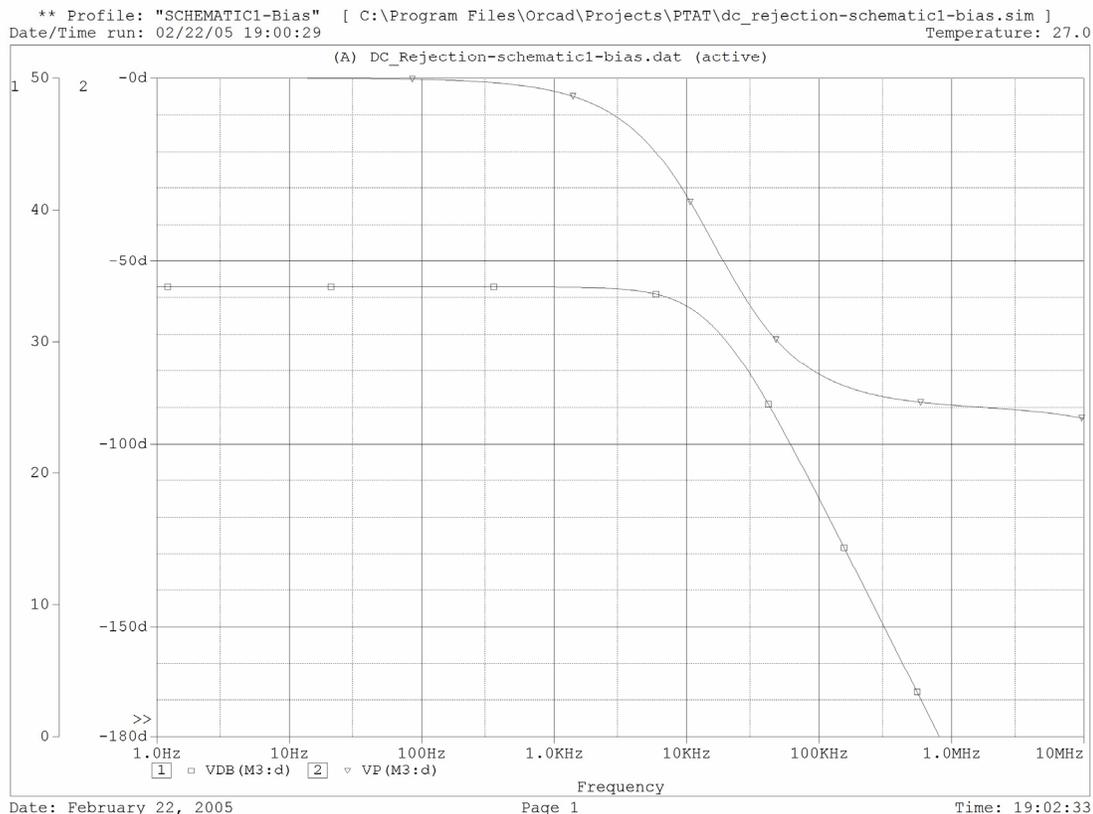


Figure 18 Frequency response of the error amplifier with low-pass filtering (10 kHz bandwidth)

As can be observed from this equation, the loop gain is dependent on the current that the NMOS sinks (through the transconductance of the MOSFET). Since the gain increases with drain current one can see that the feedback loop becomes more effective in high DC current conditions however the following equations show a disadvantage of this phenomenon. We can describe the error amplifier gain $A_{COMP}(s)$ as a single pole system with the pole set by the low-pass filter.

$$A_{COMP}(s) = \frac{A}{1 + \frac{s}{\omega_P}} \quad (20)$$

Since ω_p can be taken to be the bandwidth of the whole DC cancellation loop we can describe the gain bandwidth product of this system as:

$$|A(j\omega_p)| \cdot \omega_p = \omega_t \quad (21)$$

$$\omega_t = \sqrt{2\mu_n C_{OX} \frac{W}{L} I_D R_f A \omega_p} \quad (22)$$

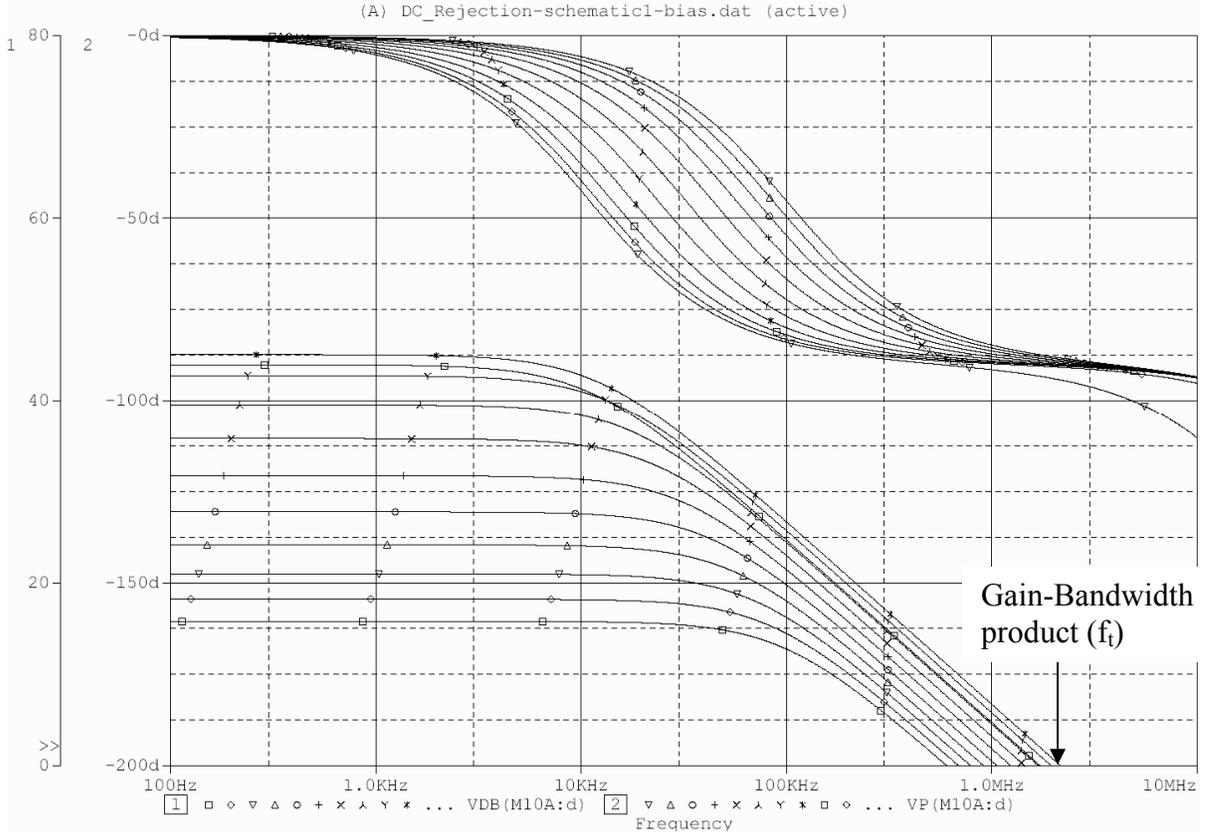


Figure 19 DC current cancellation loop frequency response with changing DC current inputs

The gain of the DC current cancellation loop in this design is also dependent on the gain of the error amplifier, which is not linear. Figure 19 shows the bode plot of the open loop gain and phase of the DC current cancellation loop at different DC current levels. The simulation results are achieved with changing the differential input of the error amplifier to simulate DC current entering the TIA. Initially as the current that is sunk through the MOSFET increases and the gain of the error amplifier increases, the overall open loop gain of the DC current cancellation loop increases. However as the MOSFET reaches its fully on state the average output of the error amplifier reaches its peak, the error amplifier begins to

saturate flattening the gain curve and reducing the loop gain of the DC current cancellation loop. The change in loop gain changes the gain-bandwidth product of the loop. The lowest and highest current values in this plot correspond to the traces denoted by the square symbols.

Looking at the overall system response in Figure 20 we can see that ω_t (or rather f_t in Figure 19) corresponds to the lower cutoff frequency where the effectiveness of the DC cancellation diminishes. We can also see the dependence of f_t on the DC current in this plot.

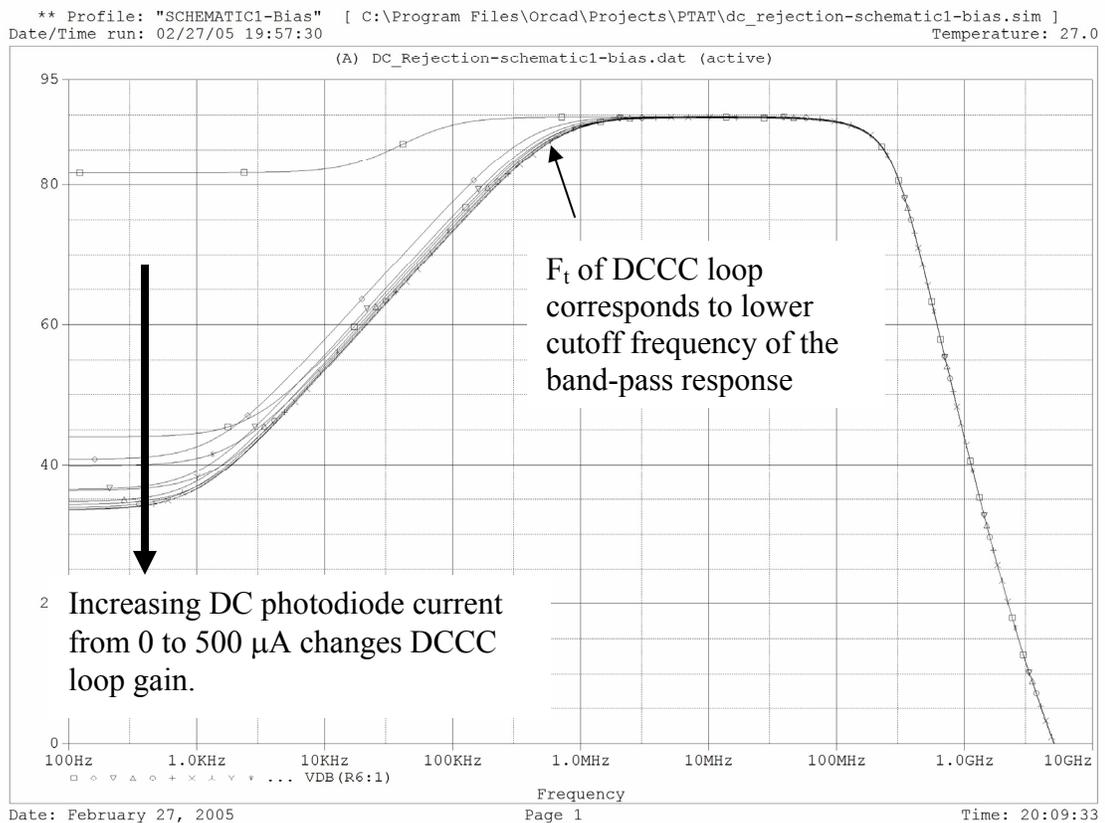


Figure 20 Overall system frequency response with DC cancellation loop

The change in f_t is not a big issue as long as the pass-band is not made too narrow by increasing the bandwidth of the DCCC loop filter. In the case that the lower cutoff frequency is too close to the pass-band frequency, any change in DC current may affect the pass-band gain of the system due to peaking. For this application it is imperative to keep the gain and

bandwidth of the system stable over all light conditions so the bandwidth of the DC cancellation loop must be set low enough to avoid the peaking phenomenon. Another concern here is the speed at which the DC cancellation loop reacts to changes in ambient light which primarily affects the speed with which the optical coherence tomography device can scan a specimen laterally. If the bandwidth is set too low, speed of the DCCC step response suffers, limiting the speed with which lateral scanning can be achieved. In simulations, a bandwidth of 100kHz was observed to yield fast settling times on the step response without affecting the pass-band response of the system. The low-pass loop filter is designed to be implemented off the chip so the user can tune the lower cut-off frequency. An on-chip implementation would consume significant silicon area since the filter elements are large.

The error amplifier in this project is implemented with a single gain stage differential amplifier and because of the low g_m of the CMOS process, the open loop gain of the amplifier is 50. This makes this particular amplifier poorly suited to the DC cancellation application if it is used with local feedback. Although feedback makes the gain of the amplifier more linear, lower gain means slower step response to changes in ambient light. When it is used in the open loop configuration, fastest step response is achieved from 100 μA to 300 μA , but the settling times increase as the current approaches 400 μA (Figure 21).

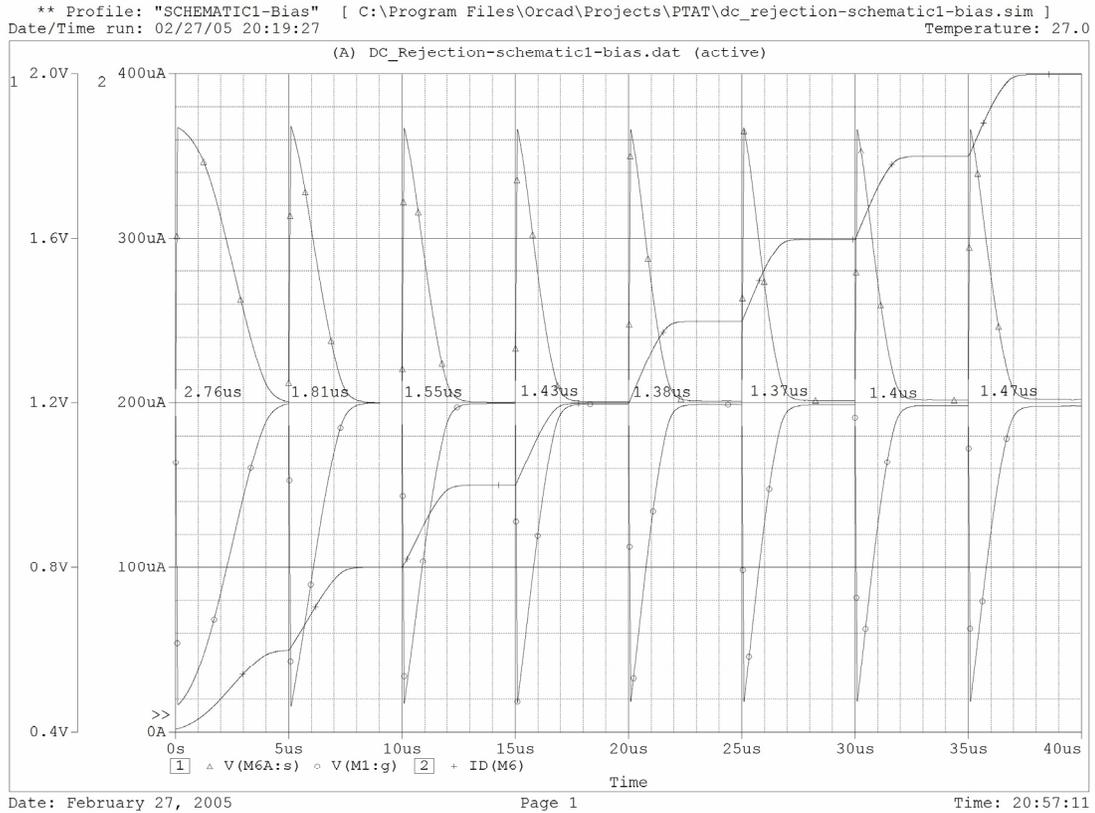


Figure 21 DC cancellation loop step response vs. input DC photodiode current

Further improvements on this circuit could be the implementation of a high gain feedback amplifier with linear gain that would result in a uniform step response over all DC photodiode current conditions. Higher open loop gain also decreases the steady state error at the outputs of the TIA.

Degenerating the source of the DC cancellation MOSFET with a resistor proved to be beneficial since this makes the gain of the DC cancellation loop less dependent on the g_m of the device, however making the value of this resistor too large affects the gain at the desired frequency of 100 MHz. Figure 22, 23 and 24 and Table 3 show the relationship between the value of the degeneration resistor, the frequency spread at different DC current levels and the gain at 100 MHz.

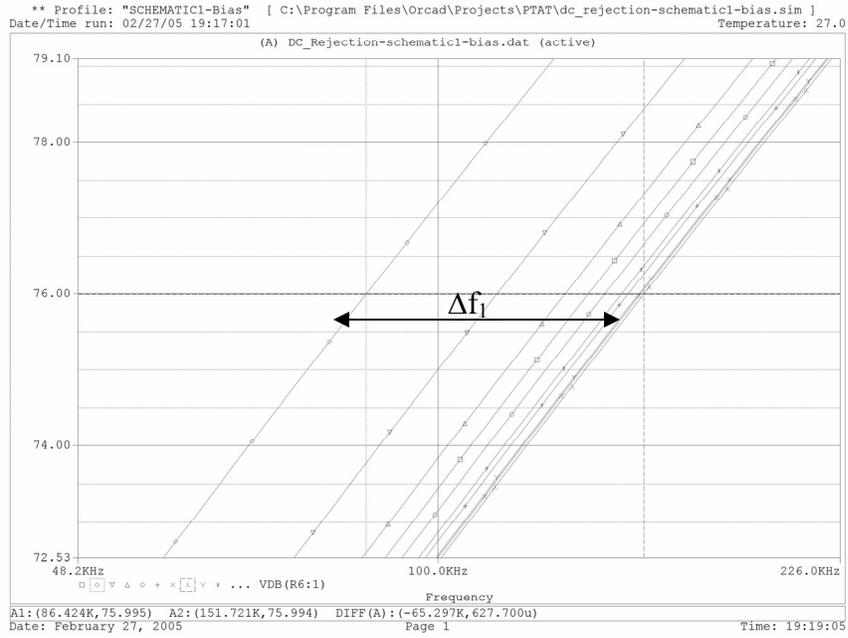


Figure 22 Frequency spread Δf_1 due to DC current at 0 Ω degeneration (65kHz)

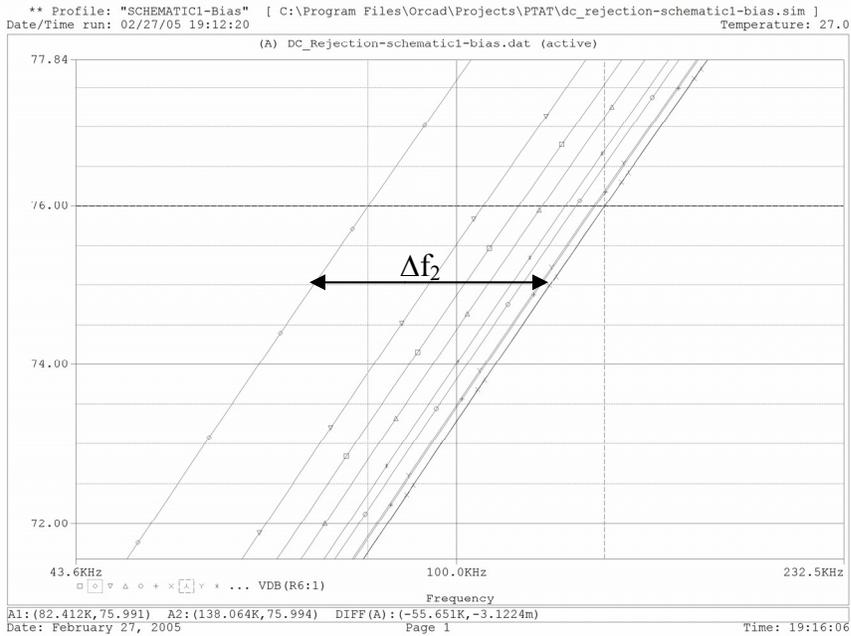


Figure 23 Frequency spread Δf_2 due to DC current at 200 Ω degeneration (56kHz).

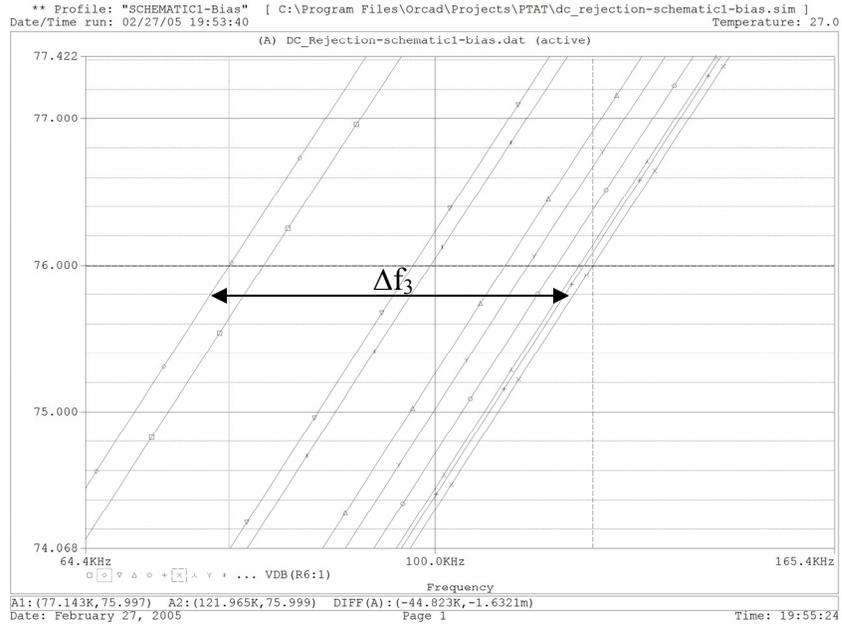


Figure 24 Frequency spread Δf_3 due to DC current at 500 Ω degeneration (45kHz)

Degeneration Resistor (Ω)	Gain Spread at 100 MHz (dB)	Gain Ratio at 100 MHz (Max/Min)
0	0.141	1.016
200	0.221	1.026
500	0.510	1.060

Table 3 Gain behavior at 100 MHz with different degeneration resistor values

It is apparent that although increasing the degeneration resistor's value reduces the frequency fluctuation in the lower cutoff frequency of the system, it affects the gain at the desired frequency of 100 MHz. Since the aim of this design is to achieve a constant gain over a range of DC input currents, a value of 200 Ω is a good compromise between gain stability and lower cutoff frequency fluctuation.

9 Output Buffer

The output buffer enables the TIA to drive an external load of 50Ω . In bipolar circuits, output buffers are usually implemented using emitter followers, however in CMOS, the low transconductance of the source follower results in gains much lower than 1 [2]. Since this is unacceptable, a differential common source stage was used instead for the output buffer. Moreover the design requires that the buffer must be able to sink 9mA of current which necessitates that the device widths be large in order to keep the voltage swing large. This in turn leads to increased capacitance at the input of the buffer which degrades the bandwidth. For this reason a circuit called the f_t doubler is implemented which effectively reduces the input capacitance by half using the same geometry devices as the regular differential pair [2]. The f_t doubler is formed by having two differential pairs that have common outputs. Figure 25 shows this configuration.

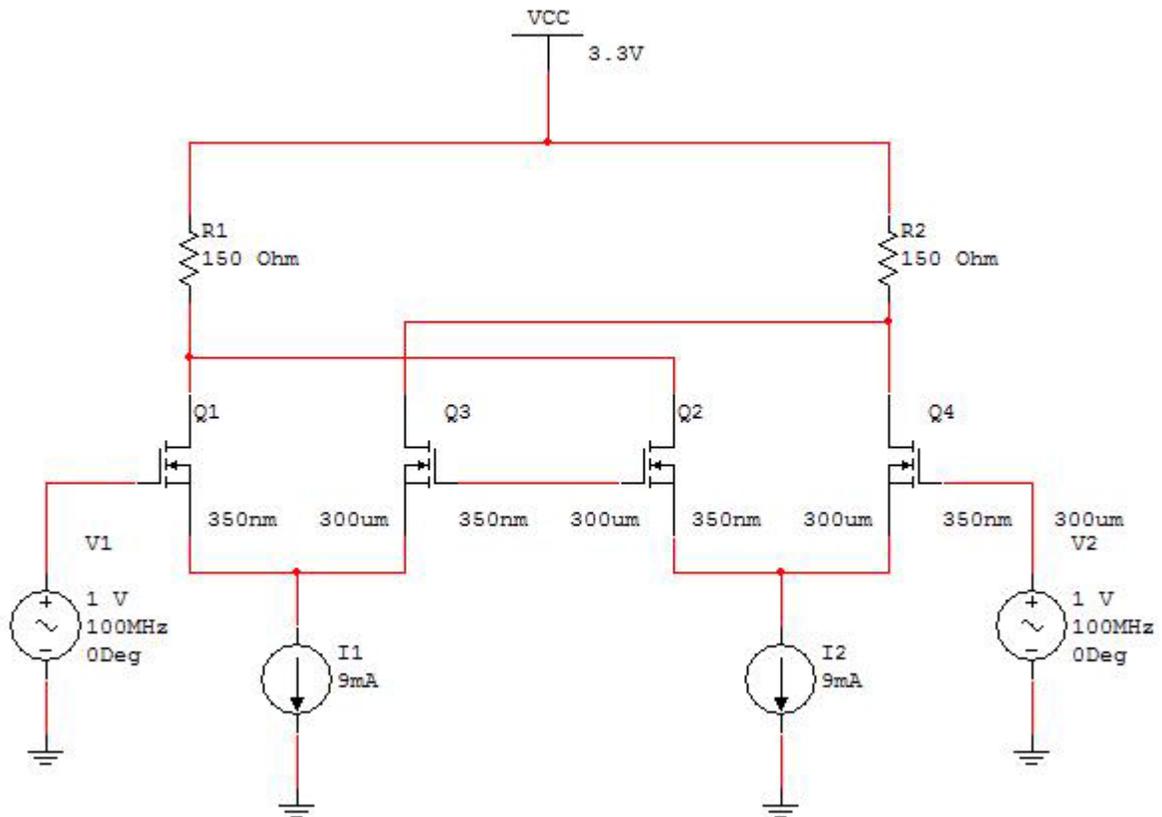


Figure 25 f_t doubler configuration

The current that passes through the load resistors are shared between two devices which reduces the amount of current that goes through the individual differential pairs. This allows for smaller devices to be utilized while retaining the same gain which reduces the overall input capacitance. In addition to the f_t doubler the buffer has a separate input stage which is a source follower. The primary function of this stage is shifting the 1.2V common mode voltage to 2V while the smaller dimensions of the transistors used in this stage present a smaller capacitance to the rest of the circuit. Although this stage presents a gain which is less than one, the gain of the following f_t doubler stage compensates for this loss. The buffer was designed so that the parallel transistors that form the output differential pair, along with the output resistance of 150 Ω present an effective output impedance of almost 120 Ω . This value, considering the frequency of operation is not high is a good balance between good matching and good power consumption. It is explained in [2] that with the addition of the package parasitics, the output impedance seen by the outside world is less than the calculated value so the output impedance was designed to be a higher value than 50 Ω . With the additional gain of the buffer, the total gain of the amplifier comes up to 22 k Ω with no impact on bandwidth.

10 Automatic Gain Control

Linearity of the gain over a wide input range is an important parameter in this project because any nonlinearity in the gain curve requires calibration of the post processing circuitry for this nonlinearity for correct amplitude detection. An uncalibrated circuit in the presence of a nonlinear gain will result in larger signals (where the gain curve starts to fall off due to saturation of the output devices) to be understated resulting in loss of contrast. In this design, greater linearity over a wide input power range is achieved by using a bilinear gain profile.

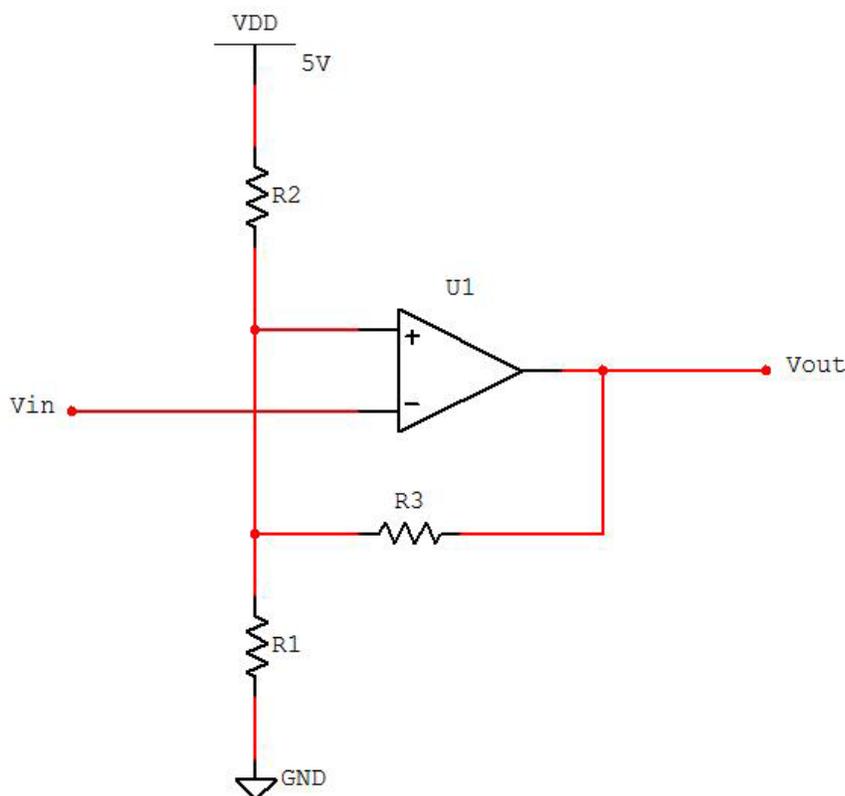


Figure 26 Schmitt Trigger

In [27] a novel circuit is described which achieves high dynamic range by changing the gain of the transimpedance amplifier at a particular output level. The output of the amplifier is the weighed sum of two separate outputs that increase “monotonically” [27] which eliminates the need for hysteresis. However the differential nature of the amplifier in

this project did not allow such a scheme to be used so automatic gain control is achieved by switching a MOSFET that is connected in series with a second feedback resistor. This setup is in parallel with the original feedback resistor which effectively reduces the gain of the amplifier in half when the MOSFET is turned on. This is a common AGC scheme in amplifiers but in most applications, the MOSFET is used in the triode region (linear) continuously adjusting the gain of the amplifier through channel resistance manipulation to keep it in its most linear range. In this application however, continuous adjustment of the gain is not desired because it creates ambiguity in sensing the current if the gain curve is not characterized properly. Therefore in this application, the automatic gain control MOSFET is switched on and off which leads to gain curve with two distinct slopes (bilinear) similar the application in [27] but different in the sense that the gain does not increase monotonically which is reflected in the graph in Figure 29. The point at which the gain curve changes is externally adjustable and is realized with a differential amplifier with hysteresis utilizing three external resistors to set the thresholds (Schmitt Trigger) [4].

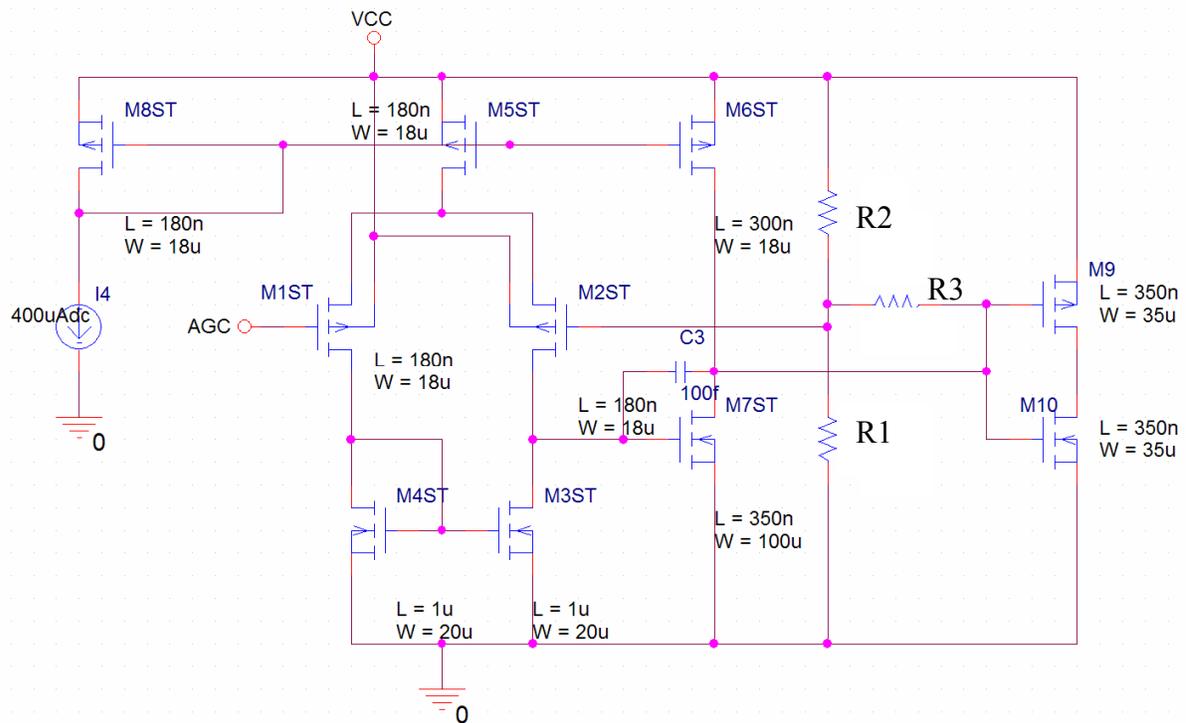


Figure 27 Schmitt trigger circuit implementation with two gain stages and inverter output stage

Hysteresis is required to eliminate the ambiguity at the point of switching and prevent an oscillation because unlike the circuit in [27] the output voltage does not always increase with increasing current. The Schmitt Trigger is an amplifier in which the reference voltage at the non-inverting input changes in response to the state of the output. Figure 26 is the system level diagram of this circuit.

In the case where the output is high (3.3V) the reference voltage is equal to:

$$V_{REF} = \frac{R_1}{R_{23} + R_1} \quad (23)$$

where R_{23} is the parallel combination of the resistors R_2 and R_3 .

If the output is low then the reference voltage is defined as:

$$V_{REF} = \frac{R_{13}}{R_{13} + R_2} \quad (24)$$

where R_{13} is the parallel combination of the resistors R_1 and R_3 .

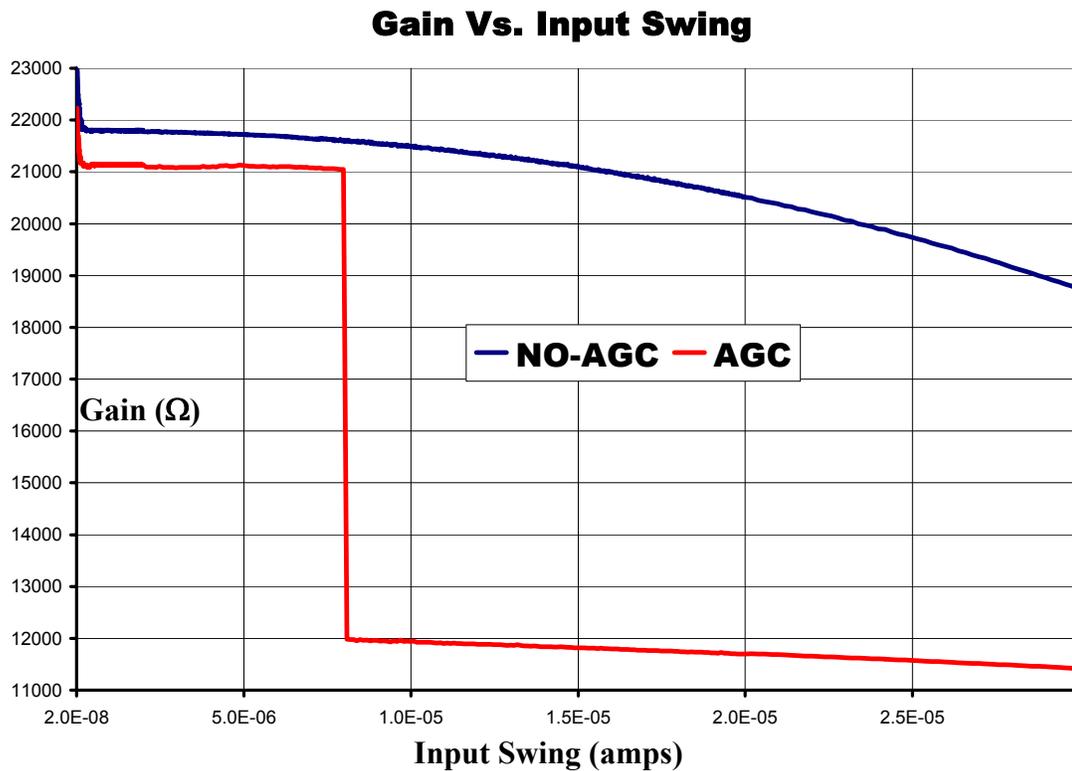


Figure 28 Gain of the transimpedance amplifier vs. input current amplitude with and without the automatic gain control. Note that the AGC results in increased linearity over a wide range of inputs (the switch point corresponds to the high threshold)

The Schmitt trigger used in this design is an op-amp with 2 gain stages with the first stage having a differential PMOS input (Figure 27). It utilizes Miller compensation [1, 26] and has an inverter output stage. The input to the Schmitt Trigger is provided by a peak detector which is tied to the non-inverted output of the transimpedance amplifier and is realized by a diode connected BJT whose area is large to keep the base emitter voltage drops small. The resistor and capacitor used to set the time constant of the peak detector are connected externally for the prototype for testing.

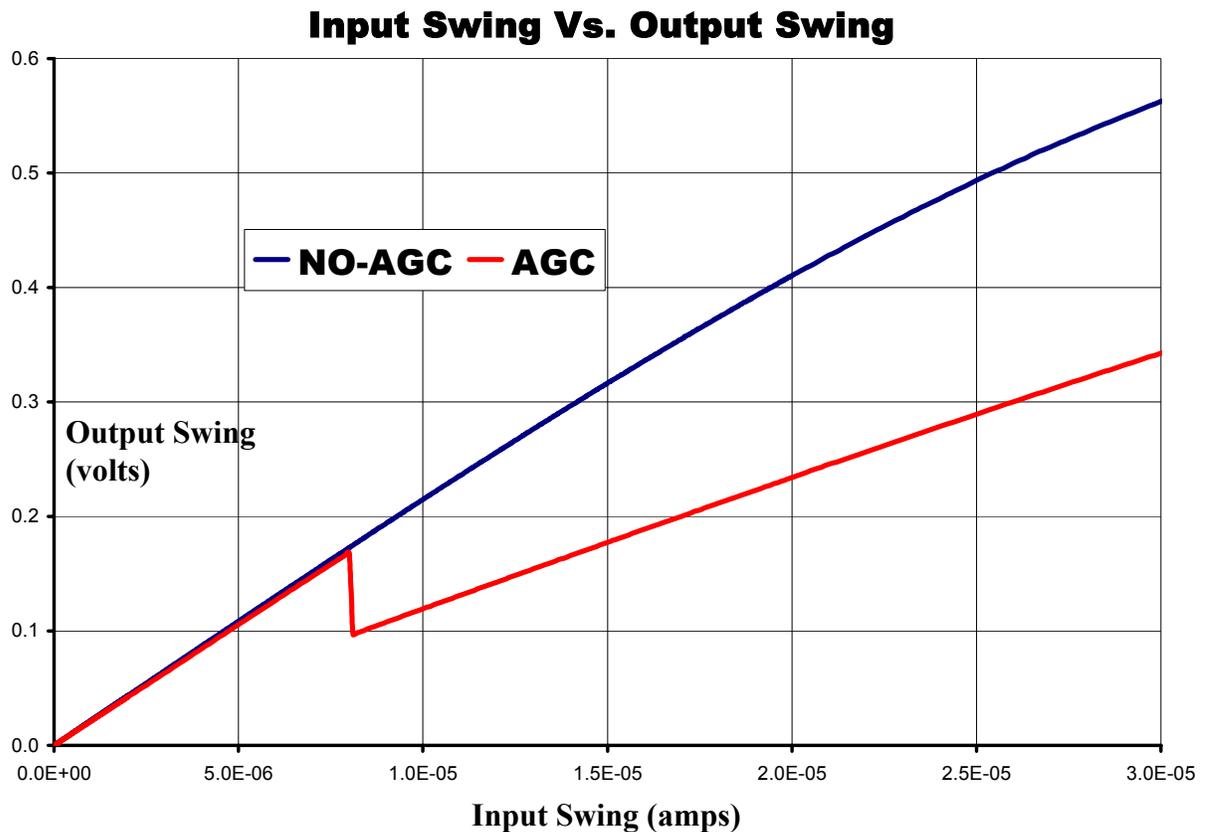


Figure 29 Output voltage swing vs. input current swing with and without the automatic gain control. It can be seen that at the switching point, the output drops off sharply. Because the output of the amplifier does not increase continuously, hysteresis is essential to prevent oscillation around the switching point

The Schmitt Trigger is followed by an inverter since the Schmitt Trigger has an inverting gain and is unable to drive the AGC MOSFET properly for this reason. The inverter also has additional gain and rail-to-rail swing to completely turn the AGC MOSFET on and off. The NMOS and the PMOS both have a W/L ratio of 100 which result in fast

transition speeds. The inverter is the only digital component in this design and thus care was taken during the layout process to isolate this circuit from the analog components. This was achieved through using a double guard ring structure which consists of a substrate contact that is surrounded by an n-well ring. These rings ensure good substrate and n-well coupling to ground and V_{DD} around the noisy circuit which protects the substrate around the analog parts from spikes caused by switching.

As can be seen from Figure 28 and Figure 29, the linearity of the gain increases with the bilinear gain and the amplifier is able to measure signals that are larger in contrast to the case without the automatic gain control. One disadvantage of using the automatic gain control is the increase in noise current when the second resistor is switched in. The RMS noise current from the feedback resistors is multiplied by a factor of $\sqrt{2}$.

11 Current Reference Circuit

Current reference circuits are important components of analog circuits. Single-ended and differential amplifiers use current source loads and differential amplifiers require tail current sources which need a current reference to operate. Current sources are essentially constructed from current mirrors. The most basic current source consists of a current mirror and a resistor to produce the reference current. This topography however is not widely used because of its sensitivity to outside disturbances. In most applications, it is important for the current source to be insensitive to outside effects such as power supply noise so a resistor is a poor choice for a reference current generator. It is essential to study the different types of current sources to gain an understanding of their advantages and disadvantages. Current reference circuits can be analyzed in two categories, temperature independent references and supply independent references. It can be concluded that the resistor based reference is neither of these because the resistor has a temperature coefficient and the current through the resistor changes with the supply voltage. The following circuits are improvements over this current reference.

11.1 Self Biasing (Bootstrapped) Reference

A current references dependence on the supply voltage can be reduced by making the reference current dependent only on the output current. Since the output current is ideally independent of the supply the reference current also becomes independent. This is achieved by connecting two current sources together as shown in Figure 30 which if all the devices are identical, forces the current on both legs to be equal. The reference current is mirrored at the output and the output is mirrored at the reference [25] essentially making the circuit biases itself. If an output current which is a multiple of the reference is desired, the W/L ratios of M2 and M3 must be multiplied by the desired factor. This is only true however when the channel length modulation is not taken into account. For this reason, long channel devices are often used.

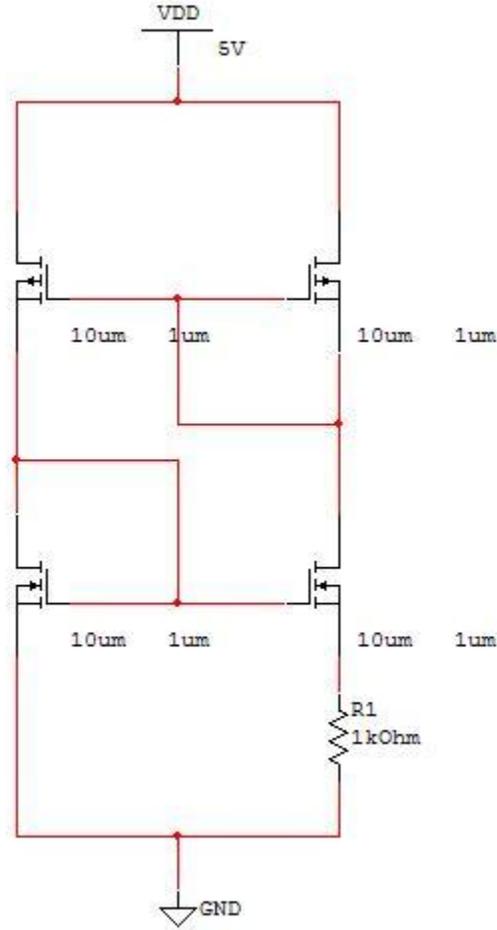


Figure 30 Self-biasing reference

As seen from Figure 30 a resistor is tied to the source of M2. This enables the designer to determine the current from doing a KVL around M1, M2 and R1.

$$\sqrt{\frac{2I_{REF}}{\mu_n C_{OX}(W/L)_1}} + V_{TH1} = \sqrt{\frac{2I_{OUT}}{\mu_n C_{OX}A(W/L)_2}} + V_{TH2} + I_{OUT}R_1 \quad (25)$$

And since $I_{OUT} = I_{REF}$

$$\sqrt{\frac{2I_{OUT}}{\mu_n C_{OX}(W/L)_1}} \left(1 - \frac{1}{\sqrt{A}}\right) = I_{OUT}R_1 \quad (26)$$

Rearranging this equation to bring out I_{OUT} gives

$$I_{OUT} = \frac{2}{\mu_n C_{OX}(W/L)_1} \cdot \frac{1}{R_1^2} \left(1 - \frac{1}{\sqrt{A}}\right)^2 \quad (27)$$

In conclusion the output current does not depend on the supply but still has a dependence on temperature through the electron mobility and the resistor. It also depends on the process because of the dimensional parameters W and L. Like all self biased references, this circuit requires a startup circuit to drive it out of a possible 0 current state [2, 22].

11.2 V_{BE} Referenced Current Source

V_{BE} referenced current sources can be produced by adding a diode connected BJT to the source of M1. In this case, the dimensions of the MOS devices are kept equal. A KVL around the BJT, M1, M2 and the resistor shows the following relationship.

$$\begin{aligned} V_{BE1} + V_{GS1} - V_{GS2} - I_{OUT} R_1 &= 0 \\ V_{GS1} &= V_{GS2} \\ I_{OUT} &= \frac{V_{BE1}}{R_1} \end{aligned} \quad (28)$$

The output current is complementary to absolute temperature because of V_{BE} . This circuit is also supply independent but has temperature has a large negative temperature coefficient [1, 12, 22].

11.3 V_T Referenced Current Source

As opposed to the negative temperature coefficient of the V_{BE} referenced current source, this reference demonstrates a PTAT (proportional to absolute temperature) behavior [1, 12, 22]. This circuit has one additional BJT which is tied between R1 and ground. By forcing the same current to flow through two transistors of different sizes, we get a voltage across R1 which is the difference between the base emitter voltages of the BJTs [1].

$$\begin{aligned} V_{BE1} + V_{GS1} - V_{GS2} - I_{OUT} R_1 - V_{BE2} &= 0 \\ I_{OUT} &= \frac{V_{BE1} - V_{BE2}}{R_1} \\ I_{OUT} &= \frac{V_T \ln\left(\frac{I_C}{I_S}\right) - V_T \ln\left(\frac{I_C}{nI_s}\right)}{R_1} \end{aligned}$$

$$I_{OUT} = \frac{V_T \ln(n)}{R_1} \quad (29)$$

This type of reference circuit displays a smaller dependence on temperature than the V_{BE} referenced source hence it is a more popular reference circuit. The only true temperature independent reference is the band-gap reference which is explained below.

11.4 Band Gap Reference

Band gap references combine the characteristics of a PTAT and CTAT reference circuit and exhibits a true independence from temperature over a narrow range. The resulting reference current is derived from the voltage created using the weighted sum of V_{BE} and V_T . A simple band-gap reference is shown below. In this example the output of the op-amp is equal to:

$$V_{OUT} = V_{BE2} + V_{R3} + V_{R2} \quad (30)$$

Moreover the voltage across R3 is the difference between the base emitter voltages of the two transistors because the op-amp forces its inputs to be at the same potential. The voltage across R3 is:

$$\Delta V_{BE} = V_T \ln \frac{I_1 I_{S1}}{I_2 I_{S2}} = V_T \ln \frac{R_2 I_{S2}}{R_1 I_{S1}} \quad (31)$$

The voltage drop across R1 and R2 must be the same therefore the ratio of the currents I_1 and I_2 must be the same as the ratio of R2 and R1 which explains the above derivation. The voltage across R2 is:

$$V_{R2} = \frac{R_2}{R_3} V_{R3} = \frac{R_2}{R_3} V_T \frac{R_2 I_{S2}}{R_1 I_{S1}} \quad (32)$$

Substituting these voltages to into the first equation results in:

$$V_{OUT} = V_{BE2} + \left(1 + \frac{R_2}{R_3}\right) V_T \ln \frac{R_2 I_{S2}}{R_1 I_{S1}} = V_{BE} + M V_T \quad (33)$$

Which clearly shows the output of the op-amp is a weighted sum of the V_{BE} and V_T hence the circuit is a band-gap reference. The name band-gap is given because the output voltage at which the temperature coefficient is 0 is about 1.26 volts which is approximately the band

gap voltage of silicon. The same circuit can be manufactured in CMOS processes by using PNP BJTs.

The band-gap reference used in this project utilizes the V_T referenced source explained before and has cascoded transistors for better supply rejection. The current generated by this source is passed through a resistor xR and a BJT which has the same area as Q_2 . This generates the band-gap voltage defined as:

$$V_{OUT} = V_{BE} + xV_T \ln(n) \quad [1] \quad (34)$$

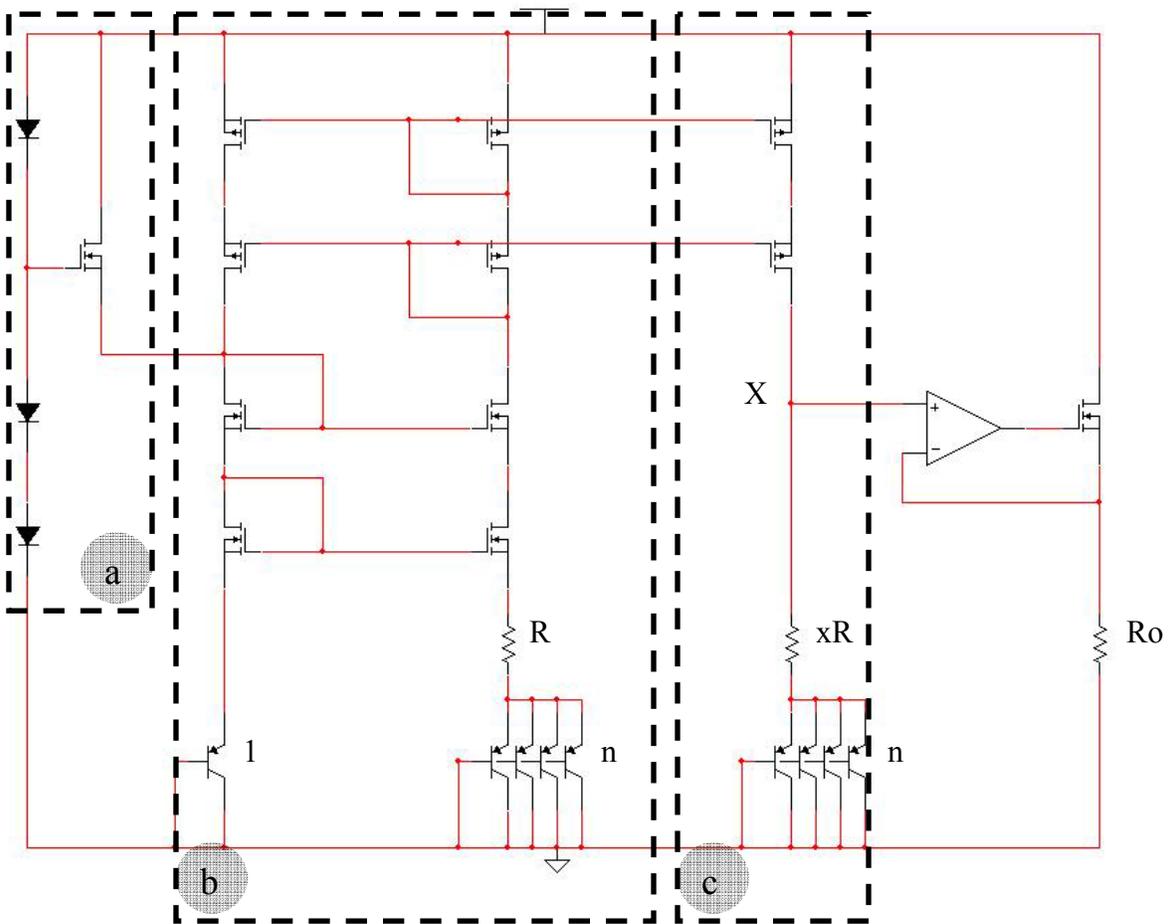


Figure 31 Band-gap current reference; a) Start-up circuit, b) V_T referenced current source providing PTAT temperature dependence, and c) V_{be} referenced current source with a negative temperature coefficient. The voltage at node X combines these temperature dependences [22]

A voltage to current converter/buffer is used to produce a current that is proportional to the band-gap voltage. The magnitude of this current can be set by a single resistor which simplifies the design. In the prototype circuit, this feature along with multiple voltage-to-current converters allows for setting currents for each sub circuit of the system independently and externally.

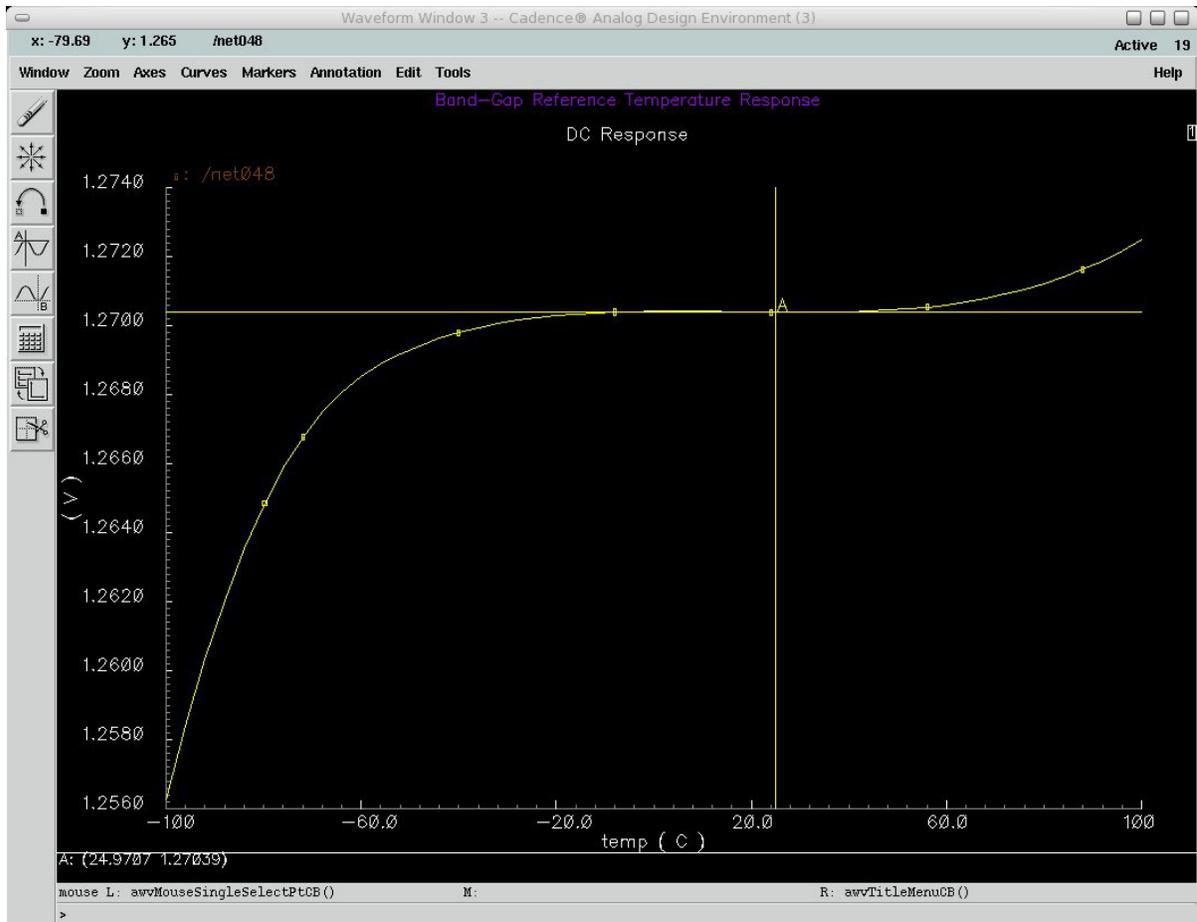


Figure 32 Temperature characteristic of the band-gap reference. Temperature dependence is minimized around 25 degrees Celsius

The band-gap current reference is insensitive to both the supply and temperature (Figure 32). Like all other self biased circuits however it requires a startup circuit to ensure that the circuit is not stuck in a 0 current state. This is achieved by having another current path from V_{DD} to the left leg of the NMOS cascoded devices. The transistor which controls this current is designed to turn off when the reference reaches its target state. Figure 31 is a simplified diagram of the reference with the startup circuit.

The diodes used in the diagram are implemented with MOS devices in the actual design and the voltage at the gate of the startup MOS device is set by the geometry of these devices. It is important for this voltage to be less than or equal to the source voltage of the startup device when the reference is operating to prevent interference of the startup circuit with the operation of the reference circuit. The resistor R_o in Figure 31 is external to allow for current tuning and has to be a “high precision resistor” [22].

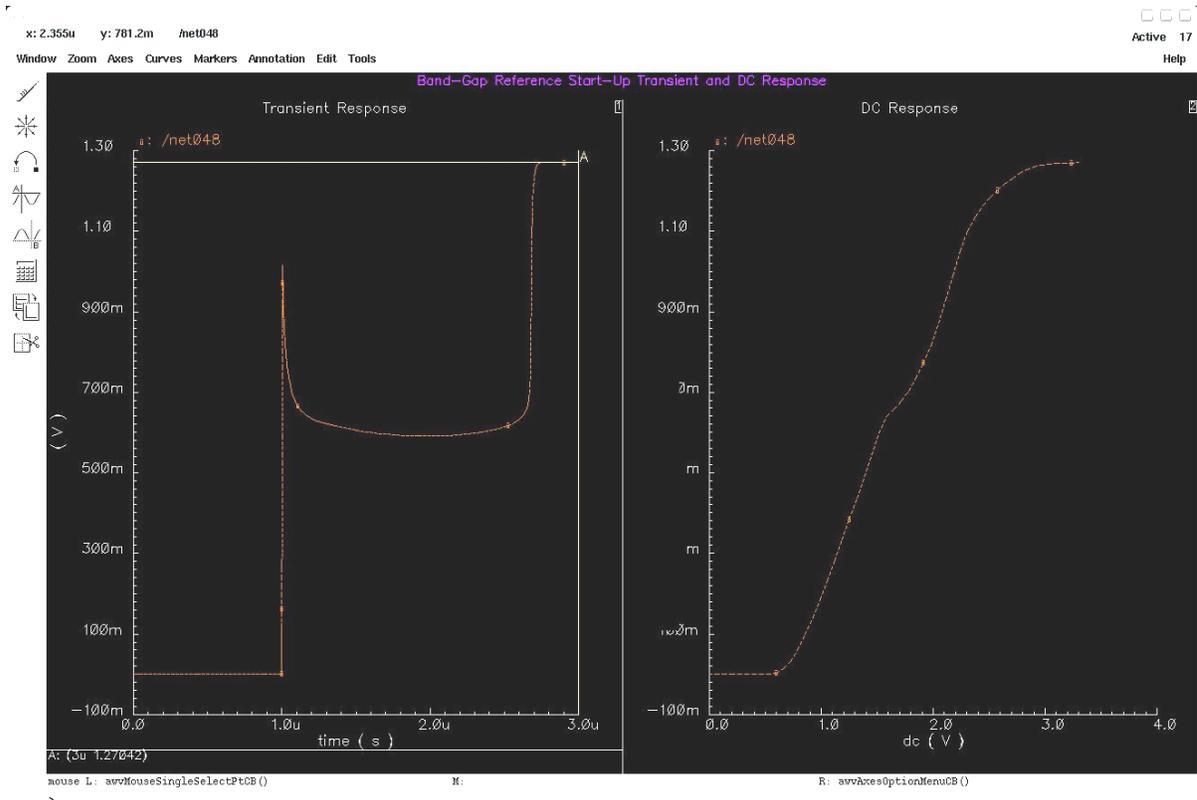


Figure 33 Start-up transient and DC sweep of the band-gap reference

Figure 33 shows the response of the start-up circuit to a power supply step from 0 to 3.3 V. The power is stepped up at $1 \mu\text{s}$ and it takes the band-gap reference to reach its final operating point $1.7 \mu\text{s}$. As can be observed from the second graph, the power supply dependence reduces significantly as the power supply reaches 3 V.

12 Layout Considerations

This section discusses the issues relating to the layout of each of the components of the system. Placement sizing and symmetry of the devices is very important for achieving the desired performance of the circuit. In order to minimize gate resistance and at the same time optimize noise performance, finger structures were used in each device in the design. Also the isolation of digital and analog sub-circuits was achieved through the use of guard ring structures which are also important for noise rejection. This section will explain in detail the important layout issues for each sub-circuit in the design.

12.1 Transimpedance Stage

The layout challenge in this stage is the placement of the large feedback resistors. The 16 k Ω feedback resistor was divided into smaller units that were then connected in series in a folded fashion which saved significant silicon space [2]. In order to reduce the impact of process variations, the devices were laid out symmetrically. As many substrate and n-well connections were utilized as the space permitted.

12.2 Output Buffer

The buffer stage consumes the largest area in the layout and the devices that form the circuit utilize many fingers. It is important in this portion of the layout that the contacts to the gates of the devices are adequate and it is essential that the longer connections between gates are made with metal paths instead of poly because of the lower resistance of metal lines. In addition the higher currents that flow in this portion of the circuit demand that the paths that carry this current be wide enough to prevent voltage drop and electron migration over time. The width required for a particular current is provided by the design rules from TSMC and is calculated at 70 degrees Celsius.

12.3 Inverter

The only digital circuit in this project is the inverter which inverts the signal from the peak detection and automatic gain control stage. Because this is a switching circuit, a double

guard ring structure [2, 21] is used to couple this noise to ground and prevent the substrate around the analog circuits from getting contaminated. A double guard ring is formed by placing a rectangle of substrate contacts around the inverter which is enclosed in a rectangle of n-well contacts. While the substrate contacts make sure that any noise in the substrate around the inverter have a low impedance path to ground, the n-well works as a trench to provide further isolation. The devices in the inverter circuit were made wide to increase transition speeds.

12.4 Current Reference

Being able to accurately reproduce currents from the reference requires careful layout. It is known that in current mirror circuits, the output current is much more sensitive to changes in the gate voltage of the devices than the drain voltage. If the gate voltage of one transistor in the mirror differs from the other, the output current will not be the exact copy of the input whereas the same amount of difference in the drain voltage may not affect the output current significantly, in fact if the output impedance of the mirror transistors are high sensitivity to drain-source voltage is very low. This property presents itself in layouts where the current reference device is far away from the part of the circuit where this current is to be supplied. To be able to reproduce the currents at the target devices accurately, the longest path between these devices must carry current instead of voltage. In other words the current mirroring must be done close to the devices to which the current is supplied. The diagram below further clarifies this issue [2, 21].

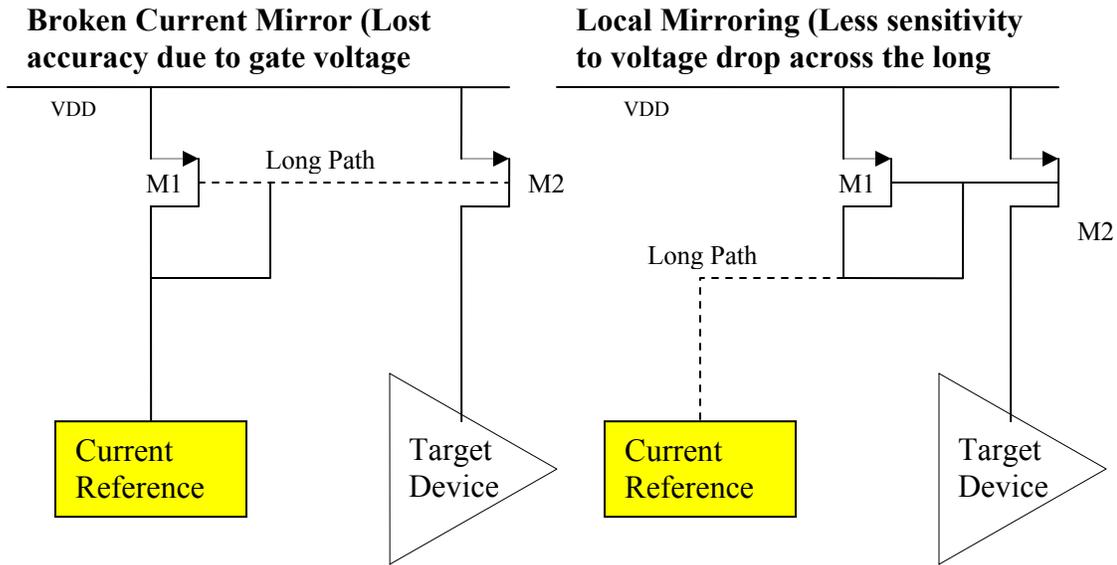


Figure 34 Current distribution in a system. If the target device is far away from the reference, the designer should do the current mirroring locally to avoid voltage drop over long traces.

12.5 ESD Protection

This design also includes custom electro-static-discharge (ESD) protection circuitry. Because of the unavailability of an input/output pad ring with ESD devices for the technology used, it was necessary to design a pad and ESD MOS devices with the design rules supplied from TSMC. The ESD protection devices include an NMOS device which is connected to the path between the signal and ground and likewise a PMOS device is connected between the signal and V_{DD} . These transistors must include sufficient amounts of contacts to the source and the drain of the ESD devices to be able to handle large currents that may be conducted during an ESD spike. The design rules also demand that the drain regions of these transistors are not covered with silicide (which reduces the resistance of these regions) so a resist protect oxide (RPO) mask was created over these regions. In conclusion a full custom pad ring with ESD protection was utilized in this project.

12.6 Traces

Traces on the chip were designed to carry their respective currents at a core temperature of 70 degrees Celsius. The widths were calculated using the TSMC design rules manual. Correct specification of the widths of the traces prevents open circuits in the long

term due to electron migration. Electron migration is caused by excess number of charges displacing the electrons in the metal trace. It was also important to keep the long traces that carry the reference voltages wide enough to minimize resistance and prevent voltage drop from the pad to the core circuit. Furthermore, traces that are connected to the pads are tapered rather than having an abrupt junction in order to assist in smooth flow of electrons.

TSMC required a power ring be utilized around the core circuit. The power ring uses all metal layers connected together with vias that are separated according to the design rules supplied by TSMC. The power ring is actually two rings, one carrying the VCC and the other GND (Figure 45).

13 Simulation Results

This section summarizes the results obtained from the various simulations done in the Cadence design environment and Orcad Pspice. System properties in the presence of package and layout parasitics are shown in sections 13.1 and 13.2, and section 13.3 presents the properties of the common mode feedback loop and the DC current cancellation loop.

13.1 System Performance

These results show the outputs of the simulations done in the Cadence environment and Orcad Pspice. The differences in the results are due to the accuracy of the device models used in the two simulations. Models provided from MOSIS for Cadence are more complete than the Orcad Pspice models therefore Cadence results should be treated as being closer to a real world outcome.

	ORCAD	CADENCE
Ideal Gain (dB)	87.08	87.87
Layout Gain (dB)	N/A	89.94
Ideal Bandwidth (MHz)	214.759	164.687
Layout Bandwidth (MHz)	N/A	129.225
Low Freq. Cutoff Point at 50uA DC current (MHz)	3.633	5.248
Input RMS Noise Current at 500uA DC current (pA/Hz ^{1/2})	3.197	4.834
Output Swing (V)	0.6	0.6

Table 4 Comparison of simulation results

13.2 Package Parasitics

The following tables show the results of simulations that were used to determine the possible effects of package parasitics on the performance of the transimpedance amplifier.

EFFECT OF PACKAGE PARASITICS

Pad Capacitance = 100fF (Calculated using approximations described in [2])

Bond Wire L (nH)	GAIN (dB)	Bandwidth (MHz)	Resonance Freq. (GHz)
1	87.696	213.672	>10
6	87.734	215.318	4.9
11	87.769	216.777	3.6
16	87.800	217.980	3.0
21	87.829	218.941	2.6

Bond Wire Inductance = 4nH

Pad Capacitance (fF)	GAIN (dB)	Bandwidth (MHz)	Resonance Freq. (GHz)
100	87.719	214.680	5.9
250	87.772	184.120	4.2
400	89.963	157.397	3.5
550	91.139	137.771	3.1
700	91.890	122.909	2.7
850	91.642	111.208	2.5
1000	90.311	101.757	2.4

Table 5 Combined effect of parasitic bonding pad capacitances and bond wire inductances on system performance

It can be seen from the simulation results that the bond wire inductance has very little effect on the pass-band response of the amplifier however resonance occurs in higher frequencies. There is slight gain and bandwidth increase with increasing bond-wire inductance. The second part of the table shows the results where the bond wire inductance is held constant and the pad capacitance is increased. The effect of the increase in capacitance is more dramatic and results in a drop in the bandwidth of the system. Gain is slightly increased due to peaking in the pass-band frequency. Since it has been shown that the capacitance at the input of the TIA is forms the dominant pole with the input impedance of the amplifier it is necessary to sweep just this capacitance to find its contribution to the overall result. The table below shows the results from this simulation.

EFFECT OF PARASITIC INPUT CAPACITANCE

Pad Capacitance = 100fF

(Calculated using approximations described in [2])

Bond Wire Inductance = 4nH

Input Pad Capacitance (fF)	GAIN (dB)	Bandwidth (MHz)	Resonance Freq. (GHz)
100	87.719	214.680	5.9
250	87.634	201.519	4.7
400	87.516	189.367	4.2
550	87.369	178.159	3.9
700	87.196	167.775	3.7
850	87.000	158.286	3.6
1000	86.784	149.565	3.4

Table 6 Effect of the isolated parasitic input pad capacitance on the frequency response

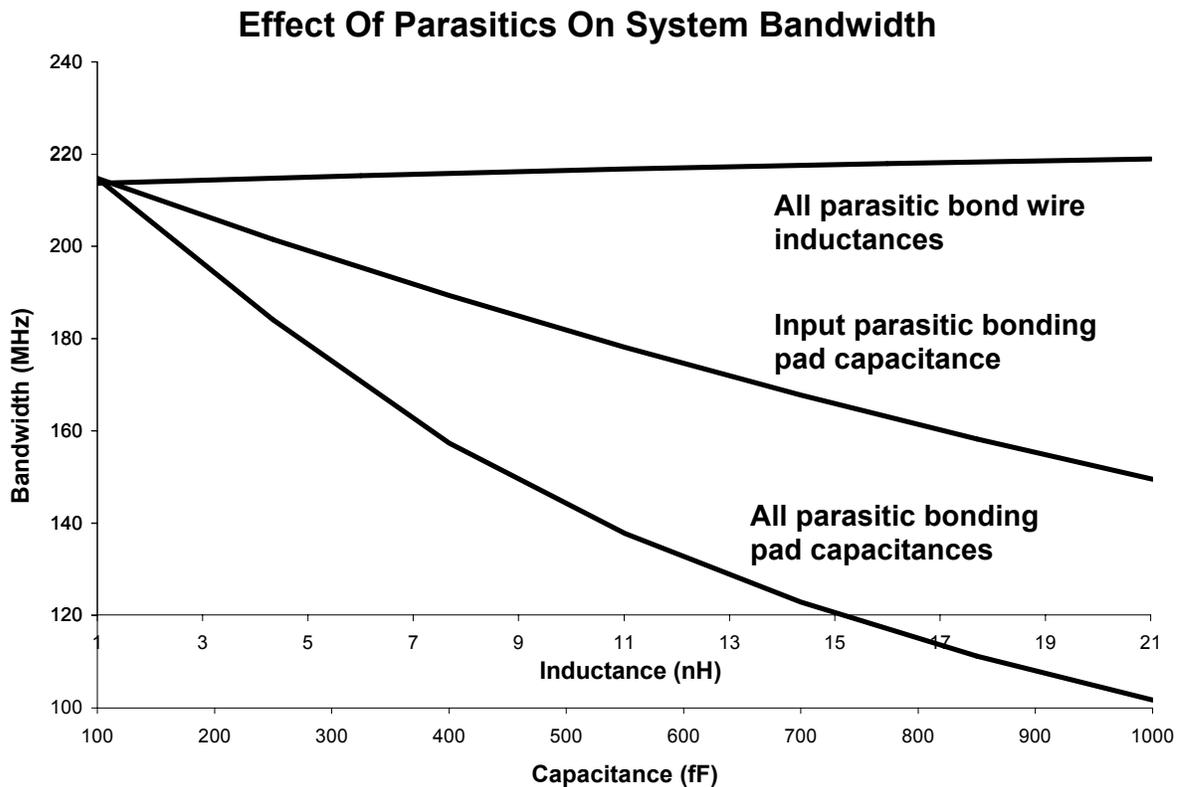


Figure 35 Bandwidth vs. all bonding pad parasitic capacitances, all bond wire parasitic inductances and input bonding pad parasitic capacitance

Table 7 and Figure 36 show the effect of increasing the photodiode parasitic capacitance on the gain and bandwidth of the system. As seen in the plot, increasing capacitance significantly reduces the bandwidth. Results are obtained from the Cadence Spectre simulator and encompass all the package and layout parasitics.

EFFECT OF PARASITIC PHOTODIODE CAPACITANCE

Photodiode Capacitance (pF)	GAIN (dB)	Bandwidth (MHz)
1	89.400	126.000
2	88.270	104.300
3	82.060	93.090
4	78.140	84.810
5	75.400	78.850

Table 7 Effect of parasitic photodiode capacitance on the realistic system

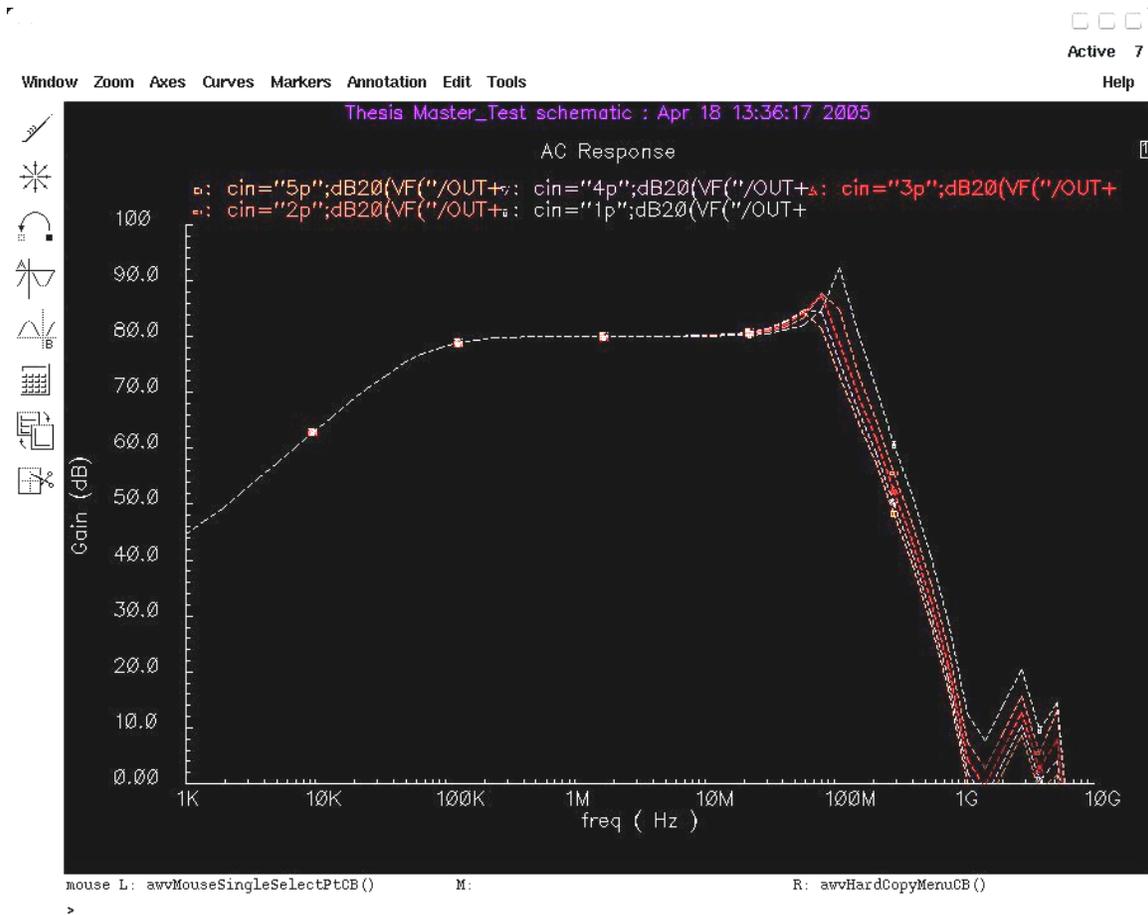


Figure 36 Effect of parasitic photodiode capacitance on the realistic system

It can be concluded from these results that the input parasitic capacitance is a large contributor to the degradation of the system bandwidth and the capacitance of the photodiode is a significant part of the total parasitic capacitance. It can also be concluded that the inductance of the bond wires actually help increase the bandwidth if the parasitic capacitances are low and no peaking occurs in the pass-band. Figure 35 is a plot of the cumulative results from this simulation.

13.3 DC Current Cancellation Loop and CMFB Loop

Settling Time Values

Feedack Loop	Input DC Current (μA)	Settling Time (s)
DCCC	0-50	2.76 μ
	50-100	1.81 μ
	100-150	1.55 μ
	150-200	1.43 μ
	200-250	1.38 μ
	250-300	1.37 μ
	300-350	1.40 μ
	350-400	1.47 μ
CMFB	N/A	41.46n

Table 8 Step response settling time values for the DCCC and CMFB loops

Table 8 contains the settling time values for the DC current cancellation loop and the common mode feedback loop. Note that the settling times for the DCCC loop change with the amount of DC current sunk by the DC cancellation MOSFET. This behavior is previously discussed in Chapter 8. Highest settling time is obtained at the transition between 250 and 300 μA .

14 Conclusions

This project was completed with all design goals completed and exceeded. The design was done and simulated on two different simulation programs for the sake of precision. In the end, results obtained from Cadence Virtuoso (Spectre simulator) and Orcad Pspice were observed to be close. Simulations done on the extracted schematic with the parasitic capacitances from the layout showed a slight decrease in bandwidth as expected largely due to the increased capacitance at the input of the TIA but the results were still over the 100 MHz target.

Two differential TIA schemes were considered which included a system with two feedback loops from the two outputs and another system with only one feedback loop from the inverting output to the input. It was seen in simulations that the dual feedback achieved the same gain as the single feedback system only if the feedback resistor was doubled in value. This however decreased the bandwidth to unacceptable levels. Although the noise performance of the dual feedback system was superior due to the increased feedback resistor value, the bandwidth specification was not fulfilled. The single feedback system achieved a gain of 90 dB with a feedback resistor of 16 k Ω (the additional gain was provided by the output buffer) with a bandwidth of 129 MHz. This result fulfills the gain specification of more than 15 k Ω and bandwidth more than 100 MHz.

Simulations focused on the input capacitance of the TIA showed that the parasitic capacitance of the photodiode is a significant portion of the total input parasitic capacitance. The results obtained from the Spectre simulations run on the realistic system (with all parasitics from the layout and package included) indicate that bandwidth falls sharply with increasing capacitance and falls below the specified 100 MHz target when the photodiode capacitance exceeds 2 pF. It is therefore very important that low capacitance diodes are used in this application. One way to lower the capacitance of a photodiode is to increase the reverse bias therefore if higher voltages than 3.3 V is available in a system, the photodiode cathode must be connected to the highest power supply. Furthermore, the anode of the photodiode must be placed close to the input pin of the TIA to minimize trace parasitics.

The DC current cancellation scheme used in this design does not allow the photodiode to be connected to a negative power supply which may be available on some systems because the DC current cancellation scheme uses a MOSFET that is only able to sink current from the photodiode. One design change that was not in the scope of this project may be the use of a second MOSFET that is controlled by the same error amplifier.

The noise performance of the amplifier was decent with an input referred RMS noise current of $4.834 \text{ pA/Hz}^{1/2}$. This result was obtained in the Cadence Spectre simulation which used the most accurate spice models for the TSMC 0.18 μm process. The parasitic resistances and capacitances were also included in the simulation. Orcad Pspice results which used a less accurate model reported a result of $3.197 \text{ pA/Hz}^{1/2}$ which was closer to the hand calculations which focused on the most dominant noise sources in the design including the core amplifier, the feedback resistor and the DC current cancellation MOSFET device. These devices referred the noise directly to the input while other elements of the system referred the noise through the TIA which has a large gain.

The operation of the DC cancellation circuit was demonstrated in simulations up to 500 μA of DC current which was the specified limit. Slight steady state error was observed at the outputs due to the low open loop gain of the error amplifier. A more sophisticated op-amp with a high open loop gain should provide a lower steady state error. Step response times of the DC cancellation were reasonably fast with the slowest response of 2.76 μs from 0 to 50 μA DC current. The gain of the DC cancellation loop was observed to be dependent on the amount of DC current passing through the DC cancellation MOSFET since the transconductance of the MOSFET was part of the loop gain. The transconductance of a MOSFET increases with increasing DC bias current. This causes the gain associated with the MOSFET to increase. However another factor in the total loop gain was the gain of the error amplifier which was not linear due to the fact that the error amplifier was operated in the open loop configuration. The overall gain of the DC cancellation loop which includes the transconductance of the MOSFET and the gain of the error amplifier was observed to be the highest when the DC current was around 300 μA as seen in Figure 21 (DC cancellation loop step response) where the fastest response time reflects the highest loop gain.

The common mode feedback circuit was stable in all simulations and demonstrated successful operation although the frequency responses of the two outputs were not identical. Open loop step response of the outputs to a common mode disturbance showed different settling behavior on the two legs however, the closed loop step response was symmetric on both legs. Closed loop settling time was found to be 41.46 ns.

The final layout of the circuit was done in the TSMC 0.18 μm process according to the latest device models obtained from MOSIS, however a suitable pad ring was not supplied from MOSIS for this particular process. This required a custom design and thus a pad ring was constructed that complied with the design rules supplied from TSMC. ESD protection devices were also custom designed using the supplied design rules however the effectiveness of the ESD devices was not proven due to cancellation of the testing phase.

Due to scheduling issues with TSMC the design did not go into fabrication which resulted in the testing part of the thesis to be postponed, therefore the effects of circuit board layout on performance remains unknown, however simulations were performed on the extracted circuit from the layout which included the parasitic resistances and capacitances. The effects of bond-wire inductance was also investigated and slight increase in bandwidth for a range of inductance values was observed. Future work can be done in the future to investigate these issues on a test bench.

In conclusion this thesis successfully demonstrated the design of a high gain differential transimpedance amplifier with a DC current cancellation circuit that is able to sink up to 700 μA of DC current. The bilinear gain curve demonstrated increased linearity over a wider range of input power which resulted in increased dynamic range. The design utilized the TSMC 0.18 μm Mixed-Signal CMOS process and was laid out using the Cadence Virtuoso Design Suite. Two simulation platforms were used and the results that were obtained from these simulations were consistent.

APPENDICES

Appendix 1	Cadence Schematics
Appendix 2	Cadence Layouts

APPENDIX 1

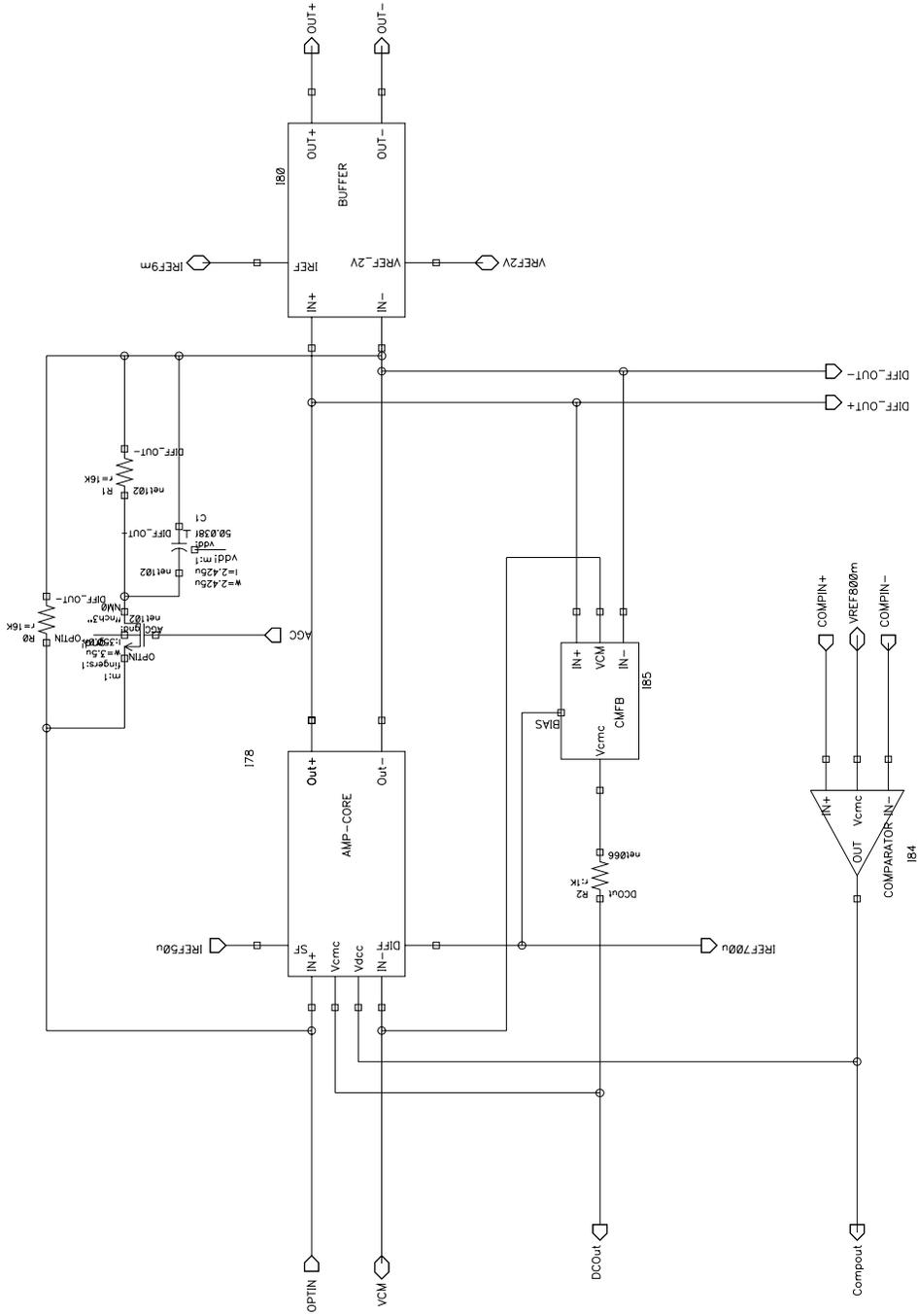


Figure 37 System schematic

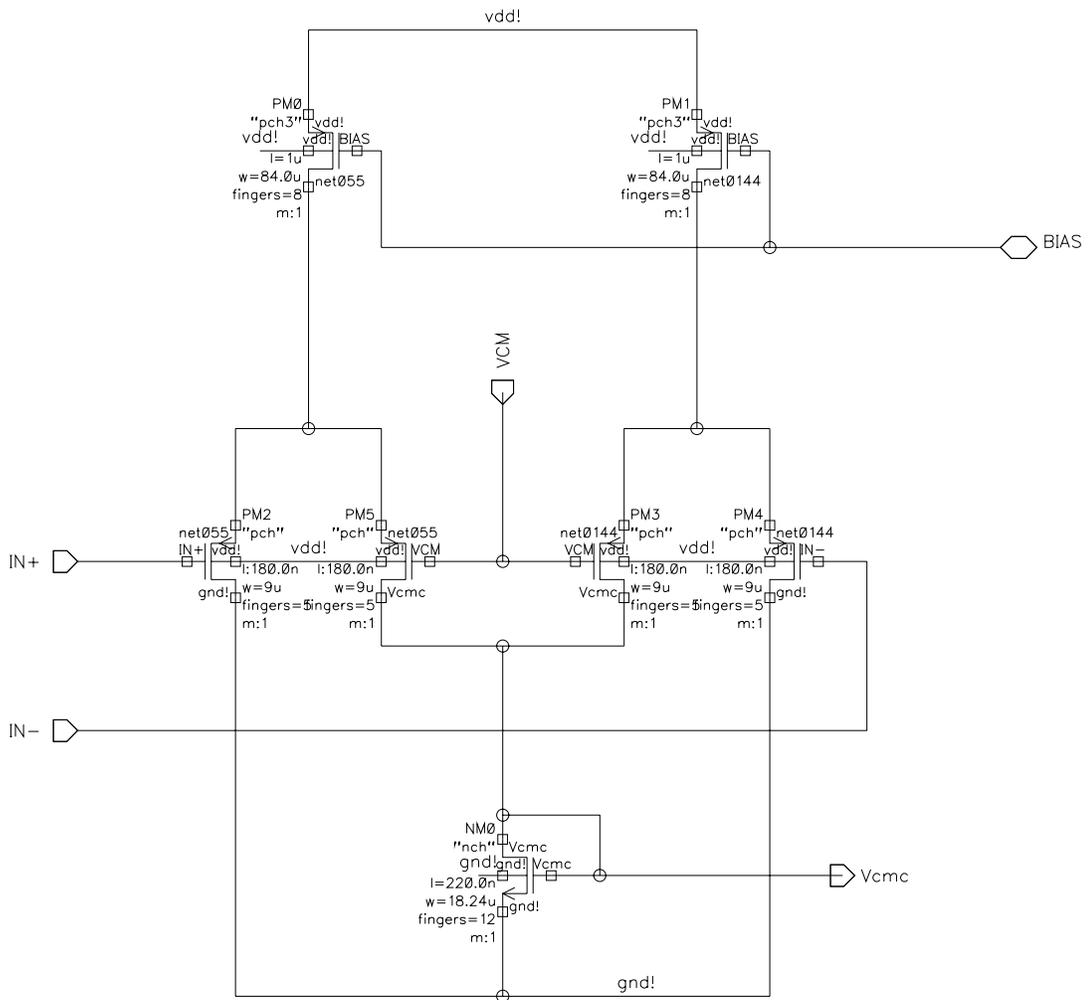


Figure 39 Common mode feedback stage

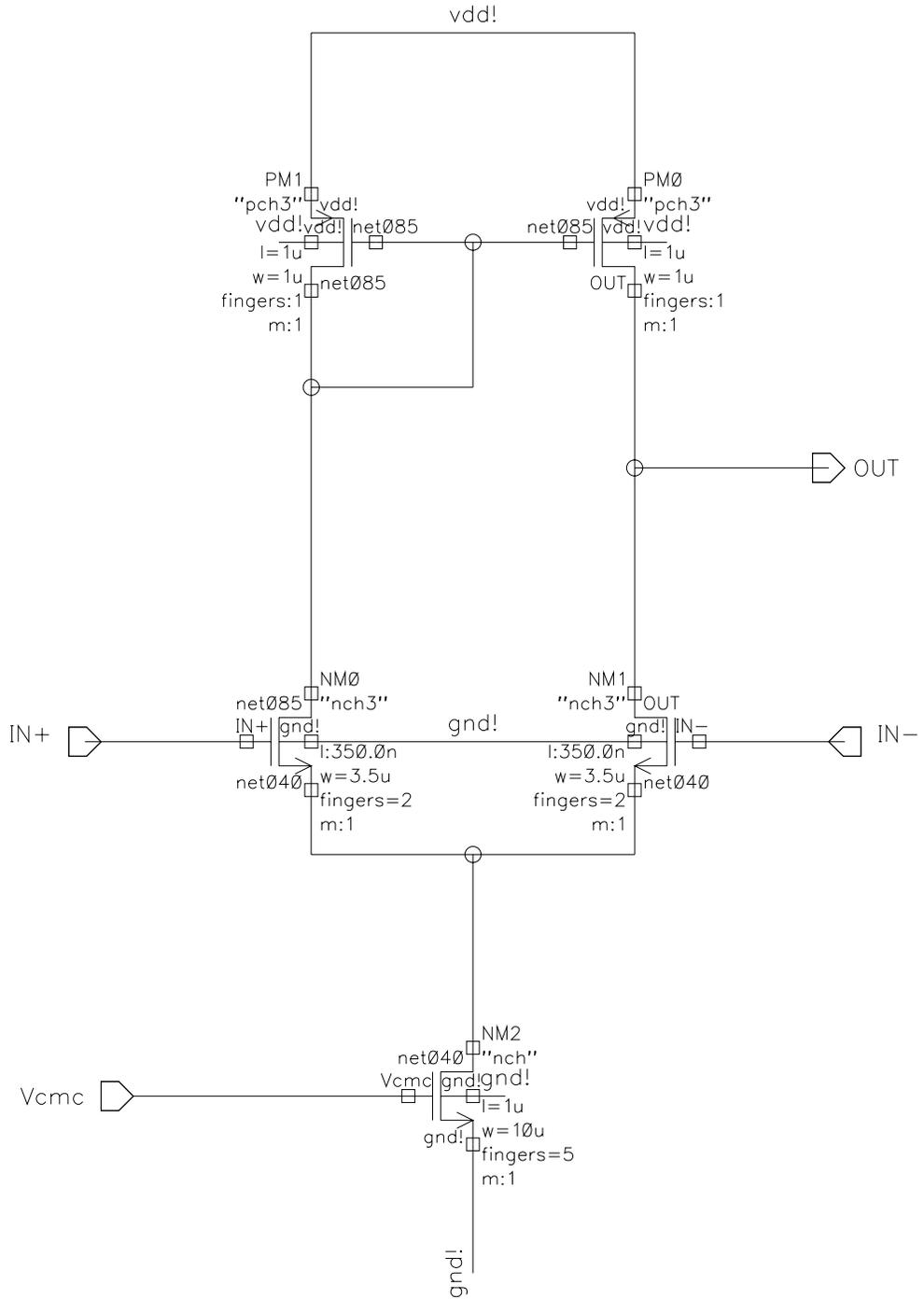


Figure 40 DC cancellation circuit (Error amplifier)

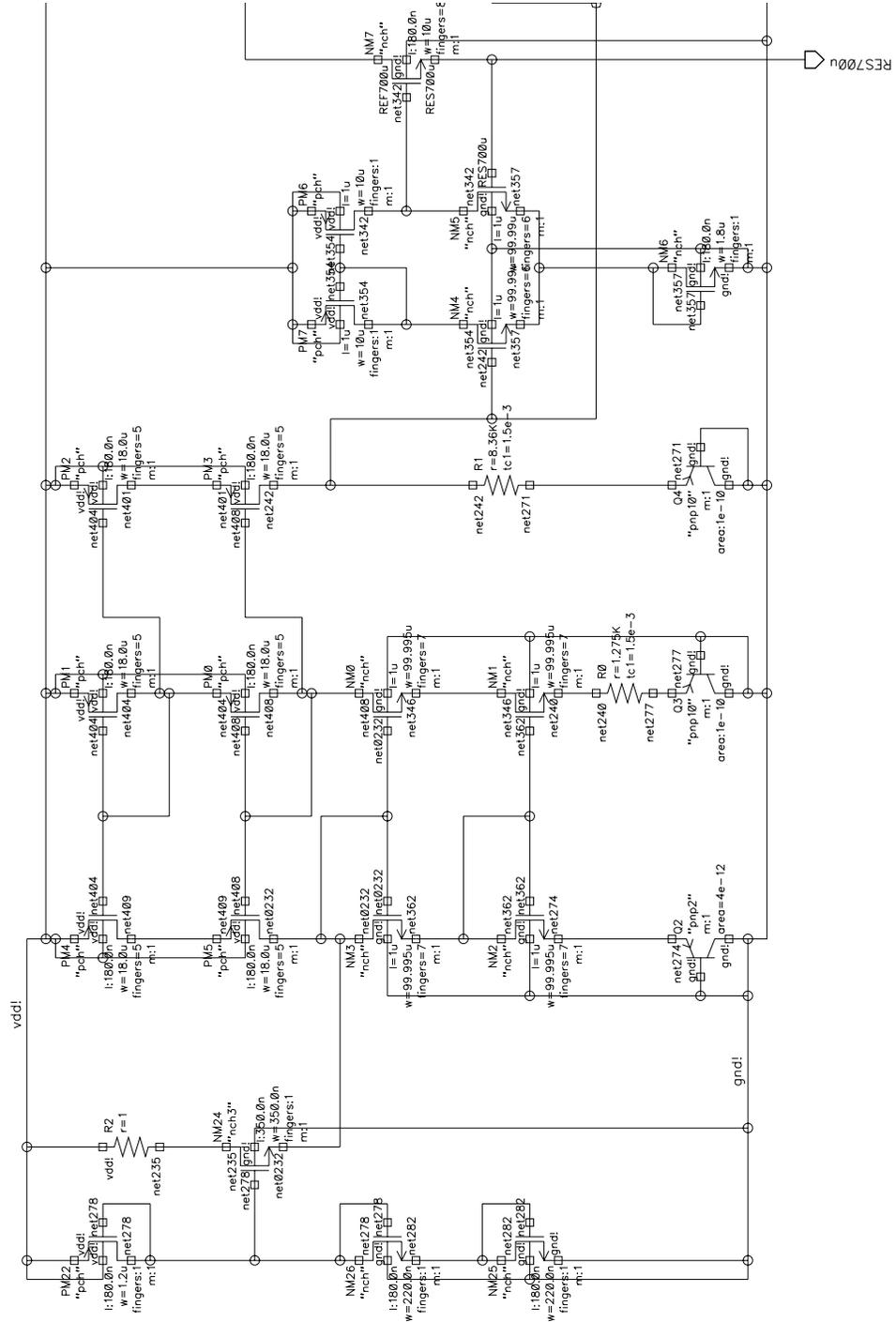


Figure 42 Band-Gap current reference

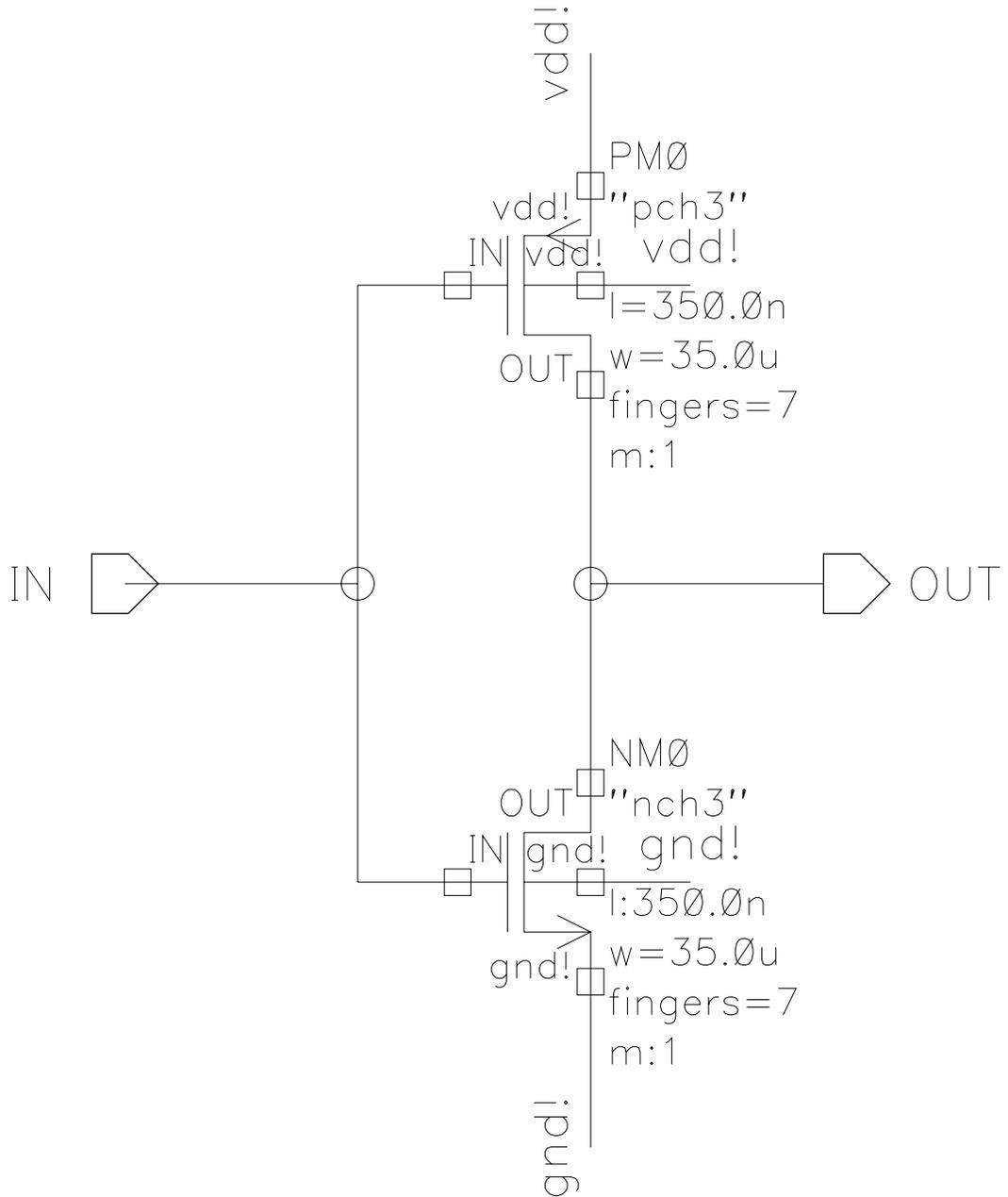


Figure 43 Inverter

APPENDIX 2

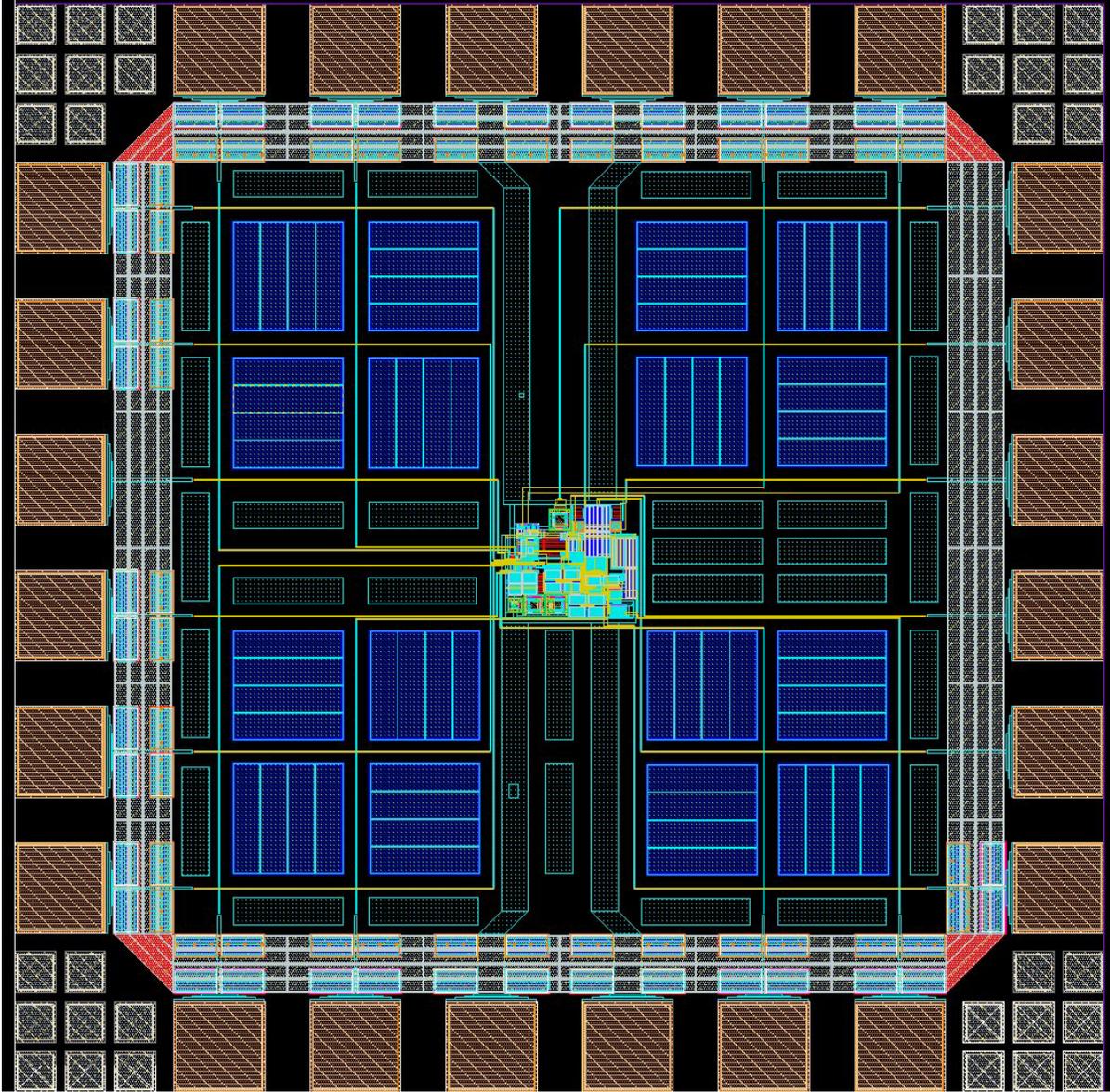


Figure 45 TIA chip

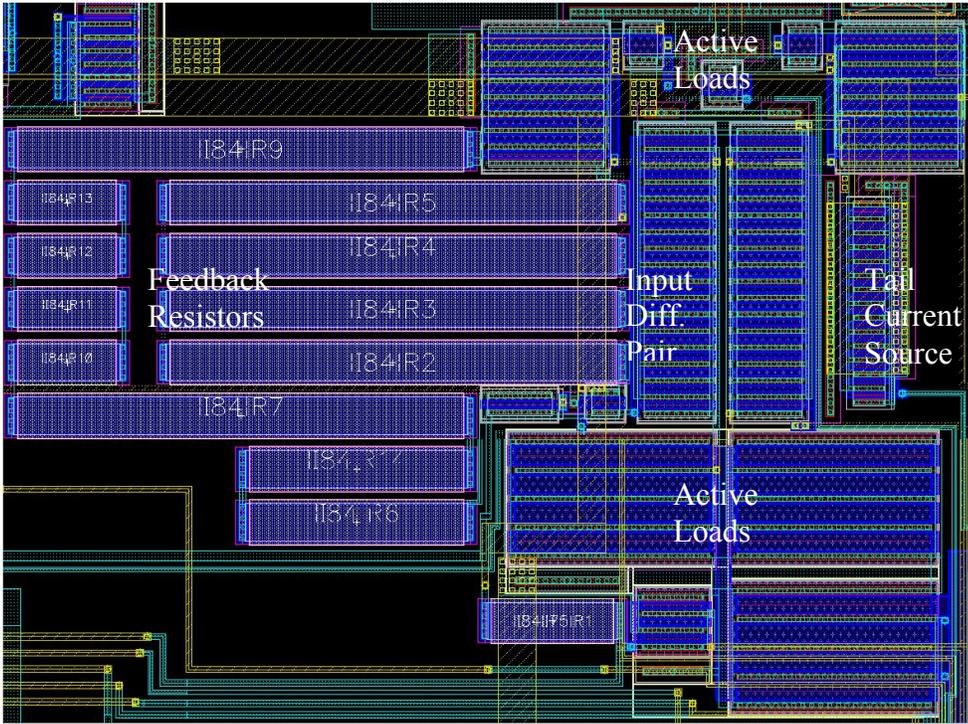


Figure 46 Transimpedance stage

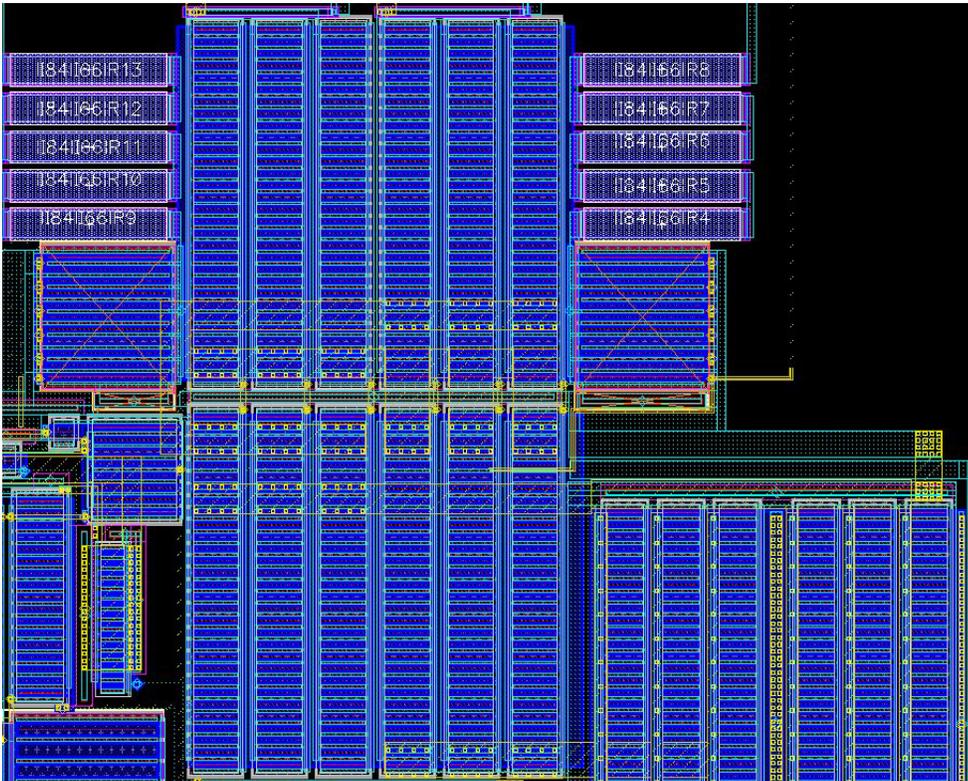


Figure 47 Output buffer stage

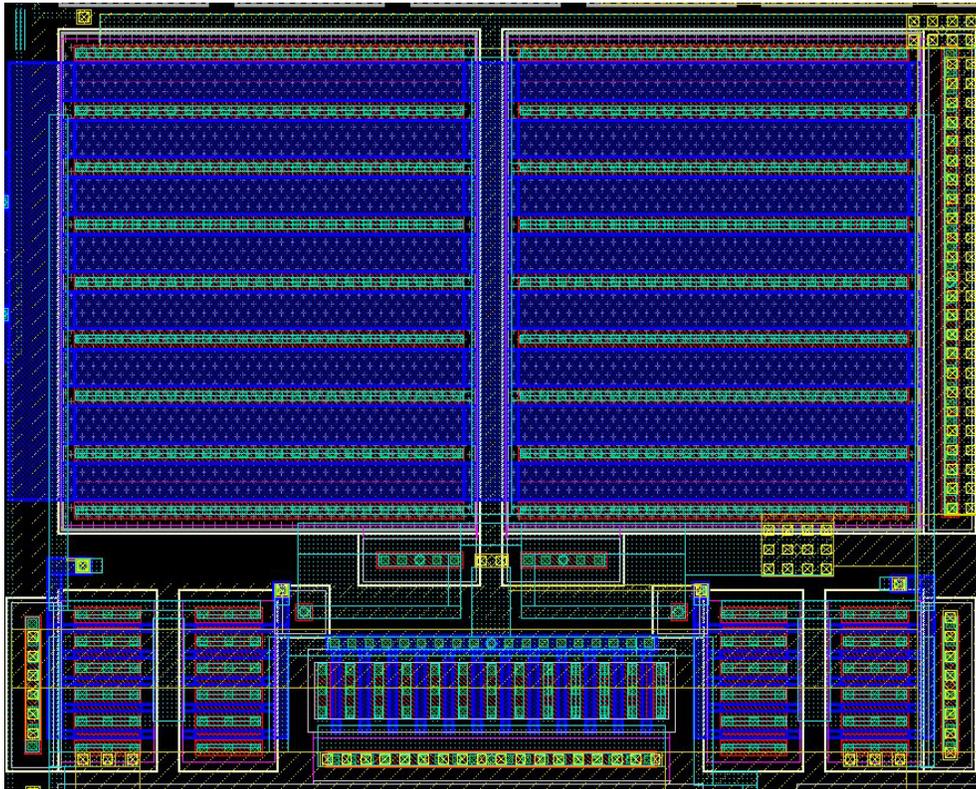


Figure 48 Common mode feedback stage

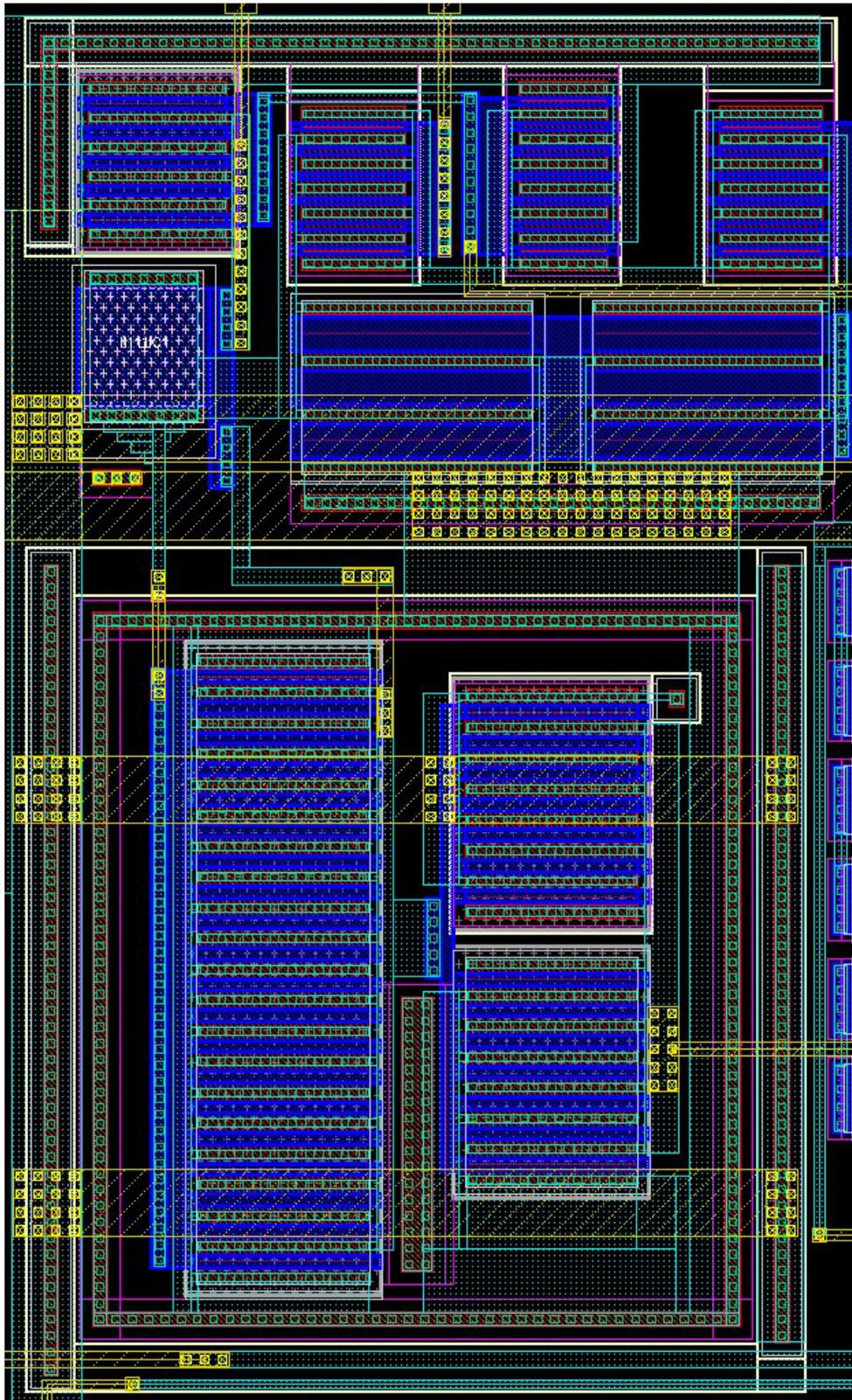


Figure 49 Schmitt trigger

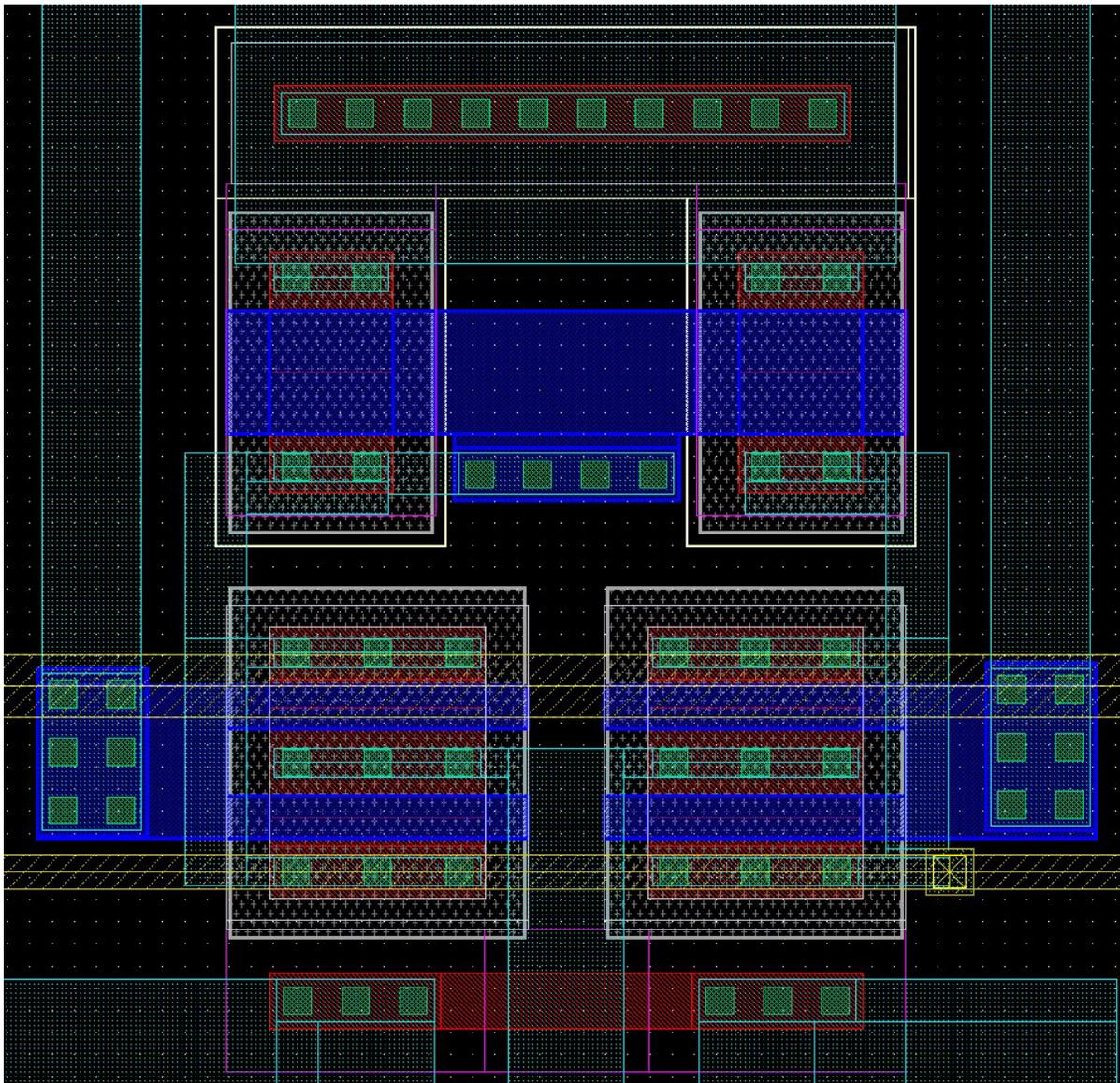


Figure 50 Error amplifier

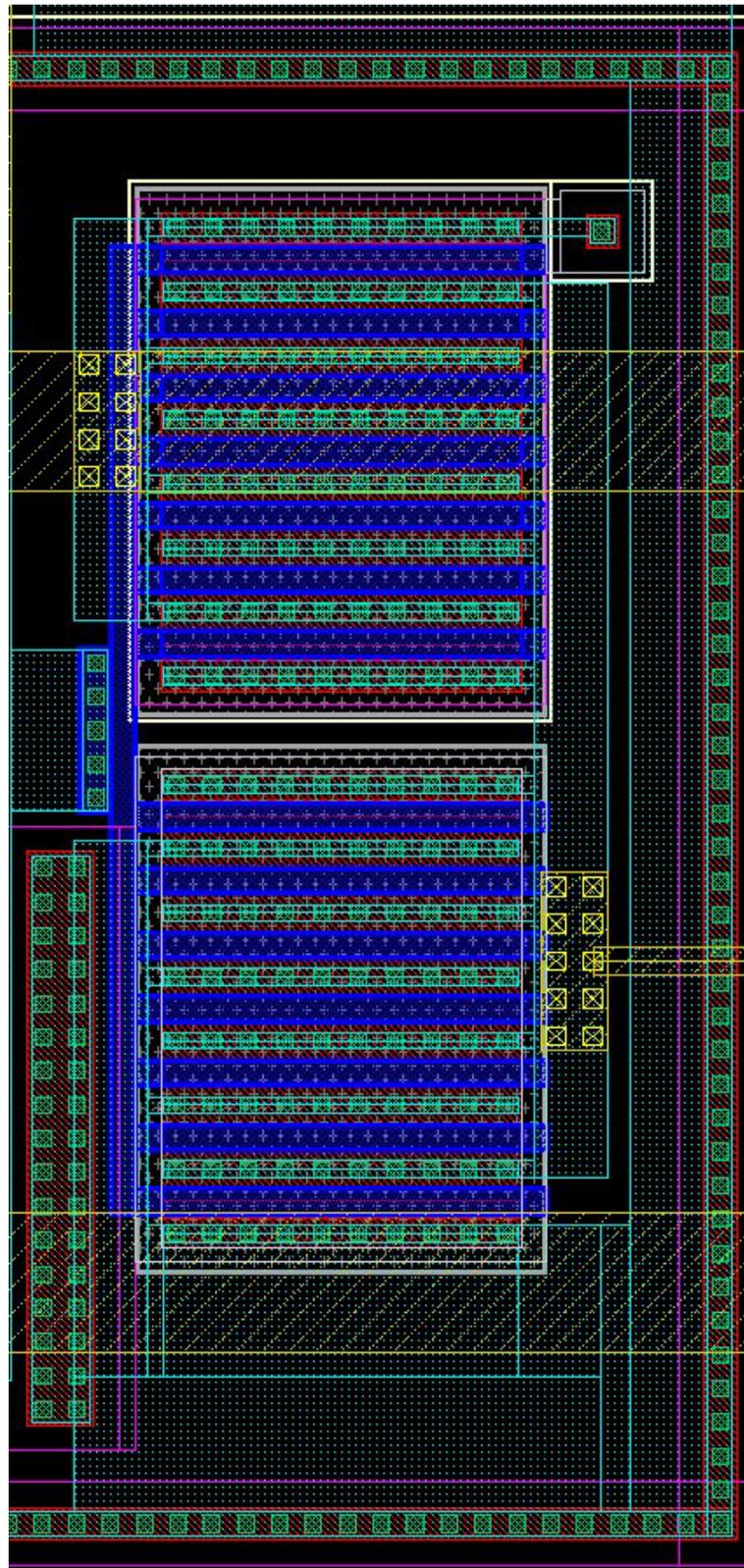


Figure 51 Inverter

Literature Review

This section gives the summaries of the most significant pieces of literature used as references in this thesis. The literature are listed by their subjects relating to the various design issues in this project.

DC Photodiode Current Rejection

Khoman Phang, David A. Johns, "A CMOS Optical Preamplifier for Wireless Infrared Communications," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, vol. 46, no. 7, July 1999.

The design and operation of an "ambient photocurrent rejection" is described in this article. The DC rejection scheme employed by Phang and Johns is the basis of the DC rejection circuit in this thesis. The authors make use of an error amplifier to measure the DC level differences of the transimpedance amplifier's outputs and drive the gate voltage of a MOSFET. The MOSFET is utilized as a current sink that prevents the DC component of the photocurrent from entering the TIA. Besides DC photocurrent rejection, advantages of using a differential structure for the transimpedance amplifier are discussed.

CMOS Design Techniques

B. Razavi, Design of Integrated Circuits for Optical Communications, First Edition, McGraw-Hill, 2003.

This book deals extensively with optical amplifier design including transimpedance amplifiers. Different types of optical amplifiers are presented in the text and their advantages and disadvantages are discussed. Single-ended and differential transimpedance amplifiers are evaluated on the basis of gain, bandwidth and noise current. Razavi describes all aspects of transimpedance amplifier design from the preamplifier to the output buffer with emphasis on the CMOS process.

B. Razavi, Design of Analog CMOS Integrated Circuits, International Edition, McGraw-Hill, 2001.

Both the design and layout of CMOS circuits is covered in this textbook. The section on current references explains the generation of PTAT and negative temperature coefficients as well as V_T and V_{BE} referenced current sources and band-gap current generation. The band-gap current reference described in this textbook utilizing cascoding was used in this project for its stability and supply rejection. Analog circuit layout techniques are explained in the last chapter which include guard rings, symmetry and finger structures which were used during the layout phase of this project.

Common Mode Feedback Circuits

H. Maarefi, A. Parsa, H. Hatamkhani, D. Shiri, "A Wide Swing 1.5V Fully Differential Op-Amp Using a Rail-to-rail Analog CMFB Circuit."

Various types of common mode feedback circuits for operational amplifiers are presented and compared in this article. The authors introduce a novel differential design that has the advantage of operating with high voltage swings. This scheme was considered for this project but rejected in favor of the differential scheme with diode connected bias setting devices that is also shown in the article. This version does not have the large swing tolerance which is not required by the amplifier in this project and it does not utilize polysilicon resistors that take up more silicon space.

Bilinear Gain Concept

M. J. Hayes, "A Nonlinear Optical Preamplifier for Sensing Applications," IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, vol. 49, No. 1, January 2002.

Hayes describes a bilinear amplifier design that serves to increase the dynamic range of the transimpedance amplifier. The proposed system senses the voltage at the output and compares this voltage with a reference. When the output voltage exceeds the reference voltage, a second feedback path that utilizes an additional feedback resistor is switched on resulting in a change in the gain profile. The amplifier provides two outputs with the total output voltage of the system being the weighted sum of these two outputs. The author states that both output voltages increase with increasing current making hysteresis unnecessary.

Although the circuit presented here is stable, the differential architecture of the transimpedance amplifier used in this project demanded another solution and a switching MOSFET was used to change the gain profile along with a hysteresis amplifier to sense the output levels. Instead of being summed with a reference as explained in the article, the output voltage in this project is sensed by a Schmitt trigger and the gain profile switches at a determined point that is externally adjustable.

Bibliography

- [1] P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, Analysis and Design of Analog Integrated Circuits, Fourth Edition, John Wiley and Sons, 2001.
- [2] B. Razavi, Design of Analog CMOS Integrated Circuits, International Edition, McGraw-Hill, 2001.
- [3] B. Razavi, Design of Integrated Circuits for Optical Communications, First Edition, McGraw-Hill, 2003.
- [4] A. S. Sedra, K. C. Smith, Microelectronic Circuits, Fifth Edition, Oxford University Press, 2004.
- [5] J. Gowar, Optical Communication Systems, Prentice-Hall International, 1984.
- [6] G. P. Agrawal, Fiber-optic Communication Systems, Second Edition, Wiley, 1997.
- [7] K. Phang, D. A. Johns, "A CMOS Optical Preamplifier for Wireless Infrared Communications," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, vol. 46, no. 7, July 1999.
- [8] R. G. Swartz, Y. Ota, M. J. Tarsia, V. D. Archer, "A Burst Mode, Packet Receiver with Precision Reset and Automatic Dark Level Compensation for Optical Bus Communications," AT and T Bell Laboratories Holmdel, New Jersey, 07733 USA.
- [9] L. Luh, J. Choma, Jr., J. Draper, "A Continuous-Time Common Mode Feedback Circuit (CMFB) for High-Impedance Current Mode Application"
- [10] Y. H. Chee, C. Tsang, EECS 240 Final Project, Spring 2002.
- [11] H. Maarefi, A. Parsa, H. Hatamkhani, D. Shiri, "A Wide Swing 1.5V Fully Differential Op-Amp Using a Rail-to-rail Analog CMFB Circuit," Kavosh Asia Corp.
- [12] Anonymous, Class Notes, EE 532 – Analog IC Design II, Spring 2002.
- [13] T. H. Lee, The Design of Radio-Frequency Integrated Circuits, Second Edition, Cambridge University Press, 2004.
- [14] C. R. Calvo, "A 2.5 GHz Optoelectronic Amplifier in 0.18 μ m CMOS", Thesis, Worcester Polytechnic Institute, May 2003.

- [15] R. Tao, M. Berroth, "A 10 Gb/s Fully Differential CMOS Transimpedance Preamplifier," Institute of Electrical and Optical Communication Engineering, University of Stuttgart.
- [16] B. Razavi, "Design of High-Speed Circuits for Optical Communication Systems," IEEE Custom Integrated Circuits Conference, 2001.
- [17] S. Mohan, T. Lee, "A 2.125 GBaud 1.6k Ω Transimpedance Preamplifier in 0.5 μ m CMOS," CICC, May1999.
- [18] S. Mohan, M. Hershenson, S. Boyd, T. Lee, "Bandwidth Extension in CMOS with Optimized On-Chip Inductors," IEEE Journal in Solid-State Circuits, vol. 35, no. 3, March 2000.
- [19] S. H. Park, D. Y. Jung, C. S. Park, "Bandwidth Extension in Preamplifier Design Maintaining Low Power Consumption," 3rd International Conference on Microwave and Millimeter Wave Technology Preceedings, 2003.
- [20] T. Yoon, B. Jalali, "Front-End CMOS Chipset for Fiber-Based Gigabit Ethernet," Symposium on VLSI Circuits Digest of Technical Papers, 1998.
- [21] J. Twomey, "Analog and Mixed Signal Circuits on Digital CMOS Processes," IEEE.
- [22] K. V. Noren, J. Choma, Jr., J. Trujillo, D. G. Haigh, B. Redman-White, R. Akbari-Dilmaghani, M. Ismail, S-C. Huang, C-C. Hung, T. Saether, The Circuits and Filters Handbook, Second Edition, CRC Press LCC, 2003.
- [23] R. G. Smith, B. L. Kasper, The Communications Handbook, CRC Press LLC, 2002.
- [24] C. Toumazou, A. Payne, High Frequency Amplifiers, CRC Press LLC, 2000.
- [25] J. Lu, Y. Wang, N. Xu, M. Gao, "Temperature Compensation in Bootstrapped Current Reference Source," IEEE, 2003.
- [26] Lecture 7 - Operational Amplifiers II, Linkopings Universitet Department of Electrical Engineering, p83 – 90.
- [27] M. J. Hayes, "A Nonlinear Optical Preamplifier for Sensing Applications," IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, vol. 49, no. 1, January 2002.

- [28] T. Vanisri, C. Toumazou, "Low-Noise Optimization of Current-Mode Transimpedance Optical Preamplifiers," Imperial College of Science, Technology and Medicine, Department of Electrical and Electronic Engineering, London, IEEE, 1993.
- [29] J. D. Cressler, SiGe Technology, CRC Press LLC, 2000.
- [30] K. Washio, "SiGe HBT and BiCMOS Technologies for Optical Transmission and Wireless Communication Systems," IEEE Transactions on Electron Devices, vol. 50, no. 3, March 2003.
- [31] C. M. Snowden, "Compound Interest," IEE Review, January 2002.
- [32] M. Abe, T. Mimura, K. Nishiuchi, A. Shibatomi, M. Kobayashi, "Recent Advances in Ultra-High-Speed HEMT Technology," IEEE Journal of Quantum Electronics, vol. QE-22, no. 9, September 1986.
- [33] Y. Suzuki, K. Honjo, "Wide-Band Transimpedance Amplifiers Using AlGaAs/In_xGa_{1-x}As Pseudomorphic 2-D EG FETs," IEEE Journal of Solid-State Circuits, vol. 33, no. 10, October 1998.
- [34] J. D. Cressler, "SiGe HBT Technology: A New Contender for Si-Based RF and Microwave Circuit Applications," IEEE Transactions on Microwave Theory and Techniques, vol. 46, no. 5, May 1998.
- [35] B. Razavi, "Prospects of CMOS Technology for High-Speed Optical Communication Circuits," IEEE Journal of Solid-State Circuits, vol. 37, no. 9, September 2002.