Highly Linear LNA Design for 4G WiMAX Applications

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Abstract

This Major Qualifying Project involves the design, implementation and testing of input and output matching circuits for an RF Low Noise Amplifier for an operating frequency spectrum between 3300MHz and 3600MHz. Based upon the request of our project sponsor, the report reflects a design approach emphasizing computer simulations, using Agilent's ADS software. The simulations are subsequently employed to develop a physical circuit. This circuit is then refined through testing and tuning.

Acknowledgements

We would like to thank Skyworks Solutions, Inc. for their generosity in sponsoring this project. More specifically, we would like to thank Ambarish Roy and Vivian Tzanakos for sharing their knowledge and expertise. Special thanks go to Professor Ludwig and Professor McNeill for their endless guidance and their contributions to our understanding of conceptual RF amplifier design, upon which this project is based.

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1 Introduction

For over 20 years, there has been an increasing demand for personal wireless communications. [1] As a result, there is a continual drive within the wireless communication industry to design and use the most advanced technology available. Numerous firms have addressed this need; among them is Skyworks Solutions, Inc.

Skyworks Solutions, Inc. offers a portfolio of high-performance RF components for fixed and mobile Worldwide Interoperability for Microwave Access (WiMAX) applications. These devices are suitable for use in base stations, enterprise customer-premises equipment (CPE), and low-cost mobile/portable subscriber equipment targeting the licensed WiMAX bands at 2.5 and 3.5 GHz. The company's portfolio includes key components within the radio chain, one of which being low noise amplifiers (LNA). A generic transceiver radio chain is shown in Figure 1. The receiver chain is displayed on the upper half of Figure 1. After the signal is received by the antenna it is filtered and then amplified by an LNA. The signal is amplified so that the full range of the Analog to Digital Converter (ADC) can be utilized. The LNA should not add much noise to the analog signal thereby reducing the bit error rate when the signal is decoded. After the LNA, the signal is down converted to an intermediate frequency using a down converter mixer. The signal is then further filtered and further down converted before being sampled using an ADC.

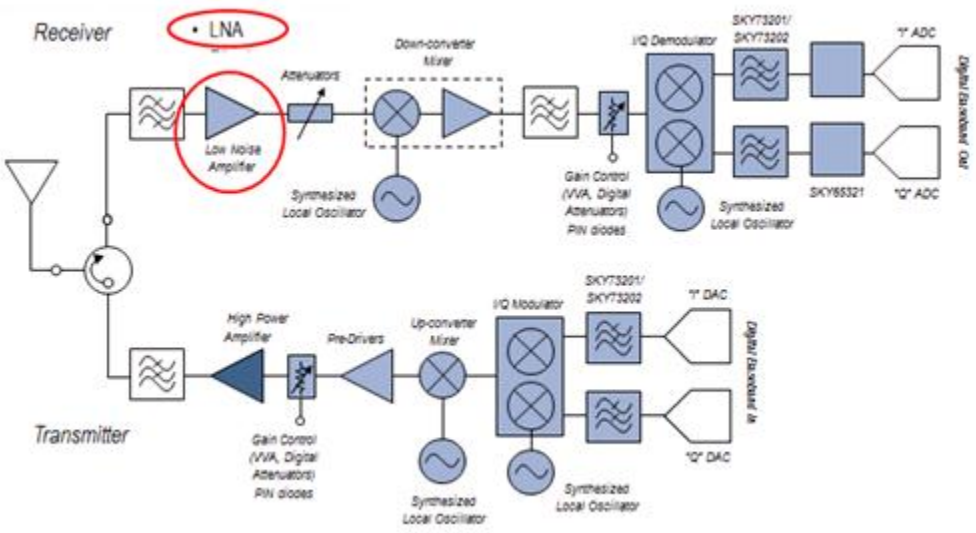

Figure 1 RF Front-End Architecture for Generic Infrastructure Transceiver [1]

WiMAX is a trademark for a family of telecommunications protocols that provide fixed and mobile Internet access. It is a wireless digital communications system, also known as IEEE 802.16, which is intended for wireless "metropolitan area networks". WiMAX is an Internet Protocol (IP) based, wireless broadband access technology that provides performance similar to 802.11/WiFi networks with the coverage and quality of service (QOS) of cellular networks.

As the technology advances in the area of communication systems, such as cellular networks, so do the requirements for the LNA. An LNA is a key component which is placed at the front-end of a radio receiver circuit. Receiving multiple signals, at different power levels over different frequency ranges, place high requirements on the LNA performance for low noise and high linearity. While the optimization of an LNA design is fairly mature for the GSM and CDMA standards, the emerging fourth generation (4G) application areas offer an open field for design innovation.

The purpose of this project is to design and test application circuitry for a cellular-base station 4G receiver chain, using the SKY67003 LNA from Skyworks Solutions, Inc. Matching and bias networks will be designed for the LNA to operate at the WiMAX 3.5 GHz frequency band. Since the LNA is used in a base station the signal performance of the device is a higher priority as opposed to its power consumption. The key considerations for our design will include stability, linearity, Noise Figure, input match, output match and protection from electrostatic discharge; each of the topics will be explained in detail in the background chapter.

The design will be simulated using Advanced Design System (ADS), an industry standard RF circuit simulator, and implemented on an evaluation board. The performance of the final design will go through a series of tests and measurements for verification. The data from these measurements will be recorded, documented, and compared to the theoretical and simulated predictions.

2 Background

This section puts into context our research and describes the main concepts required for realizing the LNA design project for a frequency of 3.5 GHz and achieving the performance characteristics required by Skyworks Solutions, Inc.

2.1 WiMAX

Fourth Generation mobile standards, widely advertised as 4G, is the fourth generation of standards for mobile phones and mobile telecommunications that adheres to the International Mobile Telecommunications (IMT) Advanced specifications by the International Telecommunication Union. The fourth generation of standards for mobile phones and mobile telecommunications will be based on Orthogonal Frequency Division Multiplexing (OFDM) – the next generation in access technologies. The evolution of standards for mobile telecommunications is shown in Figure 2.

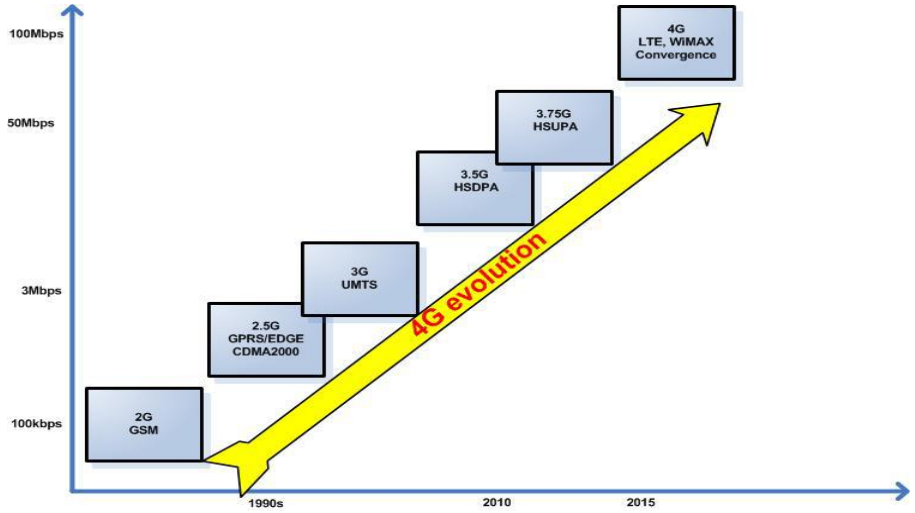

Figure 2 A graph showing the evolution of wireless cellular standard [2]

WiMAX is an Internet Protocol (IP) based, wireless broadband access technology that provides performance similar to 802.11/WiFi networks with the coverage and quality of service

(QOS) of cellular networks. WiMAX can provide broadband wireless access up to 30 miles for fixed stations, and 3 - 10 miles for mobile stations, as compared to WiFi/802.11 standard which is limited to 100-300 feet. WiMAX supports data rates similar to WiFi but has fewer problems with regard to multipath interference and shadow fading. It provides data rates of up to 40Mbit/s for mobile stations and 1Gbit/s for fixed stations. WiMAX operates on both licensed and non-licensed frequencies, providing a regulated environment and viable economic model for wireless carriers. [3]

OFDM and Orthogonal Frequency-Division Multiple Access (OFDMA) control interference by breaking the signal into subcarriers. OFDM is a combination of modulation and multiplexing. In OFDM, the signal is split into independent channels, modulated by data and then re-multiplexed to create the OFDM Carrier. It is spectrally efficient and it mitigates the severe problem of multipath propagation that causes massive data errors and loss of signal. OFDMA is a multi-user version of the OFDM digital modulation scheme. Multiple access is achieved by assigning subsets of subcarriers to individual users which allows simultaneous low data rate transmission from several users. OFDMA is also very well suited for use with Adaptive Antenna Systems (AAS) and multiple-input multiple-output (MIMO) which can significantly improve throughput, increase link range, and reduce interference. Figure 3 graphically describes the difference between OFDM and OFDMA. [4]

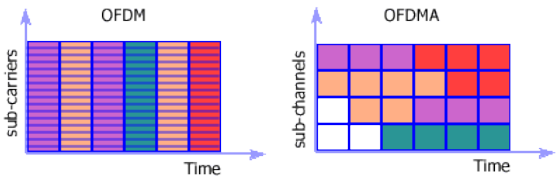

Figure 3 Uplink Sub channelization in WiMAX [4]

As plotted along the y-axis in Figure 3, sub channelization defines sub-channels that can be allocated to subscriber stations (SS) depending on their channel conditions and data requirements. Using sub channelization, within the same time slot a Mobile WiMAX Base Station (BS) can allocate more transmit power to user devices (SSs) with lower Signal-to-Noise Ratio (SNR), and less power to user devices with higher SNR. Sub channelization also enables the BS to allocate higher power to sub-channels assigned to indoor SSs resulting in better in-building coverage.

Scalable OFDMA (SOFDMA) is the OFDMA mode used in Mobile WiMAX. It supports channel bandwidths ranging from 1.25 MHz to 20 MHz. With bandwidth scalability, Mobile WiMAX technology can comply with various frequency regulations worldwide. SOFDMA scales the Fast Fourier Transform (FFT) to the channel bandwidth to keep the carrier spacing constant across different channel bandwidths. This results in higher spectrum efficiency; WiMAX is the most energy-efficient pre-4G technique among LTE and HSPA+. WiMAX offers a very low latency, less than 10 milliseconds from base station to CPE.

There is prioritization of traffic in WiMAX to provide good quality of service. The modulation schemes used are 64-QAM, 16-QAM and QPSK that guarantee steady signal strength over distance. WiMAX offers a wide frequency spectrum, which means greater bandwidth can be transported. On the other side, with lower frequency, the carry range is greater, as well as the penetration of a signal. To resolve this issue, a band spectrum is allocated high power levels to aid with tree and building wall dispersion. The 3 GHz licensed spectrum allows for higher data rates and can transmit over longer distances since there is no interference from competing services. Combining SOFDMA with smart antenna technology leads to spectral efficiency of 3.7 bit/s/Hz. WiMAX offers 99.999 % reliability by using redundant radios to cover a marketplace. Radios have a mean time between failures of 40 years.

2.2 Scattering parameters

The scattering or S-matrix is a mathematical, but also practical tool, that quantifies how RF energy propagates through a multi-port network. The S-matrix is what allows us to accurately describe the properties of complicated linear networks as simple "black boxes". For an RF signal incident on one port, some fraction of the signal bounces back out of that port, some of it scatters and exits other ports, and some of it disappears as heat or even electromagnetic radiation. The S-matrix for an N-port contains N^2 individual S-Parameters, each one representing a possible input-output path. The incident voltage is denoted by “a”, while the voltage leaving a port is denoted by “b”. A generalized two-port network is displayed in Figure 4.

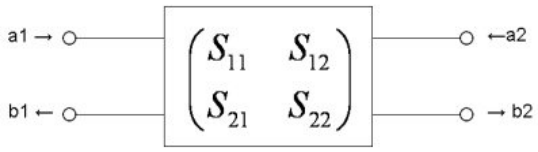

Figure 4 Generalized two-port network [5]

Here's the matrix algebraic representation of 2-port S-Parameters:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \times \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \quad (1)$$

S_{11} is the input port voltage reflection coefficient

$$S_{11} = \frac{b_1}{a_1} \quad (2)$$

S_{12} is the reverse voltage gain

$$S_{12} = \frac{b_1}{a_2} \quad (3)$$

S_{21} is the forward voltage gain

$$S_{21} = \frac{b_2}{a_1} \quad (4)$$

S_{22} is the output port voltage reflection coefficient. [5]

$$S_{22} = \frac{b_2}{a_2} \quad (5)$$

2.3 DC Biasing Point

The purpose of the DC bias is to select the proper quiescent point and hold the quiescent point constant over variation in transistor parameters and temperature. A resistor bias network can be used for moderate temperature ranges. However, an active bias network is usually preferred for large temperature ranges. The selection of the biasing point is dependent on which class of amplifier is being used. Since the SKY67003 is a class A amplifier, the DC bias point chosen should be able to conduct 360 degrees of the input cycle. The bias circuitry should also decouple RF from DC. This is achieved by means of blocking capacitors, which allow RF signals to pass, and RF chokes which block the high frequency signals. [6]

2.4 Stability

Unconditional stability means that with an arbitrary, passive load connected to the output of the device, the circuit will not become unstable, i.e. will not oscillate. Instabilities are primarily caused by three phenomena: internal feedback of the transistor, external feedback around the transistor caused by external circuits, or excess gain at frequencies outside of the band of operation.

The main way of determining the stability of a device is to calculate the so-called Rollett's stability factor (K), which is calculated using a set of S-Parameters for the device at the frequency of operation.

The conditions of stability at a given frequency are $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$, and must hold for all possible values Γ_L & Γ_S obtained using passive matching circuits. We can calculate two stability parameters K and $|\Delta|$ to give us an indication as to whether a device is likely to oscillate or whether it is conditionally/unconditionally stable.

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (6)$$

and

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}-S_{21}|} > 1 \quad (7)$$

The parameter K must satisfy $K > 1$, $|\Delta| < 1$ and the parameter B must be greater than 0 for a transistor to be unconditionally stable.

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \quad (8)$$

All devices with $|S_{11}|$ and $|S_{22}| < 1$ must be stable for a passive load impedance. Therefore, the center of the Smith Chart must always be the stable region. However, in the case where $|S_{11}|$ or $|S_{22}| > 1$ and the stability circle covers the center of the Smith Chart, then this region is unstable.

The stability factor, μ, defines the minimum distance between the center of the Smith Chart and the unstable region in the load plane. The function assumes that port 2 is the load. The stability factor, μ', defines the minimum distance between the center of the Smith Chart and the unstable region in the source plane. The function assumes that port 1 is the source. Having $\mu > 1$ or $\mu' > 1$ is the necessary and sufficient condition for the 2-port linear network to be unconditionally stable, as described by the S-Parameters. [7][8]

$$\mu = \frac{1-|S_{11}|^2}{|S_{22}-S_{11}{}^*\Delta|+|S_{21}S_{12}|} \quad (9)$$

$$\mu' = \frac{1-|S_{22}|^2}{|S_{11}-S_{22}{}^*\Delta|+|S_{21}S_{12}|} \quad (10)$$

2.5 Linearity and Gain Compression

LNA linearity is an important parameter. High linearity is necessary for low adjacent channel leakage power. Adjacent Channel Power Ratio (ACPR) or Adjacent Channel Leakage Ratio (ACLR) is a measure of the transmitter energy that is 'leaking' into an adjacent or alternate channel. Ideally, a transmitter could retain all of its transmitted energy in its assigned channel, but realistically some small amount of the transmitter energy will show up in other nearby channels. A spectrum analyzer is the ideal choice for making this measurement. WiMax profiles have channel spacing between 5 MHz to 10 MHz. Since the channel spacing is so low there is more chance of leakage into adjacent channels and signal integrity being degraded.

The input and output loads of the amplifier can be swept directly through source and load pull techniques. Load pull is the process of varying the impedance seen by the output of an active device to other than 50 Ω in order to measure performance parameters, in the simplest case, gain. In the case of a power device, a load pull power bench is used to evaluate large signal parameters such as compression characteristics, saturated power, efficiency and linearity as the output load is varied across the Smith Chart. [9]

Figure 5 shows the 1dB compression point (P1dB) and 3rd order intercept point (IP3). The IP3 is a figure of merit for linearity. A two-tone test is typically used for the derivation of IP3. IP3 has emerged as an important parameter in LNA design. IP3 is an important parameter for system designers to estimate the spurious free dynamic range (SFDR). SFDR is the strength

ratio of the fundamental signal to the strongest spurious signal in the output. At high frequencies, and particularly with narrowband circuits, it is more common to characterize the distortion produced by a circuit in terms of a P1dB or an intercept point. Gain compression in an electronic amplifier circuit is a reduction in 'differential' or 'slope' gain caused by nonlinearity of the transfer function of the amplifying device. The large signal input/output relation can display gain compression or expansion. Physically, most amplifiers experience gain compression for large signals. The P1dB is defined as the point where the gain has dropped by 1dB on the logarithmic scale of gain as a function of input power. The extrapolated point where the curves of the fundamental signal and third order distortion product signal meet is identified as IP3. The input power level is known as IIP3, and the output power when this occurs is the OIP3 point. Figure 5 shows the output power vs. input power of the fundamental frequency and the third order intermodulation (IMD_3) product. [10][11]

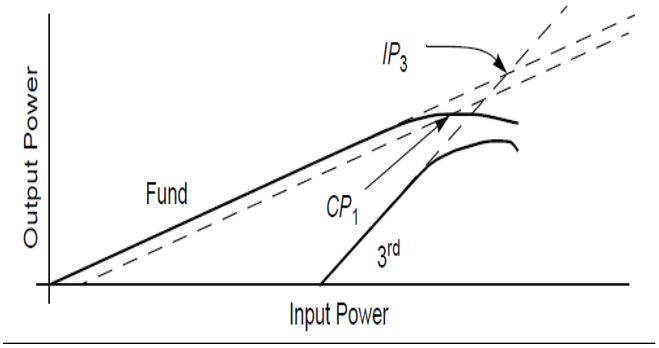

Figure 5 CP1 and 3rd order intercept point [11]

To measure the P1dB point of a circuit, a sinusoid (or tone) is applied to its input and the output power of this fundamental signal is plotted as a function of input power. Circuits which are operated within a narrow bandwidth are tested by applying two sinusoid terms with slightly different frequencies, within the narrow bandwidth. Intermodulation is a scenario where signals outside the monitored channel combine nonlinearly to produce a frequency of monitored channel. The traditional approach to measuring a two-tone IP3, begins by applying two sinusoids

to the circuit's input at frequencies f_1 and f_2. The frequencies at which the IMD_3 products appear for the signals, f_1 and f_2, would be:

$$2f_1 \pm f_2$$
$$2f_2 \pm f_1$$

where $2f_1$ is the second harmonic of f_1 and $2f_2$ is the second harmonic of f_2.

Figure 6 shows the two tones with the IMD_3 products.

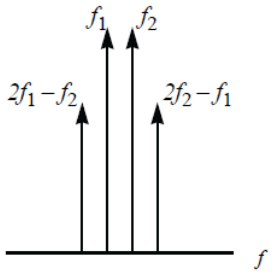

Figure 6 Response of a circuit to a traditional two-tone IP3 test [11]

Distortions in a system are represented with the help of a Taylor series. This series does not account for memory losses in the system. The Taylor series is represented by the following equation:

$$x = au + bu^2 + cu^3 \ldots \quad (11)$$

where a, b, c are constants from the device transfer function and multiplies the signal by the value of the constant. This derivation does not take into account the memory effects of the amplifier.

Here the two tones are given by

$$u = \alpha \cos(\omega_1 t) + \beta \cos(\omega_2 t) \quad (12)$$

where ω_1 and ω_2 are two different frequencies within the same narrow band, and α and β are the amplitudes of each of the cosine terms.

The system transfer function, with u as input and x as output, can be represented in block diagram form by Figure 7:

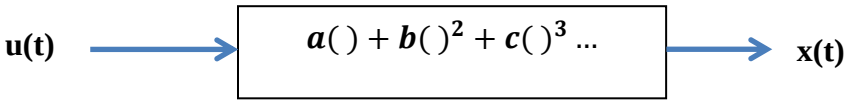

Figure 7 Transfer Function of a Generalized System

When computing the IP3 only the first two odd order terms need to be considered.

$$x = au + cu^3 \tag{13}$$

The following equations describe how the IP3 can be calculated by applying the dual tones.

$$OIP3 = P_{1st} + \frac{(P_{1st} - P_{3rd})}{2} \quad \text{dBm} \tag{14}$$

$$IIP3 = OIP3 - G \quad \text{dBm} \tag{15}$$

where P_{1st} is the power of the fundamental in dBm and P_{3rd} is the power of the third order inter-modulation product in dBm. [12]

The easiest way to improve IP3 performance, for a given frequency, is to increase the current density or current draw of the LNA. Until the current density reaches relatively high levels, it will continue to improve with increasing current draw. If current draw is less important than IP3 performance, then it can be increased with the usual slight increase in gain and Noise Figure. So, in this case, IP3 improves with the trade-off in current draw and Noise Figure.

2.6 Noise Figure and Input Return Loss

The input matching network plays the most important consideration in the Noise Figure performance of the overall LNA Design. This is because the input matching stage is the first stage of the LNA design.

$$F_{cas} = F_1 + \frac{1}{G_1}(F_2 - 1) + \frac{1}{G_1 G_2}(F_3 - 1) \tag{16}$$

where F_{cas} is the overall linear noise factor of the cascaded system, F_i are the noise factors for the first, second and third stage, respectively, and $G_{1,2}$ are the gains for the first and second stage. As equation 16 of the cascaded Noise Figure shows, the first stage is the most critical in Noise Figure performance. This equation shows that the first stage should have a low Noise Figure and a moderate gain.

The next step in the LNA design consists of noise match measured through the input return loss (IRL). IRL defines how well the circuit is matched to 50 Ω impedance of the source. A typical approach in LNA design is to develop an input matching circuit that terminates the transistor to Gamma optimum (Γ_{opt}), which represents the terminating impedance of the transistor for the best noise match. In many cases, this means that the IRL of the LNA will be compromised. The optimal IRL can be achieved only when the input-matching network terminates the device with a conjugate of S_{11}, which in many cases is different from the conjugate of Γ_{opt}. An emitter inductor feedback may rotate S_{11} closer to Γ_{opt}, which can help with obtaining close to minimum Noise Figure and respectable IRL simultaneously. This additional inductance at the emitter of the transistor will also reduce the overall available gain of the network and can be used in balancing trade-offs between the gain, IIP3, and stability of the LNA design. However, this so called inductive degeneration does not as seriously impact Noise Figure performance, as resistive degeneration does. At high frequencies this inductance will be achieved with small strip lines (stubs) connected directly to the emitters of the transistor. The inductive reactance of the stubs is usually no greater than 10 Ω and the line lengths are typically ~2mm or less with characteristic impedances 50 Ω or greater. [7]

The noise factor of an active RF system can be defined as:

$$F_{total} = \frac{signal\ to\ noise\ ratio\ at\ the\ input}{signal\ to\ noise\ ratio\ at\ the\ output} = \frac{S_i/N_i}{S_o/N_o} \qquad (17)$$

where S_i is the input signal power, S_o is the output signal power, N_i is the noise power at the input, and N_o is the noise power at the output.

The Noise Figure of a two-port network active device is given by [7]

$$F = F_{min} + 4\frac{R_n}{Z_0}\frac{|\Gamma_s - \Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2(1-|\Gamma_s|^2)} \quad (18)$$

where F_{min} is the minimum Noise Figure, Γ_{opt} is the optimum reflection coefficient, R_n is the equivalent noise resistance and Z_o is the system impedance to be taken as 50 Ω.

Source pull is the process of varying the impedance seen by the input of an active device to other than 50 Ω in order to measure performance parameters. In the case of a low noise device, source pull is used in a noise parameter extraction setup to evaluate how the signal-to-noise ratio (Noise Figure) varies with source impedance. In noise parameter extraction, the output is load-pulled to an impedance that provides high gain, and then the input is swept all over the Smith Chart.

2.7 Gain

The need to obtain a desired gain performance is another important consideration in the amplifier design task. The transducer power gain G_T, quantifies the gain of the amplifier placed between source and load.

$$G_T = \frac{Power\ delivered\ to\ the\ load}{Available\ power\ from\ the\ source} = \frac{P_L}{P_{Avs}} = \frac{(1-|\Gamma_L|^2)|S_{21}|^2(1-|\Gamma_S|^2)}{|1-\Gamma_L\,\Gamma_{out}|^2|1-S_{11}\,\Gamma_S|} \quad (19)$$

Here, P_L is the average power delivered to the load and P_{Avs} is the maximum power available from the source. Figure 8 shows the block diagram of the transducer power gain with P_{Avs} and P_l labeled.

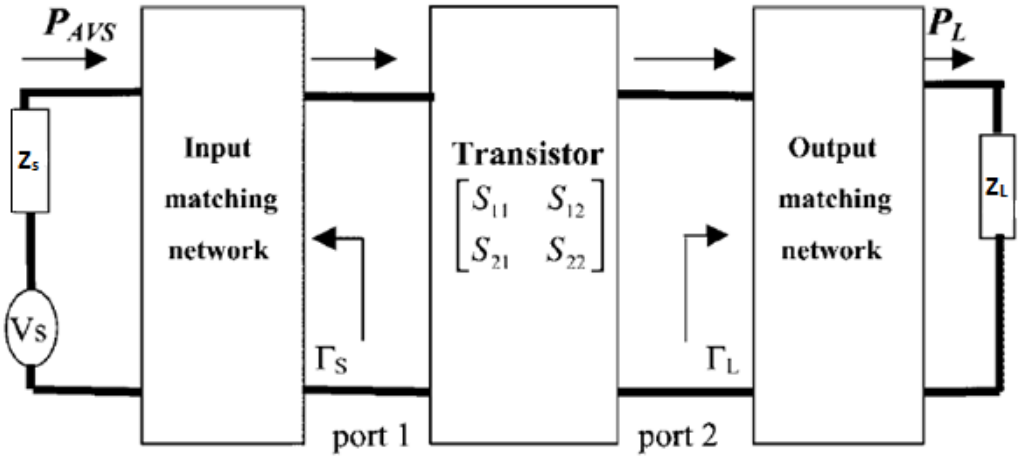

Figure 8 Block Diagram of the transducer power gain

Furthermore,

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S} \tag{20}$$

A unilateral device is one whose scattering parameter $S_{12} = 0$, implying that the transistor network has no internal feedback. The unilateral transducer power gain is

$$G_{TU} = \frac{(1-|\Gamma_L|^2)|S_{21}|^2(1-|\Gamma_S|^2)}{|1-\Gamma_L S_{22}|^2|1-S_{11}\Gamma_S|} \tag{21}$$

This equation can be rewritten such that the individual contributions of the matching networks become identifiable:

$$G_{TU} = G_S \cdot G_0 \cdot G_L \tag{22}$$

Where G_0 is the insertion gain of the transistor, G_s and G_L are gain associated with input and output matching networks. The individual blocks are

$$G_S = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2} \tag{23}$$

$$G_0=|S_{21}|^2 \tag{24}$$

$$G_L = \frac{1-|\Gamma_L|^2}{|1-\Gamma_L S_{22}|^2} \tag{25}$$

If $|S_{11}|$ and $|S_{22}|$ are less than unity, the maximum unilateral power gain ($S_{12}=0$) results when both input and output are matched. For this case it is seen that

$$G_{Smax} = \frac{1}{1-|S_{11}|^2} \tag{26}$$

$$G_{Lmax} = \frac{1}{1-|S_{22}|^2} \tag{27}$$

The contributions from G_s and G_L can be normalized to their maximum values such that:

$$g_i = \frac{G_i}{G_{i\,max}} = \frac{1-|\Gamma_i|^2}{|1-\Gamma_i S_{ii}|^2}(1-|S_{ii}|^2) \tag{28}$$

where i can be either S or L, for source and load respectively, and ii can be either 11 or 22.

The gain circles have center locations of

$$d_{g_i} = \frac{g_i S^*_{ii}}{1-|S_{ii}|^2(1-g_i)} \tag{29}$$

and radii

$$r_{g_i} = \frac{\sqrt{1-g_i}(1-|S_{ii}|^2)}{1-|S_{ii}|^2(1-g_i)} \tag{30}$$

The network gains can be greater than unity as without any matching a significant power loss can occur at the input and output sides of the amplifier.

The bilateral case is more complicated, this is where feedback connects part of the output back to the input of the amplifier. In order to determine the error involved in assuming $S_{12}=0$, the ratio of unilateral gain and total gain needs to be obtained.

$$\frac{G_T}{G_{TU}} = \frac{1}{|1-X|^2} \tag{31}$$

where

$$X = \frac{S_{12}S_{21}\Gamma_S\Gamma_L}{(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)} \tag{32}$$

When $\Gamma_s=S_{11}^*$ and $\Gamma_L=S_{22}^*$ the above equation changes into:

$$U = \frac{S_{12}S_{21}S_{11}S_{22}}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \tag{33}$$

In Eq. (32) U is known as the unilateral figure of merit and the ratio changes to:

$$\frac{G_T}{G_{TU}} = \frac{1}{|1-U|^2} \tag{34}$$

When this ratio is less than 1 the error is small enough to justify that $S_{12} \approx 0$ and use the unilateral assumption. When $S_{12}\neq 0$, generally the unilateral assumption cannot be made. The conditions required to obtain maximum gain result in:

$$\Gamma_s=\Gamma_{in}^* \tag{35}$$

and

$$\Gamma_L=\Gamma_{OUT}^* \tag{36}$$

where

$$\Gamma_s^* = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \tag{37}$$

and

$$\Gamma_L^* = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S} \tag{38}$$

This case is known as the bilateral figure of merit. [5]

2.8 Electrostatic Discharge

Static charge is the net electrical charge at rest. It can be created in various occasions when the insulator surfaces rub together or pull apart. One surface would gain electrons and the other surface loses electrons. The unbalanced electrical condition is called the static charge. When static charges moves from one surface to another, it becomes electrostatic discharge (ESD). If the voltage potential difference between two surfaces is sufficiently high, the current created by the movement of static charges can damage or destroy the gate oxide, metallization and junctions in integrated circuits (ICs). ESD problems are increasing in the electronics industry because of the trend toward higher speed and smaller device sizes. ESD is now a major consideration in the design and manufacture of ICs. [13]

There are three major test methods widely used in the industry to describe uniform methods for establishing ESD-withstand thresholds. The Human Body Model (HBM) was developed to simulate the action of a human body discharging the accumulated static charge through a device to ground. An RC series network is used for the HBM simulation consisting of a 1500 Ω resistor and a 100 pF capacitor. The simulation of a machine discharge accumulated static charge through a device to ground is called the Machine Model (MM). The third model, Charged-Device Model (CDM) simulates charging/discharging events that occur in production equipment and processes. [13]

2.9 Device Technology

This section explains some of the semiconductor physics and the circuit design of the SKY67003 LNA. The behavior of passive components such as resistors, capacitors and inductors at radio frequencies is also discussed.

2.9.1 Semiconductor Physics

A semiconductor is a material with electrical conductivity due to electron and hole flow intermediate in magnitude between that of a conductor and an insulator. Semiconductors are commonly inorganic materials made from elements in the fourth column in the periodic table. Semiconductor materials can also be made from a combination of elements from either group III and group V or group II and group VI. The common semiconductor materials used in integrated circuit design are silicon, germanium and gallium arsenide. Gallium arsenide (GaAs) is a III/V semiconductor that is commonly used in the manufacture of high frequency integrated circuits. Compared to silicon, GaAs has a higher saturated electron velocity, higher electron mobility and lower heat sensitivity. The high electron mobility allows the transistors to function at higher frequencies. [14]

2.9.2 High Electron Mobility Transistors

High Electron Mobility Transistor (HEMT) is a field effect transistor (FET) incorporating a junction between two materials with different band gap energy levels as the channel, instead of a doped region. In the HEMT structure, compositionally different layers are grown in order to optimize and to extend the performance of the FET. Semiconductors are doped with impurities to allow conduction that donate electrons (or holes). Nevertheless, these electrons are slowed down through collisions with the dopants. HEMTs avoid this by using high mobility electrons generated using the heterojunction of a highly-doped wide-bandgap n-type donor-supply layer and a non-doped narrow-bandgap channel layer with no dopant impurities. HEMTs have shown current gain to frequencies greater than 600GHz and power gain to frequencies greater than 1THz. A HEMT grown on a GaAs substrate is shown in Figure 9.

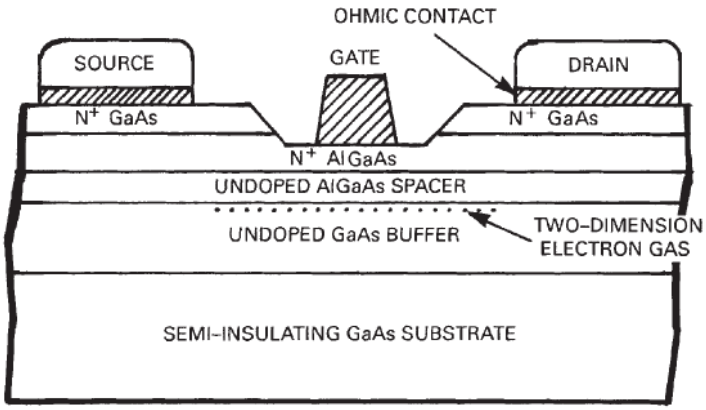

Figure 9 GaAs Substrate High Electron Mobility Transistor [14]

LNAs for high frequency applications have been based on pseudomorphic HEMT (pHEMT) technologies for some time. These transistors avoid deep-level traps –discontinuities in the semiconductor crystal lattice- by having an extremely thin layer. This technique allows the construction of transistors with larger bandgap differences than otherwise possible, giving them better performance. The newer enhancement-mode pHEMT (E-pHEMT) technologies have been used primarily for power amplifier applications. E-pHEMT is a semiconductor process optimized for wireless applications that operates from a single positive voltage source. Other gallium arsenide metal-semiconductor FETs and HEMTs also operate from a positive voltage supply and require a negative voltage to turn on.[15]

Amplifiers used in wireless infrastructure receiver applications have key requirements of low noise, high linearity, and unconditional stability. In order to meet these needs, Skyworks Solutions, Inc. has developed a new family of LNAs implemented in 0.5 μm E-pHEMT. Furthermore, Skyworks Solutions, Inc. has developed SKY67003 LNAs which are made of GaAs substrate and are pHEMT LNAs with an active bias and high linearity performance. [16][17]

2.9.3 Cascode Topology

The Skyworks Solutions, Inc. LNA family uses a cascode LNA topology. The cascode amplifier is a two-stage amplifier, where the first stage is generally a transconductance amplifier and the second stage is the current buffer. The cascode topology is used when a single stage amplifier provides insufficient gain. The major advantage of the cascode arrangement is because of the placement of the upper FET. The upper FET exhibits a low input resistance to the lower FET, making the voltage gain of the lower FET very small, which reduces the Miller feedback capacitance from the lower FET's drain to gate. This loss of voltage gain is recovered by the upper FET. Thus, the two FETs in combination reduce the Miller effect, improving the bandwidth of the amplifier [18]. A generic picture of a common source amplifier as the input stage driven by a signal V_{in} with cascode architecture is shown in Figure 10. This circuit diagram is similar to the one used by Skyworks Solutions, Inc. on the SKY67003 LNA.

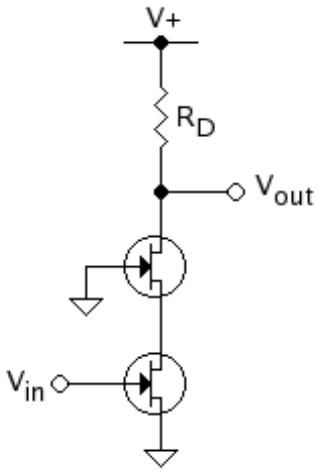

Figure 10 Generic Cascode Design [18]

Another advantage of using the cascode design is the reduction of unwanted distortion created by the capacitive feedback in amplifiers. This makes the arrangement very stable. The distortion is prevented because the output is effectively isolated from the input. The lower FET has nearly constant voltage at both drain and source which results in no feed back into its gate.

The upper transistor has constant voltage at its gate and source. Therefore only the input and output nodes have significant voltages. This means that such cascade amplifiers are essentially unilateral because of the minimum feedback. Compared to the single stage amplifier the cascaded amplifier may have higher input-output isolation, higher input impedance, higher output impedance, higher gain and higher bandwidth. [19][20]

2.9.4 RF Behavior of Passive Components

The input matching, output matching and bias networks for the LNA will be created using lumped resistors, capacitors and inductors. The components are all 0402s (0.40mm x 0.20mm) surface mount devices. At RF frequencies these passive components have parasitic effects which start to dominate as the frequency is increased. Therefore each component has its own equivalent circuit model. The choice of these components is based upon its quality factor and resonant frequency. For low frequencies each of these components behaves as predicted by its impedance formulas. However at higher frequencies resistors change their impedances as a function of frequency, inductors become capacitive and capacitors show inductive responses. [5]

An ideal capacitor should lose zero amount of energy over any frequency. However, due to the dielectric loss of the dielectrics as well as the loss caused by the resistive components, an actual capacitor dissipates energy. The energy lost is indicated by the parameter Q. The higher Q value means the less energy is lost. The internal generation of heat of a capacitor increases in proportion to the equivalent series resistance (ESR). Because the ESR of a Hi-Q capacitor is lower than that of general-purpose capacitors, the power capacity of the Hi-Q capacitor is larger.

The Murata GJM series is a High Q, ultra-small capacitor series for high frequency applications in the 500 MHz to 10 GHz range. The GJM series is made with copper electrodes as a cost effective solution for low equivalent series resistance and power consumption due to the

high Q performance. A variety of tight tolerance versions are available, offered in EIA sizes 0201 and 0402 with a capacitance range of 0.1 to 33 pF. Figure 11 shows the structure of Murata GJM series capacitors. On the other hand, Murata's GRM series capacitor is the general purpose capacitor with lower Q factor. In RF design, high Q components are more expensive than components with lower Q factor. [21]

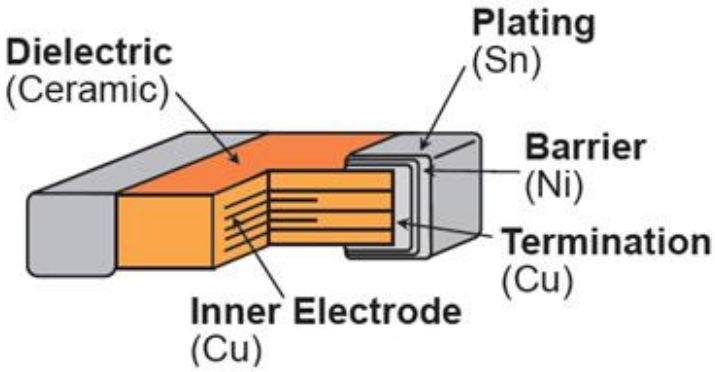

Figure 11 Murata GJM series high Q capacitor structure[21]

High Q or tight inductance tolerance is also required to improve signal quality and reduce signal loss. Murata's LQW series RF inductors are recommended for LNA matching and RF chokes. Figure 12 shows the structure of Murata's LQW series RF inductors. Comparing to the expensive LQW inductors, LQG series inductor from Murata is a cheaper replacement at places where high Q is not required. In general, a high Q inductor or capacitor is more than 10 times more expensive than a general purpose inductor or capacitor. Therefore, to be cost efficient, this project will only use the high Q components on the input matching network since most of the noises are introduced on the input side. [22]

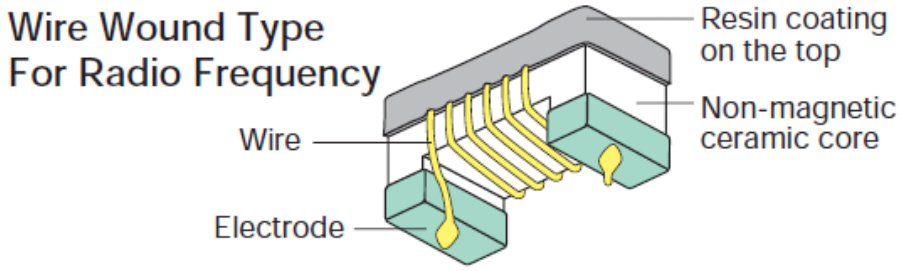

Figure 12 Murata LQW series high Q inductor construction[22]

Resistors

Figure 13 shows the equivalent circuit model of a resistor and Figure 14 shows a typical resistor's impedance change over a range of frequencies. As you can see in Figure 14, once a resistor is operated up to a certain frequency, the capacitive effect will dominate and start reducing the impedance. When the frequency goes up even farther, the impendence of the resistor will then start increasing due to the inductive effect.

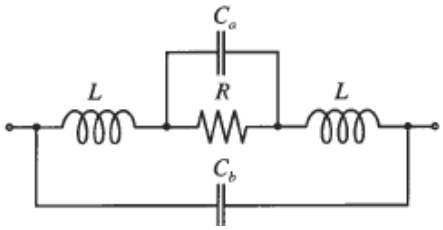

Figure 13 Equivalent circuit model of a resistor [5]

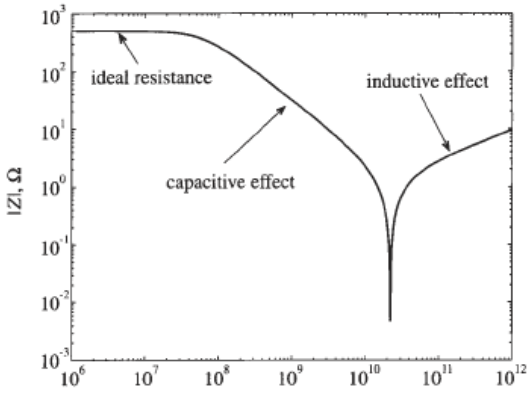

Figure 14 Impedance response of a resistor [5]

Inductor

The equivalent circuit of an inductor consists of the series combination of an inductor and a resistor in parallel with a capacitor, as shown in Figure 15. Figure 16 shows the impedance response of an inductor. An ideal inductor has linear impedance as function of frequency. However, a real inductor will have nonlinearity in high frequency.

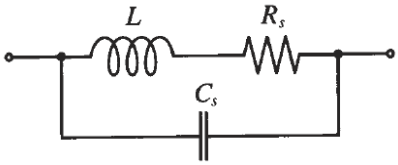

Figure 15 Equivalent circuit of an inductor [5]

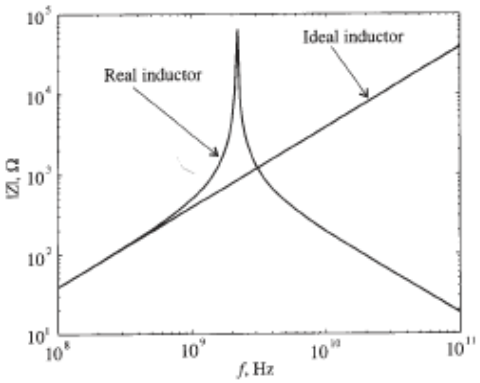

Figure 16 Impedance Response of an inductor [5]

Capacitor

Figure 17 shows the equivalent circuit of a capacitor and Figure 18 depicts the impedance response. In Figure 18, the linear declining line is the impedance response of an ideal capacitor as function of frequency. In high frequency, the nonlinearity of a real capacitor is also represented in Figure 18.

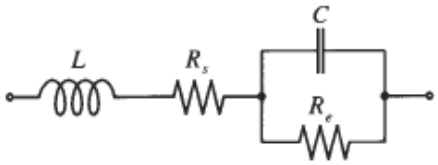

Figure 17 Equivalent circuit of a capacitor [5]

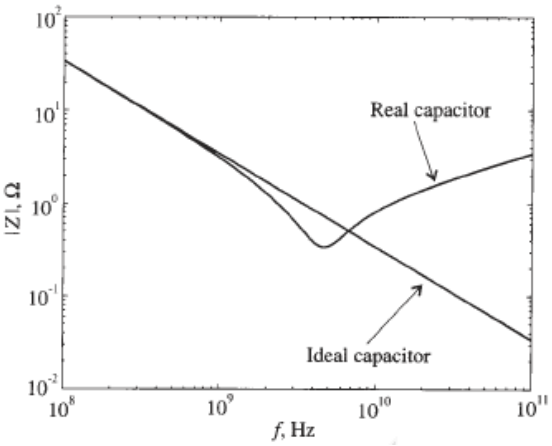

Figure 18 Impedance Response of a capacitor [5]

In modeling these components in ADS 2009 for frequencies up to 6 GHz, their S-Parameters will be used. For wide band frequencies the equivalent Spice model can be used. The Spice model represents an added level of complexity. However, it provides a good model for the component, especially at higher frequencies.

2.10 Printed Circuit Board

The board material FR-4 is a grade designation assigned to glass-reinforced epoxy laminate sheets, tubes, rods and PCBs. It stands for Flame Retardancies and the 4 is a #4 epoxy. Most of the PCBs are produced using FR-4. A thin layer of the copper foil is laminated on an FR-4 glass epoxy panel. FR-4 copper-clad sheets are fabricated with circuitry etched into copper layers to produce PCBs. FR-4 features high flexural, impact, high mechanical strength, light

weight, resistance to moisture and bond strength at temperatures up to 130 °C. The PCB material selected for our project will be an FR-4 PCB. [23]

Figure 19 shows the scaled assembly drawing of the FR-4 PCB we will be using to test our matching network. The SKY67003 LNA is placed on the center of the PCB. To the left of the LNA is the input matching network and to the right is the output matching. As shown in the layout, the input matching is limited to two series components and three shunt components. The output matching is limited to two series components and one shunt components. One of the important steps prior to implementing our design is simulations. In order to get the best results from the simulation, lengths of the individual microstrip lines are required. Once the board layout is open in ADS, we are able to calculate the distance of all microstrip lines on the PCB. The top of the figure is where the DC supply, V_{dd} and ground, will be connected. The RF_{In} signal will be received at the left and the amplified RF_{out} signal will leave at the right. The SKY67003 LNA will be soldered in the center of the figure. The matching components and bias components will be soldered on the appropriate sections from M1 through M18.

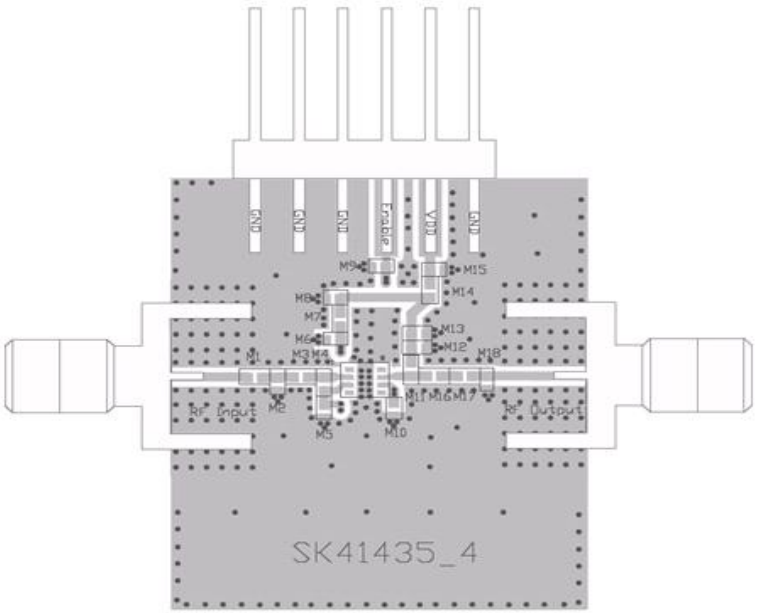

Figure 19 RF-4 PCB layout from Skyworks Solutions, Inc.

3 Project Statement and Objectives

The LNA is a critical functional block at the front end of the signal receiver chain in cellular base stations. Receiving multiple signals at different power levels over different frequency ranges places severe requirements on the performance for noise and linearity. Therefore, given today's market demands and state-of-the-art amplifier design principles, the objective of this project is to design and test application circuitry for a cellular-base station 4G receiver chain, using the SKY6700 series LNAs from Skyworks Solutions, Inc.

The SKY67003 LNA is optimized for a frequency of 2.6GHz with input matching, output matching and bias networks. The requirement for our project is to achieve a similar performance when the frequency of operation is increased to 3.3 to 3.6 GHz. Since the frequency is changing, the values for the maximum gain, optimum IIP3 and Γ_{opt} are different. This means that matching and bias networks for the LNA will have to be redesigned. An added complication of designing these networks is that as the frequency of operation increases the parasitic effects of the components used in these networks play a more dominant effect. The parasitic effects restrict the choice of components to those with a high quality factor.

The LNA is used in a base station the signal performance of the device is a higher priority as opposed to its power consumption. The key considerations for our design are shown in Table 1.

Table 1 Targeted RF and DC specifications

Specification	Minimum	Typical	Maximum
Supply Voltage		5V	
Supply Current	90mA		100mA
Frequency	3.3 GHz		3.6 GHz
S_{11}			-16 dB
S_{12}			-29 dB
S_{21}	15 dB		
S_{22}			-10 dB
IIP3	21 dBm		
IP1	5 dBm		
Stability (μ & μ1)		> 1	
Noise Figure			1.4 dB

The design will be simulated using ADS 2009 and implemented on the SKY67101 Evaluation Board. The performance of the final design will go through a series of tests and measurements for verification. The data from these measurements will be recorded, documented, and compared to the theoretical and simulated predictions.

4 Simulation for LNA 2.6 GHz configuration

In order to translate the 2.6 GHz matching network design into the 3.5 GHz matching network we need to understand how well the simulation results of the 2.6 GHz matching network reflect those that are measured. Therefore, the SKY67003 LNA was initially simulated for its previous match of 2.6 GHz. The simulation is broken down into the narrowband response and broadband response. The narrowband response runs from 0 to 6 GHz and the broadband response runs from 0 to 20 GHz. There are 3 different types of simulations performed: S-Parameter simulation, DC simulation, and Harmonic Balance Simulation. The simulation was done using lumped components, manufacturer component libraries (Murata Library, Panasonic Library, Coilcraft Library and TDK Library) and Murata calculator for equivalent circuits for each component.

4.1 Input and output matching circuit for 2.6GHz

Three different circuit schematics will be discussed in this section for the SKY67003 2.6 GHz matching network design. The need for having 3 different schematics is to understand how accurate the circuit results are with the measured results. All the circuits' components have the same uniform naming scheme consistent with the layout board explained in the background section and are numbered from M1 through to M18.

4.1.1 Bill of Material for 2.6 GHz matching circuit

Table 2 summarizes the bill of material (BOM) for 2.6 GHz matching circuit design.

Table 2 BOM for 2.6GHz matching circuit

Component	Type	Value	Size	Manufacturer
M1	Resistor	0Ω	0402	Panasonic
M2	Inductor	2nH	0402	Coilcraft HP
M3	Capacitor	1.6pF	0402	Murata GJM
M4	Inductor	15nH	0402	Coilcraft HP
M5	Capacitor	6pF	0402	Murata GJM
M6	Not Included			
M7	Resistor	5.6kΩ	0402	Panasonic
M8	Capacitor	1000pF	0402	Murata GRM
M9	Not Included			
M10	Resistor	0Ω	0402	Panasonic
M11	Inductor	39nH	0402	TDK MLG
M12	Capacitor	10pF	0402	Murata GRM
M13	Capacitor	1000pF	0402	Murata GRM
M14	Resistor	0Ω	0402	Panasonic
M15	Capacitor	0.1µF	0402	Murata GRM
M16	Capacitor	2.2pF	0402	Murata GRM
M17	Resistor	0Ω	0402	Panasonic
M18	Inductor	1.7nH	0402	TDK MLG

4.1.2 Lumped Component Circuit for 2.6 GHz

The circuit in Figure 20 shows the 2.6 GHz lumped circuit employed in the SKY67003 datasheet. The circuit does not contain any of the microstrips which are on the layout board. The need for this is to understand the effect of the microstrip lines present on the board. Furthermore, the use of lumped components as opposed to actual component parameters shows how the results deviate due to the component parasitics.

The circuit schematic in Figure 20 displays the initial matching and bias configuration using lumped components. The lumped model simplifies the behavior of spatially distributed physical systems into a topology consisting of discrete entities that approximate the behavior of

the distributed system under certain assumptions. This assumption here is that the length of the circuit is less than the circuit's operating wavelength. The box in the middle of the circuit schematic is the Skyworks Solutions, Inc. Black Box model. The Black Box is a distributed model of the SKY67003 LNA. The lumped components will be later replaced with the more accurate distributed model available from the manufacturer.

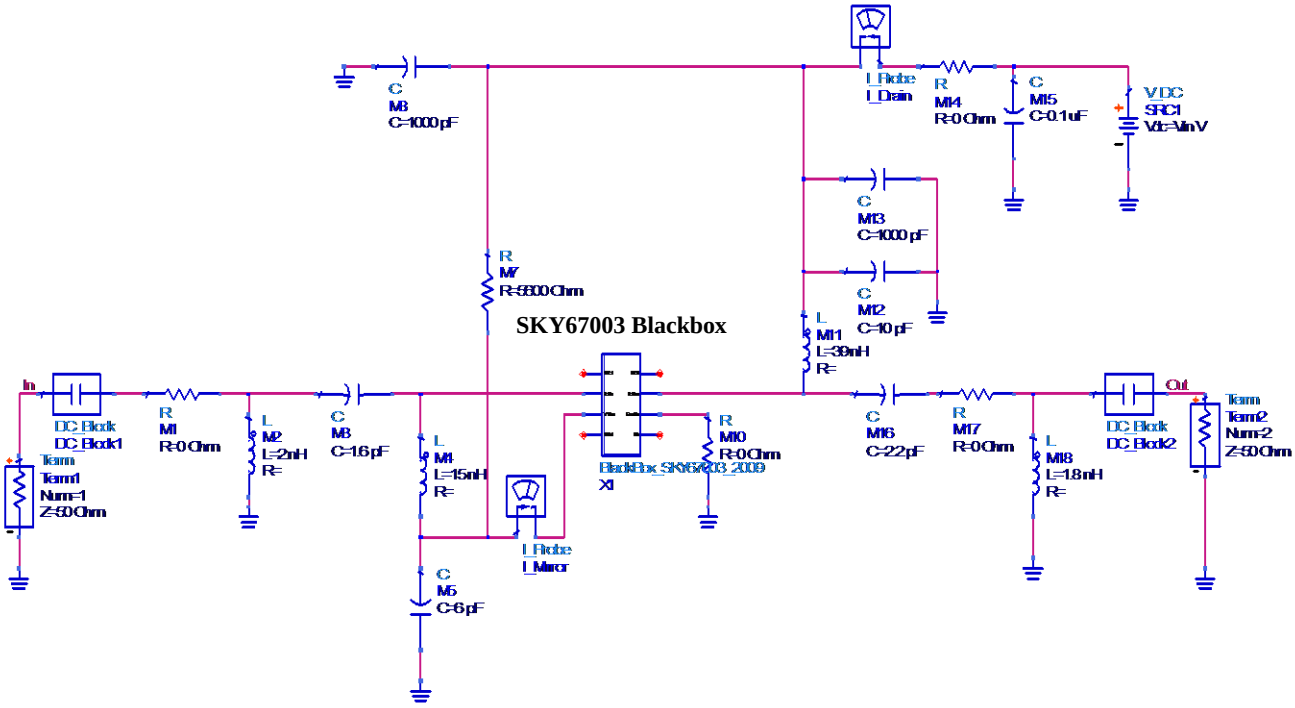

Figure 20 Simulation using lumped components

4.1.3 Narrowband Circuit Schematic for 2.6 GHz

The circuit in Figure 21 Simulation using manufacture components has the manufacturer component libraries included. This enables us to simulate the actual component characteristics as well as the effects of parasitics. The box in the middle is again the Skyworks Solutions, Inc. Black Box model. The circuit also has the equivalent microstrips and vias calculated from the Gerber files of the layout board. Microstrips are electrical transmission lines which can be fabricated using printed circuit board technology. They are widely used in microwave and radio

frequency circuits. They are made of a conducting strip separated from a ground plane by a dielectric layer known as the substrate. Vias are vertical connections between the different layers on the printed circuit board. The Gerber format is a file format used by the printed circuit board (PCB) industry software to describe the images of a printed circuit board. The manufacturer libraries used were the Murata Libaries, Coilcraft Libraries, TDK Libraries and Panasonic Libraries. The manufacturer libraries are only valid up to 6 GHz. Beyond 6 GHz, ADS extrapolates the data in the libraries and the results are no longer accurate. The simulated results will then be compared to the results on the datasheet.

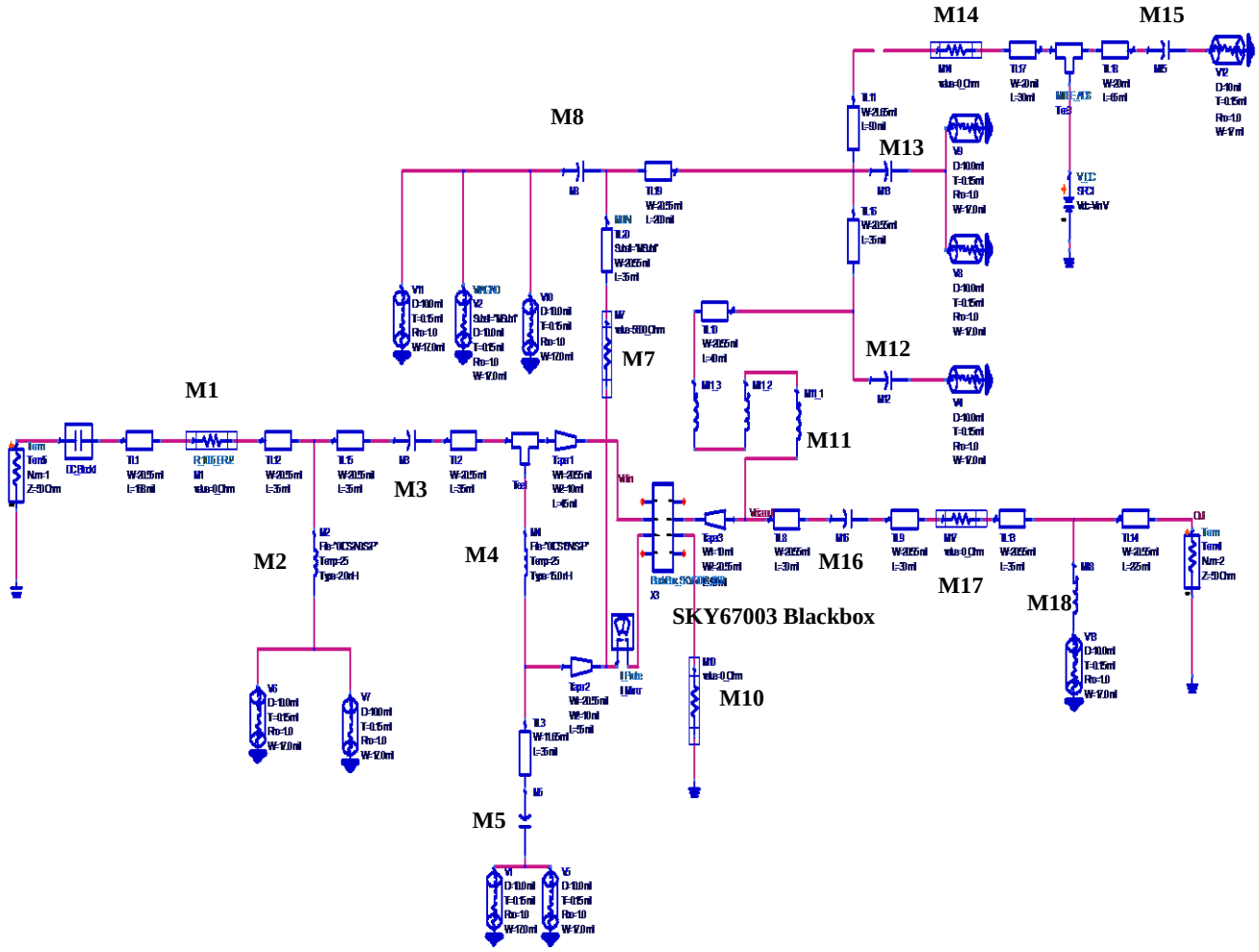

Figure 21 Simulation using manufacture components

4.1.4 Broadband Circuit Schematic for 2.6 GHz

Figure 22 shows the broadband circuit for the 2.6 GHz simulation. In order to simulate the circuit accurately up to 18 GHz the Murata Component Website has a calculator which gives the equivalent circuit schematic for each component. This will enable us to obtain an accurate view of the circuit behavior up to 18 GHz to make sure the circuit is also stable at harmonics of the fundamental frequencies that we are interested in. The reason the circuit has to be simulated to such a high frequency is because Skyworks Solutions, Inc. requires the LNA to be unconditionally stable up to 18 GHz. The circuit has the equivalent microstrips and vias calculated from the Gerber files of the layout board.

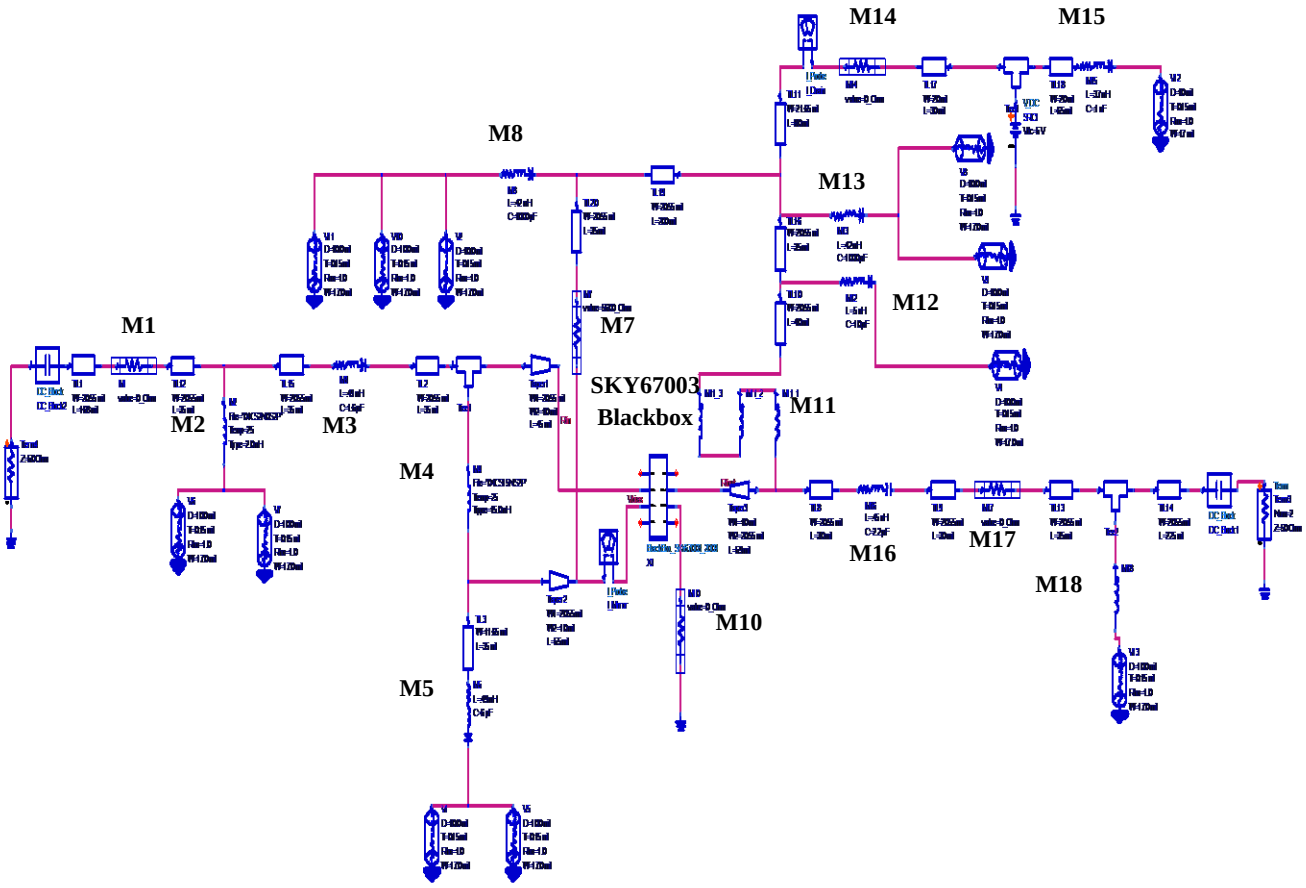

Figure 22 Simulation using RF equivalent components

4.2 Simulation Results for 2.6 GHz matching circuits

The simulation results for the 2.6 GHz matching circuits is shown in this section. The simulation results are broken down into DC simulation, S-Parameter Sweep and Harmonic Balance Simulation.

4.2.1 DC Simulation

The DC simulation consists of sweeping the input voltage from 3 to 5V and graphing the drain current. Figure 23 shows the drain current for the lumped component circuit, narrowband circuit and broadband circuit, respectively. The lumped circuit has a drain current of 87.5 mA. The narrowband and broadband circuits show that the drain currents are in the range of 90-100mA, which matches the measured results.

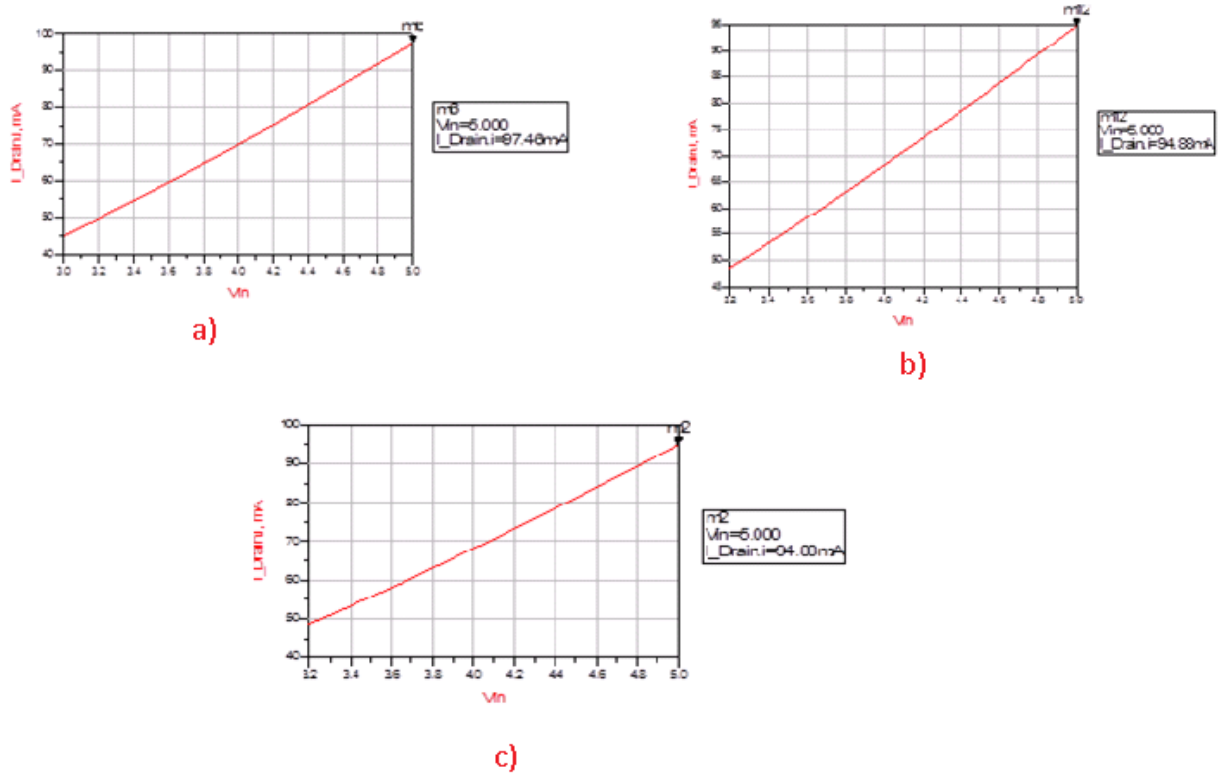

Figure 23 DC Bias Simulation: a) Lumped Circuit b) Narrowband Circuit c) Broadband Circuit

4.2.2 S-Parameter Sweep

The following graphs detail the results from the S-Parameter sweeps for the lumped, narrowband and broadband circuits respectively.

Input Voltage Reflection Coefficient (S_{11}) for 2.6 GHz simulations

Figures 24 - 26 show the simulation results for S_{11} for the 2.6 GHz lumped, narrowband and broadband circuits respectively. The graphs show the magnitude response on rectangular chart, and the normalized input impedance and S_{11} on the Smith Chart.

For the lumped circuit the magnitude of S_{11} is 0.624 which is equal to -4.096 dB at 2.6 GHz. The Smith Chart for the lumped circuit shows that S_{11} is not matched for 2.6 GHz.

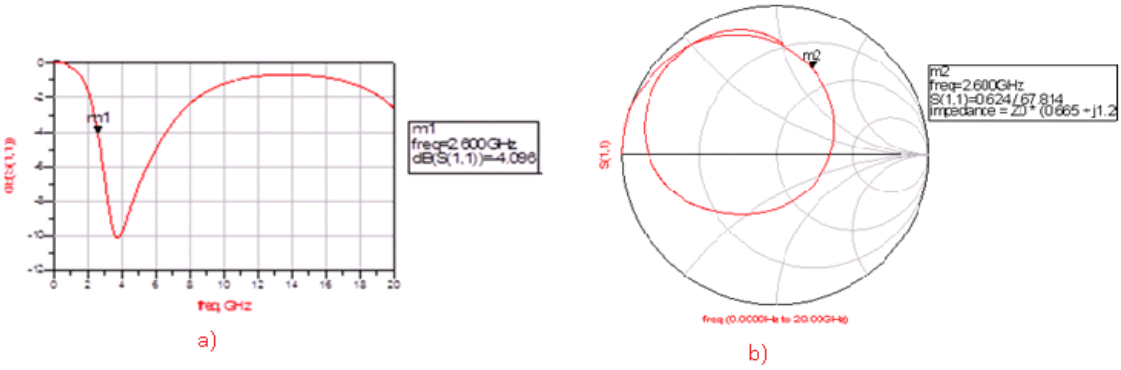

Figure 24 S_{11} for Lumped Component 2.6 GHz matching circuit: a) Rectangular Chart b) Smith Chart

The narrowband circuit has an S_{11} with a magnitude of 0.039 which is equal to -28 dB at 2.6 GHz, as seen in Figure 25. The Smith Chart shows that at this frequency the input matching circuit is well matched at 2.6 GHz.

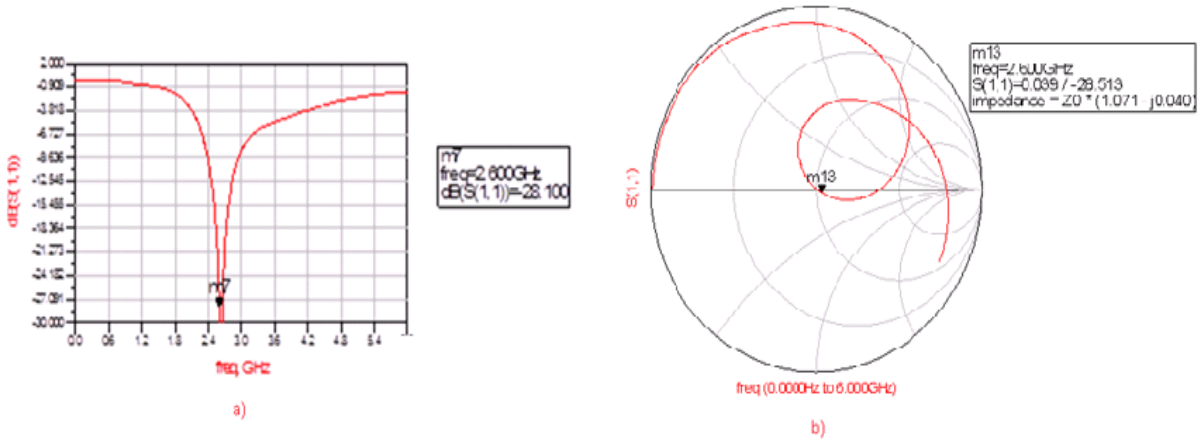

Figure 25 S_{11} for narrowband circuit 2.6 GHz matching circuit: a) Rectangular Chart b) Smith Chart

The broadband circuit response for S_{11} is shown in Figure 26. S_{11} has a magnitude of 0.097 at 2.6 GHz which is equal to -20.282 dB. This shows that S_{11} is well matched for 2.6 GHz. However the broadband circuit shows that magnitude response is not as good as that shown in the narrowband circuit response for S_{11}.

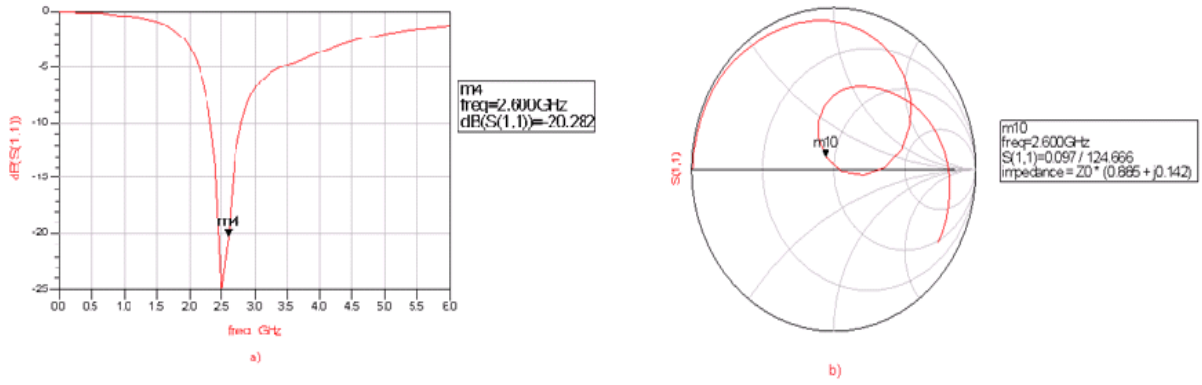

Figure 26 S_{11} for broadband circuit for 2.6GHz matching circuit: a) Rectangular Chart b) Smith Chart

Reverse Isolation (S_{12}) for 2.6 GHz Simulations

Figure 27 shows the S_{12} simulations for the 2.6 GHz lumped, narrowband and broadband circuits respectively. The lumped circuit has a reverse isolation of -38 dB. The narrowband circuit and broadband circuit have a reverse isolation of -33 dB. All the circuits show that there is

hardly any reverse feedback in the circuit so we can assume a unilateral assumption when designing the 3.5 GHz circuit.

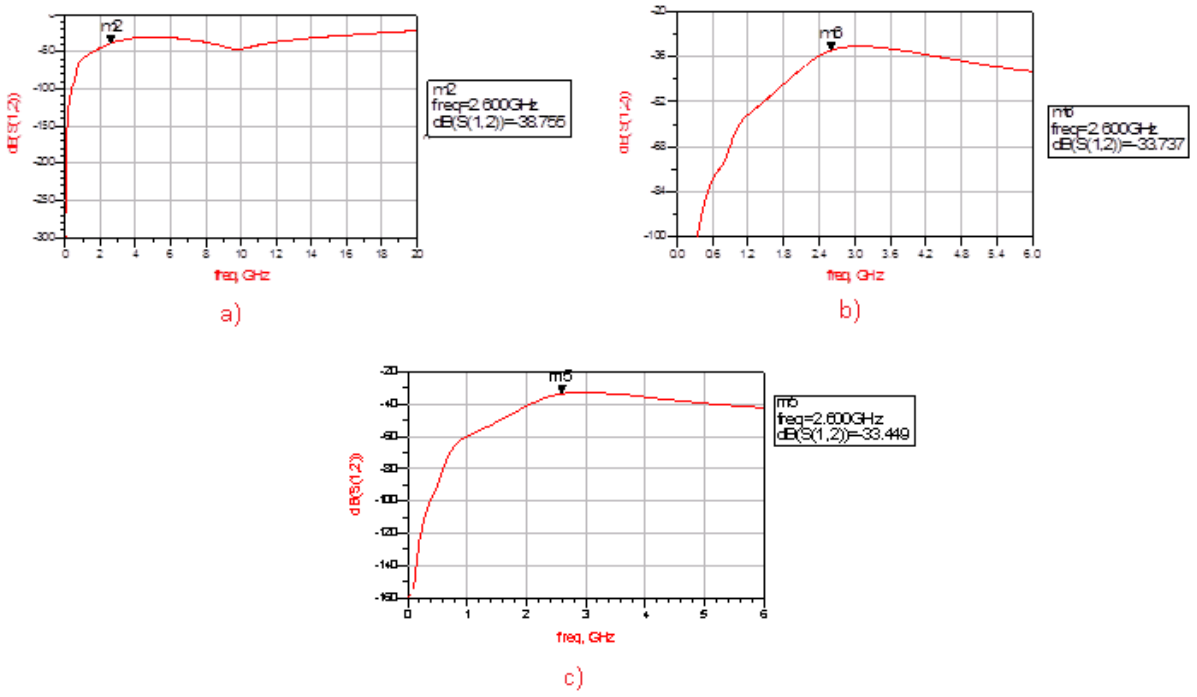

Figure 27 S_{12} for 2.6 GHz: a) Lumped Circuit b) Narrowband Circuit c) Broadband Circuit

Forward Voltage Gain (S_{21}) for 2.6 GHz Simulations

Figure 28 shows the S_{21} for the lumped, narrowband and broadband 2.6 GHz matching circuit respectively. The lumped circuit has a gain of 12.6 dB at 2.6 GHz while the narrowband circuit and broadband circuits have a gain of 17 dB. The S_{21} response is similar for the narrowband and broadband circuits while it is very different from the lumped circuit.

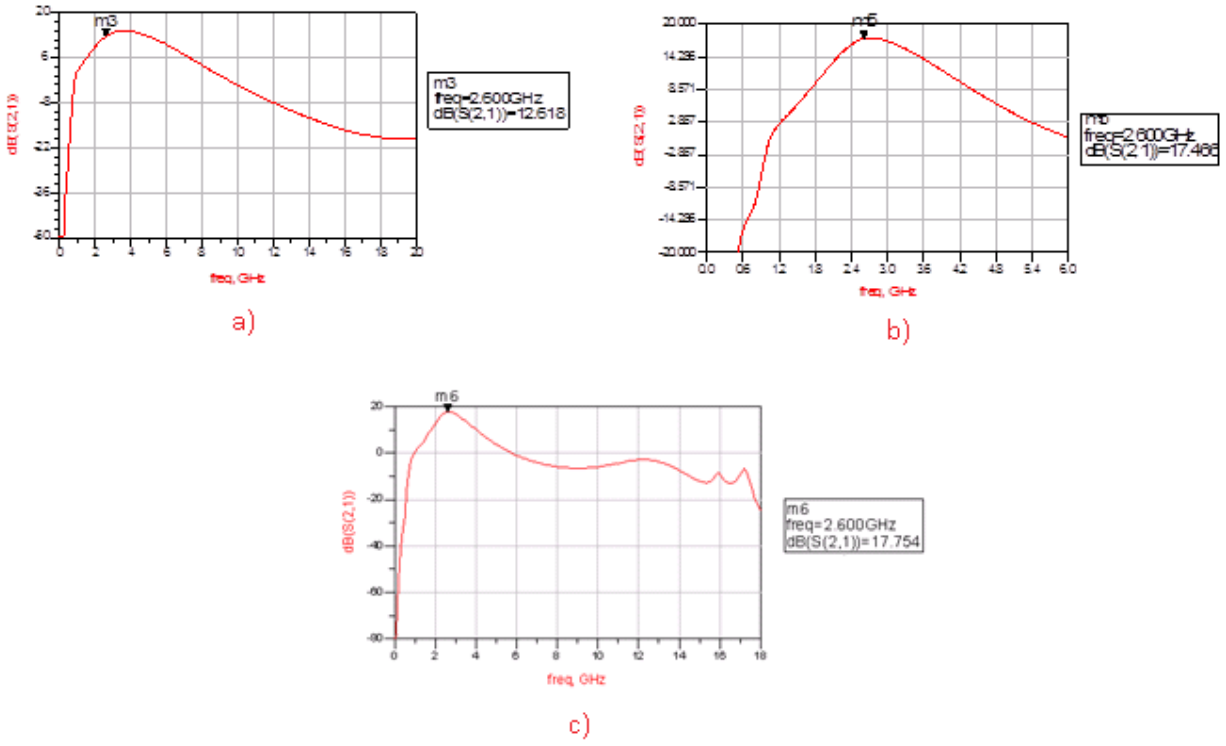

Figure 28 S_{21} for 2.6 GHz a) Lumped Circuit b) Narrowband Circuit c) Broadband Circuit

Output Voltage Reflection Coefficient (S_{22})

Figures 29 - 31 show the S_{22} simulation results for the 2.6 GHz lumped components, narrowband and broadband circuits respectively. The results contain the magnitude on a rectangular chart, and the normalized impedance and S_{22} on the Smith Chart.

The S_{22} of the lumped circuit has a magnitude of 0.845 which is equal to -1.467 dB at 2.6 GHz. This shows the reader that lumped circuit is not well matched for 2.6 GHz.

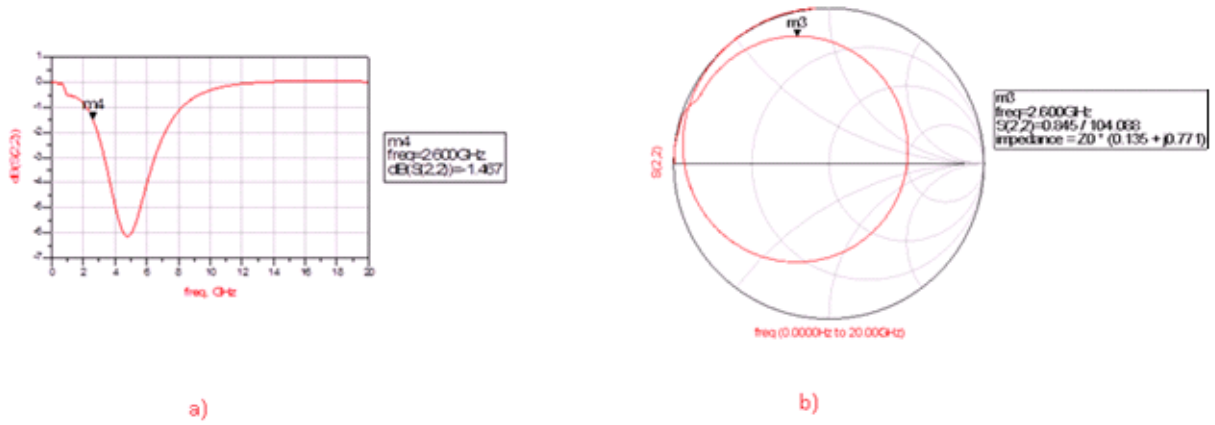

Figure 29 S_{22} for the lumped component 2.6GHz matching circuit: a) Rectangular Chart b) Smith Chart

The narrowband circuit shows that the magnitude for S_{22} is 0.468 which is equal to -6.588 dB at 2.6 GHz. The Smith Chart and the rectangular chart suggest that the output matching circuit is matched for 3.2 GHz rather than 2.6 GHz.

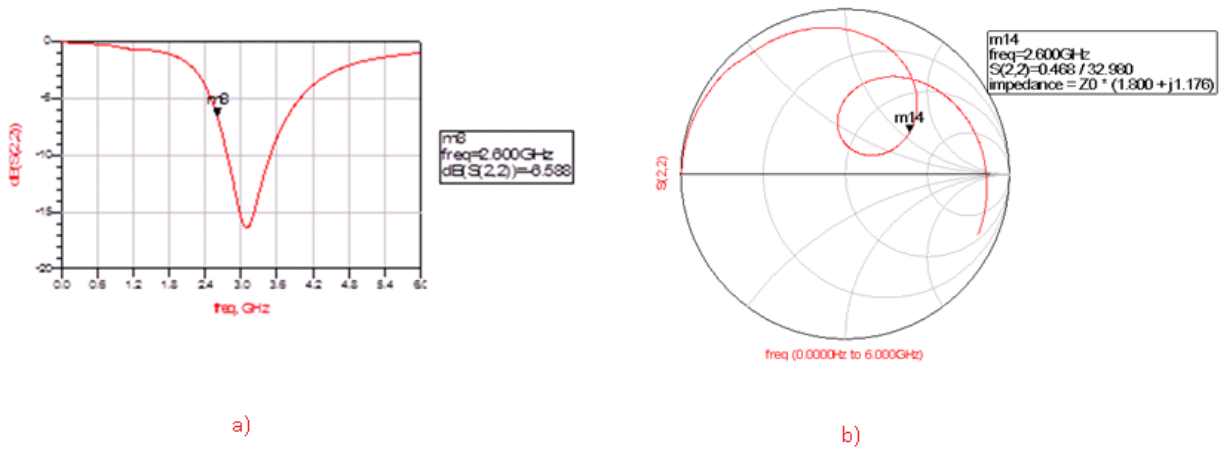

Figure 30 S_{22} for the narrowband 2.6GHz matching circuit: a) Rectangular Chart b) Smith Chart

The magnitude response of S_{22} for the broadband circuit response is 0.411 which is equal to -7.7 dB. The magnitude response and the Smith Chart show that the output matching circuit is matched for 3.2 GHz rather than 2.6 GHz. This response for S_{22} is similar to that of S_{22} in the narrowband circuit.

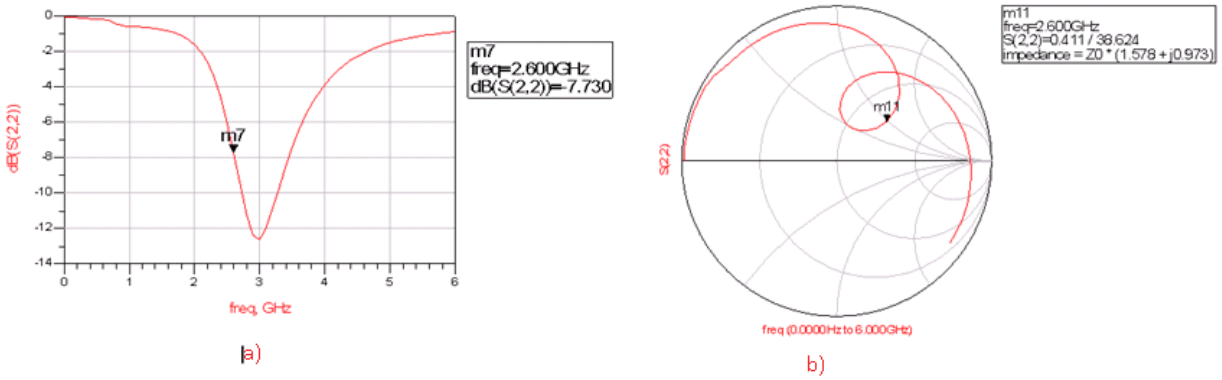

Figure 31 S_{22} for the broadband 2.6GHz matching circuit: a) Rectangular Chart b) Smith Chart

Stability

Figures 32 – 34 show the Stability graphs for the 2.6 GHz lumped component, narrowband and broadband circuits. The graphs shown for each circuit are: the stability factor (K), the stability measure (B), μ and μ'. The stability criteria for a circuit to be stable are shown in the background section.

The lumped component circuit and the broadband circuit show that the circuit becomes unstable after 10-12 GHz. The narrowband circuit is stable throughout its frequency range. This is because the narrowband circuit is simulated till 6 GHz.

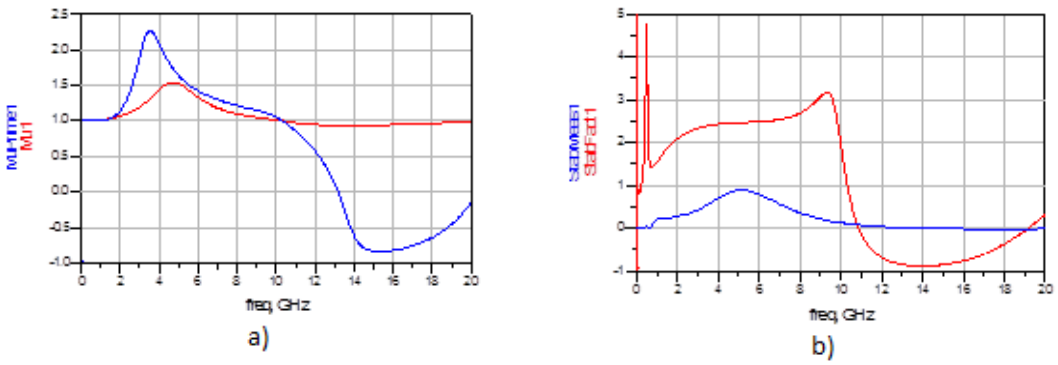

Figure 32 Stability for the lumped component 2.6GHz matching circuit: a) μ and μ' b) K and β

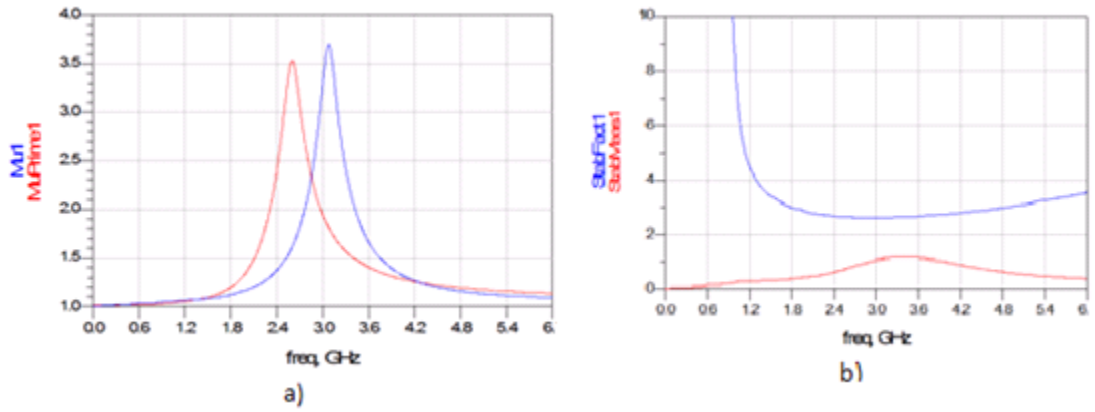

Figure 33 Stability for the narrowband 2.6GHz matching circuit: a) μ and μ' b) K and β

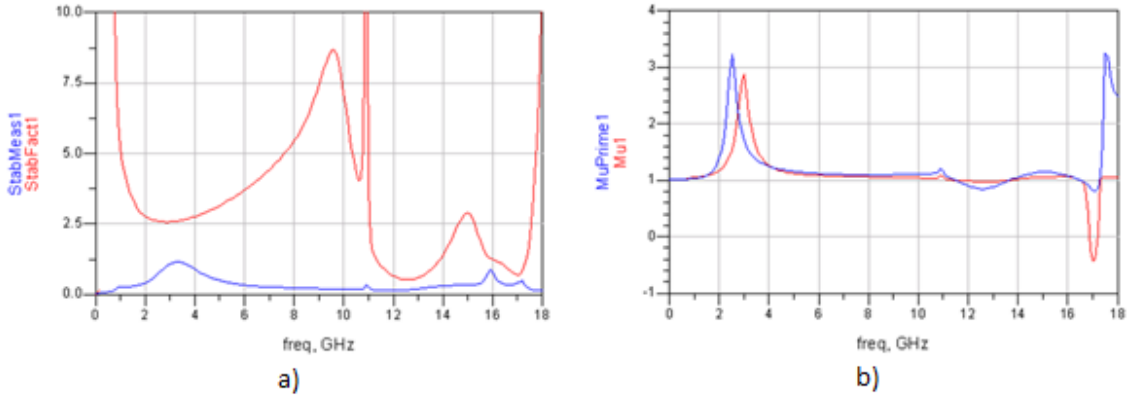

Figure 34 Stability for the broadband 2.6GHz matching circuit: a) K and β b) μ and μ'

Noise Figure

Figure 35 shows the graphs of the Noise Figure for the 2.6 GHz lumped component, narrowband and broadband circuits. The average Noise Figure for LNAs operating at this frequency is 1.5 dB. According to these lower values achieved for the Skyworks Solutions, Inc. LNA, this is a better product than other ones in the market for this requirement.

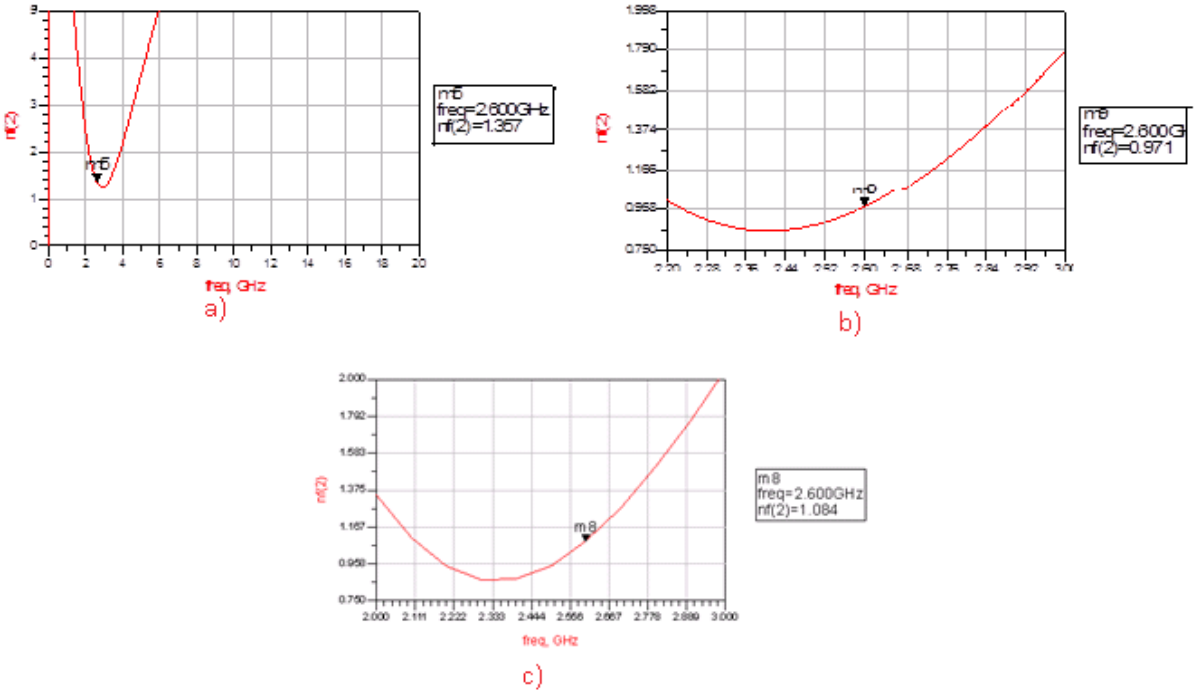

Figure 35 Noise Figure: a) Lumped circuit b) Narrowband circuit c) Broadband circuit

4.2.3 Harmonic Balance

The Harmonic Balance (HB) analysis is a nonlinear simulation in ADS which measures linearity parameters such as IP3 and P1dB. In this section, we will discuss some of the results from the harmonic balance simulation.

Tables 3 and 4 show the results of the IP3 points and P1dB, respectively. Table 3 shows that OIP3 for the 3 circuits vary within a range of 4 dBm whereas the IIP3 vary by 10 dBm. The narrowband and broadband circuits have a much lower IIP3 than the lumped circuit. A similar result is seen for IP1 where the lumped circuit has a much higher IP1 than the narrowband and broadband circuits.

Table 3 Third order intercept points

Parameter	Lumped Component Circuit (dBm)	Narrowband Circuit (dBm)	Broadband Circuit (dBm)
Third Order Input Intercept Point	22.253	14.852	12.679
Third Order Output Intercept Point	34.88	32.33	30.44

Table 4 1dB Gain Compression Point

Parameter	Lumped Component Circuit (dBm)	Narrowband Circuit (dBm)	Broadband Circuit (dBm)
1dB Input P1dB	9.0	0	-1.0
1dB Output P1dB	20.11	16.68	15.70

Figure 36 shows the gain compression graphs for the 2.6 GHz for the lumped component, narrowband and broadband circuits. The y-axis shows the gain in dB and the x-axis shows the output power in dBm. The figures highlight the results seen in Table 4. The lumped circuit has a higher OP1 dB than the narrowband and broadband circuits.

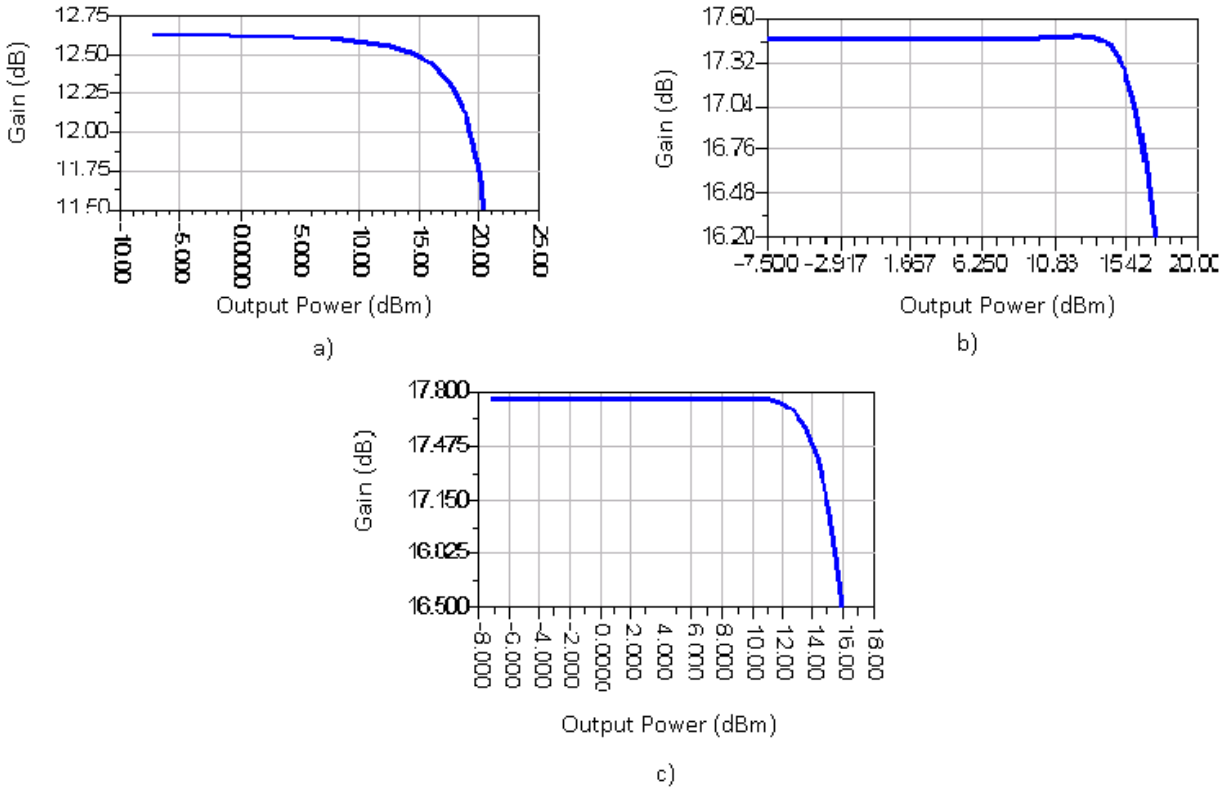

Figure 36 2.6 GHz Gain Compression for: a) Lumped Circuit b) Narrowband Circuit c) Broadband Circuit

4.2.3 Final Simulation Results Compared for 2.6 GHz

Table 5 shows the final simulated results along with the measured results of the LNA at 2.6 GHz. The simulation results show that the lumped component circuit results and the measured results do not match. This shows us that the parasitic behavior of the circuit components and the layout board characteristics play a significant role. It also shows that in future simulations the lumped schematic should not be used as they do not give an accurate match.

The other two circuit results show that they match the measured results quite well. They match particularly well for the narrowband circuit for S_{11}, S_{12}, S_{21}, Noise Figure and Stability Factor. However the results do not match for S_{22}, IP3 and P1dB. The measured results for these parameters are better than the simulated results. This shows us that the simulated linearity

parameters will be better when they are actually measured. The broadband circuit has similar results but for stability it deviates after 10-12 GHz.

The circuit simulation also showed the importance of inductors M4 and M11. M4 is the gate inductor and M11 is the drain inductor. They set the voltage bias at RF_{in} and RF_{out} respectively. They are also used as part of the input and output matching networks.

The three capacitors placed at the voltage supply are to filter out any high frequency fluctuations from the supply. The highest capacitor of 0.1 μF filters out low frequency fluctuations, the capacitor of 1000 pF is for mid-range frequencies and the capacitor of 10 pF is for very high frequencies. All three caps have a similar quality factor. For our design we may need to change the cap of 10 pF to a high Q component if the noise level is too high. If the noise level is acceptable it can remain a low Q component in order to save costs.

Table 5 WPI Simulation VS Skyworks Solutions, Inc. datasheet at 2.6GHz

Parameter	Test Condition	Lumped Circuit	Narrowband Circuit	Broadband Circuit	Measured Results			Units
					Minimum	**Typical**	**Maximum**	
Voltage		**5**	**5**	**5**		**5**		**V**
Current		**97.46**	**94.88**	**94.88**	**90**		**100**	**mA**
S_{11}	**@ 2.6 GHz**	**-4.096**	**-28.100**	**-20.82**	**-12.5**	**-14.5**		**dB**
S_{22}	**@ 2.6 GHz**	**-1.467**	**-6.588**	**-7.730**	**-14**	**-17**		**dB**
S_{21}	**@ 2.6 GHz**	**12.618**	**17.466**	**17.754**	**16.5**	**17.5**	**18.5**	**dB**
S_{12}	**@ 2.6 GHz**	**-38.755**	**-33.737**	**-33.349**	**-27**	**-30**		**dB**
Third Order Input Intercept Point	**@ 2.6 GHz, Δf=1MHz, Pin=-20dBm/tone**	**34.88**	**14.852**		**37.5**	**39.0**		**dBm**
Third Order Output Intercept Point	**@ 2.6 GHz, Δf=1MHz, Pin=-20dBm/tone**	**22.265**	**32.33**		**20.0**	**21.5**		**dBm**
Noise Figure	**@ 2.6 GHz**	**1.375**	**0.971**	**1.084**		**0.88**	**1.10**	**dB**
Stability		**>1 upto 10GHz**	**>1**	**>1 upto 10GHz**		**>1 upto 18GHz**		**N/A**
Output P1dB	**@ 2.6 GHz**	**20.11**	**16.68**		**18.7**	**19.7**		**dBm**
Input P1dB	**@ 2.6 GHz**	**9.0**	**0**		**2.2**	**3.2**		**dBm**

4.3 Mismatch between 2.6 GHz and 3.5 GHz

Apart from understanding the 2.6 GHz matching circuit and layout, one of the main reasons for simulating the 2.6 GHz circuit is to see how well the circuit performs at 3.5 GHz. If the circuit meets the design targets set out in the objective section, then there is no need to design another matching network. However, if it does not meet them, there is a need to redesign the matching networks and bias networks.

S_{11} Mismatch

Figure 37 shows the difference between S_{11} at 2.6 GHz and 3.5 GHz. At 2.6 GHz S_{11} is -20.82 dB and at 3.5 GHz it is -4.771dB. The required target for S_{11} at 3.5 GHz is a maximum of -16 dB. The 2.6 GHz matching network is over 10dB less than the required maximum.

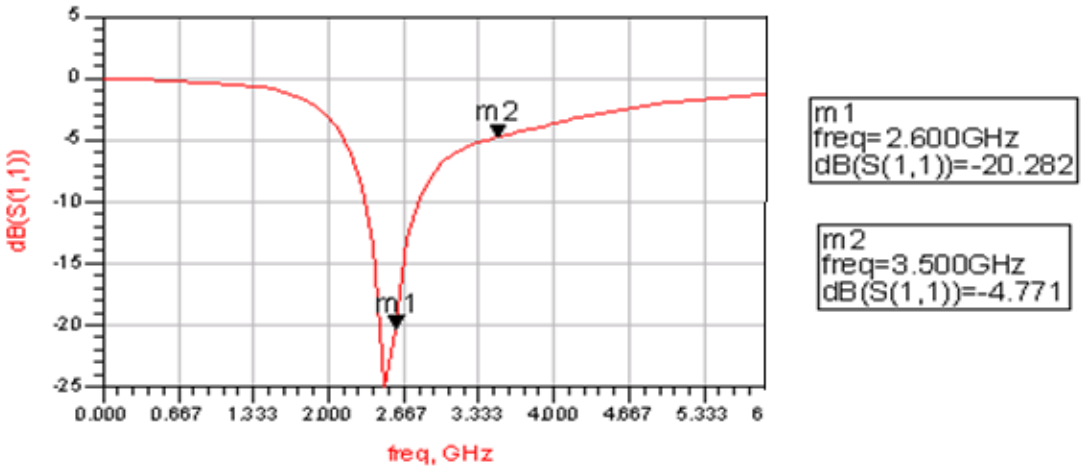

Figure 37 S_{11} Mismatch

S_{22} Mismatch

Figure 38 shows S_{22} with the 2.6 GHz matching circuit. At 3.5 GHz it is -7.4dB. The required design target for 3.5 GHz is a maximum of -10 dB. Therefore the 2.6 GHz circuit is off by 2 dB to meeting the design target.

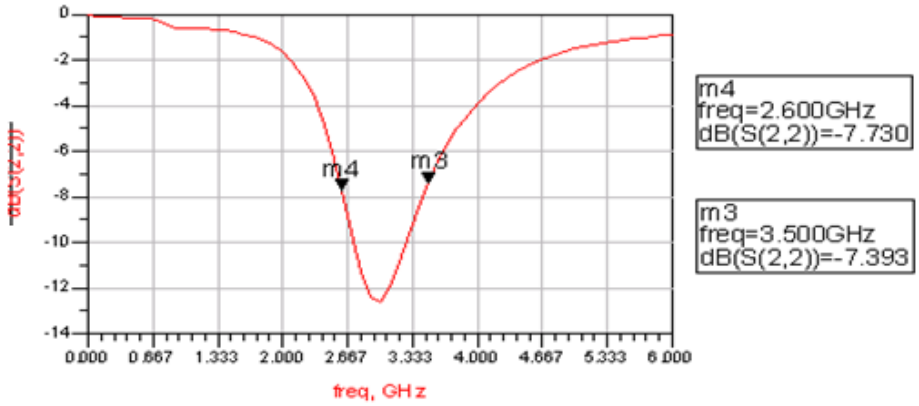

Figure 38 S_{22} Mismatch

S_{21} Mismatch

Figure 39 shows the small signal gain for the 2.6 GHz matching network circuit. At 3.5 GHz the gain is 13.68 dB. The design target for the small signal gain is a minimum of 15 dB. Therefore the small signal gain is 1.5 dB away from its target.

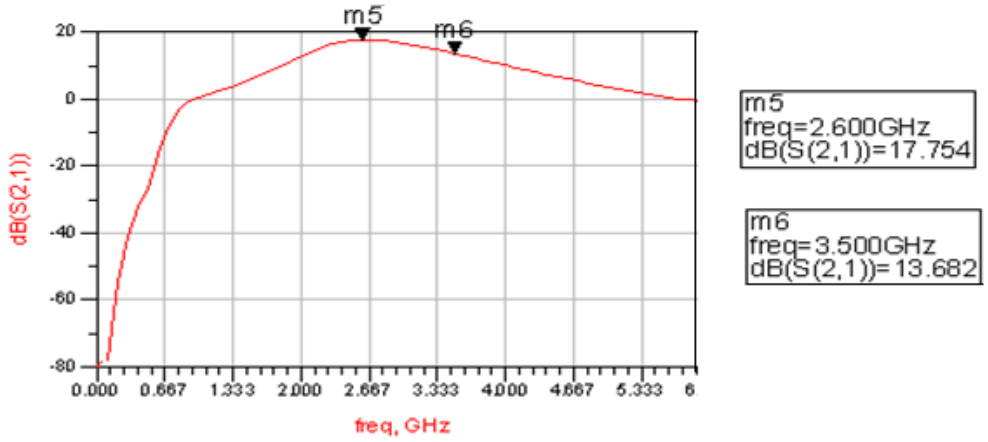

Figure 39 S_{21} Mismatch

Noise Figure Mismatch

Figure 40 shows the Noise Figure simulated with the 2.6 GHz matching circuit. At 3.5 GHz the Noise Figure is 3.239 dB. The design target for the Noise Figure is a maximum of 1.4 dB. Therefore the 2.6 GHz circuit deviates from the target by more than 1.8 dB.

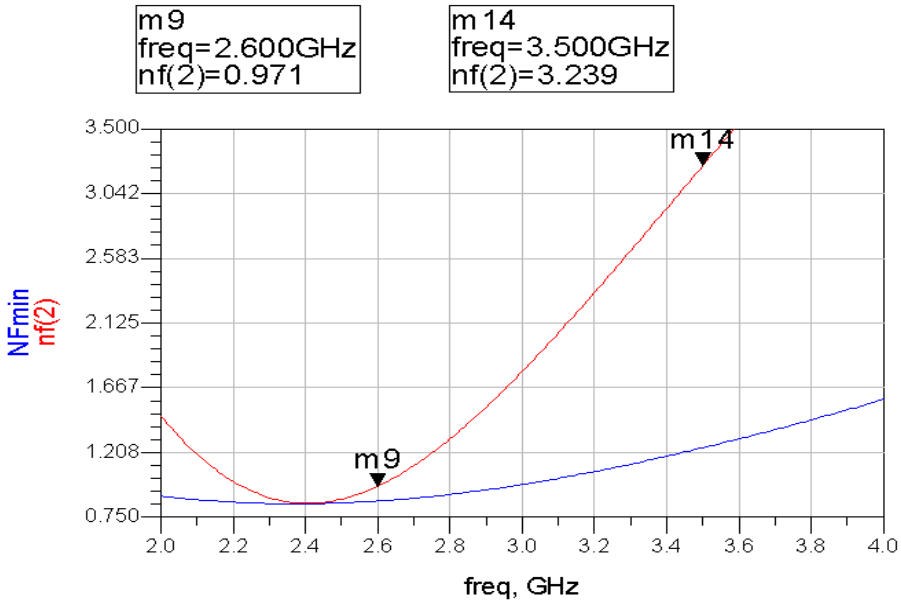

Figure 40 Noise Figure Mismatch

All these results show that the 2.6 GHz matching network fails to meet the needs of an LNA operating at 3.5 GHz. Therefore a new design is needed.

5 Approach

An approach is needed in order to find a matching solution for the SKY67003 amplifier. The first step involves breaking down the problem into different sections which can be tackled separately. This is outlined in the system block diagram section. The next step involves finding a viable solution for each section through simulations. This is outlined in the simulation approach. The next step is to test the simulation findings on the layout board and tune the device according to the experimental findings. This is outlined in the experimental approach section.

5.1 System Block Diagram

The first step to developing a 3.5 GHz solution involves breaking down the problem into different sections. A system block diagram enables us to do this. Even though all the sections affect each other, we assume a unilateral configuration which allows us to address each block independently. Figure 41 shows the generic system block diagram for the project. The input matching stage, the output matching stage and the bias circuitry will be designed for the LNA. The signal entering into the LNA RF_{in} will go through our input matching circuit before reaching the Cascode LNA provided by Skyworks Solutions, Inc. The amplified signal coming out from the LNA will go through the output matching circuit. A bias circuitry will be necessary, if the bias point for the LNA, V_{bias}, needs to be changed for the operating frequency of 3.5 GHz. The Miller effect is the effective multiplication of impedance across an amplifier. At low frequencies of operation the Miller effect is desired because it creates a low frequency cut off and therefore reduces instability by increasing the phase margin. At higher frequencies, this is undesired because it limits the slew rate of an amplifier and limits the available gain. As the SKY67003 is a cascode amplifier, the Miller Effect is very small. Therefore, there is hardly any feedback from the output to the input. This means that the reverse voltage gain is very small and a unilateral approach can be used to design the matching network.

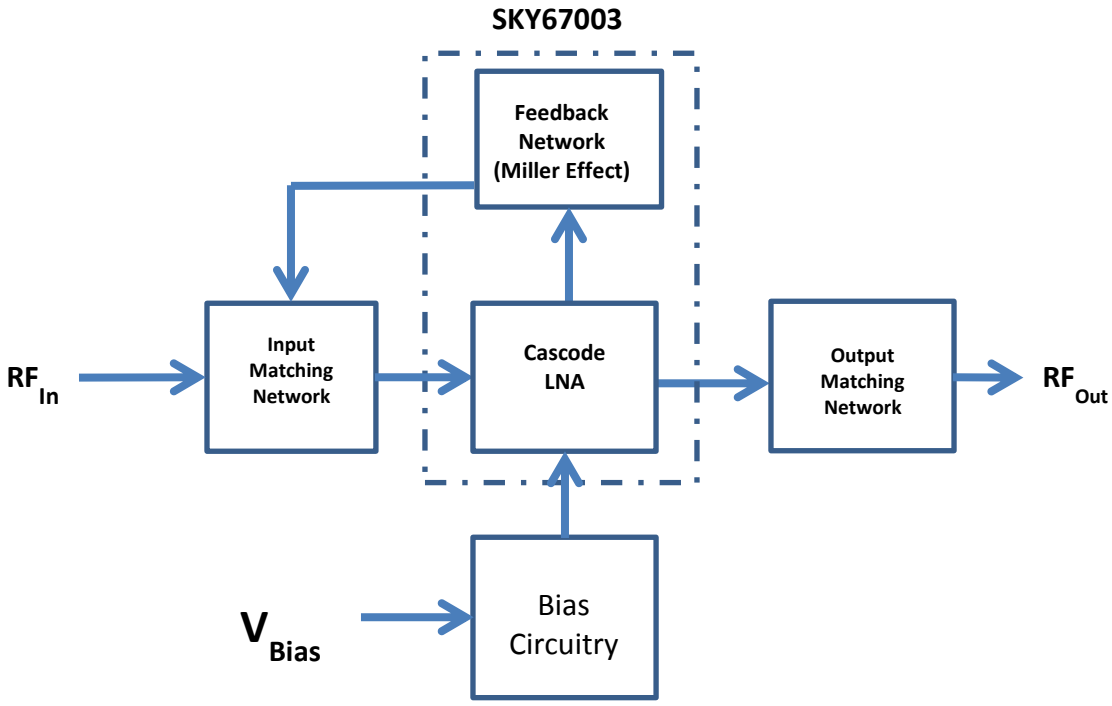

Figure 41 System block diagram

5.2 Simulation Approach

As discussed in the background section, this project will use ADS as the simulation environment. The simulation encompasses importing the Skyworks Solutions, Inc. layout of the LNA's S-Parameters and Evaluation board into ADS and converting the layout into a corresponding schematic. This schematic will be used to simulate all the tests described above. The matching network will be configured for 3.5 GHz and the tests described below will be performed. This phase will be repeated until the required objectives described above are obtained. [26]

5.2.1 Skyworks Solutions, Inc. LNA Modeling Options

There are several different methods of modeling the SKY67003. This ranges from S-Parameter Files to a Black Box Model Provided by Skyworks Solutions, Inc. Each method has its own advantages and disadvantages as well as complexity. The Skyworks Solutions, Inc. Black

Box model is the model that will be used most frequently for simulations. It includes the same model used by designers at the initial design stage. It is also most flexible for simulation as it allows simulation for DC bias, S-Parameters, IP3 , P1dB, Noise Figure and EM simulations. [1]

Table 6 shows the different modeling options available and their associated advantages and disadvantages. The table shows that there are 4 different available options to simulate the SKY67003 LNA. Only the Black Box model allows for the bias voltage to be changed. Furthermore, it is easy to simulate and provides a good representation of the amplifier behavior at higher frequencies. Therefore most of the simulations will be done using the Black Box model. In order to characterize the LNA at 3.5 GHZ the Deembedded S-Parameters will be used.

Table 6 Skyworks Solutions, Inc. LNA Modeling Methods

Model	Advantages	Disadvantages	Availability
S Parameter File	• Quick • Linear Simulations	• Not most accurate • No nonlinear simulations • 2 Ports only • Fixed Bias	Early
Black Box	• Flexible Bias • Flexible feedback • Linear and non-linear simulation	• Not most accurate • Fitted to application data • Platform Specific	1st Fabrication Run
Deembedded S-Parameters	• Measured • Good Accuracy • Linear Simulation	• 2 Ports only • Fixed Bias • Fixed Feedback • Time Consuming	1st Production Run
Load-Pull Contours	• Measured • Best Accuracy • True non-linear data	• 2 ports only • Fixed Bias • Fixed Feedback • Time Consuming • Difficult to simulate	1st Production Run

5.2.2 Scattering Parameter Sweep Simulation

The S-Parameter simulation from ADS sweeps the frequency of the device under test from a start to end frequency and calculates the S-Parameters for the device. The simulation is performed by putting 50 Ω terminations at all ports. The S-Parameter palette also enables you to calculate the gain, Noise Figure and stability circles. Furthermore, the S-Parameter palette has components to simulate for good DC to RF separation. This includes DC blocking capacitors and RF chokes. [27]

5.2.3 Harmonic Balance Simulation

The HB analysis is a non-linear, frequency-domain, steady-state simulation. The voltage and current sources create discrete frequencies resulting in a spectrum of discrete frequencies at every node in the circuit. HB simulations will be used to compute quantities such as IP3 and the P1dB. To perform an HB simulation, one or more fundamental frequencies and the order of each fundamental frequency need to be specified. HB simulation enables the multi tone simulation of circuits that exhibit intermodulation frequency conversion.

The HB method is iterative: it is based on the assumption that for a given sinusoidal excitation there exists a steady-state solution that can be approximated to satisfactory accuracy by means of a finite Fourier series. The circuit node voltages take on a set of amplitudes and phases for all frequency components. [28]

To calculate the P1dB point of the amplifier, the simulator sweeps the input power upward from a small value, and when the required amount of gain compression is seen at the output, the analysis is complete. A single tone harmonic balance simulation applies a single tone to the amplifier and finds the input and output power when the difference between the idealized linear power-gain slope and the corresponding point on the actual power curve is 1 dB.

Intermodulation distortion is one of the key design requirements of radio frequency circuits. The standard approach for analyzing distortion using circuit simulators is to mimic measurement environments and compute the response due to a two-tone input. When the input power drives the non-linear device into saturation or distortion, third order products near the desired frequency can become large. The point at which 3rd order products intercept the linear rise in output power is the IP3. IP3 equations will be used to find the input and output third-order intercept point. [29]

5.2.4 Tuning in Advanced Design System

Advanced Design System's tuning capabilities enable changing one or more design parameter values to quickly see its effect on the output without re-simulating the entire design. This helps to find the best results and the most sensitive components or parameters more easily. When analyzing a network, a considerable amount of information is compiled by the simulator prior to the actual network simulation. The simulator must set up the network topology, load all the values of the component parameters, and organize the measurement requests. The tuning capability in ADS allowed for a relatively short development time and better understanding of the finer details of the matching network design, such as modifying components and the trends associated with these modifications. Knowing these trends would prove helpful in the physical testing stages of the project. Tuning in ADS reduces the total simulation and experimentation time by recognizing the most sensitive parameters in the circuit and identifying the general trend when changing the parameter values.[30]

5.3 Experimental Approach

The matching network will be configured for 3.5 GHz and the tests described below, will be performed. This phase will be repeated until the required objectives described above are obtained.

5.3.1 S-Parameters and Stability Testing

S-Parameter tests are used to obtain the S-Parameters of nonlinear systems. The amplifier was biased at the desired operating point. A bench for the physical testing of the new amplifier circuit was assigned while the boards were still in the manufacturing process. The test bench was similar to others used at Skyworks Solution, Inc. for the analysis and testing of amplifier circuits. Some of the first measurements taken from the new design were those for IRL and gain. A network analyzer is used to characterize the 2-port amplifier. The network analyzer measures the S-Parameters and stability. A signal generator at -20dBm is built in the network analyzer, which is used to provide a test signal. A test set takes the signal generator output and sends it to the device under test. The signal to be measured is then sent to the receivers. Before making any measurements, the device needs to be calibrated to improve the accuracy of the measurements. Calibration compensates for adjustments in transmission line lengths, losses and feedthroughs. Calibration involves measuring known standards and using those measurements to compensate for systematic errors. After making these measurements, the network analyzer can compute some correction values to produce the expected answer. For answers that are supposed to be zero, the analyzer can subtract the residual. For non-zero values, the analyzer could calculate complex factors that will compensate for both phase and amplitude errors. A calibration using a mechanical calibration kit may take a significant amount of time. To avoid that work, network analyzers can employ automated calibration standards. The network analyzer used for this project is displayed in Figure 42; it uses automated calibration standards. An already

standardized box is connected to the analyzer. The box has a set of standards inside and some switches that have already been characterized. The network analyzer can read the characterization and control the configuration using a digital bus.

Figure 42 Network analyzer [31]

5.3.2 Noise Figure Testing

For any two-port network, the Noise Figure measures the amount of noise added to a signal transmitted through the network. The noise contribution of each two-port network can be minimized through a judicious choice of operating point and source and load resistances.

To design an amplifier for minimum Noise Figure, the first step is to force the actual source impedance to "look like" that optimum value with all stability considerations still applying.

RF input matching is an important aspect in an LNA design. It is a way to achieve a low Noise Figure, higher gain and better input return loss. The goal for the input matching is to achieve low return loss and Noise Figure while maintaining acceptable gain. [7]

Along with tuning work, lab measurements have to be considered for determining the proper final values. The computational values are required to set up the type of structure and target component values.

To get the maximum power transfer from a source to a load, the source impedance must equal the complex conjugate of the load impedance. In addition, for efficient power transfer, this condition is required to avoid the reflection of energy from the load back to the source. A Smith Chart graph can be developed by examining the load where the impedance must be matched. Since the impedances are fixed at the two access ends (the source and the load), the objective is then to design a network to insert in-between so that proper impedance matching occurs. Other inputs need to be considered as well, such as quality factor and limited choice of components.

The input matching circuit usually sacrifices the input return loss of an LNA. This is because the input matching circuit terminates to impedance Γ_{opt} for the best noise match. The optimal input return loss can be achieved when the input matching network terminates the device to a conjugate of S_{11}, which is not necessarily a conjugate of Γ_{opt}. [7]

A typical Noise Figure analyzer attached to the device under test (DUT) is displayed in Figure 43:

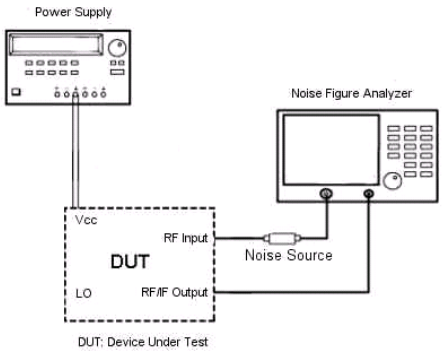

Figure 43 Noise Figure Measurement Test Setup[24]

The Noise Figure analyzer generates a pulse signal to drive a noise source, which generates noise to drive the device under test (DUT). The output of the DUT is then measured by the Noise Figure analyzer. Since the input noise and Signal-to-Noise ratio of the noise source is known to the analyzer, the Noise Figure of the DUT can be calculated internally and displayed. Certain parameters need to be set up in the Noise Figure meter before the measurement, such as frequency range, application, etc. An engineer can measure the Noise Figure over a certain frequency range, and the analyzer can display the Noise Figure to help the measurement. [24][25]

The basis of most Noise Figure measurements depends on a fundamental characteristic of linear two-port devices, noise linearity. The noise power out of a device is linearly dependent on the input noise power. One way to determine the noise slope is to apply two different levels of input noise and measure the output power change. A noise source, shown in Figure 44, is a device that provides these two known levels of noise. Precision noise sources have an output attenuator to provide a low Standing Wave Ratio to minimize mismatch errors in the measurements. If there is a difference between the on and off state impedance, an error can be introduced into the Noise Figure measurement.[24]

Figure 44 Series Noise Source [32]

To make Noise Figure measurements, a noise source must have a calibrated output noise level represented by an excess noise ratio (ENR). ENR is a normalized measure of how much the

noise source is above thermal in its power. Electronic storage of ENR calibration data decreases the opportunity for user error. Automatic download of ENR data to the Noise Figure analyzer speeds the overall set-up time. Temperature compensation improves measurement accuracy leading to tighter specification of device performance. The ENR measurement is based on comparing the DUT to a reference standard which is a calibrated noise source with known ENR values.

5.3.3 Third Order Intercept Point and Gain Compression

A simple and repeatable method to measure intermodulation distortion is the two-tone third order intermodulation technique. The IP3 technique measures the third order distortion products produced by the non-linear elements of the system under test when two tones, closely spaced in frequency, are applied to the inputs of the system. For example, if two -20 dBm tones are applied to an amplifier with 15 dB gain, the fundamental frequencies at the output will have a power of -5 dBm. There will also be two IMD_3 products at $2f_1$-f_2 and $2f_2$-f_1. If these IMD_3 products have a power level of -90 dBm, the OIP3 can be calculated using Equation 14 described in the background section. The OIP3 is then equal to 37.5 dBm. The IIP3 is the OIP3 minus the gain of the amplifier. These distortion products are so close to the original input signals that they cannot be filtered out and therefore represent significant interference in communication systems.

A spectrum analyzer measures the magnitude of an input signal versus frequency within the full frequency range of the instrument. By analyzing the spectra of electrical signals, dominant frequency, power, distortion, harmonics, bandwidth, and other spectral components of a signal can be observed that are not easily detectable in time domain waveforms. Figure 45 is a block diagram that shows the two tone test setup.

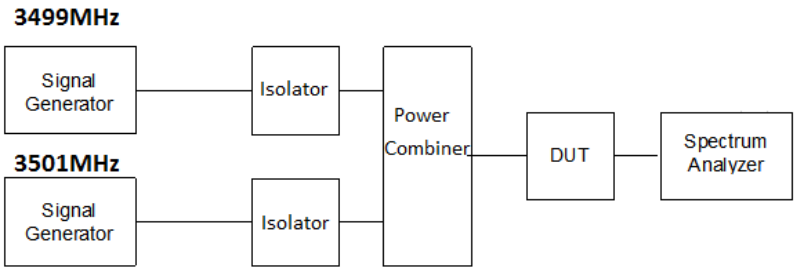

Figure 45 Two tone test setup [33]

The method used to measure IP3 is to inject two test signals, tones, at f_1 and f_2 using 1MHz spacing, and examine the level of the IMD_3, found at $2f_1$-f_2 and $2f_2$-f_1, as shown in Figure 45. The spectrum analyzer has a high dynamic range and isolators are used to improve the match to the device under test. Isolators allow energy to flow only in one direction. A resistive combiner is used, which is well matched at all three ports and presents constant, power-independent impedance to both of the signal sources as well as the DUT. It does not create any inter-modulation products of its own, since it is linear.

Prior to the measurements, the power meter is calibrated to zero. Afterwards, the signal generators are calibrated so that the input power is -20 dBm.

Measuring the P1dB of a device requires driving the DUT into compression without driving the Spectrum Analyzer into compression. This requires proper attenuation at the Analyzer and a Signal Generator to provide a signal at a specific power and frequency. At a given frequency, the power keeps increasing until the DUT compresses. Figure 46 shows the P1dB measurement setup.

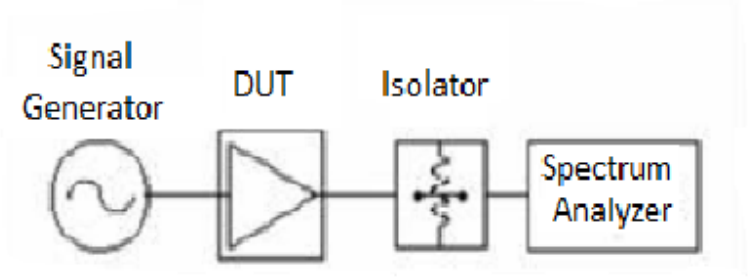

Figure 46 P1dB point measurement setup

The P1dB is derived from the gain relationship between output power and input power. Using the measurement setup shown in Figure 46, the source amplitude is slowly increased while the DUT output is monitored. The input P1dB (IP1dB) is the input power that causes the output

power to drop by 1 dB from the signal value produced by the small signal gain. The output power where the gain drops by 1 dB is known as the output P1dB (OP1dB).

6 Software Simulation and Experimental Findings for 3.5 GHz

This section describes the simulation and experimental findings, using the approach described in the previous sections to develop a 3.5 GHz matching solution for the SKY67003 LNA.

6.1 LNA Characterization at 3.5 GHz

In order to develop a matching solution at an operating frequency of 3.5 GHz the characteristics of the LNA need to be obtained. More specifically, gain circles, noise circles, stability circles, Γ_{opt} and the source and load impedances are needed. To obtain these parameters and circles, we run an S-Parameter sweep of the de-embedded S-Parameter file of the SKY67003 LNA and plot the various circles on a Smith Chart. A de-embedded S-Parameter file is one which contains the non-linear model based S-Parameters of the device. Simulating a non-linear S-Parameter file gives us more accuracy, as it accounts for the non-linear effects of the amplifier. The de-embedded S-Parameter file was obtained from Skyworks Solutions, Inc. The circuit used to obtain such parameters is shown in Figure 47. The disadvantages to this simulation are that the voltage bias level cannot be set and the IP3 contours cannot be plotted. Furthermore, since the de-embedded S-Parameters don't account for the parasitics of the evaluation board and the passive response of the elements in the matching network, the results they show are fairly optimistic.

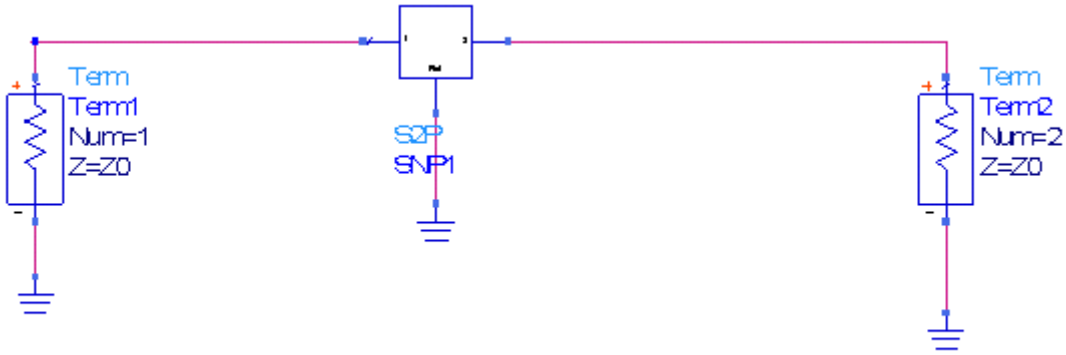

Figure 47 De-embedded S-Parameter file simulation

6.1.1 Stability Circles

Figure 48 shows the S_{11} and S_{22} for the LNA from 3.2 to 3.8 GHz. They show that S_{22} is 0.467 and S_{11} is 0.63. As the absolute value of S_{22} is less than 1, it shows that any input impedance inside the Smith Chart is stable. Similarly, as the absolute value of S_{11} is less than 1, it shows that any output impedance inside the Smith Chart is stable. Therefore the input and output stability circles reside outside the Smith Chart.

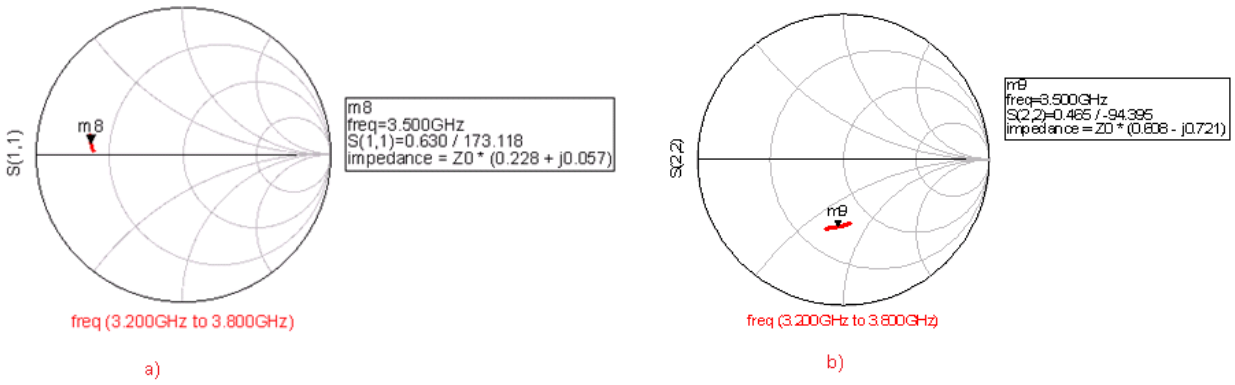

Figure 48 Reflection coefficients for LNA between 3.2 and 3.8 GHz: a) S_{11} b) S_{22}

6.1.2 Gain Circles and Maximum Available Gain

Figure 49 shows the input and output gain circles on a Smith Chart obtained from the S-Parameter simulation. As the circles become bigger, the gain drops by 1 dB. The maximum gain

is shown by the markers m_3 and m_4. The markers show that this value is is 16.937 dB. This gain includes the transducer gain and assumes the other side is optimally matched. The Smith Chart shows that this maximum gain point is very small and difficult to achieve. Therefore even though the maximum gain is 16.937 dB it is more realistic to have a gain of 15.937 dB as this circle is much bigger in area. In order to achieve this gain the normalized impedance should be matched to (0.209-j·0.116)Ω and the normalized output impedance should be matched to (0.464+j·0.585)Ω.

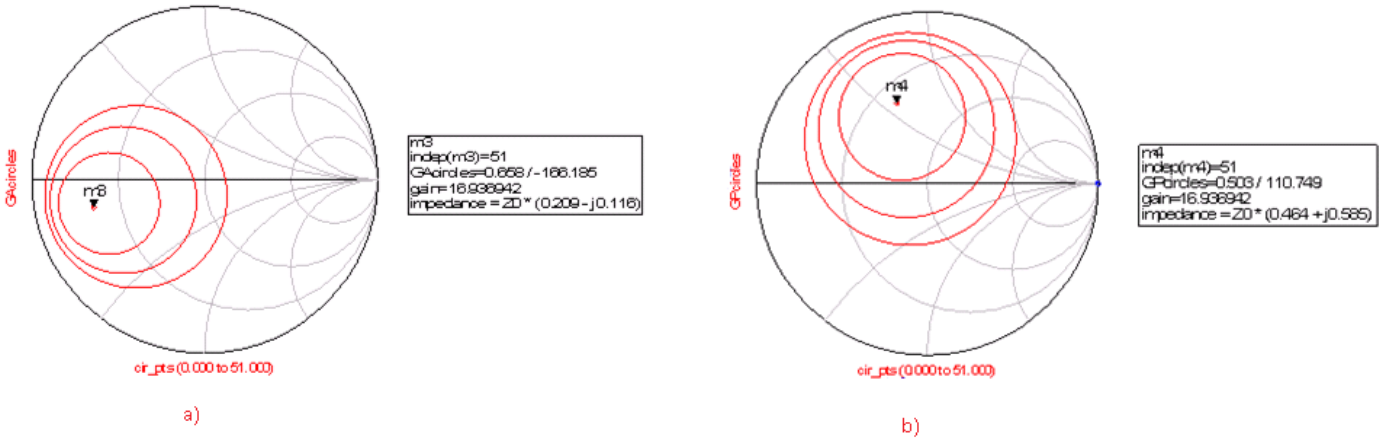

Figure 49 Gain Circles: a) Input Gain Circles b) Output Gain Circles

6.1.3 Noise Circles

Figure 50 shows the noise circles on a Smith Chart for 3.5 GHz. Table 7 shows the noise impedances and minimum Noise Figure. They both show that F_{min} is 1.134 dB. As the circles become bigger the Noise Figure increases by 0.2dB. The Γ_{opt} is the reflection coefficient that gives the minimum Noise Figure. This can be converted into an impedance and this is known as Z_{opt}. The noise circles show that this reflection coefficient is 0.576 / -164.492 and the normalized impedance is (0.273-j*0.126) Ω. As with the maximum gain point the F_{min} point is very difficult to achieve; a more realistic minimum Noise Figure circle is 1.334dB. The input impedance

which give us the best Noise Figure is (13.674-j*6.308)Ω and the optimal load impedance when the input impedance is Z_{opt} is (24.381-j*30.580)Ω.

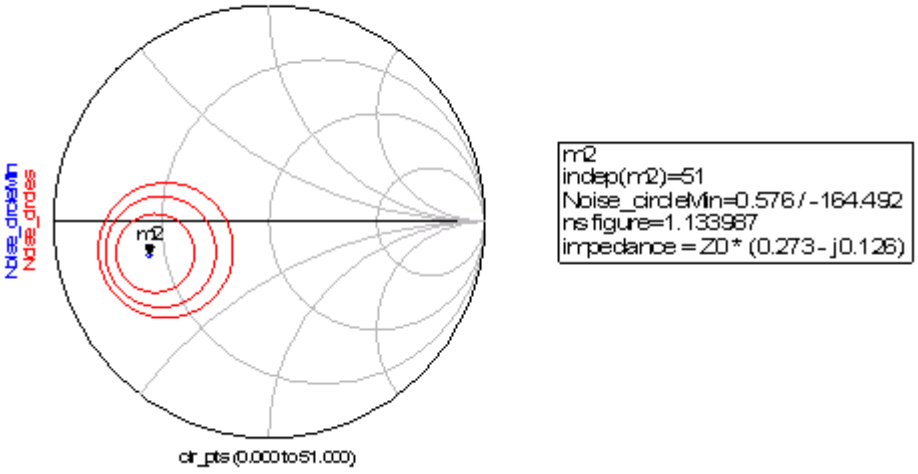

Figure 50 Noise Circles at 3.5 GHz

Table 7 Noise Impedances and F_{min} at 3.5 GHz

Parameter	Value	Units
F_{min}	1.134	dB
Source Impedance(Z_{opt}) for Minimum Noise Figure	13.674-j*6.309	Ω
Optimal Load Impedance for power transfer when source is Z_{opt}	24.381+j*30.580	Ω
Tranducer Power Gain	16.863	dB

6.1.4 Source Reflection and Load Reflection Coefficient

The Smith Chart in Figure 51 shows the normalized optimal source and load impedance points which give us the best S_{11} and S_{22}. The normalized optimal input impedance which gives us the best S_{11} is (0.209-j*0.116) Ω. The normalized optimal output impedance which gives us the best S_{22} is (0.464-j*0.585) Ω. One point to note is that these impedances are the same impedances which give us the best gain.

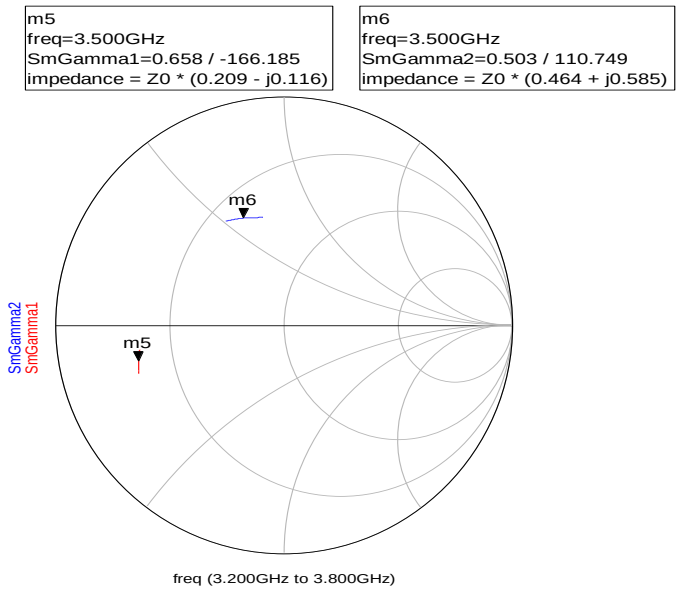

Figure 51 Source and Load Impedance points

6.1.5 Input Gain and Noise Circles Compared

The circles in Figure 52 show the gain and noise circles on the same Smith Chart. The red circles are the gain circles and the blue circles are noise circles. Marker m_3 shows the maximum gain and marker m_4 shows the F_{min}. The Smith Chart shows that the gain and noise circles are concentric Therefore any match which gives us a good gain should in theory also gives us a good Noise Figure and simultaneously a well matched input.

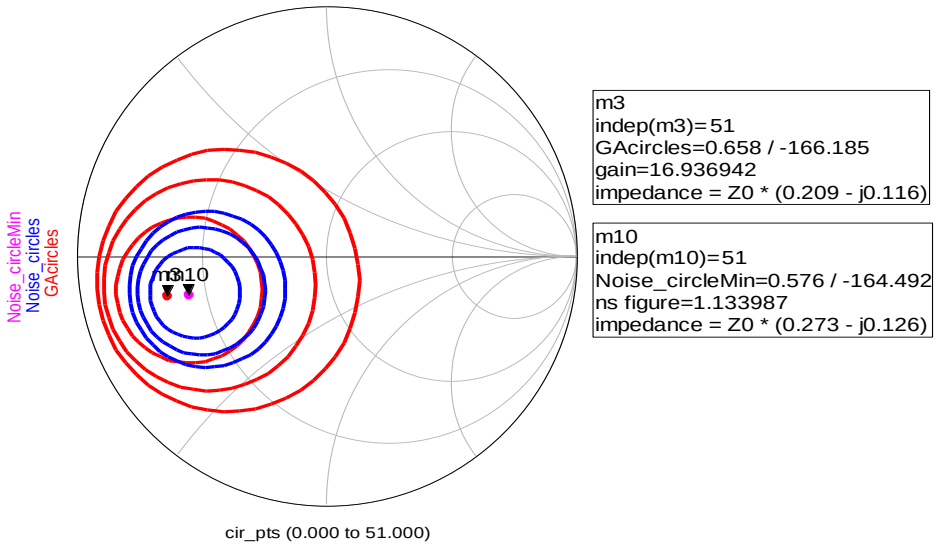

Figure 52 Input Gain and Noise circles

6.2 Simulation and Experimental tuning

Using the LNA characterization results, the device is optimized for a frequency range of 3.3 to 3.6 GHz, with a center frequency of 3.5GHz. Matching and bias networks are designed using ADS, experimentally tested in the lab, and tuned to achieve the requirements of this project.

6.2.1 Simulation for LNA 3.5 GHz configuration

The circuit schematic is configured based on the previous calculations and is displayed in Figure 53. The schematic shows the initial matching and bias configuration components. The input matching and output matching is done with lumped components. The box in the middle is the Skyworks Solutions, Inc. Black Box model. The circuit uses the microstrip lines and vias present on the evaluation board. The lumped components will be later replaced with the manufacture components and tuned using the ADS tuner.

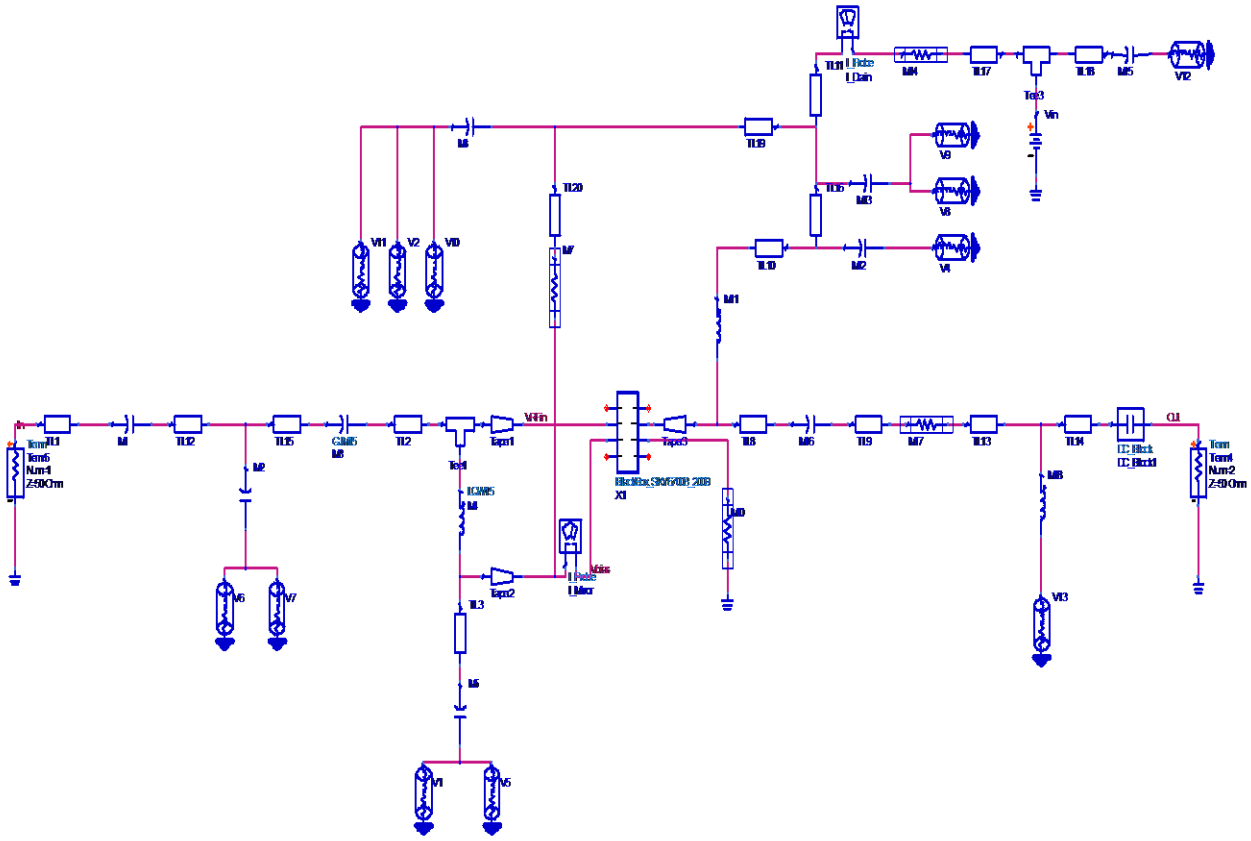

Figure 53 Circuit Schematic

The DC bias network in this configuration sets a current of 77.49 mA at 5 V through a resistor of 5.6 kΩ. According to the DC simulation result shown in Figure 54, the resistor that sets this current should be reduced for a current between 90 to 100 mA at 5 V.

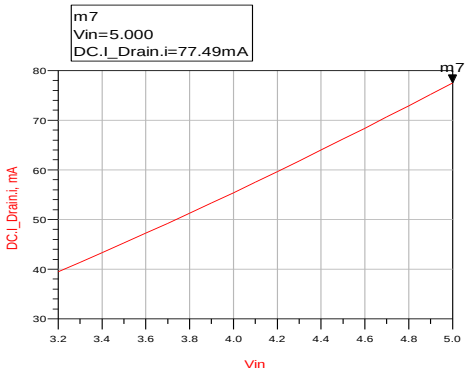

Figure 54 DC Supply current vs. voltage

The next step in the design is the input matching network, which is shown in Figure 55. Capacitor M1 serves as a DC block and inductor M4 is an RF choke. Along with capacitor M2, M3 and M5 also serve as part of the input matching circuit. The characteristics that are being optimized through the input matching circuit include S_{11}, Noise Figure and gain, while keeping the device stable.

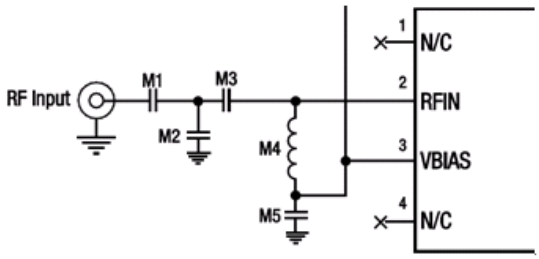

Figure 55 Input matching circuit

After having an initial design for the input matching network, the ADS tuner is used to identify the general trend when changing parameter values. Figure 56 shows the capture of the tuner in ADS. The maximum and minimum are set manually for each of the components to be tuned. The values are changed and the effects they have on the results are observed to obtain the best component values for input and output matching circuits.

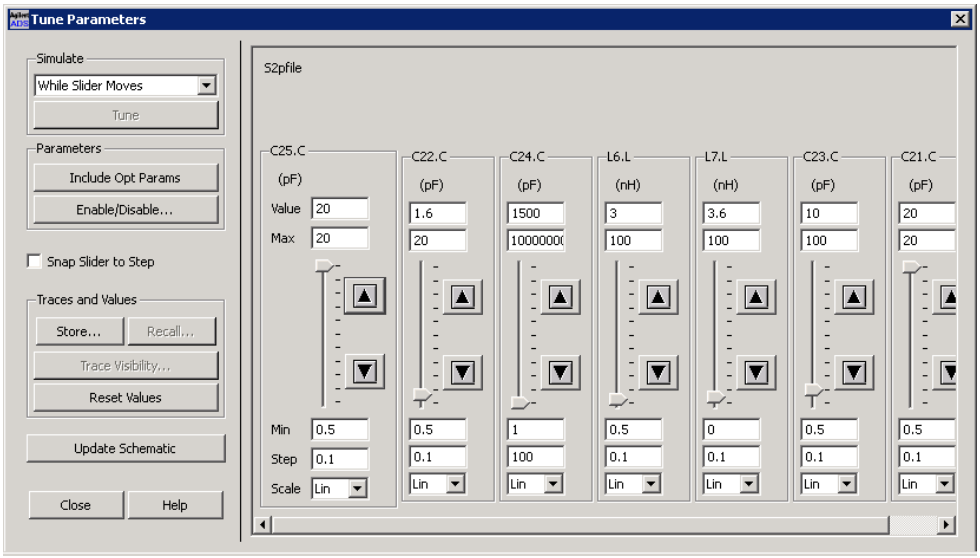

Figure 56 Capture of the tuner in ADS

Increasing M3 above 6.2 pF increases the tolerance for M2 to be between 1 pF and 1.5 pF, but makes Noise Figure worse. At 6.2 pF we get the best Noise Figure of 1.29 dB but M2 has to be exactly 1.2 pF. Decreasing M4 makes S_{11} better but Noise Figure worse. Decreasing the drain inductor increases S_{11} and decreases S_{22}. M5 should be at least 10 pF so that it acts as a good DC block. The range of values we worked with is shown in the Table 8.

Table 8 Component range using ADS tuner

Component	Type	Range
M1	DC Blocking GJM Cap	20pF Exact
M2	GJM Cap	1-1.3pF
M3	GJM CAP	6.2-20pF
M4	LQW Inductor	10-15nH
M5	GJM Cap	10pF-15pF (better to be left alone)
Drain Inductor	LQW Inductor	2-3nH

The best simulation results for this configuration are reached using the values shown in Table 9.

Table 9 Best result components in ADS

Component	Value
M1	20pF
M2	1.2pF
M3	6.2pF
M4	13nH
M5	10pF
Drain Inductor	2.2nH

The results as displayed in Figures 57 - 59. They are: S_{11} = - 18.785 dB, S_{12} = - 31.116 dB, S_{21} = 16.496 dB, S_{22} = - 12.271 dB, and Noise Figure = 1.285 dB. All the requirements are met, except for stability. According to the simulation, the device is not stable at a frequency of 15 GHz.

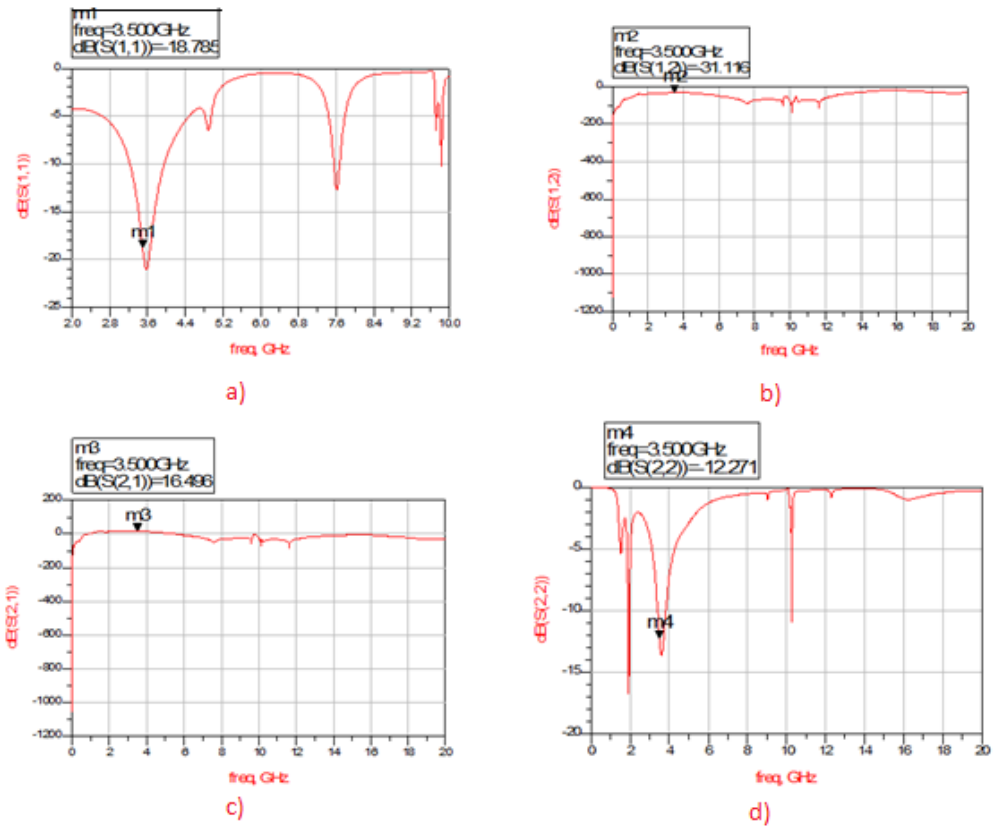

Figure 57 S-Parameter simulation result with input matching. a) S_{11} b) S_{12} c) S_{21} d) S_{22}

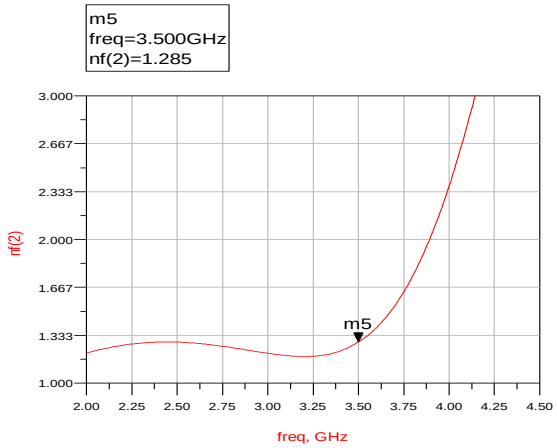

Figure 58 Noise Figure simulation result with input matching

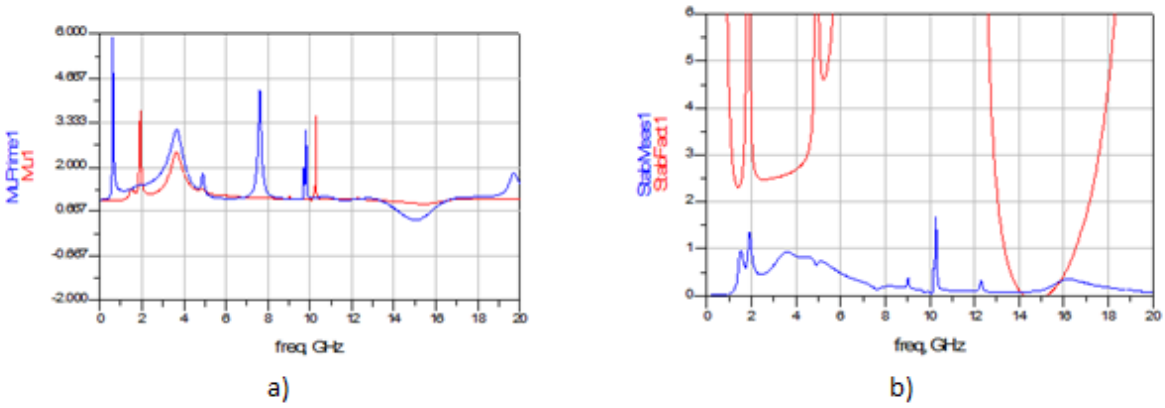

Figure 59 Stability simulation result with input matching. a) μ and μ' b) K and β

Next, the output matching circuit is designed in ADS to optimize S_{22} and further improve the gain of the LNA. The configuration shown below is tuned in ADS. The best values for the capacitor M16 and inductor M18 are 2.2 pF and 4.7 nH respectively. The output matching network is shown in Figure 60.

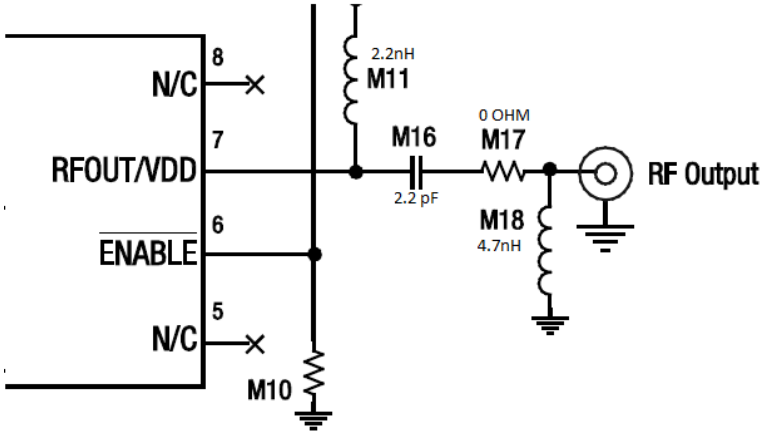

Figure 60 Output matching network

The simulated results from ADS are shown in Figures 61 – 63. S_{22} is improved to -20 dB and the gain is further improved to 16.5 dB. The design is still unstable at a frequency of 15 GHz.

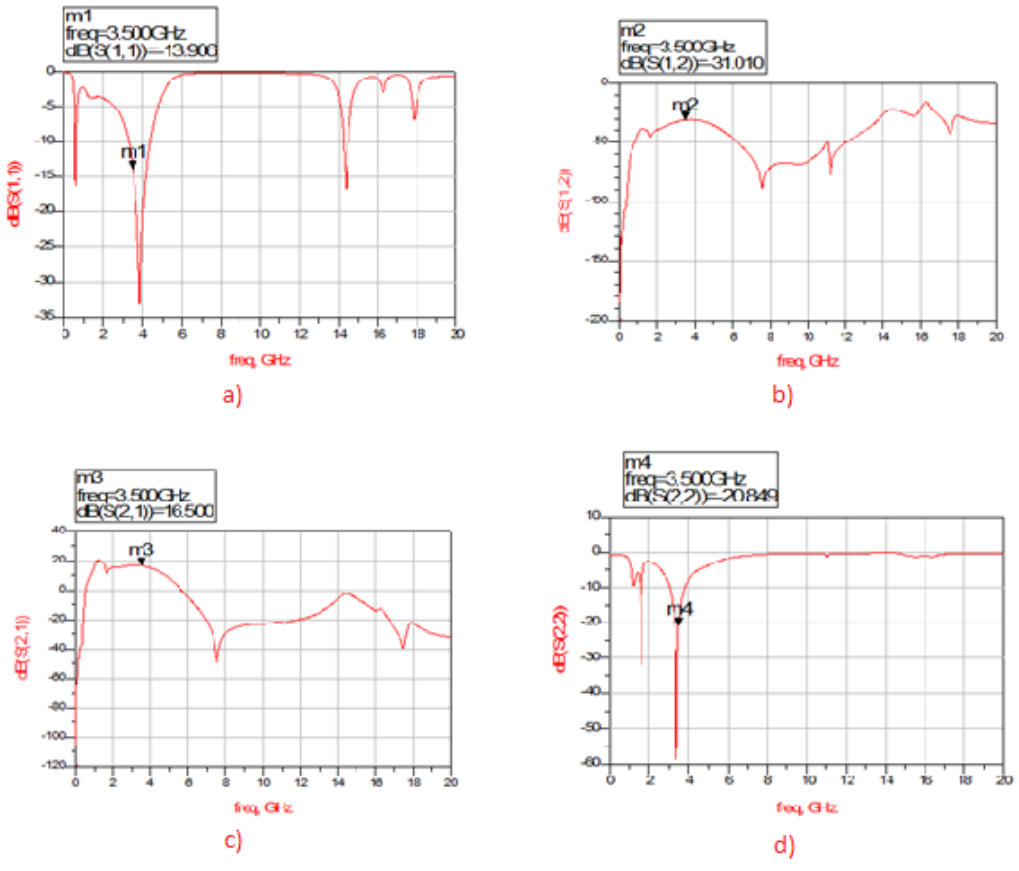

Figure 61 S-Parameter simulation result with input and output matching. a) S_{11} b) S_{12} c) S_{21} d) S_{22}

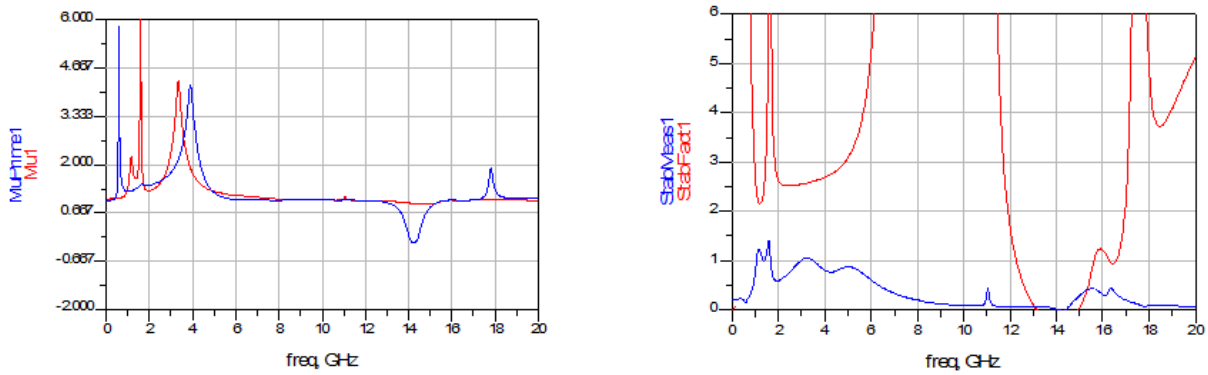

Figure 62 Stability simulation with input and output matching a) μ and μ' b) K and β

From the ADS simulations, it can be seen in Figure 63 and Table 10 that OIP3 is 29.63 dBm and the P1dB is around -1 dB.

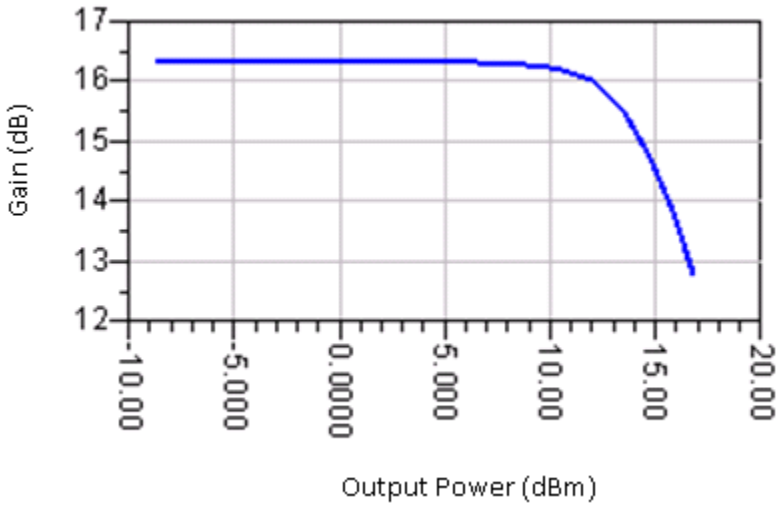

Figure 63 Transducer Power Gain

Table 10 Two tone test at fundamental frequencies of 3499MHz and 3501MHz

Available Source Power, Both Tones (dBm)	Fundamental Output Power, Both Tones (dBm)	Transducer Power Gain(dB)	Gain Compression(dB)	Low and High Side Output IP3 (dBm)		Low and High Side Input IP3 (dBm)	
-25	-8.650	16.35	N/A	29.63	29.63	13.280	13.275
-20	-3.652	16.35	-1.81m	29.53	29.52	13.180	13.175
-15	1.342	16.34	-7.88m	29.20	29.19	12.857	12.852
-10	6.319	16.32	-31.50m	28.07	28.07	11.754	11.749
-8	8.291	16.29	-59.25m	27.01	27.00	10.714	10.709
-6	10.22	16.22	-128.8m	25.14	25.14	8.923	8.918
-4	12.01	16.01	-337.9m	22.85	22.85	6.839	6.834
-2	13.49	15.49	-858.0m	21.17	21.14	5.680	5.651
0	14.73	14.73	-1.616	21.46	21.42	6.730	6.686
2	15.83	13.83	-2.520	22.31	22.31	8.484	8.480
4	16.79	12.79	-3.671	22.56	22.54	9.770	9.756

6.2.2 Experimental Results and tuning for 3.5 GHz configuration

The design is built and tested using the equipment described in the experimental approach section of this report. In the first trial, the component values that are used are those that produced the best results during simulations. The results from this design are shown in Figure 64. The value for the input voltage reflection coefficient, S_{11}, does not meet the requirement of -16 dB. The forward and reverse voltage gain values (S_{21} and S_{12}) are very close to the requirements and the value of the output voltage reflection coefficient is 3 dB more than the required minimum.

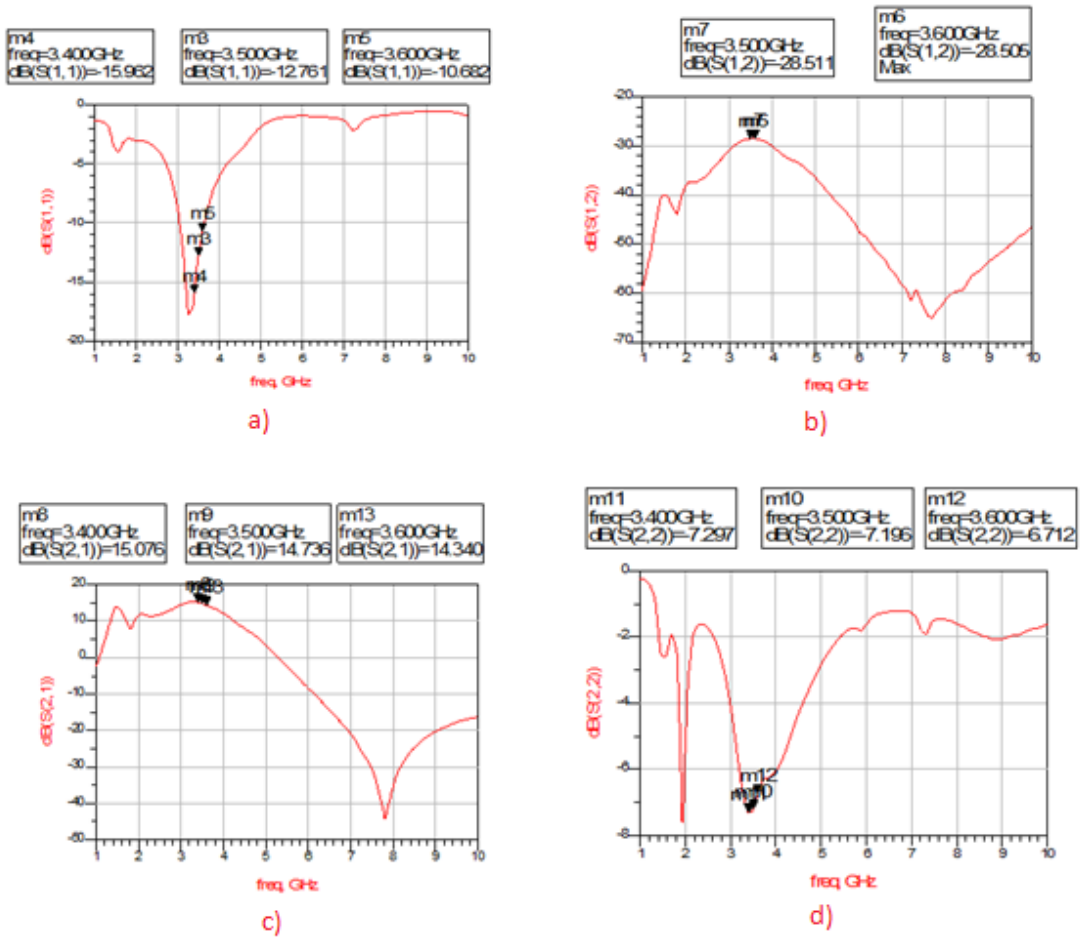

Figure 64 Trial 1 S-parameters. a) S_{11} b) S_{12} c) S_{21} d) S_{22}

Noise Figure for this design is summarized in Table 11. The Noise Figure is higher than the required minimum of 1.4 dB even when 0.1 dB is subtracted from the results to account for board losses.

Table 11 Trial 1 Noise Figure

Frequency	Noise Figure (dB)
3.3	1.39
3.5	1.69
3.6	1.68

As shown in Figure 65, the device is stable over the frequency range, with a K value above 1, a β value above 0, and μ and μ` above 1.

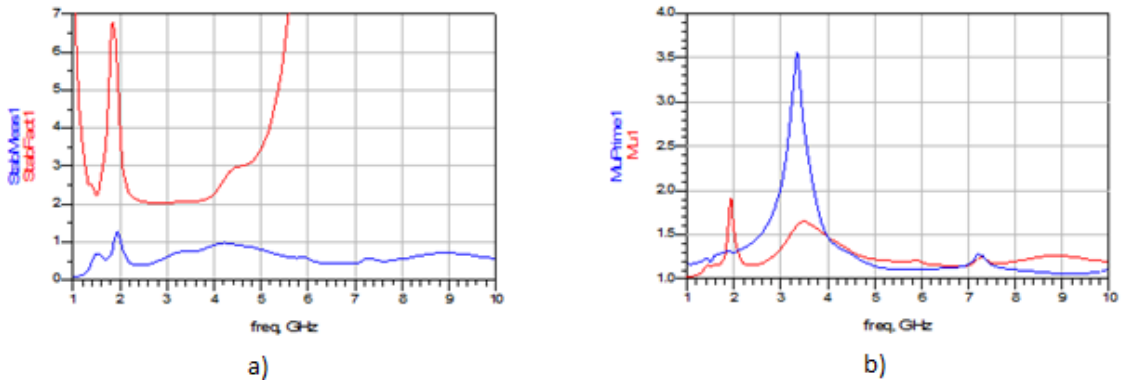

Figure 65 Trial 1 stability: a) K and β a) μ and μ'

Trying to decrease the Noise Figure and S_{11}, the value of the capacitor M2 is reduced from 1.2 pF to 1 pF, as it was observed in the tuner in ADS while performing simulations. The new values are displayed in the Table 12.

Table 12 Trial 2 BOM

Component	Value
M1	20 pF
M2	1.0 pF
M3	6.2 pF
M4	13 nH
M5	10 pF
Drain Inductor	2.2 nH

The results from the simulations are shown in Figure 66. The value for S_{11} has improved and is -15.703 dB. The Noise Figure has also improved, even though by a small amount.

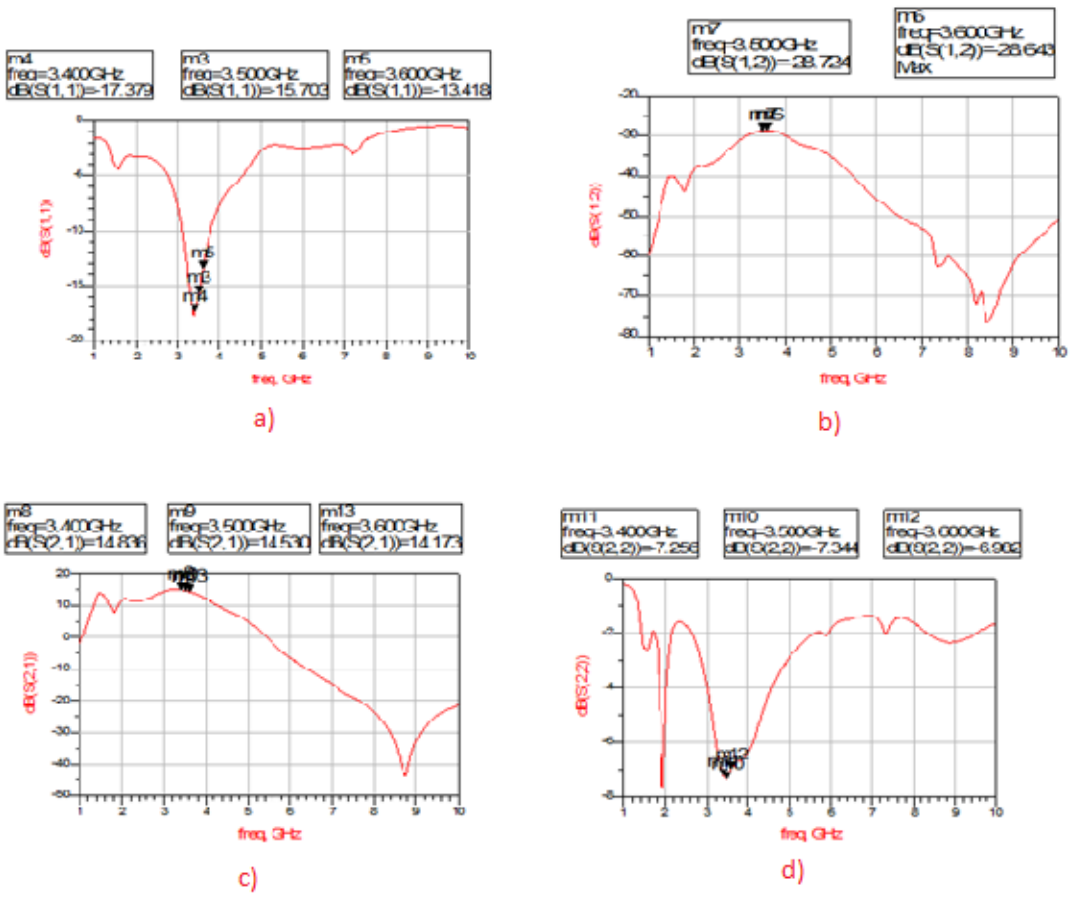

Figure 66 Trial 2 S-Parameters a) S_{11} b) S_{12} c) S_{21} d) S_{22}

Table 13 displays the new Noise Figure.

Table 13 Trial 2 Noise Figure

Frequency	Noise Figure (dB)
3.3	1.34
3.5	1.62
3.6	1.61

Since reducing the capacitor seems to help, we reduce M2 to 0.9pF. The new BOM is shown in Table 14.

Table 14 Trial 3 BOM

Component	Value
M1	20 pF
M2	0.9 pF
M3	6.2 pF
M4	13 nH
M5	10 pF
Drain Inductor	2.2 nH

The S-Parameter results are shown in Figure 67. The graphs show that S_{11} decreased, the Noise Figure decreased and the gain increased.

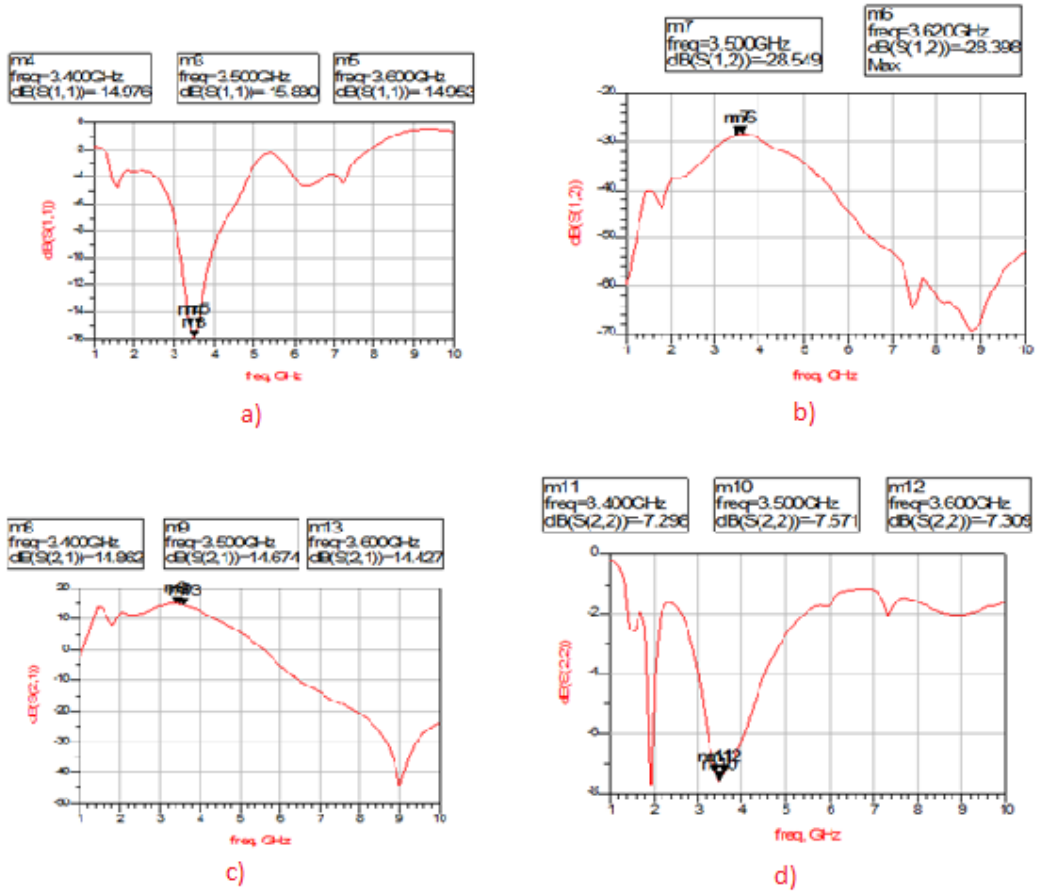

Figure 67 Trial 3 S-Parameters. a) S_{11} b) S_{12} c) S_{21} d) S_{22}

The Noise Figure is displayed in Table 15.

Table 15 Trial 3 Noise Figure

Frequency	Noise Figure (dB)
3.3	1.31
3.5	1.54
3.6	1.54

Reducing the capacitor M3 improves the design further. Since the Noise Figure is still higher than required, M3 is reduced from 6.2 pF to 5.6 pF. The new BOM is shown in Table 16.

Table 16 Trial 4 BOM

Component	Value
M1	20 pF
M2	0.9 pF
M3	5.6 pF
M4	13 nH
M5	10 pF
Drain Inductor	2.2 nH

The S-Parameter results are shown in Figure 68. The Noise Figure is displayed in Table 17. The change in capacitor M3 does not change the S-Parameters significantly. However it reduces the Noise Figure.

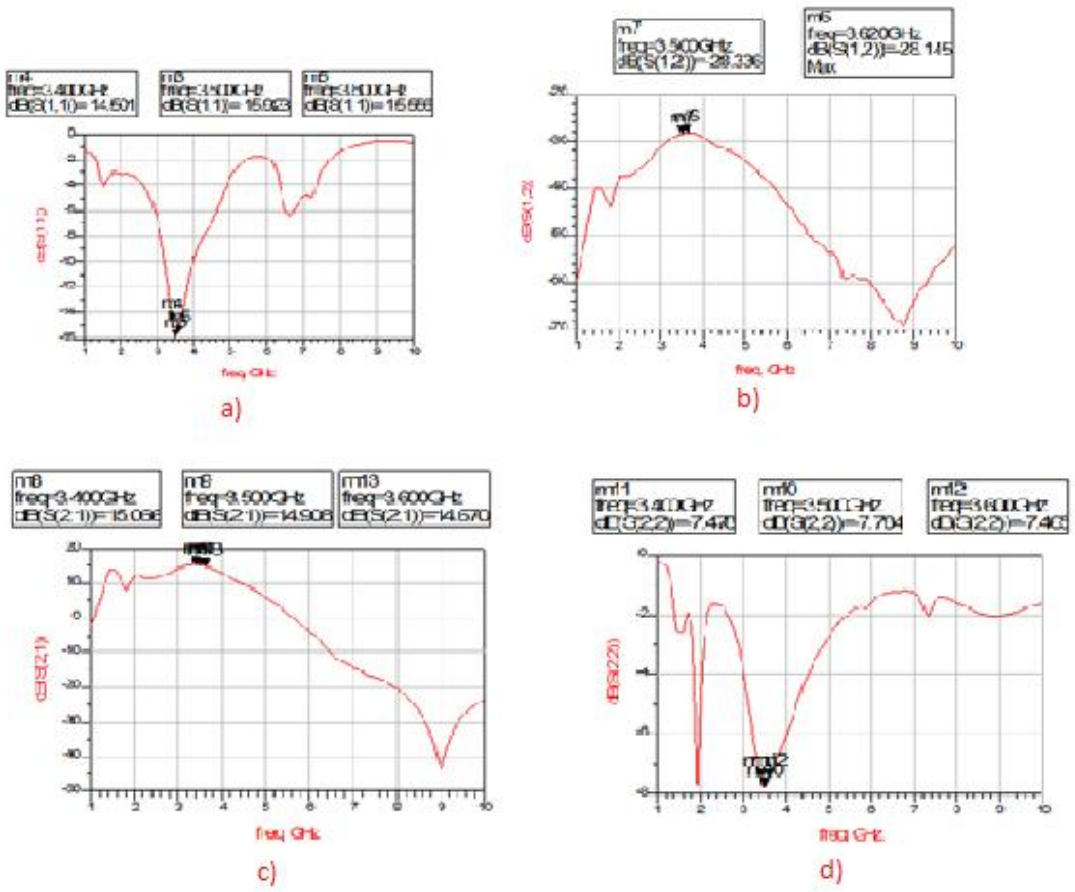

Figure 68 Trial 4 S-Parameters. a) S_{11} b) S_{12} c) S_{21} d) S_{22}

Table 17 Trial 4 Noise Figure

Frequency	Noise Figure (dB)
3.3	1.30
3.5	1.50
3.6	1.48

The capacitor M3 is further reduced to 5.1 pF. The new BOM is shown in Table 18.

Table 18 Trial 5 BOM

Component	Value
M1	20 pF
M2	. 9 pF
M3	5.1 pF
M4	13 nH
M5	10 pF
Drain Inductor	2.2 nH

The S-Parameter results are shown in Figure 69. The Noise Figure data is displayed in Table 19. This is the best input matching circuit. S_{11} is -21.5 dB, the gain is 14.86 dB and the Noise Figure after 0.1dB correction for board losses is 1.41 dB.

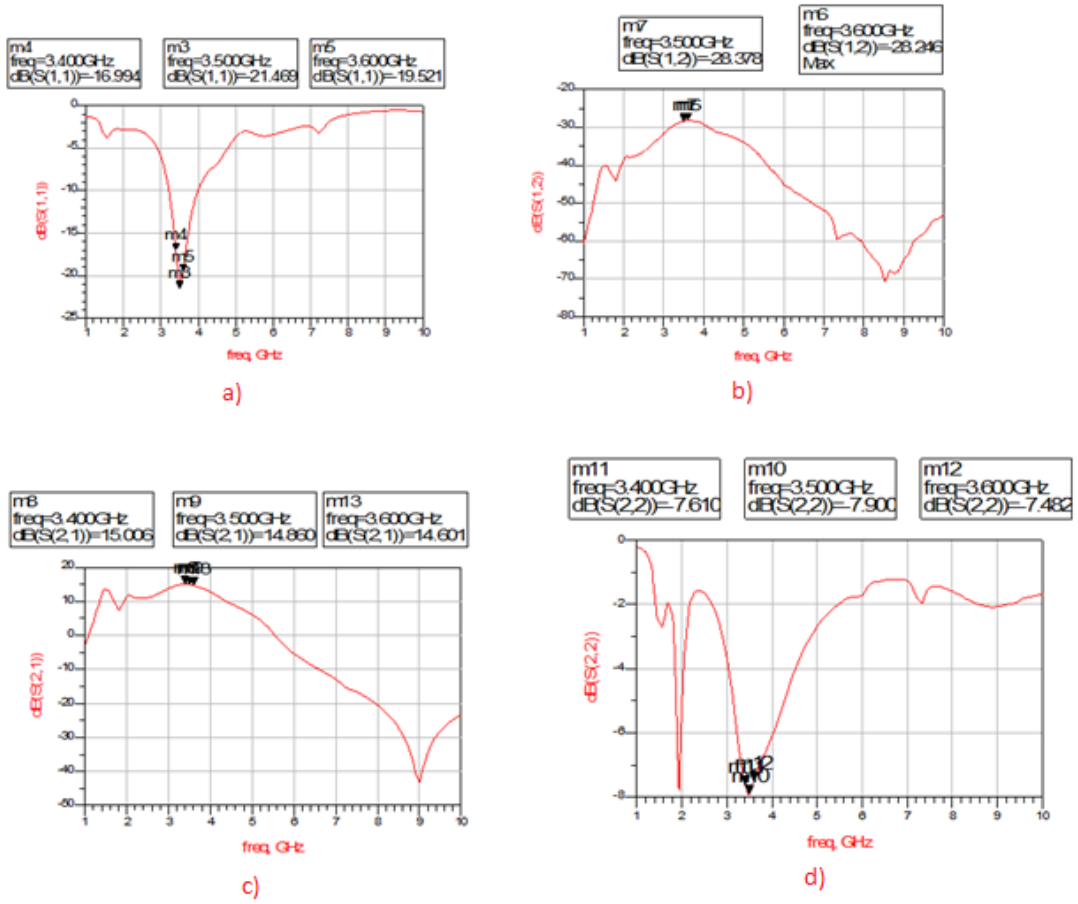

Figure 69 Trial 5 S-Parameters: a) S_{11} b) S_{12} c) S_{21} d) S_{22}

Table 19 Trial 5 Noise Figure

Frequency	Noise Figure (dB)
3.3	1.20
3.5	1.41
3.7	1.39

Next the output matching is tested. The S-Parameter results are displayed in Figure 70. S_{22} now meets the requirement of -10 dB and the gain has improved to 15.594 dB, which meets the requirement of 15 dB. S_{12} is -27.952 dB, only 1 dB higher the minimum requirement of -29 dB. The LNA is stable as shown in Figure 71; this is in contrast to the ADS simulations.

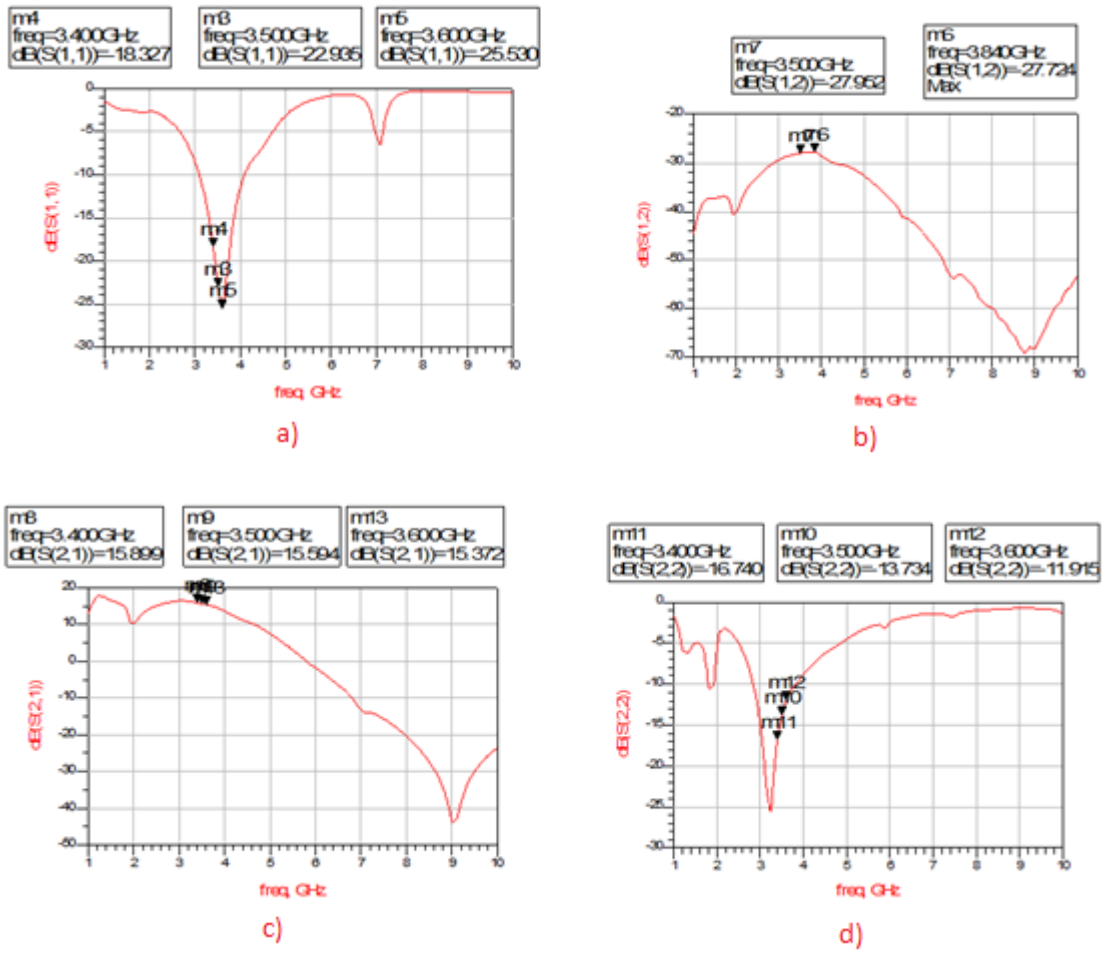

Figure 70 Final experiment S-Parameters: a) S_{11} b) S_{12} c) S_{21} d) S_{22}

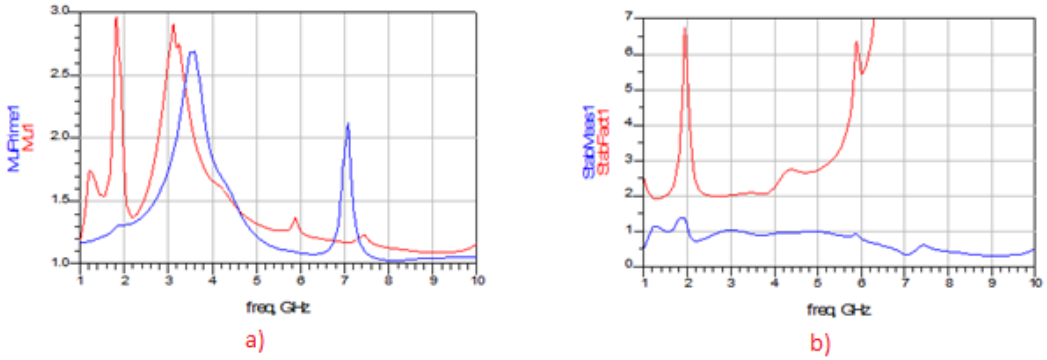

Figure 71 Final experiment stability: a) μ and μ' b) K and β

Figure 72 displays a plot of uncorrected Noise Figure over a frequency range of 3.1 to 3.6 GHz. The corrrected Noise Figure is 1.414 dB at 3.5 GHz as shown in Table 20.

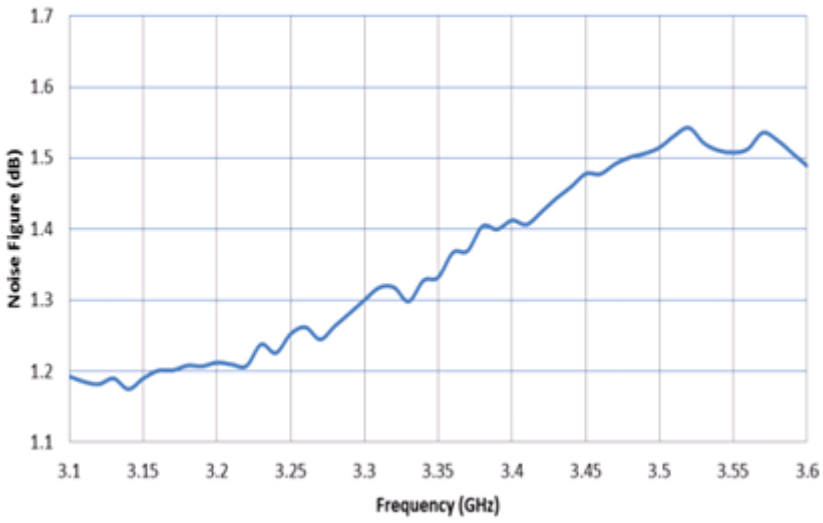

Figure 72 Measured Noise Figure

Table 20 Corrected Noise Figure

Frequency (GHz)	Corrected Noise Figure (dB)
3.3	1.200
3.4	1.312
3.5	1.414
3.6	1.389

Table 21 shows the measured IIP3 and OIP3 and the conditions they were measured in. The OIP3 is measured to be 34.2 dBm. IIP3 is OIP3-gain = 18.69 dBm. That is 2.3 dBm less the minimum requirement of 21 dBm.

Table 21 IIP3 and OIP3

Parameter	Value	Unit
OIP3	34.2	dBm
Gain	15.51	dB
IIP3	18.69	dBm
* Test Conditions • Frequency 3.5 GHz • Input Power -20 dBm • Tone Spacing 1 MHz		

The P1dB, as seen in Table 22 and Figure 73, is 2 dB. The minimum requirement for the P1dB was 5 dB, but considering that the compression at 2.6 GHz was 2dB and that we are moving to a higher frequency, this is still regarded a good result.

Table 22 P1dB measurement

5V_97mA				
P1dB, 3500MHz				
Pin (dBm)	Pout (dBm)	Gain (dB)	Compression	I (mA)
-20	-4.5	15.5	0	97
-15	0.27	15.27	-0.23	97
-14	1.25	15.25	-0.25	97
-13	2.2	15.2	-0.3	97
-12	3.31	15.31	-0.19	97
-11	4.27	15.27	-0.23	97
-10	5.31	15.31	-0.19	97
-9	6.32	15.32	-0.18	97
-8	7.33	15.33	-0.17	96.5
-7	8.3	15.3	-0.2	96.5
-6	9.33	15.33	-0.17	96
-5	10.33	15.33	-0.17	96
-4	11.32	15.32	-0.18	96
-3	12.3	15.3	-0.2	96
-2	13.24	15.24	-0.26	96
-1	14.12	15.12	-0.38	95.5
0	14.95	14.95	-0.55	95
1	15.66	14.66	-0.84	94
2	16.23	14.23	-1.27	94
3	16.7	13.7	-1.8	94
4	17.05	13.05	-2.45	91

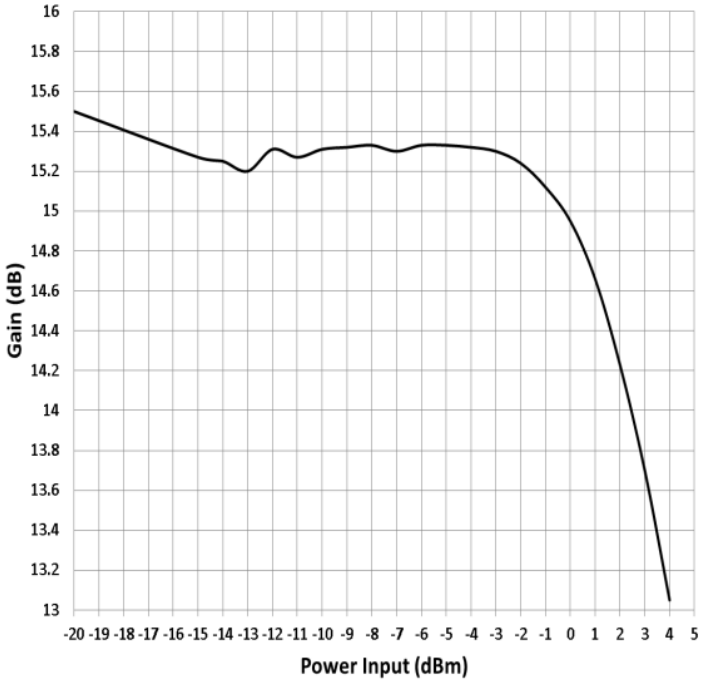

Figure 73 P1dB point plot

In the end, the supply current was 103 mA. This current was above the required limit. Therefore, the resistor that sets the DC bias is increased from 5.6 kΩ to 6.2 kΩ to reduce the current to 97 mA. Table 23 is a list of the BOM with the cost of each component if it is bought in reels of 100,000 components. The total cost of all the components in the matching and biasing networks is $0.30357. The cost of the components in input matching network is higher as they have a high Q factor. These components have a price range in the order of a few cents while the output components have a price range in the order of tenths of a cent. The input needs to have high Q components in order to achieve a low Noise Figure. The inductor M11 is a high Q component in the output matching network because it helps to achieve a low S_{11}. It is the most expensive component in the list and accounts for one third of the costs of the whole component list. As S_{11} is already within the design target, it is better to change it into a low Q component. This will increase S_{22}, IP3 and P1dB, and reduce the overall component cost dramatically.

Table 23 Final BOM with bulk price of 100,000 units

Component	Type	Value	Manufacturer	Size	Unit price (US dollars)
M1	DC Blocking Capacitor	20pF	Murata GJM	0402	0.015
M2	Capacitor	0.9pF	Murata GJM	0402	0.022
M3	Capacitor	5.1pF	Murata GJM	0402	0.01470
M4	Gate Inductor	13nH	Murata LQW	0402	0.099
M5	Capacitor	15pF	Murata GJM	0402	0.011
M6	DNI				
M7	Resistor	6.2kΩ	Panasonic	0402	0.00248
M8	Capacitor	1000pF	Murata GRM	0402	0.003
M9	DNI				
M10	Resistor	0Ω	Panasonic	0402	0.00248
M11	Drain Inductor	2.2nH	Murata LQW	0402	0.112
M12	Capacitor	10pF	Murata GRM	0402	0.004
M13	Capacitor	1000pF	Murata GRM	0402	0.003
M14	Resistor	0Ω	Panasonic	0402	0.00248
M15	Capacitor	0.1uF	Murata GRM	0402	0.00273
M16	Capacitor	2.2pF	Murata GRM	0402	0.005
M17	Resistor	0Ω	Panasonic	0402	0.00248
M18	Inductor	4.7nH	Murata LQG	0402	0.019

6.3 Final Experimental and Simulation Results Comparison for 3.5 GHz configuration

In this section, we compare our final results of the ADS simulations with the tests carried out at Skyworks Solutions, Inc. The key components presented in this section are S-Parameters, Noise Figure, stability, IIP3, OIP3, IP1dB, and OP1dB.

6.3.1 S_{11} Comparison

In Figure 74, the S_{11} simulation results are depicted on the left and the measurement results are shown on the right. Interestingly, the simulated S_{11} notch appears earlier than in reality. With our matching network, the notch is almost centered at 3.5 GHz and produces an S_{11} of -24.014 dB. As the frequency goes higher than 4 GHz, some notches were not present in the simulations but appeared in our measurements.

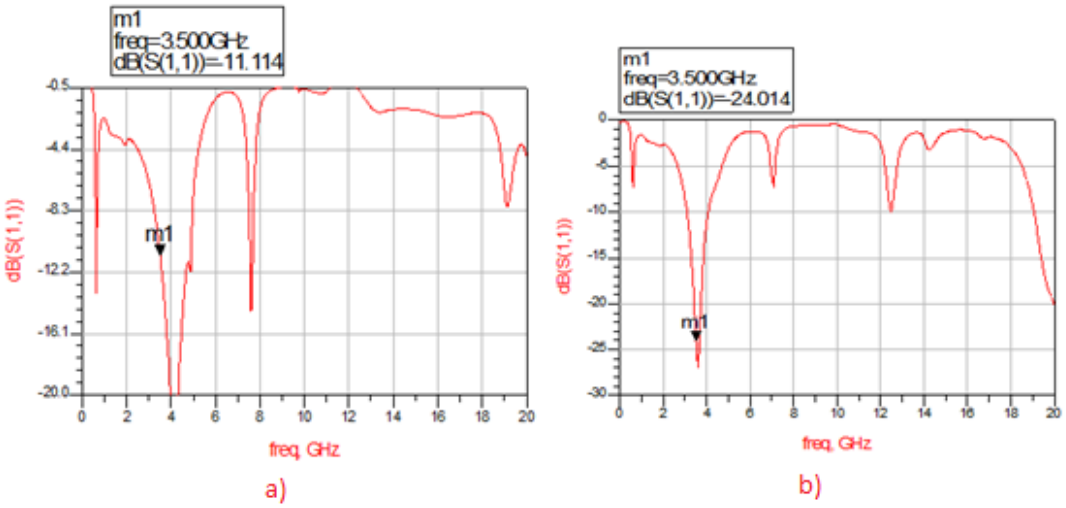

Figure 74 S_{11} comparison: a) Simulated S_{11} b) Measured S_{11}

6.3.2 S_{12} Comparison

In Figure 75, the S_{12} simulation results are shown on the left and the measurement results are shown on the right. The simulated S_{12} is better than the actual measurement. After the careful tuning process, we were able to get an S_{12} of -27.98 dB at 3.5GHz. This result is only 1dB below our targeted S_{12}.

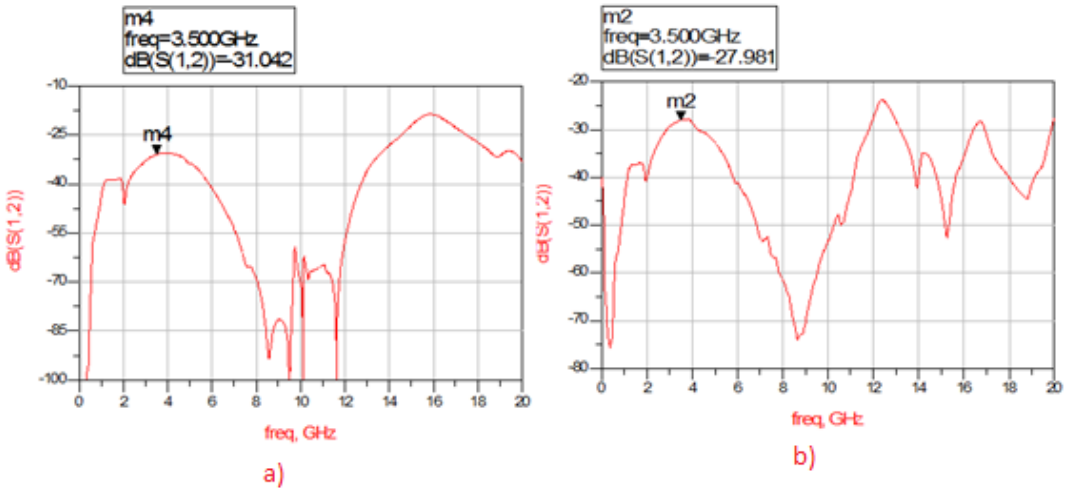

Figure 75 S_{12} comparison: a) Simulated S_{12} b) Measured S_{12}

6.3.3 S_{21} Comparison

In Figure 76, the S_{21} simulation results are shown below on the left and the measurement results are shown on the right. The simulated S_{21} is 16.366 dB and the measured S_{21} is 15.511 dB. The variability between the simulations and measurements is expected and our final measured S_{21} is above our target of 15 dB. As it can also be seen in the figure, the S_{21} simulation is very accurate for frequencies up to 6 GHz.

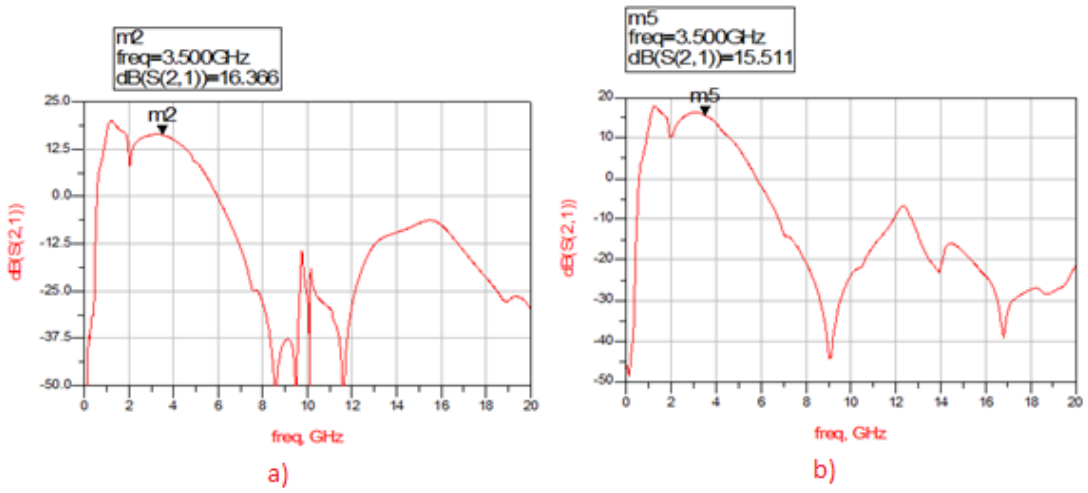

Figure 76 S_{21} comparison: a) Simulated S_{21} b) Measured S_{21}

6.3.4 S_{22} Comparison

The simulated and measured results of S_{22} are shown in Figure 77. Similar to the S_{11} results, the S_{22} simulations appear slightly shifted. However, they maintain the general shape throughout as the frequency is varied. The measured S_{22} is -13.625 dB at 3.5GHz. This result is well below the targeted S_{22} of -10dB.

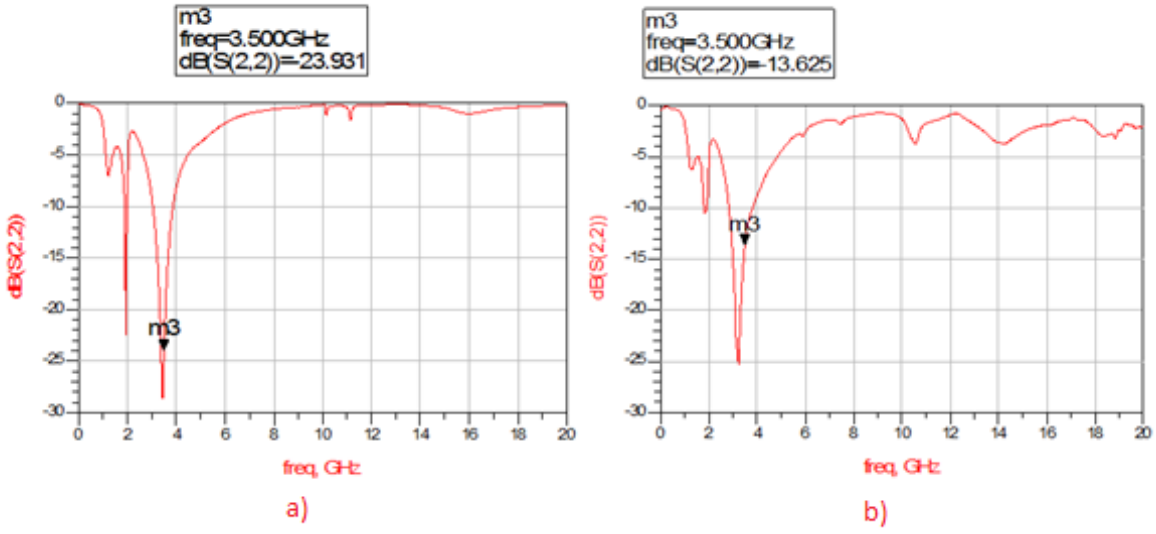

Figure 77 S_{22} comparison: a) Simulated S_{22} b) Measured S_{22}

6.3.5 IP3 and P1db Comparison

The simulation results for IP3 and P1dB are shown in Figure 78 and

Table 24. We note, the OIP3 is 29.53 dBm and the IIP3 is 13.180 dBm. The measured results displayed in Table 25 show that our measured OIP3 is 34.2 dBm and IIP3 is 18.69 dBm. The measured results are higher than the simulated ones. This is close to the minimum requirement of 21 dBm, being off by only 2.39 dBm.

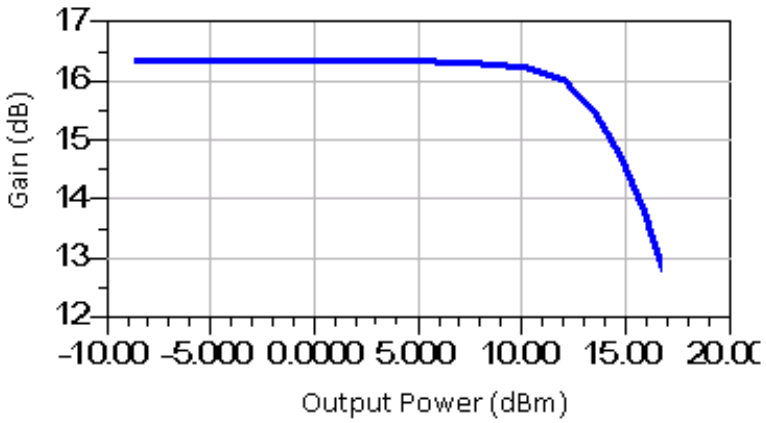

Figure 78 Simulated transducer power gain

Table 24 Simulated IP3 and P1dB at fundamental frequencies of 3499MHz and 3501MHz

Available Source Power, Both Tones (dBm)	Fundamental Output Power, Both Tones (dBm)	Transducer Power Gain(dB)	Gain Compression(dB)	Low and High Side IP3 (dBm)		Low and High SideInput IP3 (dBm)	
-25	-8.650	16.35	N/A	29.63	29.63	13.280	13.275
-20	-3.652	16.35	-1.81m	29.53	29.52	13.180	13.175
-15	1.342	16.34	-7.88m	29.20	29.19	12.857	12.852
-10	6.319	16.32	-31.50m	28.07	28.07	11.754	11.749
-8	8.291	16.29	-59.25m	27.01	27.00	10.714	10.709
-6	10.22	16.22	-128.8m	25.14	25.14	8.923	8.918
-4	12.01	16.01	-337.9m	22.85	22.85	6.839	6.834
-2	13.49	15.49	-858.0m	21.17	21.14	5.680	5.651
0	14.73	14.73	-1.616	21.46	21.42	6.730	6.686
2	15.83	13.83	-2.520	22.31	22.31	8.484	8.480
4	16.79	12.79	-3.671	22.56	22.54	9.770	9.756

Table 25 Measured OIP3 and IIP3

Parameter	Value	Unit
OIP3	34.2	dBm
Gain	15.51	dB
IIP3	18.69	dBm
* Test Conditions • Frequency 3.5 GHz • Input Power -20 dBm • Tone Spacing 1 MHz		

The simulated P1dB as shown in the table above is around -2 dBm. The measured results are displayed below. The P1dB point that we measured is 2 dBm.

Table 26 Measured results for the P1dB

P1dB, 3500MHz (5V, 97mA)				
Pin (dBm)	Pout (dBm)	Gain (dB)	Compression	I (mA)
-20	-4.5	15.5	0	97
-15	0.27	15.27	-0.23	97
-14	1.25	15.25	-0.25	97
-13	2.2	15.2	-0.3	97
-12	3.31	15.31	-0.19	97
-11	4.27	15.27	-0.23	9
-10	5.31	15.31	-0.19	97
-9	6.32	15.32	-0.18	97
-8	7.33	15.33	-0.17	96.5
-7	8.3	15.3	-0.2	96.5
-6	9.33	15.33	-0.17	96
-5	10.33	15.33	-0.17	96
-4	11.31	15.32	-0.18	96
-3	12.3	15.3	-0.2	96
-2	13.24	15.24	-0.26	96
-1	14.12	15.12	-0.38	95.5
0	14.95	14.95	-0.55	95
1	15.66	14.66	-0.84	94
2	16.23	14.23	-1.27	94
3	16.7	13.7	-1.8	94
4	17.05	13.05	-2.45	91

6.3.6 Noise Figure Comparison

Figure 79 shows the simulated and measured Noise Figure. The measurements were done using a Noise Figure analyzer. The room in which the measurements were taken was set up to block interference and maintain constant room temperature. The simulation shows a Noise Figure of 1.54 dB at 3.5 GHz, whereas our measurements show 1.51 dB. The board introduced a 0.1 dB loss at 3.5 GHz; therefore, the corrected Noise Figure at 3.5 GHz is 1.41 dB. Moreover, the corrected Noise Figure at the 3.3 GHz is 1.20 dB and at 3.6 GHz it is 1.389 dB.

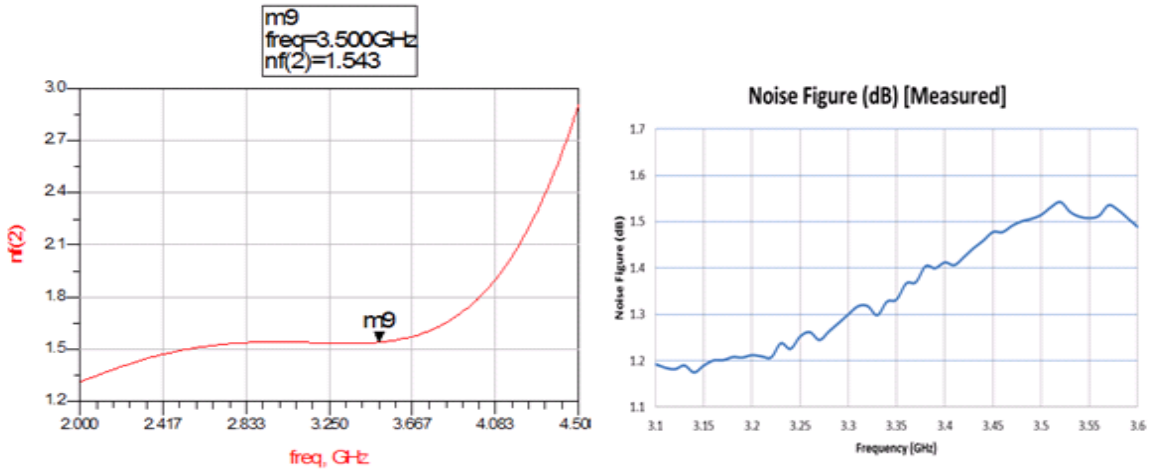

Figure 79 Noise Figure comparison: a) Simulated Noise Figure b) Measured Noise Figure

6.3.7 Stability Comparison

The stability plots are shown in Figure 80, the simulated plots are on the left and the measured plots are on the right. For an LNA to be unconditionally stable, the stability factor has to be greater than 1, and β has to be greater than 0. The simulations show that the LNA becomes unstable from 12 to 16 GHz. However, the measured results of the physical device show that the LNA is stable up to 20 GHz. After numerous tests on the device, we concluded that the device is unconditionally stable up to 20 GHz and there might be some inaccuracies in the simulation for stability factor.

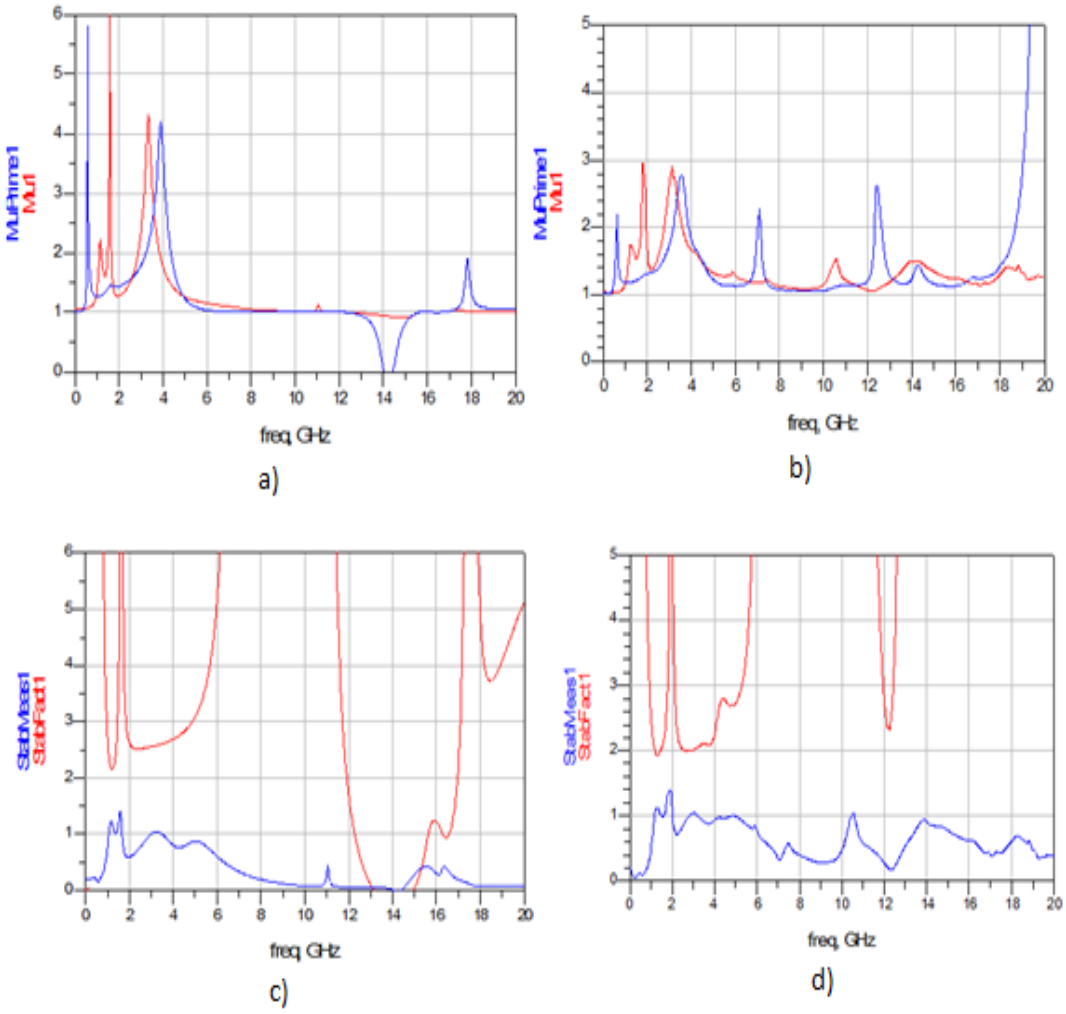

Figure 80 Stability: a) Simulated μ & μ' b) Measured μ & μ' c) Simulated K & β d) Measured K and β

7 Conclusion and Recommendations

This project set out to design an application circuitry for a cellular-base station 4G receiver chain, using the SKY67003 LNA from Skyworks Solutions, Inc. Matching and bias networks were designed for the LNA to operate at the WiMAX 3.5 GHz frequency band. Since the LNA is used in a base station the signal performance of the device is a higher priority as opposed to its power consumption. The key considerations for the design included stability, linearity, Noise Figure, gain, input matching and output matching networks. The project required a design process for the actual development of the matching networks and then a series of tests to validate the design.

The system was simulated using ADS, an RF circuit simulator, and was implemented on an evaluation board. The performance of the final design went through a series of tests and measurements for verification. The data from these measurements was recorded, documented, and compared to the simulated predictions.

The design process began by simulating separate sections of the amplifier's topology and designing them around Skyworks Solutions, Inc.'s Black Box model. Several different designs were produced for the input matching network in an attempt to generate the lowest Noise Figure and input return loss, while maintain stability and achieving a high gain. The output matching circuit was designed to lower IMD3 products as well as reducing the output return loss. Finally, the tradeoff between IP3 and gain was considered.

Once the design was thoroughly simulated and analyzed, the amplifier layout was constructed and tested to be further optimized. The device was tuned to improve the performance of the amplifier. In order to optimize the performance of an LNA, the input and output matching circuits have to be tuned to tradeoff between Noise Figure, return loss, gain and linearity. The

design process lead to the construction of an RF LNA which met most of Skyworks Solutions, Inc.'s expected performance targets. Table 27 summarizes the measured results of our matching and bias circuit.

Table 27 Measured RF and DC specifications

Parameter	Symbol	Test Condition	Typical	Units
RF specification				
Noise Figure	NF	@3.5 GHz	1.41	dB
Small signal Gain	$\|S_{21}\|$	@3.5 GHz	15.51	dB
Input return loss	$\|S_{11}\|$	@3.5 GHz	-24.01	dB
Output return loss	$\|S_{22}\|$	@3. 5GHz	-13.62	dB
Reverse isolation	$\|S_{12}\|$	@3.5GHz	-27.98	dB
3rd Order Input Intercept Point	IIP3	@3.5 GHz, Δf = 1 MHz, PIN = –20 dBm/tone	18.64	dBm
3rd Order Output intercept Point	OIP3	@3.5 GHz, Δf = 1 MHz, PIN = –20 dBm/tone	34.2	dBm
1 dB Input Compression Point	IP1dB	@3.5 GHz	2	dBm
1 dB Output Compression Point	OP1dB	@3.5 GHz	16.23	dBm
Stability	μ, μ1	Up to 20 GHz	>1	-
DC Specifications				
Supply Voltage	V_{DD}		5	V
Supply Current	I_{DD}		97	mA

Referring to the design targets we established in our project statement, Table 28 shows the comparison of measured results and target parameters. As shown in the table, most of our results are well above the design targets except for IIP3, OIP3, IP1dB and S_{12}. The reverse isolation S_{12} of -27.98 dB is only 1 dB away from the targeted -29 dB. Converting dB to decimal units, the 1dB difference is only 0.00033. We believe the reverse isolation S_{12} is close enough to the target. The target IP1dB is 5 dBm and our result shows only 2.0 dBm. However, according to the existing datasheet, at 2.6 GHz the IP1dB is only 2.2 dBm. Therefore, using our design to upgrade the operating frequency from 2.6 GHz to 3.5 GHz, IP1dB drops only 0.2 dBm, which is

acceptable. IIP3 and OIP3 are two of the important parameters to be improved in the future design. Our IIP3 is 2.4 dBm smaller than the targeted IIP3, sacrificing S_{22} and changing the drain inductor may improve the IIP3. From simulation aspect of the project, we recommend improving the Black Box model of the LNA for better simulation results at higher frequency and upgrade Black Box model to be compatible for ADS2011.

Table 28 Design target and measured result comparison

Parameter	Symbol	Test Condition	Design Targets			Measured (Typical)	Units
			Minimum	Typical	Maximum		
RF specification							
Noise Figure	NF	@3.5GHz	1.4			1.41	dB
Small signal Gain	S_{21}	@3.5GHz	15			15.51	dB
Input return loss	S_{11}	@3.5GHz			-16	-24.01	dB
Output return loss	S_{22}	@3.5GHz			-10	-13.62	dB
Reverse isolation	S_{12}	@3.5GHz			-29	-27.98	dB
3rd Order Input Intercept Point	IIP3	@3.5 GHz, Δf = 1 MHz, PIN = –20 dBm/tone	21			18.64	dBm
3rd Order Output intercept Point	OIP3	@3.5 GHz, Δf = 1 MHz, PIN = –20 dBm/tone	36			34.2	dBm
1 dB Input Compression Point	IP1dB	@3.5GHz	5			2	dBm
1 dB Output Compression Point	OP1dB	@3.5GHz	19			16.23	dBm
Stability	μ, μ1	Up to 20 GHz		>1		>1	-
DC Specifications							
Supply Voltage	V_{DD}			5		5	V
Supply Current	I_{DD}		90		100	97	mA

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