Inrush Transient Current Mitigation

A Major Qualifying Project

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Abstract

The main goal of this Major Qualifying Project was to design and implement an inrush transient current mitigation technique for high power full-wave bridge rectifiers with capacitive loads. The inrush current was simulated using PSpice V9.1 for both single-phase and three-phase bridge rectifiers. The mitigation was obtained by gradually charging the capacitive load using small pulses of current, before energizing the system. These pulses of current were controlled by an MSP430 microprocessor synchronized with the input source.

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Executive Summary

Full-wave bridge-rectifiers used for high power AC-to-DC conversion have a high capacitance load. If the voltage across this load is zero when the system is first energized, the capacitor will act as a short circuit, drawing a high inrush current that can potentially damage parts in the system. The goal of this project is to mitigate this inrush current.

This report studies two of the most common methods that are used to mitigate this current, the first one being the use of Negative Temperature Coefficient Thermistors. These thermistors behave as a resistor whose resistance varies with changes in temperature. The thermistor initially has a high resistance, but as current begins to flow through it, it heats up and its resistance decreases. The high initial resistance of the thermistor allows for the high inrush current to be limited, and once the current flows through the thermistor, the resistance decreases to a negligible value, causing the voltage drop across it to be negligible as well.

However, the main disadvantage is that thermistors have a relatively large thermal time constant, meaning that they take a long time to cool down. If the rectifier system is energized when the thermistor's resistance is low, the capacitor could still draw a high inrush current, damaging the circuit.

The other mitigation technique uses a current limiting resistor (CLR) or inductor (CLI) in series with the bridge-rectifier. This impedance will limit the current, protecting the system from the high inrush current, and then it would be shorted once the capacitor was charged, to avoid power losses.

Although this method provides a solution to mitigate inrush transient currents, these resistors and inductors have high power ratings and are large in size, occupying too much space.

The design proposed in this report consists of previously charging the capacitive load of the system, in order to avoid the inrush current. This is done by using a Triode for Alternating Current (TRIAC) controlled by a microprocessor.

The microprocessor is synchronized with the voltage source and provides pulses to the TRIAC. This enables the TRIAC to supply small pulses of current into the capacitor to gradually charge it. Once the capacitive load is charged, then the TRIAC is left turned ON to continue the rectification. The advantages of this method include reducing the peak inrush current to the peak steady-state current while introducing minimal power losses and keeping the pre-charging module compact.

On the other side, one disadvantage is the delay introduced for bigger capacitance loads; the pre-charging module would take a longer time to charge capacitive load. However, the system will not begin the rectification until the load is charged, eliminating the possibility of a high inrush current.

The method proposed in this report successfully mitigates the inrush current caused by the capacitive load of high power applications full-wave bridge-rectifiers.

1. Introduction

Inrush current is the instantaneous flow of electric charge that an electric device experiences when it is energized. It is a surprisingly complex topic, and one that is becoming more important than ever before. More and more household and industrial products are using switch mode power supplies, and almost all of these supplies draw a significant over-current when power is applied [1]. At the startup of a switched-mode power supply, inrush currents often exceed the maximum safety ratings of components that are specified by manufacturer. This can cause serious problems such as tripping circuit breakers, welding switch contacts, thermal wear down of components, and premature failure of circuit breakers, transformers and converters.

Some of the most common methods of reducing inrush currents include Negative Temperature Coefficient (NTC) thermistors, current limiting resistors, and solid-state relays. The selection of the best method to implement is usually dependent upon the desired inrush current amplitude and the startup delay time of the system [2]. Each of the available methods reduces inrush currents to some extent, however there is a tradeoff involved with each one of them.

NTC thermistors are thermally-sensitive resistors whose resistance varies with temperature. Current limiting resistors are used to react to the peak inrush current of the system, by simply providing a protective load. Solid state relays aim to improve the current handling efficiency of the system through rapid switching. However, when the switch contacts close, the resistance is increased and during inrush conditions the contacts are overloaded. The contacts could then potentially weld together, producing a short circuit and damaging the system.

The objective of this project was to find new mitigation methods to reduce inrush currents in the switch contacts of high voltage systems. It encompasses a wide range of sub-disciplines that includes analog microelectronics, power systems engineering, and computer engineering. The initial designs included phase delayed switching and shunt impedances. Simulations were done in Cadence PSPICE V9.1 and TI Multisim V11.0 to obtain insight on the expected behavior of each system, as well as to observe which method provided the best inrush current reduction.

2. Literature Search

2.1.Negative Temperature Coefficient Thermistor

One of the most common methods used to suppress inrush current is to connect NTC (Negative Temperature Coefficient) power thermistors in series to the line, similar to the Figure 2.1 [3]. A thermistor behaves as a variable resistance offering a range of resistances that depends on its temperature [4]. This resistance is inversely proportional to the temperature and as current flows through the thermistor the capacitor can be slowly charged.

Before the system is turned ON, the thermistor has a high resistance. Once the system is turned ON, the load capacitor begins to charge, and the current that flows through the NTC heats it up and causes its resistance to drop. By the time the capacitor is charged up, the voltage drop across the NTC is negligible [5]. One of the main problems with this method is that the thermistor requires a cool down-time to increase its resistance before it can take the next impulse of inrush current. If the system were turned OFF and ON repeatedly in a short amount of time, the thermistors would not have sufficient time to recover in order to limit the current again.

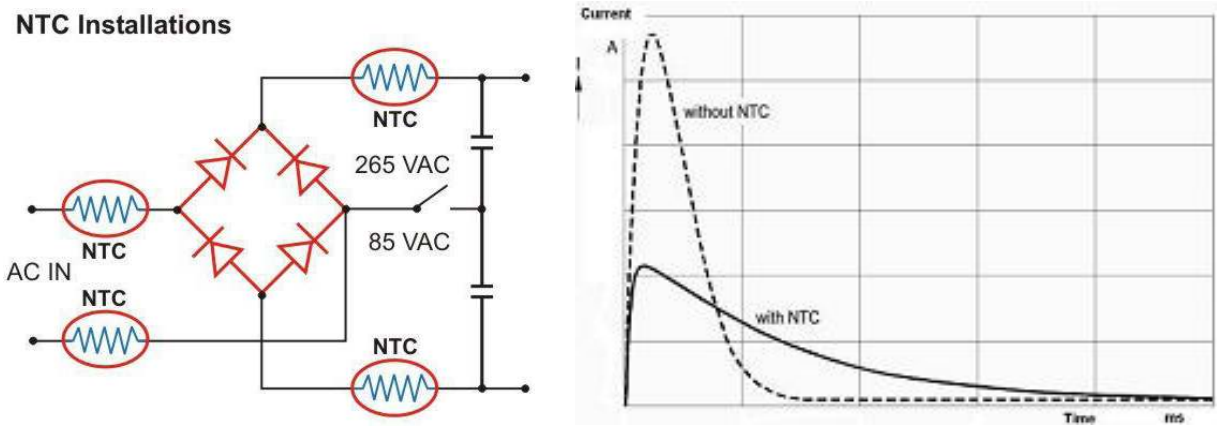

Figure 2.1 - NTC Installations (courtesy of Amertherm, Inc) [2]

2.2.Current Limiting Resistance/Inductance

Another technique that has been implemented in the past involves a current limiting impedance that would be bypassed by a short circuit after some time has passed in order to limit the current at the start, but still conserve power in steady state. This impedance could be a resistor, an inductance, or a series combination of both. Figure 2.2 shows the block diagram of the current limiting impedance in a full-wave bridge rectifier.

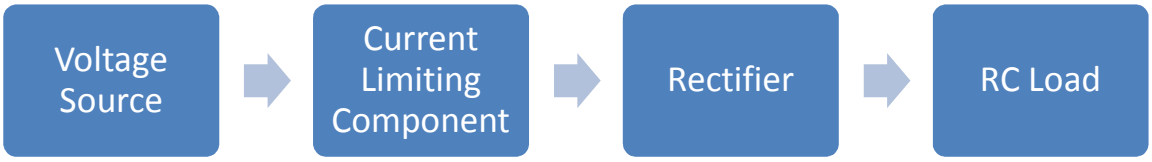

Figure 2.2 - Circuit Flow Diagram

Current limiting resistors are less efficient than NTC thermistors because of the power losses that result from steady state current flowing through them. However, these resistors are commonly bypassed by short-circuiting them to suppress such losses.

Similarly, current limiting inductors are used to limit inrush currents, but the behavior is different in this case. Since the current alternates once the circuit is closed, the impedance of the inductor depends on the frequency which is defined by (2.1). Once the current goes into steady state, the inductor is also bypassed to remove and additional power losses.

$$Z_L = j\omega L = j(2\pi f)L \tag{2.1}$$

Throughout the years, several inventions and applications have been implemented to try to fix and lessen this issue, with the main obstacle still resting in the packaging and sizes limitation, because these impedances are often large components that take up too much space. Another obstacle relies in the power losses, caused by lowering the high current levels efficiently [6].

2.3.Phase-Delayed Switching

Another method used to suppress the inrush transient current is to trigger the system at a phase angle that is different from the supply voltage source. The concept behind this technique is to trigger the circuit at the specific phase at which the transient response of the circuit would be minimized.

In order to better explain this concept, and how it applies to resonant circuits, it is useful to analyze the behavior of such resonant circuit.

2.3.1. RL Circuit

When an AC circuit has a series connection of an inductor (*L*) and a resistor (*R*), as shown in Figure 2.3, the current that flows through the total impedance depends on the voltage across the inductor, according to (2.2):

$$i(t) = \frac{1}{L}\int v_L(t) \tag{2.2}$$

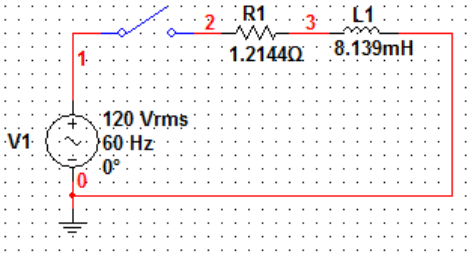

Figure 2.3 - RL Circuit

Therefore, if the input voltage is a sinusoidal wave at a frequency *f*, the current flowing through the system will have a phase-shift (ϑ) once it reaches steady state, where

$$\theta = \tan^{-1}\left(\frac{X_L}{R}\right); \text{ where } X_L = 2\pi f * L \tag{2.3}$$

When such system is energized, it experiences a transient response due to the reactance of its impedance. This behavior can be described with (2.4), whose solution is given by (2.5) below. This system is being energized at a given phase angle (α) with respect to the supply source.

$$\left(R * i(t)\right) + L\left(\frac{di(t)}{dt}\right) = V_{pk} * \sin(\omega t + \theta - \alpha) \tag{2.4}$$

$$i(t) = K_1 + K_2 * e^{-\frac{t}{\tau}}; \text{ where } \tau = L/R \tag{2.5}$$

As the system reaches its steady state, the current will be a constant sinusoidal wave with a phase-shift (ϑ) and a magnitude of $I_{pk} = V_{pk} * |Z_{RL}|$; where $|Z_{RL}| = \sqrt{{X_L}^2 + R^2}$. Therefore, the behavior is described in (2.6):

$$\begin{gathered} i(0) = K_1 + K_2 = 0 \\ i(\infty) = K_1 = I_{pk} \\ K1 = -K_1 \end{gathered} \tag{2.6}$$

Using (2.5) and (2.6), the steady state current can be expressed as (2.7):

$$i_{ss}(t) = \frac{V_{pk}\left[\sin(\omega t+\alpha-\theta) - e^{-\frac{t}{\tau}}\sin(\theta-\alpha)\right]}{Z_{RL}|\angle\theta|} \tag{2.7}$$

From this relationship, the transient could be eliminated by energizing the system at the angle $\alpha = \theta$.

2.3.2. LC Circuit

A different behavior is observed if an AC system has a capacitor (*C*) and an inductor (*L*) connected in series as shown in Figure 2.4. If such a system is purely reactive (i.e. no resistance), then the current flowing through the impedance will oscillate at a frequency $f_R = \frac{1}{2\pi\sqrt{LC}}$, in addition to the frequency of the input source.

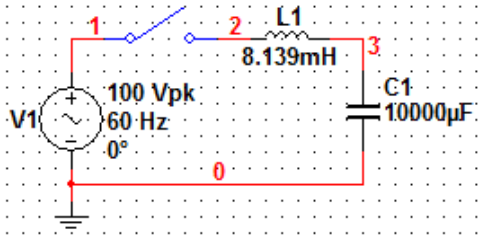

Figure 2.4 - LC Circuit

The reason behind these oscillations is that, when the capacitor gets charged by the voltage source, the current not only flows through the capacitor but also through the inductor. The behavior of this current is defined by (2.8).

$$v_{IN}(t) = L\frac{di(t)}{dt} + \frac{1}{C}\int i(t)dt \qquad (2.8)$$

Once the system is energized, and while the input is positive, the capacitor will charge up to the peak voltage, however the inductor will prevent the current from changing instantly, causing oscillations at the resonant frequency (f_R) in the capacitor voltage and current. The same behavior is observed when the input is negative, causing oscillations at f_R as well as at the input frequency.

2.3.3. Clock-Driven Switching with TRIACs

In order to trigger the system at a specific phase-angle compared to the voltage source, a delay was implemented in the switching mechanism that depends on the phase-angle which is contingent upon the impedance of the system. Such delays are usually achieved by a separate clock, synchronized with the voltage source [7].

For the simulations, a clock signal was generated using two comparators to compare the supply voltage to a value slightly lower than the peak of the supply. The resulting signal was a 120Hz square wave with approximately 90° of phase, in relation to the supply voltage.

The clock was used to drive a TRIAC and keep it continuously turned ON. This is not a completely new approach to handling AC voltages, since TRIACs have been used in AC signal analysis due to their multidirectional capabilities in the design field [8].

For high power bridge rectifier applications where the load is mainly capacitive, like the circuit shown in Figure 2.5, this technique would not be applicable because the capacitive load needs to be charged up in order to avoid the high inrush current.

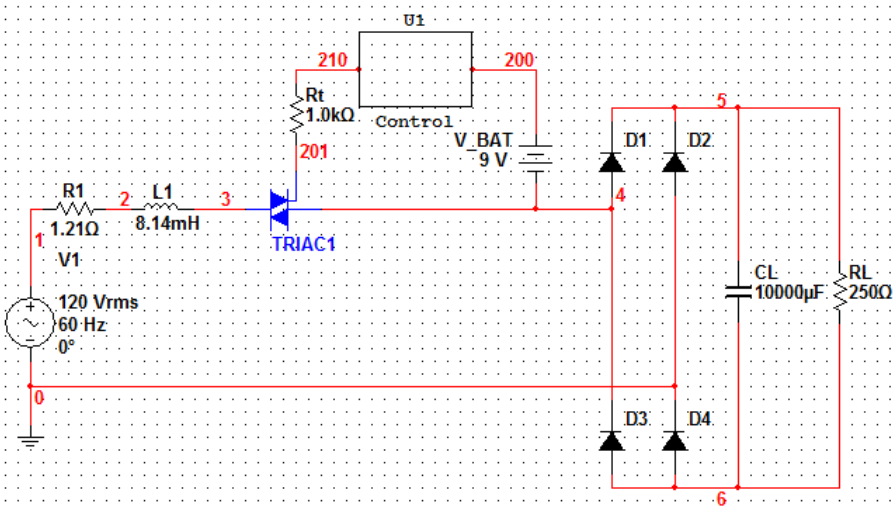

Figure 2.5 - Single-Phase Full-Wave Bridge Rectifier

In such systems, the inrush current occurs due to the rapid charge of the capacitor that happens immediately after the circuit is closed. The charging of a capacitor is predicated on the fundamental relationship between capacitors and the rate of change from the supply voltage [9]. Therefore, the minimum peak current that can be obtained using the Phase-Delayed Switching mechanism is approximately 50% of the initial inrush current. This mitigation is obtained when the capacitive load is charged up to 50% of the input peak voltage in the first half-cycle, and then it reaches the maximum input voltage after the second half of the first cycle.

In order to charge the capacitive load in this manner, the switching has to happen at a phase angle approximately between 120 and 150 degrees from the input voltage. However, the precise phase angle depends on the RC combination of the output load.

3. Design Method

Since the current flowing into the capacitor depends mainly on how much and how fast the capacitor voltage changes, the most efficient approach to avoid the transient current is to previously charge the capacitor up to the value of the supply voltage.

3.1. Time-Delayed Switching with Capacitor Pre-Charging Circuit

In order to pre-charge the capacitor without having a big transient current, the circuit in Figure 3.1 was built. This uses a Silicon Controlled Rectifier (SCR) thyristor which is controlled by a specific clock signal that allows the capacitor to be charged up without causing a big transient current.

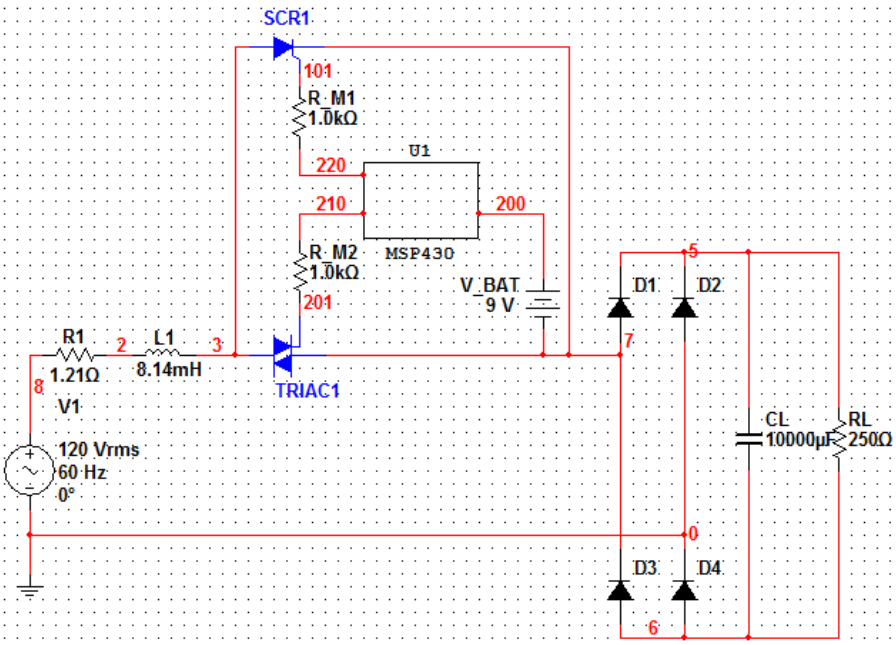

Figure 3.1 - Single-Phase Full-Wave Rectifier with Pre-Charging Circuit

The clock signal would generate a pulse, increasing in width with every cycle, similar to the one shown in Figure 3.2. The purpose of this pulse is that the SCR would slowly charge the capacitor, starting very close to the zero-crossing of the sinusoidal wave, where the voltage would be minimal. The pulse width will continually increase until it matches the supply voltage maximum (90^{o} on the sinusoidal). Once the capacitor is charged to the maximum voltage, the SCR would be turned OFF and a TRIAC would be triggered to continue the rectification.

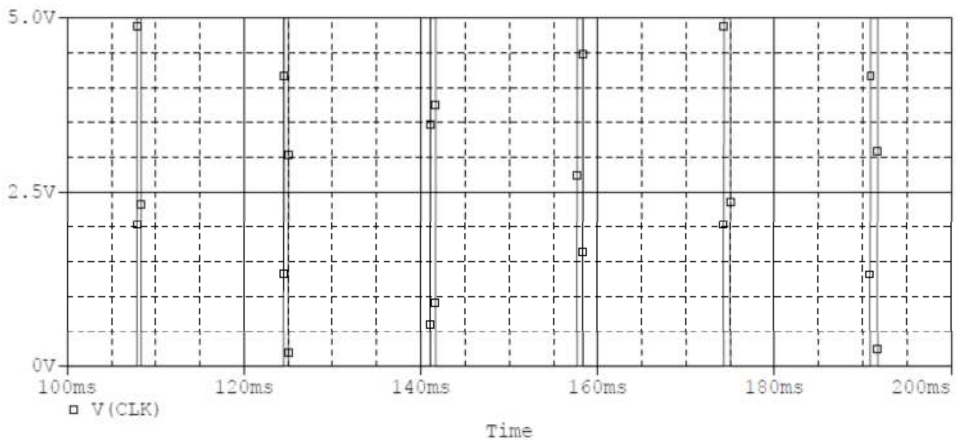

Figure 3.2 - Clock Signal to Pre-Charge the Capacitor

The pre-charging circuit was also implemented on a three-phase system, and the complete circuit is shown below in Figure 3.3, where the SCR would be triggered by the same pulse mentioned above, and similarly the TRIACs would be activated once the capacitor reached maximum voltage.

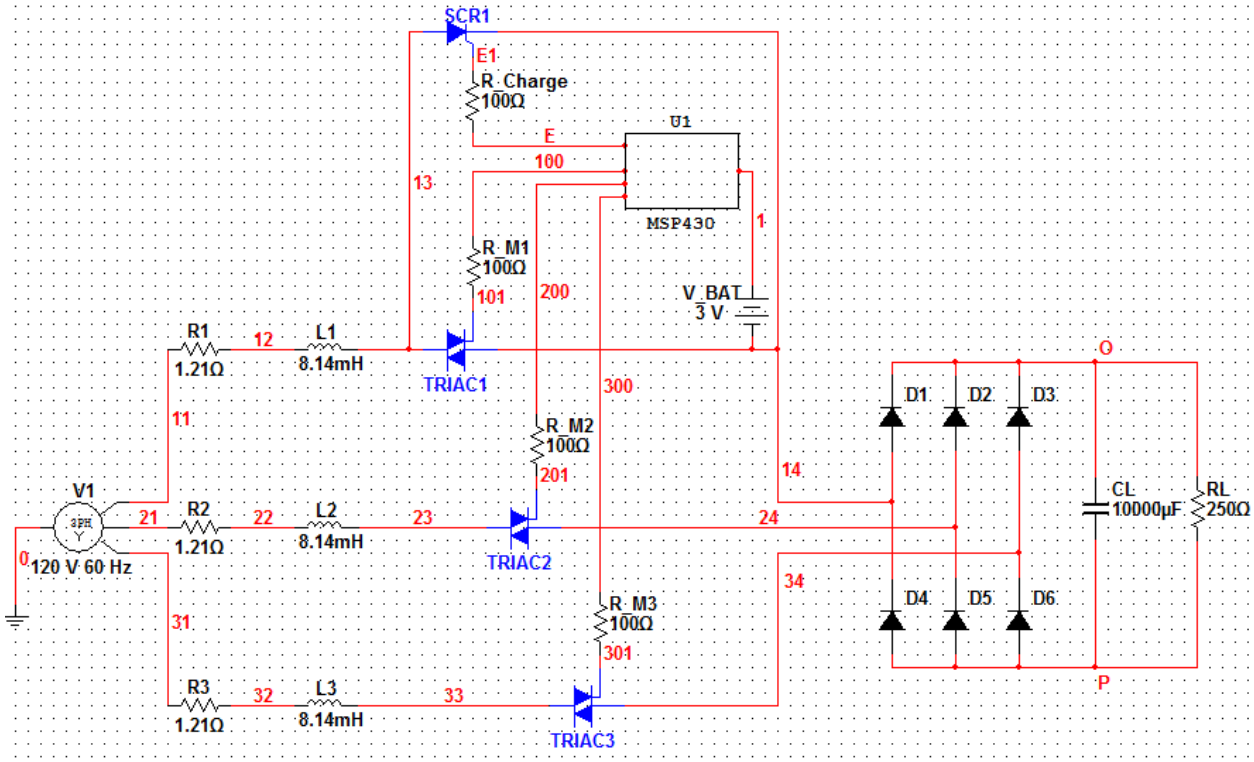

Figure 3.3 - Three-Phase Full-Wave Rectifier with Pre-Charging Circuit

3.2.Clock Source Generation

The signal of Figure 3.2 (above) is generated by the MSP430 Launchpad Microcontroller, which is driven by a comparator producing a signal that is synchronized with the input voltage phase. The circuit that will be driving the microcontroller has some design specifications, as well as some maximum ratings. The MSP430 microcontroller has an input voltage threshold of approximately 3.5V (See Appendix - MSP430 Documentation). The goal of our design was to take a standard 120V AC voltage and bring it down to a clean AC wave peaking at 3V. Although there are numerous options of DC/DC converter circuits to choose from, ranging from the use of switches and comparators to transformers and rectifiers, they all have their advantages and disadvantages.

3.2.1. Clock Source Generation Methods

Since the microcontroller needs to detect the positive zero-crossing of the input AC voltage, the best approach was to generate a square wave that would follow the sinusoidal input. However, this square wave needs to be precise, and must not have a phase shift introduced into it. In other words, because the microcontroller will be using a time precision of 0.1ms, the clock must be precise to less than 0.1ms.

One method to generate this clock was to implement a “super diode” or precision rectifier, as shown in Figure 3.4. The breakdown characteristic of the 2.4V Zener diode was the key to obtaining the sub-3V clock source, for the safety rating of the MSP430 Launchpad. However, this circuit requires the most physical electrical parts to construct and, because of the voltage drop across the negative feedback diode, the output square wave was not rising precisely on time.

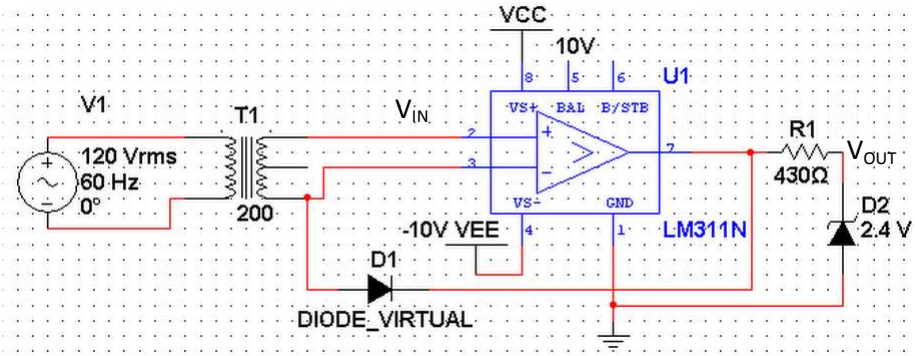

Figure 3.4 - Circuit Simulating a Precision Rectifier or “Super Diode”

Figure 3.5 shows that the output of the comparator starts rising approximately 0.3ms after the sinusoidal input crosses over to the positive half of the cycle:

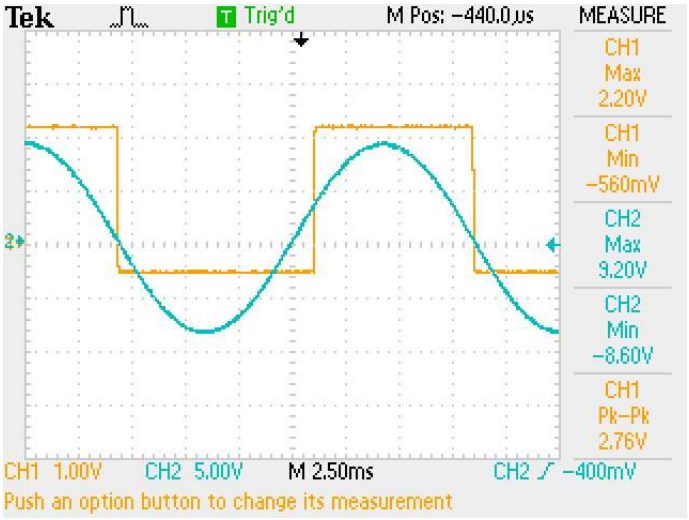

Figure 3.5 - Oscilloscope Measurements for Super Diode
CH1 = V_{IN} (Square), CH2 = V_{OUT} (Sinusoidal)

The next method implemented for the clock source generation, rectified the sinusoidal input by connecting a resistor in series with the Zener diode to obtain the low voltage at the specific time. As Figure 3.6 shows, the design required fewer components but had greater power losses due to the voltage drop across resistor.

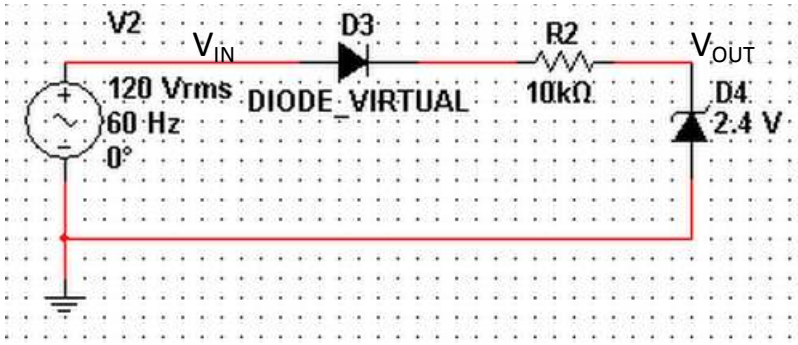

Figure 3.6 - Clock Generator with Rectifier

In addition, similar to previous clock source design method a time delay was observed, as Figure 3.7 shows:

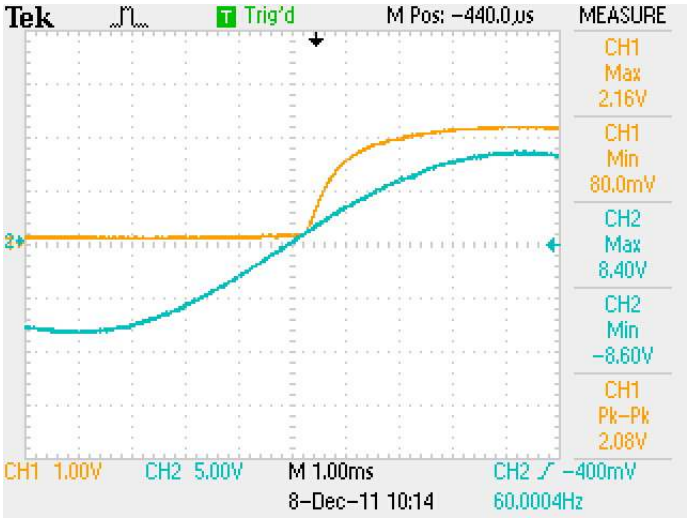

Figure 3.7 - Oscilloscope Measurements for Clock Generator with Rectifier
CH1 = V_{IN} (Rising edge), CH2 = V_{OUT} (Sinusoidal)

3.2.2. Final Clock Source Design

The Super Diode circuit from Figure 3.4 was modified to the circuit of Figure 3.8. This enhanced method provides a faster switching speed to meet the microcontroller specifications. The 120 VAC input will be brought down to approximately 6.3 VAC (RMS) using a transformer, in order to work within the operating conditions of the amplifier.

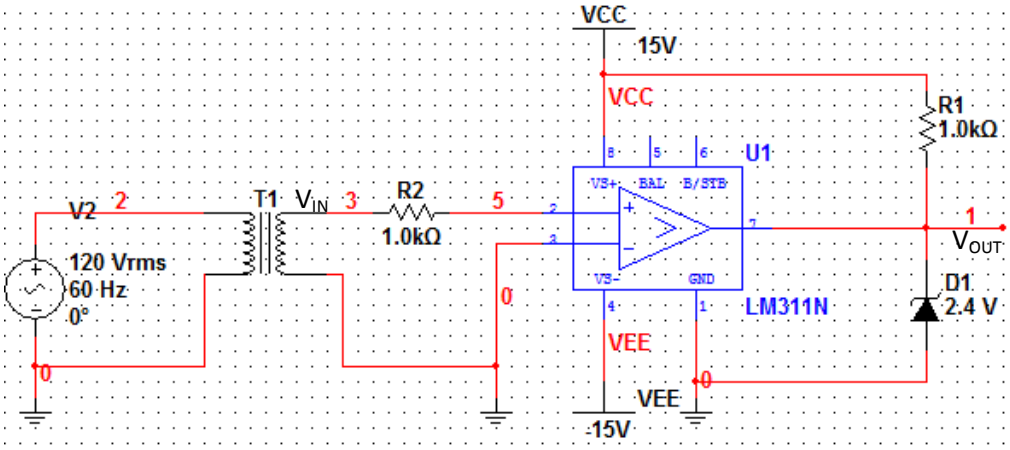

Figure 3.8 - Clock Source using Comparator

With this configuration, the comparator will ramp up to 2.4V when the input is positive, because of the Zener diode, and to zero when the input is negative. In addition, there will be no relevant delay in the switching. Figure 3.9 shows the output square wave of the comparator.

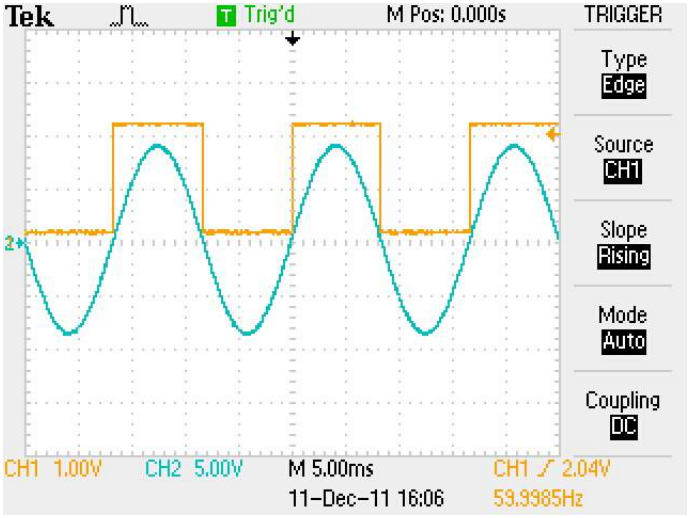

Figure 3.9 - Oscilloscope Measurements for the Comparator
CH1 = V_{IN} (Square), CH2 = V_{OUT} (Sinusoidal)

3.2.3. MSP430 Launchpad

The MSP430 gets a 60 Hz square wave described above from the comparator and then outputs the desired clock signal. This signal will be used to drive the SCR that would charge the load capacitor. The full C-code can be found in the Appendix, under *Microcontroller Code*. The functionality is described below.

The system will set the pins `P1.4` and `P1.5` as digital outputs, and `P1.7` to digital input. `P1.7` will be receiving the square wave from the comparator. `P1.5` will control the rectifying TRIAC after the load capacitor is charged up by the SCR controlled by `P1.4`.

Once `P1.7` receives the rising edge of the square wave, the system sets `Timer-A` to `SMCLCK` to count in the Up-mode, enables the interrupt, and sets the precision of the clock to 0.1ms.

Once `Timer-A` is ON, the variable `timerCount` is used to count up to 8.2ms. After that, the SCR will be triggered until the zero-crossing of the sine wave. Then, on the next rising edge, `timerCount` will count up to 0.1ms less than before. After the trigger time is decreased to 1.7ms (past the point where voltage is maximum) the SCR will stay OFF, and the TRIAC will be triggered to allow for the rectification to continue.

The behavior of this program was tested by connecting the microcontroller input to a 60 Hz square wave. This clock signal was first generated by a Tektronix AFG3021 Function Generator, but it was finally tested with the signal created by the comparator. Figure 3.10 and Figure 3.11 display the behavior of the programmed signal outputted by the MSP430 Microcontroller, driven by a 60 Hz AC source.

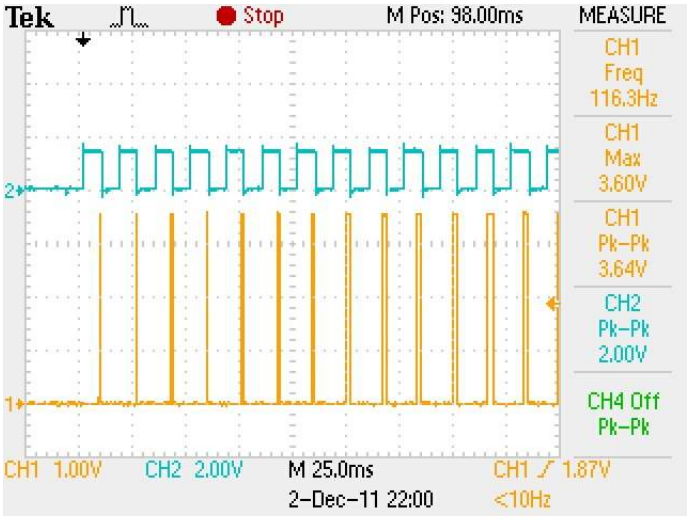

Figure 3.10 - Oscilloscope Measurements for MSP output signal
CH1 = V_{MSP}, CH2 = V_{SQ}

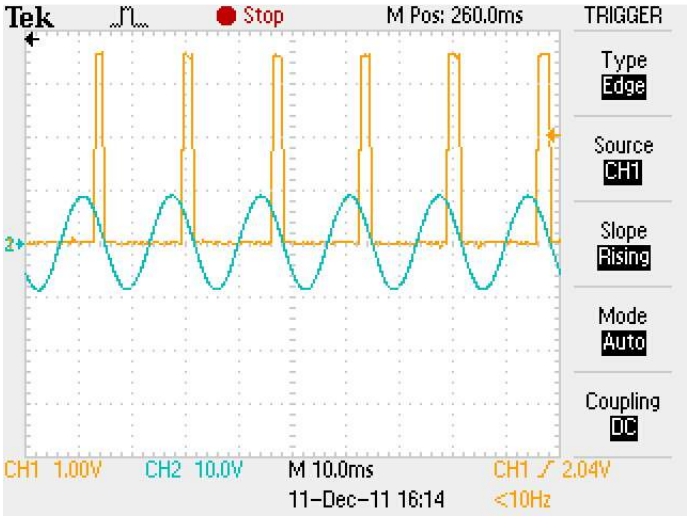

Figure 3.11 - Oscilloscope Measurements for MSP output signal
CH1 = V_{MSP}, CH2 = V_{SIN}

Figure 3.10 compares the MSP signal with the clock generated by the comparator (V_{SQ}), and Figure 3.11 compares it with the input sinusoidal wave (V_{SIN}).

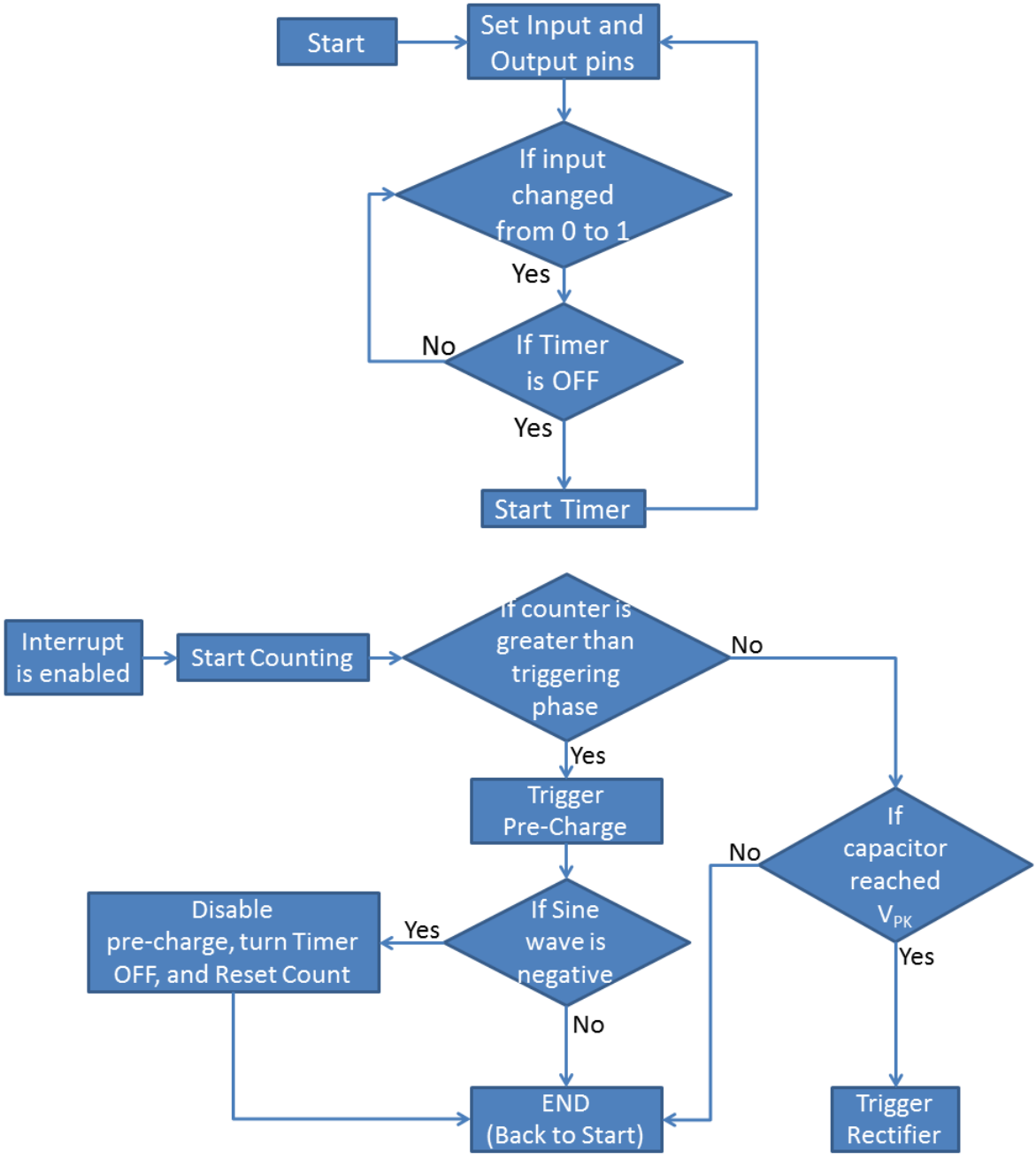

Figure 3.12 - C-Code Flow Diagram

4. Simulations

Every scenario described above was simulated using Cadence PSpice software, to assess the feasibility of physically implementing the system without risking safety or wasting time. The first system to be simulated was the full-wave bridge rectifier of Figure 4.1, in order to compare it to the other designs and evaluate their performances.

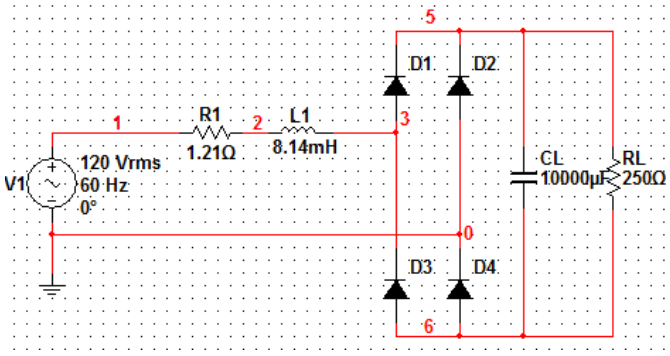

Figure 4.1 - Full-Wave Bridge Rectifier (Unprotected)

4.1. General Transient Behavior

The series impedance of R1 and L1 in Figure 4.1 represent the internal impedance of the power line, and the load impedance consisted on a parallel combination of a 10,000µF capacitor and a 250Ω resistor. Figure 4.2 and Figure 4.3 show the behavior of this system.

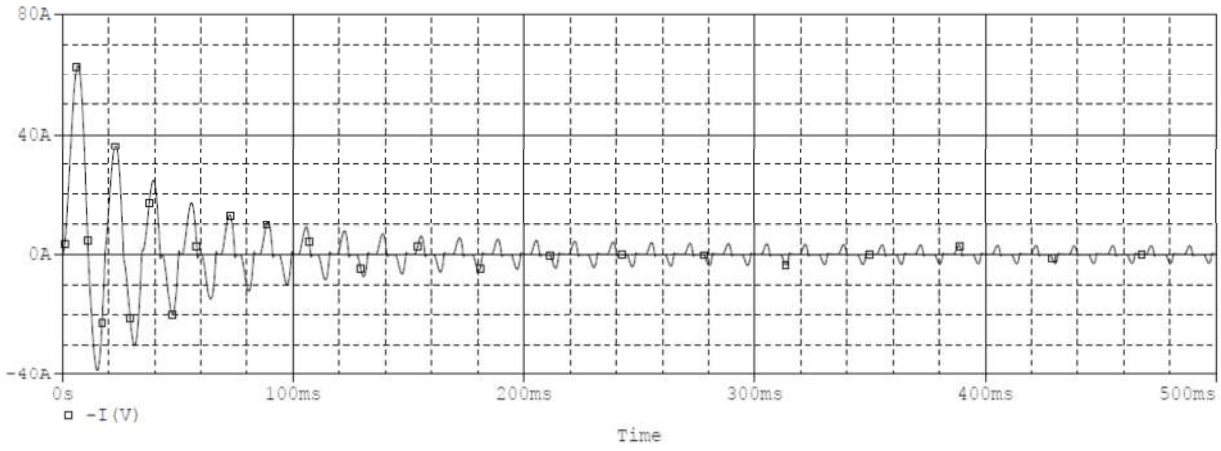

Figure 4.2 - Bridge Rectifier Inrush Current

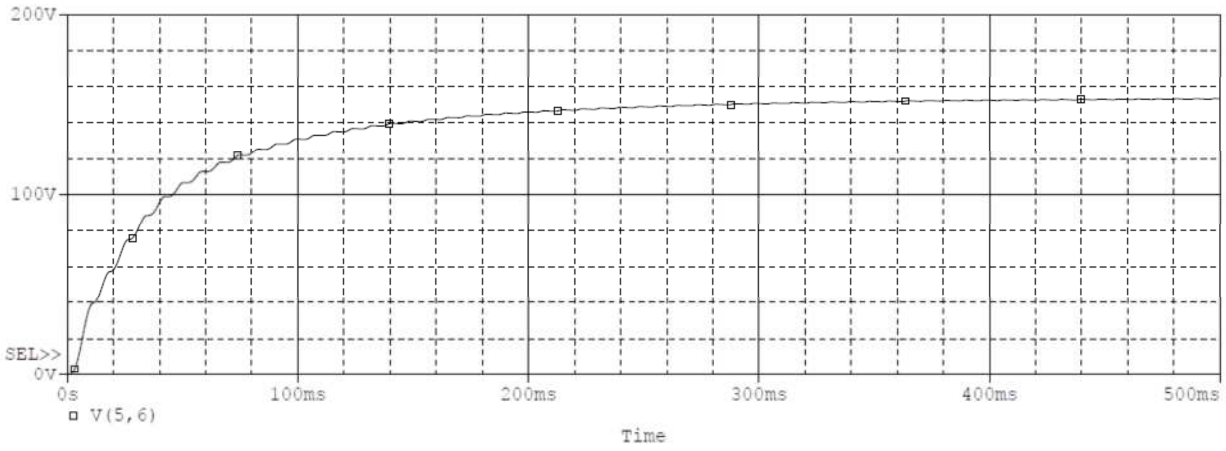

Figure 4.3 - Bridge Rectifier Load Voltage

Because the load capacitor has to be charged up to the maximum voltage supplied by the source before the system can go into steady state, a high current is drawn by the capacitor. From the simulation plot in Figure 4.2, this inrush current peaks at approximately 65A lasting for less than 5ms. Although this current does not last too long, it is still potentially harmful to other components in the system (i.e. contacts of a switch).

4.1.1. RL Circuit

The behavior of the RL circuit of section 2.3.1 was simulated before and after the mitigation technique. In such RL systems, the current lags the input voltage by the angle θ, determined by (2.3):

$$\theta = \tan^{-1}\left(\frac{2\pi * 60 * 0.008139}{1.2144}\right) = 68.41°$$

Figure 4.4 shows the simulated behavior of the system for firing angles $\alpha = 0°$ and $\alpha = \theta$. From these plots, the peak current in the first cycle is greater than the steady state for the top waveform. Once the circuit was energized at $\alpha = \theta$, the transient disappeared. (2.7) also confirms the sinusoidal behavior of the steady state current:

$$i_{ss}(t \to \infty) = \frac{100 * \sin(2\pi * 60 * t)}{\sqrt{(2\pi * 60 * 0.008139)^2 + 1.2144^2}} = 29.06\sin(2\pi * 60 * t)\ [A]$$

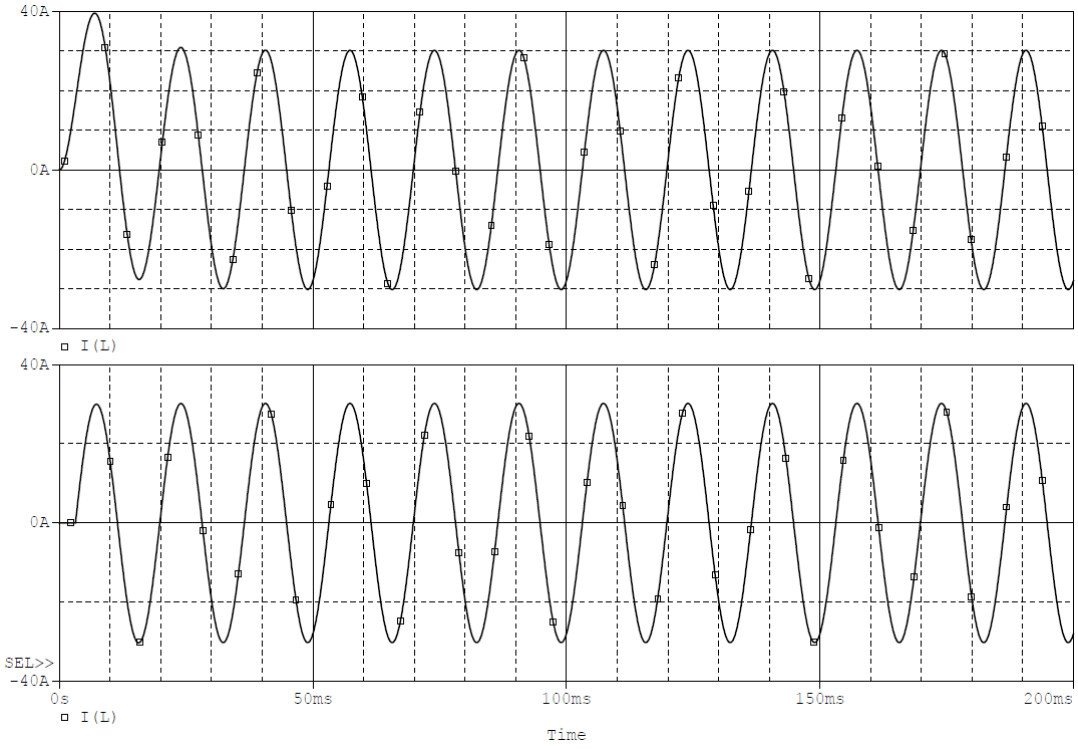

Figure 4.4 - RL Circuit Current
α = 0º (Top)
α = θ (Bottom)

4.1.2. LC Circuit

The behavior of the LC circuit in section 2.3.2 was also simulated. And Figure 4.5 shows the behavior of the system; the capacitor voltage and the current through the system oscillate at the resonant frequency $f_R = \frac{1}{2\pi\sqrt{0.0002*0.01}} = 112.54\ Hz$, in addition to the $60Hz$ of the sinusoidal input.

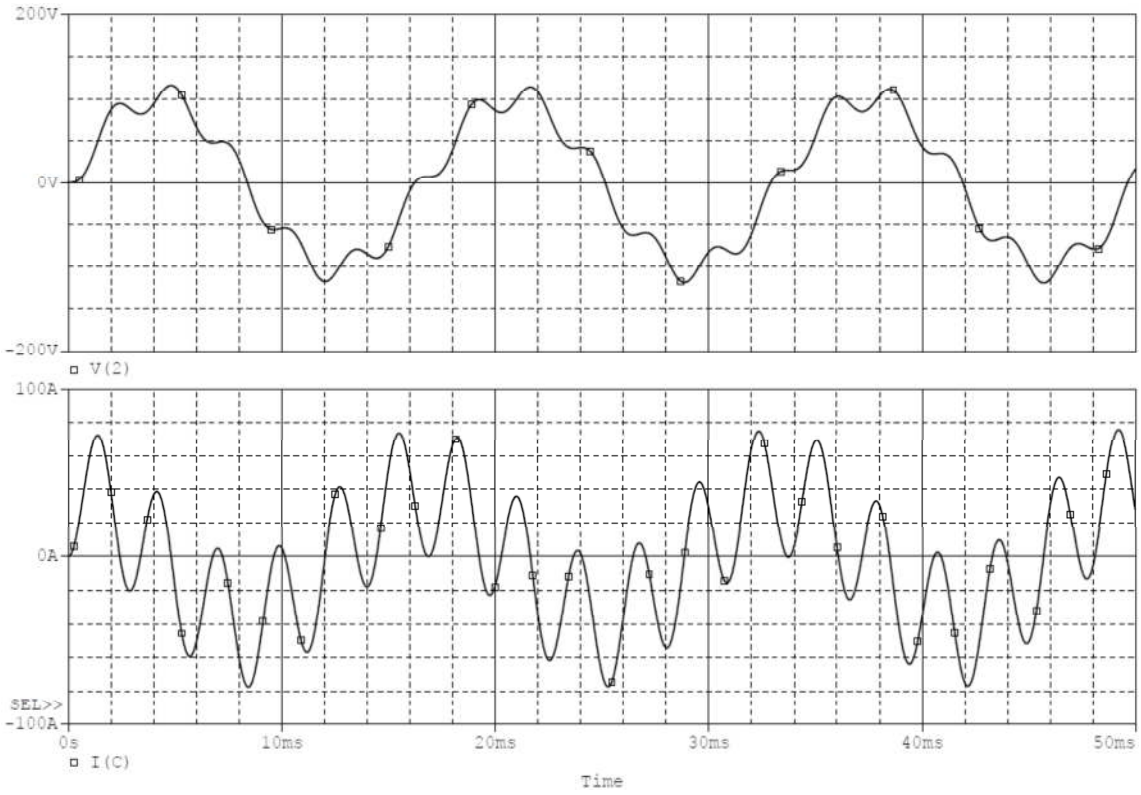

Figure 4.5 - LC Circuit Behavior ($V_C(0) = 0V$)
Current (Top), Capacitor Voltage (Bottom)

If the circuit of Figure 2.4 was to be modified with a rectifying diode as shown in Figure 4.6, then the current will flow into the capacitor and the diode would avoid the current from discharging the capacitor, and this inrush current could be mitigated by previously charging the capacitor.

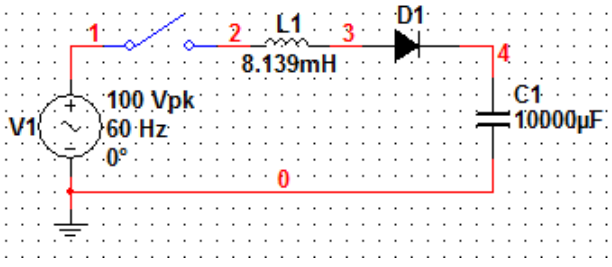

Figure 4.6 - LC Circuit with Rectifying Diode

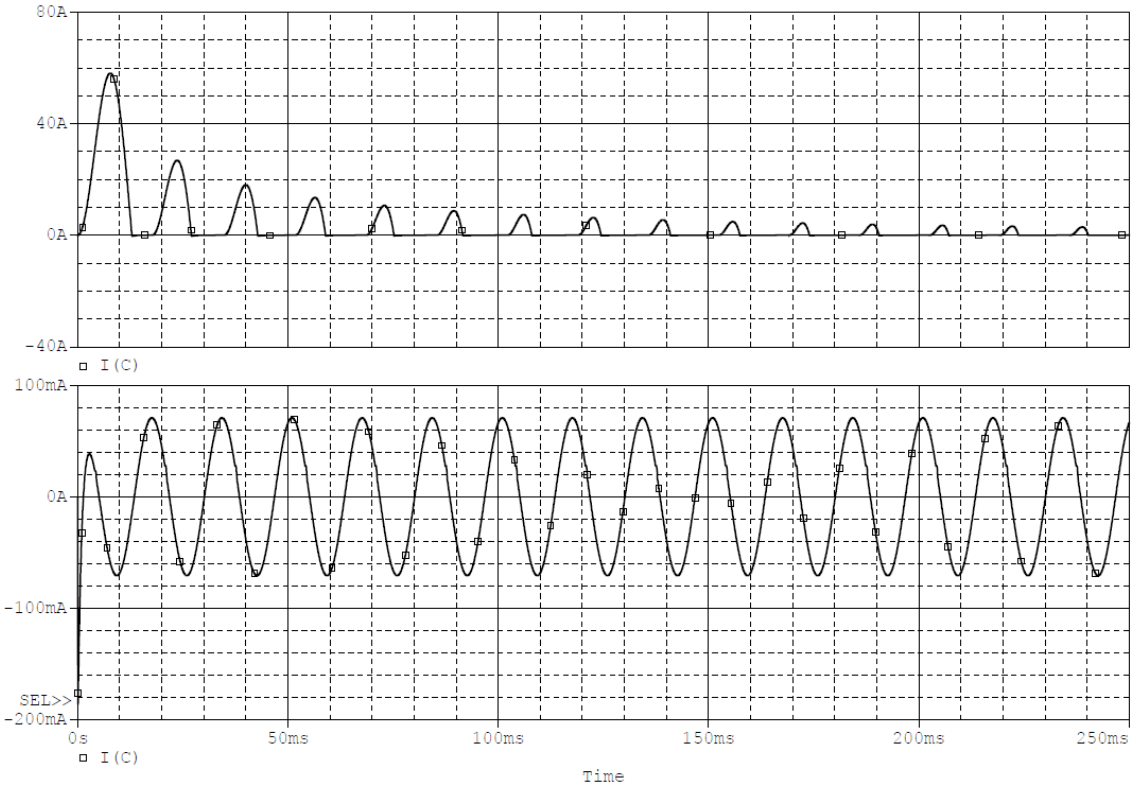

Figure 4.7 - LC Rectified System Behavior
V_C = 0V (Top)
$V_C = V_{PK}$ (Bottom)

Figure 4.7 shows the current through the capacitor for the conditions when the capacitor is completely discharged and when it is charged up to the input voltage. When the capacitor is discharged, the current peaked at about 50A. When the capacitor was previously charged, the current started in a steady state, oscillating at f_R and peaking at 100mA.

4.2.Current Limiting Impedance

The circuit design with the current limiting impedance yielded fairly strong results for reducing the inrush current, but not without consequence. For these specific simulations, the current limiting resistance and inductance were chosen to be 5Ω and 15mH, respectively.

Figure 4.8 through Figure 4.11 show the behavior of the circuit with a current limiting resistor, and with a current limiting inductor. On each figure, the graphs show the input current and the load voltage versus time.

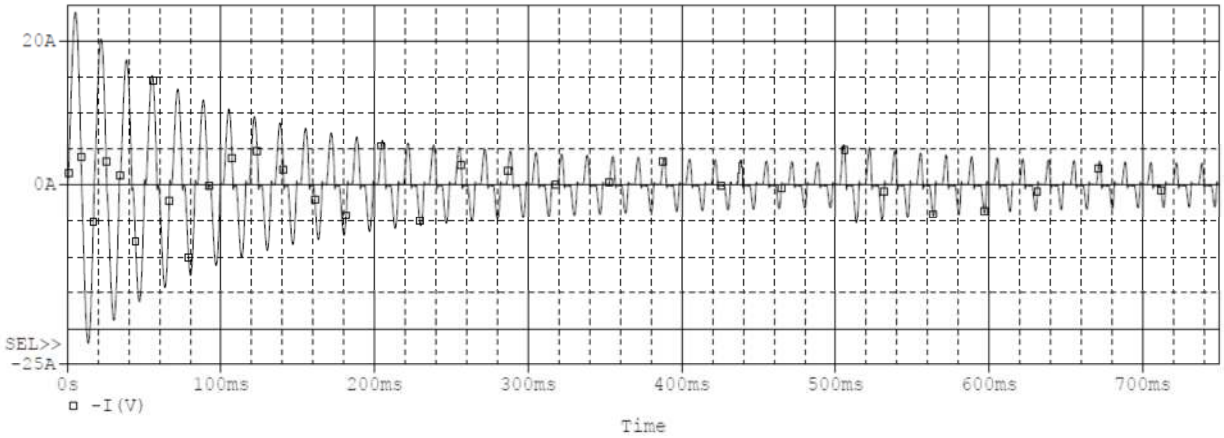

Figure 4.8 - Bridge Rectifier Current (with 5Ω Current Limiting Resistor)

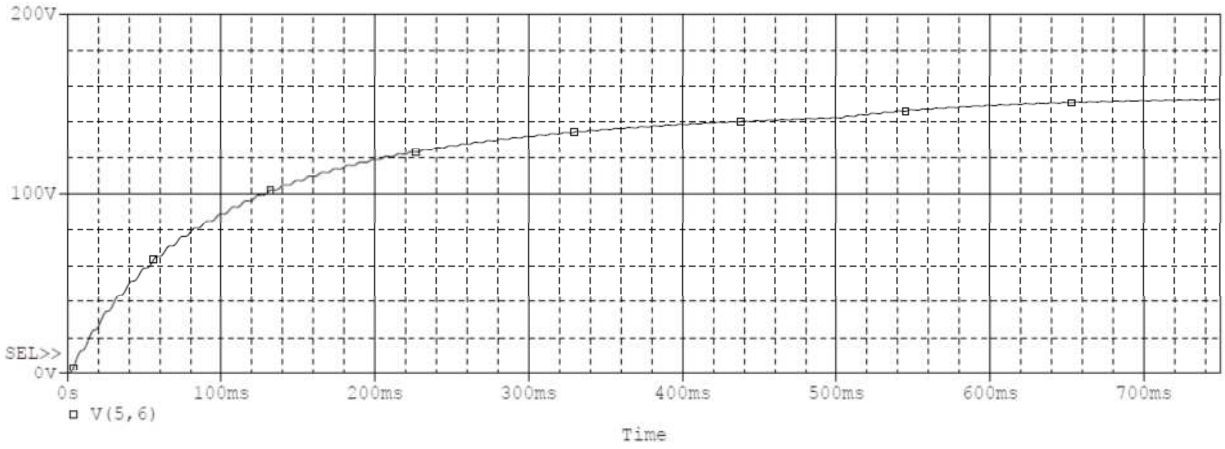

Figure 4.9 - Bridge Rectifier Load Voltage (with 5Ω Current Limiting Resistor)

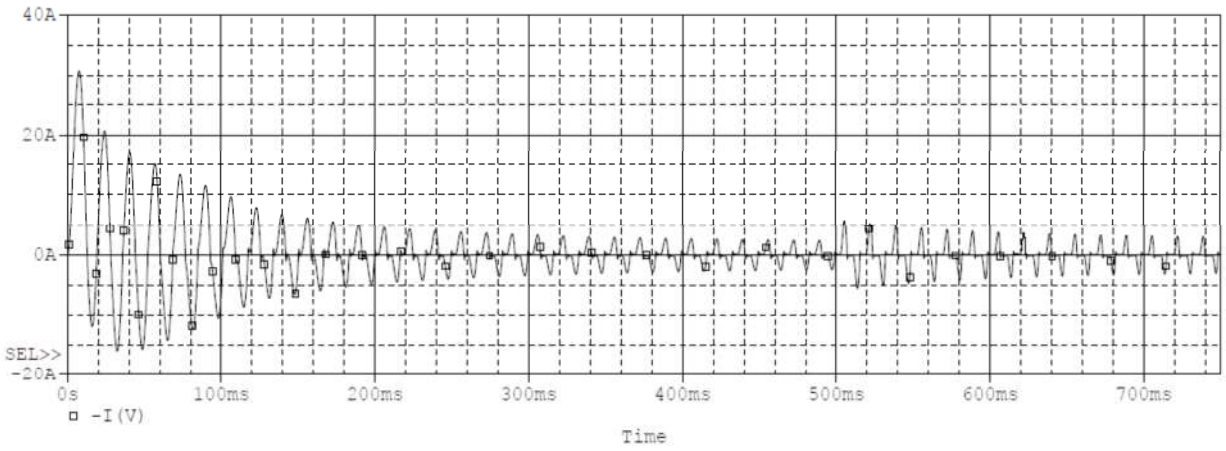

Figure 4.10 - Bridge Rectifier Current (with 15mH Current Limiting Inductor)

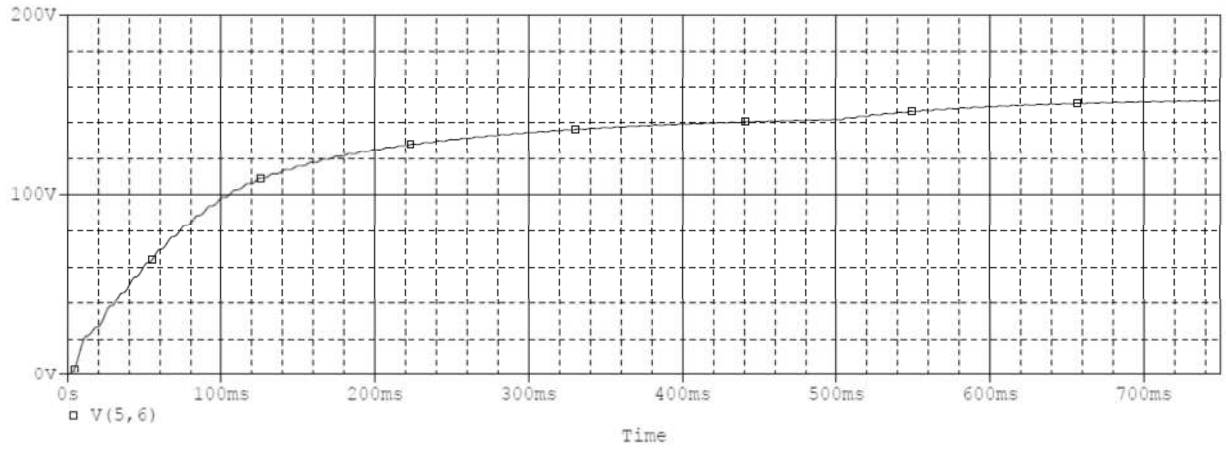

Figure 4.11 - Bridge Rectifier Load Voltage (with 15mH Current Limiting Inductor)

Although the current limiting impedances lowered the current to a peak of approximately 30A in the later circuits, this outcome had a cost. The peak current was reduced, but the current limiting impedances caused a significant voltage drop while they were active in the circuit, which is translated into unnecessary power losses; while the current limiting impedance is suppressing the current, the power losses are approximately 600 Watts.

Choosing the appropriate value for these impedances involves a tradeoff: the inrush current could be reduced, but once the impedance is bypassed, the voltage drop across that impedance could cause another inrush current. If the impedance is small, then the inrush current would not be significantly reduced, but there will not be a surge current after bypassing it. On the other hand, if the impedance is sufficiently high, the inrush current will be significantly reduced, but there will be a high current once the impedance is bypassed because of the voltage drop across the impedance. The balance for choosing this impedance happens when the voltage drop across the impedance is half of the peak voltage that the capacitor can be charged to, where $V_Z = V_{C_{PK}}/2$.

4.3.Phase-Delayed Switching

The shunt impedance method is not very efficient because it increased power losses. The next system to be simulated was the phase-delayed switching. Although this system does not mitigate the inrush current significantly, the inrush peak is still reduced.

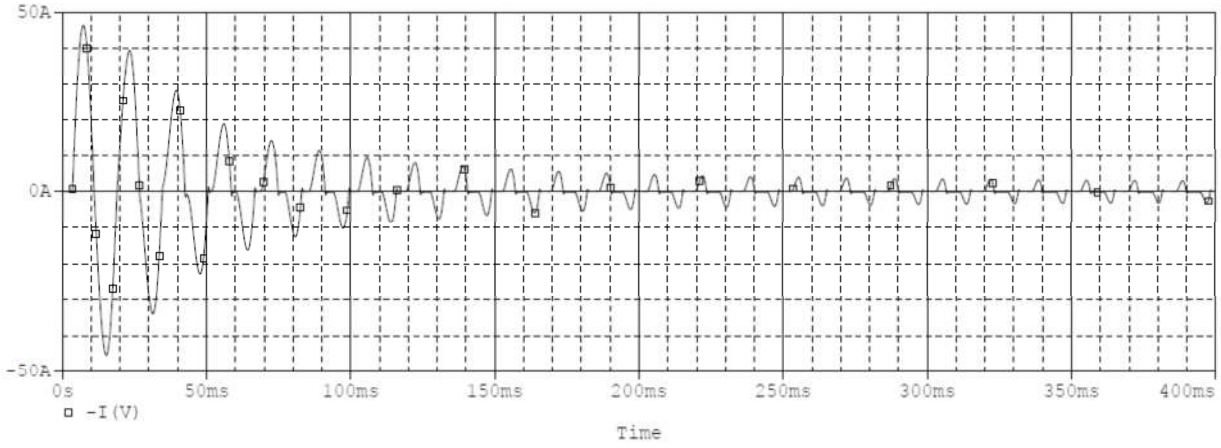

Figure 4.12 - Bridge Rectifier Inrush Current (with Phase-Delayed Switching)

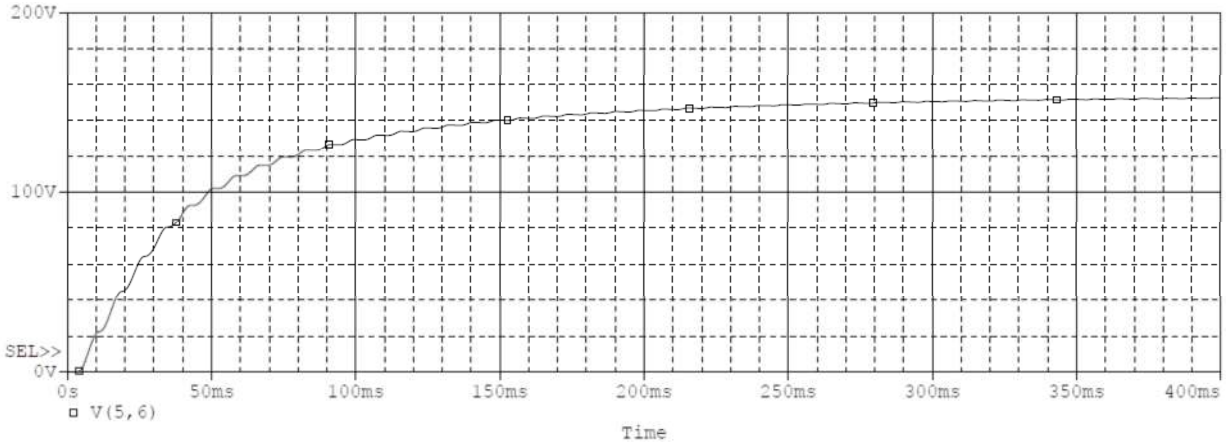

Figure 4.13 - Bridge Rectifier Load Voltage (with Phase-Delayed Switching)

Figure 4.12 and Figure 4.13 show the input current and the load voltage for the system when it is triggered at a phase of 75º. This shows that, in the best case scenario, the current can be mitigated by a factor of approximately $\sqrt{2}/2$. This is because the capacitor needs to be fully charged before going into steady state, and hence suppressing the inrush current, and one cycle is not enough time due to the time constant:

$$Z_{IN} = \sqrt{R1^2 + (2\pi f L)^2} = 3.3\ \Omega$$
$$Z_{IN} C_L = 3.3 * 0.01 = 33\ ms$$
$$5\tau = 165 ms$$

4.4.Time-Delayed Switching with Pre-Charging Circuit

After analyzing the previous methods, the pre-charging circuit was simulated, triggering the rectifier once the capacitor was fully charged. Figure 4.14 and Figure 4.15 below, show the current that charges the capacitor once the circuit is energized, as well as the voltage across the load capacitor.

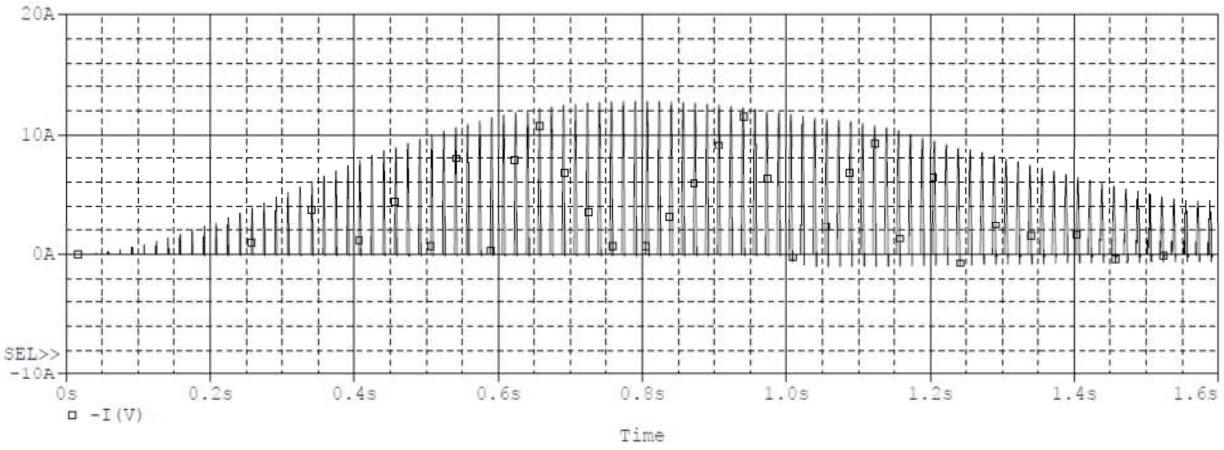

Figure 4.14 - Current Drawn to Pre-Charge the Load Capacitor

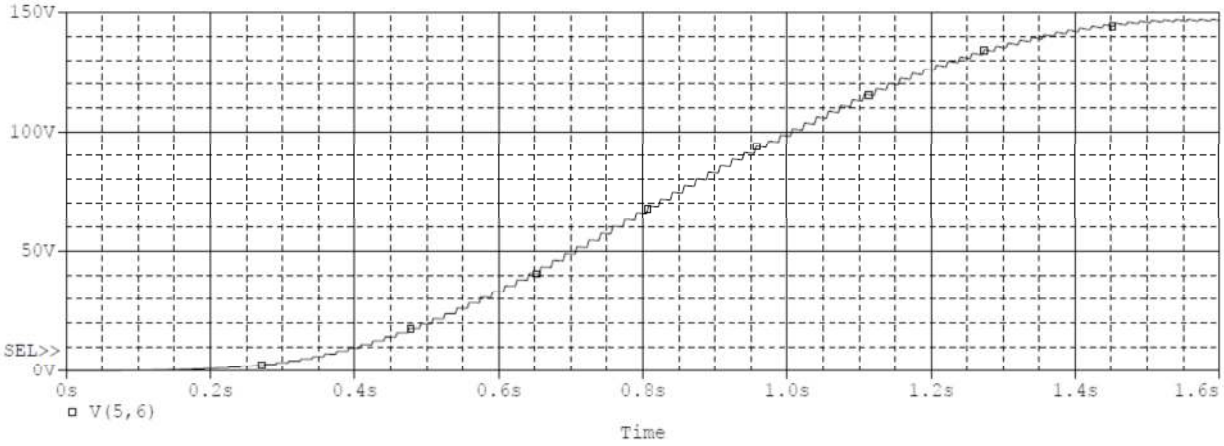

Figure 4.15 - Pre-Charging Voltage across the Load Capacitor

Figure 4.16 and Figure 4.17 show the peak inrush current and the voltage across the load capacitor, once the system has pre-charged the load.

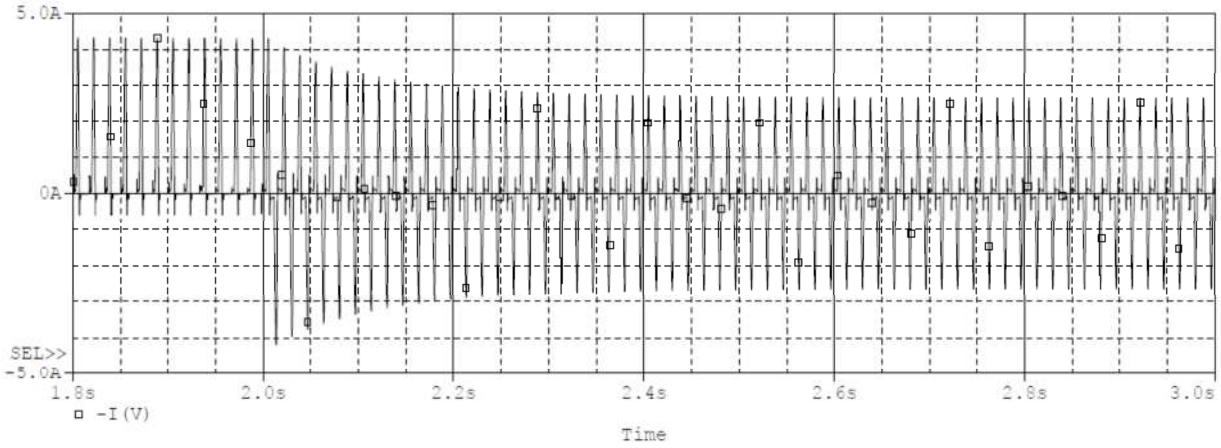

Figure 4.16 - Current Peak after Charging Load Capacitor

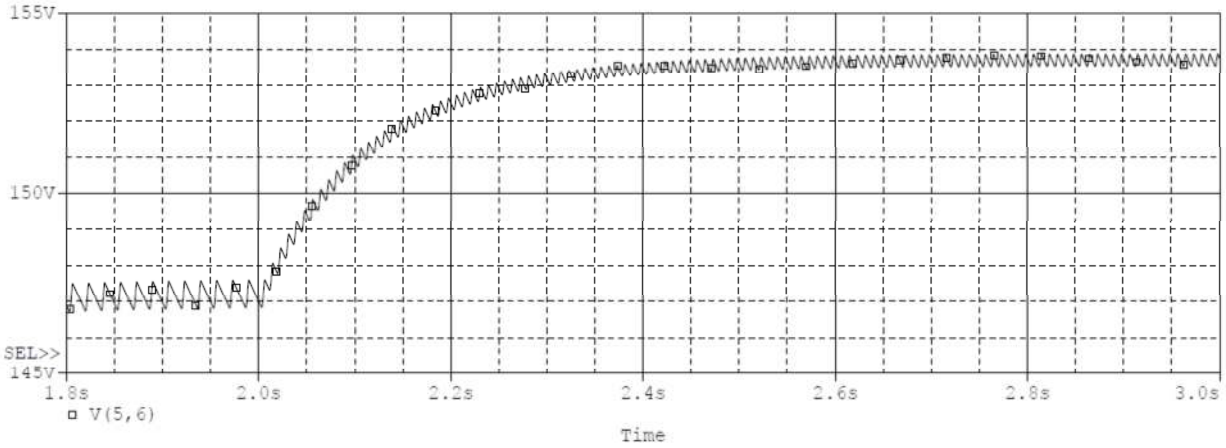

Figure 4.17 - Load Voltage after Charging Load Capacitor

Compared to the results obtained from the unprotected circuit (Figure 4.2), these results reveal the significance that the pre-charging circuit has on the efficiency of the system. The maximum current peak was reduced to approximately 13A, and the starting rectifying current (once the capacitor was fully charged) was reduced from 65A down to roughly 4A.

4.4.1. Three-Phase System Application

Since Three-Phase systems are more common than Single-Phase ones in high power applications, the designed method was also simulated on a Three-Phase system.

Initially, the three-phase circuit was simulated with no protection and the resulting current and the load voltage are shown below in Figure 4.18 and Figure 4.19:

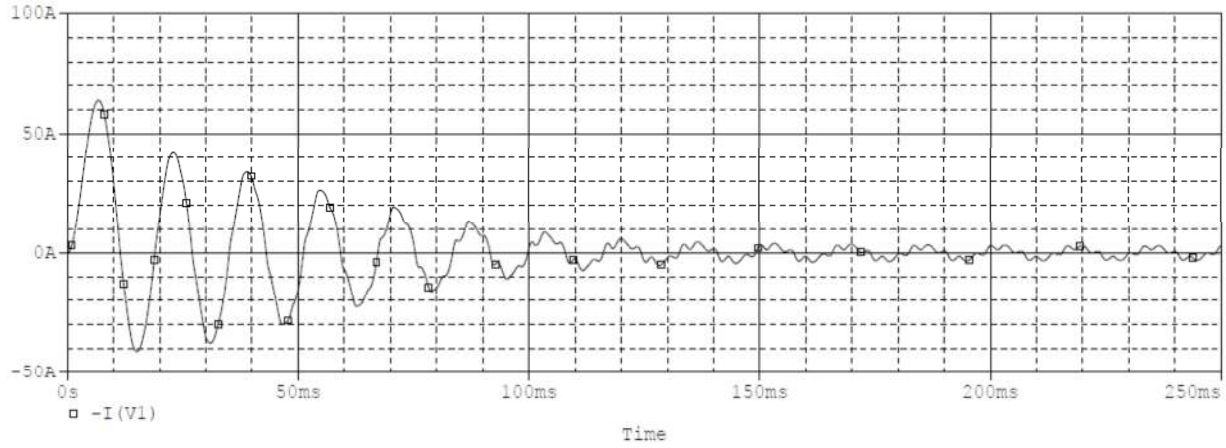

Figure 4.18 - Bridge Rectifier Inrush Current (Three-Phase System)

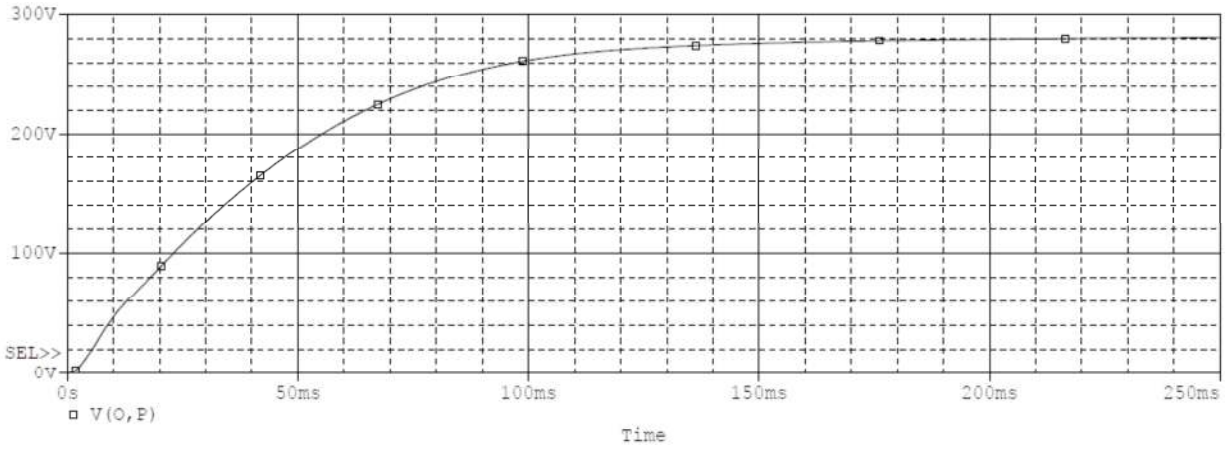

Figure 4.19 - Bridge Rectifier Load Voltage (Three-Phase System)

Since these systems consist of three different sources with different phases, the power ratings are much higher especially because the line-to-line voltage is $294\ V_{PK}$. From the simulation plot, the inrush current peaks at approximately 65A.

Similar to the single-phase system, the three-phase system showed significant improvement once the pre-charging circuit was implemented. Figure 4.20 and Figure 4.21 show the current and the load voltage of the system while the load capacitor is being charged.

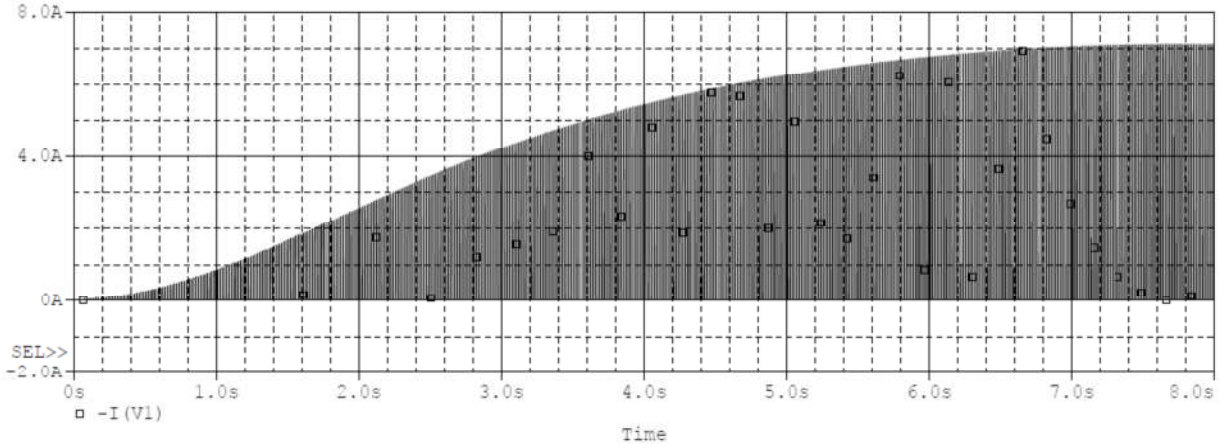

Figure 4.20 - Current Drawn to Pre-Charge the Load Capacitor (Three-Phase System)

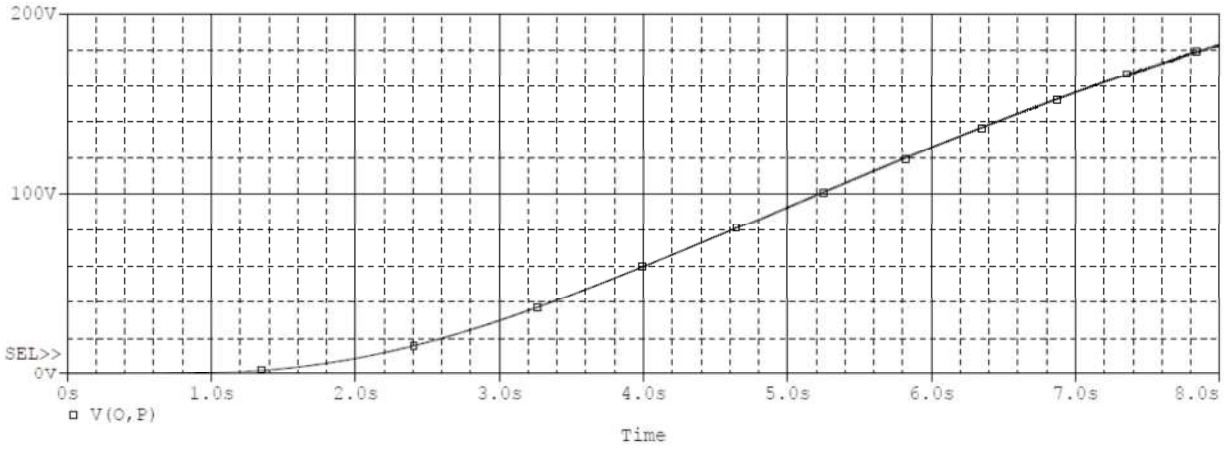

Figure 4.21 - Pre-Charging Voltage across the Load Capacitor (Three-Phase System)

Figure 4.22 and Figure 4.23 show inrush current and the load voltage after the capacitor has been pre-charged.

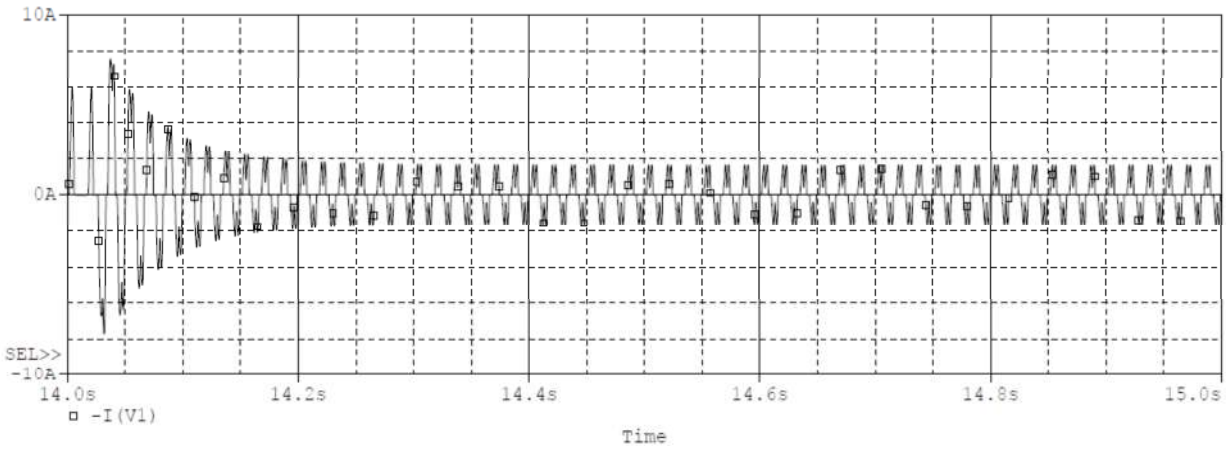

Figure 4.22 - Current Peak after Charging Load Capacitor (Three-Phase System)

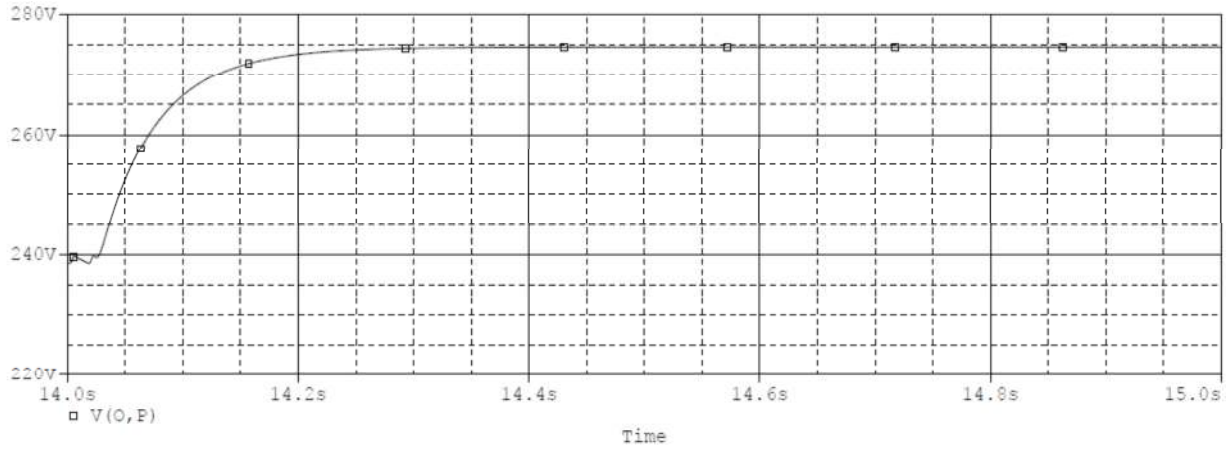

Figure 4.23 - Load Voltage after Charging Load Capacitor (Three-Phase System)

After the modification, the peak inrush current of 65A (Figure 4.18) was reduced to approximately 8A, with the voltage across the load reaching the maximum value in about 14 seconds.

The time it takes to charge up the capacitor before triggering the rectifier depends on the specified current ratings of the SCR that charges the capacitor; for pulses of greater amplitude, the time to charge would be smaller, and vice versa.

5. Results

5.1. Power Factor Analysis

One of the major deliverables of our inrush current limiting efforts was to maintain a good power rating even in our attempts to lower the initial dangerous current spikes. In order to take into account the effects of internal impedance in power lines, we added a series RL combination of a 1.2Ω resistance and an 8.14mH inductance.

Understanding the short circuit power analysis gives insight into the input power of our system. The short-circuit power is given by (5.1):

$$S_{sc} = \frac{V^2}{Z_{(MVA)}}\ [VA]$$
$$Z = \sqrt{R^2 + (\omega L)^2}\ [\Omega] \qquad (5.1)$$

After applying the equations above with the inductance, resistance and frequency of $2\pi 60 \cong 377$ from our AC voltage supply of 120Vrms, we were able to calculate the estimated input impedance and power ratings. The short circuit power rating (S_{sc}) was calculated to be:

$$S_{SC} = \frac{120^2}{\sqrt{1.2^2 + (377 * 0.00814)^2}} = 4{,}634.75\ VA$$

Next, we explored the output rating at DC due to the fact that our system contains a full-wave rectifier bridge. The rectifier will create measurable power losses which can be seen by looking at comparison between final output power and the previously measured input power. (5.2) governs the output DC power rating:

$$P_{OUT} = \frac{{V_{dc}}^2}{R_{LOAD}}\ [W] \qquad (5.2)$$

The measured DC voltage tapers off to approximately 167V steady state with a <10% ripple, while the load resistance used for testing was 250Ω. Using the measured values, the output power was calculated:

$$P_{OUT} = \frac{167^2}{250} = 111.556\ W$$

This meant that in the short period of time between the capacitor starting at 0 V and charging up, approximately 114.87 Watts would be dissipated through the rectifier circuit and the internal impedance of the power supply. These measurements also yielded the following power factor

$$\frac{P_{OUT}}{S_{SC}} = \frac{111.556\ W}{4{,}363.75\ VA} * 100\% = 2.56\%$$

5.2.Inrush/Steady-State Current Ratio

In order to visualize the effect of our efforts to reduce the inrush current we created current ratio variable that we could graph. The current ratio (K_I) represents the ratio of peak inrush current to peak steady-state current.

$$K_I = \frac{I_{inrush}}{I_{steady-state}} \tag{5.3}$$

At time $t = 0$, when the circuit was closed, the load capacitor behaved as a short circuit causing a high inrush current. Figure 5.1 and Figure 5.2 respectively show the current behavior when the capacitor was charging, and when the load current came to a steady state.

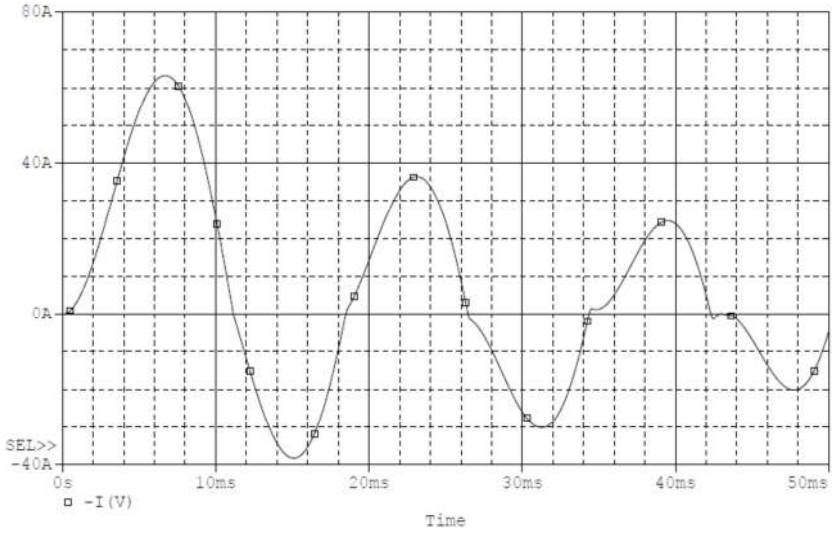

Figure 5.1 - Peak Inrush Current

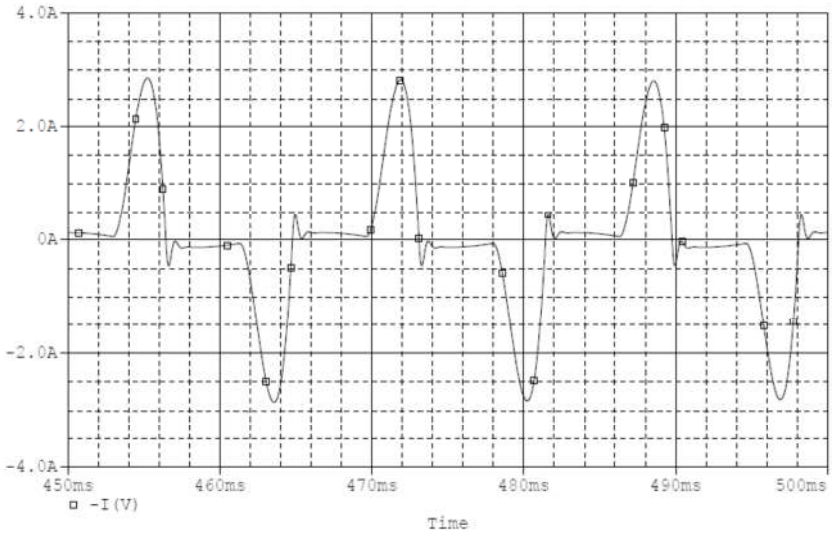

Figure 5.2 - Steady State Current

The main goal was to reduce the inrush current to have a current ratio (K_I) that is closer to unity. From Figure 5.1, the current peaked at approximately 64.65A, and from Figure 5.2 the

current stabilized to a steady state peak of approximately 2.68A. These measurements yielded a current ratio $K_I = \frac{64.65}{2.68} = 24.08$

5.2.1. Current Limiting Impedance

With the 5Ω shunt resistor being bypassed after 5 seconds, the current factor was reduced to 1.58. Similarly, with the 15mH inductor being part of the circuit, the current factor was approximately 1.80 after the inductor was bypassed after 5 seconds. However, during those 5 seconds when either the resistor or the inductor was part of the circuit, the power dissipated was approximately 600 Watt across each impedance.

5.2.2. Time-Delayed Switching with Pre-Charging Circuit

Finally, with the pre-charge design, the current surge was limited by several short pulses peaking at 5.57A. Once the capacitor was charged up and the circuit was closed, starting the rectification, the first current pulse peaked around 4.49A, stabilizing to a steady state current of approximately 2.65A, yielding a 1.70 current factor. Table 5.1 summarizes the final conclusions.

Table 5.1 - Current Measurements for Different Mitigation Methods

Technique Used	I_{SURGE} (A)	$I_{STEADY-STATE}$ (A)	K_I
Control	64.65	2.68	**24.08**
5Ω CLR	4.17	2.65	**1.58**
15mH CLI	4.77	2.65	**1.80**
Pre-Charging Cap	4.49	2.65	**1.70**

5.3. Quantified Results

The current factor (K_I) of each mitigation technique was plotted versus the factor S_{SC}/P_{OUT} for the different time constants (τ) of distinct load conditions.

From these plots (Figure 5.3 to Figure 5.6), it can be seen that as the short circuit apparent power increases, the ratio of inrush versus steady-state current increases exponentially. Similarly, as the time constant is increased, the current ratio increases in magnitude.

The data belonging to the capacitor pre-charging technique (Figure 5.6) does not show this behavior. However, the current factor K_I is within a very small range (from 1.5 to 1.95).

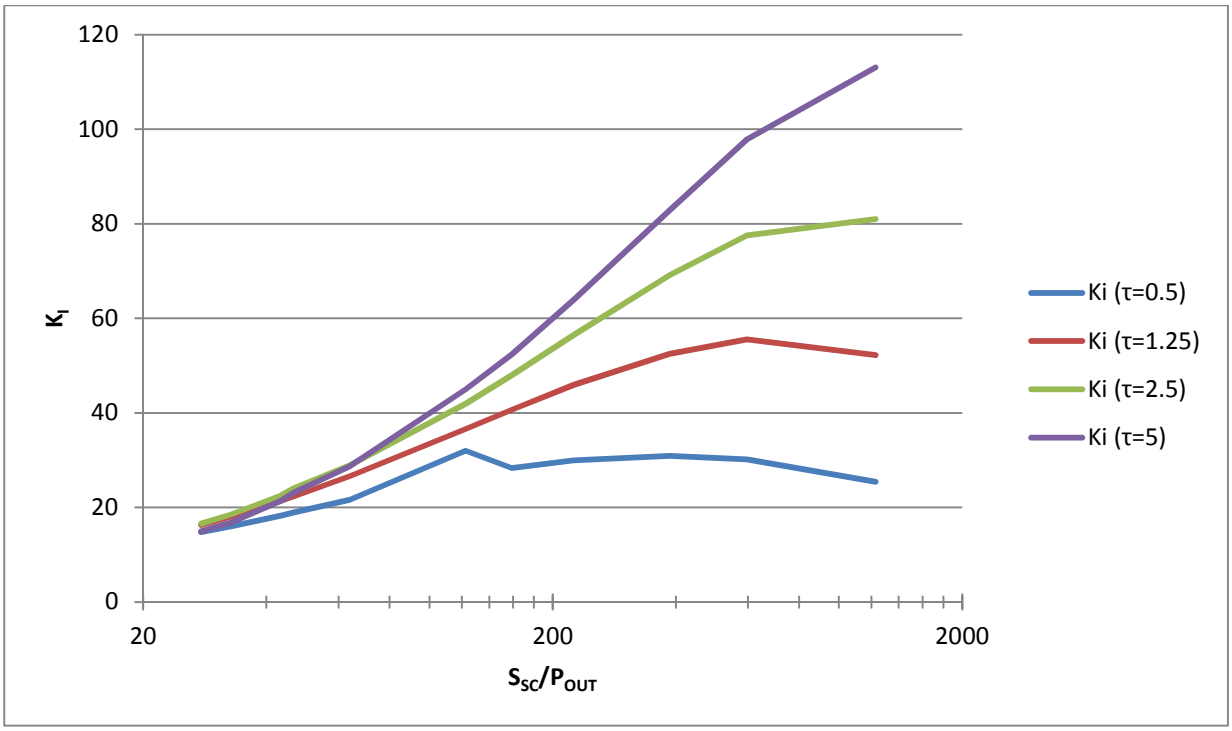

Figure 5.3 - K_I S_{SC}/P_{OUT} for Control Circuit

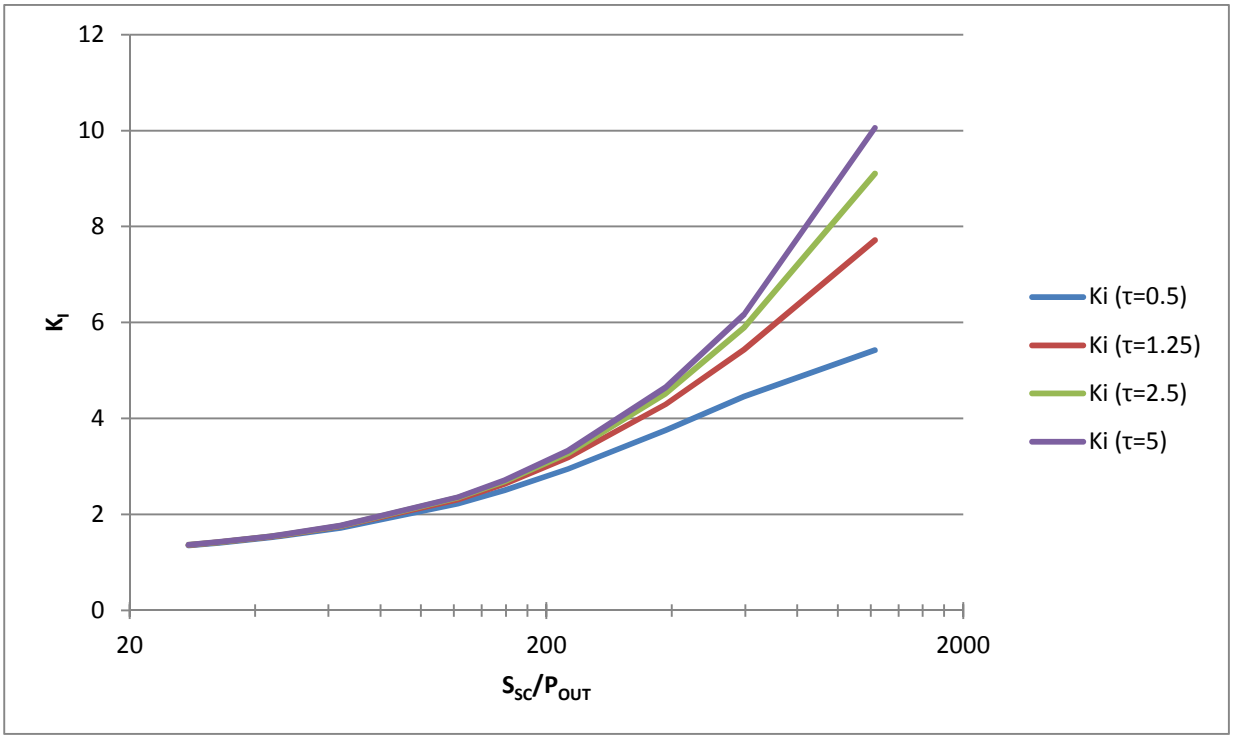

Figure 5.4 - K_I S_{SC}/P_{OUT} for 5Ω CLR Circuit

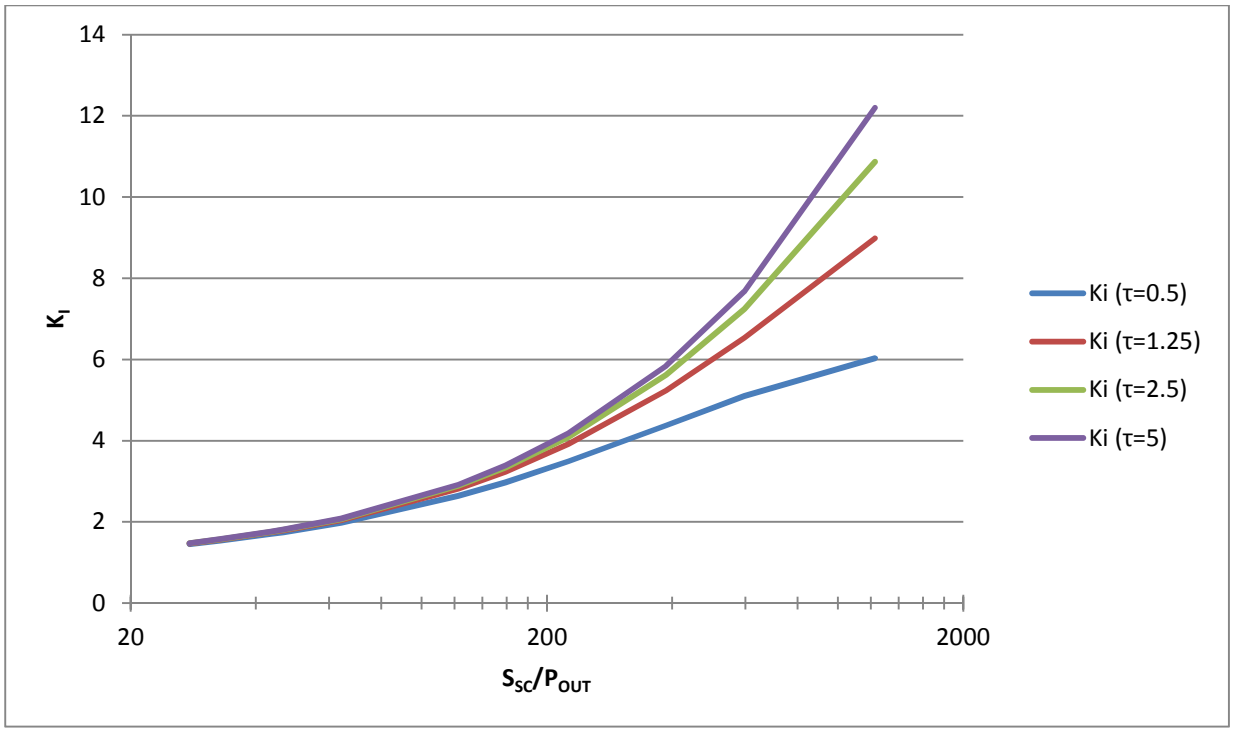

Figure 5.5 - K_I S_{SC}/P_{OUT} for 15mH CLI Circuit

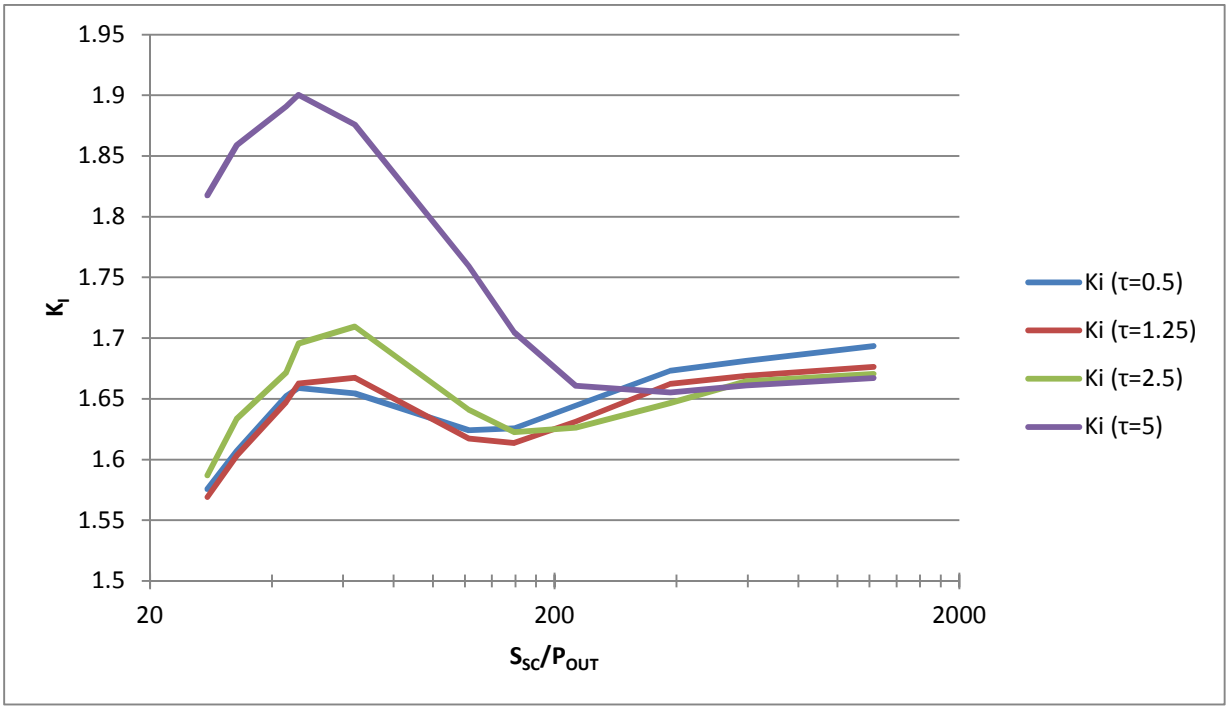

Figure 5.6 - K_I S_{SC}/P_{OUT} for Pre-Charging Capacitor Circuit

5.4.Experimental Results

The design approach was physically tested, specifically using the single-phased bridge rectifier circuit. All the measurements were done with the GW INSTEK GDS 2062 Digital Oscilloscope.

To evaluate the effectiveness of the design, the current of the control system and the pre-charging module were compared, as well as the voltage across the load.

5.4.1. Control Circuit

When the control circuit was energized, the oscilloscope recorded the voltage across the capacitor in Figure 5.7. The capacitor was charged up to 150V in less than 250ms after triggering the circuit.

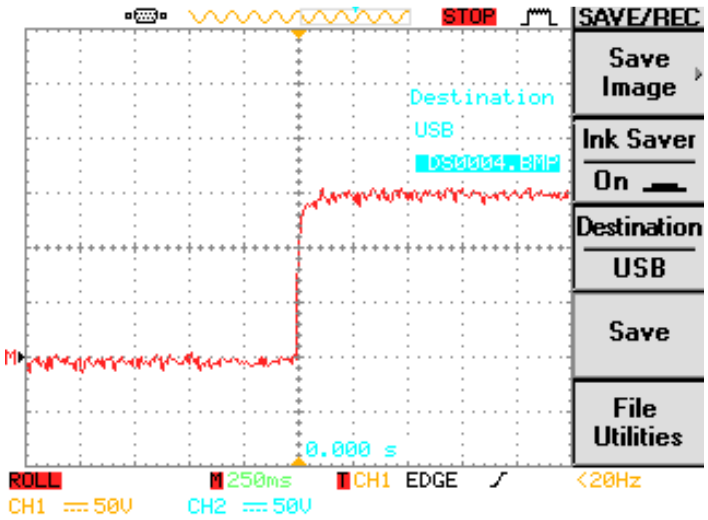

Figure 5.7 - Bridge Rectifier Load Voltage

A current transformer was used to measure the current. The primary coil was connected in series with the supply in order to precisely measure the current being drawn by the system. The current transformer had a turn ratio of 100:5, and a high precision resistance of 0.182Ω was connected to the secondary coil. Therefore the current drawn by the system, as a function of the voltage drop across the resistance is given by (5.4):

$$I = \frac{V_R}{0.182\Omega} * \frac{100}{5} \tag{5.4}$$

Due to the rapid change in voltage across the capacitor, the current needed to charge the capacitor exceeded 100A in more than one cycle. Using (5.4), the peak current measured in Figure 5.8 was calculated:

$$I_{PK} = \frac{(3.5 * 500mV)}{0.182\Omega} * \frac{100}{5} = 192.31A$$

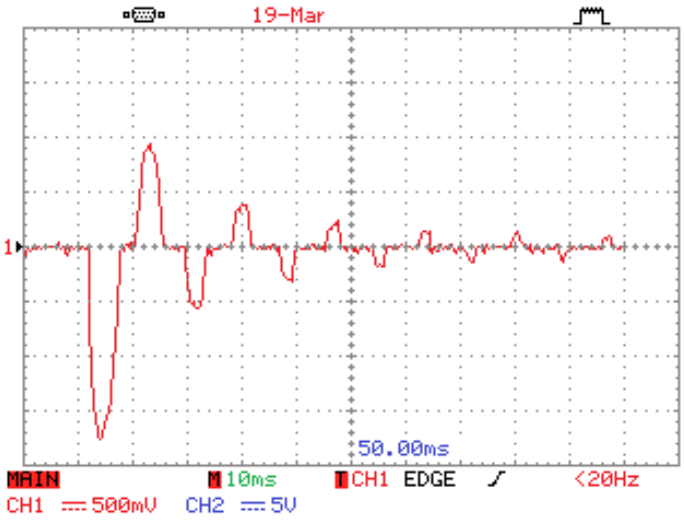

Figure 5.8 - Bridge Rectifier Input Current

This current, initially peaking at 192.31A, lasts for 8.33ms, and has the potential to damage several components in the system, including welding the contacts of a switch.

This system eventually reaches steady state, once the capacitor is completely charged. The steady state current drawn by this system with a load of 250Ω is shown in Figure 5.9. This current peak was also calculated:

$$I_{SS} = \frac{(3.5 * 20mV)}{0.182\Omega} * \frac{100}{5} = 7.7A$$

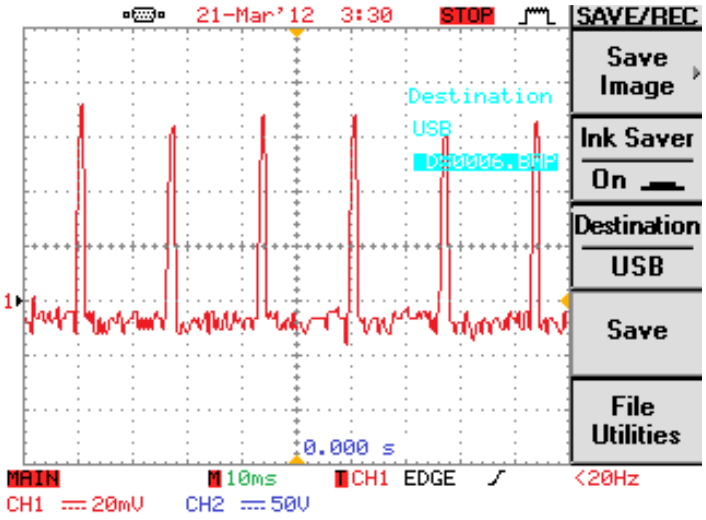

Figure 5.9 - Bridge Rectifier Input Steady State Current

With these measurements for the inrush and steady state currents, we calculated the inrush/steady-state current ratio (K_I). The new ratio was comparable to the ratio of 24.08, calculated in section 5.2:

$$K_I = \frac{I_{PK}}{I_{SS}} = \frac{192.31A}{7.7A} = 24.98$$

Figure 5.10 - Aluminum bars welding marks

To show the effects of inrush currents, two aluminum rods were placed next to each other, completing the circuit of the control system. Once the system was energized, the current needed to charge the capacitor started to flow through the rods, heating up the rods due to their resistances. As a result of the inrush current, the rods were welded together and required a small force to be separate from each other. The welding marks are shown in Figure 5.10.

5.4.2. Time-Delayed Switching with Pre-Charging Module

Once the pre-charging module was added to the bridge-rectifier system, the behavior was significantly different. The voltage across the load capacitor was raised slowly over approximately two seconds, as shown in Figure 5.11:

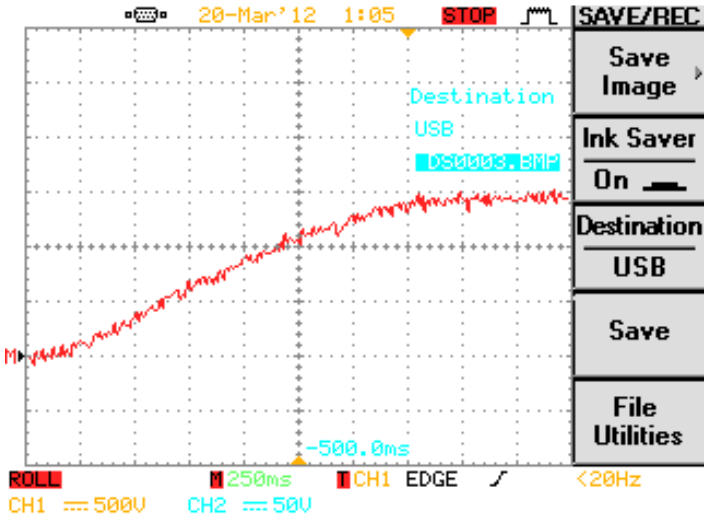

Figure 5.11 - Bridge Rectifier Load Voltage (with Pre-Charging Circuit)

This behavior was accomplished by the pre-charging module that accurately controlled the pulses that were used to slowly charge the load capacitor. Since the current used to charge up a capacitor depends on the rate of change of the voltage, the pulses prevented this rate of change from being too large, thus keeping the current pulses at relatively low amperage, as shown in Figure 5.12:

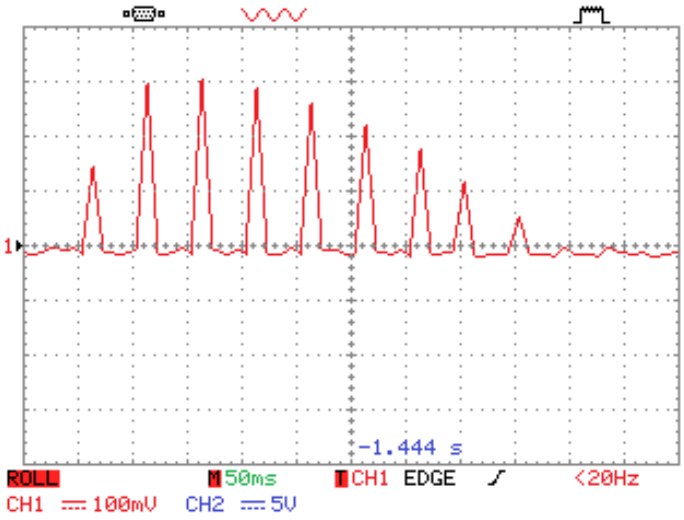

Figure 5.12 - Bridge Rectifier Input Current (with Pre-Charging Circuit)

Using (5.4), the peak current calculations are as follows:

$$I = \frac{0.3V}{0.182\Omega} * \frac{100}{5} = 32.97A$$

keeping a steady state current of 7.7A, bringing the inrush/steady-state current ratio (K_I) from 24.98 down to 4.28.

6. Conclusions and Recommendations

The inrush current mitigation method described in this project consisted of a module that charges the capacitive load of a full-wave bridge rectifier. The virtual simulations and physical experimentations of the system provided a better insight on the complexity and imperfections of such applications.

Even though the existent methods available today reduce transient currents, they all have disadvantages, such as power losses, synchronization issues and phase-lags. Our design approach effectively mitigates the inrush current while adding a time delay, which for most applications can be negligible.

The simulation tool provided enough data to support the success of our approach. After the simulations, this approach was implemented on a full-wave bridge rectifier with capacitive load. These results verified the effectiveness of the pre-charge module over the previous methods. The inrush to steady-state current ratio was reduced from 24.98 down to 4.28.

The creative approach of soft-charging the capacitive load has the advantage of being more efficient regarding power losses, but it can be modified to properly function at different frequencies.

Lastly, one recommendation for engineers using this method in the future is substituting the TRIACs that conduct once the capacitor is charged, and replace them with contact switches, in order to reduce the voltage drop across the thyristors.

7. Appendix

7.1.PSpice Codes

7.1.1. Single-Phase Bridge Rectifier

```
Single Phase Rectifier

* Voltage source and Series impedance
V  1  0  SIN(0 169.71 60)
R1 1  2  1.2144
L1 2  4  8.139m IC=0A

* Bridge Rectifiers
X_D1  5  4  DISNUB
X_D2  5  0  DISNUB
X_D3  4  6  DISNUB
X_D4  0  6  DISNUB

* Load Impedance
C2    5  6  10000u IC=0V
R2    5  6  250

* Diode with Snubber Filter
.SUBCKT DISNUB a  b
      D     b  a  DIX
      .MODEL DIX  D(BV=1000 RS=1u N=0.0001)
      Rd    c  b  50
      Cd    a  c  2u IC=0V
.ENDS

.PROBE
.TRAN 500m 500m 0 1u UIC
.END
```

7.1.2. Single-Phase Bridge Rectifier with Pre-Charging Circuit

```
Single Phase Rectifier

* Voltage source and Series impedance
V  1  0  SIN(0 169.71 60)
R1 1  2  1.2144
L1 2  3  8.139m IC=0A

* Phase-Delayed Switching
Xtr1  3  4  50  0  TRIAC
Vtr1  50 0  PULSE(0 5 2000.1m 1u 1u 9 10)
Rtr1  50 0  1

* Capacitor Pre-Charge
Xscr1 3  4  CLK 0  SCR

* Pre-Charging Signal
Vt    t  0  PULSE(0 10 16.6657m 8.332m 1u 1u 16.667m)
Rt    t  0  1
Vct   ct 0  PWL(0,10 0.1m,10 2000m,0 2000.01m,15 10,15)
Rct   ct 0  1
Xoa   t  ct CLK OP-AMP
Roa   CLK  0   100

* Bridge Rectifier
X_D1  5  4  DISNUB
X_D2  5  0  DISNUB
X_D3  4  6  DISNUB
X_D4  0  6  DISNUB

* Load Impedance
C2    5  6  10000u IC=0V
R2    5  6  250

* Triode for Alternating Current
.SUBCKT TRIAC AA  BB    CC    DD
   SW AA    25000 55000 0     SWITCH
   .MODEL SWITCH  VSWITCH(RON=1m ROFF=1MEG VON=1 VOFF=0)
   VS 25000 BB    0
   RS AA    45000 1000
   CS 45000 BB    33n   IC=0V
   RG CC    DD    1MEG
   EG 65000 DD    TABLE {V(CC)+(I(VS)*I(VS))}=(0,0) (0.1,1) (1,1)
   CE 55000 DD    1u    IC=0V
   RE 55000 65000 1
.ENDS
```

```
* Silicon Controlled Rectifier
.SUBCKT SCR AA    BB    CC    DD
   SW AA    25000 55000 0     SWITCH
   .MODEL SWITCH  VSWITCH(RON=1m ROFF=1MEG VON=1 VOFF=0)
   VS 25000 BB    0
   RS AA    45000 1000
   CS 45000 BB    33n   IC=0V
   RG CC    DD    1MEG
   EG 65000 DD    TABLE {V(CC)+I(VS)}=(0,0) (0.1,1) (1,1)
   CE 55000 DD    1u    IC=0V
   RE 55000 65000 1
.ENDS

* Diode with Snubber Filter
.SUBCKT DISNUB a  b
   D     b  a  DIX
   .MODEL DIX  D(BV=1000 RS=1u N=0.0001)
   Rd    c  b  50
   Cd    a  c  2u IC=0V
.ENDS

* Op-Amp
.SUBCKT OP-AMP P N O
   RI P N 3MEG
   EG 1 0 TABLE {V(P)-V(N)}=(-1,0) (-0.01,0) (0.01,10) (1,10)
   RO 1 O 100
.ENDS

.OPTIONS RELTOL=0.01 ITL4=100 ABSTOL=1N VNTOL=1M
.PROBE
.TRAN 3 3 0 2u UIC
.END
```

7.1.3. Three-Phase Bridge Rectifier

```
3-Phase Rectifier (Star Connection)

* Input Voltage
V1 11 0  SIN(0 169.71 60 0 0 0)
V2 21 0  SIN(0 169.71 60 0 0 120)
V3 31 0  SIN(0 169.71 60 0 0 240)

* Series Input Impedance
R1 11 12 1.2144
R2 21 22 1.2144
R3 31 32 1.2144
L1 12 13 8.139m   IC=0A
L2 22 23 8.139m   IC=0A
L3 32 33 8.139m   IC=0A

* Bridge Rectifiers
X_D1  O  13 DISNUB
X_D2  O  23 DISNUB
X_D3  O  33 DISNUB
X_D4  13 P  DISNUB
X_D5  23 P  DISNUB
X_D6  33 P  DISNUB

* Load Impedance
Cl    O  P  10000u IC=0V
Rl    O  P  250

* Diode with Snubber Filter
.SUBCKT DISNUB a  b
      D     b  a  DIX
      .MODEL DIX  D(BV=1000 RS=1u N=0.0001)
      Rd    c  b  20
      Cd    a  c  10u IC=0V
.ENDS

.PROBE
.TRAN 500m 500m 0 1u UIC
.END
```

7.1.4. Three-Phase Bridge Rectifier with Pre-Charging Circuit

```
3-Phase Rectifier (Star Connection)

* Input Voltage
V1 11 0  SIN(0 169.71 60 0 0 0)
V2 21 0  SIN(0 169.71 60 0 0 120)
V3 31 0  SIN(0 169.71 60 0 0 240)

* Series Input Impedance
R1 11 12 1.2144
R2 21 22 1.2144
R3 31 32 1.2144
L1 12 13 8.139m   IC=0A
L2 22 23 8.139m   IC=0A
L3 32 33 8.139m   IC=0A

* Phase-Delayed Switching
Xtr1  13 14 51 0  TRIAC
Xtr2  23 24 52 0  TRIAC
Xtr3  33 34 53 0  TRIAC
Vtr1  51 0  PULSE(0 5 14025m 1u 1u 9 10)
Vtr2  52 0  PULSE(0 5 14025m 1u 1u 9 10)
Vtr3  53 0  5
Rtr1  51 0  1
Rtr2  52 0  1
Rtr3  53 0  1

* Capacitor Pre-Charge
Xscr1 13 14 CLK 0  SCR

* Clock Signal
Vt t 0 PULSE(0 10 15.303m 8.332m 1u 1u 16.6667m)
Rt t 0 1
Vct ct 0 PWL(0,10 23.636m,10 15023.636m,0 15024m,15 20,15)
Rct ct 0 1
Xoa t ct CLK OP-AMP
Roa CLK 0 100

* Bridge Rectifiers
X_D1  O  14 DISNUB
X_D2  O  24 DISNUB
X_D3  O  34 DISNUB
X_D4  14 P  DISNUB
X_D5  24 P  DISNUB
X_D6  34 P  DISNUB

* Load Impedance
Cl    O  P  10000u IC=0V
Rl    O  P  250
```

```
* Triode for Alternating Current
.SUBCKT TRIAC AA  BB    CC    DD
   SW AA    25000 55000 0     SWITCH
   .MODEL SWITCH  VSWITCH(RON=1m ROFF=1MEG VON=1 VOFF=0)
   VS 25000 BB    0
   RS AA    45000 1000
   CS 45000 BB    33n   IC=0V
   RG CC    DD    1MEG
   EG 65000 DD    TABLE {V(CC)+(I(VS)*I(VS))}=(0,0) (0.1,1) (1,1)
   CE 55000 DD    1u    IC=0V
   RE 55000 65000 1
.ENDS

* Silicon Controlled Rectifier
.SUBCKT SCR AA    BB    CC    DD
   SW AA    25000 55000 0     SWITCH
   .MODEL SWITCH  VSWITCH(RON=1m ROFF=1MEG VON=1 VOFF=0)
   VS 25000 BB    0
   RS AA    45000 1000
   CS 45000 BB    33n   IC=0V
   RG CC    DD    1MEG
   EG 65000 DD    TABLE {V(CC)+I(VS)}=(0,0) (0.1,1) (1,1)
   CE 55000 DD    1u    IC=0V
   RE 55000 65000 1
.ENDS

* Diode with Snubber Filter
.SUBCKT DISNUB a  b
      D     b  a  DIX
      .MODEL DIX  D(BV=1000 RS=1u N=0.0001)
      Rd    c  b  50
      Cd    a  c  2u IC=0V
.ENDS

* Op-Amp
.SUBCKT OP-AMP P N O
   RI P N 3MEG
   EG 1 0 TABLE {V(P)-V(N)}=(-1,0) (-0.01,0) (0.01,10) (1,10)
   RO 1 O 100
.ENDS

.OPTIONS RELTOL=0.01 ITL4=100 ABSTOL=1N VNTOL=1M
.PROBE
.TRAN 20 20 0 0.01 UIC
.END
```

7.2.Microcontroller Code

```
#include <msp430g2231.h>

unsigned int timerCount = 0;
int trig, timerOff;
int pt1pn7, slow_charge;
int prev_st = 0;

void main(void)
{

	WDTCTL = WDTPW + WDTHOLD;		// Stop watchdog timer

	P1SEL &= ~(BIT0 + BIT4 + BIT5 + BIT6 + BIT7); // Select pins as digital I/O
	P1DIR &= ~(BIT7);                             // Set P1.7 as digital Input
	P1DIR |= (BIT0 + BIT4 + BIT5 + BIT6);         // Set P1.0, P1.4, P1.5 and P1.6
                                                      // as digital Output
	P1OUT &= ~(BIT0 + BIT4 + BIT5 + BIT6);        // Turn P1.0, P1.4, P1.5
                                                      // and P1.6 OFF
	trig = 82;                        // Initial value to trigger the pre-charge
	timerOff = 1;                     // Timer is OFF
	slow_charge = 0;                  // Reset 'slow_charge' counter

	__enable_interrupt();

	while(1)
	{
		pt1pn7 = P1IN & BIT7;     // Set to 128 if P1.7 receives a signal
		if(prev_st != pt1pn7)     // Detect if the input had changed
		{                         // from 0 to 1, instead of staying at 1
			if((pt1pn7 != 0) && (timerOff))  // If the timer is OFF and if
		{                                        // P1.7 receives a signal
				TACTL = TASSEL_2 + ID_0 + MC_1;  // Set the timer A to
                                                                 // SMCLCK, Up-mode
				TACCTL0 = CCIE;     // Enable timer interrupt
				TACCR0 = 105;       // Set the max_count to have
                                                    // precision of 0.1ms
				timerOff = 0;       // Timer is ON
			}
		}
		prev_st = pt1pn7;         // Set the prev_st to the previous state
	}
}
```

```
// Timer A0 interrupt service routine
#pragma vector=TIMERA0_VECTOR
__interrupt void Timer_A (void)
{
      timerCount++;                                    // Start counting every 0.1ms
      if((timerCount >= trig) && (trig > 17))          // if the time is greater than
      {                                                // or equal to the triggering
                                                       // phase (and) if the triggering
                                                       // phase is more than 36 degrees
            P1OUT |= (BIT0 + BIT4);              // Trigger the pre-charge switch
            if(timerCount == 83)                 // If the sine wave turns negative
            {
                  P1OUT &= ~(BIT0 + BIT4);       // Open the pre-charge circuit
                  TACTL = MC_0;                  // Turn the counter off
                  timerOff = 1;                  // Timer is OFF
                  if(slow_charge == 3)
                  {
                        trig = trig - 1;         // Reduce triggering phase
                        slow_charge = 0;         // Reset 'slow_charge' counter
                  }
                  slow_charge++;                 // Increment 'slow_charge' counter
                  timerCount = 0;                // Reset the timerCount
            }
      }
      else if(trig == 17)       // If the pre-charge reached maximum input voltage
      {
            P1OUT |= (BIT5 + BIT6);    // trigger the rectifier main switch (P1.5)
            TACTL = MC_0;              // Turn the counter off
            timerOff = 1;              // Timer is OFF
      }
}
```

7.3.MSP430 Documentation

Absolute Maximum Ratings(1)

Voltage applied at V_{CC} to V_{SS}		–0.3 V to 4.1 V
Voltage applied to any pin(2)		–0.3 V to V_{CC} + 0.3 V
Diode current at any device pin		±2 mA
Storage temperature range, T_{stg} (3)	Unprogrammed device	–55°C to 150°C
	Programmed device	–55°C to 150°C

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program execution	1.8		3.6	V
		During flash programming	2.2		3.6	
V_{SS}	Supply voltage			0		V
T_A	Operating free-air temperature	I version	–40		85	°C
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(1)(2)	V_{CC} = 1.8 V, Duty cycle = 50% ± 10%	dc		6	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ± 10%	dc		12	
		V_{CC} = 3.3 V, Duty cycle = 50% ± 10%	dc		16	

(Courtesy of Texas Instruments) [10]

8. References

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[10] Texas Instruments, **"Mixed Signal Microcontroller"**. *MSP430G2231 datasheet*, Feb. 2010 [Revised Dec.2011].