Class D Audio Amplifier

The design of a live audio Class D audio amplifier with greater than 90% efficiency and less than 1% distortion.

A Major Qualifying Project

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Abstract

The purpose of this project was to design and produce a 90% efficient, 80W Class D audio amplifier, with less than 1% Total Harmonic Distortion (THD) for the NECAMSID Lab. The amplifier consisted of a second order, three-level $\Delta\Sigma$ modulator, an H-bridge power stage, and a second order, passive Butterworth filter. Testing confirmed that the efficiency, THD, and power specifications were met in the final revision of the design.

ACKNOWLEDGEMENTS

We would like to thank Professor McNeill and Professor Klein for advising this project. We would also like to thank the NECAMSID lab for sponsoring this project.

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Executive Summary

The purpose of this project was to design and implement a Class D audio amplifier. Class D amplifiers improve upon the traditional amplifier design by amplifying a digital signal instead of an analog signal for drastically superior efficiency. These amplifiers, because of their efficiency specifications, are often used in portable applications where small size and low power consumption are important for portability and battery use. This report discusses the design of a Class D audio amplifier that, at 80 Watts, is powerful enough to facilitate a small concert while maintaining 90% efficiency for lower energy usage and costs. With the growing concern regarding the human impact on the environment and increasing energy costs, it is becoming necessary to design higher power devices more efficiently to reduce environmental repercussions and improve marketability. The efficiency also removes the need for heat sinks, which often contribute significantly to the weight of a system, as little power is dissipated in the amplifier. This increases the portability of the sound system for touring artists or others who wish to transport audio equipment. While sound quality is often compromised in Class D audio amplifiers, this system was designed with less than 1% Total Harmonic Distortion (THD) and with a Signal to Noise Ratio (SNR) of greater than 90dB to provide quality comparable to Compact Disc (CD) recordings. This project was advised by Professors John McNeill and Andrew Klein and was possible largely as a result of the generous sponsorship provided by the NECAMSID Lab.

Class D audio amplifiers achieve impressive efficiency specifications using a technique that, until recently, was impractical due to component constraints that limited sound quality. The amplifier functions using a modulator to convert the analog input to a digital signal. This modulation could be accomplished in a number of ways, provided that the audio signal could be reconstructed from its digital representation with a filter. Common techniques include Pulse-Width Modulation (PWM), Delta-Sigma ($\Delta\Sigma$) modulation or the implementation of

a Digital Signal Processing (DSP) chip. This modulation stage was restrictive until recently when advancements in Integrated Circuit (IC) design, combined with the use of feedback, were able to provide a low-noise solution that was practical for audio applications. Once the modulation stage produces a digital signal, transistors can increase the power in the digital signal while acting in only the saturation and cutoff regions, thus avoiding the losses introduced in the linear region. The remarkable efficiency of the Class D amplifier is a result of this mode of operation. Traditional amplifiers, in contrast, use transistors to directly amplify audio signals, and are therefore forced to operate in the linear region where the most losses are incurred. The high-powered digital signal produced by the transistors in a Class D amplifier is finally applied to a filter. This reconstructs an amplified version of the original audio signal, removing the noise introduced by the modulator to the frequency spectrum above the audio band. The filtered signal is then applied to a load, usually a speaker or a recording device in the case of audio amplifiers.

Extensive research showed that the optimal design for this product would utilize $\Delta\Sigma$ modulation and an H-Bridge power stage connected to a passive Butterworth filter. Once these system-level decisions were made, the details of each stage were considered. To maximize efficiency and quality, the modulator became a three-state, second order modulator. The three-state operation minimized switching when the input signal approached zero to improve efficiency and audio quality, and the second order configuration provided better noise shaping which also improved the quality of the output signal. In the power stage, Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) and MOSFET driver choices became the most important design decisions. After careful analysis of different MOSFETs, the IRF6645 emerged as the best choice because of its low R_{DS-on} and C_{GS} values. The driver chosen was designed specifically to work with the IRF6645. With the filter design, components were, again, the most important factors. The Coilcraft D1787 inductors and polyfilm capacitors were instrumental in reducing microphonics and unwanted losses in the filter.

This project went through two major design revisions. The first implementation included

a bread-boarded, first order, modulator and a PCB that contained the power stage and the filter. This was mainly to ensure the functionality of the design and to find issues with system implementation. Once the known errors in the initial implementation were rectified, a final, smaller PCB was created that included space for the modulator as well as the power stage and filter. Though the modulator on the PCB did not work due to errors in the layout, a new second order, three state modulator was realized on a breadboard that worked with the smaller, improved power stage and filter.

The final design was tested extensively to verify that it met the original specifications. The product was successful in producing output power greater than 80 Watts with an 8Ω load. The amplifier efficiency was greater than 95% at full output power, the SNR of the system was above 90dB and the THD was below 1%, as expected.

This design was successful in achieving the goals established at the onset of the project. All specifications were met and the members of the team learned a great deal throughout the design process. Taking an idea throughout all the stages of production, including background research, design, implementation, functionality testing, revision and specification verification, was an extremely rewarding process. Class D is essential to the future of audio amplification and environmental sustainability, and this project has demonstrated that the technology can be applied to higher power systems without diminishing efficiency or audio quality.

Chapter 1

Introduction

Class D amplification is achieved by modulating a signal, amplifying the modulated signal and then filtering the amplified signal back into its original form. Since Class D amplifiers work with digital signals, they do not require that the transistors involved operate in the triode region and, as a result, they are much more efficient than other amplifiers. This method has been used in portable audio devices, cell phones and low fidelity audio where size, power and heat dissipation are of great concern. The advantages of Class D, however, can also be applied to the larger systems required for live audio.

The purpose of this project was to produce a live audio Class D amplifier. The reduction in power consumption made possible by a Class D system is sometimes considered unnecessary for live audio because the size and efficiency of an audio system is not usually a concern when the system is permanently installed in a venue and the power is drawn from the wall. There are traveling musicians, however, who require a more compact system that can be easily moved from one venue to another. With a more efficient system comes smaller heat sinks and thus smaller systems that can be portable even if they must be plugged into the wall. Furthermore, with environmentalism becoming more and more important, especially among those in the music industry, the advent of audio systems that require less power than current systems is very attractive. Finally, venues themselves may wish to purchase these

systems simply to save energy, which is becoming increasingly expensive. These savings may be significant for venues that have shows every night.

1.1 Project Objectives

This project produced a prototype for a live Class D audio amplifier. The specifications in Table 1.1 show the specifications that were outlined for this project.

Specification	*Value*
Output Power (RMS)	80W
Efficiency	¿90%
Total Harmonic Distortion (THD)	¡1%
Signal to Noise Ratio (SNR)	¿90dB
Frequency Response	3dB from 20Hz to 20kHz

Table 1.1: Project Specifications

1.2 Report Organization

This report follows the progress made throughout this project. In Chapter 2, background research is presented to prepare the reader for the remainder of the report. Chapter 3 deals with the preliminary design that led to the first revision of the prototype. The results of the testing done on this revision are given in Chapter 4. Chapter 5 explains the changes made to advance the prototype to the final revision. Chapter 6 gives the results from the testing of the final revision as well as a discussion of how well the product met the specifications outlined in Section 1.1. Finally, Chapter 7 presents the conclusions reached over the course of the project and Chapter 8 makes recommendations for future projects in Class D audio amplification.

Chapter 2

Background

This chapter discusses the Class D audio amplifier and each of its principal components. It presents two different possibilities for the modulation stage: Pulse Width Modulation and Delta Sigma Modulation. It also examines the power stage and explores half- and full-bridge amplifiers. Filtering is also discussed in this chapter and different types of noise are investigated.

2.1 Class D Amplification

The Class D amplifier is one of many classes of amplifier. Some other amplifier designs, like Class A, Class B, and Class AB, are widely used because of their simplicity and ease of use in almost any application. Class D amplifiers have historically only been used in a limited number of applications, like motor control, because it is more difficult to generate the high quality signals required for audio applications with a Class D amplifier. Recently, however, Class D technology has advanced sufficiently to allow these amplifiers to accurately and cleanly amplify audio signals. There are many advantages to using Class D amplifiers for audio applications, and the number of disadvantages is shrinking every year with further advances in technology.

2.1.1 Operation of Class D Audio Amplifiers

To understand how a Class D amplifier works, it is important to present the basics for amplification with a discussion of the Class A amplifier. A Class A amplifier usually uses a Bipolar Junction Transistor (BJT) to directly amplify an input audio signal. This is a simple process, involving the input signal, the amplifying BJT, power rails, and the output, configured as shown in Figure 2.1.

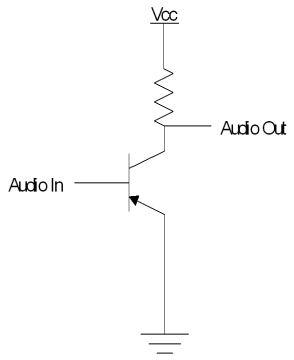

Figure 2.1: A Class A audio amplifier.

The BJT amplifies the signal by operating in the linear region. This allows the output voltage to vary based upon the principle that the current flowing between the collector and the emitter of the transistor is proportional to that flowing between the base and the emitter. As a result, the high power output signal follows the input signal very accurately, reducing noise and distortion. The linear region of the transistor, however, is very inefficient. It constantly drains energy from the power supply, even if the input is grounded and there is no signal to amplify. The maximum theoretical power efficiency of a Class A amplifier is between 25% and 50%, depending upon the type of output coupling used. This becomes a problem when an amplifier is used in an audio application because audio is an AC signal and most of the time the input will be closer to zero volts than it will to one of the rails [Qui93]. For many audio applications, such as home theater or live concert audio, the power efficiency was not considered until very recently, as there was an "unlimited" amount of power available when the device was not dependant on a portable energy source. With recent trends towards

environmentalism, increased energy costs, and higher powered amplifiers, power efficiency is quickly becoming paramount to the design of audio amplifiers. There are modifications to Class A, Class B and Class AB amplifiers that increase power efficiency at the expense of increased distortion, but the maximum theoretical power efficiency is still lower than desired specifications for this project at 78.5%.

Once the power efficiency specification becomes a top priority, Class D amplifiers become a more appealing choice. A Class D amplifier is theoretically 100% efficient and can reach greater than 95% efficiency in practice with current technology [IRF07]. Class D amplifiers are much more complicated than the other designs that were described, which was a significant factor in the preference for other amplifiers until more recent years. Their complexity can lead to a highly noisy output signal, which made them useless for many applications. With recent advances in technology, however, the noise can be reduced and then filtered out, leaving a highly efficient, but still accurate, audio amplifier.

A Class D amplifier has three main stages, the first of which is the modulation stage. In a Class D amplifier, the signal must be converted to a digital signal before being amplified. There are several ways to accomplish this; the two most widely used are Pulse Width Modulation and Delta-Sigma ($\Delta\Sigma$) Modulation. Each method has advantages and disadvantages which will be discussed in a later section. After the signal is modulated, it must be amplified. The amplification stage in a Class D amplifier uses several Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), a different kind of transistor with very low power loses. The MOSFETs in a Class D amplifier can switch between fully on and fully off because they are amplifying a digital signal, avoiding the triode region where power efficiencies drop. When completely on in the active region, or completely off in the cutoff region, MOSFETs are theoretically lossless and in practice have very low power losses. After the modulated signal is amplified, it must be filtered before it can be sent to a speaker. The last stage is the filtering, or demodulation, stage, which consists of a low pass filter. This allows everything in the audible range (20 Hz - 20 KHz) to pass through, but significantly

attenuates everything above 20 KHz. After being filtered, the signal is an amplified replica of the original input signal, and can be applied directly to a speaker. Figure 2.2 shows how these blocks fit together.

Figure 2.2: Block Diagram of a Class D Amplifier

2.1.2 Advantages and Disadvantages of Class D

Class D amplifiers have several advantages over Class A, AB, and B amplifiers. The biggest advantage is the increased power efficiency. A Class D amplifier can reach theoretical power efficiencies of 100%, and over 95% in actual applications. This is a significant improvement over the Class B amplifier, which has a maximum efficiency of 78.5%. In high power applications even a small difference in efficiency is considerable because it allows for a large reduction in the amount of waste heat generated by the amplifier. Another benefit to Class D amplifiers is that for lower power applications, they can be fit entirely on an integrated circuit. For higher power applications a heat sink may be required, but the size of the heat sink would be much smaller than on a Class A, AB, or B amplifier of comparable power output. The reduced size of the amplifier leads to lower costs associated with enclosures for the amplifier. In addition, while the amplifier design itself is more complicated, many of the internal components, such as the MOSFETs, integrated circuits, and capacitors, are extremely cheap when purchased in bulk.

While Class D amplifiers have been in use for many years, only recently have they come to the forefront of audio amplification. This is because Class D amplifiers have a number of disadvantages that make them less suitable for audio amplification, though many of these have been overcome with recent advances in technology.

One major disadvantage is that a Class D amplifier has a very high amount of high

frequency noise, generated by the switching design [Qui93]. This noise must be kept at a high enough frequency to be inaudible, yet to a minimum amplitude to meet FCC regulations. To help reduce extraneous noise, a filter is added after the amplifying stage. This filter is an additional component of the Class D amplifier, and adds complexity, weight, and cost. The added weight is negligible, however, when compared to the weight of the heat sink required for a Class A, Class AB or Class B amplifier. The additional cost of a filter may also be minimized using careful design techniques. Since the filter only needs to attenuate signals above the audible frequencies, it is not essential that the filter be extremely precise. The filter may therefore be realized by a fairly simple, low-pass, passive filter.

A second deficiency of Class D amplifiers is the increased complexity in design. This may result in increased design time and expense. Increased design expenses are generally considered acceptable, however, if the result is a lower manufacturing cost because design is singular expense, whereas manufacturing expenses are recurring. After the amplifier is designed, most of the components, with the possible exception of any inductors used in the filter and specialized MOSFETs in the power stage, are extremely inexpensive when purchased in bulk. So while the increased complexity seems like a major disadvantage, it may become irrelevant when the amplifiers are mass-produced.

The last major disadvantage of Class D amplifiers is that historically, distortion has been a major problem. High Total Harmonic Distortion (THD) is indicative of high noise levels, which detract significantly from the audio quality of the output. Advances in technology have allowed for faster modulation techniques, however, which can reduce THD to fractions of a percentage in Class D audio amplifiers.

2.1.3 Applying Class D to Audio Design

High power efficiency, combined with a compact and lightweight design, distinguishes Class D amplifiers from other amplification techniques. Power efficiency is becoming very important, as concerns regarding power usage increase. A tangible benefit of reduced power consumption

is that it becomes less expensive to use the amplifier. While this may not be a major concern for homeowners, in the live audio market power is sometimes generated on site, especially for large concerts, and larger generators are more expensive to use. From a marketing standpoint, the compact and lightweight design made possible by high efficiency is attractive to all users. Home audio systems can be designed to be hidden away, helping to reduce clutter in a room. In the touring market, smaller amplifiers mean lower shipping costs and a reduction in labor when setting up before and packing up after a concert.

2.2 The Modulation Stage

The modulation stage of an analog Class D audio amplifier is primarily influential within the system in that it drastically affects the quality of the output. The modulation stage is the first stage in the amplifier, other than the input channel over which the system has little control. Any information in the original signal that is lost during modulation, either by attenuation or the introduction of excessive noise, will create distortion in the final analog output and will decrease the maximum sound quality that is possible at the output.

There are a wide variety of modulation techniques which may be considered for use in a Class D audio amplifier. Some, however, are more reasonable than others for reasons of simplicity, effectiveness, and availability for commercial use. Simplicity must be considered because a simpler design will have fewer components and be lighter and more portable, thereby increasing its appeal in the live audio market. Effectiveness must also be considered because modulation is essential to sound quality and the amplifier must achieve less than 1% distortion and greater than 90dB Signal to Noise Ratio (SNR). The modulation technique is also limited by availability for commercial use, as it would be impractical to implement a proprietary modulation scheme or a technique with similar limitations, in the development of an independent product. With these limitations, the most feasible options are Pulse Width Modulation (PWM) and Delta Sigma Modulation ($\Delta\Sigma$) [Dal97].

2.2.1 Pulse Width Modulation (PWM)

Pulse Width Modulation is a technique that represents the amplitude of the input signal using the duty cycle of the output signal, which is usually bi- or tri-state. While there are many ways to achieve this, one of the simplest is to compare the analog input signal to a ramp signal or a triangle wave of a frequency that is at least twice that of the analog input, in accordance with the Nyquist-Shannon sampling theorem. The resulting output will consist of a digital signal that contains a logic high whenever the analog signal is higher than the triangle wave, and a logic low when it is not. This creates a signal with a duty cycle that represents the instantaneous voltage of the analog input signal [Ber03].

While very simple, available for commercial use, and even somewhat effective, PWM systems are, in some ways, restrictive. PWM is commonly demodulated using a low pass filter. The noise spectrum, while having a higher SNR than other types of modulation contains a large amount of high amplitude noise contained in a series of very narrow frequency bands. This makes the noise more difficult to remove with filters than if the noise were of equal or even higher energy, but were spread evenly over a larger number of frequencies. Systems that contain PWM are also limited in how they can be modified if theory and practice should differ in the physical implementation of the system. The frequency or amplitude of the triangle wave may be modified, but without adding feedback to the system, it is very difficult to modify the response of the modulator. Adding feedback provides the system with greater flexibility regarding any modifications that may be required; however, it also distributes a greater number of the frequency bands containing high amplitude noise in lower frequencies, closer to those contained in the analog input signal. This increases the complexity of the necessary demodulation filters. If a simple system were required and sound quality were not a priority, pulse width modulation would be a highly effective choice. A slightly more complex modulation technique may, however, provide a significant increase in sound quality and reduce the minimum distortion to below 1% without incredibly complicated filters, making it a more optimal choice for this particular system [Max06].

2.2.2 Delta Sigma Modulation ($\Delta\Sigma$)

$\Delta\Sigma$ is another modulation technique that may be realized with a circuit that requires only an integrator and a D-latch. In this implementation, the input audio signal serves as the input to a simple integrator circuit. When this signal surpasses a threshold, it resets the integrator and triggers the D-latch, so that it outputs a pulse of a set width. This provides a series of set-width pulses with variable spacing between them, whose time-density distribution represents the instantaneous amplitude of the original input signal.

$\Delta\Sigma$ separates itself from PWM by its inherent use of feedback to create a system with superior noise performance. A system model of a $\Delta\Sigma$ modulator, showing this feedback, is displayed in Figure 2.3.

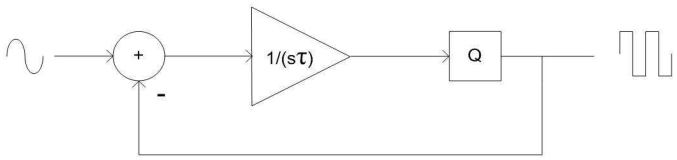

Figure 2.3: A system model of a first order $\Delta\Sigma$ Modulator.

The quantizer in this figure poses a problem, however, when attempts are made to model or simulate this modulator because it is a non-linear component. It is therefore replaced with additive quantization noise, as shown in Figure 2.4.

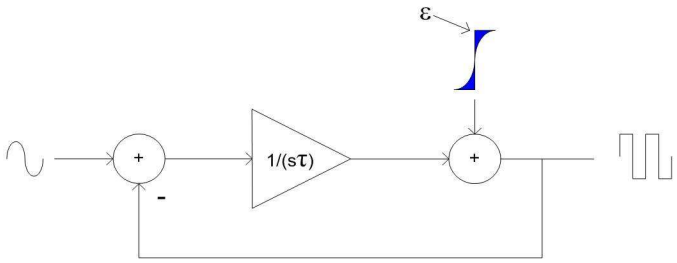

Figure 2.4: A system model of a first order $\Delta\Sigma$ Modulator after the quantizer is replaced with additive quantization noise for modelling and simulation.

Analysis of this system provides Equation 2.1.

$$V_{OUT} = (V_{IN} - V_{OUT})\frac{1}{s\tau} + \epsilon \tag{2.1}$$

Solving for V_{OUT} produces Equation 2.2.

$$V_{OUT} = [\frac{1}{1 + s\tau}]V_{IN} + [\frac{s\tau}{1 + s\tau}]\epsilon \tag{2.2}$$

This equation contains a signal transfer function and a noise transfer function for the modulator. These transfer functions produce a graph of the shape shown in Figure 2.5 with the signal transfer function shown in red and the noise transfer function shown in blue.

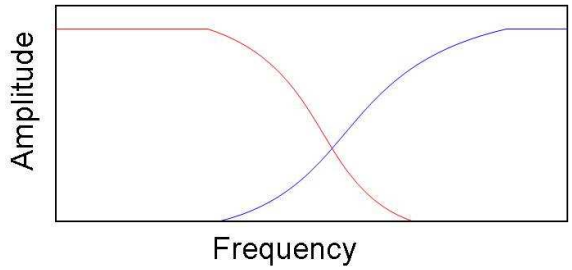

Figure 2.5: An approximate representation of the signal (red) and noise (blue) transfer functions of a simple delta sigma modulator.

In an audio application, it would be ideal for the signal transfer function to be as flat as possible throughout the audio band and for the noise transfer function to push the noise as far out of the audio band as possible. The specifics of the transfer functions depend on the coefficient of integration for the integrator. The feedback may also be scaled to further affect the transfer function. The order of the modulator may also be increased by adding integrators and levels of feedback. This increases the slope of the transfer functions. In an audio application this noise shaping may improve sound quality by decreasing the amount of quantization noise in the audio band. The modulation frequency also affects the system by determining the placement of the transfer function in the frequency domain. A higher modulation frequency will push the noise up to higher frequencies, further reducing its presence in the audio band.

Like with the PWM system, the output of a $\Delta\Sigma$ modulator may be demodulated with a low pass filter. The $\Delta\Sigma$ system, however, has fewer bands with very high noise amplitudes and generally produces a smoother waveform due to noise shaping. The noise floor in the audio band is considerably lower than that of the PWM system. Also, when both are simulated with a modulation frequency that is two orders of magnitude above the highest signal frequency, the noise reaches a maximum point in PWM systems that is not reached in $\Delta\Sigma$ systems until a frequency that is two orders of magnitude higher than that in the PWM system. The $\Delta\Sigma$ system also responds extremely well to feedback, unlike PWM. This is an important quality because it allows the system to respond to any changes in load that it might experience, as well as allowing for an improved SNR. $\Delta\Sigma$ is therefore extremely effective, has a lower SNR than PWM in the audio band, as well as in other, lower frequency bands. It is also extremely simple to implement and is commercially available, making it a solution that is close to ideal [Dal97].

2.3 The Power Stage

After the signal passes through modulator, it must be amplified. There are a variety of methods that can be used to amplify a modulated signal. Most Class D systems use either a half-bridge configuration or an H-bridge (full-bridge) configuration. No matter what the configuration, the main components of the amplifier are MOSFETs that are powered by drivers designed for that purpose. This is why the Class D amplifier is so efficient. The transistors do not have to operate in the triode region because they are amplifying a digital signal.

2.3.1 Half-Bridge Amplifiers

One configuration of the power stage is the half-bridge amplifier. Figure 2.6 shows the schematic for a basic half-bridge amplifier. In this configuration, two MOSFETs are used

and either one or the other is turned on. Each of these MOSFETs exposes the load resistor to either a positive or negative rail. This design is very simple and requires very few components.

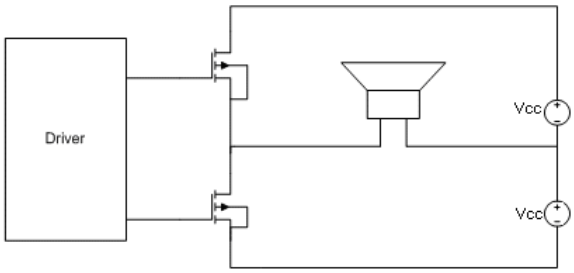

Figure 2.6: A Half-Bridge Amplifier

2.3.2 H-Bridge Amplifiers

Another common configuration is the H-bridge or full-bridge amplifier. Figure 2.7 shows the schematic of a full-bridge amplifier.

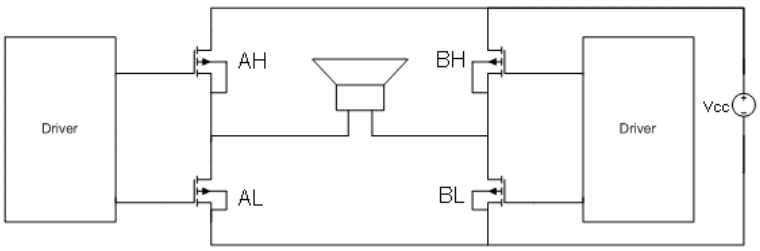

Figure 2.7: An H-Bridge Amplifier

A full bridge amplifier always has two of the four MOSFETs on at a time. This differs from the half-bridge amplifier, which has only two possible states, in that the full bridge can achieve three different states. The states are positive, negative and neutral. The amplifier gives the load a positive voltage when switches AH and BL are on at the same time, a negative voltage when BH and AL are on, and the load is grounded when AL and BL are on at the same time. When using an H-bridge it is extremely important to make sure that

AH and AL are never on at the same time and that BH and BL are never on at the same time because this would short the rails and damage both the amplifier and the speaker.

2.3.3 A Critical Evaluation of Half- and H-Bridge Amplifiers

There are advantages and disadvantages to each of the different amplifier designs. Table 2.1, taken from an International Rectifier application note [HA05], outlines the clear advantages and disadvantages of each with respect to Class D amplification. This table shows that the main problem with a full bridge is that there are more components. Additional MOSFETs and drivers are necessary. The advantages far outweigh the disadvantages, however. Two of the big advantages of the full-bridge are that even order harmonic distortion and DC offsets are canceled out, which is extremely important in audio systems. Harmonic distortion negatively affects the quality of the output and DC offsets can damage a speaker. Removing this harmful DC offset in a half-bridge amplifier would require using a more complicated power conditioning stage. This application note goes on to say that, "a full-bridge is better in audio performance ... a full-bridge topology allows of the use of a better ... modulation scheme, such as three-level PWM" [HA05], thus increasing the capability of the amplifier.

Half-Bridge vs. Full Bridge

	Half-Bridge	Full-Bridge
Supply Voltage	0.5 x 2ch.	1
Current Ratings	1	2
MOSFETs	2 MOSFETs/CH	4 MOSFETs/CH
Gate Driver	1 Gate Driver/CH	2 Gate Drivers/CH
Linearity	Even and Odd Order HD	No Even Order HD
DC Offset	Adjustment is needed	Can be canceled out
Modulation Pattern	2 level	3 level can be implemented

Table 2.1: A Comparison of Half-Bridge and Full-Bridge Amplifiers [HA05]

2.3.4 MOSFET Drivers

A MOSFET gate may be modeled as a small capacitor that must be charged for the MOSFET to turn on. The voltage across the gate must be at least 5 volts higher than the drain voltage for the MOSFET to turn on. For Class D audio amplifiers, the MOSFET between the high voltage rail and the load must be referenced to the high voltage rail. This is a problem because the modulator output will be at the low voltage levels used in logic circuits. To resolve this issue, a MOSFET driver must be used to convert the low voltage level to the higher voltage required, as well as to provide a higher current to more quickly change the voltage of the gate of the MOSFET. Additionally, using a driver will more easily allow for controlling the "dead time", or the small delay in turn on times. This helps to prevent shoot-through as well as to reduce total harmonic distortion.

2.4 Noise and the Filtering Stage

The output of the amplifying stage must be filtered before reaching the speaker because the signal is a modulated pulse wave, not an analog audio signal that can serve as an output to the speaker. The image shown in Figure 2.8 displays a 2kHz signal modulated at 10MHz using the MATLAB code found in Appendix A. This represents a typical output from a delta sigma modulator in the frequency domain, although depending upon the modulation frequency the noise response may be shifted up or down in frequency.

The 2kHz signal is evident, but there is a significant amount of noise surrounding it that needs to be filtered out. There are a number of ways to filter out the noise, and it can be categorized into several different types of noise. The following section of this document discusses noise and the different filters available to attenuate it.

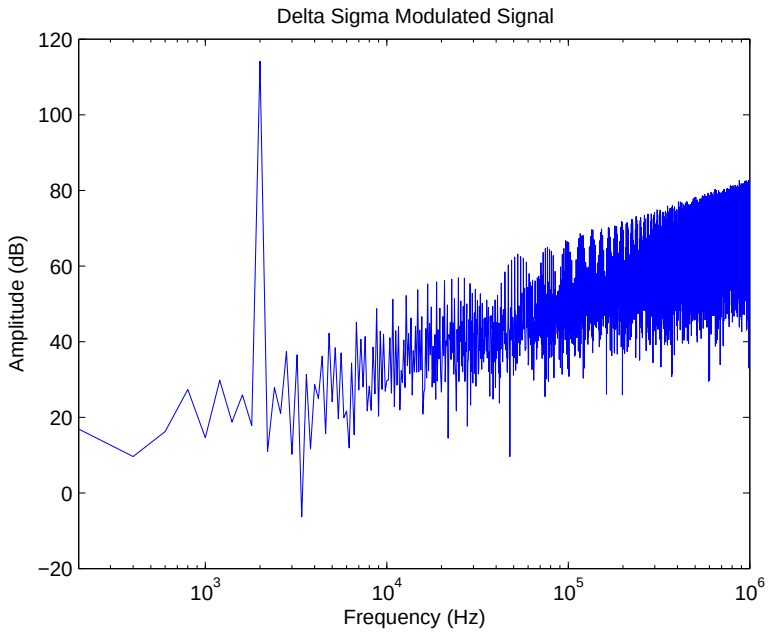

Figure 2.8: A 2kHz signal modulated at 10MHz with delta sigma modulation.

2.4.1 Types of Noise

One of the easiest ways to determine the quality of any amplifier is by evaluating the amount of noise present in the output. This is especially true for audio amplifiers that are noted for efficiency, as noise will waste power as well as degrading the quality of the signal and possibly damaging the speaker. Class D amplifiers are extremely susceptible to noise, as the modulation of the signal adds noise to the system. While it is easy to identify that the presence of excessive noise will degrade the audio quality of the system, there are actually several different types of noise, each with their own characteristics. To actively compete in the audio amplifier market, any new amplifier design must have impressive specifications regarding two different types of noise: general noise which is represented by the Signal to Noise Ratio (SNR) of the output, and harmonic noise, which is evaluated using the Spurious Free Dynamic Range (SFDR) standard. The latter is related to Total Harmonic Distortion (THD) which is a much more commonly understood specification. While the influence of SFDR on a system is not recognized by many marketing professionals and purchasers of

audio amplifiers, its relationship to the more common specification allows it to contribute to the marketability of an amplifier.

Signal to Noise Ratio (SNR)

A Signal to Noise Ratio is a parameter that describes the ratio of the signal power to the noise power in a system. In the application of audio amplifiers, the output SNR is measured on the output of the filtering stage and is considered to be the ratio of the final amplified signal power to the final amplified noise power. THD is excluded from this noise power measurement because it is specified separately. For audio signals, this ratio is represented in decibels (dB), and can be calculated using Formula 2.3.

$$\text{SNR} = 10 \log \frac{P_{signal}}{P_{noise}} \tag{2.3}$$

In general, the SNR measures the difference between the audio signal and the noise floor. The noise in the noise floor contains several different types of noise that can sum to create an audible "hiss" in high power applications. For the most part, it is impossible to eliminate this background nose entirely by conventional means, although it can be reduced significantly with careful design. One cause of noise is thermal excitation in the amplifier. While MOSFETs are generally very accurate, there can be random thermal excitation in the silicon, which may cause a small current to flow when none is desired. Similarly, if there is any sort of background noise in the input signal, it will be amplified and will contribute to the system noise floor, reducing the SNR. It is therefore important to have an SNR that is as high as possible, because a higher SNR allows for a higher quality output.

Spurious Free Dynamic Range (SFDR) and Total Harmonic Distortion (THD)

Spurious Free Dynamic Range (SFDR) is an important specification in amplifier design. It is usually used in reference to analog to digital converters (ADC) and digital to analog converters (DAC) but because $\Delta\Sigma$ modulation, an ADC technique, is implemented in the

modulation stage, SFDR may be considered. The SFDR refers to the ratio between the desired signal and the highest amplitude spurious, or unwanted, signal. The spurious signal does not need to be a harmonic of the fundamental signal, but in many cases it will be. If the spurious signal is a harmonic of the fundamental frequency, then it will be a portion of the Total Harmonic Distortion (THD). THD is a ratio of the fundamental frequency to the sum of the harmonics, though in practice anything more than the fifth harmonic usually will not contribute significantly to the THD.

Both SFDR and THD can be caused by several different problems in the system. One such example is clipping of the audio signal. The modulator is designed to support signals up to a certain amplitude. At that amplitude, the modulator outputs a signal that is a constant logic high. The filter will then be designed such that at that amplitude, the output signal will also have a known amplitude. For any input values higher than the system can support, the output signal will have the same known amplitude that it does when the input value is exactly as high as the system can support. The information that represents the exact amplitude will therefore be lost, and the system will only indicate that the amplitude is at or above a threshold. Fortunately, this is easy to avoid by carefully monitoring input levels to ensure that the input stays within the correct range. Another issue that may decrease SFDR and THD values is non-linearity in the amplifier. Class A amplifiers are known for their exceptional linearity, but they are also notoriously inefficient. Class AB amplifiers are a compromise, sacrificing some linearity for a higher power efficiency. Class D amplifiers are more complicated, however. Acceptable linearity can be achieved, but that linearity is dependent upon modulation technique and filter quality. Even if the amplifier is not perfectly linear, a filter may be able to help reduce spurious noise if it is above the audible band of frequencies.

2.4.2 Passive Filters vs. Active Filters

The first decision in filter design is determining whether to use a passive or active filter. Passive filters are made up of powerless or passive components like resistors, capacitors and inductors. An active filter contains one or more powered components, usually operational amplifiers. This allows for the addition of gain to the filter and allows the filter to be more accurate. Figures 2.9 and 2.10 show simple schematics of an active low-pass filter and a passive low-pass filter, respectively.

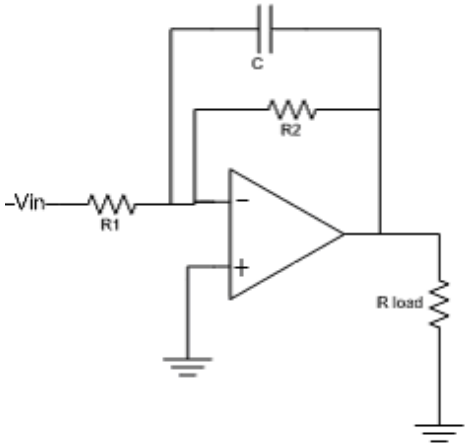

Figure 2.9: A basic active low pass filter.

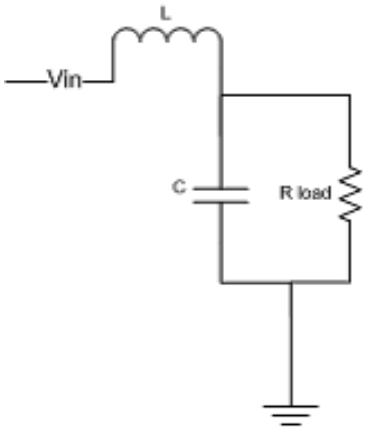

Figure 2.10: A basic passive low pass filter.

The components in each design that introduce complexities into the system are the op-amp in the active filter and the inductor in the passive filter. The difficulty with op-amps is that they require external power and are limited in what frequencies they can handle [Lac91]. Inductors, on the other hand, are difficult to tune accurately and are can be bigger and more expensive than op-amps [Lac91]. Active and passive filters also differ in that an active filter contains resistors and an op-amp which introduce losses, whereas a passive filter can be realized with just inductors and capacitors, which have very low losses associated with them. This is significant because of the efficiency specification for this project. Because of the nature of the noise that must be eliminated, as shown in Figure 2.8, the cutoff frequency has no need to be extremely accurate. Most of the noise that must be removed is outside the audio band, and as long as the filter attenuates most of the noise above the audio band and not the signal in the audio band, it will be effective. Therefore the benefits of a passive filter outweigh the disadvantages for Class D audio amplification.

2.4.3 Single Ended Filters vs. Balanced Filters

Choosing a passive or active filter is merely the first step in filter design. There are multiple configurations within either of those subsets. Once the configuration is chosen, the order of the filter and the values for each of the components required in the filter must be determined. The first filter consideration is whether to filter just on one side of the signal with a single-ended filter, or both sides, with a balanced filter. Figure 2.11 shows the difference in design of the two filters.

The only advantage to using the single ended design is that there are fewer components. For Class D, however, using a balanced filter is desirable because it eliminates the DC offset by centering the signal around zero without the use of a negative rail [TI:99].

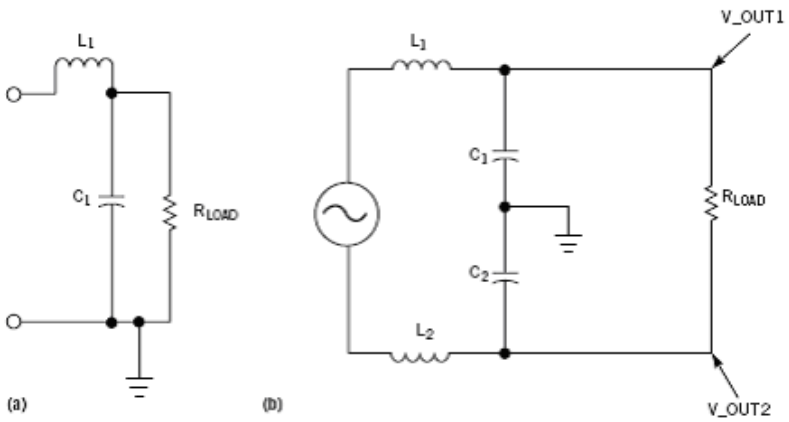

Figure 2.11: Single Ended and Balanced Filter [McD01]

Chapter 3

Preliminary Design

The following section outlines the design of the preliminary stage of the Class D audio amplifier. This iteration of the design included a bread-boarded first order modulator connected to a PCB that contained the power stage and the filter. It was known that this design was not likely to meet the specifications described in Section 1.1. It was, however, important to make an iteration of the amplifier early on to demonstrate that the design was functional and test for unforeseen problems that may not appear in simulation. The sections in this chapter describe how each stage was created, discussing layout and component decisions as well as the initial PCB and breadboard construction.

3.1 The Modulation Stage

The first step in designing the modulation stage of the system was to determine what modulation scheme was to be used. Delta Sigma Modulation was chosen because of the superior noise response and the use of feedback, as explained in Section 2.2.2. Once this was decided it was possible to design and implement a simulation in MATLAB.

3.1.1 The First Order Delta Sigma Modulator Design

The first system that was simulated and constructed was the first order delta sigma modulator. The simulation itself was based on the schematic shown in Figure 3.1, and the code was designed to represent the physical system as closely as possible.

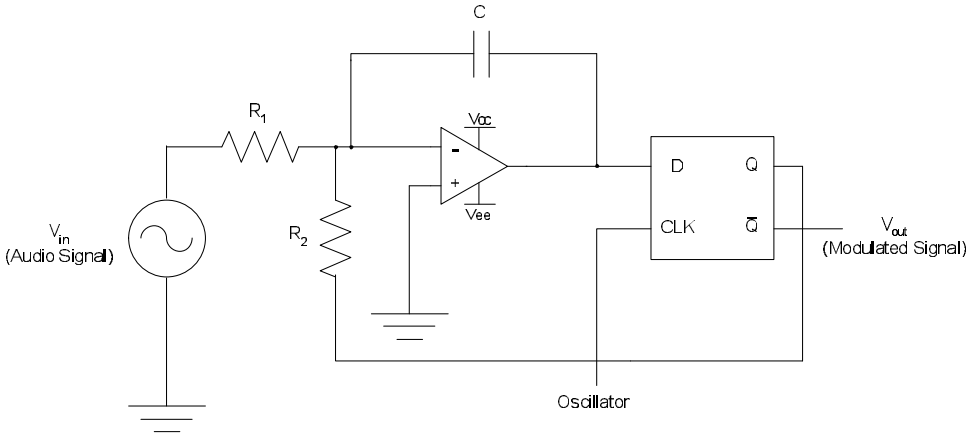

Figure 3.1: The schematic used to simulate a first order delta sigma modulator.

The input signal used to test the system was a sine wave that was biased so that the entire wave was below zero volts. R_1 and R_2 were both set to $100K\Omega$, C was set to $0.01\mu F$, V_{Qout} was represented by 4.9V, and V_{thres} was 4.2V. These values were taken from data sheets of actual components and from the idea of a physical system.

Feedback plays a large role in the functionality of this circuit. The operational amplifier (op amp) is configured to integrate an input voltage using the capacitor, C, in the feedback loop in conjunction with R_1 and R_2. The feedback also implies that the voltage on the input and output terminals is the same, as with many op amp circuits. This property, combined with the fact that negligible current can flow into or out of the input terminals of the op amp, allows the op amp to simultaneously be used as a summing amplifier. This provides the opportunity for another level of feedback, this time from the output of the flip-flop.

The input of the circuit has been biased so that the entire signal is below zero volts and the voltage on the negative terminal of the op amp is held at zero volts. This causes a current to flow across R_1 towards the input, drawing current through C. When the input signal has

a higher amplitude it will actually have a lower absolute voltage, causing the voltage drop across R1, and therefore the resulting current, to be smaller. The feedback from the flip-flop has the opposite effect. Because the output from the flip flop ranges from zero to five volts, when the output signal on $\bar{Q}$ is high, the voltage on Q is low (0V) and has no effect on the summer. When the output signal on $\bar{Q}$ is low, however, the voltage on Q is high (5V), and generates a current that flows from Q to the negative terminal of the op amp that is larger than the current drawn by the input. This nullifies any effect that the negative input voltage would have, and pushes a current through the capacitor from the negative terminal to the output. This resets the integrator, allowing for the removal of the resistor in the usual parallel capacitor and resistor combination seen in most integrator circuits. It also acts as an adjustable feedback that can be altered by changing the value of R_2. The result is a modulator with a well behaved noise response and a digital, two-state output that can be filtered with a simple low-pass filter to reconstruct the original signal.

The MATLAB simulation that was based on this circuit is available in Appendix A. The results of the simulation can be seen in Figure 3.2. They are significant because of the modulation frequency and the SNR with respect to the signal and the noise floor in the audio band. The modulation frequency is approximately accurate. With the MOSFETs that will be used, the maximum modulation frequency possible is likely to be 1MHz to optimize efficiency. Because the SNR improves with an increased modulation frequency, and 1MHz is the maximum modulation frequency, the SNR in the audio band is at its maximum for this modulator at approximately 50dB. This is unacceptable because the SNR specification for the project is 100dB. Since the modulation frequency cannot be increased without compromising efficiency, it seems that the optimal solution is to increase the order of the modulator. For this reason, a second order delta sigma modulator will be implemented.

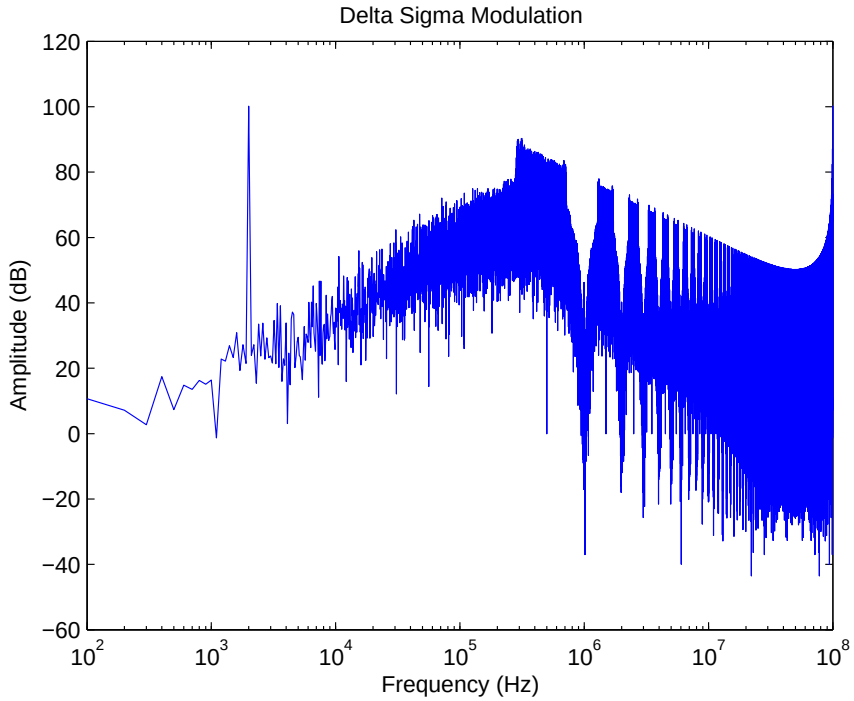

Figure 3.2: The results of the first order delta sigma simulation, conducted with a 2kHz sine wave and a 1MHz modulation frequency.

3.2 The Power Stage

The design of the power stage was important for the amplifier to meet the 90% efficiency specification. Both the configuration of the amplifier and the decision of which MOSFETs to use were key in reaching this goal.

3.2.1 Amplifier Configuration

As discussed in Section 2.3 of this document, there are two different amplification configurations that are used in Class D systems. These are the H-Bridge and the Half-Bridge. Table 2.1 shows a comparison of these systems that demonstrates that an H-Bridge would be a much better configuration for this application. Essentially, the H-Bridge eliminates DC offsets and only requires one power rail. Further, it allows for the possibility of using three-state modulation, which would increase the efficiency of the system.

3.2.2 MOSFET Selection

The choice of MOSFET is a significant factor in whether or not the amplifier will meet its efficiency specification. The most important characteristics of the MOSFET in this application are the peak drain-source voltage it can handle, the resistance in the drain-source (R_{DS-on}), the gate capacitance (C_{GS}), the time it takes to turn on and off (t_{rise} and t_{fall}) and the voltage required to drive it.

Peak Voltage

Since the system must be able to handle an average of 80 Watts, it must be designed to survive peaks of up to 160 Watts. The resulting peak voltage can be therefore be found using the following equations.

$R = 8\Omega$ and

$P = 160$ watts

$P = \frac{V_{Peak-RMS}^2}{R}$

$V_{Peak-RMS} = \sqrt{PR}$

$V_{Peak-RMS} = \sqrt{8 \cdot 160}$

$V_{Peak-RMS} = 35.8V$

$V_{Peak} = V_{Peak-RMS} \cdot \sqrt{2}$

$V_{Peak} = 50.6V$

Based on this, the MOSFET must be able to handle a 50V rail in order to be considered.

Loss Terms

The losses in the MOSFETs are mainly a result of two different terms. The first is the R_{DS-on} loss term that describes the losses when the MOSFET is on. This is caused by an equivalent resistance in the switch. The equation for R_{DS-on} losses is shown in Equation 3.1.

$$PD_{Resistive} = I_{out}^2 \cdot R_{DS-on} \tag{3.1}$$

In the worst-case scenario there would be $40V_{RMS}$ across an 8Ω load that would produce a current output of $5A_{RMS}$. The final equation for resistive power dissipation is therefore:

$$PD_{Resistive} = 25 \cdot R_{DS-on} \tag{3.2}$$

In addition to these resistive losses, there are losses associated with switching. These are a result of the gate capacitance of the MOSFET, which implies that the gate must charge up when there is a voltage applied to it. This determines the rise and fall times. A general timing diagram of how a MOSFET works is shown in Figure 3.2.2.

These losses can be calculated using the following equations. The derivation for these equations is included in Appendix D:

$$PD_{Switching} = (t_{rise} + t_{fall}) \cdot \frac{V_{DD}}{R_{Load}} \cdot f_{sw} \tag{3.3}$$

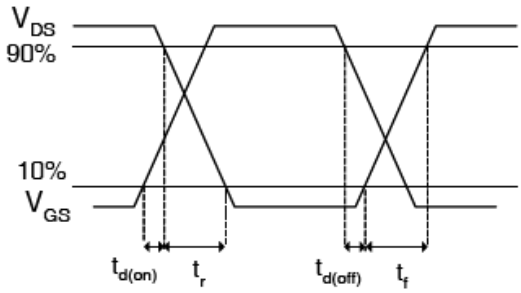

Figure 3.3: A MOSFET timing diagram.

$$PD_{C_{GS}} = f_{sw} \cdot C_{GS} \cdot V_{Drive} \tag{3.4}$$

Note: In these equations f_{sw} is the switching frequency of the MOSFET, V_{Drive} is the driving voltage of the MOSFET, I_{out} is the output current from the MOSFET, and V_{DD} is the voltage across the MOSFET.

There are also some important loss equations that depend on the filter. The derivations for these equations are also given in Appendix D. They will become increasingly important when deciding which filter components to choose, but also play an important part in determining how the system will interact with different MOSFETs.

$$PD_{FilterInductor} = \frac{V_{DD}^2 \cdot r_L}{192 \cdot L^2 \cdot f_{sw}^2} \tag{3.5}$$

$$PD_{FilterCapacitor} = \frac{V_{DD}^2}{192 \cdot r_C \cdot R_{Load}^2 \cdot C^2 \cdot f_{sw}^2} \tag{3.6}$$

Using these equations and the loss equation for resistive power dissipation, the total losses for a MOSFET at a given frequency can be determined.

Comparison Chart

The MOSFETs in Table 3.1 were considered because they met the peak voltage requirement and had relatively low drain-source resistance and gate capacitance.

Part Number	Peak Voltage	R_{DS-on}	C_{GS}	t_{rise}	t_{fall}	Price
IRF1010EZ	60V	8.5 mΩ	2810 pF	90 ns	54 ns	4.80
IRF3805	75V	3.3 mΩ	7960 pF	150 ns	93 ns	6.48
IRF3808	75V	7.0 mΩ	5310 pF	140 ns	120 ns	4.11
IRF1405	55V	4.9 mΩ	4780 pF	110 ns	82 ns	5.35
IRF3205	55V	6.5 mΩ	3450 pF	95 ns	67 ns	3.34
IRF6645	100V	28 mΩ	890 pF	5 ns	5.1 ns	2.98
IRF6665	100V	53 mΩ	530 pF	2.8 ns	4.3 ns	2.98

Table 3.1: MOSFET Comparison Table

Based on the values in Table 3.1 and the equations above, the losses for each MOSFET were calculated. In order to do this, a "dummy filter", based on the values in Table 3.2, was applied [TI:99]. Combining all the loss terms, the curves in Figure 3.4 were produced to compare the different MOSFETs to see which ones would incur the lowest losses.

DC Load Resistance $(R_L - \Omega)$	Cutoff Frequency $(f_C - kHz)$	Inductor Value $(L - \mu H)$	Capacitor Value $(C_L - \mu F)$
4	20	22.5	1.41
4	25	18	1.13
4	30	15	0.94
4	35	12.9	0.80
8	20	45	0.70
8	25	36	0.56
8	30	30	0.47
8	35	26	0.40

Table 3.2: The values for the "dummy filter" [TI:99]

Immediately one MOSFET stands out among the rest. Based on this loss curve, the IRF6645 MOSFET was used for this project.

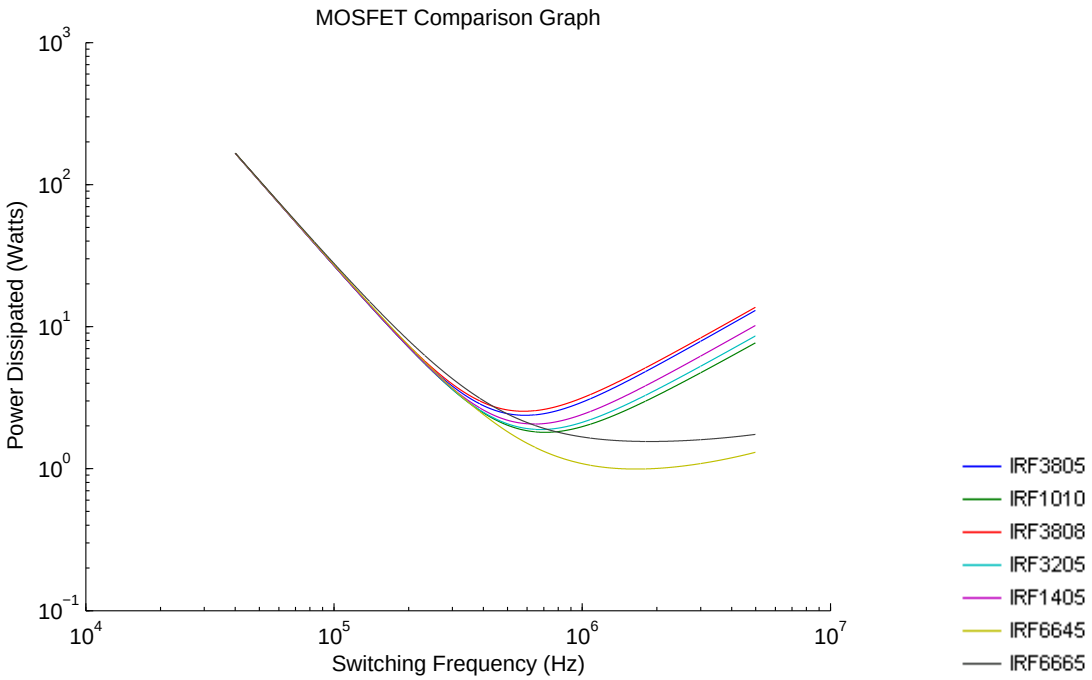

Figure 3.4: The curves for each simulated MOSFET.

3.2.3 MOSFET Drivers

As an International Rectifier MOSFET was chosen for the power stage, it was decided to use International Rectifier MOSFET drivers to control the MOSFETs. This has several advantages, most important being that the parts are designed by the manufacturer to work together. This helped to reduce issues in the design of the power stage, including shoot-through, which is the biggest concern for the first revision of the power stage. Shoot-through in an H-Bridge occurs when both MOSFETs on one side turn on at the same time, allowing a direct path from the high voltage rail to ground. There were several choices of MOSFET drivers from International Rectifier, each with slightly different features. The most useful driver was the IRS20124s, which has a user-selectable dead time. Being able to control the amount of dead time was very useful, and allowed for finer control of total harmonic distortion and reduce the chance of shoot-through.

3.3 Filter

As discussed in the Chapter 2, the third stage of a Class D amplifier is the filtering stage. The switching nature of the Class D amplifier causes it to emit a significant amount of noise above the audio band. While this noise is shaped by the modulator to be above the 20 KHz upper limit of human hearing, it can still cause problems. The biggest concern is electromagnetic interference (EMI) in equipment along the path of the cabling from the amplifier to the speaker. To help mitigate the issues caused by the higher frequency content of the signal, a low-pass filter must be placed before the final output of the amplifier.

The filter stage is the simplest stage of a Class D audio amplifier. A simple low-pass filter is all that is required, as the audible band of frequencies can be considered a base band signal when designing an audio amplifier. Since the power stage is an H-Bridge, the filter is required to be a balanced filter. This means that there are essentially two separate, but identical filters on either side of the load. This does increase the cost of the final product, but it is necessary due to the type of power stage used. The H-Bridge and balanced filter design help reduce noise in the output by eliminating odd harmonics, which improves the THD.

While there are a number of different filter types, the nature of audio suggests the use of a Butterworth filter. A Butterworth filter has a very flat pass-band, important for the frequency response specification of an audio amplifier. The slope of the cutoff of a Butterworth filter can be easily adjusted by increasing the order of the filter, which is accomplished by cascading additional inductors and capacitors. Due to the shape and location of the high frequency noise generated by a $\Delta\Sigma$ modulator it was determined that a second order Butterworth filter would provide the best cost and efficiency to performance ratio.

Once the order is decided, the two parameters that define a Butterworth filter are the cutoff frequency and the slope of the cutoff. A second order filter results in a slope of -40 dB/decade, which is sharp enough to reduce the high frequency noise to acceptable levels. The second parameter, the cutoff frequency, determines the component values that should

be used. For the first filter design, a cutoff frequency of 25 kHz was selected to provide a slight buffer above the audio band, while still attenuating most of the out-of-band noise. This allows for some tolerance in filter components, which decreases the cost of the filter. Once the cutoff frequency and the slope of the cutoff were chosen, it was possible to consider specific filter components.

3.3.1 Filter Components

The specifications of a Butterworth filter are entirely determined by the value and configuration of the components, in this case the inductors and capacitors. Since a balanced filter consists of two identical filters, one on either side of the load, it is possible to use a half circuit model to derive filter component values. The half circuit model is depicted in Figure 3.5.

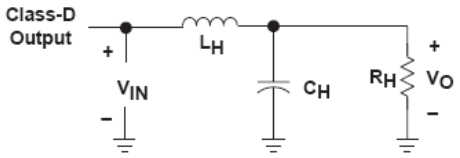

Figure 3.5: Half circuit model of the second order Butterworth filter.[TI:99]

Equations 3.7, 3.8, and 3.9 were derived using the half model circuit to determine the filter components.

$$R_H = \frac{R_L}{2} \tag{3.7}$$

$$C_H = \frac{1}{2\pi f_c \sqrt{2} R_H} \tag{3.8}$$

$$L_H = \frac{\sqrt{2} R_H}{2\pi f_c} \tag{3.9}$$

Using these equations, discrete filter components were selected.

$$C_H = \frac{1}{2\pi \cdot 25\text{kHz} \cdot \sqrt{2} \cdot 4\Omega} = 1.13\mu\text{F} \tag{3.10}$$

$$L_H = \frac{\sqrt{2} \cdot 4\Omega}{2\pi \cdot 25\text{kHz}} = 18\mu\text{H} \tag{3.11}$$

Once ideal component values were chosen, real world components were identified. This resulted in a problem, as a 1.13 μF is not a standard capacitance. Several ceramic surface mount capacitors were found with a capacitance of 1.2 μF, but they were prohibitively expensive. However, it was possible to slightly adjust the component values with Equation 3.12, potentially allowing for a pass-band that was not as flat as desired.

$$f_c = \frac{1}{2\pi\sqrt{2L_H C_H}} \tag{3.12}$$

While 1.13 μF is not a standard capacitance, 1 μF is. Using the same cutoff frequency of 25 kHz and a C_H of 1 μF it was determined that a 22 μH inductor was required. In addition to the specific inductance, a low Equivalent Series Resistance (ESR) was required. It was necessary for the inductor to have a low ESR because it was in series with the speaker, so all of the power from the amplifier flowed through the inductor. Using an inductor with a high ESR would have significantly lowered efficiency measurements, which would have been very undesirable for a Class D amplifier. The ESR of the capacitor was of less importance, as the desired audio signal went through the load, which was in parallel with, and therefore unattenuated by, the capacitor. The components chosen for the filter were:

Capacitor - Taiyo Yuden UMK325BJ105KH-T (1 μF)

Inductor - Bourns JW Miller 2305-H-RC (22 μH, 7mΩ)

These components were then placed between the MOSFETs and the load, as depicted in Figure 3.5. Once these filter components were chosen it was possible to construct the first amplifier revision.

3.4 System Implementation

After designing the stages for the first iteration of the Class D Audio Amplifier, the pieces had to be put together. Since the modulator was not in a final design stage, it was assembled on a breadboard. The power stage and filter were fabricated on a PCB because of the need for surface mount parts and the fact that at high frequencies there would have been a significant amount of noise and signal attenuation with the use of a breadboard, especially at 100 watts. The following section describes how the designs described in the above sections were assembled and implemented.

3.4.1 First Order Modulator

The first order modulator was constructed on a breadboard for testing with the power stage, as well as to prove that the concept was feasible. It was assembled based on the schematic shown in Figure 3.1. Only through-hole components were used in the assembly of the modulator. R_1 and R_2 were both 5% $100K\Omega$ ceramic resistors, C was a $0.01\mu F$ ceramic capacitor, an LM356 was used for the op amp, and the flip-flop was a 74HC74A. The clock signal for the flip-flop was generated by an ECS_2100 1MHz oscillator. This configuration can be seen on the bread-board in Figure 3.6.

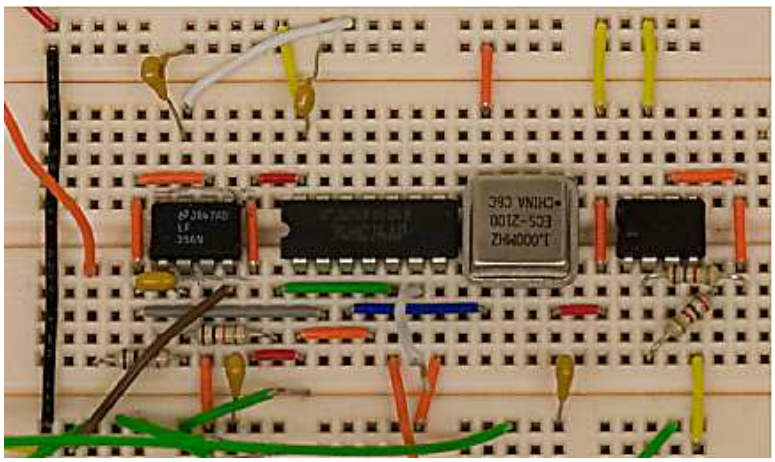

Figure 3.6: The bread-board containing the modulator shown in the schematic in Figure 3.1.

3.4.2 PCB Layout for Power Stage and Filter

Since the power stage had specialized surface mount MOSFETs and drivers, the stage had to be fabricated on a PCB. This was created using the Multisim and Ultiboard software package from National Instruments. First a schematic was created in Multisim. This schematic is shown in Appendix G. This was transferred to Ultiboard to begin the process of laying out a PCB.

In designing the PCB, logical layout was extremely important. Since there was a degree of uncertainty regarding whether or not the design would work, since none of the team members had used this particular MOSFET and driver set, it was crucial to leave room for changes and set up test points to simplify debugging. All of the components aside from the inductors were surface mount components to avoid cluttering up the board and incurring excess losses. There were two BNC connectors used as injection points for each side of the H-Bridge. Either a modulated signal or a square wave and an inverted square wave could be applied to these inputs to test the functionality of the board.

Figures 3.7 and 3.8 show the evolution of the board.

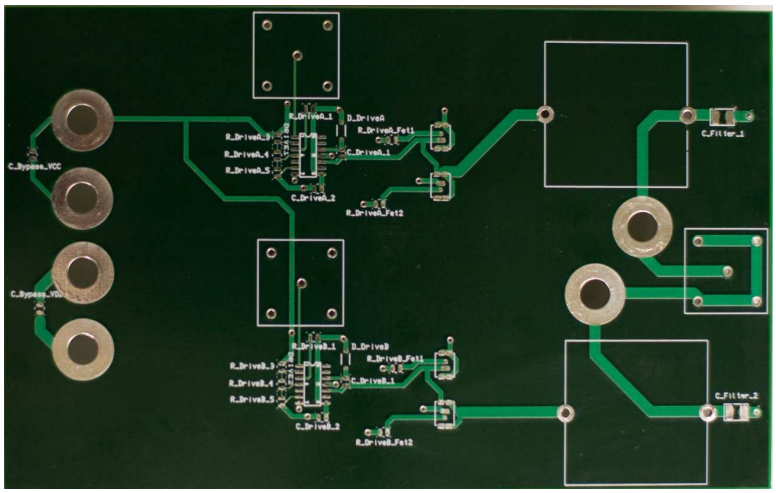

Figure 3.7: The PCB of the Power Stage without Components

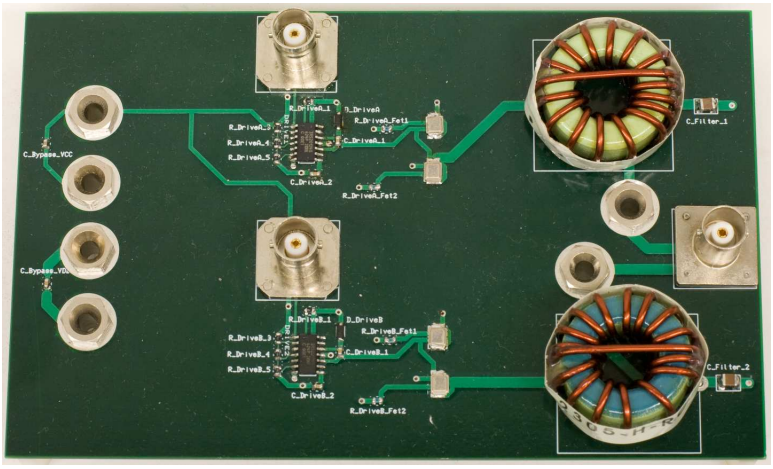

Figure 3.8: The PCB of the Power Stage with soldered components Components

3.4.3 Full System Assembly

Once the PCB and modulator were constructed, the next step was to assemble the full system by connecting them. The PCB had already been designed to take two inputs from any modulator and output to a speaker. Since there were tests to be conducted on the PCB and uncertainties regarding the functionality of the system, the team decided not to use a speaker directly for this iteration. An 8Ω resistor was fashioned by wiring up 8 - high-power 1Ω resistors together and screwing them all onto a heat-sink. Figure 3.9 shows this resistor configuration.

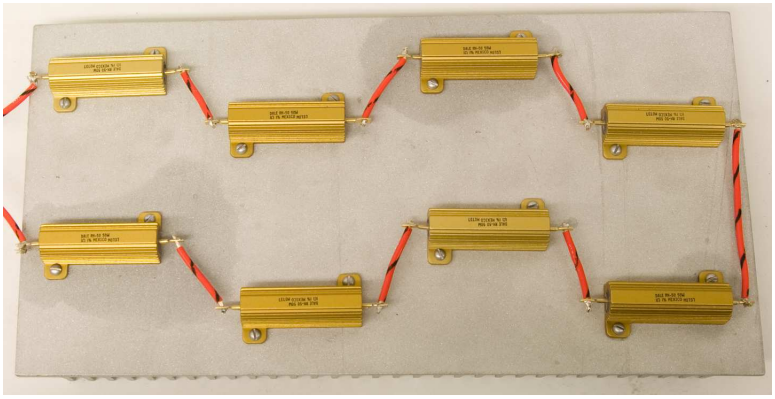

Figure 3.9: The Resistor Used for Testing

Finally all the parts were in place to begin testing. Figure 3.10 shows the entire system connected together with all the components in place.

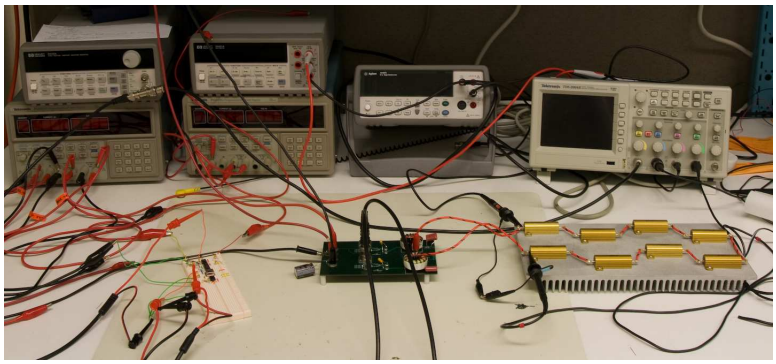

Figure 3.10: The PCB of the Power Stage without Components

Chapter 4

Preliminary Results

The following section discusses the results obtained from the testing conducted on the design described in Chapter 3. As stated in that chapter, it was not expected that this design was going to meet all of the specifications outlined in Section 1.1. The testing for this iteration was mainly for functionality and to see determine the efficiency and signal quality performance of the amplifier, despite the known flaws in the initial design. The following section discusses the results of the tests that demonstrated that this preliminary design was fully functional.

4.1 Functionality Testing

Testing for functionality was the most important aspect of preliminary testing because the goal was to make sure the design would amplify an input signal. To do this, testing was conducted on each stage independently and the results were compared to an expected outcome. Once each stage had passed a unit test for functionality, the whole system was assembled to determine whether the different stages would interact with each other as expected.

4.1.1 Modulator Functionality

The modulator, as the first stage, was tested for functionality to determine whether it could pass a modulated sine wave to the power stage for amplification. A qualitative analysis of the modulator output indicated that it was functioning as expected. Figure 4.2 shows the input to the system in yellow on Channel 1 and the output of the modulator in blue on Channel 2, as captured by the oscilloscope. The output of the modulator has the maximum number of state-transitions when the input waveform is closer to zero, which was an effect seen in simulation of the first order modulator, shown in Figure 4.1. Like the simulation, the output also contains longer pulses, either high or low depending upon the amplitude of the input, that correspond to the maximum and minimum points of the input. The only significant difference between the appearance of the simulation and the oscilloscope readings is the scaling that has been performed on the output of the modulator in the simulation. This simulated signal was halved in order to match the 2 volts/division setting that was used on the output of the actual system to allow it to fit on the oscilloscope screen. In the original simulation, both the input and output signals of the simulation and the oscilloscope matched in amplitude.

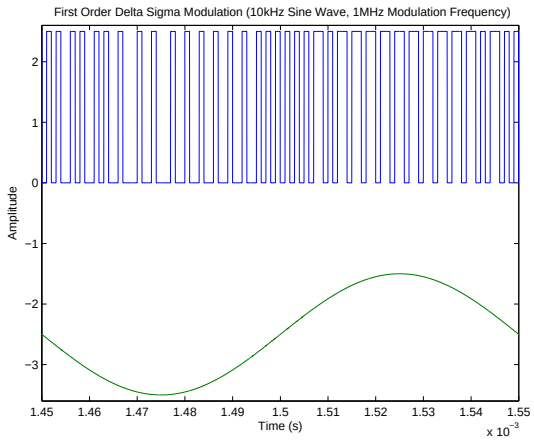

Figure 4.1: The MATLAB simulation of the first order modulator.

Further proof of the functionality of the first order modulator is offered in Section 4.1.4,

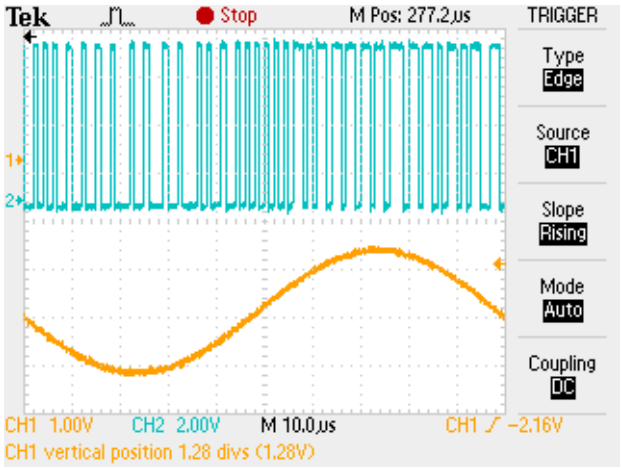

Figure 4.2: The output of the first order delta sigma modulator, with a 1MHz modulation frequency and a 10kHz sine wave.

when the entire system is assembled and the modulator output is fed into the power stage, and filtered. A quantitative analysis of the modulator as a unit was not performed. This was because it was already clear from simulations that the first order modulator would not meet the necessary specifications, and that it would make sense to move to a second order modulator. The construction of the first order modulator was simply a tool to determine that the general design was functional and to provide the means for testing the remainder of the system: the power stage and filter on the PCB.

4.1.2 Power Stage Functionality

Once the power stage was assembled on the PCB, it was necessary to test it before connecting it to the bread-boarded modulator. Since there were two BNC connectors to serve as inputs to either side of the H-Bridge, this did not pose any major problems. The first point to check was whether or not the drivers could produce an output signal. After assembling only the driver circuit without the MOSFETs, a square wave was applied to the input and the output was monitored. The driver circuit was proven functional when a square wave was observed on the high side of the driver that followed the input square wave, along with another square wave on the negative side of the driver that was an inverted form of the input.

Once the drivers were working, the MOSFETs were added and the rails on the MOSFETs were powered to determine whether they were switching based on the signal from the driver. This test was still conducted one stage at a time. The result was a square wave that followed the input signal, ranging from 0V to 40V on the output, as expected. Figure 4.3 shows an example of one of these outputs. In this figure, Channel 1 (yellow) represents the input while Channels 3 and 4 (purple and green, respectively) represent the driver outputs. Channel 2 (blue) is the full output of the power stage.

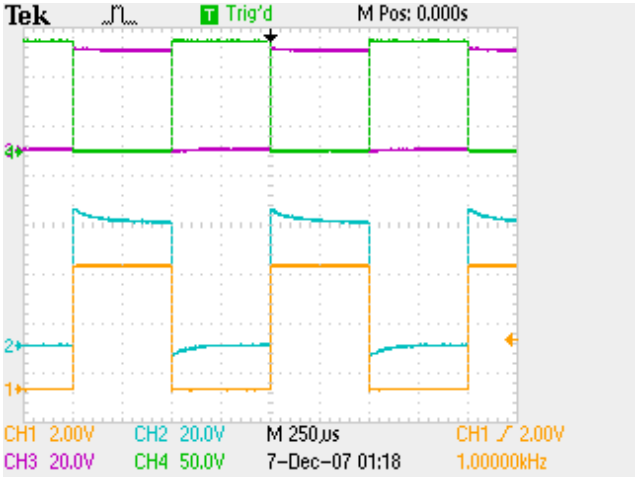

Figure 4.3: The Power Stage Output

These tests proved that the drivers and MOSFETs were working correctly.

4.1.3 Filter Functionality

Once the power stage was working it was necessary to test the filter. Because the filter was a balanced filter designed for an H-bridge, it was extremely difficult to test the filter independently of the power stage. As a result, the method used to test the filter involved connecting it to the power stage and applying a square wave on one half of the H-Bridge. The input to the other half of the H-bridge was supplied by a 74C04 inverter, which applied the inverse of the original square wave. This was the first time that the full power stage was in use. Since the filter was to be low-pass with a cutoff frequency of 25kHz, the output was

expected to vary based on the input frequency. If the frequency of the square wave input was significantly below the cutoff frequency, enough to allow three or four harmonics to pass through the filter, then a square wave from -40V to 40V would be the expected output.

This was originally tested by connecting the oscilloscope across the resistor load in the filter. In this configuration, due to the internal grounding of the oscilloscope, the grounding loop of the probe was connected to the same ground as the PCB causing the test to fail. The testing procedure was then modified to use a grounded probe at each end of the resistor and subtract the two values using the MATH function on the oscilloscope. A picture of this setup is shown in Figure 4.4.

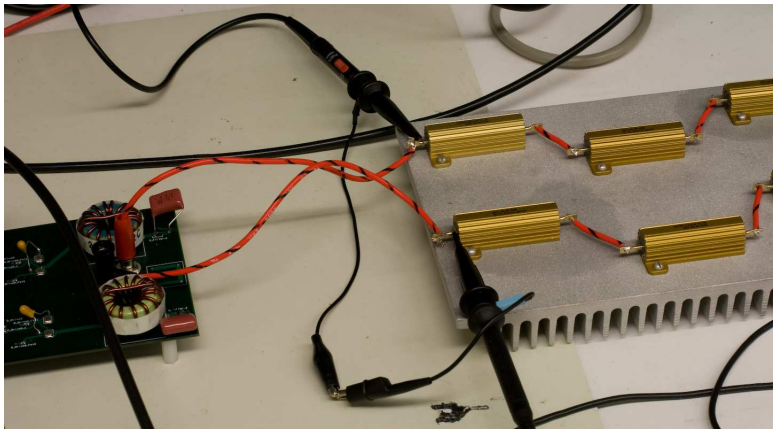

Figure 4.4: The configuration of the test resistor and the oscilloscope probes.

The Figures 4.5 and 4.6 show some of the results of 1kHz and 10kHz square wave inputs to the power stage and the filter. Figure 4.5 shows that the 1kHz square wave was applied to the system, was amplified, and remained unfiltered. This is because it had many harmonics that were within the pass-band of the filter. In contrast, Figure 4.6 shows that the 10kHz square wave was amplified but since it only had two harmonics in the pass-band, the output more closely represented a sine wave than the input did.

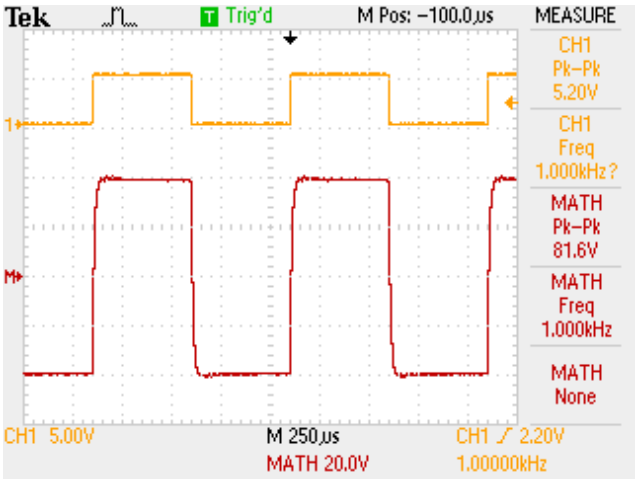

Figure 4.5: The power stage and filter with a 1kHz square wave input

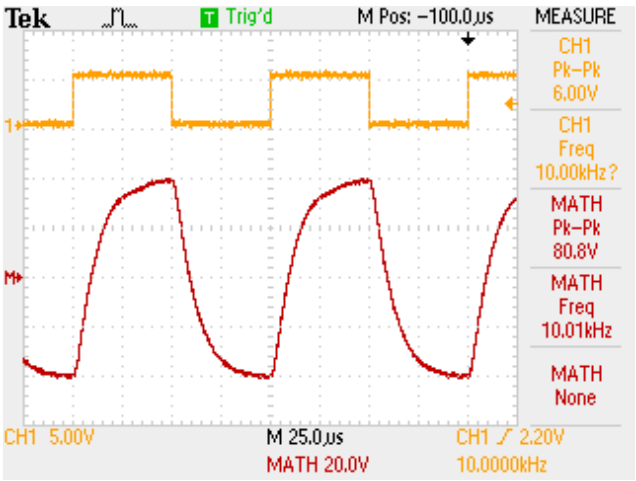

Figure 4.6: The power stage and filter with a 10kHz square wave input.

4.1.4 System Functionality

Once all the individual tests were completed, the final step was to connect the modulator to the inputs of the PCB. In this stage of testing, the functionality tests of the modulator were verified when the system output was filtered. This test indicated that the modulator was functional because the input waveform was replicated at the output of the filter.

For this functionality test, a sine wave served as the input to the modulator. This input was offset by -1.5V, for reasons noted in Section 3.1.1. It was determined that if the output was an amplified version of the input, with some reasonable amount of distortion due to the known issues with the modulator, then that would prove that the full system was functional. Figures 4.7 and 4.8 show the outputs of the full system.

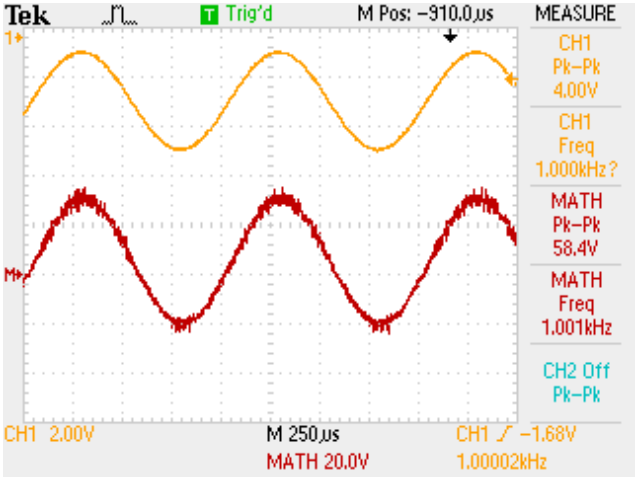

Figure 4.7: The full system with a 1kHz sine wave input.

These figures show that the complete system was able to modulate both a 1kHz and 10kHz signal, amplify them, and filter them back out to produce sine waves at the output. The outputs are noisier than would be desired, but this is because the design was still in its first revision.

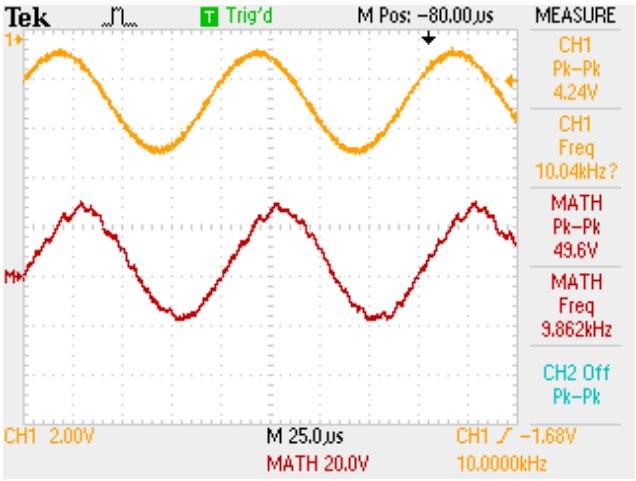

Figure 4.8: The full system with a 10kHz sine wave input.

4.2 Efficiency Testing

Once it was shown that the filter was completely functional, tests were run to determine how efficient the first iteration of the system was. It was noted that changing the input frequency and amplitude would change the efficiency measurements, so this test included sweeping through a set of frequencies in the audio band and going from a small input signal to the largest input signal that the system could handle while measuring efficiency. The efficiency was calculated by taking the input current from the power stage, measured with digital ammeter, multiplying it by the measured input voltage to get the input power. Then, the output RMS voltage was measured on the load and that was squared and divided by the output resistance (8.05Ω) to get the output power.

$$\text{Efficiency} = \frac{P_{out}}{P_{in}} \tag{4.1}$$

$$P_{in} = V_{in(DC)} \cdot I_{in(DC)} \tag{4.2}$$

$$P_{out} = \frac{V_{out(RMS)}^2}{R_{load}} \tag{4.3}$$

$$\text{Efficiency} = \frac{V_{in(DC)} \cdot I_{in(DC)}}{\frac{V_{out(RMS)}^2}{R_{load}}} \tag{4.4}$$

Using this data, various frequencies and amplitudes were tested and the values were recorded to calculate efficiency. As shown in the plots in Figures 4.9 to 4.13, the efficiency was above the specification of 90% for some input values but not for others. This was improved upon in the final design.

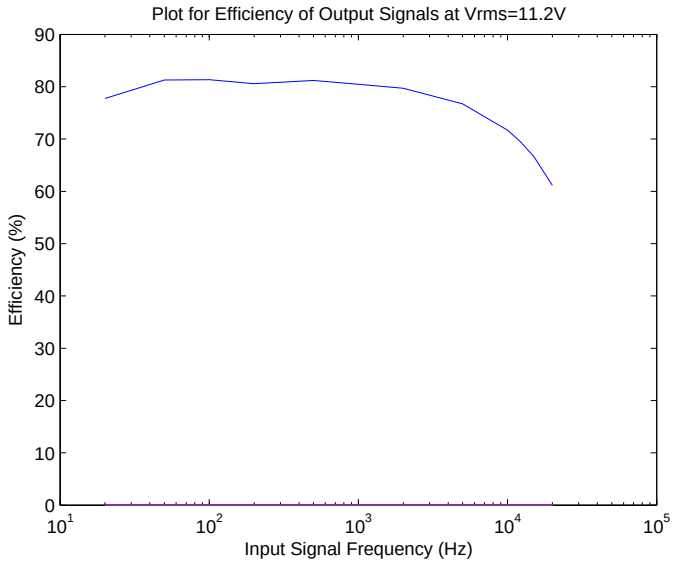

Figure 4.9: Efficiency Plot at $11V_{RMS}$ at the Output

4.3 Frequency Response Testing

The frequency response of the system was also tested on the first iteration of the board. This test was conducted using the same data as was used in Section 4.2. For these plots, the gain was calculated by dividing the output RMS voltage by the input RMS voltage (see Equation 4.5).

$$Gain = \frac{V_{out(RMS)}}{V_{in(RMS)}} \tag{4.5}$$

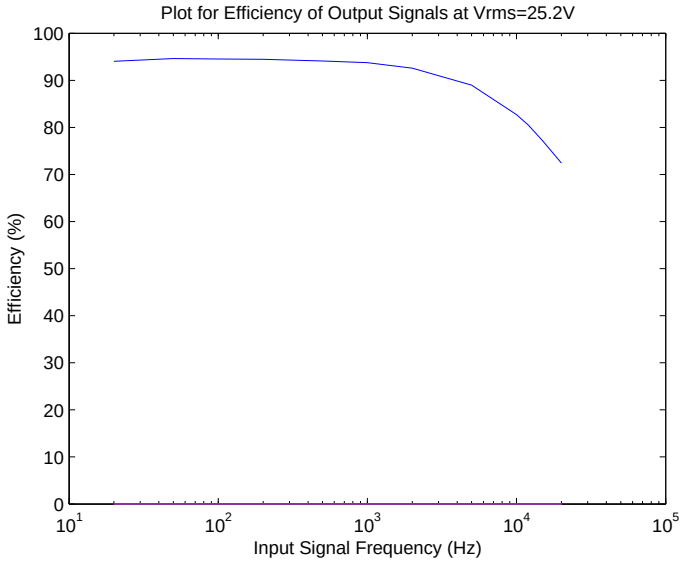

Figure 4.10: Efficiency Plot at $25V_{RMS}$ at the Output

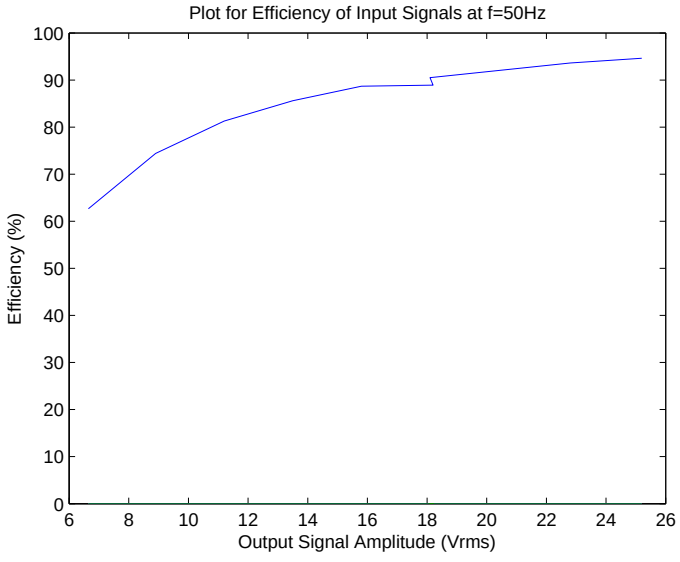

Figure 4.11: Efficiency Plot at 50Hz

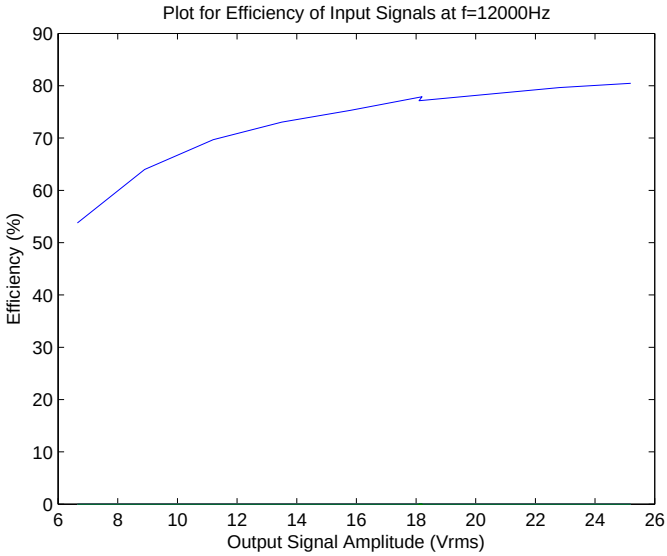

Figure 4.12: Efficiency Plot at 1200Hz

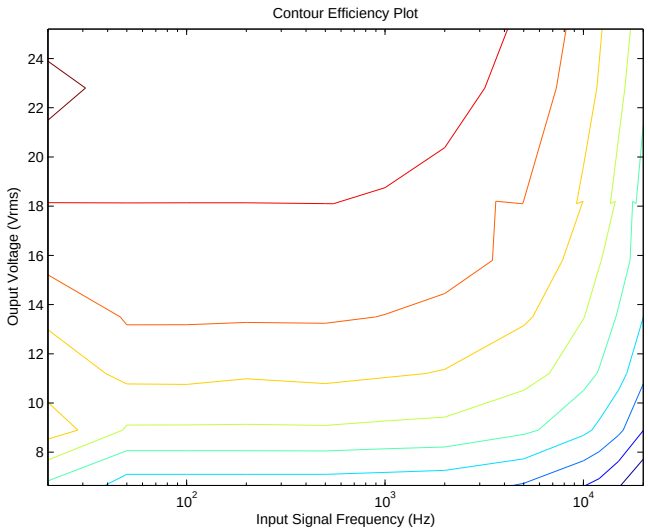

Figure 4.13: Efficiency Plot at all Frequencies and Output Voltages

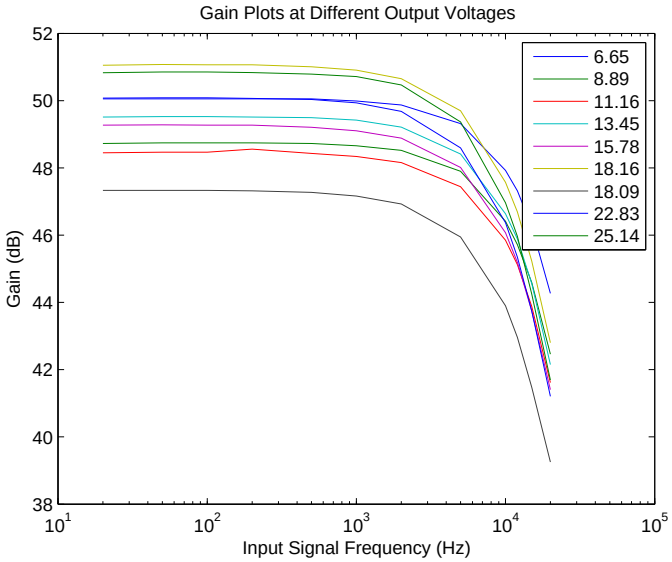

Figure 4.14: Frequency Response Plots

As shown in Figure 4.14, the frequency response was not ideal. The frequency roll-off began inside the audio band. This was remedied with a change of the cut-off frequency from 25kHz to 30kHz and a recalculation of the filter component values.

4.4 Problems with the Preliminary Design and Tests

There were a number of problems with this design. Some of them were expected and some were not. It was expected that the output would be fairly noisy since the modulator was only a first order, two-state modulator, whereas in the final design the modulator was a second order, three-state modulator. This also explained why the efficiency did not meet the specification. A few other problems surfaced during the testing phase, however. This section discusses the different problems discovered. The solutions to these problems are discussed in Chapter 5.

The first major problem was the instability of the MOSFETs. During normal testing the MOSFETs would burn out after minimal use. This was fairly difficult to diagnose because there were a number of reasons for it. One of the major reasons was that it was very

difficult to solder the IRF6645 MOSFETs because of the unexposed pads on the bottom of the package. Even when the MOSFETs were adhered to the board, it was difficult to determine whether or not the leads on the inner pads were actually connected. Another reason for this failure was that there was some initial testing with the filter stage without a load resistor. It was later discovered that this could be very harmful to the components in the power stage because the inductor and capacitor on the filter could store a lot of energy with no discharge point. This energy could build up and damage the MOSFETs. Another problem that caused burning out of MOSFETs was the original testing design. Originally it was thought that the oscilloscope probe could simply be placed across the resistor in the H-Bridge. The resistor was ungrounded, however, and since the oscilloscope probe grounds are tied to earth ground, any voltage on the resistor was incorrectly shorted to ground.

Another problem with this design was that the board was "singing" whatever was at the output. It was later found out that the X7R capacitors were causing problems with microphonics. In general, the dielectric in an X7R causes physical movement at its operating frequency. If that frequency is in the audible band and has high enough power, it will be audible. This can also add distortion to the system. This was fixed by using different capacitors in the final design.

There was also a problem using the function generator. During the efficiency and frequency response tests, the function generator was set to act like there was a 50Ω load, since this was the default setting. For this application, however, it was necessary for that setting to be changed to "High Z". This was fixed in the test plan for the final iteration.

The final problem was that the filter response was not ideal. It was discovered that there was a calculation error in the filter design of this stage. This problem and its resolution are discussed in Section 5.3.

Chapter 5

Final Design

The preliminary design had many problems which were outlined in Section 4.4. These problems were all addressed and corrected in the final design of the Class D Audio Amplifier. Most notably, the modulator stage was changed from a first order, two-state modulator to a second order, three-state modulator. This chapter explains how these changes were made to each of the stages and how the final PCB was constructed.

5.1 The Second Order Modulator

The design of the second order modulator differed greatly from the design of the first. Because the first order modulator was extremely simple, due to its single feedback path, designing a simulation to match a typical schematic required little preparation. The only components that could be altered were the input resistor, the feedback resistor, and the capacitor that affected the constant of integration. A second order modulator typically contains two integrators and either two or three feedback paths, creating stability issues and a need to consider a number of different feedback paths at once. As a result, it was not immediately feasible to simulate the second order modulator as a circuit with real resistor and capacitor values. Developing a system model and determining the coefficients of feedback, the constants of integration for both integrators, and the coefficients in the signal path made it possible to

determine how the system would react using more theoretical, and therefore more simple, methods.

5.1.1 System Model

The system model of a second order delta sigma modulator is developed in Schreier's Understanding Delta-Sigma Data Converters, and is shown in Figure 5.1 [ST05]. Using this model of a second order modulator, the coefficients were determined to adjust the noise transfer function in Equation 5.1.

$$Q_{IN} = Q_{OUT}[\frac{-a_3 \cdot C_3 \cdot s^2 - a_2 \cdot C_2 \cdot C_3 \cdot s - a_1 \cdot C_1 \cdot C_2 \cdot C_3}{s^2}] + V_{IN}[\frac{B \cdot C_1 \cdot C_2 \cdot C_3}{s^2}] \quad (5.1)$$

Noise shaping is one of the greatest advantages of delta sigma modulation, and this model provided an opportunity to optimize the noise transfer function. The feedback coefficients (a_1, a_2, a_3) were determined, using the MATLAB script in Appendix B to be: $(a_1, a_2, a_3) = (\frac{4}{9}, \frac{4}{15}, \frac{11}{90})$. The MATLAB simulation in Appendix C was then developed to represent the system model, using the values determined by the a coefficients, and setting $B = C_1 = C_2 = C_3 = 1$. B, C_1, C_3 and C_3 were then adjusted to produce the desired noise transfer function. As shown in the simulation, the final values were $(B, C_1, C_2) = (1/3, 1000000, 1000000)$. C_3 was eliminated because it was determined to equal to one, and therefore had no effect on the system. C_1 and C_2 were determined to be equal to the modulation frequency of 1MHz. It was also determined that for efficiency reasons, the modulator should output a three-level signal. The simulation reflects this, as the quantizer was developed to have three levels. This simulation, with these coefficients, produced the results shown in Figure 5.2.

5.1.2 Physical Realization

Once the coefficients were determined, it was necessary to turn the system model into a physical system. It is important to note that the coefficients could still be adjusted, under

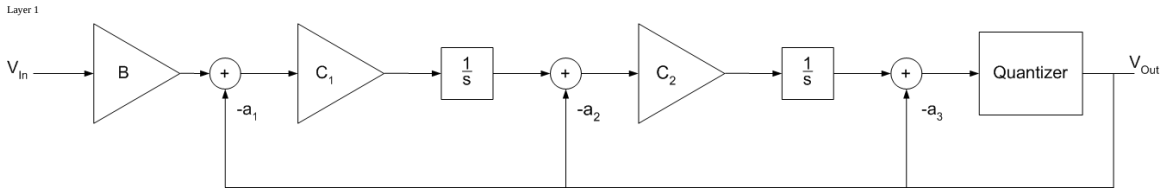

Figure 5.1: The discrete model of a second order delta sigma modulator [ST05].

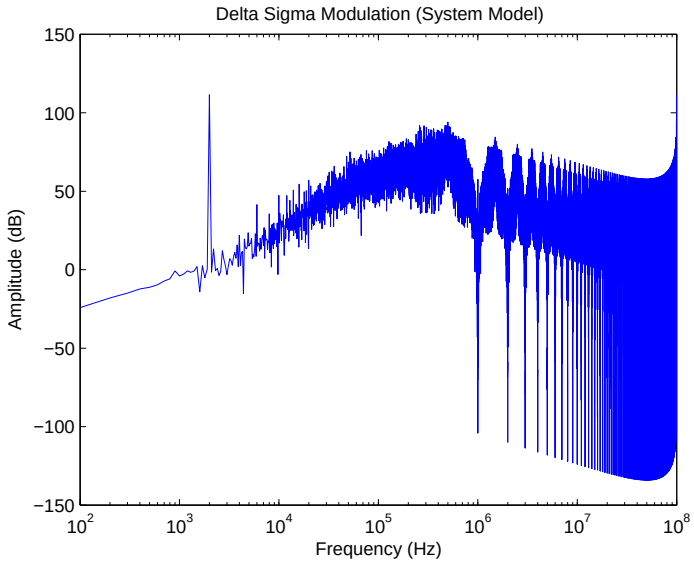

Figure 5.2: The results of the system model simulation after adjusting the coefficients.

the condition that the four terms in the noise transfer function, $-a_3 \cdot s^2 \cdot$, $-a_2 \cdot C_2 s$, $-a_1 \cdot C_1 \cdot C_2$ and $B \cdot C_1 \cdot C_2$, remained the same. If C_1 were halved, for instance, a value of another coefficient in the third and fourth terms must be doubled to compensate. An approximation of a physical system was accomplished using a spice package, because it was easier to simulate a system with real components in a spice package than in MATLAB, and it was less expensive and time-consuming to do so than to use real components. The first step was to develop a system that would be less than practical to implement, but that served as an intermediate step between the MATLAB simulation and the final implementation of the system. In the final design, the op amps used as integrators also served as summing amplifiers, integrating the sum of the input to the integrator and the modulator system feedback. This idea, in the developmental stages, is complicated by the fact that the resistors that scale the input and feedback for summing also contribute to the coefficient of integration of the integrator. In order to simplify the system and allow it to, at first, more directly represent the system model simulation, an extra summing amplifier was added before each integrator, as shown in Figure 5.3. Figures 5.4 and 5.5 show the results of the simulation.

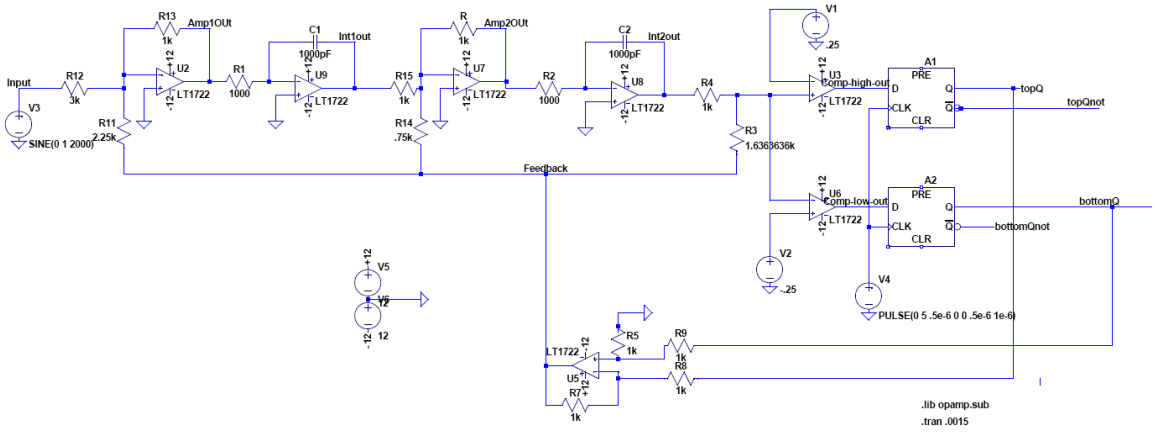

Figure 5.3: The intermediate stage between the MATLAB simulation of the system model and the final system.

The final stage was developed by replacing the summing amplifiers, one at a time, with summing resistors on the integrators and ensuring that the functionality of the system had

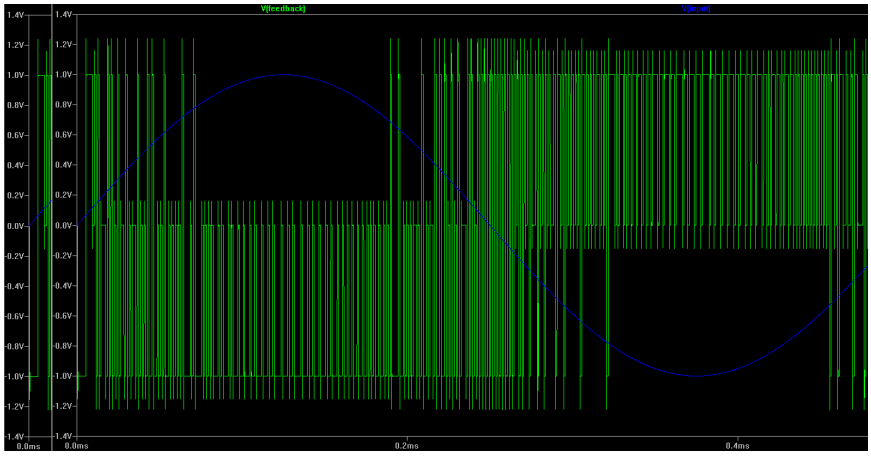

Figure 5.4: The output of the intermediate stage between the MATLAB simulation of the system model and the final system.

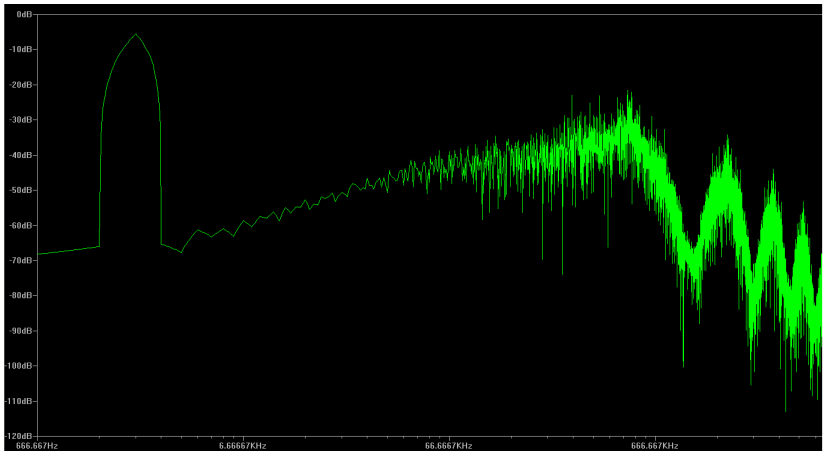

Figure 5.5: The Fast-Fourier Transform (FFT) of the intermediate stage output.

not changed. The resistor values were determined by first examining the system as a result of the input, and then as a result of the feedback. Considering one set of summing and integrator amplifiers, it was assumed, temporarily, that the feedback would be zero. The voltage output of the summing amplifier would then be a result of the input voltage alone. That voltage would then be applied to the integrator circuit, and would cause a current to flow across the input resistor to the integrator. That current was the desired current contribution to the integrator from the input, and the value for the resistor between the input and the integrator could be chosen accordingly, as the input voltage range is known. The process was repeated, assuming temporarily that the input was zero, and the feedback had a known voltage. The final circuit, with all summing amplifiers removed, is shown in Figure 5.6.

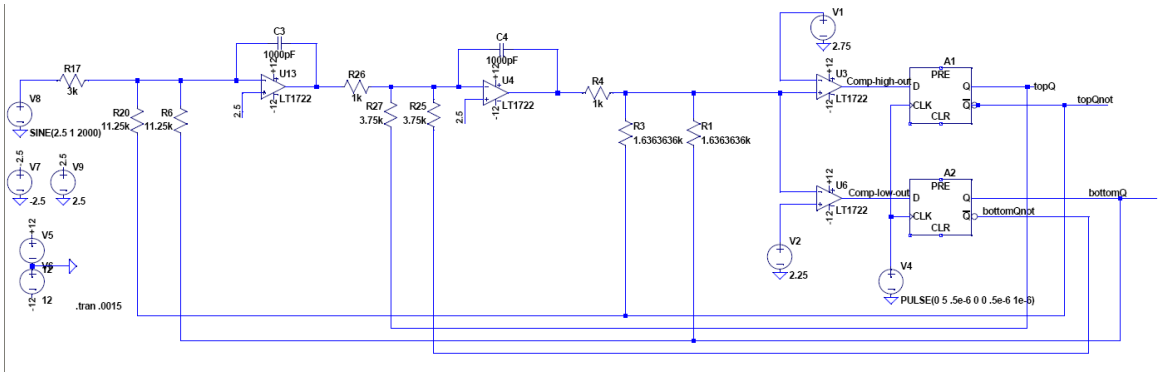

Figure 5.6: The final spice simulation of the second order delta sigma modulator.

Once the spice simulation was fully functional, the second order modulator was constructed on a bread-board, as per the simulation model. As with the first order modulator bread-board, the assembly involved ceramic capacitors and 5% resistors, LM356 op amps, and 74HC74A flip-flops. The only new component was the LF311 comparator, used for the three-level quantizer, as the first order modulator was a two-state system. The bread-boarded system was fully functional, providing the output shown in Figure 5.7. The success of the physical modulator indicated that it would be appropriate to include the second order modulator on the final full-system PCB.

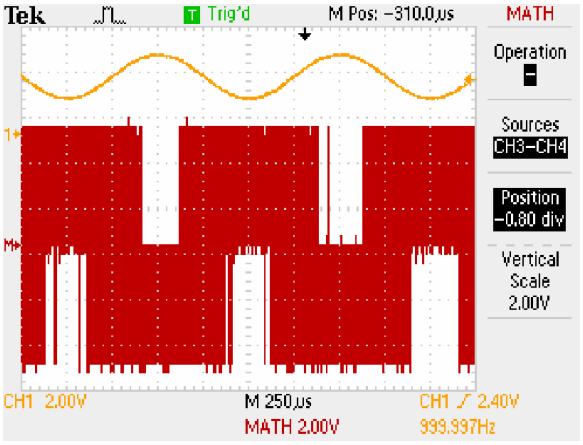

Figure 5.7: The output of the second order three-level modulator on a bread-board

5.1.3 Modulation Frequency

Once the second order, three-level modulator was realized, it was still necessary to choose the modulation frequency. There were three factors that played a role in this decision: the capabilities of the system, sound quality, and efficiency. The capabilities of the system had to be considered because the components in the modulator would have broken down at extremely high frequencies. Frequencies this high were never considered, however, so the limitations of the system did not prove to be a restriction on the modulation frequency.

The next two factors, sound quality and efficiency, had to be considered jointly because there were specifications to meet for both of them and there would prove to be a slight trade-off between them. The MOSFETs in the power stage were chosen for their efficiency. The efficiency was dependant on the switching frequency of the MOSFETs. As shown in Figure 3.4 the ideal switching frequency of the IRF6645 MOSFET was around 1MHz.

The sound quality, however, was unacceptable at 1MHz as demonstrated in Appendix L, so higher modulation frequencies were considered. Sound quality proved to meet the 90dB specification best at 5MHz because a higher modulation frequency pushes more noise out of the audio band. At 5MHz, it was also demonstrated that the efficiency specification could be met, as shown in Appendix K. Since there was not a notable difference in sound quality

between 5MHz and 10MHz and the efficiency was slightly better at 5MHz, that was chosen as the final modulation frequency of the system.

5.2 The Power Stage

The power stage did not have many problems since it was constructed entirely on a PCB. The only major change to the power stage was the addition of a larger bypass capacitor near the 40V rail and tantalum bypass capacitors right near the MOSFETs. This was because the MOSFETs failed consistently with only a small surface mount capacitor on the rail. The MOSFETs required dedicated bypass capacitors to store and receive energy from.

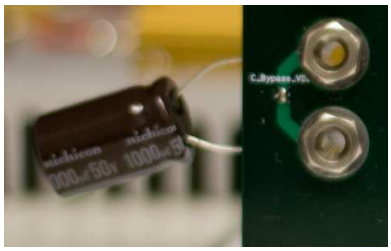

Figure 5.8: Addition of Electrolytic Bypass Capacitor at Rails

Figure 5.9: Addition of Tantalum Bypass Capacitor at MOSFET

5.3 Filter

The filter had some major unforeseen issues that needed to be resolved. First, the capacitors used in the original design produced undesired microphonics that added distortion to the

system. The choice of a 25 kHz cutoff frequency was also problematic because of non-idealities in the filter components. Finally, the configuration of the filter was changed to improve efficiency and cost.

5.3.1 Capacitor Microphonics

One problem was the issue of microphonics in the capacitors. The capacitors originally used for the filter were X7R surface mount capacitors. These are used in many applications because of their size and low equivalent series resistance (ESR), but they are subject to microphonics. This means that they emit audible noise at the frequency applied across the capacitor, so if there is a 1kHz sine wave that is large enough across the capacitor, a 1kHz tone will be heard. This will decrease the sound quality of the amplifier.

To correct this problem, research on different capacitor types was conducted. This was a very difficult decision to make because of the vast number of capacitor types. It was important to choose a capacitor that was free of significant microphonics but that still had a low ESR to make sure efficiency was still maintained. Polycarbonate film capacitors met these two specifications and were used in the final design.

5.3.2 Cut-Off Frequency

The frequency response, as shown in Figure 4.14, attenuated more than was desired within the audio band. This was a result of the fact that the filter used real components whose values had to be relatively common, so the cut-off frequency ended up being lower than desired. This was corrected by using a cut-off frequency of 30kHz instead of 25kHz. Increasing the cutoff frequency had a negligible impact on the performance of the amplifier and ensured there was no information lost within the audio band. Anything being developed on a commercial scale must, however, ensure a cutoff frequency of 30kHz is low enough to prevent Electromagnetic Interference (EMI) to meet Federal Communications Commission (FCC) requirements.

Changing the cut-off frequency necessarily changed the component values. The new value

for the inductor was determined to be $33\mu H$ using Table 3.2. The values for the capacitors will be discussed in Section 5.3.4.

5.3.3 New Inductors

In searching for new components for the filter, the Coilcraft DL1787 was found. This inductor improved the efficiency of the amplifier because it had a much lower resistance of 0.0028Ω. This inductor was also less expensive than the original.

5.3.4 Filter Configuration

The most significant change to the filter was the change in configuration. In the preliminary design there were two capacitors connected to ground from each end of the resistors (See Figure 5.10). It was determined that instead, there could be one capacitor across the resistor with half the value to give the same effect. This decreases both the losses and the cost of the filter. It was still essential, however, to have some capacitance connected to ground, but these were much less significant, allowing them to be one tenth the value of what the capacitors would have been in the old configuration. See Figure 5.11 for the new configuration.

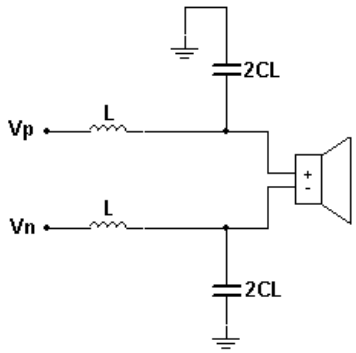

Figure 5.10: Preliminary Filter Design

The values, therefore, of the capacitors were finally calculated to be $C_L = .47\mu F$ and $C = .1\mu F$

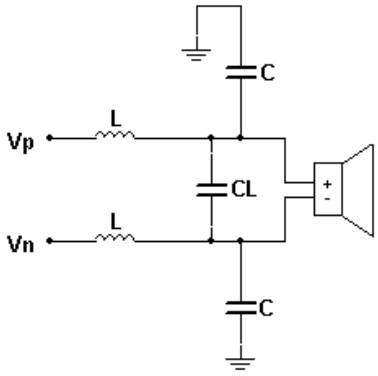

Figure 5.11: Final Filter Design

5.4 Final PCB Layout

Now that the final blocks were all designed, all that was left was to put it all together on one PCB layout. Since this was to be the final layout, size was a major factor in the design. Each stage was laid out with the smallest footprint possible. The final PCB, which included the modulator, power stage, filter, power receptacles and input and output receptacles measured 4.24 inches by 3.05 inches. This was a vast improvement over the previous PCB that was more twice that size and did not contain a modulator.

Another improvement to the final PCB was the addition of test points throughout the PCB. The board was laid out so that testing would be very easy for functionality, efficiency and signal quality. In addition to test points, jumpers and headers were included between stages, to allow for unit testing. In the preliminary design the modulator and power stage were separated and had to be connected to work together. This was beneficial because they could be tested independently of each other; it did, however, make the board a significantly larger. In the new design there were jumpers in between the modulator and power stage, as well as between the power stage and filter. Figure 5.12 shows the second revision of the PCB before it was assembled.

When the PCB arrived, the first section to be populated was the modulator. While performing functionality tests on the PCB modulator it was found the PCB layout contained

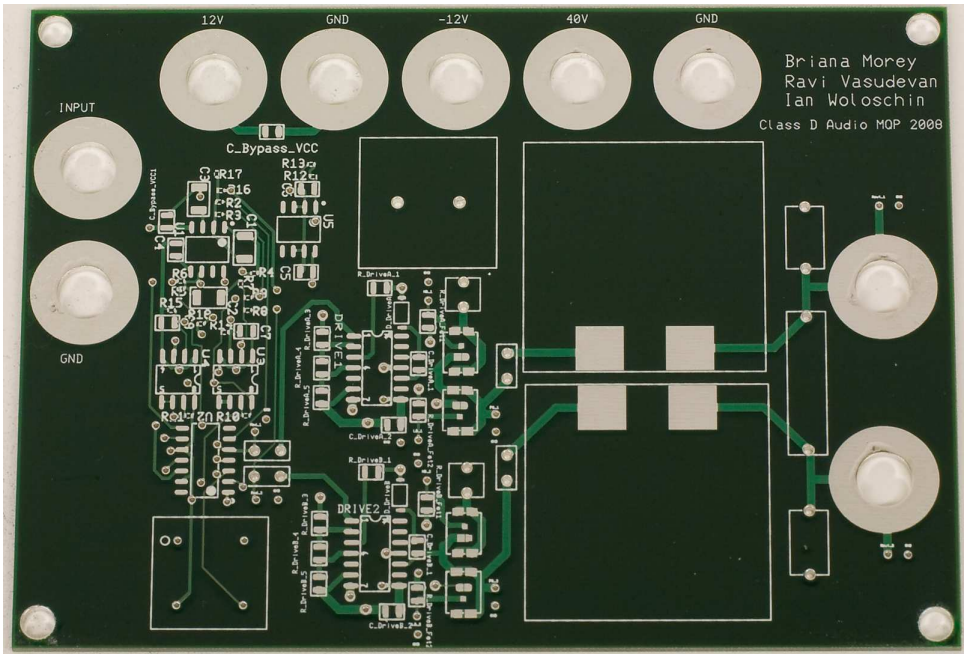

Figure 5.12: Unpopulated Second Revision Printed Circuit Board

errors in the modulator section. As the only effective way to fix the PCB would have been to order a third revision, a costly and time consuming endeavor, a decision was made to use the breadboard modulator for the project. This decision was reinforced by the fact that the PCB and breadboard modulator use identical components, save for resistor and capacitor tolerances. Figure 5.13 shows the second order, three-state, breadboard modulator used in the final design. Using the headers placed on the PCB to separate the various stages it was possible to connect the breadboard modulator to the power stage inputs on the PCB. Without these headers connecting the breadboard modulator to the power stage would have been much more difficult.

While the modulator was being tested, a separate PCB was populated with the power stage and filter. Functionality testing confirmed these two stages worked on the new PCB. Figure 5.14 shows the second revision PCB with the power stage and filter sections populated, as well as the input wires from the breadboard modulator to the power stage.

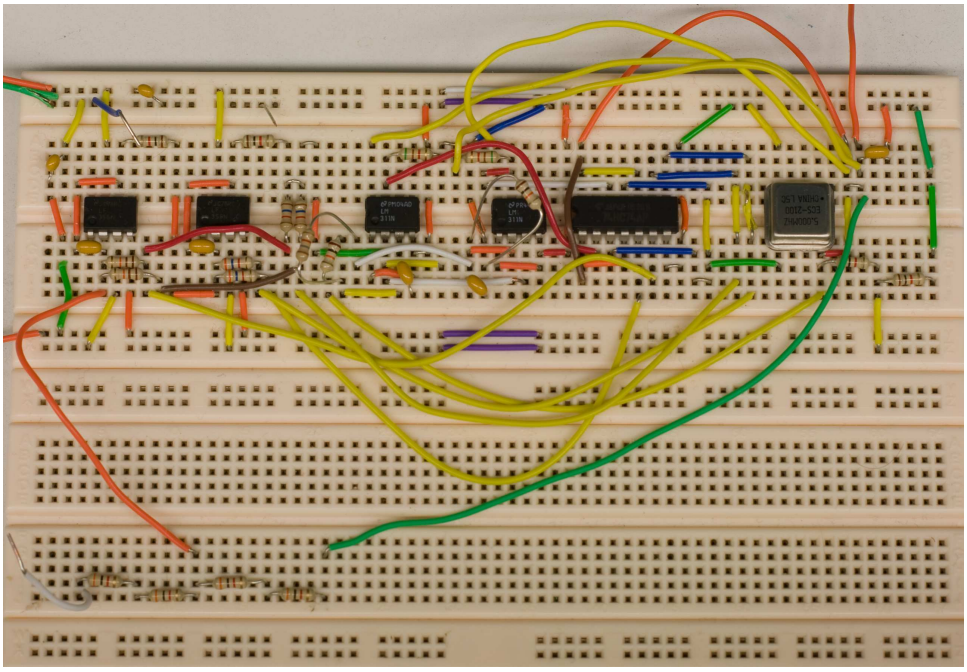

Figure 5.13: Second Order, Three State Breadboard $\Delta\Sigma$ Modulator

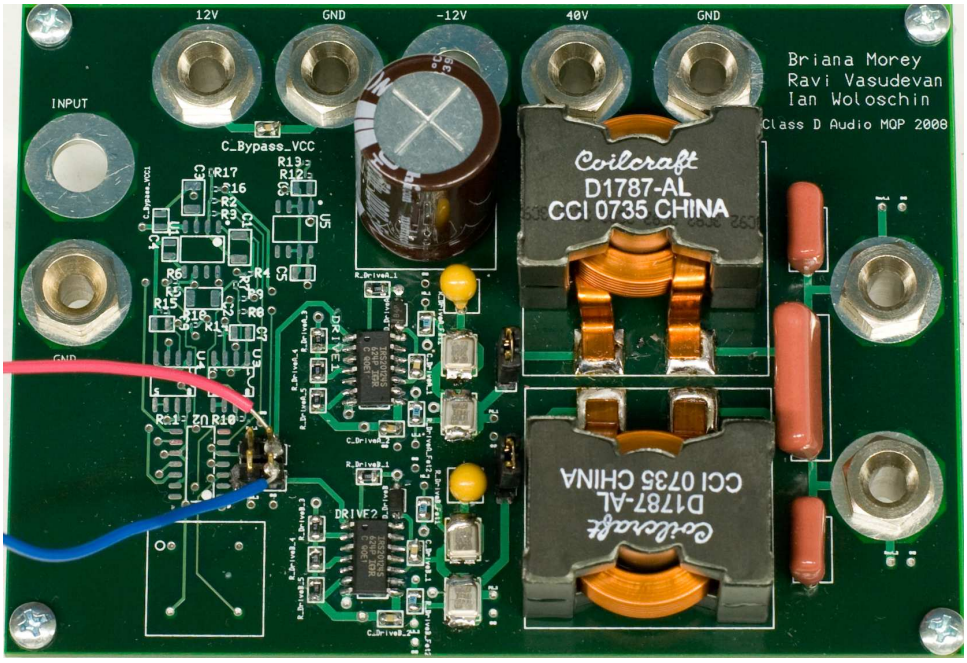

Figure 5.14: Populated Second Revision Printed Circuit Board

Chapter 6

Final Results

The following section provides an overview of the tests performed to ensure that the final design met the product specifications listed in Table 1.1. While this second testing procedure did include some of the functionality tests conducted in Chapter 4, it also included performance testing of the amplifier. The functionality testing was altered from the preliminary testing to account for the entire amplifier being on a single PCB. After the functionality testing, an efficiency test was conducted, as the purpose of a Class D amplifier is high efficiency. Finally, the signal quality was tested to ensure that the output signal was a higher power replica of the input signal. With the data provided by the testing, a quantitative analysis of the amplifier could be performed, the results of which can be found at the end of this chapter.

6.1 Functionality Test Results

The amplifier design was divided into three subsections: the modulator, the power stage, and the filter. The functionality testing was designed to thoroughly test each individual section and compare the actual results to the expected results. While one round of functionality testing had already been completed, a new PCB design necessitated retesting each component to ensure the new PCB did not contain any errors. Since the entire amplifier was on a single

PCB instead of discrete sections extra work was taken to provide a series of test points to isolate the three systems for testing.

6.1.1 Modulator

Similar to the first round of functionality testing, the modulator was the first component to be tested. The criteria used to judge the test was whether or not applying a standard audio test tone, a 1 kHz sine way, to the modulator would produce a modulated signal capable of being amplified by the power stage. The first step to performing this test involved a simple qualitative test: viewing a small sample of the modulator output and verifying that it was a modulated signal at the right levels, 0 to 5 V.

It was found that there were a number of errors on the PCB version of the modulator. Originally the modulator schematic was created as a single file and when that file was copied into the power stage file schematic to create one comprehensive PCB, there were some traces that were missing and went unseen. Because of time and money constraints, the modulator was constructed on a breadboard and the result was connected to the power stage.

After confirming that the modulator was generating a modulated signal at the right levels it could then be tested with the Power Stage to confirm the amplified signal resembled the input signal. As discussed in Section 5 the second revision of the modulator was a second order, three-state $\Delta\Sigma$ modulator, implying that were two outputs to monitor.

6.1.2 Power Stage

The power stage and filter were originally designed on a PCB because they contained several components that could only be purchased in surface mount packages. The layout was changed slightly for the second revision, however, as better components, like the new filter inductors, were found. This required that functionality testing be repeated to verify that the power stage still worked properly on the new PCB. Using two injection points it was possible to directly apply a square wave from a function generator to the power stage. A square wave

is unrealistic when compared to the expected modulator output, but it was a simple way to test the power stage independently of the modulator.

As with the first power stage test, the first point to test was the driver outputs, both low and high, to confirm that they were switching in sync with the driver input. The high side was expected follow the input, while the low side was expected to be inverted from the input. Once this was confirmed the next step was to test the MOSFET terminals. By viewing the voltage drop across the MOSFET terminals it was possible to determine whether the MOSFET was on, in the active region, or off, in the cutoff region. The MOSFETs were expected to switch in sync with the driver outputs, if the driver output was high, the MOSFET should have had approximately a 0 V drop across the terminals. If the driver output was low the MOSFET should have had 40 V across the terminals.

The final power stage was fully functional. It was able to amplify square waves applied to it.

6.1.3 Filter

The filter stage could only be tested after the power stage was working due to the balanced nature of the filter. The same test from Section 4.1.3 was performed, though the filter design had been slightly modified as described in Section 5.3. Again, a square wave was passed through the power stage into the filter, using an inverter to provide the proper signal to one driver. The frequency of the square wave was varied, from 20 Hz to 40 kHz. When the frequency was significantly below 30 kHz, enough that several harmonics were in the passband, a square wave was passed through the filter. When the frequency was increased so that harmonics were blocked by the filter the output began to look more like a sine wave. The final filter was functional. It had a fairly narrow passband and did filter out the modulated signals back to what was expected. See Section 6.3.4 for the final frequency response of the whole system.

6.2 Efficiency Results

In addition to functionality testing, some performance testing was required to quantitatively analyze the amplifier. The first performance testing conducted was the efficiency test, as a Class D amplifier should have a very high efficiency compared to other types of amplifiers. Efficiency is a measure of how much power going into a system passes through as useable power to the output, or conversely, how much power is not converted into waste heat in the system.

The efficiency of the system depends on a few different factors. The frequency of the input signal, the output power and the switching frequency of the system can all affect efficiency. Efficiency readings were recorded at 12 frequencies in the audio band: 20Hz, 50Hz, 100Hz, 200Hz, 500Hz, 1kHz, 2kHz, 5kHz, 10kHz, 12kHz, 15kHz and 20kHz. These were recorded at 4 different levels of output power: $40V_{pk}$ or full power, $30V_{pk}$, $20V_{pk}$ and $10V_{pk}$. All of these results were recorded at 4 different switching frequencies: 1MHz, 2MHz, 5MHz and 10MHz. All of this data is located in Appendix K.

The plot in Figure 6.1 shows the efficiencies for different signal frequencies. This data was recorded at full output power. The plot shows that the efficiency of the final system was above 90% at all of the clock frequencies tested while the system was at full output power. This plot also illustrates the impact of the modulation frequency on the efficiency of the system. The 1MHz modulation frequency was up to a few percentage points better in terms of efficiency but because of the noise produced it was not a viable option. The sound quality results are available in Section 6.3.

The plot in Figure 6.2 shows the efficiencies for different output levels. The efficiencies here are much higher at high output levels. This is because $\Delta\Sigma$ modulation requires a lot more switching to digitally simulate a signal at lower than full range. It is also interesting to note that on this plot, using a switching frequency of 1MHz is actually less efficient than the higher frequencies at an output level of $10V_{pk}$. This is due to the excess noise that is produced with a slower switching frequency that makes the 1MHz switching frequency

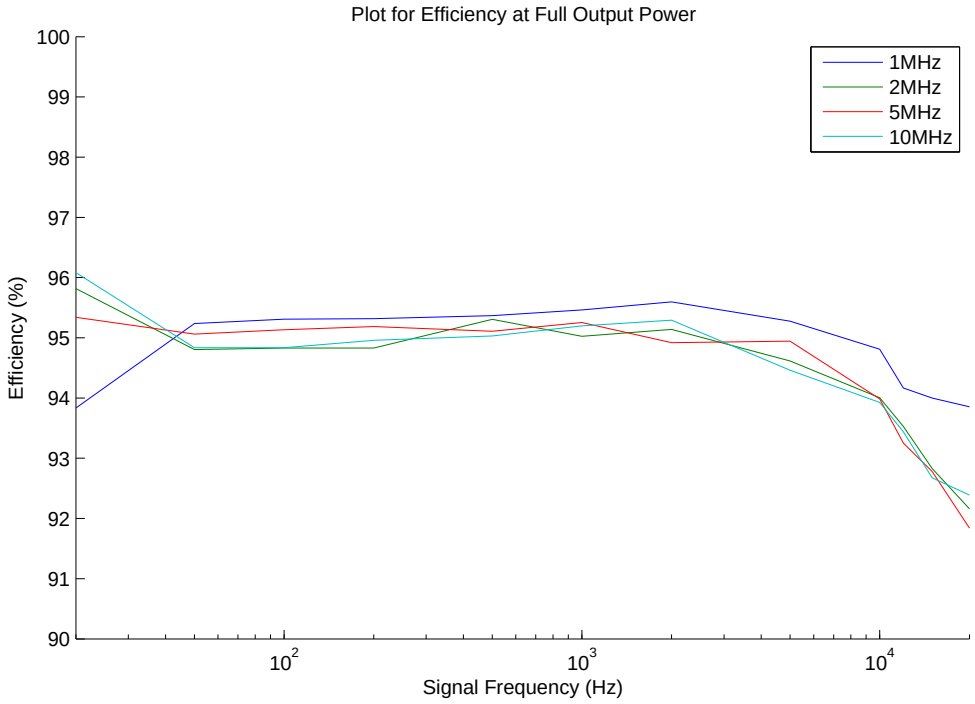

Figure 6.1: Plot of Efficiency vs. Signal Frequency

unusable.

These plots show that the specification of greater than 90% efficiency was met. In fact, within most of the audio band, the amplifier was able to produce efficiencies of greater than 95% which was far beyond the expectations of this project.

6.3 Sound Quality Results

Along with high efficiency the most important aspect of a Class D amplifier is the sound quality. To determine sound quality several tests were completed, both quantitative and qualitative. The quantitative tests looked at Total Harmonic Distortion (THD), Signal to Noise Ratio (SNR) and Frequency Response. These three specifications can describe how clean a signal is, or how free it is from unwanted noise. The qualitative test was a simple listening test, playing various well known, high quality music through the amplifier, and

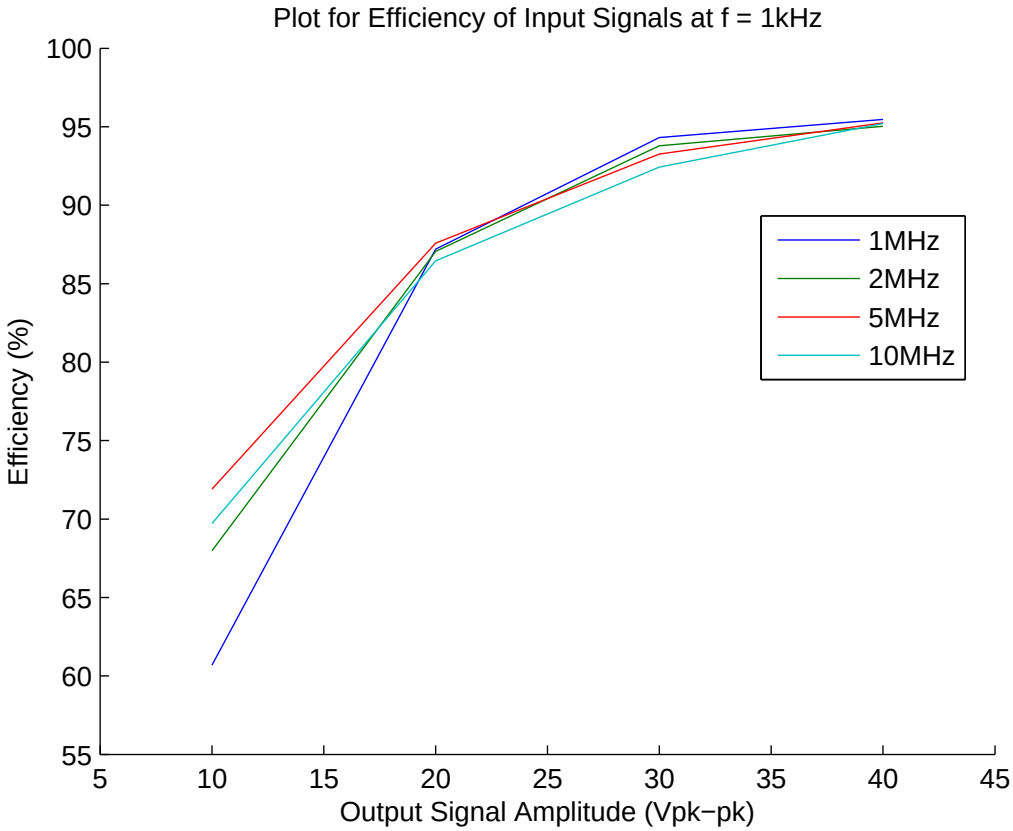

Figure 6.2: Plot of Efficiency vs. Output Peak Voltage

determining how the output sounds to the human ear.

The quantitative test was a combination of testing for THD, SNR and Frequency Response. In order to do this, a very high quality digital signal had to be recorded. This was done by generating a signal in MATLAB and using the E-MU 0202 USB sound card to apply it to the amplifier. The signal was scaled down using a voltage divider at the output of the amplifier and then recorded. Scaling the signal down was necessary because the sound card could not handle a $80V_{pk-pk}$ signal. The signal was both played to the sound card and recorded using Sonar ™. This was done because MATLAB could not record at 96kbps and 24-bit, whereas Sonar could. The wavefile of the recording was saved and cropped to avoid the transients at the beginning and end of the recording while still ensuring that it included an integer number of periods of the signal so that a proper Fast Fourier Transform (FFT) could be taken. Finally the wave files were opened with MATLAB and the resulting data was tested for sound quality.

6.3.1 Loopback Test

In order to determine that the test code functioned properly and that the sound card was good enough to use to test to the specifications outlined in Section 1.1, a loopback test was conducted. In a loopback test, the output is directly connected to the input of a sound card, and various test sounds waves are played and recorded. Then the THD, SNR and FR tests were conducted on the recordings. If the sound card had proved to have specifications that were not high enough to test for the specifications of this project then it would have been impossible to see if the amplifier met those specifcations. The plots in Figures L.1 and L.2 show the results of the loopback tests.

As these plots show, the THD for the loopback was well below 0.1% and the frequency response was well below 0.01dB and these values are good enough to calculate a THD of 1% and a frequency response of 3dB.

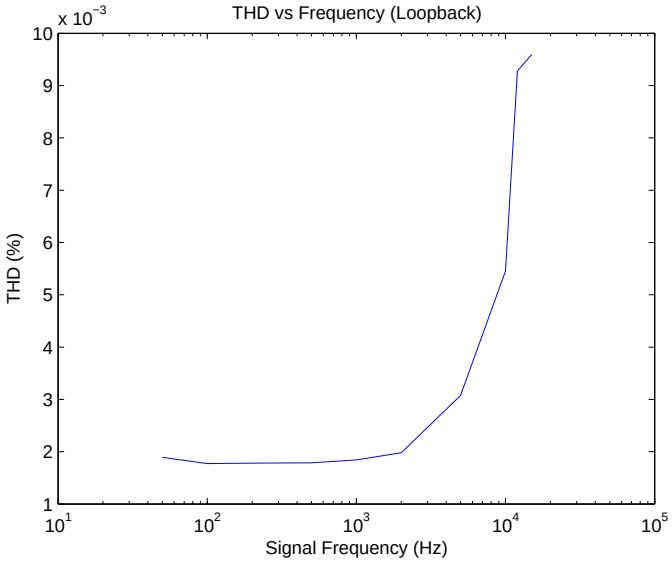

Figure 6.3: THD results for Loopback Test

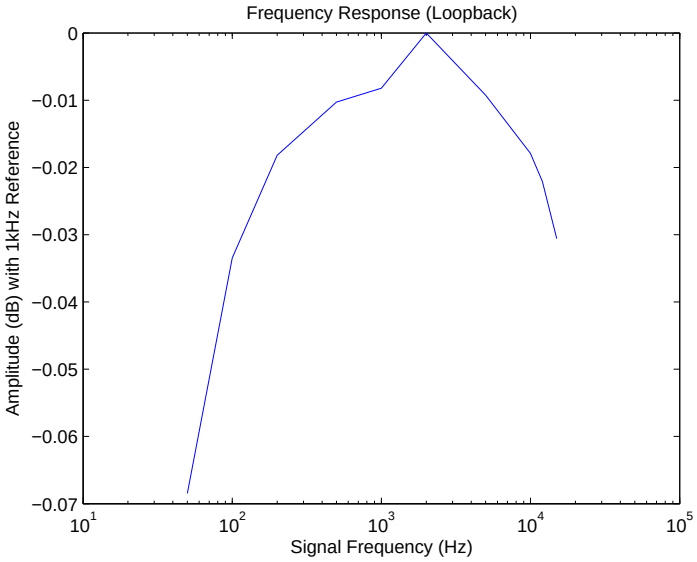

Figure 6.4: Frequency Response results for Loopback Test

6.3.2 Total Harmonic Distortion

One measure of the quality of an audio signal is the Total Harmonic Distortion (THD). THD is a relatively simple measurement, but can only be easily calculated under strict test conditions. As discussed in Section 2.4.1 THD is just the ratio between the desired fundamental frequency and all of the harmonics added together, though in practice only the first five harmonics have a significant impact on the measurement. The easiest way to calculate THD is to play pure audio tones because the output will be very easy to analyze. The Fast Fourier Transform (FFT) of the output will produce a frequency domain representation of the signal from which the fundamental and the first five harmonics can be calculated. Equation 6.1 can then be used to calculate THD:

$$\text{THD} = \frac{\sqrt{harm_1^2 + harm_2^2 + harm_3^2 + harm_4^2 + harm_5^2}}{fundamental} \cdot 100 \tag{6.1}$$

The code that was used to calculate THD from the wave files is located in Appendix I.

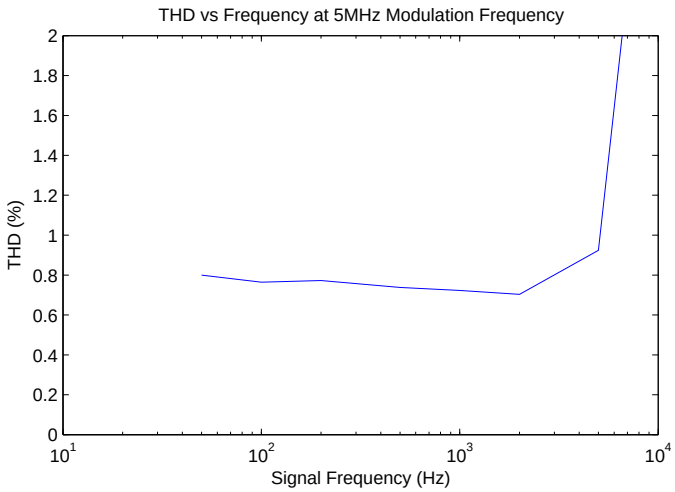

Figure 6.5: THD results at 5MHz clock frequency

As shown by the plot in Figure L.9 the THD was, for the most part, below 1%. This means that the amplifier met the specification. The only times where the result exceded the 1% barrier was at 20Hz and 20kHz. This was because the test equipment could not handle

extremely low frequencies and the signal was probably attenuated more than expected at 20kHz. This is a reasonable specification for the product because there is not a lot of sound at those frequencies.

6.3.3 Signal To Noise Ratio

Another important measure of audio quality is the Signal to Noise Ratio (SNR). Section 2.4.1 describes SNR in detail. SNR is important for high power devices because a device with a low SNR will create an audible "hiss" in the speakers. That hissing is actually the noise floor of the signal, meaning that is the quietest the signal can be. The equation for SNR is given in Equation 2.3. The code that was used to calculate SNR from the recorded wave files is located in Appendix I.

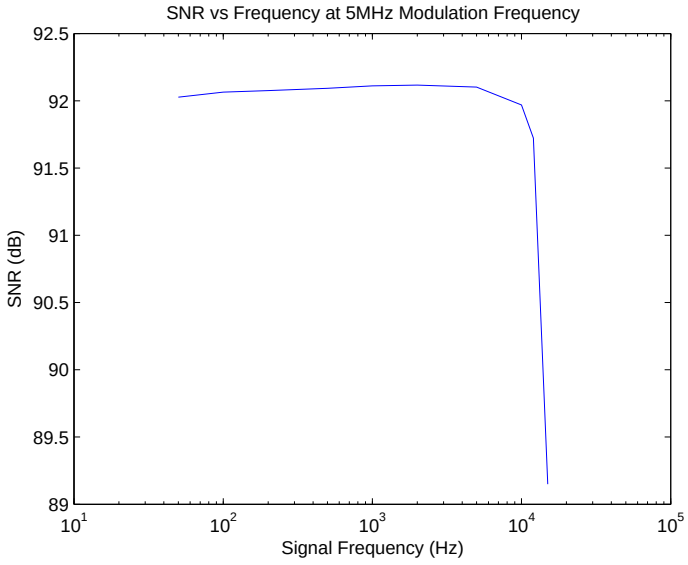

Figure 6.6: Plot of SNR vs. Frequency

The SNR was calculated by first recording a the output of the amplifier at each of the frequencies recorded for each of the other sound quality measurements. The signal power was derived from this recording. Then the output of the amplifier with no input was recorded. This allowed for the recording of the noise floor without a signal or harmonics to interfere.

The total power was summed over the audio band to develop the total noise power. The SNR was then calculated using Equation 2.3. Figure L.10 shows a plot of the SNR versus frequency.

These results indicate that the amplifier met the SNR specification, in that it was greater than 90dB, for most of the frequencies in the audio band. At the upper end of the frequency spectrum, around 20kHz, the SNR falls just below 90dB, but it is at a frequency that is difficult to hear and it only falls to 89dB. This is probably a result of the beginning of the cutoff of the filter. Further SNR plots are available in Appendix L.

6.3.4 Frequency Response

The final measure of audio quality is the frequency response. Frequency response is different from THD and SNR in that it is not measuring noise, but determining how flat the passband of the amplifier is. Ideally the amplifier will have a perfectly flat passband from 20 Hz to 20 kHz, though practical limitations may result in slight deviations. To the human ear these deviations will be manifested by different audio levels for different frequencies. As long as the deviations are within $\pm$1 dB a listener will generally not notice. Equation 4.5 can be used to calculate the frequency response.

The plot in Figure L.11 shows the frequency response. In this plot the gain at 1kHz is the 0dB reference and all other gains are the amount of dB outside of that reference. Up until 20kHz the response is definitely within 3dB of the 1kHz reference. However, at 20kHz the specification is not met. This is probably due to the response of the filter because of how inaccurate it is. This is okay, however, because there is not a lot of audio information at that high of a frequency since most people cannot hear that. Another interesting note about this result is that at 1MHz the frequency response goes higher at 20kHz and all the other clock frequencies result in the frequency response decreasing. This is another example of how the system developed does not work with a switching frequency of 1MHz.

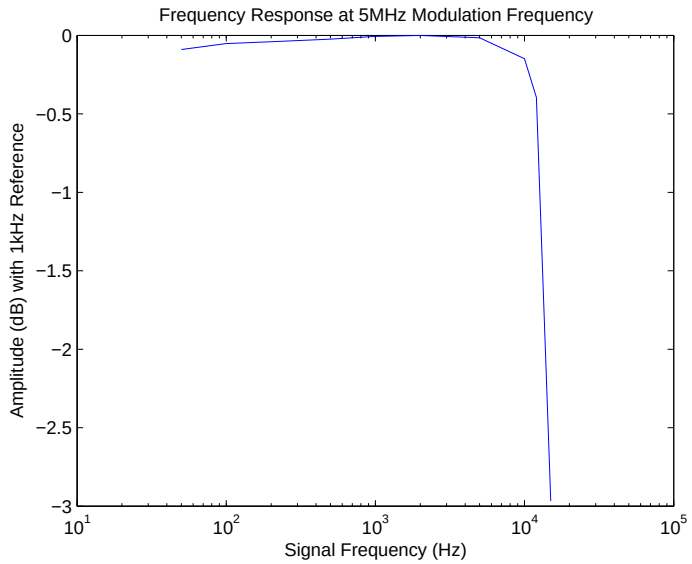

Figure 6.7: Plot of Efficiency vs. Output Peak Voltage

6.3.5 Listening Test

The listening test is a highly subjective test dependent upon the tester's musical ability. The purpose of this test is not to quantitatively identify problems, but instead to qualitatively pass or fail the amplifier design. While there is no specific song used in this test, the tester was encouraged to pick a song they knew well, one that they felt would be easy to find unwanted noise. This means that a "CD Quality" recording is needed, as poor quality audio recording will contain noticeable noise that may confuse the tester.

While playing the song through the amplifier, the tester must be sure to listen careful for any sort of static or noise. If noise is detected a note should be made of the approximate time in the audio track. If after several plays the same areas are determined to be noisy an FFT should be taken of the audio recording as well as the amplifier output at the same time. This will allow for a comparison to be made, and will help determine if the noise is inherent to the audio recording or being caused by the amplifier.

The amplifier was able to play music from a computer that "sounded good" to multiple testers. This qualitative measurement was important because the numbers and readings

mean nothing unless the amplifier actually functions correctly.

Chapter 7

Conclusion

The ultimate goal of this project was to design and build a fully functional Class D audio amplifier. Original project specifications included greater than 90% efficiency and less than 1% Total Harmonic Distortion (THD). Additonal project goals were 80 Watt Output Power and a Signal to Noise Ratio (SNR) of 90 dB. A test plan was also developed in order to determine if these goals and specifications were met and to determine if this project was successful.

The first step in accomplishing this project was to develop an understanding of how Class D amplifiers function. This was accomplished by researching past projects as well as commercial products. Once an understanding of Class D amplifiers was obtained several MATLAB simulations were created. These simulations allowed for various methods and components to be tested, ultimately saving valuable time and money in the final design.

After completing simulations the project shifted gears to begin developing working prototypes. The first stage completed was the power stage. The power stage was developed directly to a printed circuit board (PCB) because the MOSFETs used only came in surface mount packages, in order to maintain extremely high efficiencies. This did result in some complications as design flaws were more difficult to work around on a PCB as compared to a breadboard. The power stage PCB was ultimately a success, however, proving that the

project design and component choices worked. The first filter was developed alongside the power stage. This helped to minimize losses in output power by keeping power traces very short on the PCB, instead of requiring cabling to a separate board for the filter. The first power stage PCB was able to output an $80V_{pk-pk}$ signal, resulting in 80W power output to an 8Ω load.

While the power stage was being developed, a first order $\Delta\Sigma$ modulator was developed on a breadboard. This first order modulator was capable of modulating a signal, though it did not produce a high enough SNR to meet the project goal. The first order modulator proved extremely useful, however, for testing the power stage and filter to ensure that they could properly amplify a modulated signal. Using this first full system prototype the design of the amplifier was tested by performing various functionality tests. A full performance test was not completed, as simulations showed that this design would not meet the original project specifications.

Using test results from the prototype system and additional research a second order $\Delta\Sigma$ modulator was developed. A higher order modulator allowed for a higher SNR due to more control over where noise is generated. The switching frequency of the modulator was also increased, from 1 MHz to 5 MHz. This helped to push modulation noise well above the audio band, which was also instrumental in increasing the SNR of the amplifier without significantly reducing efficiency. While the second order modulator was developed work was done to slightly alter the filter. The filter was changed to a higher cutoff frequency, 30 kHz instead of 25 kHz, in an effort to increase efficiency and ensure the entire audio band is properly passed through the amplifier. The 30 kHz cutoff frequency was also decided upon by the inductor values found. The particular inductor used for the filter was both inexpensive and had an extremely low equivalent series resistance which was crucial in helping to minimize power loss in the system.

After the second order $\Delta\Sigma$ modulator was designed a second revision of the PCB was developed. In addition to having the modulator, power stage, and filter on one board, the

second revision PCB was significantly smaller than the first revision, which only had the power stage and filter. The smaller size was ideal for a production environment, as a smaller footprint may result in lower production costs. Unfortunately, the modulator on the second revision of the PCB had several issues which could not be resolved without ordering a new PCB, a costly and time consuming process. Due to the costs involved with ordering a new PCB, the decision was made to keep the second order modulator on a breadboard.

Finally, after confirming that the second revision system worked a series of performance testing was done to ensure the amplifier design met the original specifications. The performance testing was done using a high end computer sound card and MATLAB to generate test tones and record and analyze the system output. This setup allowed for semi-automated testing, by developing a MATLAB script to cycle through the frequencies of interest. The efficiency testing had to be performed by hand as measuring power in and power out required the use of an ammeter and two voltmeters, in addition to input test tones.

The result was that the amplifier met most of the specifications. The frequency response was well below 3dB for most of the audio band, THD was below 1%, SNR was around 92dB for most of the audio band and most importantly the efficiency was above 90%. In fact, the efficiency reached over 95% for almost all frequencies at full output power.

This project was successful. While there were several issues in the development of the final product, the end result was a working Class D audio amplifier that met the original project specifications. While the final design was not implemented completely on a single PCB, the completed layout shows how small a final production design of this amplifier could be. While the accomplishments of this project are significant, there are several areas of future research that were beyond the scope of the project.

Chapter 8

Future Work & Recommendations

While this project was successful in designing and implementing a fully functional Class D audio amplifier there are many additional areas that can be explored to complement the completed Class D audio amplifier. The focus of this project was to develop an amplifier to drive an 8Ω load. However, a working amplifier is a component that can be used in many different products, from guitar amplifiers to home theater receivers. This section will discuss several of the ideas for future work concerning Class D audio amplifiers.

8.1 High Efficiency Power Supply

While an amplifier can be thought of as simply a transistor that amplifies an input signal, a finished product is much more than that. While the major accomplishment of this MQP was a completed Class D audio amplifier, it was tied to the lab bench due to the need for a power supply. To be considered a finished commercial product an amplifier must have its own dedicated power supply, ideally one that can be plugged into a standard wall outlet or a high power battery. The power supply would have to provide several different voltage rails, ranging from 5 Volts to 40 Volts, for different parts of the modulator and power stage. Since the power supply would be for a Class D audio amplifier it would need to be an extremely high-efficiency power supply. Otherwise the efficiency of the entire system could

drop to unacceptable levels. Any work undertaken to develop such a power supply should also consider the power requirements of running multiple amplifiers in parallel. Many professional quality amplifiers offer 2 or 4 channels per amplifier unit, usually for stereo or surround sound systems. See Section 8.4 for further recommendations regarding multichannel amplifier units.

8.2 PCB Modulator with Full System Feedback

While this project did develop a fully working system, the final product was still a prototype design. One reason for this was that the modulator was never successfully assembled on a PCB due to complications with routing feedback lines, which are necessary for the modulator to run properly. Moving to a PCB may help reduce unwanted noise and increase the performance of the modulator. When moving to a PCB, full system feedback could be implemented. If the output of the amplifier were scaled and subtracted from the input, any noise or error introduced by the system could be compensated for, and the overall sound quality of the system would be improved. Full system feedback was not considered in this project because introducing another level of feedback to the modulator has the potential to destabilize the system. In addition, full system feedback could introduce more noise due to long cabling when not implemented directly on a PCB. A final complication that would need to be solved is the problem of delay. Within the modulator, the feedback delay is small enough that little to no effect is noticed, and the modulator functions within the specifications. With full system feedback, however, the delay would be increased significantly and could cause the feedback to decrease the sound quality rather than improve it.

8.3 Digital Input

Another area untouched by this project was the realm of digital audio signals. Currently, most live audio is generated, mixed, and amplified in the analog domain. However, many of the newer mixing consoles are digital. While these digital boards maintain analog inputs

and outputs, this is due to the analog nature of the devices they communicate with. Digital signals contain many advantages, from reduced Electromagnetic Interference (EMI) noise to being able to send multiple signals on one wire, or even wirelessly. A digital signal would not need to be modulated, but a parallel stage would be required to convert the digital signal so that it could be properly recognized and amplified by the power stage. Depending on the type of conversion used, there could be much less noise than would be generated by even a second order $\Delta\Sigma$ modulator.

In addition to the professional audio market, many home theater applications offer digital chains straight from the source material to the amplifier. The amplifier developed as a part of an MQP would be an ideal candidate for developing a high power, high efficiency home theater receiver. More information regarding digital audio is available in Appendix M.

8.4 Multichannel Systems

As previously discussed, the amplifier developed in this project is ideal for creating multichannel systems. This would be applicable to both professional and home audio. Professional audio amplifiers generally have either two or four channels per amplifier unit. This is because most sound systems are setup in symmetrical pairs, for left and right audio channels. However, many professional speakers contain multiple drivers, each powered by a single amplifier. Generally these systems use between two and four individually powered drivers per speaker, essentially placing multiple speakers in one cabinet. A quad channel amplifier unit, using the amplifier developed by this MQP, would allow for a small, but extremely powerful package to drive professional sound systems. Such a project would require an intensive signals portion, to provide proper crossovers for each channel, as well as to ensure that the gain of each channel is identical.

Developing a multichannel amplifier for home theater systems would have similar, but different issues. First, a replacement for the modulator would need to be designed to decode

the home theater audio signals, which are now usually in a digital format. Controls would need to be designed to adjust volume and equalize each channel independently, as well as all of the channels together. Research into current home theater systems would be needed to determine other features.

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Appendix A

First Order $\Delta\Sigma$ Modulation: MATLAB Simulation Code

The following is the code that was used to simulate first order delta sigma modulation prior to hardware construction.

```
% This function simulates first order delta sigma modulation without feedback.
% Its intended application is the Class D Audio Amplifier MQP, to be used with
% input signals in the audio band to assess noise and modulation techniques.

function output = dssim2(sigfreq, modfreq, simlength,C,R1,R2,Vqout,Vthres)

% Set sampling frequency
fs = modfreq*100;

% Create a basic sine wave
t = linspace(0,simlength-1/fs,fs*simlength);
f = sin(sigfreq*2*pi*t);
```

```
tqon=1/modfreq;

% Modulate!
bias = -max(f);
f=f+bias;
output = zeros(1,length(t));
dlatchstate = 0;
intvalue = Vthres-eps;
check = 0;
for i = 1:length(t)
    intvalue = intvalue - (1/(R1*C*fs))*f(i) - dlatchstate*(1/(R2*C*fs))*Vqout;
    if mod(i,100)==0
        if intvalue > Vthres
            dlatchstate=1;
        else
            check = check + dlatchstate;
            dlatchstate=0;
        end
    end
    output(i)=1-dlatchstate;
   end
check

%Plot fft
figure;
semilogx(linspace(0,fs,length(output)),20*log10(abs(fft(output))));
```

```
xlabel('Frequency (Hz)');
ylabel('Amplitude (dB)');
title('Delta Sigma Modulation');

sfft=abs(fft(output));
snrreg = sfft(11)/sum(sfft(15:floor(length(sfft)/2)));
dBsnr = 20*log10(snrreg);
```

Appendix B

MATLAB Script to Find 'a' Coefficients

The following script was used to determine a_1, a_2, and a_3, and was taken from Schreier's Understanding Delta-Sigma Data Converters [ST05].

```
%Desired NTF and its impulse response
NTF = zpk([1,1],[1,1]/3,1,1);
n_imp = 10;
y_desired = impL1(NTF,n_imp)');

% State-space description of CT loop filter
% as a 3-input, 1-output system
Ac = [0 0; 1 0 ];
Bc = [-1 0 0; 0 -1 0];
Cc = [0 1];
Dc = [0 0 -1];
td = 0.5;
sys_c = ss(Ac,Bc,Cc,Dc);
set(sys_c,'InputDelay',td*[1 1 1]);
```

```
%discrete-time equivalend and associated impulse repsonse
sy_d = c2d(sys_c,1)
yy = squeeze(impulse(sys_d,n_imp))';

%Solve for coefficients s.t. a*yy = y_desired
a = y_desired/yy;
```

Appendix C

First Order $\Delta\Sigma$ Modulation: MATLAB Simulation Code

```
% This function simulates second order delta sigma modulation.  Its
% intended application is the Class D Audio Amplifier MQP, to be used with
% input signals in the audio band to assess noise and modulation techniques.

function qoutput = secondorderdsm(sigfreq, modfreq, simlength)

% Set output pulsewidth and the reset voltage threshold for the d-latch and
% integrator
fs = modfreq*100;

%Create a basic sine wave
t = linspace(0,simlength-1/fs,fs*simlength);
f = sin(sigfreq*2*pi*t);
```

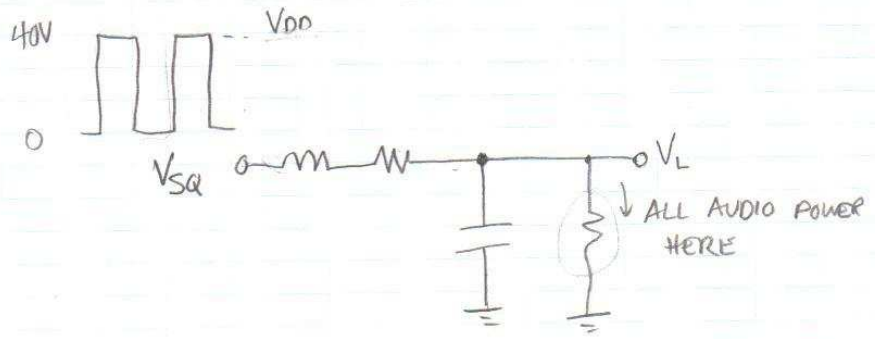
```
% insert test values
tqon=1/modfreq;
a1=4/9;
a2=1+3/9;
a3=11/18;
b1=1/3;
c1=modfreq;
c2=modfreq;

% Modulate!
qoutput = zeros(1,length(t));
c1output = zeros(1,length(t));
c2output = zeros(1,length(t));

T=1/fs;
qstate = 0;
c1value = 0;
c2value = 0;
check = 0;
for i = 1:length(t)
    c1value = c1value + (1/(fs))*(b1*f(i) - qstate*a1);
    c2value = c2value + (1/(fs))*(c1*c1value - qstate*a2);
    qin = c2value*c2 - a3*qstate;
    if mod(i,100)==0
        if qin > 0.5
            qstate = 1;
        elseif qin < -0.5
```

```
     qstate = -1;
        else
            qstate = 0;
        end
    end

    qoutput(i)=qstate;
    c1output(i)=c1*c1value;
    c2output(i)=c2*c2value;

end

plot(t,5*qoutput,'b',t,f,'r');
semilogx(linspace(0,fs,length(qoutput)),20*log10(abs(fft(qoutput))),'b');
xlabel('Frequency (Hz)');
ylabel('Amplitude (dB)');
title('Delta Sigma Modulation (System Model)');
max(20*log10(abs(fft(qoutput))))

end
```

Appendix D

MOSFET Equation Derivations

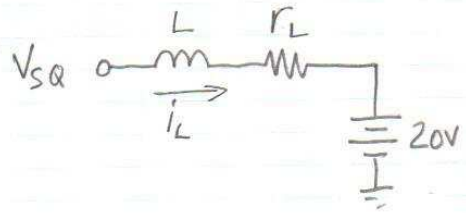
This appendix outlines the derivations for the equations in Section 3.2. These calculations were provided by Professor John McNeill.



ASSUMPTIONS: $Z_C \ll Z_L$ AT FREQ OF INTEREST
$< Z_R$

$\Rightarrow V_L$ CONSTANT 20V (AVG OF 50% DUTY CYCLE SQUARE WAVE)

REDRAW

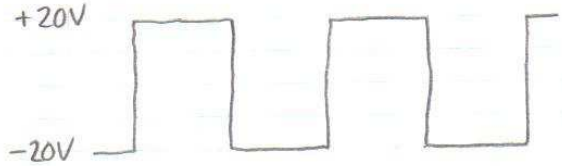


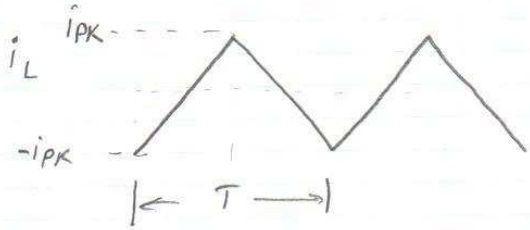
$r_L \ll Z_L$ AT FREQUENCIES OF INTEREST

$\Rightarrow$ TO DETERMINE i_L: IGNORE DROP ACROSS r_L

$$V = L\frac{di}{dt}$$

$$V_L = V_{SQ} - 20V$$





r_L LOSS DUE TO SIGNAL JUST FROM VOLTAGE DIVIDER

2 PROBLEMS:

a) WHAT IS i_{PK}

ii) WHAT IS THE AVG $i^2 r_L$ LOSS IN r_L

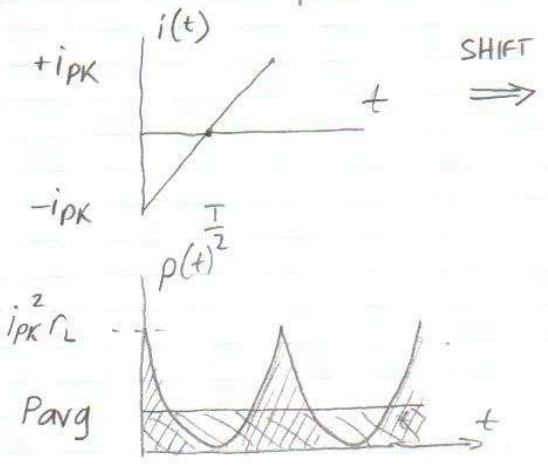
a) FOR i_{PK}

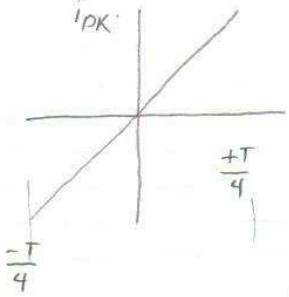
$$V = L\frac{di}{dt}$$

$$\frac{V_{DD}}{2} = L\frac{8\,i_{PK}}{T/2}$$

$$\boxed{i_{PK} = \frac{V_{DD}}{8Lf}}$$

ii) instantaneous power loss $i^2 r_L$





$$i(t) = 4\,i_{PK}\,\frac{t}{T}$$

CHECK
$t = 0 \Rightarrow 0$
$t = \frac{T}{4} \Rightarrow i_{PK}$

$$\underbrace{i^2(t)\,r_L}_{p(t)} = \frac{16\,i_{PK}^2\,r_L}{T^2}\,t^2$$

$$\int_{-\frac{T}{4}}^{\frac{T}{4}} p(t) = \frac{16}{3}\,\frac{i_{PK}^2\,r_L}{T^2}\,t^3 \Bigg|_{-\frac{T}{4}}^{\frac{T}{4}}$$

$$\frac{16}{3}\,\frac{i_{PK}^2 r_L}{T^2}\,\frac{T^3}{64} + -\frac{T^3}{64}$$

$$\frac{\cancel{16}\; i_{PK}^2 r_L\; \cancel{T^3}}{6\;\cancel{3}\;\cancel{T^2}\;\cancel{32}}\; T$$

THIS IS TOTAL LOSS IN HALF CYCLE
DIVIDE BY $\frac{T}{2}$ FOR AVERAGE POWE

$$P_{avg} = \frac{i_{PK}^2 r_L \cancel{T}\;\cancel{2}}{\cancel{6}3\;\cancel{T}} = \frac{i_{PK}^2 r_L}{3}$$

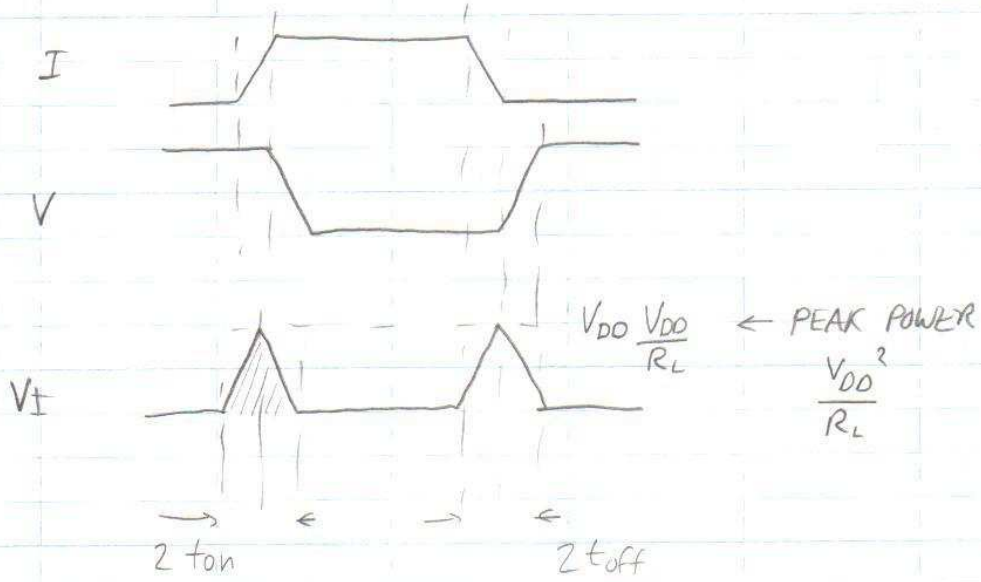
NOW SUB IN FOR i_{PK}

$$P_{avg} = \frac{V_{DD}^2 r_L}{64 L^2 f^2}\,\frac{}{3}$$

i_{PK}^2

$$\boxed{P_{avg} = \frac{V_{DD}^2 r_L}{192 L^2 f^2}}$$

FINITE SWITCHING TIME LOSS TERM



$t_{on}\frac{V_{DD}^2}{R_L}$ $t_{off}\frac{V_{DD}^2}{R_L}$

TOTAL ENERGY, 1 SWITCHING CYCLE

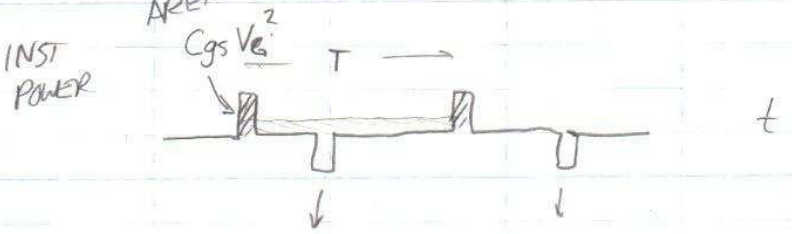
$$(t_{on}+t_{off})\frac{V_{DD}^2}{R_L}f$$

GATE CHARGE

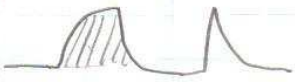
ENERGY ON GATE $C_{gs} V_G^2$
1 SWITCH CYCLE

POWER $f C_g V_G^2$

AREA $C_{gs} V_G^2$



$$\frac{C_{gs} V_G^2}{T} = f C_{gs} V_G^2$$



Appendix E

MOSFET Losses: MATLAB Simulation Code

This appendix contains the code used to determine the loss curves for a variety of MOSFETs.

```
figure;

%Range of Switching Frequencies
fSw = 40000:10:5000000;

vDrive = 20;

%Filter Values
rC = 0.01;
c = 36*10^-6;
rL = 0.01;
l = 0.56*10^-6;

%Other Values
```

```
rLoad = 4;
vPk = 40;
iOut = 5;

%MOSFET Values
hold all;

%IRF3805
rDS = 3.3*10^-3;
tOn = 150*10^-9;
tOff = 93*10^-9;
cGS = 7960*10^-12;

pInductor = (vPk.^2).*rL./(192.*(l.^2).*(fSw.^2));
pCapacitor = vPk.^2./(192.*(rLoad.^2).*rC.*(c.^2).*(fSw.^2));
pRDS = ones(size(fSw)).*rDS.*(iOut.^2);
pSwitch = (tOn + tOff).*(vPk./rLoad).*fSw;
pCgs = fSw.*cGS.*vDrive;

pTotal = pInductor + pCapacitor + pRDS + pSwitch + pCgs;

loglog(fSw, pTotal);

%IRF1010
rDS = 8.5*10^-3;
tOn = 90*10^-9;
tOff = 54*10^-9;
```

```
cGS = 2810*10^-12;

pInductor = (vPk.^2).*rL./(192.*(l.^2).*(fSw.^2));
pCapacitor = vPk.^2./(192.*(rLoad.^2).*rC.*(c.^2).*(fSw.^2));
pRDS = ones(size(fSw)).*rDS.*(iOut.^2);
pSwitch = (tOn + tOff).*(vPk./rLoad).*fSw;
pCgs = fSw.*cGS.*vDrive;

pTotal = pInductor + pCapacitor + pRDS + pSwitch + pCgs;

loglog(fSw, pTotal);

%IRF3808
rDS = 7*10^-3;
tOn = 140*10^-9;
tOff = 120*10^-9;
cGS = 5310*10^-12;

pInductor = (vPk.^2).*rL./(192.*(l.^2).*(fSw.^2));
pCapacitor = vPk.^2./(192.*(rLoad.^2).*rC.*(c.^2).*(fSw.^2));
pRDS = ones(size(fSw)).*rDS.*(iOut.^2);
pSwitch = (tOn + tOff).*(vPk./rLoad).*fSw;
pCgs = fSw.*cGS.*vDrive;

pTotal = pInductor + pCapacitor + pRDS + pSwitch + pCgs;

loglog(fSw, pTotal);
```

```
%IRF3205
rDS = 6.5*10^-3;
tOn = 95*10^-9;
tOff = 67*10^-9;
cGS = 3450*10^-12;

pInductor = (vPk.^2).*rL./(192.*(l.^2).*(fSw.^2));
pCapacitor = vPk.^2./(192.*(rLoad.^2).*rC.*(c.^2).*(fSw.^2));
pRDS = ones(size(fSw)).*rDS.*(iOut.^2);
pSwitch = (tOn + tOff).*(vPk./rLoad).*fSw;
pCgs = fSw.*cGS.*vDrive;

pTotal = pInductor + pCapacitor + pRDS + pSwitch + pCgs;

loglog(fSw, pTotal);

%IRF1405
rDS = 4.9*10^-3;
tOn = 110*10^-9;
tOff = 82*10^-9;
cGS = 4780*10^-12;

pInductor = (vPk.^2).*rL./(192.*(l.^2).*(fSw.^2));
pCapacitor = vPk.^2./(192.*(rLoad.^2).*rC.*(c.^2).*(fSw.^2));
pRDS = ones(size(fSw)).*rDS.*(iOut.^2);
pSwitch = (tOn + tOff).*(vPk./rLoad).*fSw;
```

```
pCgs = fSw.*cGS.*vDrive;

pTotal = pInductor + pCapacitor + pRDS + pSwitch + pCgs;

loglog(fSw, pTotal);

%IRF6645
rDS = 28*10^-3;
tOn = 5*10^-9;
tOff = 5.1*10^-9;
cGS = 890*10^-12;

pInductor = (vPk.^2).*rL./(192.*(l.^2).*(fSw.^2));
pCapacitor = vPk.^2./(192.*(rLoad.^2).*rC.*(c.^2).*(fSw.^2));
pRDS = ones(size(fSw)).*rDS.*(iOut.^2);
pSwitch = (tOn + tOff).*(vPk./rLoad).*fSw;
pCgs = fSw.*cGS.*vDrive;

pTotal = pInductor + pCapacitor + pRDS + pSwitch + pCgs;

loglog(fSw, pTotal);

%IRF6665
rDS = 53*10^-3;
tOn = 2.8*10^-9;
tOff = 4.3*10^-9;
cGS = 530*10^-12;
```

```
pInductor = (vPk.^2).*rL./(192.*(l.^2).*(fSw.^2));
pCapacitor = vPk.^2./(192.*(rLoad.^2).*rC.*(c.^2).*(fSw.^2));
pRDS = ones(size(fSw)).*rDS.*(iOut.^2);
pSwitch = (tOn + tOff).*(vPk./rLoad).*fSw;
pCgs = fSw.*cGS.*vDrive;

pTotal = pInductor + pCapacitor + pRDS + pSwitch + pCgs;

loglog(fSw, pTotal);

hold off;
```

Appendix F

MOSFET Data Sheet

This appendix contains the data sheet for the IRF6645, the MOSFET used in the power stage.

International
IOR Rectifier

PD - 97006

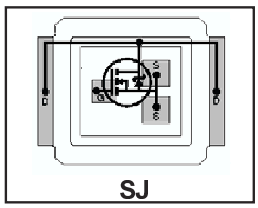
IRF6645

DirectFET™ Power MOSFET ②

- RoHs Compliant Containing No Lead and Bromide ①
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible ①
- Ultra Low Package Inductance
- Optimized for High Frequency Switching ①
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- Compatible with existing Surface Mount Techniques ①

Typical values (unless otherwise specified)

V_{DSS}	V_{GS}	$R_{DS(on)}$
100V max	±20V max	28mΩ@ 10V
$Q_{g\ tot}$	Q_{gd}	$V_{gs(th)}$
14nC	4.8nC	4.0V


SJ


DirectFET™ ISOMETRIC

Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SH	SJ	SP		MZ	MN					

Description

The IRF6645 combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of an Micro8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6645 is optimized for primary side bridge topologies in isolated DC-DC applications, for wide range universal input Telecom applications (36V - 75V), and for secondary side synchronous rectification in regulated DC-DC topologies. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance isolated DC-DC converters.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V ③	5.7	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V ③	4.5	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V ④	25	
I_{DM}	Pulsed Drain Current ⑤	45	
E_{AS}	Single Pulse Avalanche Energy ⑥	29	mJ
I_{AR}	Avalanche Current ⑤	3.4	A

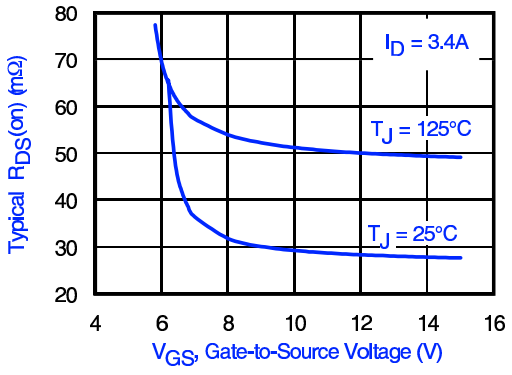


Fig 1. Typical On-Resistance vs. Gate Voltage

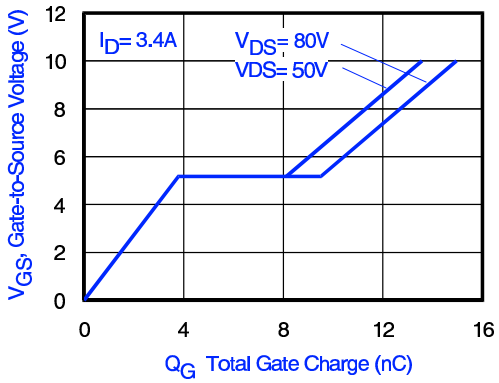


Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

Notes:

① Click on this section to link to the appropriate technical paper.

② Click on this section to link to the DirectFET Website.

③ Surface mounted on 1 in. square Cu board, steady state.

④ T_C measured with thermocouple mounted to top (Drain) of part.

⑤ Repetitive rating; pulse width limited by max. junction temperature.

⑥ Starting T_J = 25°C, L = 5.0mH, R_G = 25Ω, I_{AS} = 3.4A.

Absolute Maximum Ratings

	Parameter	Max.	Units
P_D @T_A = 25°C	Power Dissipation ①	3.0	W
P_D @T_A = 70°C	Power Dissipation ①	1.4	
P_D @T_C = 25°C	Power Dissipation ④	42	
T_P	Peak Soldering Temperature	270	°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 150	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ①⑤	—	58	°C/W
$R_{\theta JA}$	Junction-to-Ambient ②⑤	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ③⑤	20	—	
$R_{\theta JC}$	Junction-to-Case ④⑤	—	3.0	
$R_{\theta J\text{-}PCB}$	Junction-to-PCB Mounted	1.0	—	

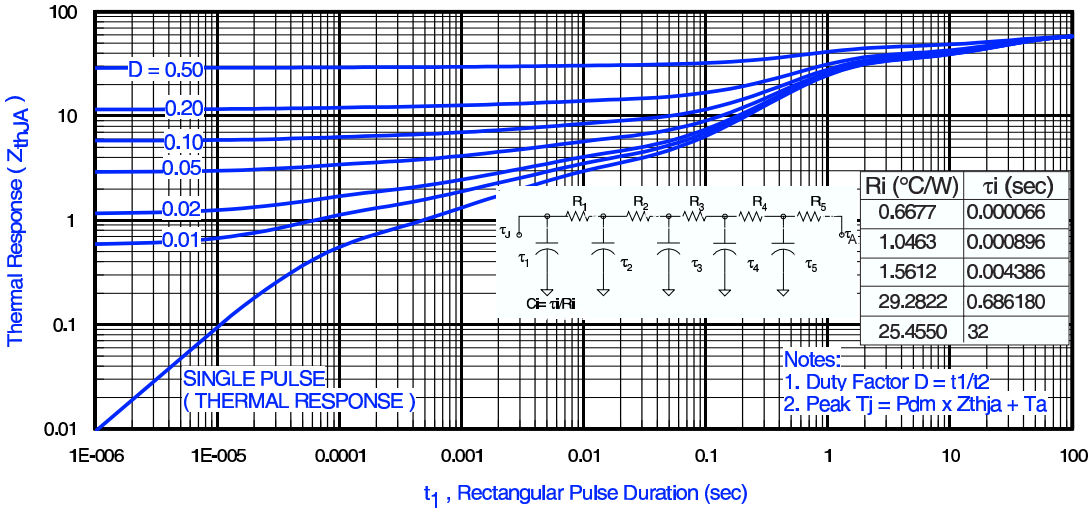


Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ①

Notes:

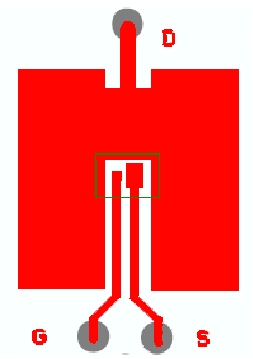
① Surface mounted on 1 in. square Cu, steady state.

② Used double sided cooling , mounting pad.

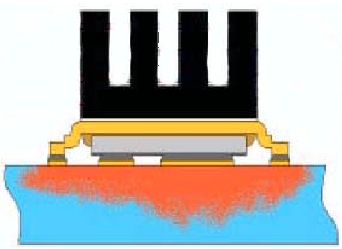
③ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.

④ T_C measured with thermocouple incontact with top (Drain) of part.

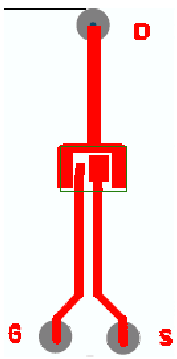
⑤ R_θ is measured at T_J of approximately 90°C.



① Surface mounted on 1 in. square Cu board (still air).



③ Mounted to a PCB with small clip heatsink (still air)



③ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

Absolute Maximum Ratings

	Parameter	Max.	Units
P_D @T_A = 25°C	Power Dissipation ①	3.0	W
P_D @T_A = 70°C	Power Dissipation ①	1.4	
P_D @T_C = 25°C	Power Dissipation ④	42	
T_P	Peak Soldering Temperature	270	°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 150	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ①⑤	—	58	°C/W
$R_{\theta JA}$	Junction-to-Ambient ②⑤	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ③⑤	20	—	
$R_{\theta JC}$	Junction-to-Case ④⑤	—	3.0	
$R_{\theta J\text{-}PCB}$	Junction-to-PCB Mounted	1.0	—	

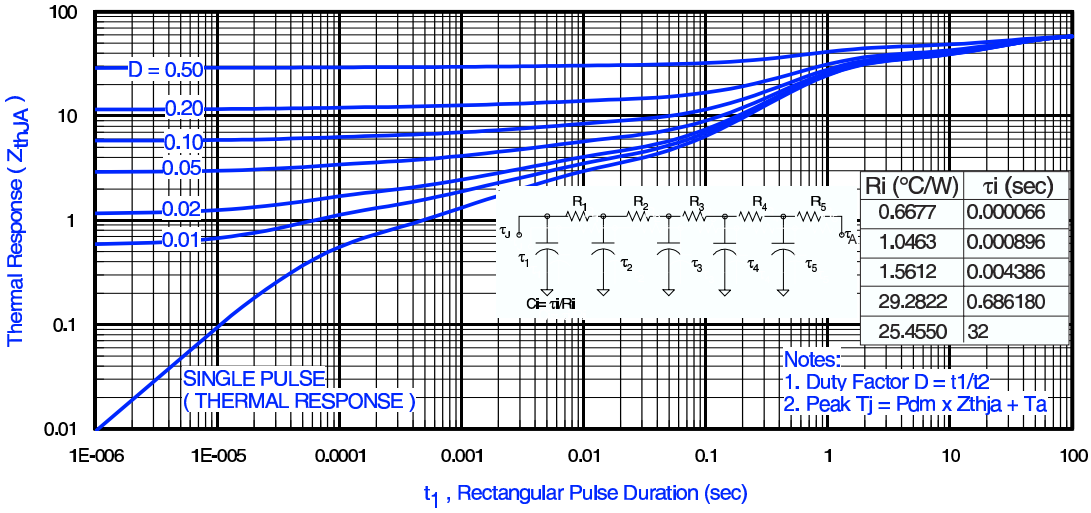


Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ①

Notes:

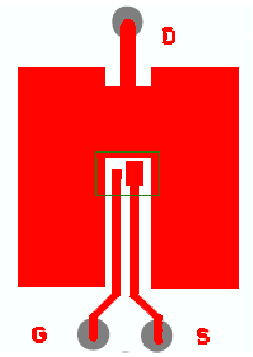
① Surface mounted on 1 in. square Cu, steady state.

② Used double sided cooling , mounting pad.

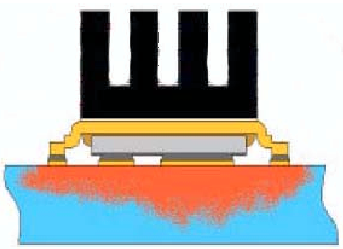
③ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.

④ T_C measured with thermocouple incontact with top (Drain) of part.

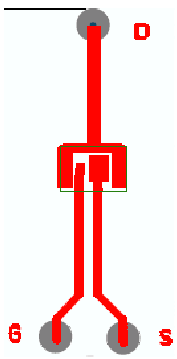
⑤ R_θ is measured at T_J of approximately 90°C.



① Surface mounted on 1 in. square Cu board (still air).



③ Mounted to a PCB with small clip heatsink (still air)



③ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

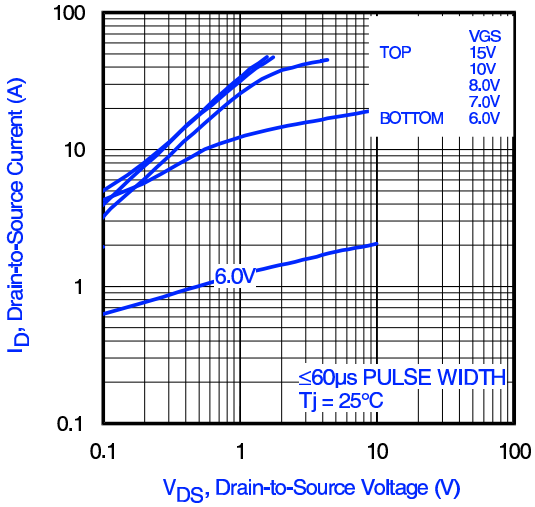


Fig 4. Typical Output Characteristics

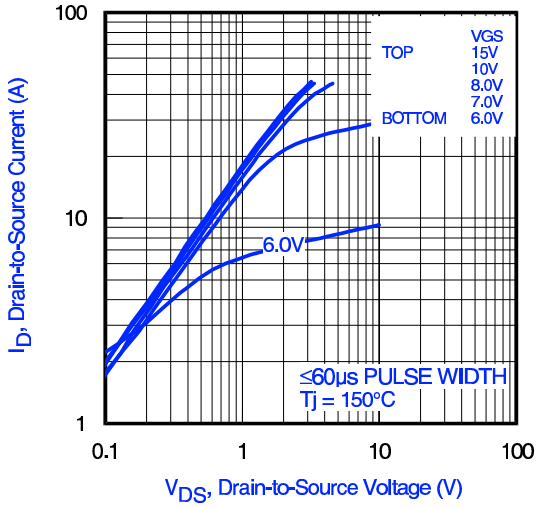


Fig 5. Typical Output Characteristics

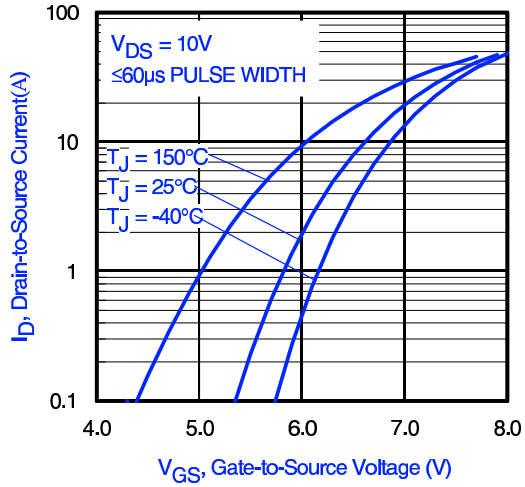


Fig 6. Typical Transfer Characteristics

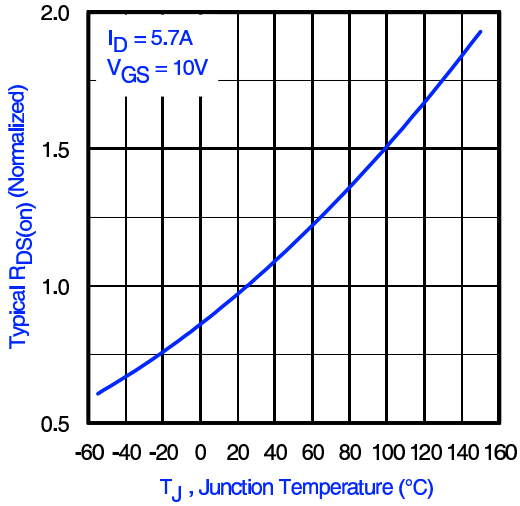


Fig 7. Normalized On-Resistance vs. Temperature

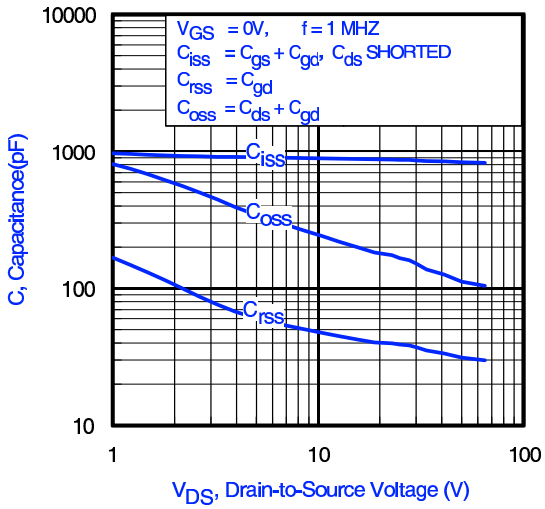


Fig 8. Typical Capacitance vs.Drain-to-Source Voltage

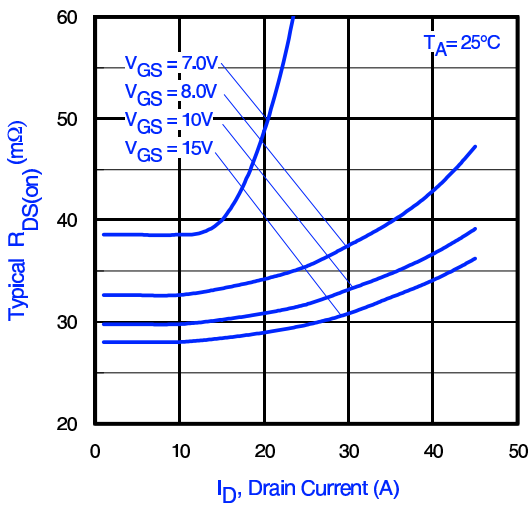


Fig 9. Typical On-Resistance vs. Drain Current

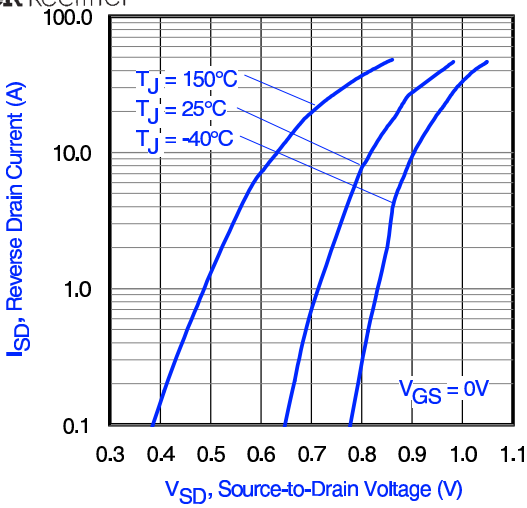


Fig 10. Typical Source-Drain Diode Forward Voltage

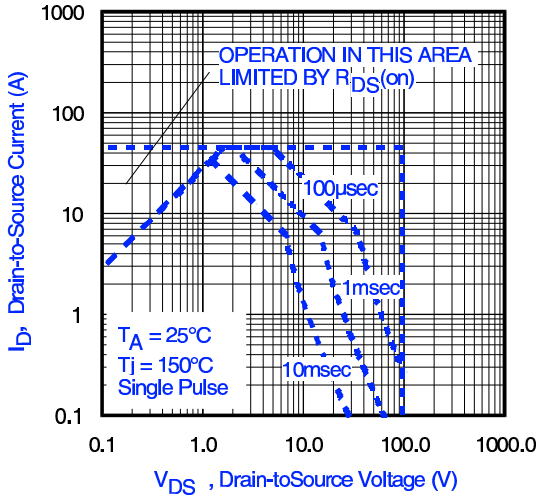


Fig11. Maximum Safe Operating Area

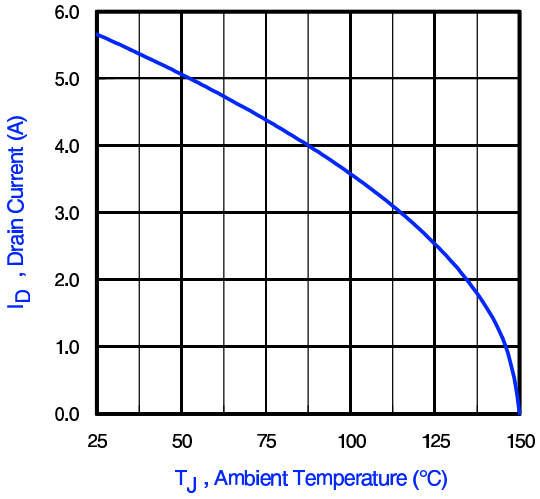


Fig 12. Maximum Drain Current vs. Ambient Temperature

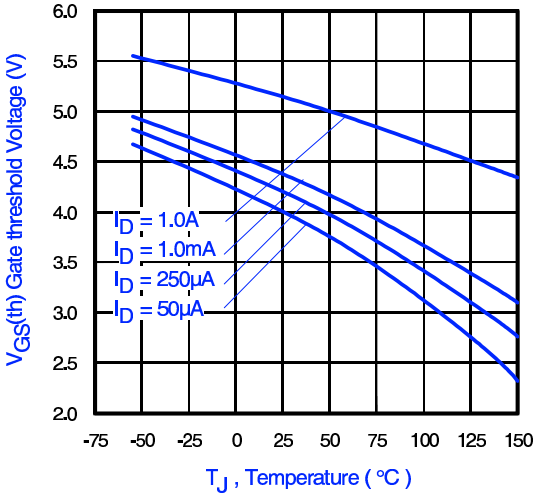


Fig 13. Typical Threshold Voltage vs. Junction Temperature

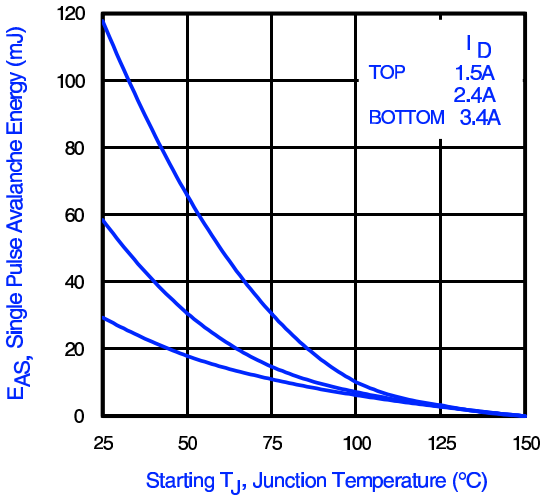


Fig 14. Maximum Avalanche Energy vs. Drain Current

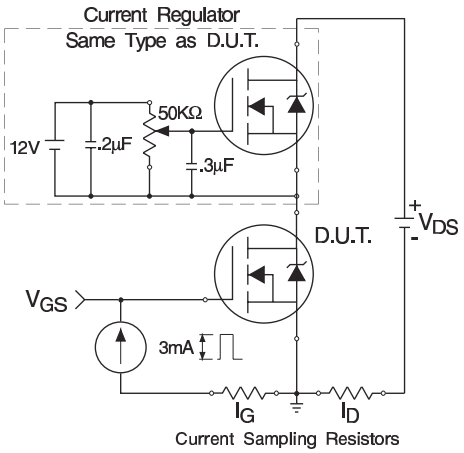


Fig 15a. Gate Charge Test Circuit

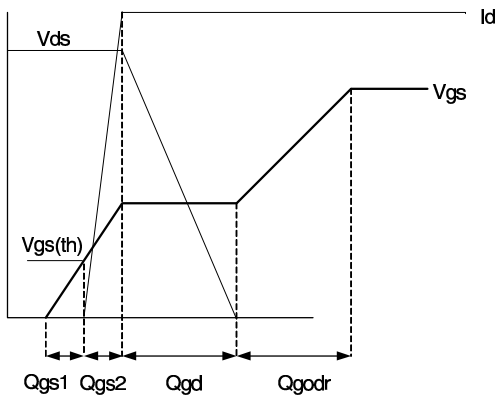


Fig 15b. Gate Charge Waveform

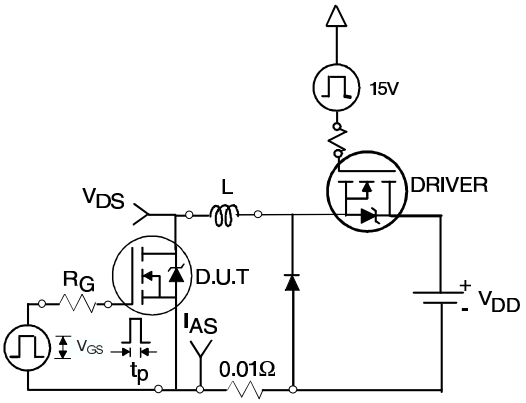


Fig 16b. Unclamped Inductive Test Circuit

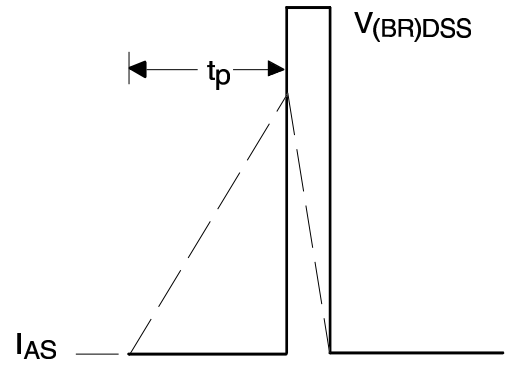


Fig 16c. Unclamped Inductive Waveforms

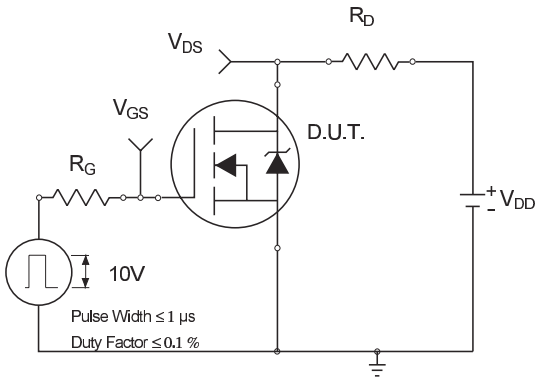


Fig 17a. Switching Time Test Circuit

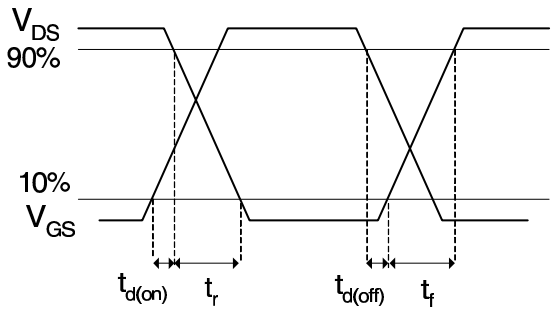


Fig 17b. Switching Time Waveforms

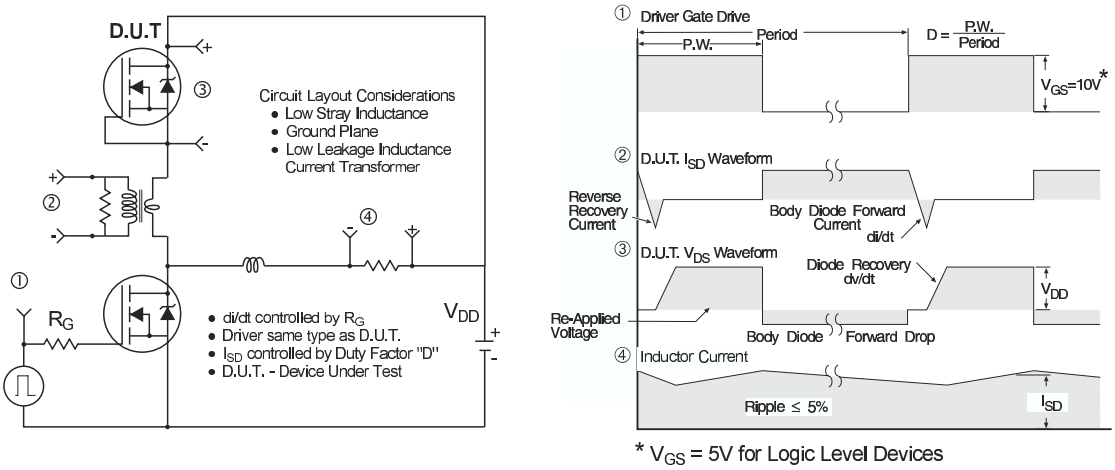
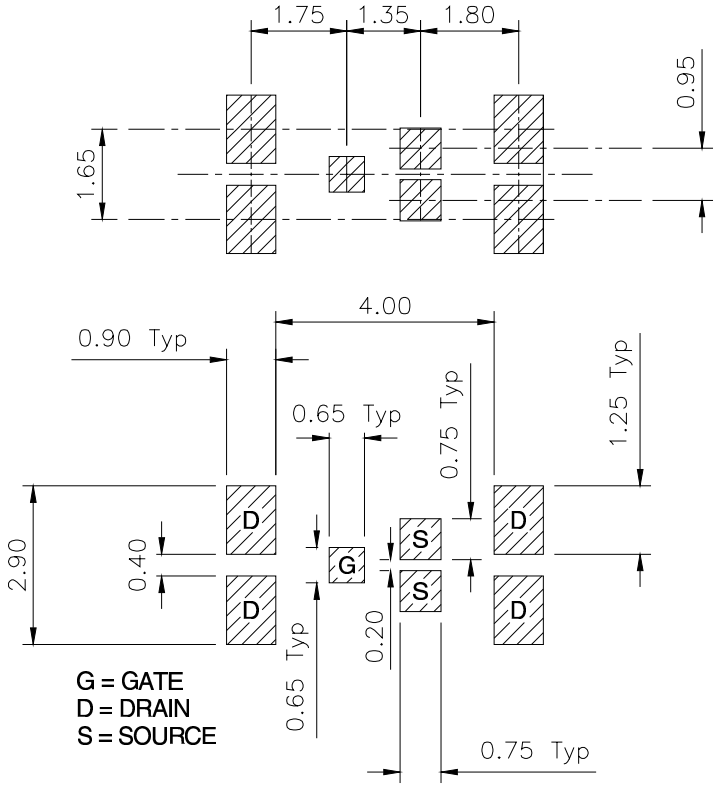


Fig 18. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

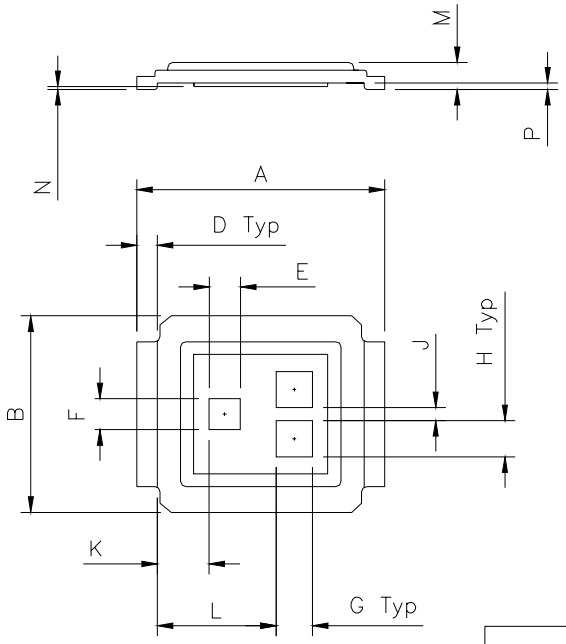
DirectFET™ Substrate and PCB Layout, SJ Outline (Small Size Can, J-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



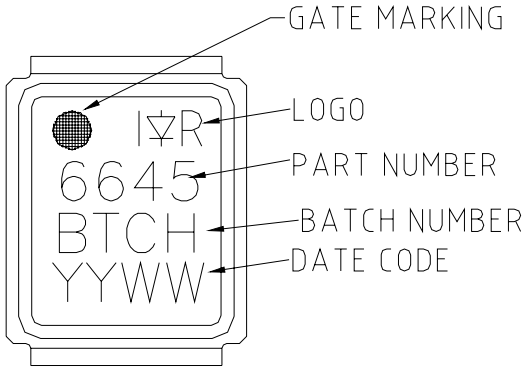
DirectFET™ Outline Dimension, SJ Outline (Small Size Can, J-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.
This includes all recommendations for stencil and substrate designs.

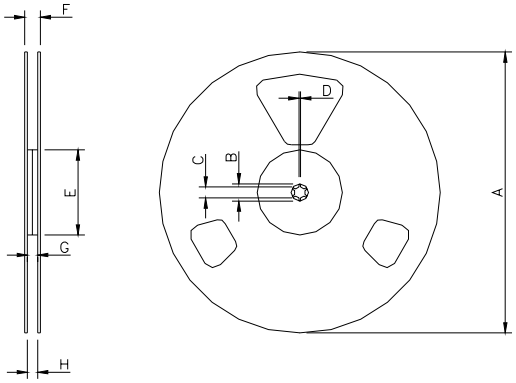


DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	4.75	4.85	0.187	0.191
B	3.70	3.95	0.146	0.156
C	2.75	2.85	0.108	0.112
D	0.35	0.45	0.014	0.018
E	0.58	0.62	0.023	0.024
F	0.58	0.62	0.023	0.024
G	0.68	0.72	0.027	0.028
H	0.68	0.72	0.027	0.028
K	0.98	1.02	0.039	0.040
L	2.28	2.32	0.090	0.091
M	0.48	0.58	0.019	0.023
N	0.03	0.08	0.001	0.003
P	0.08	0.17	0.003	0.007

DirectFET™ Part Marking

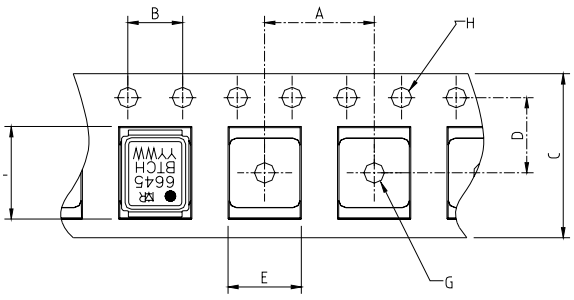


DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6645). For 1000 parts on 7" reel, order IRF6645TR1

REEL DIMENSIONS								
STANDARD OPTION (QTY 4800)					TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C



NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
	MIN	MAX		MAX
	7.90	8.10		0.319
	3.90	4.10		0.161
	11.90	12.30		0.484
	5.45	5.55		0.219
	4.00	4.20		0.165
	5.00	5.20		0.205
	1.50	N.C		N.C
	1.50	1.60		0.063

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Appendix G

Preliminary Schematic

The schematic shown in Figure G.1 represents a preliminary system design.

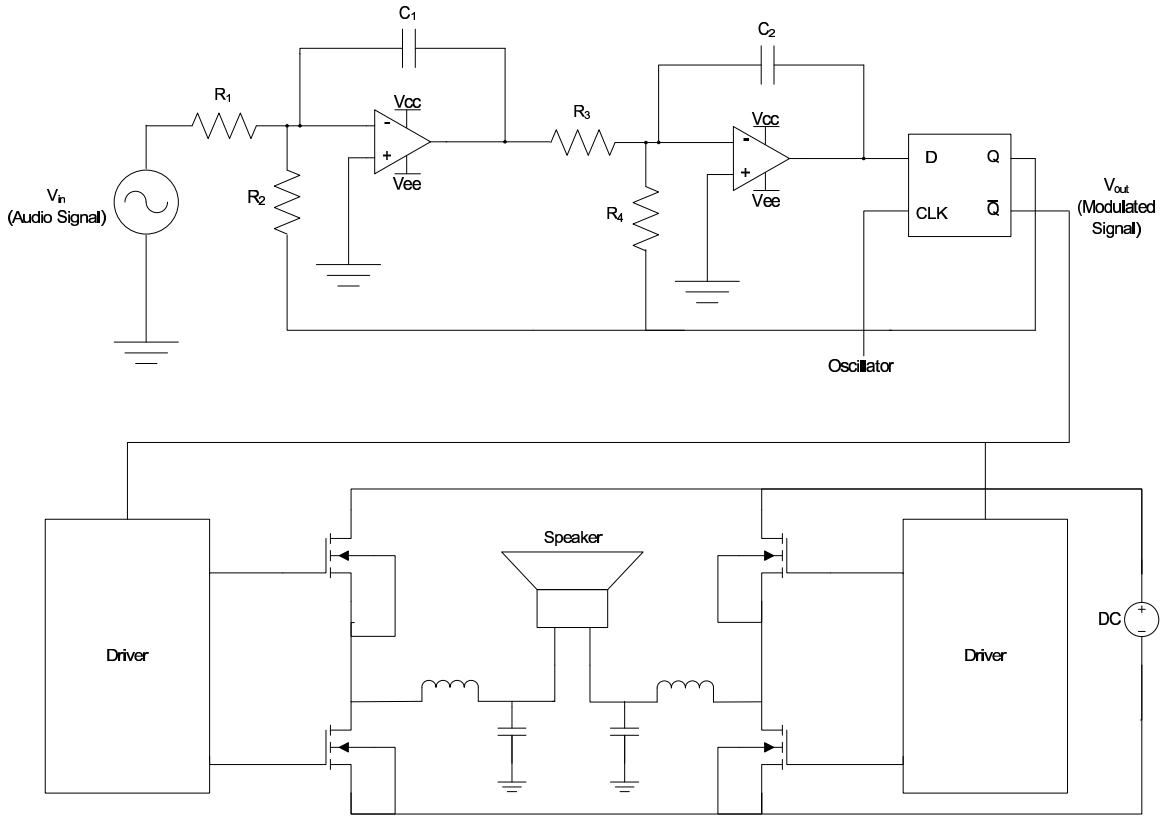

Figure G.1: A preliminary schematic

Appendix H

Final Schematics

The following appendix gives the schematics for the preliminary design and the final design.

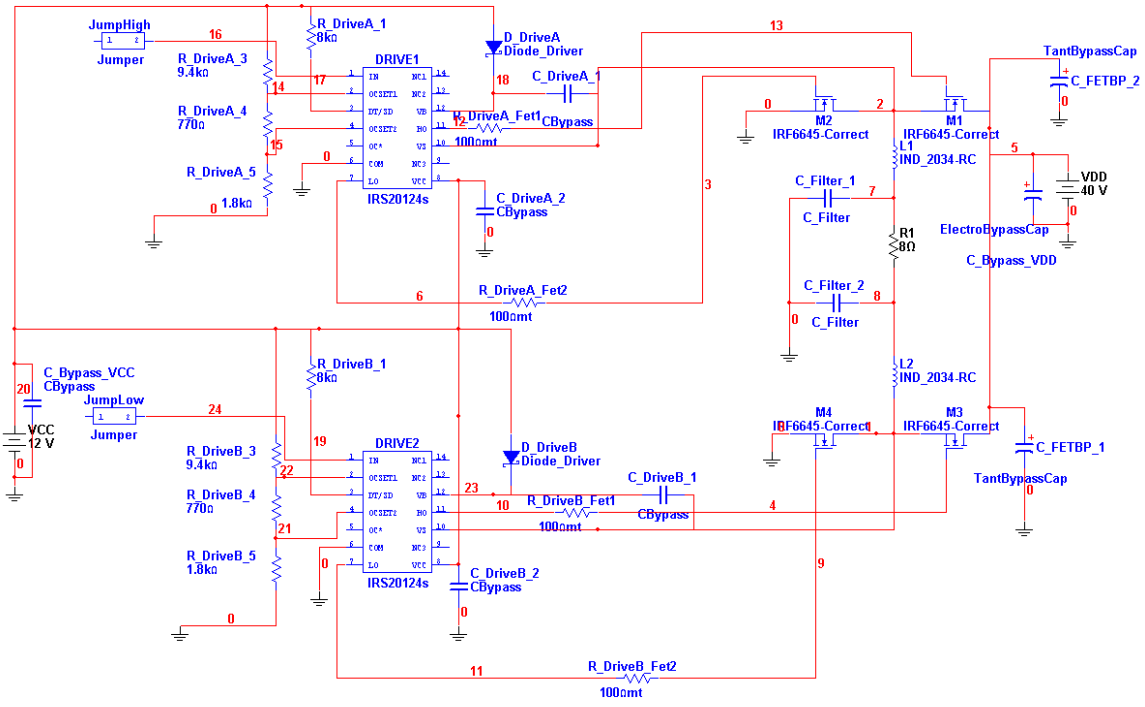

Figure H.1: Preliminary Schematic of the Power and Filter Stages

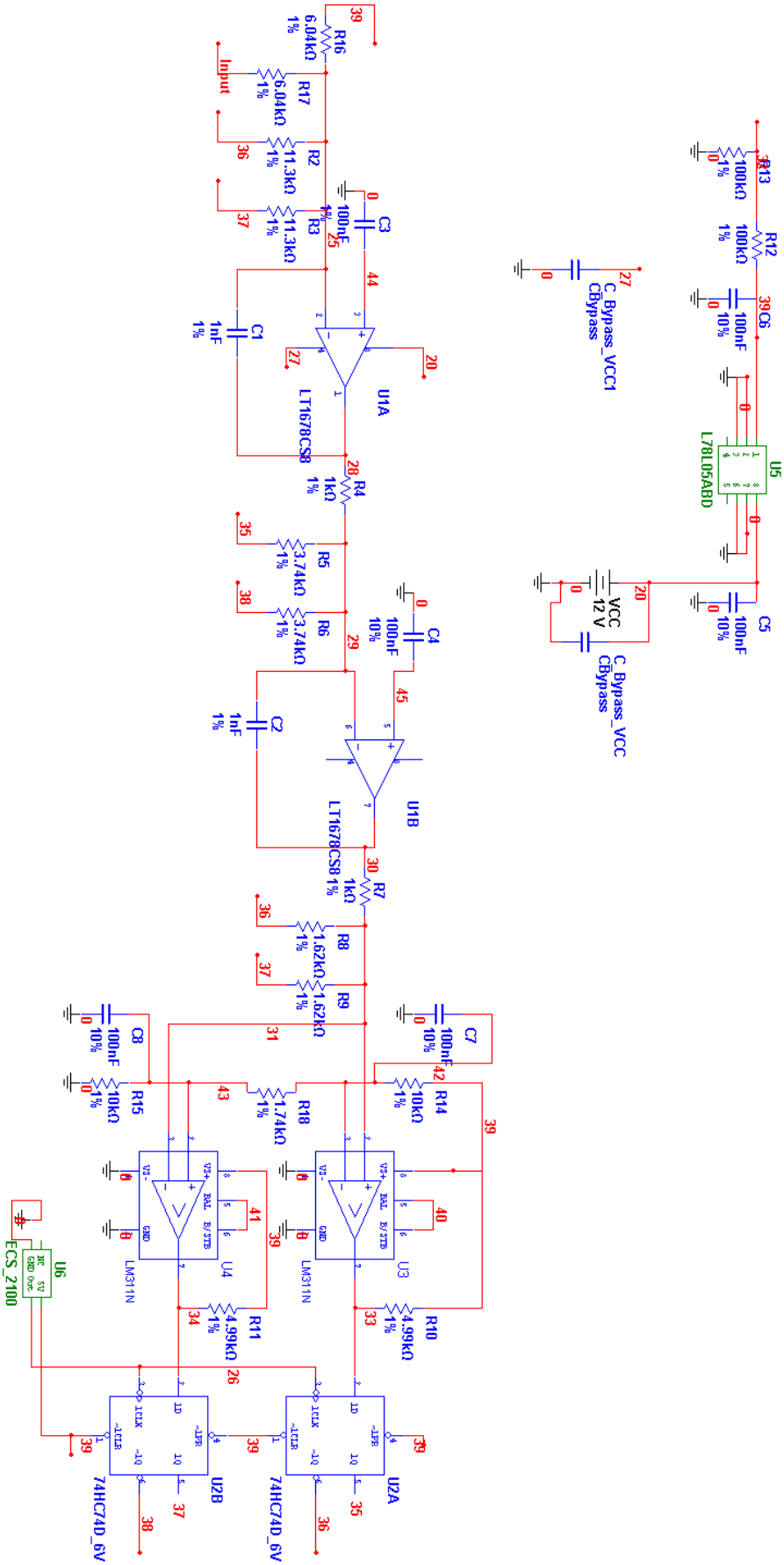

Figure H.2: Final Schematic - Modulator

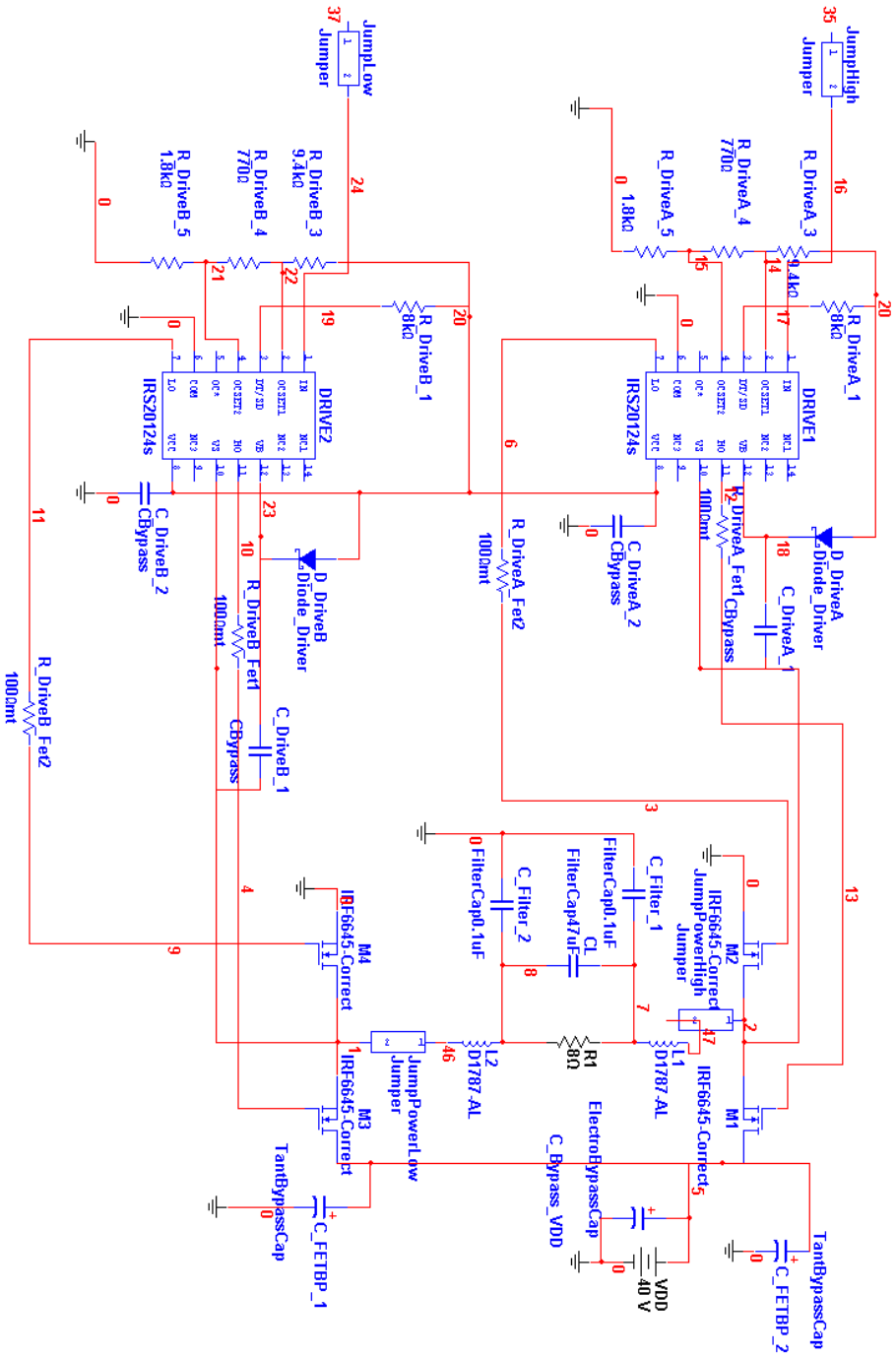

Figure H.3: Final Schematic - Power Stage and Filter

Appendix I

Final MATLAB Test Code

The following appendix gives the MATLAB code that was used to test the amplifier.

I.1 Efficiency

getValues.m

```
numFreqz = 12;
numAmps = 4;
numSwitch = 4;

amplitudes = [40,30,20,10];
freqz = [20,50,100,200,500,1000,2000,5000,10000,12000,15000,20000];
switches = [1,2,5,10];

efficiency = zeros(numSwitch,numAmps,numFreqz);
tempArr = zeros(numFreqz);

for k = 1:numSwitch
```

```
    if k==1
        filename = 'M:\MQP\final Efficiency Results\Efficiency - 1MHz';
    end
    if k==2
        filename = 'M:\MQP\final Efficiency Results\Efficiency - 2MHz';
    end
    if k==3
        filename = 'M:\MQP\final Efficiency Results\Efficiency - 5MHz';
    end
    if k==4
        filename = 'M:\MQP\final Efficiency Results\Efficiency - 10MHz';
    end
    for i = 1:numAmps
        tempArr = xlsread(filename,i,'m2:m13');
        for j=1:numFreqz
            efficiency(k,i,j) = tempArr(j)*100;
        end
    end
end
```

plotAmplitudeX.m

```
close all;
amplitudes = [40,30,20,10];

ampArr = zeros(1,numAmps);
figure;
hold all;
for i=1:numSwitch
```

```
    for j=1:numAmps
        ampArr(j) = efficiency(i,j,6);  % take the 1kHz values
    end

    plot(amplitudes, ampArr);



end
title('Plot for Efficiency of Input Signals at f = 1kHz');
xlabel('Output Signal Amplitude (Vpk-pk)');
ylabel('Efficiency (%)');
legend('1MHz','2MHz','5MHz','10MHz');
axis([5, 45, 55, 100]);

hold off;
```

plotFreqX.m

```
close all;

freqArr = zeros(1,numFreqz);
figure;
hold all;
for i=1:numSwitch
    for j=1:numFreqz
        freqArr(j) = efficiency(i,1,j);  % take the 1kHz values
    end

    semilogx(freqz, freqArr);
```

```
end
title('Plot for Efficiency at Full Output Power');
xlabel('Signal Frequency (Hz)');
ylabel('Efficiency (%)');
legend('1MHz','2MHz','5MHz','10MHz');
axis([20, 20e3, 90, 100])

hold off;
```

I.2 THD

THD.m

```
function THD = THD(signal, f, fs)
numHarm = 5;
harm = zeros(1, numHarm);



N=length(signal);
n=round(floor(N/fs*f)*fs/f); % # samples for whole number of periods
signal=signal(1:n);

SIG = abs(fft(signal));
SIG = SIG/max(SIG); % normalize the fft
```

```
[fund fundIndex] = max(SIG); % find the fundamental frequency

f = linspace(0,fs,length(signal));
fundFreq = f(fundIndex);

for i=1:numHarm % each iteration of the loop finds a new harmonic
    for j = 1:length(f) % loop through to find the harmonic
        if f(j) >= (i + 1)*fundFreq
            harmFreq = f(j); % output the frequency of the harmonic
            harm(i) = max(SIG(j-50:j+50));
            break;
        end
    end
end

% output all the values
SIG(fundIndex)

for i=1:numHarm
    harm(i)
end



% calculate the distortion
sumDist = 0;
for i=1:numHarm
    sumDist = sumDist + harm(i) * harm(i);
```

```
end

% calculate the THD
THD = sqrt(sumDist) * 100;
```

I.3 SNR

SNR.m

```
function snr = SNR(unk, noise)
%unk is the output signal, noise is the recorded "nothing" through the system
    SIG = abs(fft(unk));
    sigpwr = max(SIG)^2;
    noisepwr = sum(noise.^2);
    snr = 10*log10(sigpwr/noisepwr);

\section{Frequency Response}
\titlelineskip
\textit{plotFreqResponse.m}
\begin{verbatim}
inputRMS = input/(2*sqrt(2));

gain = zeros(1,numFreqz);

figure;
hold all;
```

```
for i=1:numSwitch
    for j=1:numFreqz
        gain(j) = output(i,j)/inputRMS(i);
    end

    reference = gain(6);
    gain = gain/reference;
    semilogx(freqz,20*10*log(gain));
end

title('Frequency Response at Full power');
xlabel('Signal Frequency (Hz)');
ylabel('Gain (dB)');
legend('1MHz','2MHz','5MHz','10MHz');

hold off;
```

Appendix J

Preliminary Efficiency Test Results

The following efficiency data was taken using a 1MHz, first order, two-level $\Delta\Sigma$ modulator.

Using an input sine wave with a V_{pk-pk} of 1.54V:

Input Freq. (Hz)	V_{in} (V_{DC})	I_{in} (A_{DC})	V_{out} (V_{RMS})	Resistance (Ω)	P_{in} (W)	P_{out} (W)	Efficiency (%)
20	39.86	0.2	6.65	8.05	7.972	5.493478261	68.90966208
50	39.86	0.22	6.65	8.05	8.7692	5.493478261	62.64514734
100	39.86	0.22	6.65	8.05	8.7692	5.493478261	62.64514734
200	39.86	0.22	6.65	8.05	8.7692	5.493478261	62.64514734
500	39.87	0.22	6.65	8.05	8.7714	5.493478261	62.62943499
1000	39.87	0.22	6.63	8.05	8.7714	5.460484472	62.25328308
2000	39.87	0.219	6.59	8.05	8.73153	5.394795031	61.78522013
5000	39.86	0.215	6.41	8.05	8.5699	5.104111801	59.5585923
10000	39.86	0.202	5.98	8.05	8.05172	4.442285714	55.17188519
12000	39.87	0.195	5.8	8.05	7.77465	4.178881988	53.75009792
15000	39.87	0.187	5.5	8.05	7.45569	3.757763975	50.40129049
20000	39.87	0.17	4.98	8.05	6.7779	3.080795031	45.45353326

Using an input sine wave with a V_{pk-pk} of 2.2V:

Input Freq. (Hz)	V_{in} (V_{DC})	I_{in} (A_{DC})	V_{out} (V_{RMS})	Resistance (Ω)	P_{in} (W)	P_{out} (W)	Efficiency (%)
20	39.83	0.3	8.89	8.05	11.949	9.817652174	82.1629607
50	39.84	0.332	8.9	8.05	13.22688	9.839751553	74.39208304
100	39.85	0.332	8.9	8.05	13.2302	9.839751553	74.37341501
200	39.85	0.332	8.9	8.05	13.2302	9.839751553	74.37341501
500	39.84	0.331	8.89	8.05	13.18704	9.817652174	74.44924846
1000	39.84	0.331	8.86	8.05	13.18704	9.751503106	73.94762665
2000	39.84	0.328	8.8	8.05	13.06752	9.619875776	73.61669067
5000	39.84	0.32	8.53	8.05	12.7488	9.038621118	70.89781876
10000	39.86	0.296	7.92	8.05	11.79856	7.792099379	66.04279996
12000	39.86	0.285	7.65	8.05	11.3601	7.269875776	63.99482202
15000	39.86	0.267	7.23	8.05	10.64262	6.49352795	61.01437381
20000	39.87	0.239	6.5	8.05	9.52893	5.248447205	55.07908238

Using an input sine wave with a V_{pk-pk} of 2.8V:

Input Freq. (Hz)	V_{in} (V_{DC})	I_{in} (A_{DC})	V_{out} (V_{RMS})	Resistance (Ω)	P_{in} (W)	P_{out} (W)	Efficiency (%)
20	39.8	0.5	11.16	8.05	19.9	15.47150311	77.74624676
50	39.81	0.479	11.17	8.05	19.06899	15.49924224	81.2798278
100	39.78	0.479	11.17	8.05	19.05462	15.49924224	81.34112481
200	39.93	0.486	11.22	8.05	19.40598	15.63831056	80.58500812
500	39.79	0.478	11.15	8.05	19.01962	15.44378882	81.19925014
1000	39.79	0.478	11.1	8.05	19.01962	15.30559006	80.47263858
2000	39.79	0.474	11	8.05	18.86046	15.0310559	79.69612565
5000	39.79	0.458	10.61	8.05	18.22382	13.9841118	76.73534858
10000	39.8	0.418	9.8	8.05	16.6364	11.93043478	71.71283921
12000	39.8	0.4	9.45	8.05	15.92	11.09347826	69.68265239
15000	39.81	0.369	8.88	8.05	14.68989	9.79557764	66.68244377
20000	39.82	0.321	7.93	8.05	12.78222	7.81178882	61.114492

Using an input sine wave with a V_{pk-pk} of 3.2V:

Input Freq. (Hz)	V_{in} (V_{DC})	I_{in} (A_{DC})	V_{out} (V_{RMS})	Resistance (Ω)	P_{in} (W)	P_{out} (W)	Efficiency (%)
20	39.8	0.7	13.45	8.05	27.86	22.47236025	80.66173815
50	39.77	0.661	13.46	8.05	26.28797	22.50578882	85.61250192
100	39.78	0.661	13.46	8.05	26.29458	22.50578882	85.59098042
200	39.77	0.661	13.45	8.05	26.28797	22.47236025	85.48533892
500	39.77	0.66	13.44	8.05	26.2482	22.43895652	85.48760114
1000	39.76	0.66	13.39	8.05	26.2416	22.27231056	84.87405707
2000	39.77	0.654	13.25	8.05	26.00958	21.80900621	83.84989766
5000	39.77	0.628	12.73	8.05	24.97556	20.13079503	80.60197662
10000	39.79	0.564	11.65	8.05	22.44156	16.85993789	75.12819023
12000	39.79	0.538	11.22	8.05	21.40702	15.63831056	73.0522537
15000	39.73	0.496	10.5	8.05	19.70608	13.69565217	69.49962739
20000	39.8	0.416	9.31	8.05	16.5568	10.76721739	65.03199526

Using an input sine wave with a V_{pk-pk} of 3.8V:

Input Freq. (Hz)	V_{in} (V_{DC})	I_{in} (A_{DC})	V_{out} (V_{RMS})	Resistance (Ω)	P_{in} (W)	P_{out} (W)	Efficiency (%)
20	39.73	0.9	15.78	8.05	35.757	30.9327205	86.50815364
50	39.73	0.879	15.79	8.05	34.92267	30.97193789	88.68719914
100	39.73	0.879	15.78	8.05	34.92267	30.9327205	88.57490134
200	39.74	0.878	15.78	8.05	34.89172	30.9327205	88.65346993
500	39.74	0.876	15.73	8.05	34.81224	30.73700621	88.29367548
1000	39.74	0.873	15.65	8.05	34.69302	30.42515528	87.6982035
2000	39.77	0.864	15.48	8.05	34.36128	29.76775155	86.63167249
5000	39.79	0.823	14.82	8.05	32.74717	27.28352795	83.31568178
10000	39.84	0.728	13.45	8.05	29.00352	22.47236025	77.48149276
12000	39.84	0.686	12.87	8.05	27.33024	20.57601242	75.28661447
15000	39.85	0.616	11.97	8.05	24.5476	17.79886957	72.50757534
20000	39.85	0.53	10.65	8.05	21.1205	14.08975155	66.71125945

Using an input sine wave with a V_{pk-pk} of 4V:

Input Freq. (Hz)	V_{in} (V_{DC})	I_{in} (A_{DC})	V_{out} (V_{RMS})	Resistance (Ω)	P_{in} (W)	P_{out} (W)	Efficiency (%)
20	39.8	1.2	18.16	8.05	47.76	40.96715528	85.77712579
50	39.8	1.16	18.18	8.05	46.168	41.05744099	88.93051679
100	39.8	1.156	18.17	8.05	46.0088	41.01228571	89.14008997
200	39.8	1.156	18.17	8.05	46.0088	41.01228571	89.14008997
500	39.82	1.153	18.12	8.05	45.91246	40.78688199	88.8361939
1000	39.82	1.149	18.03	8.05	45.75318	40.3827205	88.26210658
2000	39.83	1.136	17.8	8.05	45.24688	39.35900621	86.98722699
5000	39.84	1.078	16.97	8.05	42.94752	35.77402484	83.29706778
10000	39.8	0.909	15.26	8.05	36.1782	28.92765217	79.95879334
12000	39.81	0.854	14.6	8.05	33.99774	26.47950311	77.88606862
15000	39.83	0.772	13.57	8.05	30.74876	22.87514286	74.39370842
20000	39.84	0.68	12.02	8.05	27.0912	17.94787578	66.24983676

Using an input sine wave with a V_{pk-pk} of 4.8V:

Input Freq. (Hz)	V_{in} (V_{DC})	I_{in} (A_{DC})	V_{out} (V_{RMS})	Resistance (Ω)	P_{in} (W)	P_{out} (W)	Efficiency (%)
20	39.76	1.1	18.09	8.05	43.736	40.65193789	92.94845868
50	39.75	1.13	18.09	8.05	44.9175	40.65193789	90.50356295
100	39.73	1.13	18.09	8.05	44.8949	40.65193789	90.54912226
200	39.72	1.13	18.08	8.05	44.8836	40.60700621	90.471812
500	39.73	1.13	18.04	8.05	44.8949	40.42752795	90.04926606
1000	39.72	1.124	17.94	8.05	44.64528	39.98057143	89.55161985
2000	39.73	1.11	17.73	8.05	44.1003	39.05004969	88.54826314
5000	39.73	1.049	16.88	8.05	41.67677	35.39557764	84.9287928
10000	39.74	0.918	15.24	8.05	36.48132	28.85187578	79.08671007
12000	39.78	0.856	14.54	8.05	34.05168	26.26231056	77.12486009
15000	39.79	0.776	13.5	8.05	30.87704	22.63975155	73.32228592
20000	39.82	0.665	12.08	8.05	26.4803	18.12750311	68.45656245

Using an input sine wave with a V_{pk-pk} of 5.28V:

Input Freq. (Hz)	V_{in} (V_{DC})	I_{in} (A_{DC})	V_{out} (V_{RMS})	Resistance (Ω)	P_{in} (W)	P_{out} (W)	Efficiency (%)
20	39.76	1.7	22.83	8.05	67.592	64.7464472	95.79010416
50	39.78	1.74	22.84	8.05	69.2172	64.80318012	93.62294361
100	39.78	1.739	22.84	8.05	69.17742	64.80318012	93.67678084
200	39.78	1.739	22.82	8.05	69.17742	64.68973913	93.51279526
500	39.78	1.737	22.78	8.05	69.09786	64.46315528	93.29254955
1000	39.77	1.73	22.67	8.05	68.8021	63.84209938	92.79091682
2000	39.77	1.709	22.38	8.05	67.96693	62.21918012	91.54331397
5000	39.82	1.6	21.2	8.05	63.712	55.8310559	87.63036147
10000	39.84	1.37	18.97	8.05	54.5808	44.70321739	81.90282552
12000	39.85	1.271	18.02	8.05	50.64935	40.33793789	79.6415707
15000	39.87	1.129	16.63	8.05	45.01323	34.35489441	76.3217712
20000	39.89	0.945	14.65	8.05	37.69605	26.66118012	70.72672103

Using an input sine wave with a V_{pk-pk} of 5.6V:

Input Freq. (Hz)	V_{in} (V_{DC})	I_{in} (A_{DC})	V_{out} (V_{RMS})	Resistance (Ω)	P_{in} (W)	P_{out} (W)	Efficiency (%)
20	39.75	2.1	25.14	8.05	83.475	78.51175155	94.05420971
50	39.74	2.093	25.17	8.05	83.17582	78.69924224	94.61793372
100	39.74	2.095	25.17	8.05	83.2553	78.69924224	94.52760633
200	39.74	2.093	25.15	8.05	83.17582	78.5742236	94.46762725
500	39.72	2.092	25.09	8.05	83.09424	78.19976398	94.10972888
1000	39.72	2.085	25	8.05	82.8162	77.63975155	93.7494736
2000	39.73	2.059	24.69	8.05	81.80407	75.7262236	92.5702396
5000	39.75	1.918	23.37	8.05	76.2405	67.84557764	88.98889388
10000	39.8	1.62	20.72	8.05	64.476	53.33147826	82.71524018
12000	39.82	1.506	19.71	8.05	59.96892	48.25889441	80.47317579
15000	39.84	1.323	18.09	8.05	52.70832	40.65193789	77.12622578
20000	39.88	1.09	15.92	8.05	43.4692	31.48402484	72.42835121

Appendix K

Final Efficiency Test Results

The following appendix gives all the data that was gathered to calculate the efficiency of the final system. This was done at varying output voltages, clock frequencies and signal frequencies.

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.040	0.012	0.007	39.61	0.15	5.69	8.05	0.62	5.94	4.02	67.69%	61.26%
50	0.040	0.012	0.007	39.61	0.14	5.69	8.05	0.62	5.55	4.02	72.53%	65.19%
100	0.040	0.012	0.007	39.62	0.15	5.69	8.05	0.62	5.94	4.02	67.67%	61.24%
200	0.040	0.012	0.007	39.61	0.14	5.69	8.05	0.62	5.55	4.02	72.53%	65.19%
500	0.045	0.012	0.007	39.61	0.14	5.70	8.05	0.68	5.55	4.04	72.78%	64.79%
1000	0.045	0.012	0.007	39.62	0.15	5.69	8.05	0.68	5.94	4.02	67.67%	60.69%
2000	0.045	0.012	0.007	39.62	0.15	5.71	8.05	0.68	5.94	4.05	68.15%	61.12%
5000	0.045	0.012	0.007	39.62	0.15	5.83	8.05	0.68	5.94	4.22	71.05%	63.71%
10000	0.045	0.012	0.007	39.63	0.16	6.11	8.05	0.68	6.34	4.64	73.14%	66.02%
12000	0.045	0.012	0.007	39.60	0.17	6.20	8.05	0.68	6.73	4.78	70.93%	64.39%
15000	0.045	0.012	0.007	39.60	0.17	6.24	8.05	0.68	6.73	4.84	71.85%	65.22%
20000	0.044	0.012	0.007	39.61	0.17	6.12	8.05	0.67	6.73	4.65	69.10%	62.83%
$V_{in}(V_{p-p})$												
1.08												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.040	0.014	0.007	39.61	0.60	12.84	8.05	0.63	23.77	20.48	86.17%	83.94%
50	0.041	0.014	0.007	39.61	0.58	12.85	8.05	0.65	22.97	20.51	89.28%	86.84%
100	0.040	0.014	0.007	39.60	0.58	12.86	8.05	0.63	22.97	20.54	89.45%	87.04%
200	0.040	0.012	0.007	39.60	0.58	12.86	8.05	0.62	22.97	20.54	89.45%	87.08%
500	0.039	0.012	0.007	39.61	0.58	12.87	8.05	0.61	22.97	20.58	89.56%	87.24%
1000	0.040	0.012	0.007	39.61	0.58	12.87	8.05	0.62	22.97	20.58	89.56%	87.19%
2000	0.039	0.012	0.007	39.68	0.58	12.88	8.05	0.61	23.01	20.61	89.54%	87.22%
5000	0.040	0.012	0.007	39.60	0.59	12.97	8.05	0.62	23.36	20.90	89.44%	87.11%
10000	0.040	0.012	0.007	39.60	0.61	13.14	8.05	0.62	24.16	21.45	88.79%	86.56%
12000	0.040	0.012	0.007	39.60	0.61	13.16	8.05	0.62	24.16	21.51	89.06%	86.82%
15000	0.040	0.012	0.007	39.60	0.59	13.06	8.05	0.62	23.36	21.19	90.69%	88.33%
20000	0.040	0.012	0.007	39.60	0.55	12.46	8.05	0.62	21.78	19.29	88.55%	86.08%
$V_{in}(V_{p-p})$												
2.5												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.030	0.012	0.007	39.56	1.30	20.04	8.05	0.50	51.43	49.89	97.01%	96.06%
50	0.030	0.014	0.007	39.56	1.33	20.06	8.05	0.51	52.61	49.99	95.01%	94.09%
100	0.030	0.014	0.007	39.56	1.33	20.07	8.05	0.51	52.61	50.04	95.10%	94.18%
200	0.030	0.012	0.007	39.55	1.33	20.07	8.05	0.50	52.60	50.04	95.13%	94.22%
500	0.030	0.012	0.007	39.55	1.33	20.07	8.05	0.50	52.60	50.04	95.13%	94.22%
1000	0.030	0.012	0.007	39.55	1.33	20.08	8.05	0.50	52.60	50.09	95.22%	94.32%
2000	0.032	0.012	0.007	39.54	1.33	20.08	8.05	0.53	52.59	50.09	95.25%	94.30%
5000	0.034	0.012	0.007	39.55	1.34	20.13	8.05	0.55	53.00	50.34	94.98%	94.00%
10000	0.034	0.012	0.007	39.54	1.35	20.17	8.05	0.55	53.38	50.54	94.68%	93.71%
12000	0.034	0.012	0.007	39.54	1.35	20.12	8.05	0.55	53.38	50.29	94.21%	93.24%
15000	0.034	0.012	0.007	39.54	1.34	19.96	8.05	0.55	52.98	49.49	93.41%	92.44%
20000	0.034	0.012	0.007	39.55	1.28	19.30	8.05	0.55	50.62	46.27	91.40%	90.42%
$V_{in}(V_{p-p})$												
3.9												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.030	0.014	0.007	39.65	2.30	26.32	8.05	0.51	91.20	86.05	94.36%	93.83%
50	0.030	0.014	0.007	39.64	2.27	26.34	8.05	0.51	89.98	86.19	95.78%	95.24%
100	0.030	0.014	0.007	39.64	2.27	26.35	8.05	0.51	89.98	86.25	95.85%	95.31%
200	0.030	0.012	0.007	39.64	2.27	26.35	8.05	0.50	89.98	86.25	95.85%	95.32%
500	0.030	0.012	0.007	39.65	2.27	26.36	8.05	0.50	90.01	86.32	95.90%	95.37%
1000	0.030	0.012	0.007	39.64	2.27	26.37	8.05	0.50	89.98	86.38	96.00%	95.46%
2000	0.031	0.012	0.007	39.64	2.27	26.39	8.05	0.52	89.98	86.51	96.14%	95.60%
5000	0.029	0.012	0.007	39.64	2.28	26.40	8.05	0.49	90.38	86.58	95.80%	95.28%
10000	0.029	0.012	0.007	39.64	2.30	26.45	8.05	0.49	91.17	86.91	95.32%	94.81%
12000	0.029	0.012	0.007	39.63	2.35	26.64	8.05	0.49	93.13	88.16	94.66%	94.17%
15000	0.028	0.012	0.007	39.62	2.38	26.78	8.05	0.48	94.30	89.09	94.48%	94.00%
20000	0.021	0.014	0.008	39.60	2.71	28.53	8.05	0.42	107.32	101.11	94.22%	93.85%
$V_{in}(V_{p-p})$												
5.1												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.070	0.013	0.006	39.84	0.20	6.96	8.05	0.98	7.97	6.02	75.52%	67.27%
50	0.060	0.013	0.006	39.85	0.20	6.94	8.05	0.86	7.97	5.98	75.07%	67.78%
100	0.060	0.130	0.006	39.85	0.20	6.94	8.05	1.44	7.97	5.98	75.07%	63.57%
200	0.060	0.013	0.006	39.85	0.21	6.94	8.05	0.86	8.37	5.98	71.49%	64.85%
500	0.060	0.013	0.006	39.85	0.20	6.94	8.05	0.86	7.97	5.98	75.07%	67.78%
1000	0.060	0.013	0.006	39.85	0.20	6.95	8.05	0.86	7.97	6.00	75.29%	67.98%
2000	0.059	0.013	0.006	39.85	0.20	6.96	8.05	0.85	7.97	6.02	75.50%	68.27%
5000	0.062	0.013	0.006	39.85	0.20	7.00	8.05	0.88	7.97	6.09	76.37%	68.77%
10000	0.066	0.013	0.006	39.85	0.23	7.26	8.05	0.93	9.17	6.55	71.44%	64.86%
12000	0.067	0.013	0.006	39.84	0.24	7.37	8.05	0.94	9.56	6.75	70.57%	64.25%
15000	0.067	0.013	0.006	39.84	0.25	7.45	8.05	0.94	9.96	6.89	69.22%	63.25%
20000	0.067	0.013	0.006	39.85	0.23	7.26	8.05	0.94	9.17	6.55	71.44%	64.79%
$V_{in}(V_{p-p})$												
1.4												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.060	0.013	0.006	39.80	0.63	13.55	8.05	0.86	25.07	22.81	90.96%	87.96%
50	0.055	0.013	0.006	39.80	0.64	13.56	8.05	0.80	25.47	22.84	89.67%	86.95%
100	0.055	0.013	0.006	39.80	0.64	13.57	8.05	0.80	25.47	22.88	89.81%	87.08%
200	0.055	0.013	0.006	39.79	0.64	13.56	8.05	0.80	25.47	22.84	89.70%	86.97%
500	0.055	0.013	0.007	39.80	0.64	13.57	8.05	0.81	25.47	22.88	89.81%	87.04%
1000	0.055	0.014	0.007	39.79	0.64	13.57	8.05	0.81	25.47	22.88	89.83%	87.05%
2000	0.055	0.014	0.006	39.80	0.64	13.59	8.05	0.80	25.47	22.94	90.07%	87.32%
5000	0.059	0.014	0.007	39.79	0.65	13.65	8.05	0.86	25.86	23.15	89.49%	86.61%
10000	0.058	0.014	0.007	39.78	0.68	13.84	8.05	0.85	27.05	23.79	87.96%	85.28%
12000	0.058	0.014	0.007	39.78	0.68	13.86	8.05	0.85	27.05	23.86	88.22%	85.53%
15000	0.058	0.014	0.007	39.78	0.68	13.80	8.05	0.85	27.05	23.66	87.46%	84.79%
20000	0.057	0.014	0.007	39.79	0.63	13.18	8.05	0.84	25.07	21.58	86.08%	83.30%
$V_{in}(V_{p-p})$												
2.7												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.045	0.013	0.007	39.70	1.60	22.10	8.05	0.69	63.52	60.67	95.52%	94.49%
50	0.045	0.013	0.007	39.69	1.62	22.12	8.05	0.69	64.30	60.78	94.53%	93.53%
100	0.045	0.013	0.007	39.69	1.62	22.13	8.05	0.69	64.30	60.84	94.62%	93.61%
200	0.045	0.013	0.070	39.70	1.62	22.13	8.05	1.45	64.31	60.84	94.59%	92.51%
500	0.045	0.013	0.007	39.70	1.62	22.13	8.05	0.69	64.31	60.84	94.59%	93.59%
1000	0.045	0.013	0.007	39.69	1.62	22.15	8.05	0.69	64.30	60.95	94.79%	93.78%
2000	0.043	0.013	0.007	39.70	1.62	22.16	8.05	0.67	64.31	61.00	94.85%	93.88%
5000	0.047	0.013	0.007	39.71	1.63	22.18	8.05	0.71	64.73	61.11	94.41%	93.39%
10000	0.046	0.013	0.007	39.70	1.64	22.16	8.05	0.70	65.11	61.00	93.69%	92.70%
12000	0.046	0.013	0.007	39.71	1.63	22.05	8.05	0.70	64.73	60.40	93.31%	92.31%
15000	0.045	0.013	0.007	39.71	1.59	21.71	8.05	0.69	63.14	58.55	92.73%	91.73%
20000	0.044	0.013	0.007	39.70	1.46	20.57	8.05	0.68	57.96	52.56	90.68%	89.64%
$V_{in}(V_{p-p})$												
4.34												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.040	0.013	0.007	39.64	2.30	26.61	8.05	0.63	91.17	87.96	96.48%	95.82%
50	0.040	0.013	0.007	39.64	2.33	26.64	8.05	0.63	92.36	88.16	95.45%	94.81%
100	0.040	0.013	0.007	39.63	2.33	26.64	8.05	0.63	92.34	88.16	95.48%	94.83%
200	0.040	0.013	0.007	39.63	2.33	26.64	8.05	0.63	92.34	88.16	95.48%	94.83%
500	0.040	0.013	0.007	39.63	2.32	26.65	8.05	0.63	91.94	88.23	95.96%	95.31%
1000	0.040	0.012	0.007	39.64	2.33	26.67	8.05	0.62	92.36	88.36	95.67%	95.02%
2000	0.036	0.013	0.007	39.64	2.33	26.68	8.05	0.58	92.36	88.43	95.74%	95.14%
5000	0.040	0.013	0.007	39.64	2.34	26.67	8.05	0.63	92.76	88.36	95.26%	94.62%
10000	0.040	0.012	0.007	39.65	2.33	26.53	8.05	0.62	92.38	87.43	94.64%	94.01%
12000	0.040	0.013	0.007	39.66	2.32	26.41	8.05	0.63	92.01	86.64	94.17%	93.53%
15000	0.038	0.013	0.007	39.66	2.34	26.42	8.05	0.61	92.80	86.71	93.43%	92.83%
20000	0.034	0.013	0.007	39.67	2.26	25.87	8.05	0.56	89.65	83.14	92.73%	92.16%
$V_{in}(V_{p-p})$												
5.2												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.060	0.014	0.007	39.85	0.18	6.81	8.05	0.87	7.17	5.76	80.32%	71.59%
50	0.060	0.014	0.007	39.85	0.18	6.81	8.05	0.87	7.17	5.76	80.32%	71.59%
100	0.060	0.014	0.006	39.85	0.18	6.82	8.05	0.86	7.17	5.78	80.55%	71.91%
200	0.060	0.014	0.006	39.85	0.18	6.82	8.05	0.86	7.17	5.78	80.55%	71.91%
500	0.060	0.014	0.006	39.85	0.18	6.82	8.05	0.86	7.17	5.78	80.55%	71.91%
1000	0.060	0.014	0.006	39.85	0.18	6.82	8.05	0.86	7.17	5.78	80.55%	71.91%
2000	0.058	0.014	0.006	39.85	0.18	6.82	8.05	0.84	7.17	5.78	80.55%	72.13%
5000	0.055	0.014	0.006	39.85	0.18	6.81	8.05	0.80	7.17	5.76	80.32%	72.24%
10000	0.055	0.014	0.006	39.85	0.18	6.75	8.05	0.80	7.17	5.66	78.91%	70.97%
12000	0.055	0.014	0.006	39.85	0.18	6.70	8.05	0.80	7.17	5.58	77.74%	69.92%
15000	0.055	0.014	0.006	39.85	0.17	6.56	8.05	0.80	6.77	5.35	78.91%	70.56%
20000	0.055	0.014	0.006	39.86	0.16	6.12	8.05	0.80	6.38	4.65	72.95%	64.80%
$V_{in}(V_{p-p})$												
1.38												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.080	0.014	0.007	39.81	0.60	13.22	8.05	1.11	23.89	21.71	90.89%	86.84%
50	0.060	0.014	0.007	39.81	0.60	13.22	8.05	0.87	23.89	21.71	90.89%	87.68%
100	0.060	0.014	0.007	39.83	0.60	13.22	8.05	0.87	23.90	21.71	90.85%	87.64%
200	0.060	0.014	0.007	39.82	0.60	13.22	8.05	0.87	23.89	21.71	90.87%	87.66%
500	0.060	0.014	0.007	39.82	0.60	13.21	8.05	0.87	23.89	21.68	90.73%	87.53%
1000	0.060	0.014	0.006	39.82	0.60	13.21	8.05	0.86	23.89	21.68	90.73%	87.57%
2000	0.060	0.014	0.006	39.81	0.60	13.21	8.05	0.86	23.89	21.68	90.75%	87.59%
5000	0.060	0.014	0.006	39.82	0.62	13.29	8.05	0.86	24.69	21.94	88.87%	85.87%
10000	0.056	0.014	0.006	39.82	0.62	13.40	8.05	0.81	24.81	22.31	89.91%	87.06%
12000	0.060	0.014	0.006	39.82	0.63	13.37	8.05	0.86	25.09	22.21	88.52%	85.58%
15000	0.600	0.014	0.006	39.82	0.63	13.34	8.05	7.34	25.09	22.11	88.12%	68.17%
20000	0.060	0.014	0.007	39.82	0.61	13.13	8.05	0.87	24.29	21.42	88.17%	85.10%
$V_{in}(V_{p-p})$												
2.66												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.060	0.014	0.007	39.78	1.60	21.82	8.05	0.87	63.65	59.14	92.92%	91.67%
50	0.050	0.014	0.007	39.78	1.57	21.84	8.05	0.75	62.45	59.25	94.87%	93.74%
100	0.050	0.014	0.007	39.78	1.57	21.84	8.05	0.75	62.45	59.25	94.88%	93.75%
200	0.050	0.014	0.007	39.78	1.57	21.84	8.05	0.75	62.45	59.25	94.87%	93.74%
500	0.050	0.014	0.007	39.77	1.57	21.84	8.05	0.75	62.44	59.25	94.90%	93.77%
1000	0.050	0.014	0.007	39.77	1.58	21.85	8.05	0.75	62.84	59.31	94.38%	93.26%
2000	0.050	0.014	0.007	39.78	1.58	21.87	8.05	0.75	62.85	59.42	94.53%	93.41%
5000	0.047	0.014	0.007	39.78	1.58	21.88	8.05	0.72	62.85	59.47	94.62%	93.55%
10000	0.049	0.014	0.007	39.77	1.60	21.88	8.05	0.74	63.63	59.47	93.46%	92.38%
12000	0.048	0.014	0.007	39.77	1.59	21.79	8.05	0.73	63.23	58.98	93.28%	92.21%
15000	0.047	0.014	0.007	39.77	1.56	21.48	8.05	0.72	62.04	57.32	92.38%	91.33%
20000	0.047	0.014	0.007	39.78	1.40	20.19	8.05	0.72	55.69	50.64	90.93%	89.77%
$V_{in}(V_{p-p})$												
4.3												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.050	0.014	0.006	39.67	2.30	26.57	8.05	0.74	91.24	87.70	96.12%	95.34%
50	0.050	0.014	0.007	39.67	2.31	26.59	8.05	0.75	91.64	87.83	95.84%	95.06%
100	0.050	0.014	0.007	39.67	2.31	26.60	8.05	0.75	91.64	87.90	95.92%	95.13%
200	0.040	0.014	0.007	39.67	2.31	26.59	8.05	0.63	91.64	87.83	95.84%	95.19%
500	0.050	0.014	0.007	39.68	2.31	26.60	8.05	0.75	91.66	87.90	95.89%	95.11%
1000	0.050	0.014	0.007	39.68	2.31	26.62	8.05	0.75	91.66	88.03	96.04%	95.25%
2000	0.040	0.014	0.007	39.80	2.33	26.71	8.05	0.63	92.73	88.62	95.57%	94.92%
5000	0.040	0.014	0.007	39.75	2.32	26.64	8.05	0.63	92.22	88.16	95.60%	94.94%
10000	0.041	0.014	0.007	39.76	2.32	26.51	8.05	0.65	92.24	87.30	94.64%	93.98%
12000	0.041	0.014	0.007	39.75	2.30	26.29	8.05	0.65	91.43	85.86	93.91%	93.25%
15000	0.040	0.014	0.007	39.76	2.25	25.94	8.05	0.63	89.46	83.59	93.44%	92.78%
20000	0.036	0.014	0.007	39.77	2.14	25.17	8.05	0.59	85.11	78.70	92.47%	91.84%
$V_{in}(V_{p-p})$												
5.2												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.060	0.016	0.007	39.66	0.15	6.36	8.05	0.88	5.95	5.02	84.46%	73.54%
50	0.060	0.016	0.007	39.67	0.16	6.37	8.05	0.88	6.35	5.04	79.41%	69.71%
100	0.060	0.016	0.007	39.66	0.16	6.37	8.05	0.88	6.35	5.04	79.43%	69.72%
200	0.060	0.016	0.007	39.66	0.16	6.37	8.05	0.88	6.35	5.04	79.43%	69.72%
500	0.060	0.016	0.007	39.66	0.16	6.37	8.05	0.88	6.35	5.04	79.43%	69.72%
1000	0.060	0.016	0.007	39.66	0.16	6.37	8.05	0.88	6.35	5.04	79.43%	69.72%
2000	0.060	0.016	0.007	39.66	0.16	6.37	8.05	0.88	6.35	5.04	79.43%	69.72%
5000	0.060	0.016	0.007	39.65	0.16	6.35	8.05	0.88	6.34	5.01	78.96%	69.30%
10000	0.058	0.016	0.007	39.65	0.16	6.28	8.05	0.86	6.34	4.90	77.23%	68.01%
12000	0.058	0.016	0.007	39.64	0.16	6.22	8.05	0.86	6.34	4.81	75.78%	66.73%
15000	0.058	0.016	0.007	39.64	0.16	6.06	8.05	0.86	6.34	4.56	71.93%	63.34%
20000	0.056	0.016	0.007	39.63	0.14	5.64	8.05	0.84	5.55	3.95	71.22%	61.90%
$V_{in}(V_{p-p})$												
1.31												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.060	0.016	0.007	39.63	0.60	13.29	8.05	0.88	23.78	21.94	92.27%	88.97%
50	0.060	0.016	0.007	39.63	0.62	13.30	8.05	0.88	24.57	21.97	89.43%	86.33%
100	0.060	0.016	0.007	39.63	0.62	13.31	8.05	0.88	24.57	22.01	89.57%	86.46%
200	0.060	0.016	0.007	39.63	0.62	13.31	8.05	0.88	24.57	22.01	89.57%	86.46%
500	0.060	0.016	0.007	39.63	0.62	13.31	8.05	0.88	24.57	22.01	89.57%	86.46%
1000	0.060	0.016	0.007	39.63	0.62	13.31	8.05	0.88	24.57	22.01	89.57%	86.46%
2000	0.058	0.016	0.007	39.63	0.62	13.34	8.05	0.86	24.57	22.11	89.97%	86.93%
5000	0.055	0.016	0.007	39.63	0.62	13.41	8.05	0.82	24.57	22.34	90.92%	87.97%
10000	0.062	0.016	0.007	39.61	0.64	13.49	8.05	0.91	25.35	22.61	89.18%	86.09%
12000	0.063	0.016	0.007	39.62	0.65	13.46	8.05	0.92	25.75	22.51	87.39%	84.38%
15000	0.062	0.016	0.007	39.62	0.66	13.53	8.05	0.91	26.15	22.74	86.96%	84.05%
20000	0.060	0.016	0.007	39.61	0.63	13.23	8.05	0.88	24.95	21.74	87.13%	84.15%
V_{in}												
2.69												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.050	0.016	0.007	39.54	1.40	20.19	8.05	0.76	55.36	50.64	91.48%	90.23%
50	0.060	0.016	0.007	39.54	1.36	20.20	8.05	0.88	53.77	50.69	94.26%	92.74%
100	0.060	0.016	0.007	39.56	1.36	20.21	8.05	0.88	53.80	50.74	94.31%	92.78%
200	0.060	0.016	0.007	39.56	1.37	20.21	8.05	0.88	54.20	50.74	93.62%	92.12%
500	0.050	0.016	0.007	39.57	1.37	20.22	8.05	0.76	54.21	50.79	93.69%	92.39%
1000	0.050	0.016	0.007	39.55	1.37	20.22	8.05	0.76	54.18	50.79	93.73%	92.43%
2000	0.050	0.016	0.007	39.54	1.37	20.24	8.05	0.76	54.17	50.89	93.94%	92.64%
5000	0.052	0.016	0.007	39.55	1.37	20.26	8.05	0.79	54.18	50.99	94.11%	92.76%
10000	0.053	0.016	0.007	39.56	1.39	20.29	8.05	0.80	54.99	51.14	93.00%	91.67%
12000	0.053	0.016	0.007	39.55	1.39	20.25	8.05	0.80	54.97	50.94	92.66%	91.33%
15000	0.053	0.016	0.007	39.55	1.37	19.98	8.05	0.80	54.18	49.59	91.52%	90.19%
20000	0.050	0.016	0.007	39.57	1.23	18.77	8.05	0.76	48.67	43.77	89.92%	88.53%
$V_{in}(V_{p-p})$												
4.02												

Freq. (Hz)	I_{12} (A)	I_5 (A)	I_{-12} (A)	V_{in} (V)	I_{in} (A)	V_{out} (V_{rms})	Res. (Ω)	$P_{in-sig.}$ (W)	P_{in} (W)	P_{out} (W)	Efficiency PS (%)	Efficieny Total (%)
20	0.060	0.016	0.007	39.45	2.30	26.62	8.05	0.88	90.74	88.03	97.02%	96.08%
50	0.050	0.016	0.007	39.43	2.34	26.65	8.05	0.76	92.27	88.23	95.62%	94.84%
100	0.050	0.016	0.007	39.46	2.34	26.66	8.05	0.76	92.34	88.29	95.62%	94.84%
200	0.040	0.016	0.007	39.43	2.34	26.65	8.05	0.64	92.27	88.23	95.62%	94.96%
500	0.040	0.016	0.007	39.43	2.34	26.66	8.05	0.64	92.27	88.29	95.69%	95.03%
1000	0.040	0.016	0.007	39.42	2.34	26.68	8.05	0.64	92.24	88.43	95.86%	95.20%
2000	0.040	0.016	0.007	39.41	2.34	26.69	8.05	0.64	92.22	88.49	95.96%	95.29%
5000	0.044	0.016	0.007	39.42	2.35	26.64	8.05	0.69	92.64	88.16	95.17%	94.46%
10000	0.043	0.016	0.007	39.43	2.34	26.51	8.05	0.68	92.27	87.30	94.62%	93.93%
12000	0.042	0.016	0.007	39.44	2.32	26.33	8.05	0.67	91.50	86.12	94.12%	93.44%
15000	0.040	0.016	0.007	39.41	2.29	26.04	8.05	0.64	90.25	84.23	93.33%	92.67%
20000	0.036	0.016	0.007	39.45	2.17	25.32	8.05	0.60	85.61	79.64	93.03%	92.39%
$V_{in}(V_{p-p})$												
5.25												

Appendix L

Final Sound Quality Test Results

The following appendix gives all the plots that were taken for sound quality testing. These include Total Harmonic Distortion, Signal to Noise Ratio and Frequency Response. First the loopback results are shown. Then those that were taken by sweeping through input frequencies and using a 1MHz, 2MHz, 5MHz, and 10MHz clock frequencies are given

L.1 Loopback Results

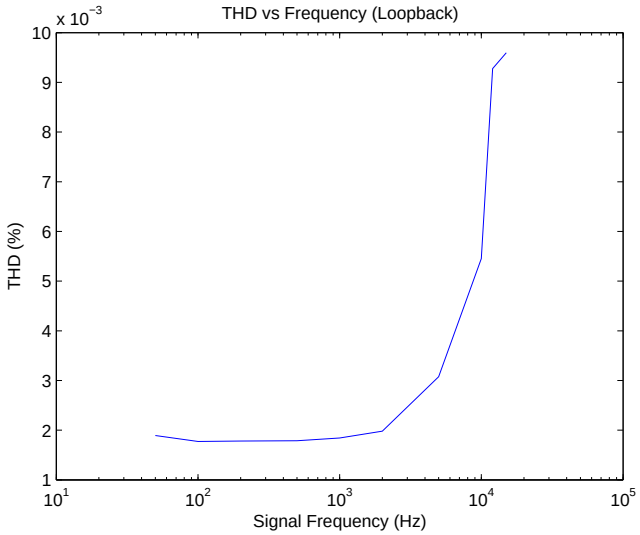

Figure L.1: THD results for Loopback Test

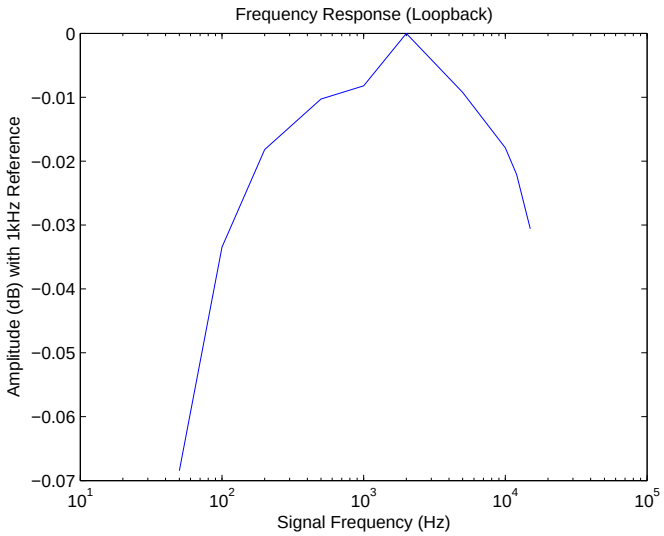

Figure L.2: Frequency Response results for Loopback Test

L.2 Signal Quality Results with 1MHz Modulation Frequency

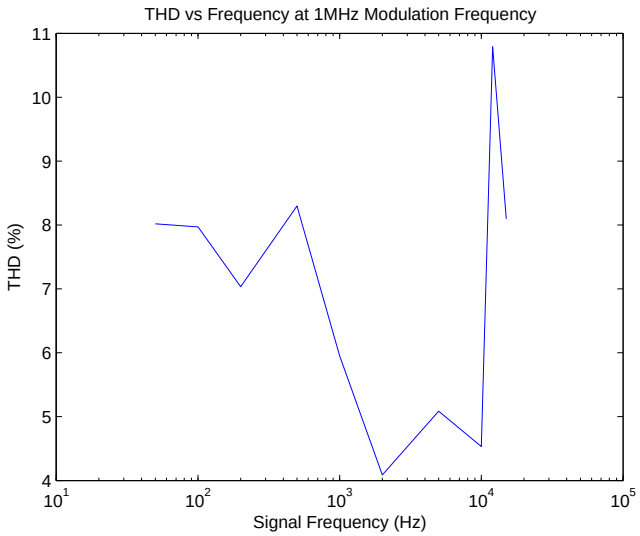

Figure L.3: THD results at 1MHz clock frequency

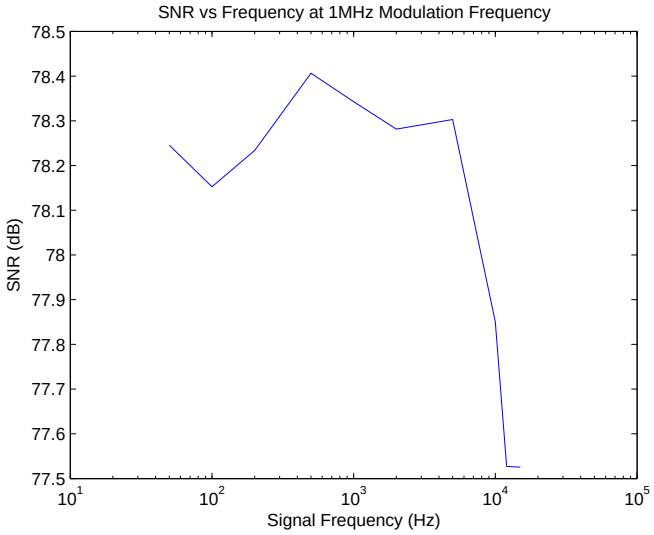

Figure L.4: SNR results at 1MHz clock frequency

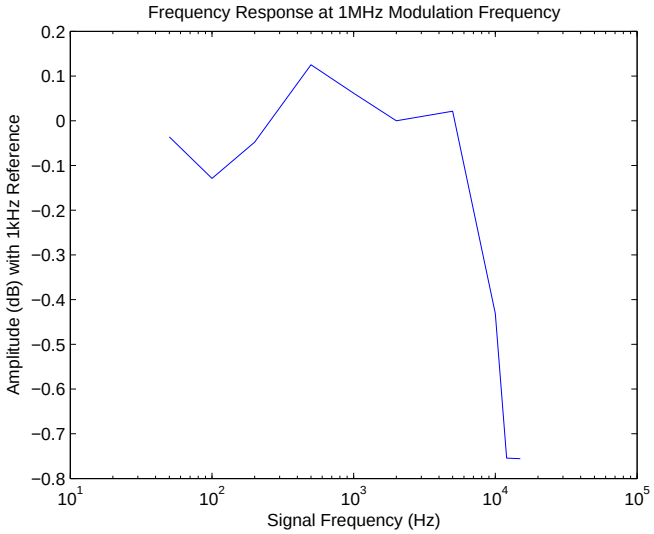

Figure L.5: Frequency Response resuplotlts at 1MHz clock frequency

L.3 Signal Quality Results with 2MHz Modulation Frequency

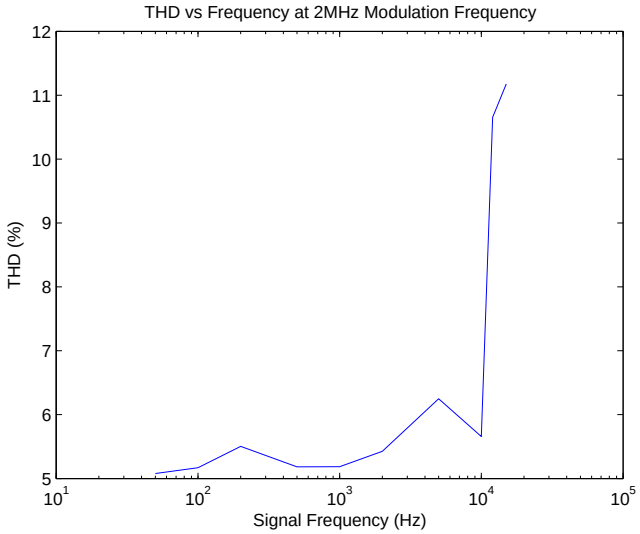

Figure L.6: THD results at 2MHz clock frequency

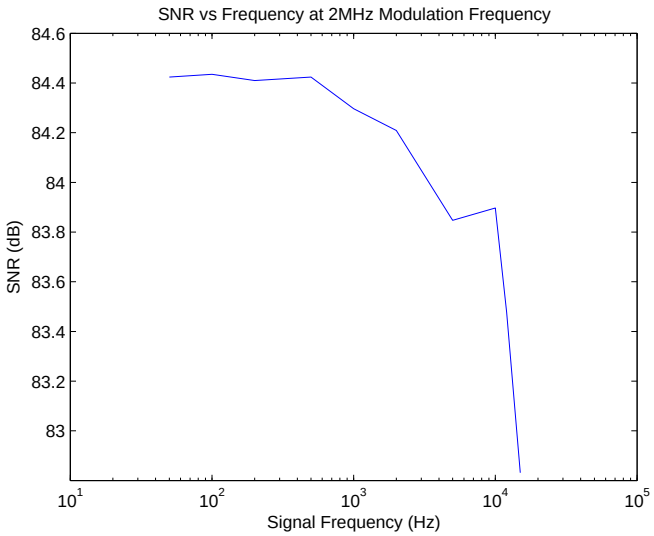

Figure L.7: SNR results at 2MHz clock frequency

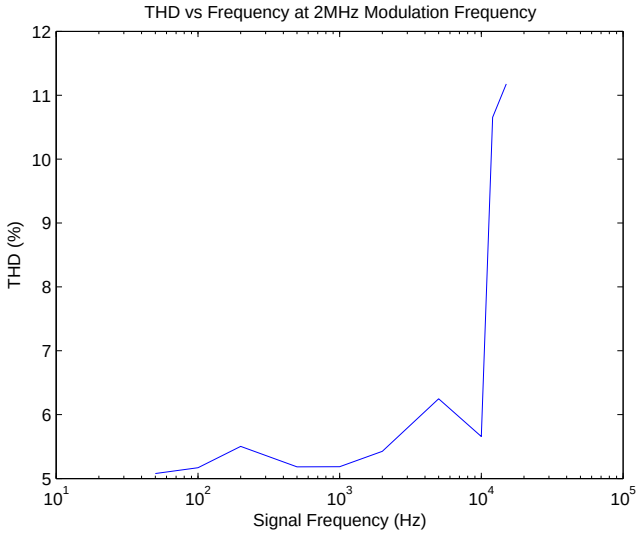

Figure L.8: Frequency Response results at 2MHz clock frequency

L.4 Signal Quality Results with 5MHz Modulation Frequency

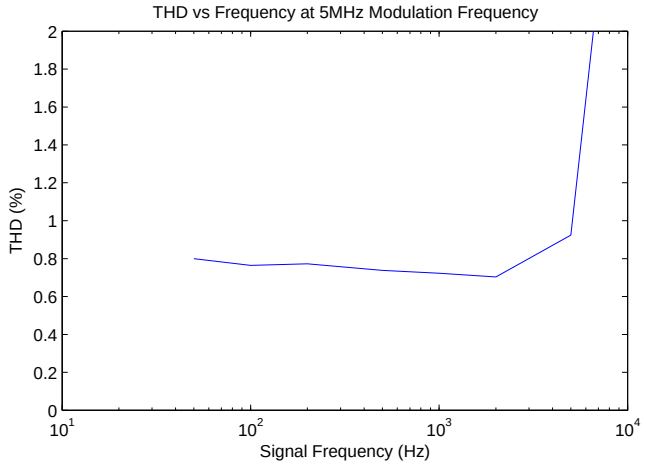

Figure L.9: THD results at 5MHz clock frequency

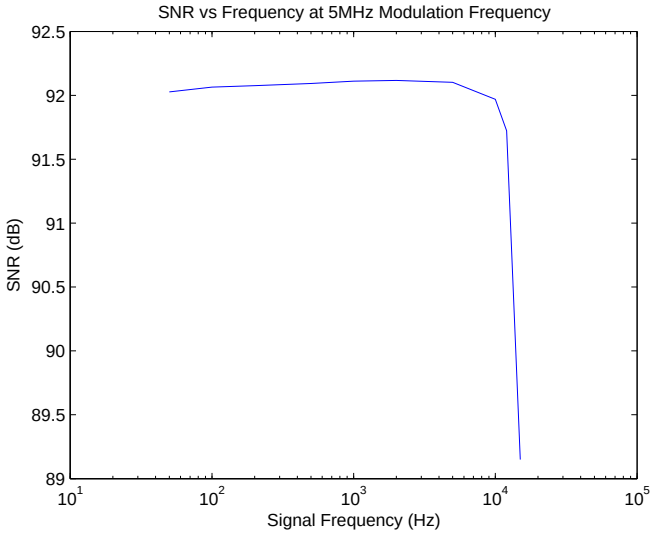

Figure L.10: SNR results at 5MHz clock frequency

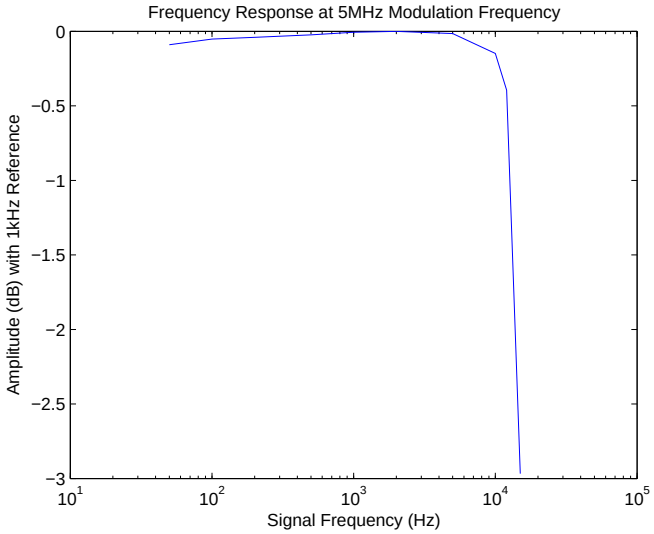

Figure L.11: Frequency Response results at 5MHz clock frequency

L.5 Signal Quality Results with 10MHz Modulation Frequency

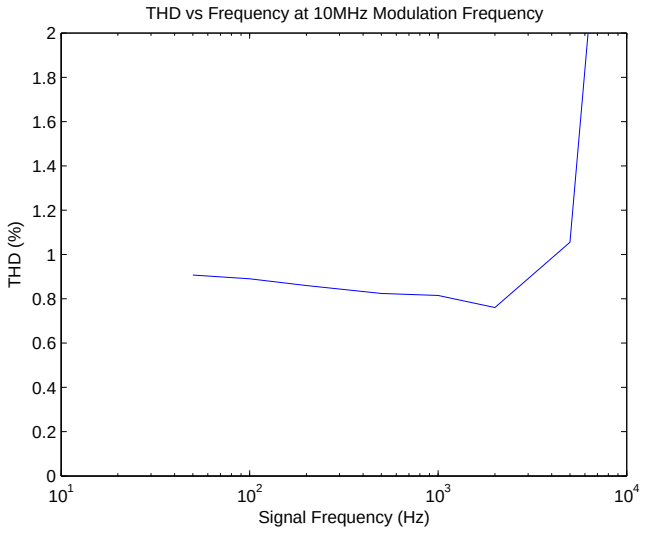

Figure L.12: THD results at 10MHz clock frequency

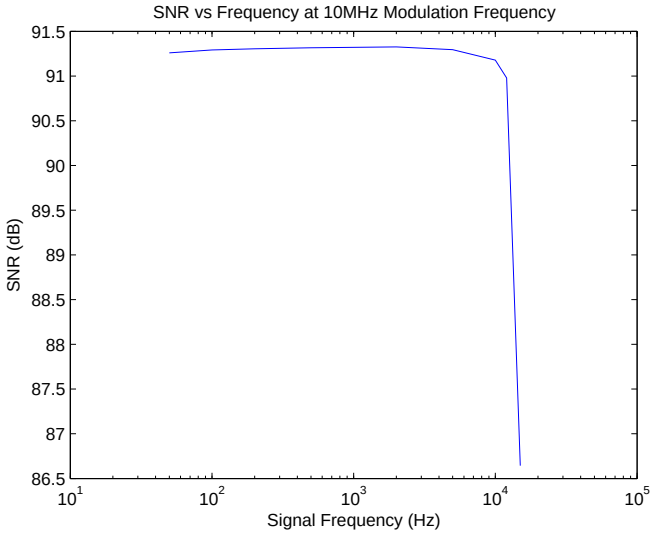

Figure L.13: SNR results at 10MHz clock frequency

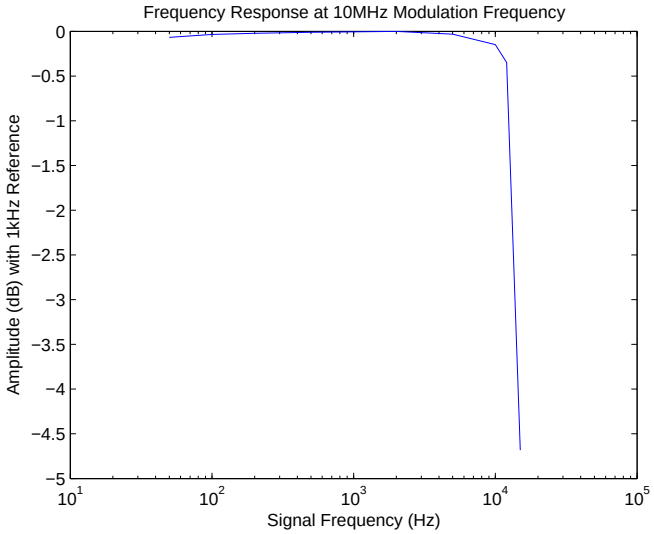

Figure L.14: Frequency Response results at 10MHz clock frequency

Appendix M

Digital Audio

Digital audio has been around in various forms for over 20 years, the most ubiquitous form being the Compact Disc (CD) format. In more recent years digital audio has moved to other media, such as the Internet, and digital audio players, such as iPods. All of the advances in digital audio have greatly benefitted consumers, especially those interested in hi-fidelity sound systems. The live audio market however, has remained mostly in the analog domain, specifically with regard to live audio mixing consoles and amplifiers. In some respects this makes sense; the purpose of live audio equipment is to amplify an analog signal for immediate playback, so converting to digital seems like it would be a cumbersome step that would introduce more problems than it would solve. With recent advances in technology, however, the hurdles associated with digital audio, such as increased noise and decreased audio fidelity, have almost been completely negated.

Before beginning a discussion of the way in which digital audio could be implemented in the live audio market, several terms need to be defined. The quality of a digital audio signal can be described by numbers, most importantly the sampling frequency, or Nyquist Rate, and the bit depth. The sampling frequency is how often a single digital sample is taken from the analog signal. A Nyquist Rate of 96 kHz means that one second of audio has 96,000 samples. This number is important because the Nyquist-Shannon Sampling Theorem dictates how

much bandwidth a digital system can capture. According to the theorem a system must sample at a rate a frequency of at least twice the highest frequency in the original signal (the Nyquist Frequency); however, most systems for digital audio oversample anywhere from 44.1 kHz (CDs) to 96 kHz, especially for high end digital mixing consoles. A small amount of oversampling is necessary to counter real world non-idealities such as imperfect filters, though in practice the amount of oversampling required is minimal at perhaps 2.2 times the Nyquist Frequency instead of twice the Nyquist Frequency. While high end digital audio has Nyquist Rates of up to 96 kHz, significantly higher than the required Nyquist Rate, it is difficult to experimentally prove this rate is necessary. Regardless of technical reasons, the market expects a higher Nyquist Rate for high end digital audio, so engineers must meet market expectations for products to be successful.

The bit depth, how many bits per sample, is somewhat more important for audio quality. A CD has a bit depth of 16 bits per sample, which means that there are 2^{16} different possible values for each individual sample. These values correspond to the analog voltage level of the original signal. The limiting factor of 16 bit audio is the maximum dynamic range, or the maximum difference between the loudest and quietest sound that a system can produce. 16 bit audio is limited to a 96 dB maximum dynamic range, though CDs rarely achieve this total range. While 96 dB may seem like an adequate dynamic range for audio, many bands require sound levels of over 110 dB in their venues. A maximum dynamic range of only 96 dB would therefore result in a relatively loud noise floor, manifested as a hissing during quiet portions of the show. The solution to this problem is to move to 24 bits per sample, which has a maximum dynamic range of 144 dB. The threshold of pain is roughly 125 dB, so a dynamic range of 144 dB is more than adequate for providing high quality sound with minimal noise in live audio. The first step towards digital audio in the live audio market was the development of digital mixing consoles. There are a number of different digital mixing consoles produced by a variety of different manufacturers, including Midas, a company known for producing the some of the highest quality analog mixing consoles. While

each digital mixing console is different, they all have the same basic operation. An analog input, such as a microphone or a guitar, is converted to a digital signal through an Analog to Digital Converter. The digital signal can then be processed in a myriad of different ways, including features like gating, compressing, and equalizing, that comparable analog mixing consoles cannot do on-board. Finally, the mixed digital signals are then passed through a Digital to Analog Converter to be sent to the amplifiers. An immediate benefit can be seen by the processing options available to a digital mixing console, though some audio purists argue that the act of converting between digital and audio will degrade the quality of the signal. Digital mixing consoles sample at rates between 44.1 kHz [YMH07] and 96 kHz and 24 bits per sample, however [MDS08]. As explained above, these values are more than adequate to capture any audio during a live concert.

The second link in the chain for a full digital signal path is the snake. A snake is a large cable that contains multiple audio channels, and is used to easily send signals between the stage and the mixing console. Traditionally audio snakes have been purely analog, consisting of many separate audio paths within one large shielded cable. This analog method works and is still used extensively, but it is expensive to produce the cable, difficult to use because of the girth of the cable, and potentially subject to noise if the shielding is improperly connected or grounding issues occur. In comparison, a digital snake is generally a single CAT5 or CAT6 twisted pair cable, the same as used in most personal computer networks. A digital snake does necessitate Analog to Digital and Digital to Analog converters on either side of the CAT5/6 cable, but the CAT5/6 cable can be run for up to 330 ft with no repeaters [AES05], and is virtually immune to any type of noise, including noise caused through improper grounding or crosstalk. Professional digital snakes use sample rates from 48 kHz to 192 kHz [SNY08] and sample at 24 bits per second, allowing for capture of signals in the 20 Hz 20 kHz audio band.

Digital mixing consoles and digital audio snakes have both been around for several years, but they are produced by different manufacturers, and these manufacturers have had little

incentive to integrate their technology. While this did not lead to technical problems in mixing for a live audio event, converting back and forth between digital and analog domains had the potential to add in noise. This argument was valid years ago, but current technology allows audio engineers to minimize the number of conversions while taking advantage of the benefits offered by digital audio. One such example is the work between Yamaha, a digital mixing console manufacturer, and Aviom, a digital audio snake producer. Yamaha designed some of their digital mixing consoles with expansion ports, for both Yamaha peripherals as well as third party peripherals. Aviom designed an expansion card that plugs into a Yamaha digital mixing console and provides a direct digital interface between Avioms digital audio snake products and Yamahas digital mixing console [AVM08].

Directly interfacing a digital audio snake to a digital mixing console has a number of benefits, the most obvious being the reduction of the number of conversions between analog and digital. Another benefit is that plugging a digital audio snake directly into the digital mixing console reduces the amount of work required to setup for a show, and more importantly eliminates a major problem area for troubleshooting. When using analog audio, each channel has a separate connector, and it can be very easy to accidentally swap channels when connecting everything to the mixing console and effects processors. Since a digital audio snake is only a single CAT 5/6 cable the chances of accidentally plugging the cable into the wrong port are greatly minimized.

While the input to a digital mixing console is beginning to move towards all-digital, the output, or returns, which provide a signal to the amplifiers, remains in the analog domain. This can be seen by looking at various amplifier specification sheets and talking to audio engineers. Most audio amplifiers operate in the analog domain, directly amplifying an input voltage to provide a high power signal to a speaker. For these amplifiers it is necessary to convert to an analog signal before amplifying; otherwise the amplifier will be unable to decode a digital signal. The Class D audio amplifier, however, is designed to use MOSFETs for switching, which is much more efficient. This switching behavior is generally controlled by

either a Pulse Width Modulator (PWM) or Delta Sigma Modulator, two different modulation schemes that produce, at a minimum, a two state digital signal that can be used to control the MOSFETs. Unfortunately, the term digital is very broad, and leads to some incorrect assumptions. The most important thing to realize is that digital audio cannot be directly amplified by a digital amplifier. The characteristics of the signals are very different, a digital audio snake would actually contain anywhere from 16 to 384 audio channels in one direction, but a Class D audio amplifier is looking for a single audio signal in a PWM-type format. A special converter module would be required in place of a standard modulator to single out a specific channel and translate the signal into something the amplifier could use.

It is necessary to deviate slightly to explain how a digital audio snake works to understand where a project would need to begin to develop a converter module for a digital interface for a Class D audio amplifier. While a digital audio snake manufacturer could develop their own proprietary cabling, as mentioned above, most manufacturers choose to use existing technology, most notably CAT5 cabling, the same as that used in computer networks around the globe. Aviom only uses the Physical Layer, as defined by the Open Systems Interconnection Basic Reference Model (OSI Model), which consists only of the actual hardware that links two devices together. It is difficult to determine how much more of the OSI Model Aviom uses, however, as the second layer, the Data Link Layer, handles routing and error correction, which may be of limited use in a digital audio snake system. As it is impossible to determine exactly how Avioms system works, it is difficult to provide a starting point for creating a converter module. Unfortunately Avioms A-Net standard is a closed, proprietary standard, so while it is easy to understand from a system level, it would be difficult to reverse engineer the standard.

While it is difficult to be sure of the protocol specifics, some generalizations can be made based on available technology. A quick primer on network traffic is useful in understanding how Avioms digital snake might work. Traffic on the internet is divided into two major protocols, User Datagram Protocol (UDP) and Transmission Control Protocol (TCP). TCP

is used for applications in which data integrity is paramount, and there is time to resend lost or damaged packets. One example would be viewing a webpage; this is not a time sensitive action, so a web browser can request the server resend any missing packets. The other protocol, UDP, is less reliable, but eschews data integrity for speed. A real-time application, such as live audio through a digital audio snake, does not have time to resend dropped packets; it must be capable of handling dropped packets without problem. It should be noted that since a digital audio snake is an isolated and highly controlled environment, a connectionless protocol like UDP would probably not drop a significant number of packets, if any. Even if it did drop a packet, there is no way the system could recognize the missing information and resend it in time without instituting a delay, which is impossible for live audio.

Another digital snake standard is called AES50-2005, and is based off of a standard known as SuperMAC/HyperMAC developed by Sony Pro-Audio Labs [SNY08]. This standard is an open standard published by the Audio Engineering Society (AES) and designed for High-Resolution Multi-Channel Audio Interconnection (HRMAI), or in more common terms, a digital audio snake. Similar to Aviom, AES50-2005 uses CAT5/6 cabling as a physical layer [AES05]. One digital mixing console that has support for AES50-2005 is the Midas XL8, Midas Consoles first digital mixing console [MDS08]. The AES50-2005 standard is very well documented, which would be essential for developing an amplifier that would be capable of reading and converting an AES50-2005 audio stream. What is interesting about the AES50-2005 standard is that it uses a specially designed protocol, similar to TCP/UDP, but designed to function at a lower OSI level and minimize overhead. By reducing the amount of processing per frame the latency of the system is increased, which is one of the most important factors for live audio. Another benefit of AES50-2005 is that the individual audio streams are encoded using Pulse-Code Modulation (PCM), the advantages from PCM will be explained below [AES05].

Due to the proprietary nature of Avioms protocol, any project focusing on digital audio

should concentrate on the open AES50-2005 standard. Since the information here is relatively generic, most of it should apply to Avioms A-Net standard, but it is impossible to be certain as A-Net is a closed standard. The first step to amplifying digital audio is to develop a decoder, a subsystem that can read AES50-2005 (or A-Net) protocol. This would require a transceiver linked to some sort of microprocessor to tune into the proper audio channel. An excellent solution to this problem would be an embedded real-time Linux system. The I/O system block would only have to read in the AES50-2005 audio streams and output a single PCM audio stream. Some sort of user interface would be require to select the channel to amplify, but that could be as simple as binary dip-switches that microprocessor monitors. The dip-switch solution is actually used for concert lighting systems, which also use a digital control scheme. After a single audio channel is isolated the microprocessor would need to output that channel to be converted into a PWM-type audio signal.

The easiest way to convert the signal into a PWM-type audio signal would be to have the embedded system output a PCM signal. In fact, as mentioned earlier, AES50-2005 uses PCM to encode each individual audio channel, so converting to PCM would be as simple as tuning in to one specific channel and ignoring the rest. Once a single-channel PCM signal is created it would need to be converted into a PWM-type signal. There are numerous designs for PCM to PWM converters, and depending on the exact needs of the system, a design could be developed from scratch. This type of converter could be designed using a Digital Signal Processor (DSP) or could be implemented with analog circuitry. DSPs are usually much easier to troubleshoot as the code contained on the chip can be easily modified, but DSPs are complicated components and can be relatively expensive. On the other hand, analog circuits require more design work and are much harder to modify once the circuit is laid out on a Printed Circuit Board (PCB), but because individual analog components are extremely inexpensive, an analog circuit may be cheaper to mass produce. Regardless of whether a DSP or analog circuitry is used, the system could be tailored with various filters to minimize distortion and noise in the audio signal. An added benefit of using a PCM to

PWM converter is that an amplifier accessory could be a USB device that outputs a PCM signal from a personal computer directly to the amplifier. Directly connecting a computer through a USB port would require additional circuitry and computer software to emulate a sound card, but it would result in a final product with much greater capabilities than anything available on the market today.

The development of a Class D audio amplifier with any type of digital interface is inevitable because the professional audio market is slowly moving towards a digital standard. At this point in time, however, there is no single defined digital standard that every manufacturer recognizes, which is greatly hampering the movement to an all digital solution. It appears at this point that the only way a digital audio standard will be adopted is by various manufacturers beginning to support one standard. The AES50-2005 standard appears to be adequate for this task, but it has yet to be used in any large capacity. This would require cooperation between digital mixing console manufacturers, digital snake manufacturers, and amplifier manufacturers, something that does not appear likely to happen in the near future. If proof of concept designs are created they may spur movement towards a unifying standard, which would have an extremely positive effect on the professional audio market.

Below is a table to help summarize some of the more important differences between analog and digital audio with regard to the live audio market:

	Analog Audio	Digital Audio (AES50-2005)
Physical Cabling	Specialized "Snake" Large, heavy, expensive	CAT5 or Twisted Pair
Interface	Specialized snake head/tail. One XLR connector per channel	RJ-45 connector: Individual channels controlled by digital interface.
Noise	Susceptible to crosstalk and EMI	No noise picked up in cable run
Number of channels	Each additional channel requires more copper	CAT5-48 channels CAT6-384 channels
Length	Up to 500ft (150m)	Up to 330ft(100m) per leg