CONTROL OF A SATELLITE BASED PHOTOVOLTAIC ARRAY FOR OPTIMUM POWER DRAW

by

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DEDICATION

To my children: William, James, and Noah

ABSTRACT

This thesis analyzes the general performance and design requirements of photovoltaic(PV) systems, and specifically how they relate to the design of a system intended to supply power to a rotating satellite.

The PV array geometry was discussed, different DC-DC converter topologies were analyzed, and optimum array geometry and converter topologies were determined. The potential reference quantities for use in control of the system are examined. Due to its comparably greater linearity with respect to changes in apparent load and its relative insensitivity to insolation changes, voltage was determined to be the best reference quantity for use in stable tracking of the maximum power operating point of photovoltaic modules.

The preceding work is used to design and model a photovoltaic system for a rotating satellite ensuring the supply of the maximum available power as well as stable operation. Simulations of the system are performed at rotational velocities up to 300 rev/min and its behavior is analyzed to demonstrate the validity of the preceding work.

It was concluded that:

- parallel connected photovoltaic panels provide greater efficiency than series connected panels.
- Buck, Boost, and Cuk Converter architectures are best suited to PV applications
- PV Voltage is the best reference quantity for use in stable control of PV systems.

ACKNOWLEDGEMENTS

To God & My wife who have steadfastly supported me throughout this endeavor, and to Phoenix Electric whose donation has paid for a data acquisition card that will be used to perform experimental verification during the summer of 2008.

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LIST OF SYMBOLS

q	electron charge	1.6E-19 C
k	Boltzmann's constant	1.38E-23 J/K
n	emissivity coefficient	(varies by device)
T	temperature	K
V	voltage	V
I	current	A
I_O	output current	
I_{SC}	short circuit current (of a photovoltaic module based on insolation level)	
I_D	current through the internal diode of the photovoltaic model	
I_S	saturation current	
V_T	thermal voltage	~26mV @ room temperature
V_{OC}	open circuit voltage	

D	duty cycle	
V_O	output voltage	
V_S	source voltage	
T_{ON}	on portion of switching period	
I_L	current through inductor	
V_L	voltage across inductor	
I_C	current into capacitor	
V_C	voltage across capacitor	
I_P	pulsed current amplitude	
$V_{SETPOINT}$	reference voltage used to determine duty cycle	

LIST OF TERMS

Maximum Power Point (MPP): The V/I operating point (for a given insolation and temperature) at which a photovoltaic sources the maximum possible power.

Continuous Conduction Mode (CCM): The mode of operation in which the inductors in a DCC never cease to conduct (i.e. the ripple current is less than the average current through the inductor).

Discontinuous Conduction Mode (DCM): The mode of operation in which the current in one or more of the inductors in a DCC drops to zero during the portion of the switching cycle in which it is discharging.

Photovoltaic (PV): A cell or module (prepackaged group of cells) that can convert photonic energy into electrical energy. Typically these are made of silicon or other semiconductors doped so that EHPs generated from the photoelectric effect are separated in order to generate a flow of current.

Electrical Series Resistance (ESR): The series resistance typically used in modeling high frequency behavior of inductors and capacitors.

DC-DC Converter (DCC): A circuit that utilizes the energy storage capabilities of inductors and/or capacitors in conjunction with high frequency switches to effect the DC equivalent of a transformer. (i.e. to step up/down the voltage or current, or to match impedances between a source and load).

State of Charge (SOC): A measure of the portion of a battery's capacity available for use. Typically expressed in percent(%).

Electron-Hole Pair (EHP): The pair of charges (one positive and one negative) that results from an electron being dislodged from its place in a semiconductor lattice by an energetic photon.

Fill Factor (FF): The ratio of the maximum power available from a PV with respect to the product of open circuit voltage and short circuit current.

1.0 Introduction

The goal of this work was to study and simulate a control system for PV modules that would help draw the maximum power from a typical PV system powering a rotating satellite. Because the insolation changes seen by a rotating satellite are much more dramatic than for non-rotating satellites and land based systems, a control system capable of handling the conditions encountered on a rotating satellite will also be suitable for these applications. The applicability of the developed analysis to land based PV systems is of particular interest because:

1) The costs associated with burning fossil fuels for energy are continually increasing (and this is unlikely to change in the near future)[1].
2) Some applications require power in locations where connection to the grid and/or use of a local generator are uneconomical (much as with the satellite case above).

The photoelectric effect was observed several times in the 19th century as a secondary effect in other experiments[2][3][4], but the effect was not understood until Albert Einstein's 1905 explanation in terms of "light quanta"[5]. Even without understanding the nature of the effect, primitive solar cells were first made in 1883 by Charles Fritts. These cells were unable to produce useful amounts of power, but were primarily used to measure light intensity levels (e.g. in photography).

This changed with the development of the first silicon solar cells by Russel Ohl in 1946.[6] At that time the installation cost was around $300/$W_C$[1] and the best available cells were less than 6% efficient. These early cost factors prevented the use of solar cells from spreading beyond the realm of expensive novelty items and satellite power systems (where the military saw the value in using solar cells instead of conventional batteries). As a result, the military/space applications became the mainstay of the PV industry. The Arab Oil Embargo of 1973 reinforced the importance of finding alternative sources of energy and over the next decade the cost of PV modules was reduced to

1 W_C is used to denote the installed wattage capability under ideal conditions

around \$20/W_C. This cost reduction allowed solar cells to be used economically in power applications remote from conventional power grids such as oil rigs, water pumps, etc. for the first time.

Recently, PVs have seen use in even more remote applications as the costs have come down, such as wireless highway call boxes in California. Unfortunately, the cost of photovoltaics both in terms of dollars (currently about \$4/W_C) and space (at least 10m^2/kW under ideal conditions with current PVs) is still higher than the costs associated with fossil fuel burning plants and this has prevented photovoltaic systems from gaining widespread acceptance as a primary power source. Optimization of PV performance, combined with improvements in PV technology, is critical to overcoming these costs.

This project is intended to accomplish several tasks in support of PV optimization:

- The design tradeoffs in selection of geometry, topology, and component values are clarified.
- The control needs of an array of photovoltaic modules intended to convert the optimal charging power for a battery storage system is investigated.

The specific case involving an array of six photovoltaic modules installed on a rotating satellite is examined as a sufficiently general case, as it addresses control in the presence of dynamically changing insolation as well as determination of optimum operating point for a given state of battery charge.

Finally, the discussed material is used to design a power control module for existing photovoltaic modules. The system was assembled and measurements were taken of the assembled prototype to verify the preceding work.

2.0 Background

2.1 Physical Basis for the Photovoltaic Model

The operation of photovoltaic modules is a direct product of the interaction of the photoelectric effect with the semiconductor physics in diodes. Semiconductor materials are transparent to photons of light whose energy is below their bandgap energy. When an incident photon is of equal or greater energy (i.e. high frequency) than the bandgap energy of the semiconductor, it may “knock loose” a single electron from the crystal matrix and generate an electron-hole pair (EHP).

Photons with energy in excess of the bandgap do not cause multiple EHPs to be generated. The excess energy in dissipated as heat (because the EHP generated has greater kinetic energy). Furthermore, if the electrons generated are of sufficient energy they may escape the lattice entirely. The practical result of this is that EHP generation occurs most effectively at a specific wavelength (defined by the type of semiconductor material) and falls off as the wavelength of incident light increases.

The photoelectric effect increases the number of free electrons in the semiconductor lattice, decreasing the electrical resistance of the semiconductor in the presence of light; In effect, we have a light intensity variable resistor. [7]

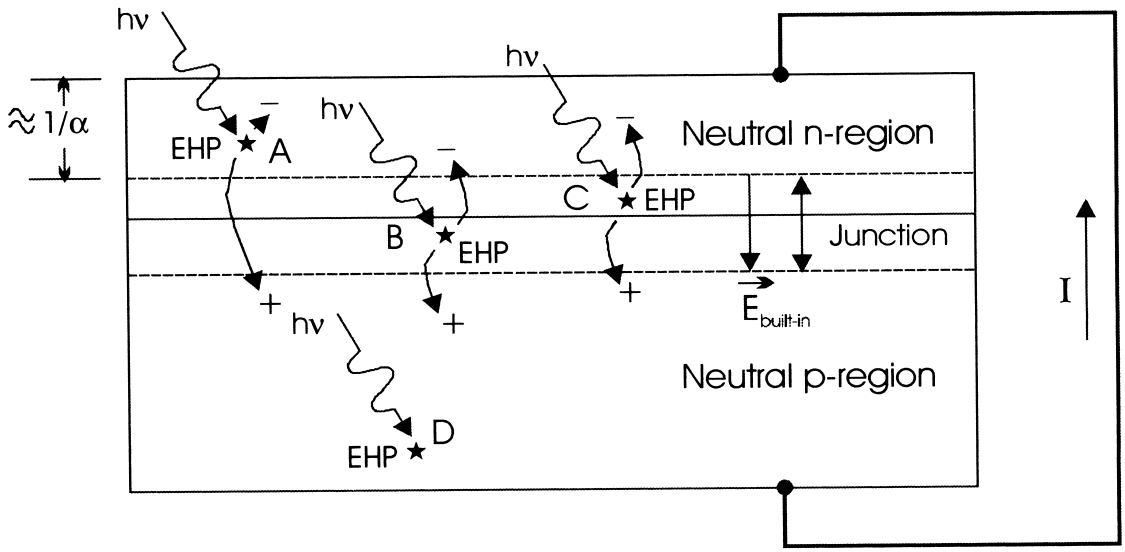

Fig. 2.1.1: Diagram showing the splitting of electron hole pairs (EHP) across the junction boundary to generate current flow. [7]

In pure (intrinsic) semiconductors, the EHPs generated eventually recombine into the lattice, instead of staying free indefinitely. The continued presence of light (insolation) will result in a higher average charge mobility, but an equalibrium is quickly reached where the greater generation of EHPs is matched by an increased recombination rate.

If the semiconductor has been doped so that there is a PN junction present, there is an additional effect that takes place. EHPs generated within the junction are swept apart by the built in electric field. Each carrier is deposited on the side of the junction where it is a minority carrier. It then diffuses away from the junction (toward the contacts). Even EHPs generated near (but not actual within) the junction can be subject to this effect if the majority carrier migrates into the junction before recombining. This results in a flow of current in the direction of the electric field, Fig. 2.1.1

2.2 Ideal PV Model

The combination of the two effects above (EHP generation and junction voltage) leads to behavior that can be modeled as a current source in parallel with a diode as shown in Fig. 2.2.1.

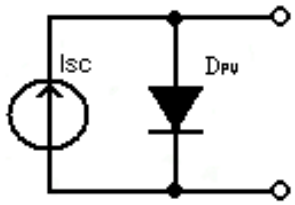

Fig. 2.2.1: Ideal PV Model

Where the value of the current source, Isc, is determined by the intensity and spectrum of insolation, the quantum efficiency of the cell material, junction area, and carrier lifetime.

The output current from the photovoltaic module can be described by the following equation:

$$I_O = I_{SC} - I_D = Isc - Is[\, e^{(\frac{qV}{nkT})} - 1\,] \approx Isc - Is\, e^{(\frac{V}{nV_T})} \qquad (1)$$

where:

I_O is the output current (A)
I_{SC} is the short circuit current (A)
I_D is the current through the parallel diode (A)
I_S is the saturation current of the parallel diode (A)
q is the charge of an electron (C)
V is the voltage across the PV cell (V)
n is the emission coefficient
k is Boltzmann's constant
T is the temperature (K)

The current through the diode is an exponential (instead of linear) function of the voltage. This causes the circuit to maintain a relatively constant current (or voltage, depending on the region of operation), except as the load approaches open circuit, as can be seen in Fig. 2.2.2.

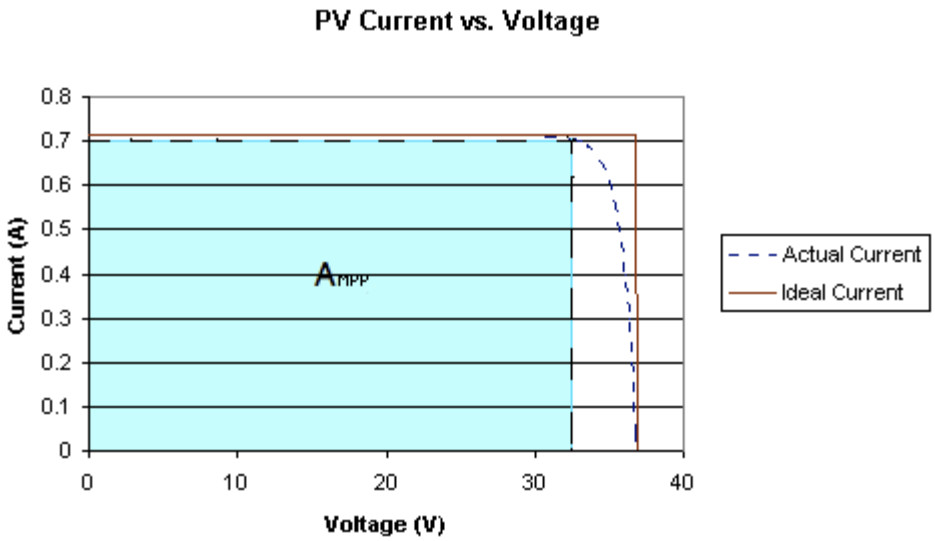

Fig. 2.2.2: Plot of PV current vs. voltage

One of the parameters frequently used to evaluate the efficiency of actual PV modules is called the fill factor(FF). Fill factor is calculated as the ratio of actual maximum power provided by the PV over the product of short circuit current and open circuit voltage.

$$\text{Fill Factor}\,(\text{FF}) = \frac{P_{MAX}}{I_{SC}\,V_{OC}} \tag{2}$$

It can be assessed visually in either of two ways:

- comparing the area of $I_{SC}V_{OC}$ with A_{MPP} shown in Fig. 2.2.2
- comparing the peak of the “Ideal Power” curve and the peak of the “Actual Power” curves in Fig. 2.2.3 (where the delivered power P=VI is shown as a function of output voltage).

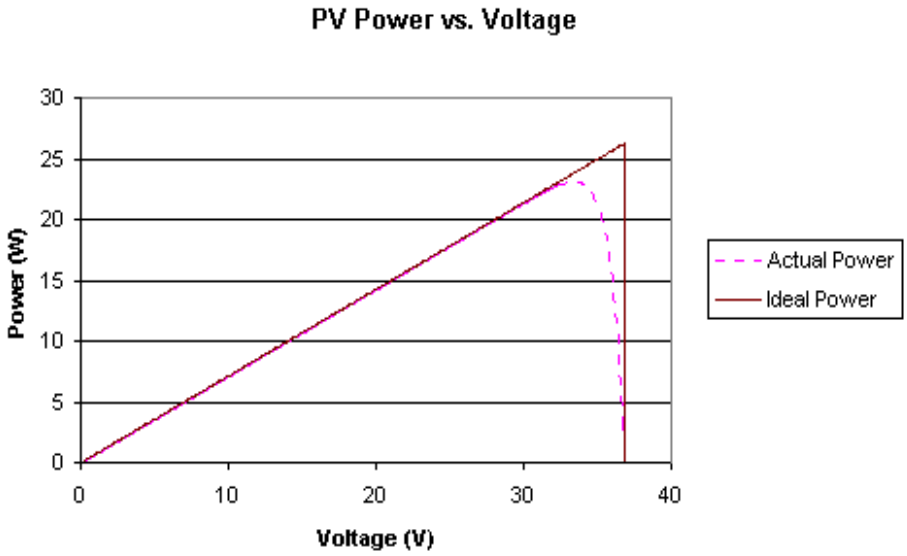

Fig. 2.2.3: Plot of PV power vs. voltage

An ideal photovoltaic module (as described by the ideal model above) would typically have a fill factor approaching 85-90%.

2.3 Sources of Loss and Nonideality

The ideal PV model shown in Fig. 2.2.1 is fairly accurate, but a more accurate representation requires the inclusion of resistances that can significantly affect PV efficiency. These are typically modeled as parallel(R_P) and series(R_S) resistances following the diode as shown in Fig. 2.3.1:

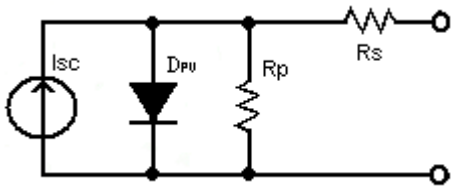

Fig. 2.3.1: Lossy PV Model

The addition of these resistances result in the fill factor of actual PVs ranging as low as 50%[7]. The model used throughout this thesis (except where explicitly stated otherwise) was provided by NASA and has the following values: $I_{SC(FULL)}$ = 0.713A, N = 38.524, R_P = 800kΩ, R_S = 1.6Ω.

2.4 Future Developments in Photovoltaics

Initially photovoltaic cells were made of large pure silicon crystals doped to generate large area PN junctions. Unfortunately the associated costs were very high in terms of dollars (manufacturing of large slabs of high purity silicon), area (due to low efficiency), weight (slabs of silicon can be heavy), etc. Much research has been done to address these concerns resulting in efficiencies as high as 40.7% in the laboratory[8].

Currently produced monocrystalline silicon cells have typically efficiencies less than 16%.[9] Polycrystalline and amorphous silicon are used to make less costly cells, but at the expense of reduced efficiency (~12% and ~6%, respectively). Other materials are used to generate photovoltaic cells, including: Cadmium Telluride, Cadmium Indium Diselenide, Cadmium Indium Gallium Diselenide, and Gallium Arsenide. Gallium Arsenide cells in particular are used in high efficiency multijunction cells, but (because of their high cost) are primarily used in niche markets (such as powering satellites) and for research.[10]

Another material that has been the source of great interest has been organic polymers. Organic cells have only reached efficiencies of 6% in the lab, but they are much less expensive to manufacture than traditional semiconductors[11].

Two additional methods of increasing PV efficiency are the development of cells using multiple junctions (separated by tunnel junctions) to take advantage of multiple bands of light, and the addition of phosphor layers to the front or rear of a single junction PV cell to up/down convert photon energy to match the bandgap of the cell. [12]

Finally, the use of concentrating lenses to focus light onto PV cells has been used to increase the effective efficiency by increasing the intensity of incident light. Lenses and the associated hardware are less expensive than PV modules so in some cases lenses have been used to concentrate the light of the sun as much as 1000x onto a much smaller PV module (which is actively cooled).

3.0 Design Elements

Operation and efficiency of a PV power system are affected by many factors. Some factors are determined by the design, such as PV array geometry, DC-DC converter topology, component selection (losses and stability), control variables& algorithm, PV characteristics, and battery/load(sink) characteristics. Other factors such as temperature can have a significant effect on the system and my need to be compensated for or contained. Finally, the actual source of power (light) is generally not under our control. For land based systems, the insolation varies as the earth rotates, with maximum available power at local noon, and as a result of weather and shade.

On a satellite, one of two situations is typically encountered. The satellite may be controlled in such a way as to continually present its PV panels directly to the sun (maximizing available energy and reducing the necessary complexity of the PV electrical draw system). Other satellites are spun up to several hundred rpms as a way to provide inertial stabilization. This reduces the available energy to the (now rotating) PV power system.

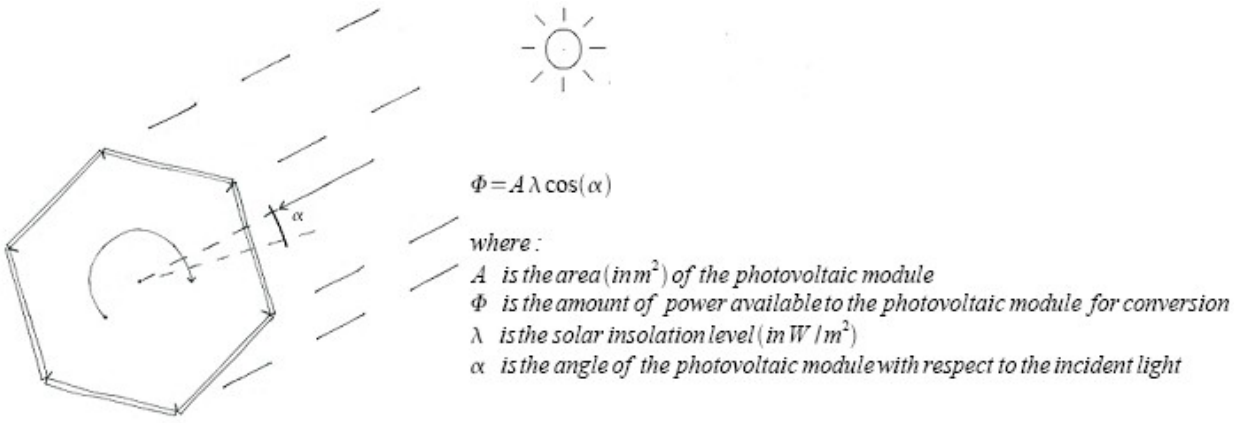

Fig. 3.0.1: A rotating satellite with six equispaced PV panels

Each PV module experiences a period of full intensity sunlight, followed by a period of effective darkness. This can be described using the cosine function where alpha represents the angle of the PV with respect to the plane of incident light, and each PV is phase shifted by its respective angle. For the hexagonal satellite, Fig. 3.0.1, the insolation can be plotted as shown in fig. 3.0.2

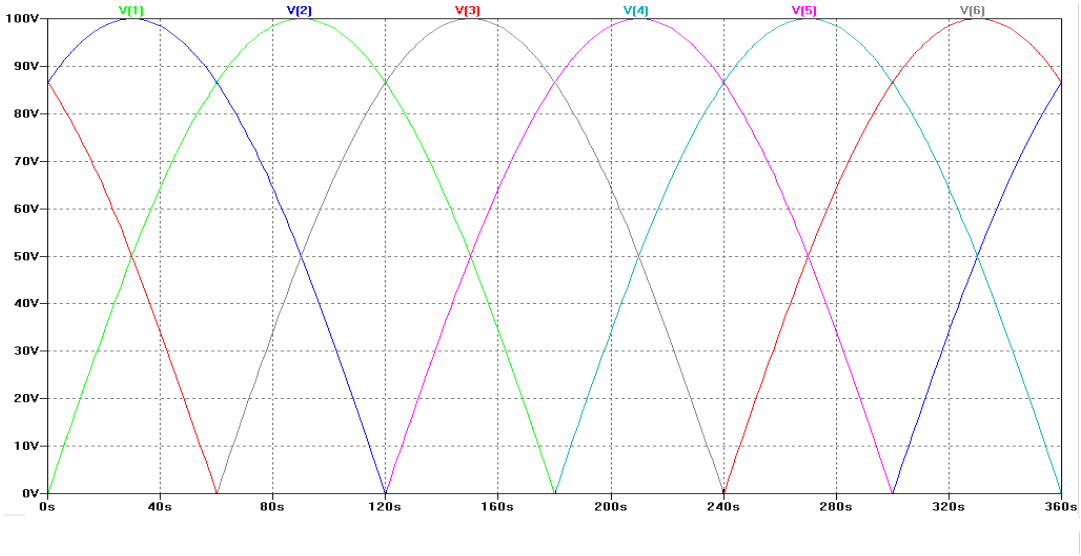

Fig. 3.0.2: Plot of insolations on each of the six PV panels as the satellite rotates. Plot was generated in SPICE, with percent insolation represented in volts and degrees of rotation represented in seconds.

This reduction in available insolation makes it particularly critical that the full available energy be captured. Therefore the control system must be able to respond fast enough to continually match the varying insolation as the satellite rotates. The following sections will discuss the pros and cons of each design decision as it impacts the system.

3.1 Array Architecture/Geometry

The way in which photovoltaic modules are interconnected can have a significant effect on the efficiency with which the available power is drawn from them. Two major design rules must be kept in mind:

1) **Each photovoltaic cell/module should have its own DC/DC converter stage.** Connecting photovoltaic cells or modules directly to the load is the least efficient method of extracting power from them.

Series modules, Fig. 3.1.1, will not supply the full available power, because series modules must all pass the same current. Differences in insolation, temperature, and/or module quality will result in different I/V curves for each module, and these differences will result in each module having a different MPP. Additionally, if any module is unable to supply the full current drawn, it will become reverse biased and dissipate some of the power generated by the other modules as heat. This condition results in significantly worse performance, and potential damage to the module.

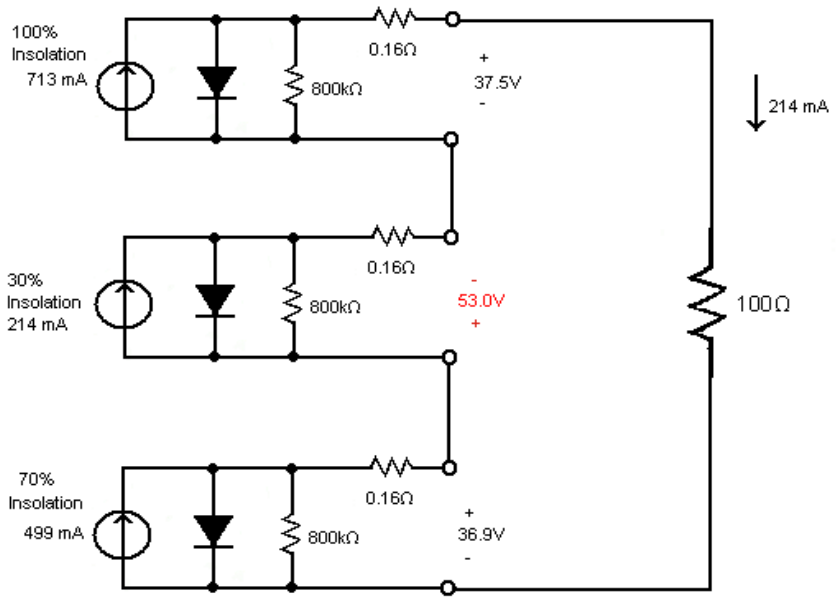

Fig. 3.1.1: Three PV modules connected in series with an equivalent 100Ω load. Shows reverse bias condition that results when modules do not receive equal insolation.

The conventional “solution” to this problem, Fig. 3.1.2, is to add bypass diodes in parallel with each photovoltaic module. These diodes prevent a weak module from becoming reverse biased by more than one diode drop (~0.7V). This has the dual effect of preventing damage to the module and reducing the power losses. Unfortunately, it still leaves the system without any contribution from the weak module.

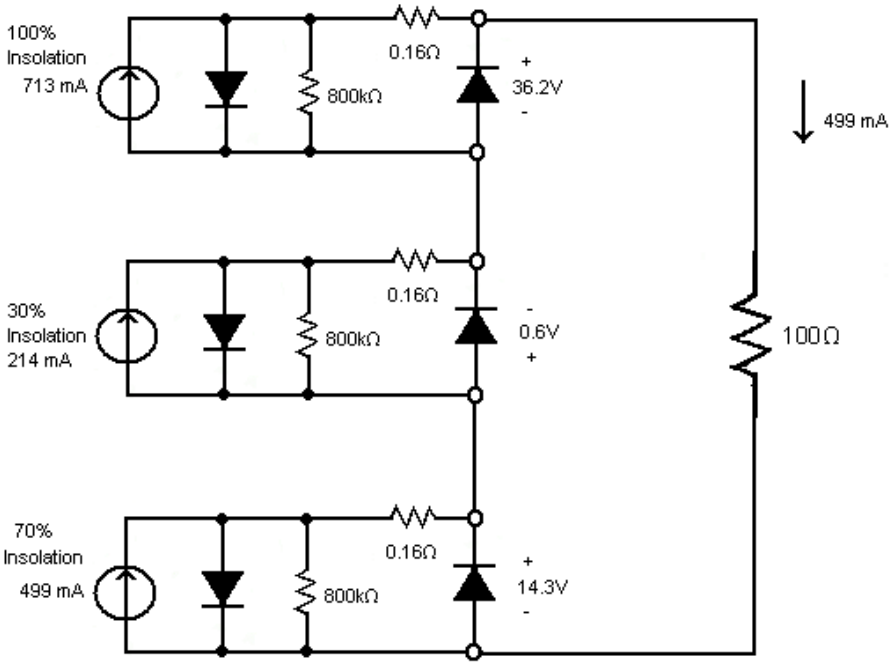

Fig. 3.1.2: Three PV modules with bypass diodes connected in series with an equivalent 100Ω load. Shows that bypass diodes significantly increase the available power to the load.

Parallel connected modules, Fig. 3.1.3, have a slightly similar problem; They do not operate at the same current, but they do operate at the same voltage. For the same reasons as series modules (insolation, temperature, and module quality differences), parallel modules have different MPPs. Since they are forced to operate at the same voltage, optimal power may be drawn from only a single module or even from none of the modules. Furthermore, if one or more of the modules is significantly weaker (is designed to operate at a lower voltage and/or is receiving less insolation) than the others, it will load down the other modules by sinking current that they might have otherwise provided (i.e. sinking power instead of sourcing it).

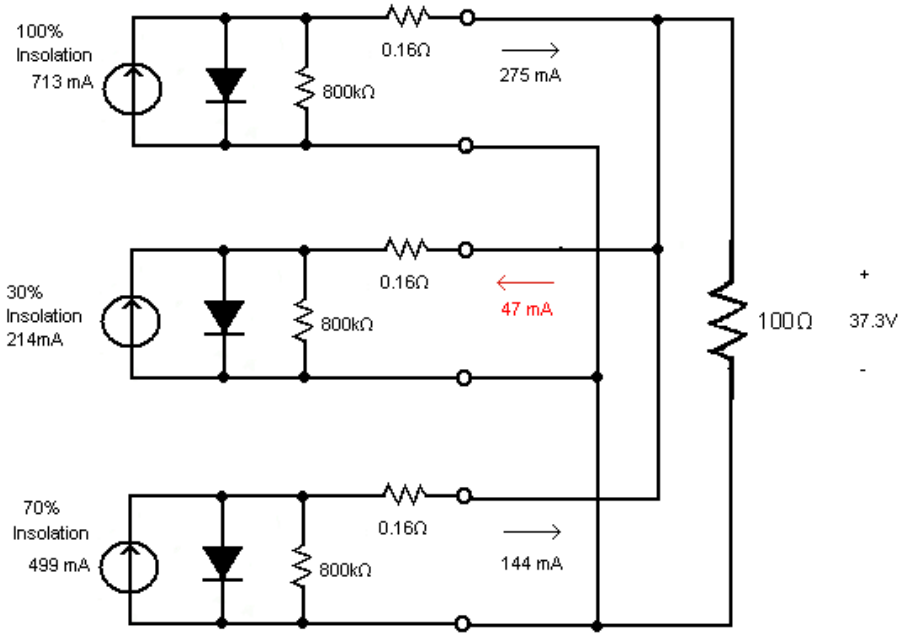

Fig. 3.1.3: Three PV modules connected in parallel across an equivalent 100Ω load. Shows the power sinking behavior that occurs when PV modules do not have equal insolation.

The actual power lost from parallel arrays is generally considered negligible, but there is some risk of damage/degradation to the PV modules due to power dissipation in the shaded modules. The solution to this is to add series blocking diodes to each module, Fig. 3.1.4. to prevent current flow into weak or damaged modules. This improvement reduces the risk of a shaded module becoming damaged and then becoming a permanent sink with respect to the rest of the array, but adds additional losses to all operating modules.

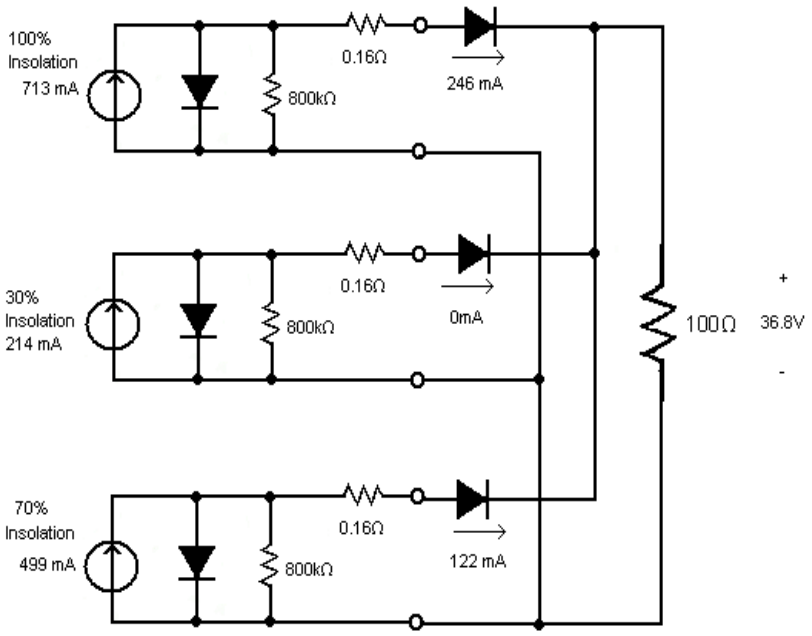

Fig. 3.1.4: Three PV modules with blocking diodes connected in parallel with an equivalent 100Ω load. Shows that current sinking behavior is prevented.

The addition of a DC-DC converter at the output of each PV module resolves the mismatch problems associated with both series and parallel connection of PV modules, because it acts as a DC transformer to adjust the V/I characteristics of the load (as seen by the PV modules) until each PV modules is operating at its own MPP. In Appendix A, simulations of direct connected systems are discussed in detail along with the conditions under which DC-DC conversion may not be necessary.

2)**Photovoltaic/DC Converter Stages should be arranged in parallel arrays if possible.**

PV-Converter stages can be connected in any combination of series or parallel and retain stable operation. However, parallel arrays cause less power loss than series arrays. In a parallel array, each stage sources power directly to the battery/load. In a series array, each stage sources power to the battery/load *through the other stages in the array.* This means that losses in the output stages of each DC-DC converter are compounded in series arrays.

Note that in particular cases where high voltages are needed, series arrays of stages may be the best solution (or even critically necessary). This would be the case if parasitic losses prevent the DC-DC converter from operating at the desired output voltage without excessive losses, Fig. 3.1.5. In these cases, parallel arrays of two or three series stages may generate the best results.

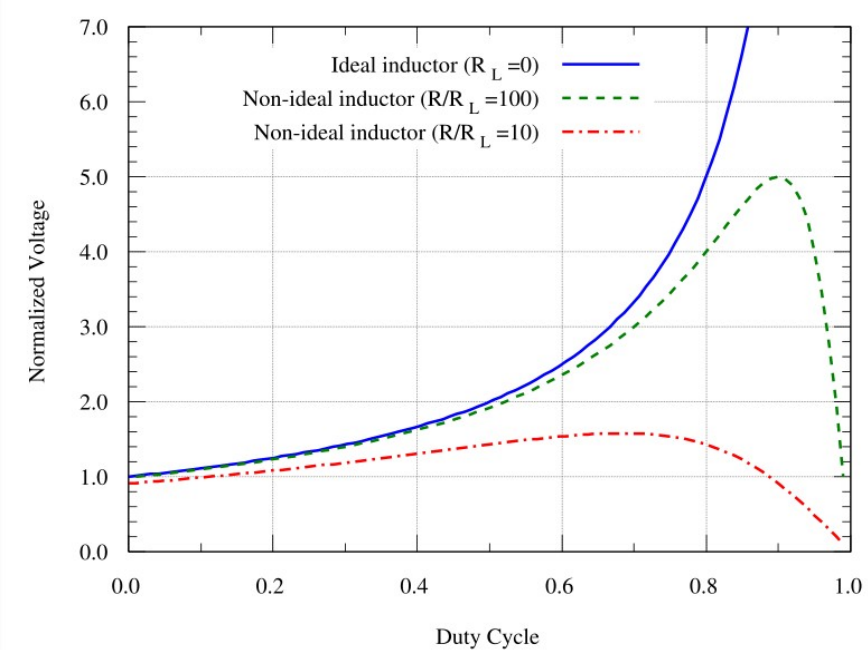

Fig. 3.1.5 Parasitic Losses in Boost Converter. [13] R is the load, R_L is inductor resistance

3.2 DC-DC converter topologies

The choice of what DC-DC converter topology to use can have a significant impact on both efficiency and effectiveness. Several types of DC-DC converters are examined to show under which circumstances (if any) they should be used.

3.2.1 Buck Converter

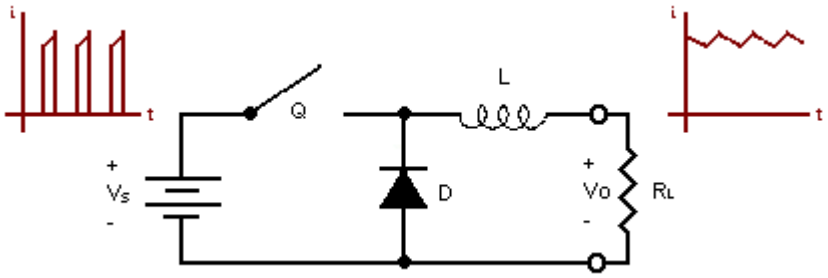

Fig. 3.2.1.1: Buck Converter Circuit Representation with input and output current waveforms shown.

The Buck Converter, Fig. 3.2.1.1, is one of the simplest converter architectures available. It consists of two switches (typically a transistor, Q, and a diode, D), and an inductor, L. The relatively small number of components allows the buck converter to reach high levels of efficiency (>95% depending on the application).

In continuous conduction mode, buck converters step down the output voltage according to the following expression[14]:

$$Vo = DVs \tag{3}$$

Where:
D represents the PWM duty cycle of the transistor Q.
Vs represents the source voltage.
Vo represents the output voltage.

This topology works in both series and parallel PV arrays *provided that the stage output voltage is lower than the source voltage*. If this condition is not met, the PV-Converter

stage will be incapable of sourcing power to the system. This is potentially a major drawback, but may be acceptable if the increased efficiency during times of high insolation outweighs the loss of power sourced during periods of intermediate/low insolation.

Another concern relating to the buck architecture is the pulsed input current of the buck converter. To ensure that PV operation remains near MPP (instead of slewing between OC and SC operation) additional input filtering is required in order to eliminate this condition. This input filtering introduces additional losses and stability concerns which need to be addressed in the design of the control system.

3.2.2 Boost Converter

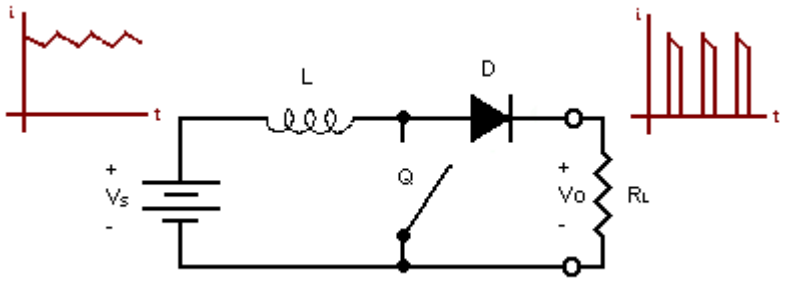

Fig. 3.2.2.1: Boost Converter Circuit Representation with input and output current waveforms shown.

The Boost converter, Fig. 3.2.2.1, is very similar to the buck converter in concept. The same components are used, but they are connected in a different order so that a voltage boost instead of a voltage drop is obtained. The equation defining operation in continuous conduction mode is[14]:

$$Vo = \frac{Vs}{(1-D)} \tag{4}$$

The boost converter is limited similarly to the buck converter, except that it is limited to providing voltages larger than the source voltage. If the battery or other load is at a lower voltage than the PV module, the converter can (at best) provide a DC connection between the module and load. This would both load down the PV module and add

additional losses (because of the inductor and diode in the current path). Provided the battery voltage relatively high voltage battery is used this should not be a problem, as batteries do not typically drop significantly in voltage unless they are nearly dead.

Another difference between the boost and buck converters is that the boost converter has pulsed output current, but the input current is only rippled. This eases (or even eliminates) the need for additional input filtering, but potentially adds the requirement of output filtering (depending on the load characteristics).

3.2.3 Buck/Boost Converter

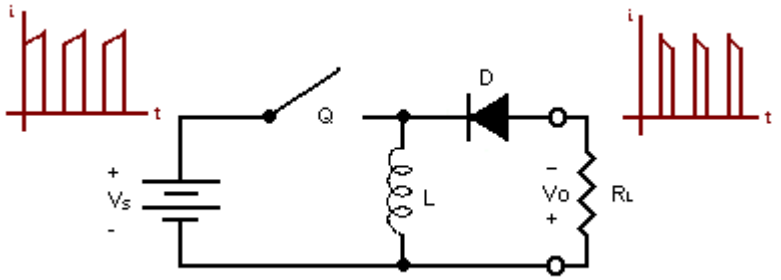

Fig. 3.2.3.1: Buck-Boost Converter Circuit Representation with input and output current waveforms shown.

The Buck/Boost converter is a hybrid of the buck converter and the boost converter. The components are again the same, but rearranged yet again to allow output voltages both above and below the source voltage. This trait is especially useful in some PV systems, because it allows the converter to extract the full available power from a module regardless of the current insolation level or battery charge state The equation for this converter type in continuous conduction mode is[14]:

$$Vo = \frac{D}{(1-D)} Vs \tag{5}$$

A potential disadvantage in some situations is that the output voltage is inverted with respect to the source voltage. This is not a problem with independent power sources such as PV modules, because they need not be explicitly ground referenced to operate correctly, and the negative terminal of the PV module can be connected to the positive

terminal of the charge device (e.g. battery). For high voltage systems this could be a safety issue and precautions may need to be taken to reduce the shock hazard by guarding access to conductive parts of the PV modules that are at high voltage.

Another disadvantage is that, like the boost converter, the buck-boost topologies has pulsed output current, and like the buck converter, it has pulsed input current. This means that it may require additional filtering on both the inputs and outputs (depending on the application).

3.2.4 Ćuk Converter

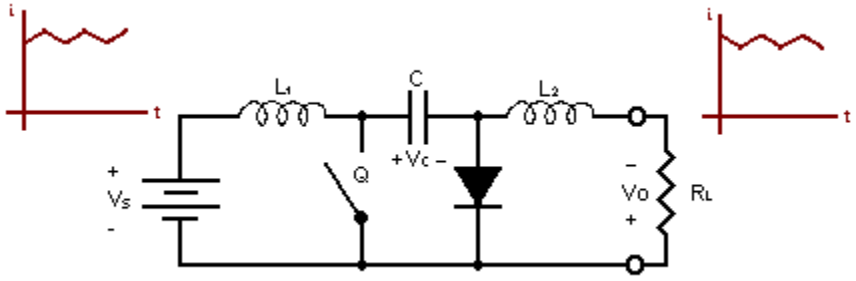

Fig. 3.2.4.1: Ćuk Converter Circuit Representation with input and output current waveforms shown.

The Ćuk converter is named for Slobodan Ćuk of the California Institute of Technology.[15] It is the result of applying the duality principle to the buck-boost converter to use a capacitor instead of an inductor as the primary energy storage device. As a result, the DC transfer function is nominally the same as that of the Buck-Boost converter, Eq. 5.

An advantage of the Ćuk converter topology is that the current pulsing occurs within the converter itself and both the input and output currents are not pulsed. Furthermore, if integrated magnetics are used, the input or output current can (theoretically) be nullified as the ripple is transferred to the other side of the converter.[16] Because only one capacitor suffers the losses associated with (internal) current pulsing, the Ćuk converter is more efficient than a filtered Buck-Boost converter.

3.2.5 SEPIC Converter

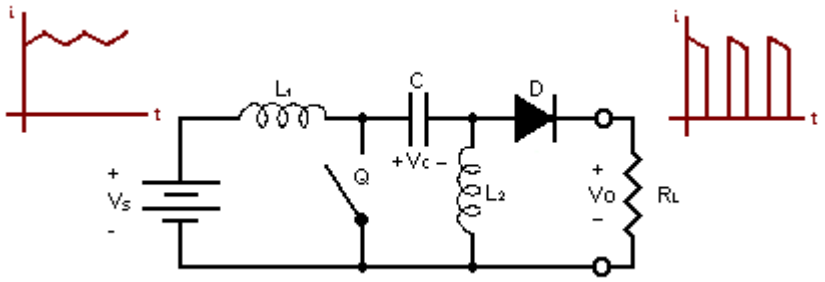

Fig. 3.2.5.1: SEPIC Converter Circuit Representation with input and output current waveforms shown.

The SEPIC (Single Ended Primary Inductor Converter) is very similar to the Ćuk converter, except that the secondary inductor, L2, and the diode, D, have been swapped so that the output polarity is the same as the input polarity. This can be an advantage in certain applications, because the negative terminals of both the input and output are common. Unfortunately, this has the negative side effect of reinstating pulsed current on the output.

3.2.6 Zeta Converter

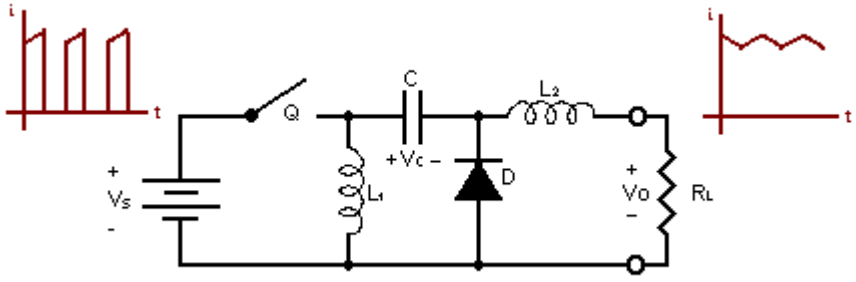

Fig. 3.2.6.1: Zeta Converter Circuit Representation with input and output current waveforms shown.

The Zeta converter is another variation off of the Ćuk converter, in which the input inductor and switch are swapped and the polarity of the output diode is reversed. This has the same advantage as the SEPIC (i.e. polarity is the same at input and output), but has the disadvantage that the input current is pulsed instead of rippled. This topology also requires a high side switch (either a P-Channel FET or an N-Chanel FET with a

high side driver). This topology can work well when integrated with another topology (such as the buck-boost) to generate both positive and negative output rails.

3.2.7 Comparison of DC-DC Converter Topologies

It would be ideal if one topology was generally superior to all others. Unfortunately, this is not the case. Each of the topologies has its own merits which make it suitable for different applications.

The buck converter is generally the most efficient topology, but it is not capable of sourcing power to a load whose voltage is greater than the source voltage. In order for this to be acceptable in a PV system, the insolation and PV characteristics must be such that V_{MPP} is greater than the load voltage nearly all of the time. The PV can continue to source power as long as the load is less than V_{OC}, but the higher the sink voltage is (relative to source) the less efficiently the PV array is utilized. The increased efficiency of this topology is desirable, but it is only relevant if the PV voltages are significantly higher than the output storage voltages, such as when charging a 12V parallel battery array from 28V PVs.

The boost converter is nearly as efficient as the buck converter, but has the opposite restriction. The output voltage must be higher than the source voltage. One advantage over the buck converter is that if the preceding condition is not met, the boost converter can still source power (although the power sourced will be non-optimal, because the PV will be excessively loaded down). Additionally, if the energy storage medium can accept pulsed current, no external filtering is required (which will increase efficiency and controllability).

The buck-boost and zeta topologies have advantages in that they can easily be merged into a single circuit that generates both positive and negative rails. Unfortunately, this benefit is not nearly as relevant for the purposes of optimizing power draw from PVs as it is within circuit designs. Both of these converters do overcome the high vs. low output voltage dilemma of the buck and boost topologies, but they are outperformed by the Ćuk and SEPIC topologies which are more efficient.

Like the buck-boost and zeta topologies, the Ćuk and SEPIC topologies can efficiently transfer power to a load regardless of its voltage relative to the source (disregarding parasitic losses at high relative differences). This makes these topologies ideal when the voltage of the PV arrays varies significantly and or operates near the voltage of the storage system. There are three main differences between these topologies:

1) The input and output polarity of the SEPIC topology are the same. This is not usually a technical requirement (although it may be easier for bookkeeping purposes), but may be relevant in some special cases.

2) The voltage across the primary energy transfer capacitor is the sum of the input and output voltages in the Ćuk converter, but the difference between them in the SEPIC. This means that a lower capacitance can be used in the Ćuk converter while maintaining continuous electrification, but that a lower voltage capacitor can be used in the SEPIC. The specific application will determine which is of greater value.

3) The polarity reversal of the output components in the SEPIC topology causes it to lose the highly desirable trait of continuous output current (present in the Ćuk topology).

For the reasons mentioned above, buck or boost topologies should be used where possible (because of their greater efficiency and simplicity). In the remainder of cases the Ćuk topology should be used, because it maintains continuous input and output current (requiring less filtering and thus leading to greater efficiency and controllability).

3.3 Selection of components

The selection of components is a critical part of effective design. The following sections will go over the reasoning and calculations used to select the critical components of the DC converters used in this thesis.

3.3.1 Selection of Energy Transfer Component(s)

While it is not necessary that the DCC operate in continuous conduction mode (CCM), it is generally desirable, because the simple operation is easier to understand/control and losses are usually smaller than in discontinuous conduction mode (DCM). In the buck and boost topologies, only one component is relevant to the determination of CCM: the primary inductance, L. In the Ćuk topology, the three power transfer components, L_1 (primary), C, and L_2 (secondary), must be sized. These component values must be determined before the input and output filter components (if used), because they determine the voltage/current ripple on the input and output of the converter core. For instance, the larger the inductor (in a buck converter), the smaller the output filter capacitor (if present) needs to be, because of the decreased output current ripple.

In order to remain in continuous conduction mode, the peak-peak current variation in an inductor must be less than twice the average current through the inductor under the conditions specified, Fig. 3.3.1.1.

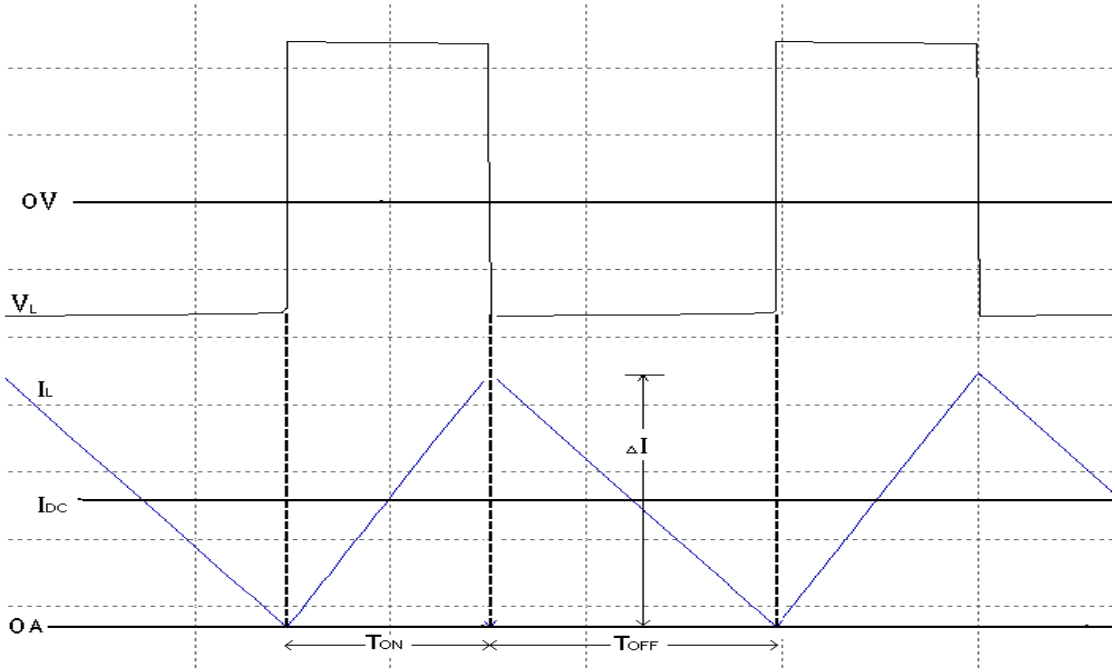

Fig. 3.3.1.1: Voltage across Inductor and Current Through Inductor vs. Time, showing the relationship between T_{ON}, I_L, and V_L. Magnitude of V_L is not shown, because it is topology dependent (and specified in the chart on pp.25).

The minimum inductance that ensures continuous conduction is defined by the following equation:

$$L \geq V_L \frac{T_{on}}{2I_L} \tag{6}$$

Where V_L is the voltage across the inductor, T_{on} is the duration of the on portion of the switching cycle, and I_L is the current sourced by the PV module.

The voltage across the inductor during T_{on} can be determined as follows:

Buck Converter	L	Vs - Vo
Boost Converter	L	Vs
Ćuk Converter	L_1	Vs
	L_2	-Vs

In the Ćuk topology, the capacitor must also remain energized continuously. In order to ensure that this is the case, the following equation (dual to Eq. 6) could be used:

$$C \geq I_C \frac{T_{on}}{2V_C} \tag{7}$$

Where V_C is the difference between the input voltage and the output voltage (i.e. sum of magnitudes), T_{ON} is the duration of the on portion of the switching cycle, and I_C is the current out of the capacitor (because the capacitor discharges, charging L_2 during the on portion of the switching cycle).

Unfortunately, unless the value of the secondary inductor is chosen to maintain relatively steady current (i.e. well above the minimum value for CCM), the current through the capacitor cannot be assumed to be static (as was the assumed for the voltage across the inductors). Because the capacitor is charging the secondary inductor, the capacitor current is equal to the secondary inductor current (and is thus time variant). Furthermore, the change in secondary inductor current is based on the capacitor voltage (invalidating Eq.6 unless a larger than minimum value for C is selected). To calculate the values for C and L_2 without these assumptions is (at minimum, assuming no output filter/load effects) a second order differential equation. Fortunately, if we are willing to accept a small amount of error we can assume that load effects are negligible. In that case the capacitor, C and inductor, L_2 form a resonant

circuit, and therefore the on time must be equal or less than one quarter of the resonant period of the capacitor, C and inductor, L_2 (i.e. before the first resonant zero crossing), Fig. 3.3.1.2:

$$C \geq \frac{4T_{ON}^2}{(\pi^2 L_2)} \tag{8}$$

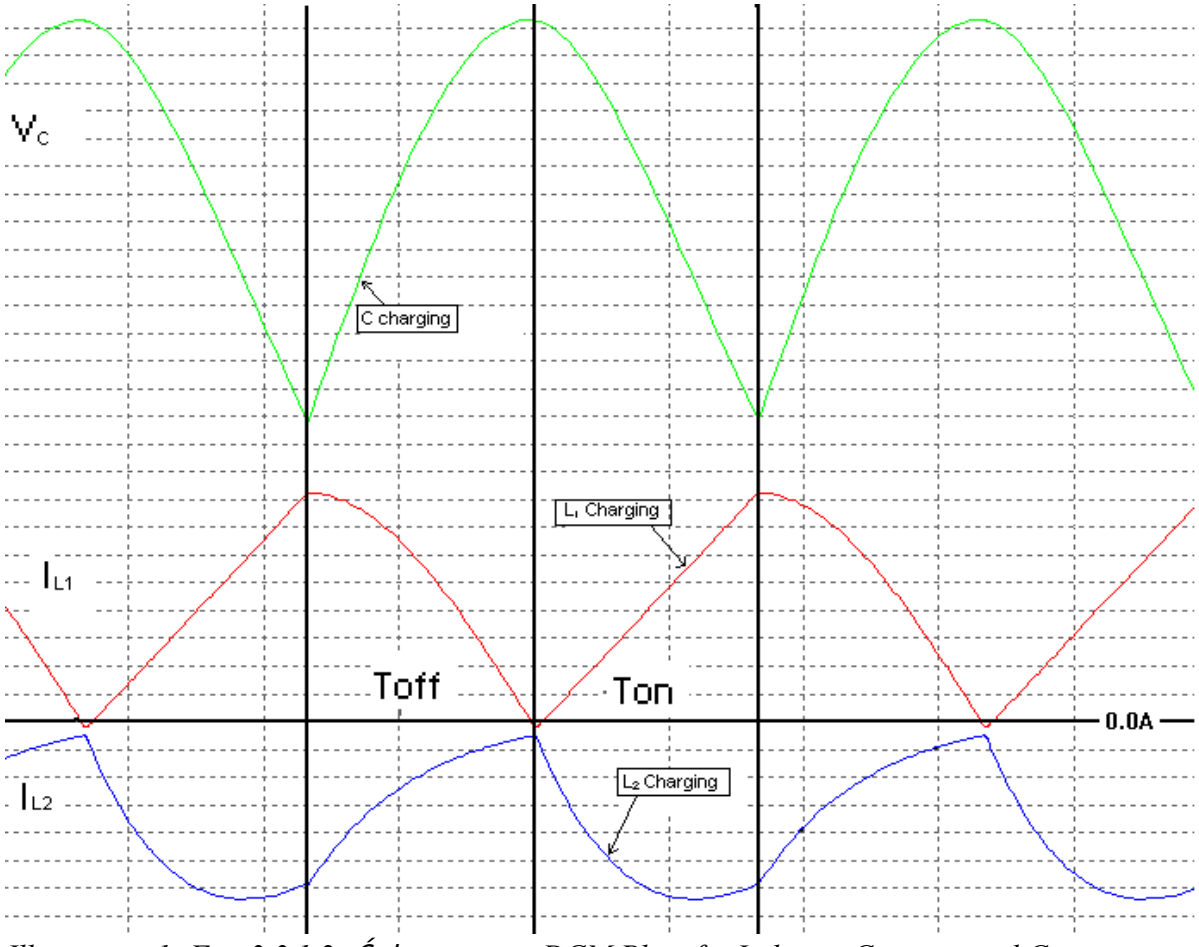

Illustration 1: Fig. 3.3.1.2: Ćuk converter DCM Plots for Inductor Currents and Capacitor Voltage

While it may be tempting to use the minimum inductor and capacitor values for CCM during MPP operation, it is often desirable to use larger value components. For example, Eq. 8 will typically result in very small values for C. Use of a capacitor value 10 times larger than the minimum is often easily realizable and results in a capacitor voltage that should ripple less than 1%. Larger inductance values for L_1 and L_2 can be even more valuable by a) ensuring that the converter retains CCM operation at lower insolation levels, and/or b) reducing ripple current so that external filtering needs are reduced (or even nullified).

In addition to the main component value(s), there are additional electrical characteristics to be considered in selecting the inductors and capacitors: Saturation current (for inductors only), self-resonant frequency, and series resistance. The nonlinear behavior of inductors in saturation and either inductors or capacitors at frequencies approaching/exceeding self resonance are harder to control and make it difficult to predict ripple behavior. The series resistance is important as it can be a major component of the system losses.

3.3.2 Selection of Input Filter Components

The operation of a DC converter is bimodal and power will be drawn from the PV based on the open and closed conditions rather than the average condition. If the DC converter topology chosen has pulsed input current, additional input filtering is necessary to ensure that the PV operates near MPP instead of fluctuating from one side of MPP to the other. Even if the topology draws rippled current instead of pulsed current, either the primary inductor must be large enough that the ripple does not significantly reduce power draw, or external input filtering must be added.

Before attempting to calculate the values of input filter components, the maximum allowable source ripple must be determined. The first step in this determination requires taking the derivative of the PV power equation (Eq.1 multiplied by V):

$$\frac{dP}{dV} = Isc - Is\left(1 + \frac{V}{nV_T}\right) e^{\left(\frac{V}{nV_T}\right)} \tag{9}$$

Eq. 9 contains terms both with and without exponentials and thus does not have a simple analytical solution, but we can solve for V by iterative calculation or by generating results across a range and selecting outer bounds of the solution. By setting the equation equal to zero, we can find the value of V at the point of maximum supplied power (i.e. MPP). We can then use V_{MPP} to determine I_{MPP} and the actual value of maximum power. If a range of values was used to determine MPP, the same range can be inspected to determine how much variation in voltage is acceptable. Furthermore, once an acceptable source voltage ripple is known, determination of acceptable current ripple is trivial.

Once the acceptable source ripple is known, it must be determined what input filtering is needed. If the topology being used does not have pulsed input current (e.g. boost and Ćuk topologies), it is possible to meet the input ripple requirement without any external filter by using an appropriately sized primary inductor. If the topology has a pulsed input current (e.g. buck topology), or if smaller inductors are desired, then input filtering is needed.

The first filter component to be defined is a shunt capacitor. This is required for pulsed current topologies, because a series inductor without a shunt capacitor would not have a current path during the off portion of the switching period, T_{off}. If the topology does not have pulsed current, a shunt capacitor is not necessary, but adding a series inductor without it would be equivalent to simply having a larger primary inductor (which has already been decided against by using filtering).

The shunt capacitor in the input filter performs a dual role. It reduces the effects of input voltage fluctuation on the operation of the DC converter, and it helps reduce the ripple on the source. If the current is pulsed, the required capacitance for a given ripple voltage can be found by rearranging the standard capacitor equation:

$$C_{SHUNT} = \frac{I_P T_{ON}}{\Delta V_C} \tag{10}$$

Where I_P is the maximum pulse current, and ΔV_C is the desired voltage ripple.

Because the current is pulsed, this case is the dual to the inductor CCM equation, Eq. 6, shown graphically in Fig. 3.3.1.1. If voltage and current are interchanged in Fig. 3.3.1.1, the only difference is that the purpose of the shunt capacitor is to maintain low ripple rather than simply to be continuously energized.

If the current is not pulsed, the primary inductance determines the initial current ripple. This allows us to obtain the desired shunt capacitance by substituting the inductor equation (used to determine current ripple from the primary inductance) into the capacitor equation (by setting the ripple as the total capacitor current):

$$C_{SHUNT} \geq \frac{V_S T_{ON}^2}{L_1 \Delta V_C} \tag{11}$$

This approximation does not include ripple added due to resistive losses in the capacitor series resistance (ESR), but it should get a close approximation of the required value (assuming relatively low ESR capacitors are used).

If the required value of C_{SHUNT} is too high (either not available or because of controllability concerns), a smaller value can be used by adding a series inductor to further filter the source ripple. The series inductor can be calculated using the following equation:

$$L_{SERIES} \geq \frac{T_{ON} \Delta V_C}{\Delta I_L} \tag{12}$$

This process of adding inductors and capacitors to the input can be continued to generate higher order input filters composed of lower value components. This can have both benefits and disadvantages as follows:

1. Each added component adds a pole to the system (increasing controllability concerns)
2. Each component adds losses to the system (reducing efficiency)
3. Filters composed of lower component values may be physically smaller (which may be a benefit in space constrained designs)
4. Poles of low value components are at higher frequencies (a potential advantage in controllability as it allows the system to settle faster).

3.3.3 Selection of Output Filter Components

Conceptually, any desired output filtering can be determined in the same way as the input filtering. The same equations apply, although they are applied to the output current instead of the input current waveforms.

If the output current is pulsed (e.g. in a boost converter), Eq. 11 would be used to determine the shunt capacitor needed to filter the pulsed current and allow a rippled output voltage. As with the input filtering, a series inductor may be added to improve filtering using Eq. 12. The likelihood of needing a series inductor is even higher on the output, because the storage device (e.g. battery) will be very low impedance (and will thus allow very high current ripple for a given voltage ripple).

As with the input filtering, adding higher order filters add extra poles (and zeros) to the system which can have negative effects on controllability, but since the values can be reduced with each new component, the unpleasant control problems can be pushed into higher frequencies that can be avoided during normal operation.

It is worth remembering that when multiple DCC stages are used, the output ripple of each stage contributes to the total system output ripple. The easiest way to ensure compliance with the output ripple specification would be to allot equal portions of the allowed output ripple to each stage and assume that each DCC will have identical ripple which adds directly. This is a very conservative approach which will likely result in filter components that are somewhat higher than absolutely necessary, but it will ensure that total system output ripple is acceptable (especially considering that in a rotating satellite half the PV modules may be in darkness at any given time).

A technique that can be used to reduce the output ripple is to arrange for the ripple of each output stage to partially cancel the ripple of the other stages. This can be accomplished by assigning each module a distinct offset within the switching period (so that T_{ON} begins at a different time in each module). This technique results in significantly less output ripple, but requires a common phase reference for each module's PWM circuit (preventing the use of a simple independent oscillator).

This technique is especially effective when similar insolations will be present on all of the modules (such as in terrestrial applications) where the ripple cancellation can be near total. Even when the modules will be operating at different power levels (and thus different duty cycles), such as on a rotating satellite where each module has distinct insolation, the cancellation effect can be striking.

As with selection of the primary energy transfer components, selection of filter components should take into account other parameters than just reactance. The self-resonant frequency of filter components can be critically important in ensuring that the filter behaves as expected. Preferably component values should be selected which will result in a resonance frequency that will not be excited by either the switching frequency, the expected insolation changes, or their harmonics.

Another important factor that can be easily overlooked is the contribution of ESR to ripple (in addition to inefficiency). This is especially true in capacitors that are filtering the pulsed current at the input of the buck or the output of the boost topologies. Care should be taken to ensure that ESR is minimal to prevent these ripple contributions from being substantial, because ESR ripple across these capacitors is determined by Ohms Law and is directly added to the capacitive ripple.

Finally, the voltage characteristics of the capacitors should be considered not only to ensure that damage does not occur (i.e. maximum voltage rating), but also to ensure that they will filter as expected (i.e. reduction in capacitance under DC bias voltage as a result of dielectric saturation). Monolithic chip capacitors can have very low ESR, but higher capacitance values may need to be selected to ensure proper behavior under DC bias if X7R, X5R, or similar materials are used.

3.3.4 Selection of Switches

Perhaps the most important part of the system is the choice of switches. Typically a combination of a transistor and a diode is used, because the transistor can operate at much higher frequencies and the diode will immediately conduct under the correct circumstances (rather than needing to be synchronized). Sometimes a transistor will be used in parallel with the diode to reduce losses once conduction has begun. Power MOSFETs are currently the most likely candidate for use as transistor switches because of their high switching speeds (given a suitable driver), and their very low ON resistance.

In looking at MOSFET datasheets, the primary specifications of interest are:

- $R_{DS(ON)}$: On resistance directly impacts power loss during on cycle time.
- I_{DSS}: Off current directly impacts power loss during off cycle time.
- $Q_{g(TOT)}$: Total gate charge combined with driver specs determine switching speed. It is important to ensure that switching speed is significantly smaller than switching period to ensure that the converter operates as expected and to reduce switching losses (which are proportional to switching frequency).
- Package: In commercial use it may be necessary to limit the size of components, making it important to be aware of the transistor package. Many power MOSFETs are currently available in SOIC-8 package which is compact and has relatively short leads (leading to lower gate lead inductance). Conversely, for hand built equipment large easily soldered components such as TO-220 packages may be beneficial).
- Thermal Dissipation: Make sure that the device chosen has a safe operating region that encompasses the expected range of system use.

3.4 Selection of PV Controls

The goal of the system is to optimize power drawn from the PV module. This means maximizing power draw when the battery is discharged, and then reducing the draw to maintain battery charge based on usage.

Fig. 3.4.1, showing the relationship between output power and duty cycle, is plotted from a spreadsheet attached in Appendix B, where the steady state values for a fully insolated PV module were generated with respect to load. Columns were added to calculate the duty cycle of a Ćuk converter that would result in this steady state condition when sourcing to a 12V battery. The relationship between provided power and duty cycle was examined for buck and boost topologies as well and the relationship was found to be qualitatively similar (although numerically different).

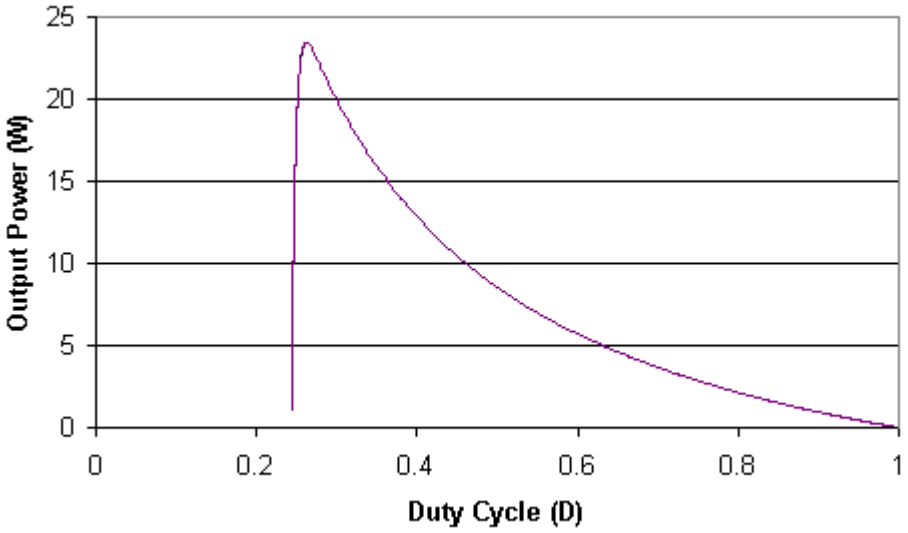

Fig. 3.4.1: Plot of power sourced to a 12V battery from a fully insolated PV module vs. the duty cycle of an intermediating Ćuk converter

We can see from Fig. 3.4.1 that the power increases precipitously from a duty cycle of 0.24 to 0.26, after which it falls off from 0.26 to 1. In the lower duty cycle region the DCC underloads the system, resulting in reduced current draw (and thus less power). In the higher duty cycle region the DCC overloads the system, resulting in reduced PV voltage (and thus less power).

When the system is attempting to recharge a depleted battery, the peak power is being sought, but once the battery is charged only trickle charging and/or maintenance power is required. During these periods of reduced power draw requirements, it must be decided on which side of MPP to operate. The lower duty cycle side of MPP results in more efficient operation of the DCC, but higher ripple current on the output. Conversely, the higher duty cycle side of MPP results in less efficient operation, but reduced output ripple. Since any photo energy that is not converted to electricity is wasted regardless of the efficiency of the conversion process, it makes sense to operate in the region above MPP when seeking reduced power conversion levels since this will not require the output filters to be designed to accommodate higher ripple than found at MPP. An addition, operating in the higher duty cycle range reduces the sensitivity of the system to any fluctuations/noise in the duty cycle, because the power falloff with respect to duty cycle is much more gradual above MPP than below.

Another important consideration is that, while directly controlling for output power (or output current since it is nearly proportional to output power in a battery charge system) may initially seem like a good idea, it can lead to serious controllability issues. This is primarily because the power drawn from the PV is neither proportional to duty cycle nor even invertible with respect to duty cycle (i.e. there are more than one duty cycle associated with any given power level except for MPP). If output power is used directly as the sole control parameter, the control system cannot make instantaneous decisions regarding how to adjust the duty cycle. It must instead make decisions based on the perceived change in power with respect to duty cycle dP/dD.

In theory this can work. In a discretely controlled system without rapid changes in insolation the changes in duty cycle can be assessed and altered after steady state operation is reached. However, In applications where changes in insolation occur on a shorter time scale (such as the case of a rotating satellite) the ratio of dP/dD must be calculated by dividing derivatives of each with respect to time. Additional processing is required to account for the fact that dD/dt will change polarities in the course of normal operation, resulting in frequent division by zero (and thus positive and negative spikes towards infinity in our assessment of dP/dD). Another factor that comes into play is the non-steady state behavior of the DCC; The poles and zeros in the DCC transfer function begin to have a more pronounced effect on behavior unless large time constants are used (which interferes with the goal of quick response to changes in insolation). Because of these issues, an alternate control parameter must be found that is better suited for stable control of the system.

Some parameters which might be suitable include: PV voltage, PV current, PV equivalent resistance. All three of these parameters are invertible functions with respect to duty cycle.

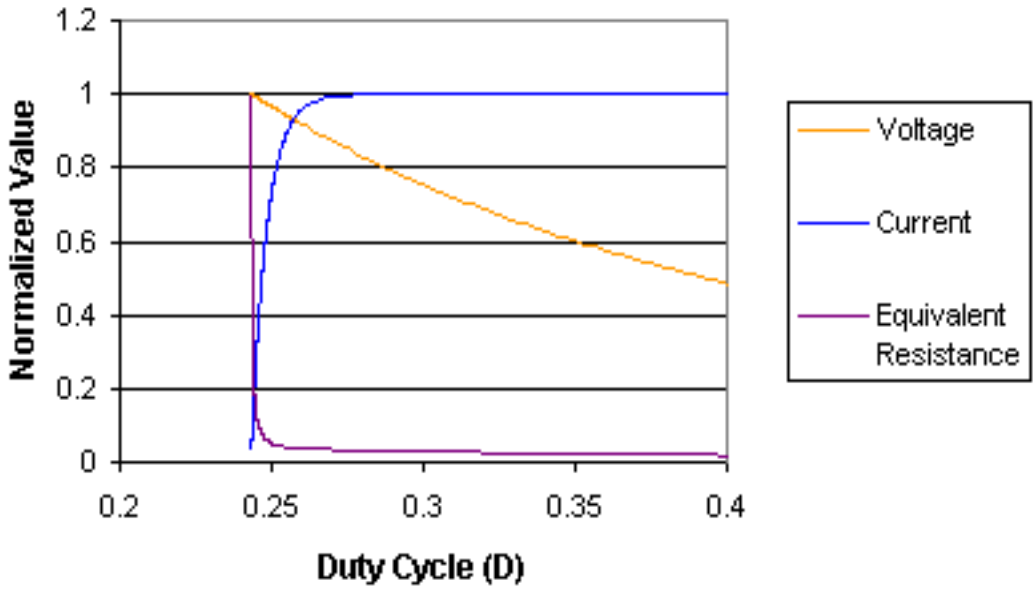

Fig. 3.4.2: Plot of Prospective Control Parameters vs. Duty Cycle

Both impedance and current range nearly from their minimum to maximum values within a small duty cycle range. This would make it difficult to operate the system at MPP, which is approximately at the V-I crossover point (near the flat region outside of the transition area). Compared to the current and impedance, the voltage is relatively linear through to 100% duty cycle. Using voltage as our control parameter allow us to control to any desired operating point.

Another important aspect to consider for each of the parameters is the sensitivity of the MPP to changes in the insolation. A relatively stable MPP will allow reasonable efficiency with a static setpoint, whereas a high sensitivity to changes is insolation will make a more complicated (dynamic) setpoint determination algorithm necessary.

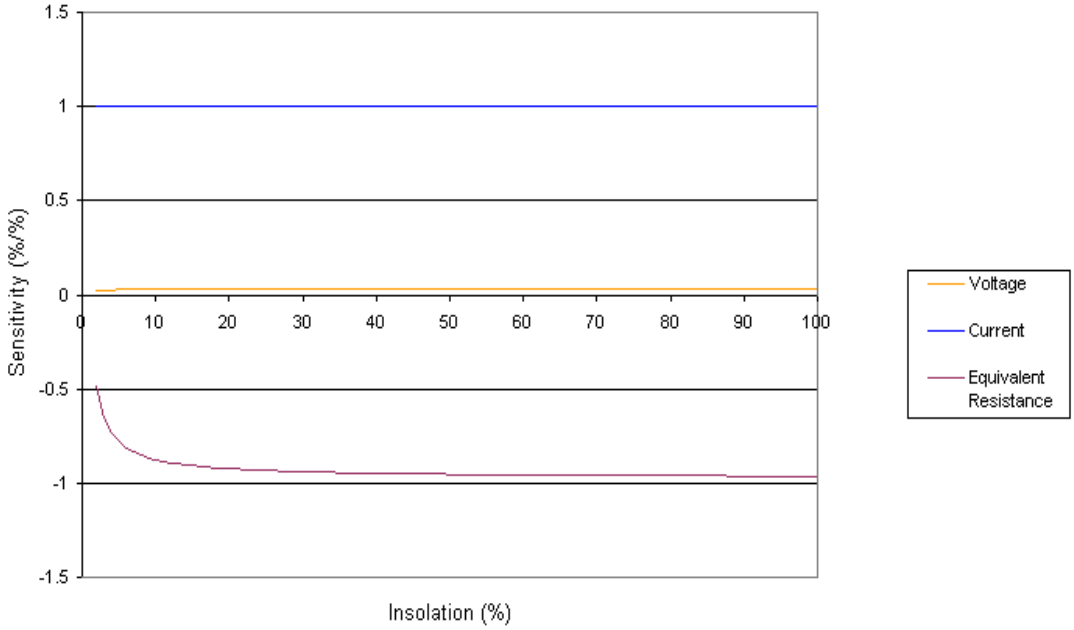

Fig. 3.4.3: Plot of relative sensitivity (XdY/YdX) of each of the potential control parameters vs. insolation level

The MPP voltage is the least sensitive of the three parameters to changes in the level of insolation. This means that for simple systems we can use a static voltage setpoint to control the system and maintain reasonably accurate MPP tracking.

A third consideration in determining what control parameter to use is the sensitivity of the output power to fluctuations in the control variable. This is important because system noise/fluctuations/ripple and the possibility of overshooting the control setpoint could have a major impact on output power. The less sensitive power is to fluctuations in the control parameter, the less the system performance will be degraded by setpoint overshoot or parameter fluctuations.

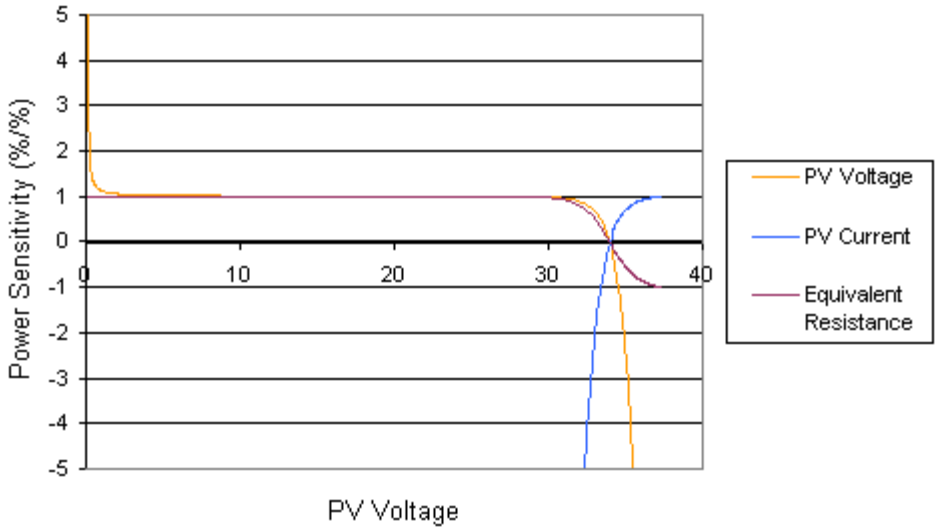

Fig. 3.4.4: Plot of Output Power Sensitivity with respect to possible control parameters

As can be seen in Fig. 3.4.4, the parameter to which power is least sensitive is equivalent resistance (which never exceeds an absolute value of 1). The power is very sensitive to both voltage and current in the regions where they are near constant (PV acting as an ideal source). Fortunately, in the primary region of interest (near MPP) the power is relatively insensitive to all three parameters.

Throughout the rest of this thesis, PV voltage will be used as the control parameter of choice due to its linear behavior with respect to duty cycle and its insensitivity to changes in insolation.

3.4.1 PV System Control

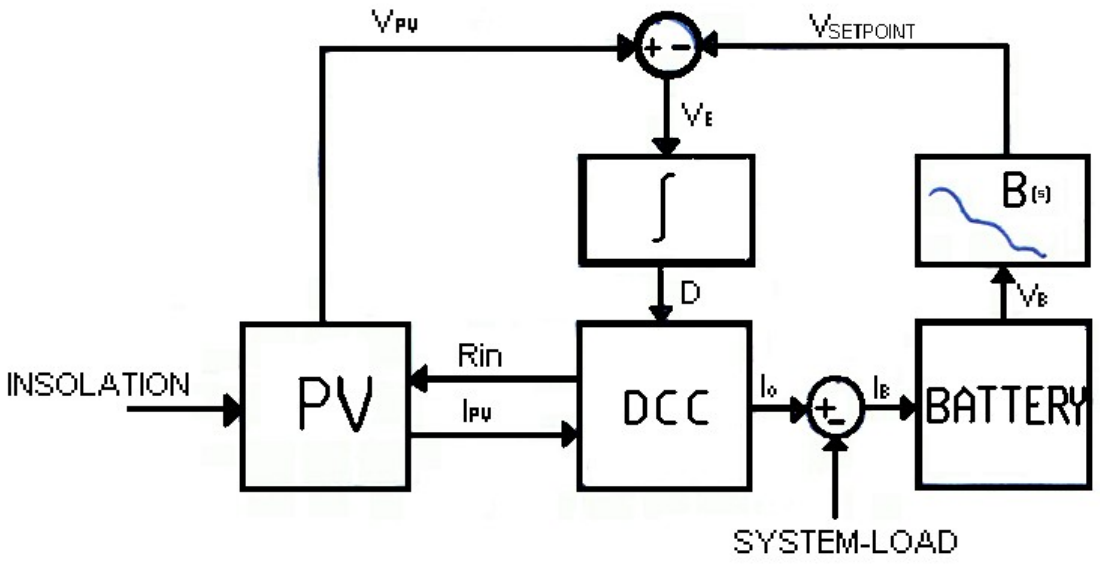

Fig. 3.4.1.1: System Block Diagram

Ultimately, there are only two inputs to the system: insolation and system load. When the battery is not fully charged, the system adjusts to ensure that the maximum available power is drawn from the PV module. Once the battery reaches full charge, the system may need to reduce the power drawn to prevent overcharging and damaging the battery (or other energy storage device) if the maximum available power is greater than the current system load.

The diagram in Fig. 3.4.1.1 is composed of five blocks and two summing nodes. The PV block represents a photovoltaic module used in the system and is functionally defined in Section 2.0. It has two inputs and two outputs, where the inputs are Insolation and Rin and the outputs are V_{PV} and I_{PV}. The V/I characteristic of the PV is determined by the insolation and the operating point on that curve is determined by the PV load condition, Rin.

The DC-DC converter (DCC) acts as a DC transformer, dynamically adjusting the PV loading condition, Rin, to ensure that the PV operates at the desired point of the V/I curve presented by the available insolation. This is accomplished by varying the duty cycle, shown as 'D' in Fig. 3.4.1.1, using a feedback loop which integrates the difference, V_E, between V_{PV} and $V_{SETPOINT}$, to ensure that the desired PV operating voltage is attained.

$V_{SETPOINT}$ is determined by the B(s) block based on battery voltage, V_B. This allows the system to change the operating point of the PV after the battery is charged, to ensure that the system does not overcharge (and thus damage) the battery.

Because the state of charge (SOC) of the battery changes over a much greater time scale than the dynamic behavior of either the DCC itself or the PV (including insolation changes), the setpoint determination block, B(s), can be designed to operate at much lower frequencies (subHz) than the main control loop (and to introduce no undesired phase shift in higher frequency regions). As such it need not contribute to stability concerns.

Two potential alterations to the diagram can be made if desired: 1) Additional PV-DCC modules can be added in parallel by duplicating everything except the summing node that feeds the battery, the system load input, and the battery itself, and 2) the setpoint determination block, B(s) could be modified to include inputs from throughout the system to allow greater control of accepted power (e.g. battery current, V_{PV}, and I_{PV}).

One benefit of using the PV voltage as the primary control variable is a partial decoupling of the DCC control from the output performance of the system. The output behavior of the system only affects the operation of the control system in two ways: The feedback path that determines $V_{SETPOINT}$, and reverse feedthrough between the output of the DCC and its input (which is minimal). This allows the effects of the output filter and load poles to be minimal. Instead of dealing with (and requiring settling of) the output transient response, we need only deal with the input transient response of the PV-DCC interactions. This can lead to greater stability in some cases, and faster response time.

3.5 Application to Satellite PV System design

The preceding sections are now used to generate the design of a specific PV system for a satellite with six panels which is rotating at 300 rev/min and has a 48V battery system.

Modules on opposite sides will be tied in parallel with blocking diodes. This allows a reduction in the number of DCCs needed by 50%, since the modules (being on opposite sides of the satellite) alternate using the converter. The three converters will be connected in parallel to the battery.

The next step is selection of the converter topology. The buck converter topology is inappropriate, because the output voltage must be greater than the input voltage. The maximum voltage of the PVs never exceeds the output voltage, therefore the full functionality of the Ćuk is not needed (although it would certainly work). Therefore the boost converter topology will be used (as it is more efficient than the Ćuk topology).

Once the converter topology is chosen, the components are selected. The core of the boost converter consists of a single inductor and two switches. The selection of the switches is trivial and involves verifying the voltage and current capacities and switching speed capability as described in section 3.3.4.

In order to ensure that the converter remains in CCM for most of the operating domain, the primary inductor was calculated for the case of 50% insolation. At 50% Insolation, V_{MPP} is ~33.2V, the operating duty cycle should be ~31%, and the PV current should be 0.347A. Applying Eq. 6 results in an inductor value of 148.3uH. In the interest of using realistic components, a Coilcraft PCV-2-184-10L will be used. It has a value of 180uH and only 48mΩ of series resistance.

The input current fluctuations at MPP will be ~565mA_{PP}, therefore input filtering is necessary to ensure proper operation. The acceptable voltage and current ripple from the PV for 1% power ripple (from PV) is +11mA/-18mA and -0.72V/+0.61V. Applying Eq. 10 results in a shunt capacitance value of 1.27uF. A 2uF capacitor will be used.

Only one component is needed as part of the input filtering, because the selected DCC topology has a relatively clean input current (i.e. non-pulsed).

The pulsed output current of the boost converter requires much more aggressive filtering. The peak value of the output current pulses is ~976.5mA. If the battery has a series resistance of 10mΩ, 1% ripple in current results in ~49uV ripple (because the DC current out is ~487.9mA). In order to ensure this voltage ripple, a solitary filter capacitor would need to be ~59786uF.

Because 60000uF is such a large and cumbersome value for a capacitor, a lesser value is chosen for the output capacitor and it will be followed by a series inductor. Selection of a 20uF capacitor will results in a voltage ripple of ~0.15V_{PP}. The inductor that reduces the output current to 1% ripple will be 91.8uH. A Coilcraft PCV-2-104-10L with an inductance of 100uH and 32mΩ of series resistance will be used.

The schematic and SPICE simulation text file for the design are shown in Appendix C.

4.0 Simulation Results

The system designed in section 3.5 was simulated and the schematic and spice file for the simulations can be found in Appendix C. The initial results show that the system works, but has a few shortcomings, Fig. 4.0.1.

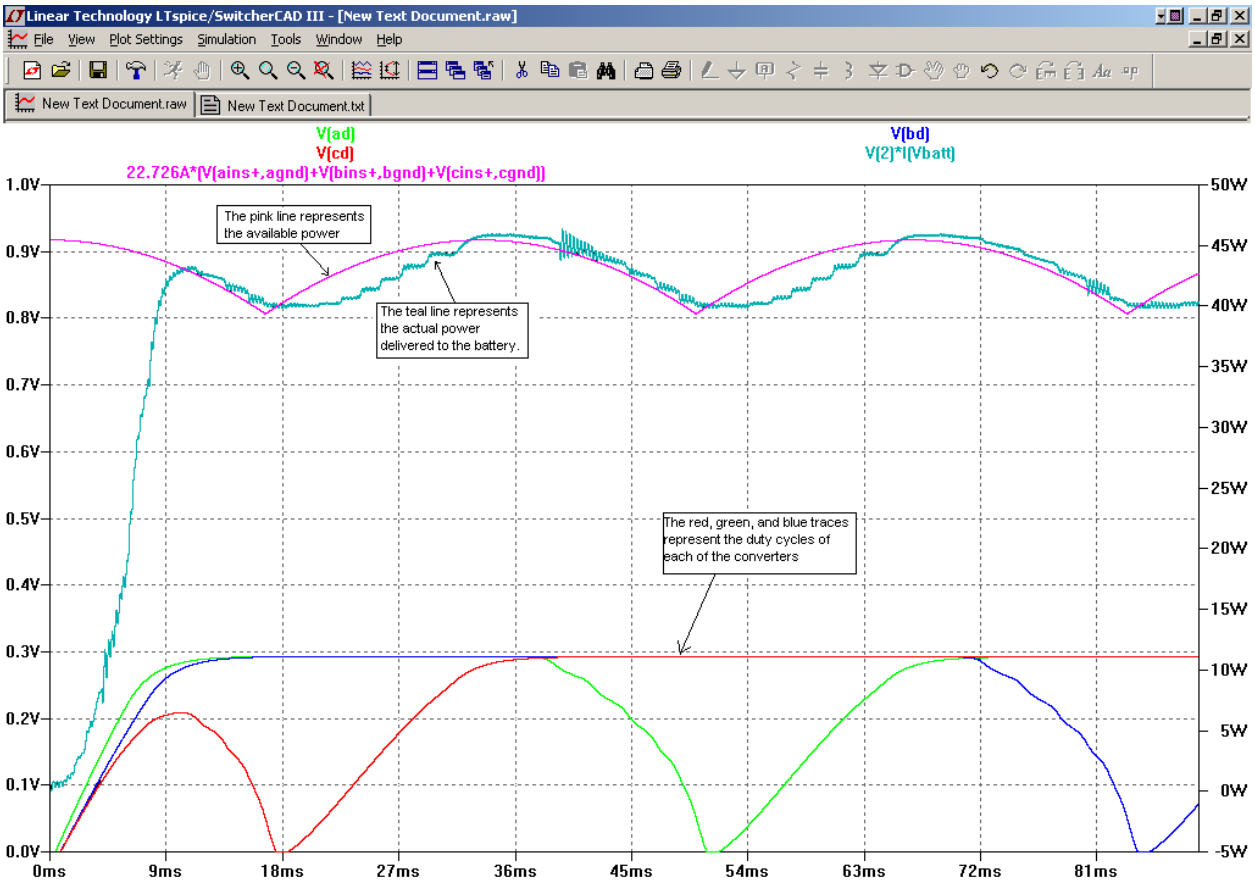

Fig. 4.0.1: Plots of Output Power and Module Duty Cycles for Designed System

There are two main issues with the system as it is currently designed:

1) There is a ringing on the output.
2) The system does not track the available power as well as expected.

The output ringing was a slight surprise as initial simulations (using the averaged model of the DCC) did not result in oscillations. However examination of the individual converters shows that the ringing behavior and failure to track MPP is occurring on the output of whichever stage is least insolated (and is thus operating in discontinuous conduction mode[DCM]).

Two phenomenon are at work here: 1) The ringing occurs at the resonant frequency of the output filter components and is a result of the discontinuous converter behavior interacting with the output filter components, Fig. 4.0.2 Because this phenomenon occurs roughly one third of the time on each converter, the total system output demonstrates this ringing on a near continuous basis. 2) The failure to track MPP in the first part of the cycle occurs because the duty cycle reacts to DCM operation by dropping back to zero and must return to its necessary operating point.

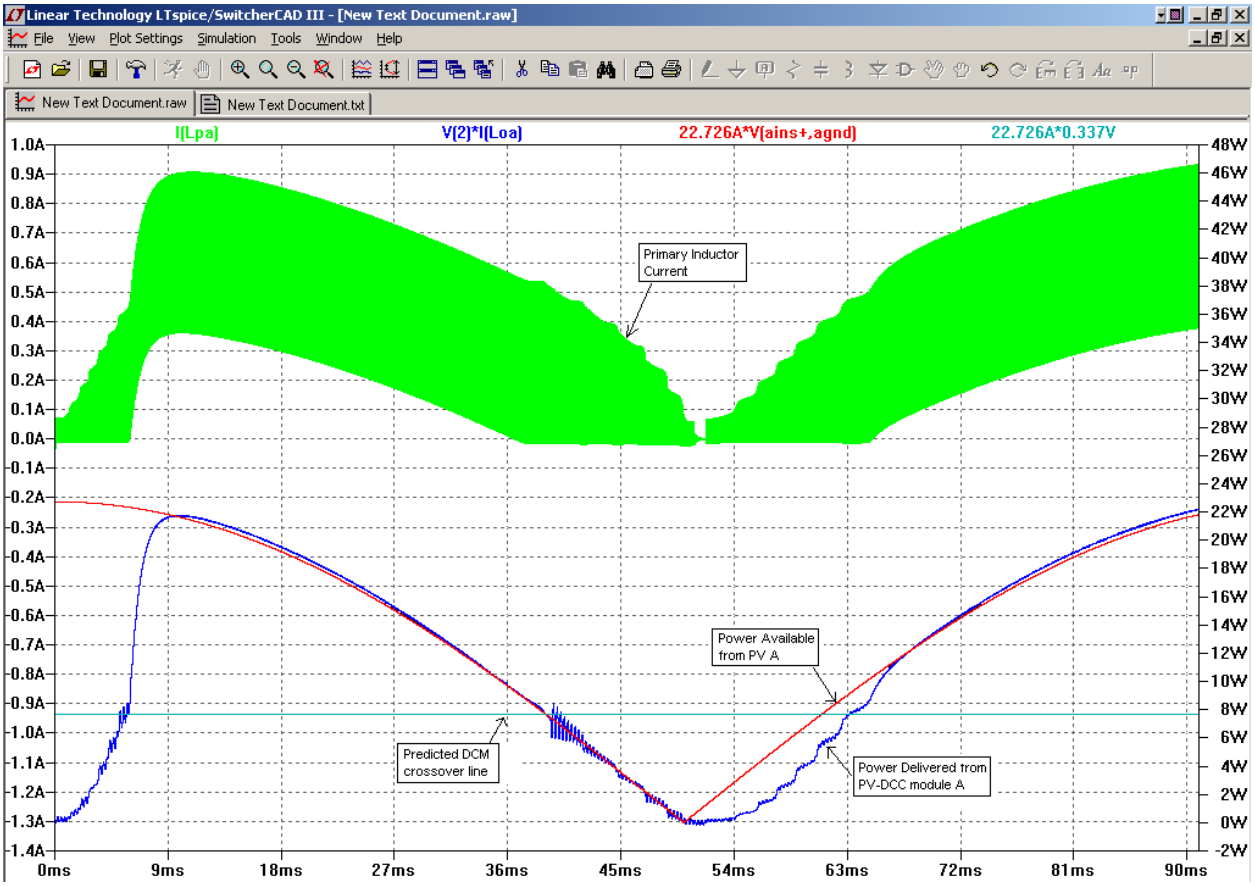

Fig. 4.0.2: Plots of Primary Inductor Current and Output Power demonstrates that oscillations occur while operating in discontinuous conduction mode (DCM).

Because the tracking error is a combination of DCM operation and the fact that the duty cycle drops back to the origin, there are two ways to address it. Either the gain can be increased so that the duty cycle can track effectively even in DCM mode, or the duty cycle must be slew rate limited so that it does not return to the origin during DCM operation.

The ripple generated by the system is shown to be within the limits specified as shown in Fig. 4.0.3 and Fig. 4.0.4. The design requirements were to ensure that input and output ripple did not exceed 1%. Fig. 4.0.3 shows an input power ripple of about 0.1W, which is 0.4%.

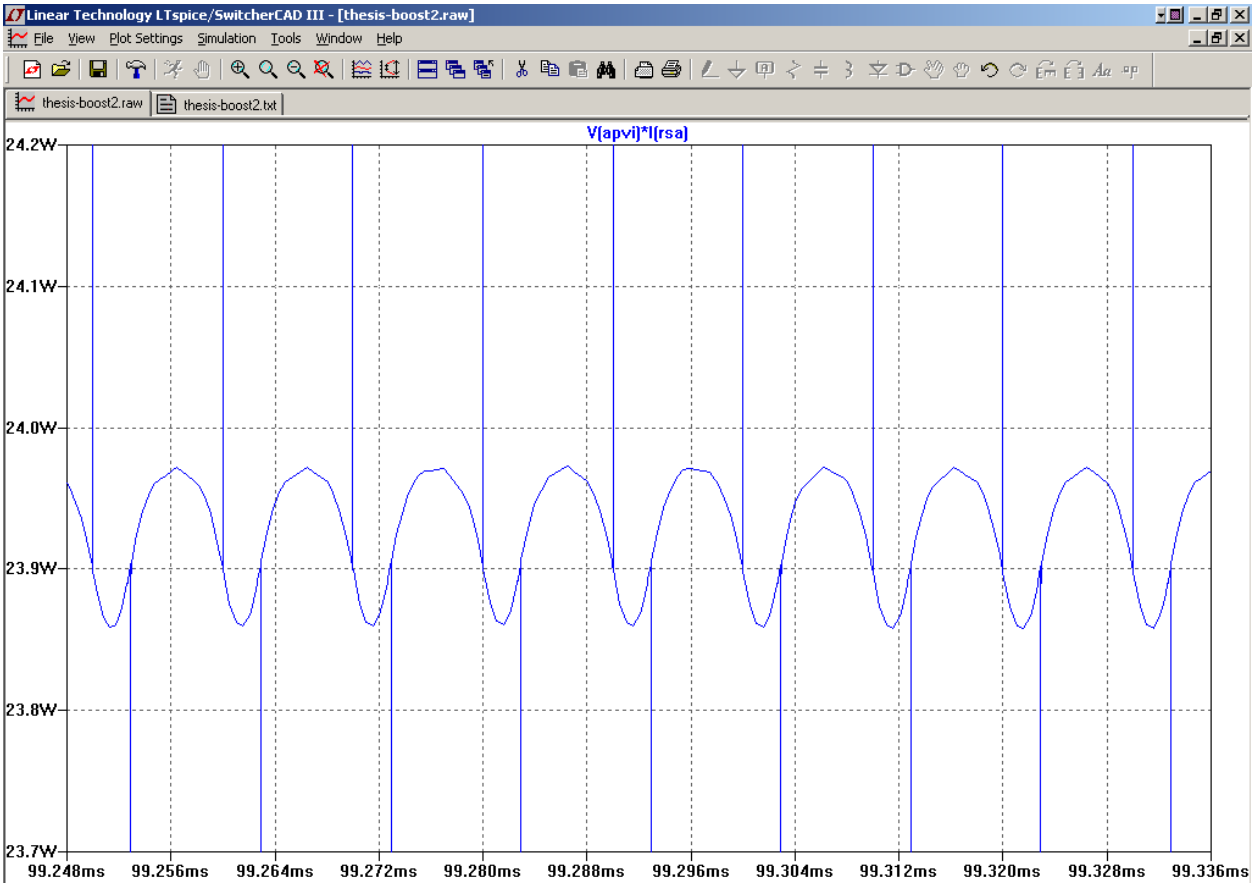

Fig. 4.0.3: Plot showing PV output power ripple <1% to DCC

The output power ripple demonstrated by the system is also about 0.1W, which is equivalent to 0.2%.

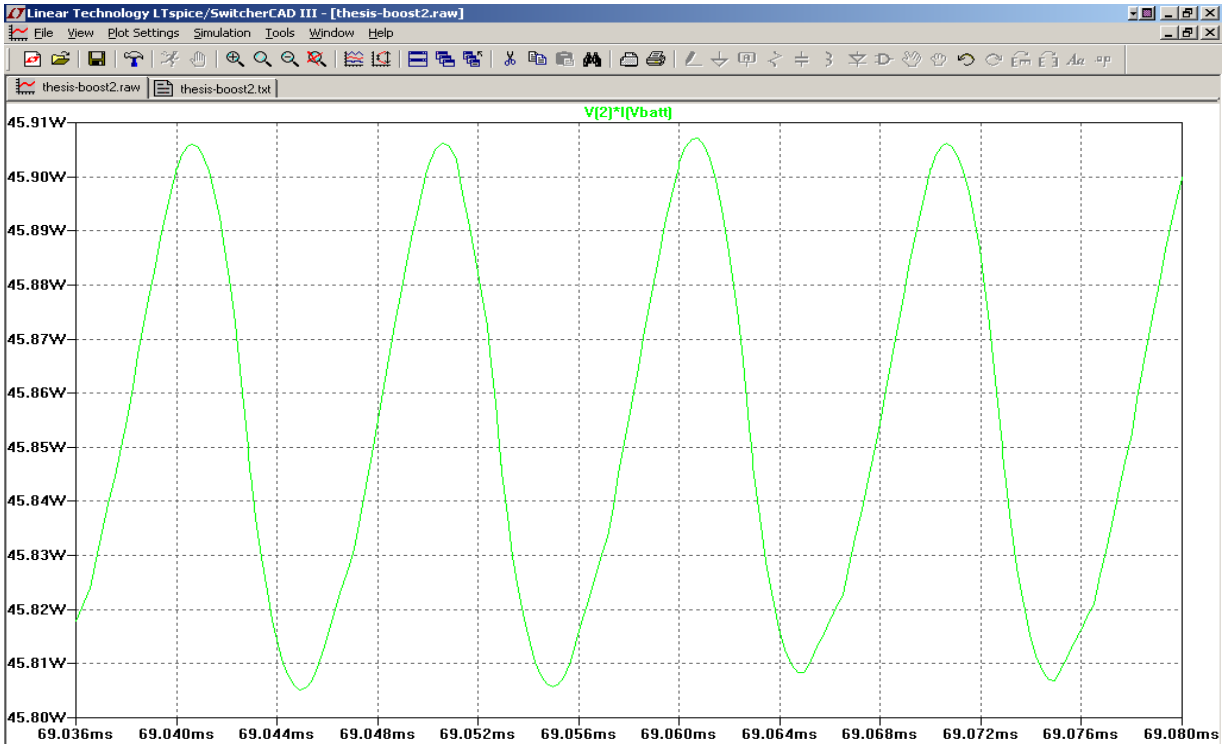

Fig. 4.0.4: Plot showing system power output ripple <1%

Revisiting the design, the primary inductor's value was recalculated to provide continuous conduction mode for insolations as low as 10%. This results in a primary inductor that is 778uH. A Coilcraft PCV-2-105-02L will be used which has an inductance of 1000uH and a series resistance of 370mΩ. This allows the use of a smaller input capacitor of 0.34uF.

The revised system was simulated two different ways. The first way was with an increased gain. The result of the increased gain is that the system continues to draw the maximum available power from the PV modules even when operating in DCM (although the output oscillations do not entirely go away). Unfortunately, the startup transient behavior is unacceptable (although that could be worked around with a soft start circuit in an actual product).

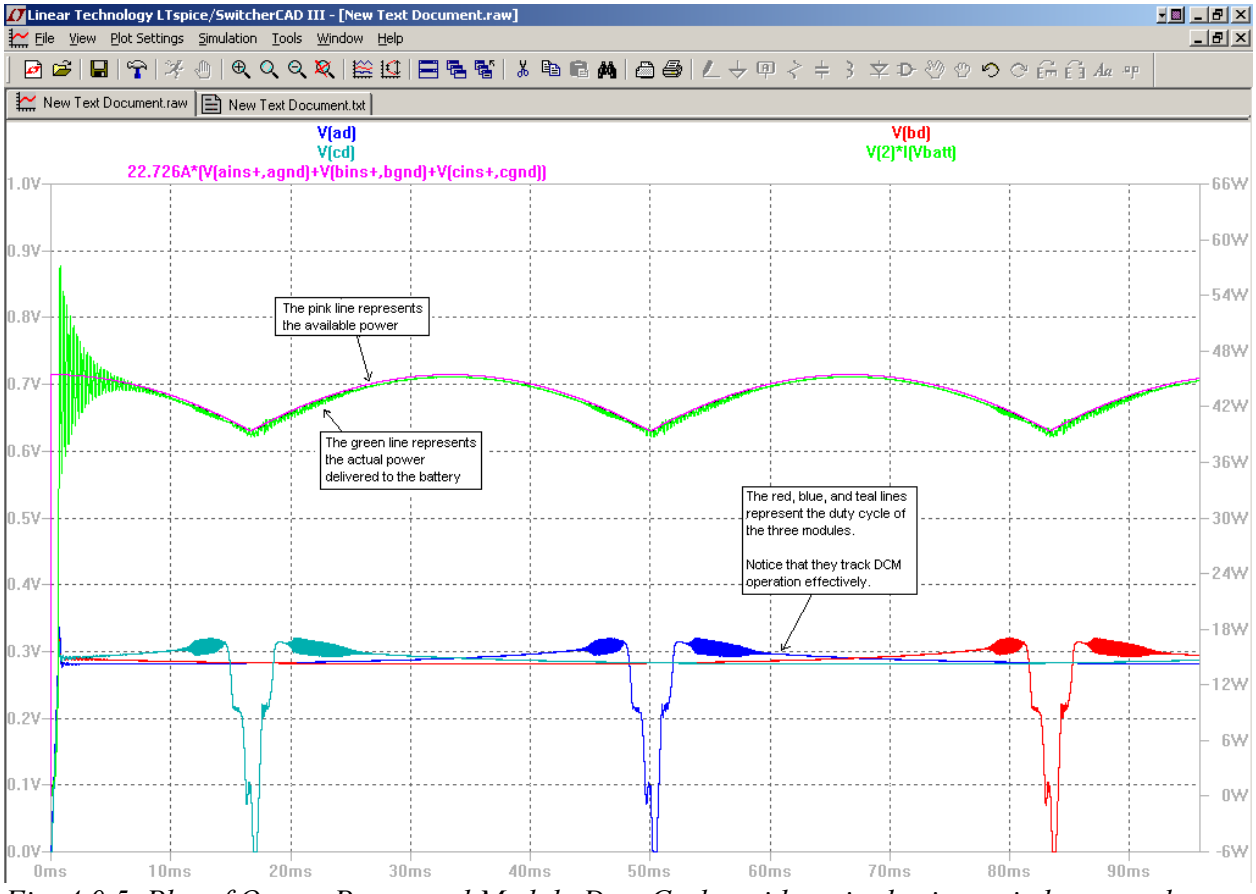

Fig. 4.0.5: Plot of Output Power and Module Duty Cycles with revised primary inductor and increased gain. Shows that increased gain can track MPP during DCM operation, but has startup transient problems.

The revised system was also simulated and implemented with the addition of duty cycle slew rate limitation and a correction factor to reduce the setpoint as insolation level falls. The resulting behavior still has some oscillations at the output, but is much more inline with initial expectations, Fig. 4.0.6.

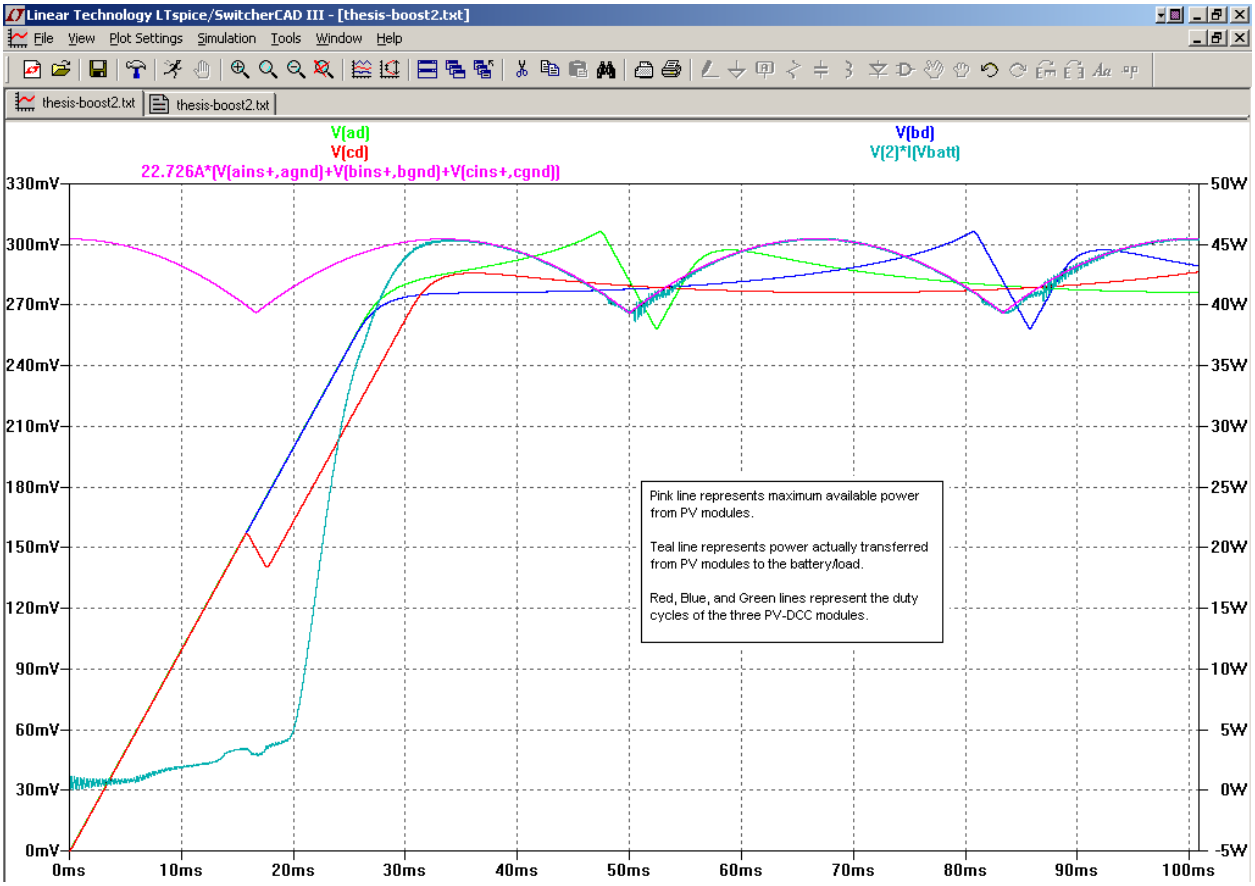

Fig. 4.0.6: Switched Model Behavior of revised PV-DCC System with duty cycle slew rate limitation and setpoint correction factor implemented.

5.0 Conclusion

The primary goal of this thesis was to investigate examine the use of photovoltaic modules (particularly in extraterrestrial applications) to determine the optimal method of extracting power from them.

Behavior of direct connected modules was examined and found to have severe limitations. PV modules connected directly in series and parallel arrays could interefere with each other depending on their relative parameters and level of insolation. Further more, any given array produced maximum power at only one load condition (which may not coincide with present operating requirements). Even at the optimal array load, total available power may not be extracted if different insolations are present (as is inevitably the case on a rotating satellite). Therefore, the use of a parallel connected DC-DC converter for each PV module is suggested.

Various DC-DC converter topologies were investigated and specific topologies (buck, boost, and Ćuk) were specifically suggested for use with PV systems due to the desired efficiency and non-pulse current requirements.

Possible control parameters for the DC-DC converters were investigated and PV voltage was found to be the most suitable.

5.1 Results of Design & Simulation

The design principles developed were used to develop a system for a satellite with six panels rotating at 300 rev/min. The results show the validity of the preceding work, but did point to a few shortcomings; The need to ensure that the module acting in DCM operation continues to behave acceptably (i.e. without excessive output oscillations), and the value of tracking changes in PV insolation. Once these are taken into account the output discrepancies are significantly reduced.

5.2 Areas for Future Investigation

Several areas of interest are open to continued investigation. In terms of system control, it was shown that while reasonable behavior can be achieved with a static setpoint, behavior can be improved by dynamically altering the setpoint voltage based on current insolation (which can be calculated from PV voltage and current for a known PV). Ideally, the correct duty cycle could be directly calculated to generate the desired setpoint if a digital controller was used.

Another factor that could be incorporated, if a digital controller was used, is the ability to assess the PV characteristics from system behavior and adjust to compensate for aging effects or damage. While this would not be as valuable in a terrestrial application where timely repairs can be made, it would be invaluable in a satellite or other space application due to the difficulties and cost associated with gaining access to do repairs.

A third area of interest would be the implementation of DCC stages with delta-sigma modulation instead of PWM. The noise spectrum of PWM can lead to emissions and immunity problems. Delta -sigma modulation has three main benefits: It spreads the noise out resulting in less emissions/immunity problems, it can allow higher resolution and range of operation than many PWM controllers, and it clearly defines the minimum interval between switching events (allowing extreme duty cycles without exceptional switching losses). The potential drawbacks would include the difficulty with characterizing the output ripple, because the same spread spectrum behavior which would reduce EMI concerns would cause the output ripple to be spread spectrum noise.

8.0 Bibliography/References

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Appendix A: Simulation of Directly Connected PV Modules

As discussed in section 3.1, the direct connection of PV modules has drawbacks. Each PV is going to require a different operating point to achieve maximum power transfer based on factors such as insolation, temperature, age/damage, and manufacturing process variation. This will result in (potentially) significant losses. The following chart shows the output power of four three-element arrays: series w/o bypass diodes, series w/ bypass diodes, parallel w/o blocking diodes, parallel w/ blocking diodes.

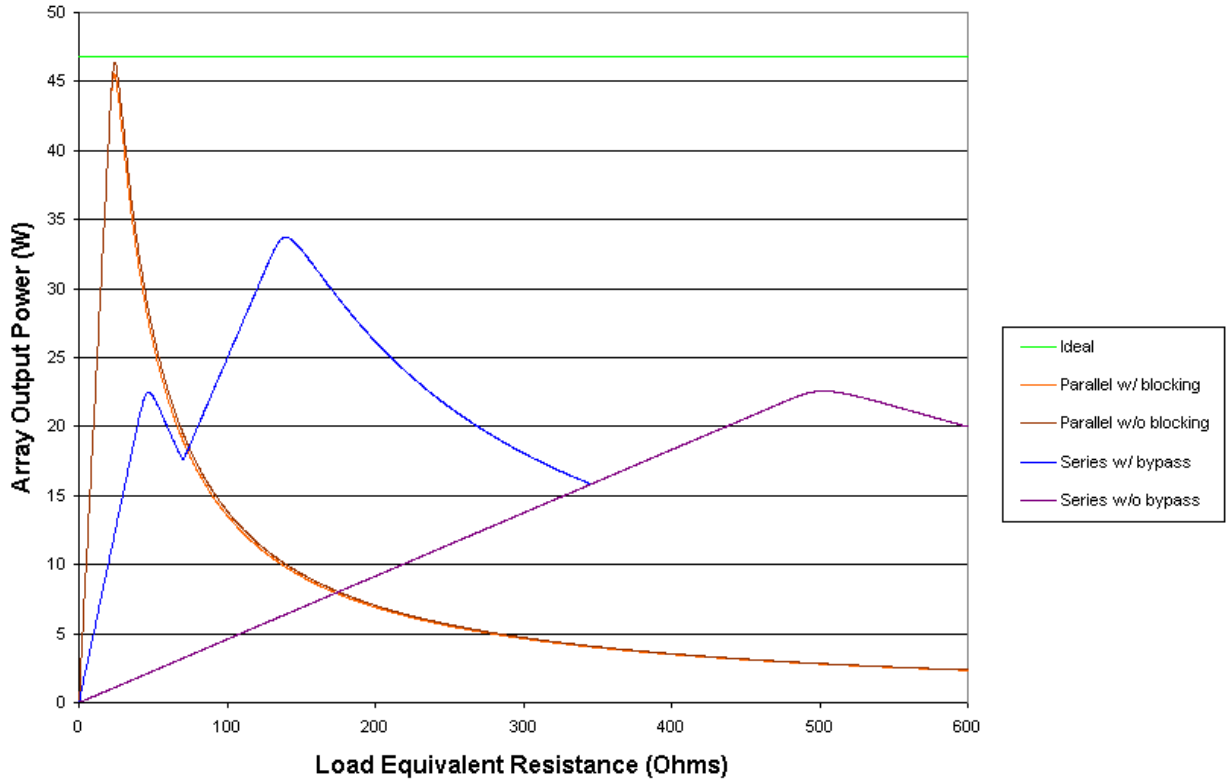


Fig. A1: Array Output power with respect to load

The losses in the series arrays are significant in either case, but the presence of bypass diodes clearly allows a significant increase in available power (when the load is tailored to allow MPP operation). However, this increase is still well below the maximum power that could be drawn from the array (in an ideal/lossless case). The requirement that 'per

module' DC-DC conversion yield greater efficiency than either 'per array' DC conversion or direct connection to battery can easily be met.

The losses in the parallel arrays do not provide as clear and obvious a case for “per module” DC-DC conversion as the series array losses (although tailoring the load to match MPP operation of the array with a DC-DC converter is still a necessity). The decision regarding whether to use 'per module' DC conversion depends on other factors such as: the losses for the specific application, whether there is a need for redundant/independent behavior from the modules (i.e. is it acceptable for the whole system to go down if one of the modules were to fail), and reducing risk of damage to shaded modules from reverse current.

The following figure shows the difference in current generated in a parallel array per module (with and without blocking diodes):

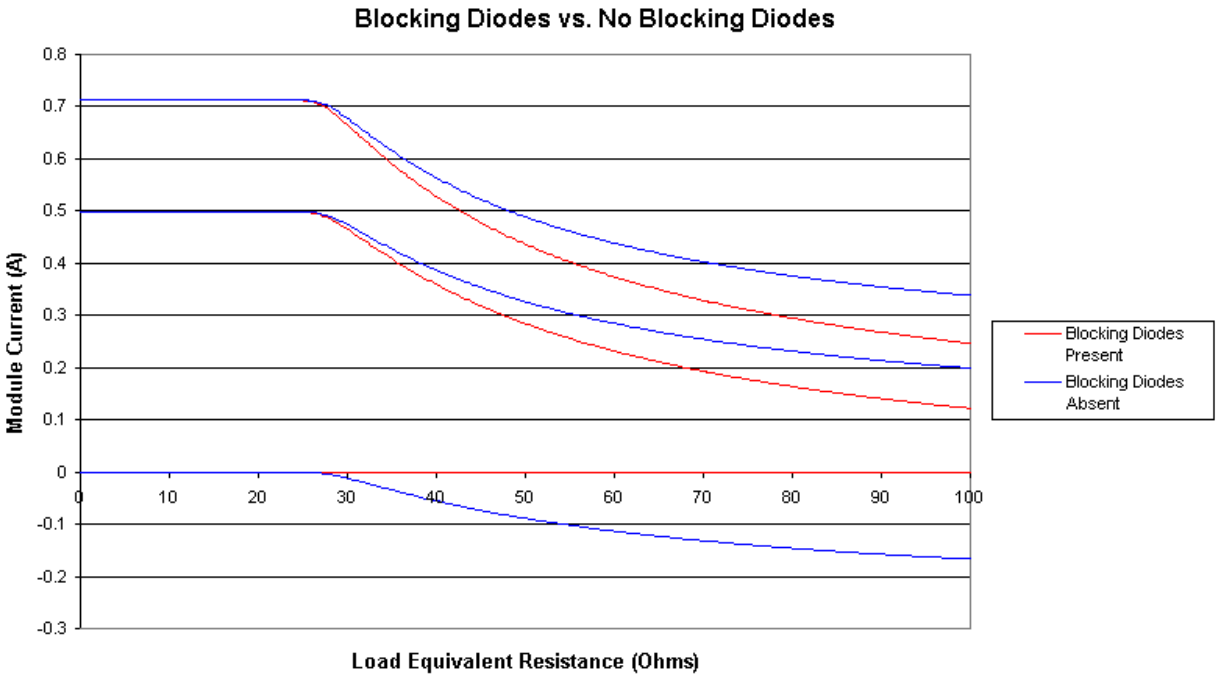


Fig. A2: Current in three parallel modules with differing insolations

The use of per module DC-DC converters acts similar to the blocking diodes (in that if a single module is damaged, it does not become a drag on the rest of the array), but with the added benefit of reducing losses (because a DC-DC converter would be necessary at the output of the array anyway, so why pay the losses for the blocking diode?)

The following SPICE script was run to show the performance of parallel and series arrays (both with and without bypass/blocking diodes).

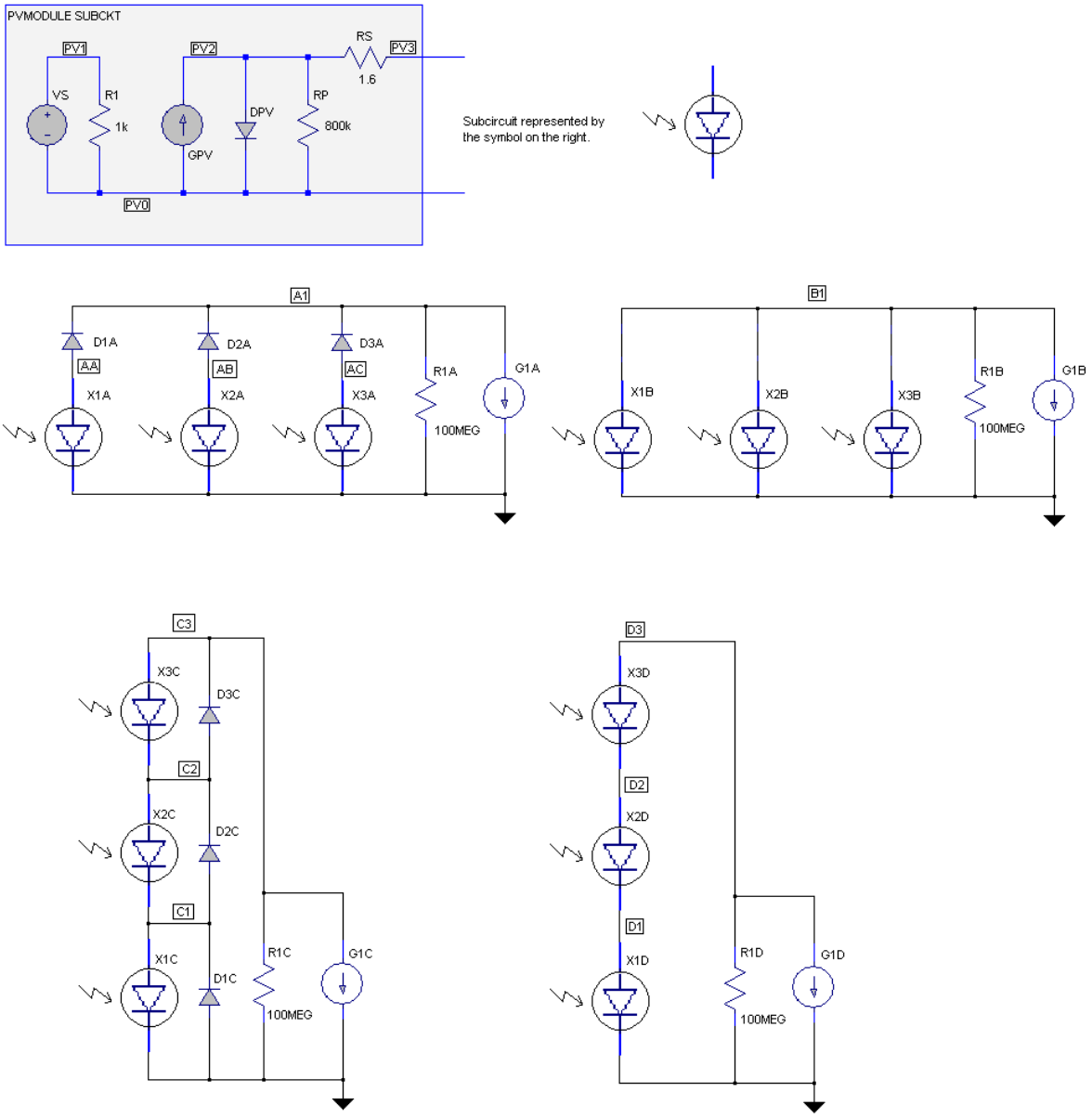


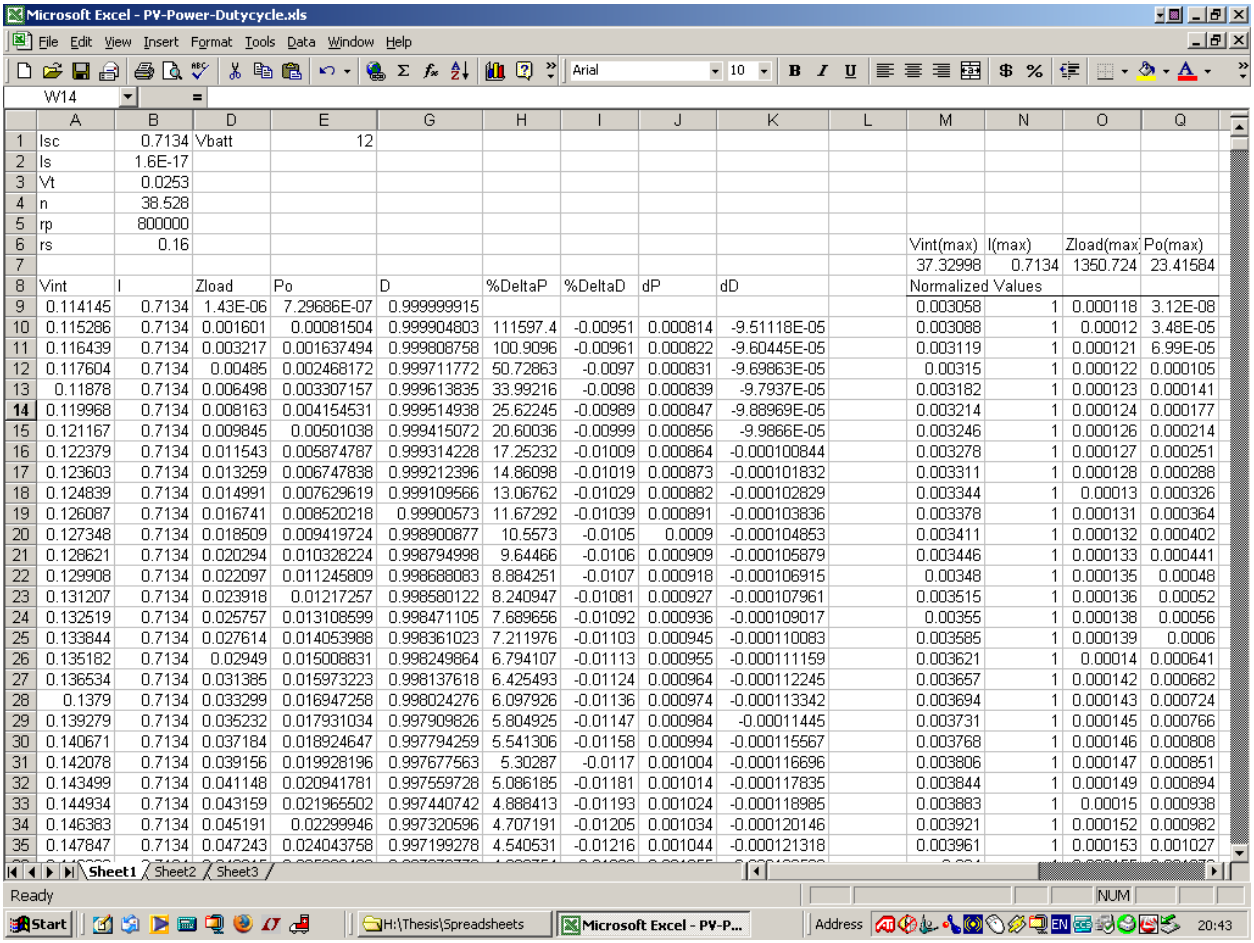
Fig. A3: PV Array Comparison Schematic

```
.TITLE 3PV-LOADSWEEP

*PARALLEL W/BLOCKING DIODES
X1A AA 0 PVMODULE PARAMS: Vinsol=1.0V
D1A AA A1 DSHOTTKY
X2A AB 0 PVMODULE PARAMS: Vinsol=0.7V
D2A AB A1 DSHOTTKY
X3A AC 0 PVMODULE PARAMS:Vinsol=0.3V
D3A AC A1 DSHOTTKY

R1A A1 0 100MEG
G1A A1 0 VALUE={V(A1,0)/((1E-9)+TIME)}
*

*PARALLEL W/O BLOCKING DIODES
X1B B1 0 PVMODULE PARAMS: Vinsol=1.0V
X2B B1 0 PVMODULE PARAMS: Vinsol=0.7V
X3B B1 0 PVMODULE PARAMS: Vinsol=0.3V

R1B B1 0 100MEG
G1B B1 0 VALUE={V(B1,0)/((1E-9)+TIME)}
*

*SERIES W/BYPASS DIODES
X1C C1 0 PVMODULE PARAMS: Vinsol=1.0V
D1C 0 C1 DSHOTTKY
X2C C2 C1 PVMODULE PARAMS: Vinsol=0.7V
D2C C1 C2 DSHOTTKY
X3C C3 C2 PVMODULE PARAMS: Vinsol=0.3V
D3C C2 C3 DSHOTTKY

R1C C3 0 100MEG
G1C C3 0 VALUE={V(C3,0)/((1E-9)+TIME)}
```

```
*

*PARALLEL W/O BYPASS DIODES
X1D D1 0 PVMODULE PARAMS: Vinsol=1.0V
X2D D2 D1 PVMODULE PARAMS: Vinsol=0.7V
X3D D3 D2 PVMODULE PARAMS: Vinsol=0.3V

R1D D3 0 100MEG
G1D D3 0 VALUE={V(D3,0)/((1E-9)+TIME)}
*
*****
.SUBCKT PVMODULE PV3 PV0 PARAMS: Vinsol=1V
VS PV1 PV0 {Vinsol}
R1 PV1 PV0 1k

GPV PV0 PV2 VALUE={0.7134*V(PV1,PV0)}
DPV PV2 PV0 DINTERNAL
RP PV2 PV0 800k
RS PV2 PV3 1.6

.MODEL DINTERNAL D(IS=16E-18 N=38.528)
.ENDS PVMODULE
*****

.MODEL DSHOTTKY D(N=0.7 RS=0)
.TRANS 1 600 0 1m
.END
```

Appendix B

The plots of PV behavior in section 3.4 are derived from the spreadsheet shown below:



Microsoft Excel - PV-Power-Dutycycle.xls

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W14 =

	A	B	D	E	G	H	I	J	K	L	M	N	O	Q
1	Isc	0.7134	Vbatt	12										
2	Is	1.6E-17												
3	Vt	0.0253												
4	n	38.528												
5	rp	800000												
6	rs	0.16									Vint(max)	I(max)	Zload(max	Po(max)
7											37.32998	0.7134	1350.724	23.41584
8	Vint	I	Zload	Po	D	%DeltaP	%DeltaD	dP	dD		Normalized Values			
9	0.114145	0.7134	1.43E-06	7.29686E-07	0.999999915						0.003058	1	0.000118	3.12E-08
10	0.115286	0.7134	0.001601	0.00081504	0.999904803	111597.4	-0.00951	0.000814	-9.51118E-05		0.003088	1	0.00012	3.48E-05
11	0.116439	0.7134	0.003217	0.001637494	0.999808758	100.9096	-0.00961	0.000822	-9.60445E-05		0.003119	1	0.000121	6.99E-05
12	0.117604	0.7134	0.00485	0.002468172	0.999711772	50.72863	-0.0097	0.000831	-9.69863E-05		0.00315	1	0.000122	0.000105
13	0.11878	0.7134	0.006498	0.003307157	0.999613835	33.99216	-0.0098	0.000839	-9.7937E-05		0.003182	1	0.000123	0.000141
14	0.119968	0.7134	0.008163	0.004154531	0.999514938	25.62245	-0.00989	0.000847	-9.88969E-05		0.003214	1	0.000124	0.000177
15	0.121167	0.7134	0.009845	0.00501038	0.999415072	20.60036	-0.00999	0.000856	-9.9866E-05		0.003246	1	0.000126	0.000214
16	0.122379	0.7134	0.011543	0.005874787	0.999314228	17.25232	-0.01009	0.000864	-0.000100844		0.003278	1	0.000127	0.000251
17	0.123603	0.7134	0.013259	0.006747838	0.999212396	14.86098	-0.01019	0.000873	-0.000101832		0.003311	1	0.000128	0.000288
18	0.124839	0.7134	0.014991	0.007629619	0.999109566	13.06762	-0.01029	0.000882	-0.000102829		0.003344	1	0.00013	0.000326
19	0.126087	0.7134	0.016741	0.008520218	0.99900573	11.67292	-0.01039	0.000891	-0.000103836		0.003378	1	0.000131	0.000364
20	0.127348	0.7134	0.018509	0.009419724	0.998900877	10.5573	-0.0105	0.0009	-0.000104853		0.003411	1	0.000132	0.000402
21	0.128621	0.7134	0.020294	0.010328224	0.998794998	9.64466	-0.0106	0.000909	-0.000105879		0.003446	1	0.000133	0.000441
22	0.129908	0.7134	0.022097	0.011245809	0.998688083	8.884251	-0.0107	0.000918	-0.000106915		0.00348	1	0.000135	0.00048
23	0.131207	0.7134	0.023918	0.01217257	0.998580122	8.240947	-0.01081	0.000927	-0.000107961		0.003515	1	0.000136	0.00052
24	0.132519	0.7134	0.025757	0.013108599	0.998471105	7.689656	-0.01092	0.000936	-0.000109017		0.00355	1	0.000138	0.00056
25	0.133844	0.7134	0.027614	0.014053988	0.998361023	7.211976	-0.01103	0.000945	-0.000110083		0.003585	1	0.000139	0.0006
26	0.135182	0.7134	0.02949	0.015008831	0.998249864	6.794107	-0.01113	0.000955	-0.000111159		0.003621	1	0.00014	0.000641
27	0.136534	0.7134	0.031385	0.015973223	0.998137618	6.425493	-0.01124	0.000964	-0.000112245		0.003657	1	0.000142	0.000682
28	0.1379	0.7134	0.033299	0.016947258	0.998024276	6.097926	-0.01136	0.000974	-0.000113342		0.003694	1	0.000143	0.000724
29	0.139279	0.7134	0.035232	0.017931034	0.997909826	5.804925	-0.01147	0.000984	-0.00011445		0.003731	1	0.000145	0.000766
30	0.140671	0.7134	0.037184	0.018924647	0.997794259	5.541306	-0.01158	0.000994	-0.000115567		0.003768	1	0.000146	0.000808
31	0.142078	0.7134	0.039156	0.019928196	0.997677563	5.30287	-0.0117	0.001004	-0.000116696		0.003806	1	0.000147	0.000851
32	0.143499	0.7134	0.041148	0.020941781	0.997559728	5.086185	-0.01181	0.001014	-0.000117835		0.003844	1	0.000149	0.000894
33	0.144934	0.7134	0.043159	0.021965502	0.997440742	4.888413	-0.01193	0.001024	-0.000118985		0.003883	1	0.00015	0.000938
34	0.146383	0.7134	0.045191	0.02299946	0.997320596	4.707191	-0.01205	0.001034	-0.000120146		0.003921	1	0.000152	0.000982
35	0.147847	0.7134	0.047243	0.024043758	0.997199278	4.540531	-0.01216	0.001044	-0.000121318		0.003961	1	0.000153	0.001027

Sheet1 Sheet2 Sheet3

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Appendix C: SPICE file for system simulation

The following schematic and spice script were used for the simulations in section 4.0:

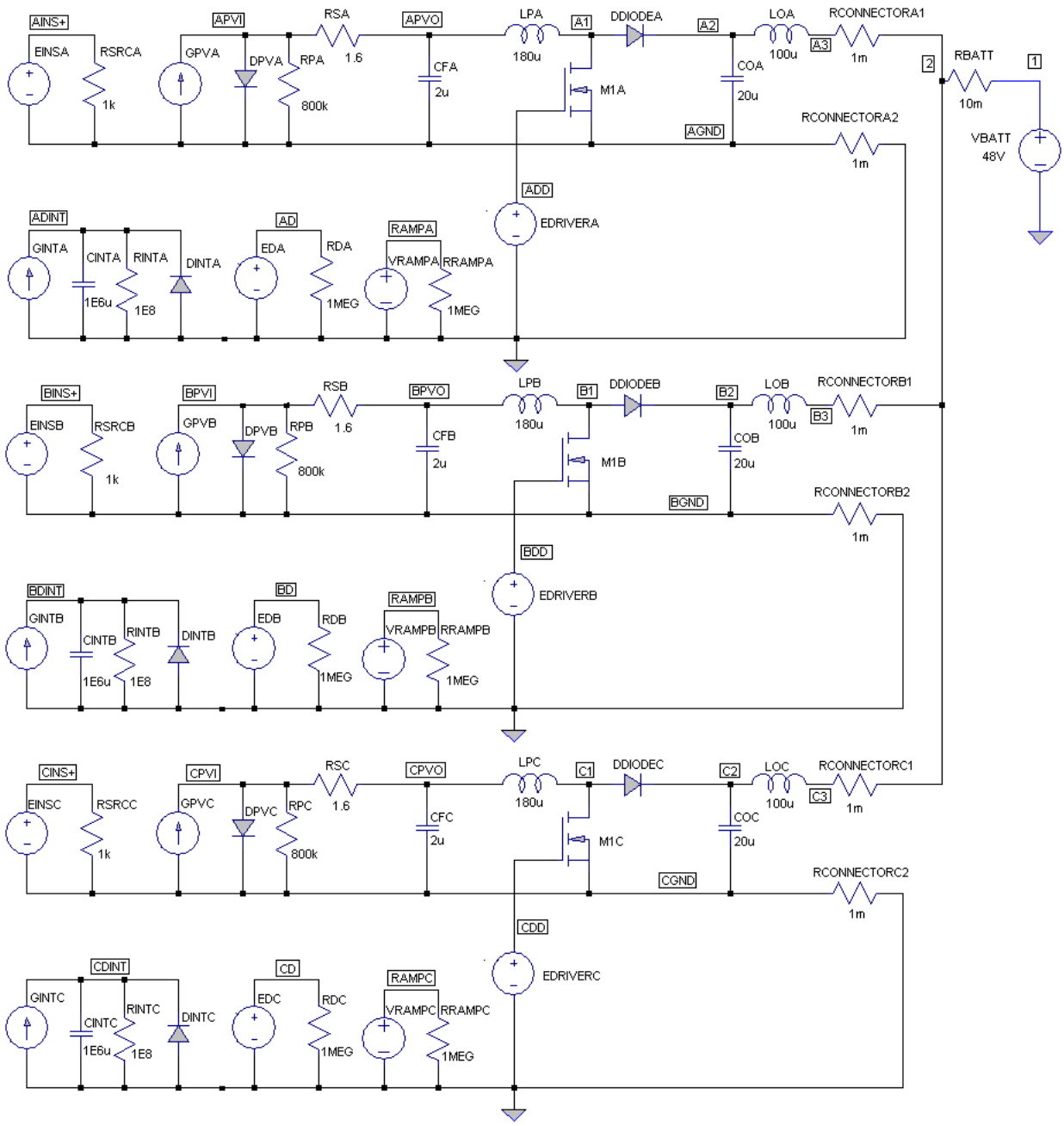

Fig. C.1: PV-DCC Simulation Schematic

```
.TITLE inputvoltagecontrol

EINSA AINS+ AGND VALUE={ABS(COS(2*3.14159265*5*TIME+2*3.14159265*0/3))};{1};
RSRCA AINS+ AGND 1k

GPVA AGND APVI VALUE={0.7134*V(AINS+)}
DPVA APVI AGND DPV
RPA AGND APVI 800k
RSA APVI APVO 1.6

CFA APVO AGND 2uF rser=10m IC=0V;0.34uF rser=10m IC=0V
LPA APVO A1 180uH rser=48m ;1000uH rser=370m;
;DDIODEA2 A1 A2B DCON;
DDIODEA A1 A2 DCON;EDDIODEA A2B A2 VALUE={-V(AD)*V(A1)/(1-V(AD))};
M1A A1 ADD AGND MSWITCH;GMIA A1 AGND VALUE={V(AD)*I(LPA)};
COA A2 AGND 20uF rser=10m IC=48V
LOA A2 A3 100uH rser=32m

EDRIVERA ADD 0 TABLE {V(AD)-V(RAMPA)} -0.0001,0 +0.0001,10
VRAMPA RAMPA 0 PULSE(0 1 0 9.95us 25ns 25ns 10us)
RRAMPA RAMPA 0 1MEG
EDA AD 0 TABLE {V(ADINT)} 0,0 1,1
RDA AD 0 1MEG

GINTA ADINT 0 TABLE {-10*(V(APVO,AGND)-(33.944*V(ASET)/37.367))} -10,-10 10,10
CINTA ADINT 0 1E6uF IC=0V
RINTA ADINT 0 1E8
DINTA 0 ADINT DCON

GSETA ASET 0 VALUE={-0.7134*V(AINS+)}
DSETA ASET 0 DPV
RSETA ASET 0 1MEG
```

```
RCONNECTORA1 AGND 0 0.001
RCONNECTORA2 A3 2 0.001

*****

EINSB BINS+ BGND VALUE={ABS(COS(2*3.14159265*5*TIME+2*3.14159265*1/3))};{1};
RSRCB BINS+ BGND 1k

GPVB BGND BPVI VALUE={0.7134*V(BINS+)}
DPVB BPVI BGND DPV
RPB BGND BPVI 800k
RSB BPVI BPVO 1.6

CFB BPVO BGND 2uF rser=10m IC=0V;0.34uF rser=10m IC=0V
LPB BPVO B1 180uH rser=48m ;1000uH rser=370m;
;DDIODEB2 B1 B2B DCON;
DDIODEB B1 B2 DCON;EDDIODEB B2B B2 VALUE={-V(BD)*V(B1)/(1-V(BD))};
M1B B1 BDD BGND MSWITCH;GMIB B1 BGND VALUE={V(BD)*I(LPB)};
COB B2 BGND 20uF rser=10m IC=48V
LOB B2 B3 100uH rser=32m


EDRIVERB BDD 0 TABLE {V(BD)-V(RAMPB)} -0.0001,0 +0.0001,10
VRAMPB RAMPB 0 PULSE(0 1 0us 9.95us 25ns 25ns 10us)
RRAMPB RAMPB 0 1MEG
EDB BD 0 TABLE {V(BDINT)} 0,0 1,1
RDB BD 0 1MEG

GINTB BDINT 0 TABLE {-10*(V(BPVO,BGND)-(33.944*V(BSET)/37.367))} -10,-10 10,10
CINTB BDINT 0 1E6uF IC=0V
RINTB BDINT 0 1E8
DINTB 0 BDINT DCON

GSETB BSET 0 VALUE={-0.7134*V(BINS+)}
```

```
DSETB BSET 0 DPV
RSETB BSET 0 1MEG

RCONNECTORB1 BGND 0 0.001
RCONNECTORB2 B3 2 0.001

*****

EINSC CINS+ CGND VALUE={ABS(COS(2*3.14159265*5*TIME+2*3.14159265*2/3))};{1};
RSRCC CINS+ CGND 1k

GPVC CGND CPVI VALUE={0.7134*V(CINS+)}
DPVC CPVI CGND DPV
RPC CGND CPVI 800k
RSC CPVI CPVO 1.6

CFC CPVO CGND 2uF rser=10m IC=0V;0.34uF rser=10m IC=0V
LPC CPVO C1 180uH rser=48m ;1000uH rser=370m;
;DDIODEC2 C1 C2B DCON;
DDIODEC C1 C2 DCON;EDDIODEC C2B C2 VALUE={-V(CD)*V(C1)/(1-V(CD))};
M1C C1 CDD CGND MSWITCH;GMIC C1 CGND VALUE={V(CD)*I(LPC)};
COC C2 CGND 20uF rser=10m IC=48V
LOC C2 C3 100uH rser=32m

EDRIVERC CDD 0 TABLE {V(CD)-V(RAMPC)} -0.0001,0 +0.0001,10
VRAMPC RAMPC 0 PULSE(0 1 0us 9.95us 25ns 25ns 10us)
RRAMPC RAMPC 0 1MEG
EDC CD 0 TABLE {V(CDINT)} 0,0 1,1
RDC CD 0 1MEG

GINTC CDINT 0 TABLE {-10*(V(CPVO,CGND)-(33.944*V(CSET)/37.367))} -10,-10 10,10
CINTC CDINT 0 1E6uF IC=0V
RINTC CDINT 0 1E8
DINTC 0 CDINT DCON
```

```
GSETC CSET 0 VALUE={-0.7134*V(CINS+)}
DSETC CSET 0 DPV
RSETC CSET 0 1MEG

RCONNECTORC1 CGND 0 0.001
RCONNECTORC2 C3 2 0.001

*****
VBATT 1 0 48.0
RBATT 2 1 0.01

.MODEL DCON D(IS=1E-15 N=0.001 BV=1k RS=1m)
.MODEL MSWITCH VDMOS(Rd=3m Rs=3m Vto=2.6 Kp=60 Cgdmax=1.9n Cgdmin=50p Cgs=3.1n
+ Cjo=1n Is=5.5p Rb=5.7m) ;Vswitch(RON=0.000001, VON=0.501, VOFF=0.499, ROFF=100MEG)
.MODEL DPV D(IS=1.6E-17 N=38.528)
**********************************************
.OPTIONS RELTOL=1e-4 ABSTOL=1e-9 VNTOL=1e-9 METHOD=GEAR
.TRAN 0.0000001 1 0 0.00001 UIC
.END
```

Appendix D: Photovoltaic Module Emulator Circuit

Scope

Due to the practical difficulties involved in trying to rotate a photovoltaic array at several hundred rpms in lab/office space, the use of an actual photovoltaic array for experimental confirmation of the PV control system is impractical. A circuit was designed which has the electrical characteristics of a PV module, but whose photo current is controlled by an electrical stimulus (so that arbitrary insolations can be modeled).

Signal Source

There are difficulties associated with the development of a low frequency oscillator circuit (such as very high capacitor and inductor values that are needed). It was suggested that a triangle wave might suffice to prove that the control system tracks insolation level, but the maximum slope of a triangle wave is much smaller than the slope of a sine wave of identical frequency.

In order to achieve a low frequency rectified sinusoid waveform a sigma delta converter algorithm was developed to convert the desired waveform to a stream of bits that could be output on the digital IO of a multifunction daq card. This necessitates the addition of a lowpass filter to the input of the PV emulation circuit.

Schematic

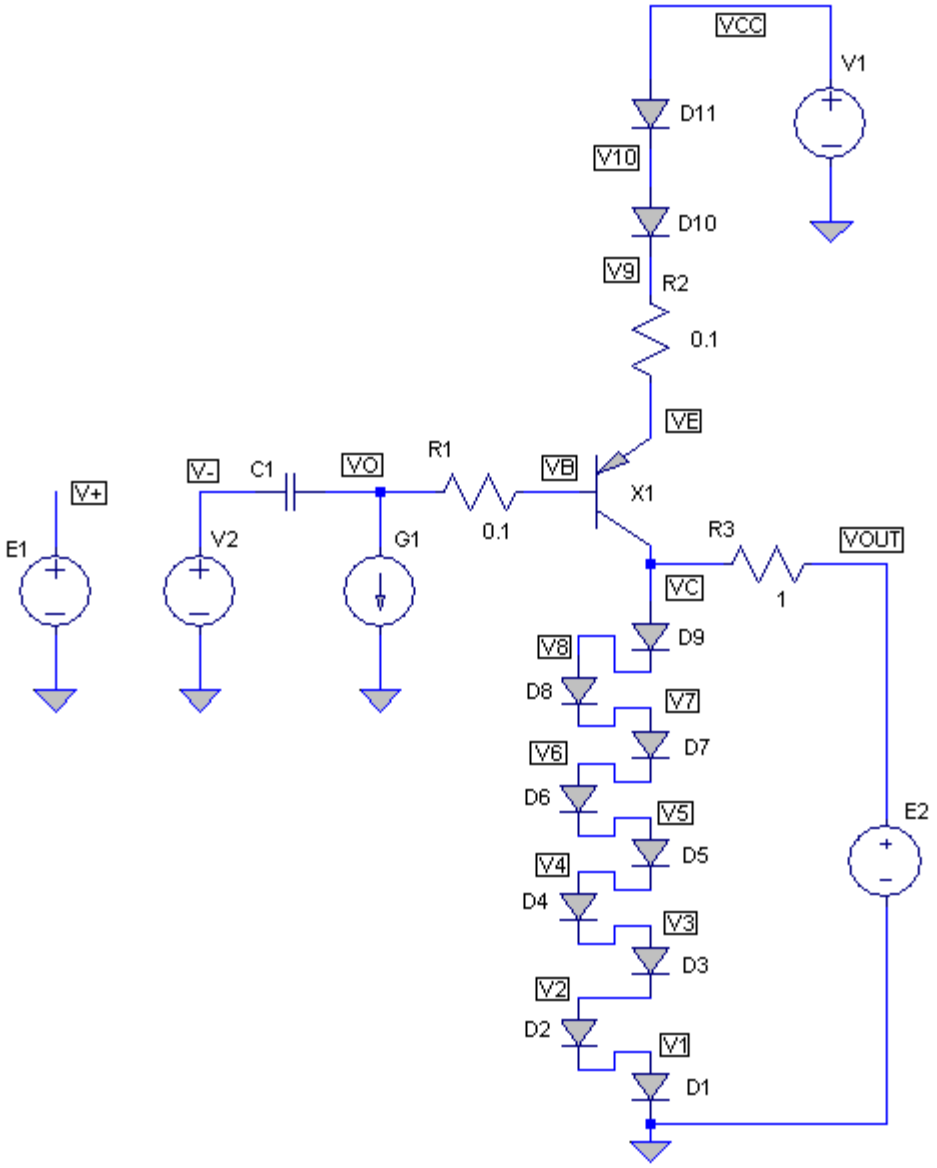

Illustration 2: Fig. D.1: SPICE Schematic of PV Emulator Circuit

The circuit described in Fig. D.1 should adequately emulate a PV module as described in the scope. The transistor acts as a current source, controlled by an integrated control loop that compares the collector current with a reference voltage value (that is low pass filtered to eliminate the sampling frequency from the digital I/O source). The sense

resistor value of 0.1Ω was chosen to maximize the measurable voltage while still keeping power dissipation below 1/4W when the collector current is $2A_{peak}$ ($1.4A_{rms}$). The load diodes were chosen to ensure that the desired test current would not cause any damage from overheating as well. The gain of the differential amplifier stage (25x) was set to convert the maximum desired current(2A) to 5V to match the maximum possible voltage from the DI/O sigma delta source. The input filter was designed to begin filtering frequencies greater than 1kHz (to allow for harmonics associated with the rectified sinusoidal source signal), but to ensure negligible switching artifacts from the sampling frequency (1MHz).

The only major concern relates to power dissipation in the transistor. A TO-220 package was selected to ensure that some reasonable level of power dissipation can safely occur, but without extra heatsinking the allowable power dissipation is limited to ~2Wrms. This is significantly less than the $6\sqrt{2}$ W that I expect to be dissipated. This limits us to running the system for short periods of time (between which we must let it cool down). Fortunately, the transient behavior we are interested in verifying can be measured within the span of a few seconds, so this limitation is not a major problem. Furthermore, the transistor can be removed and an external transistor (that is properly heatsinked) could be used if longer term operation is desired.

Simulation & Experimental Verification

The circuit described above has been simulated in SPICE, and compared to the ideal diode model description of the PV modules available in the lab. The results are very close; The emulation circuit has slightly different diode characteristics, but the V-I curve is qualitatively the same.

The circuit was assembled and measurements were taken at various load and insolation conditions. The results are consistent with the SPICE simulations, Fig. D.2

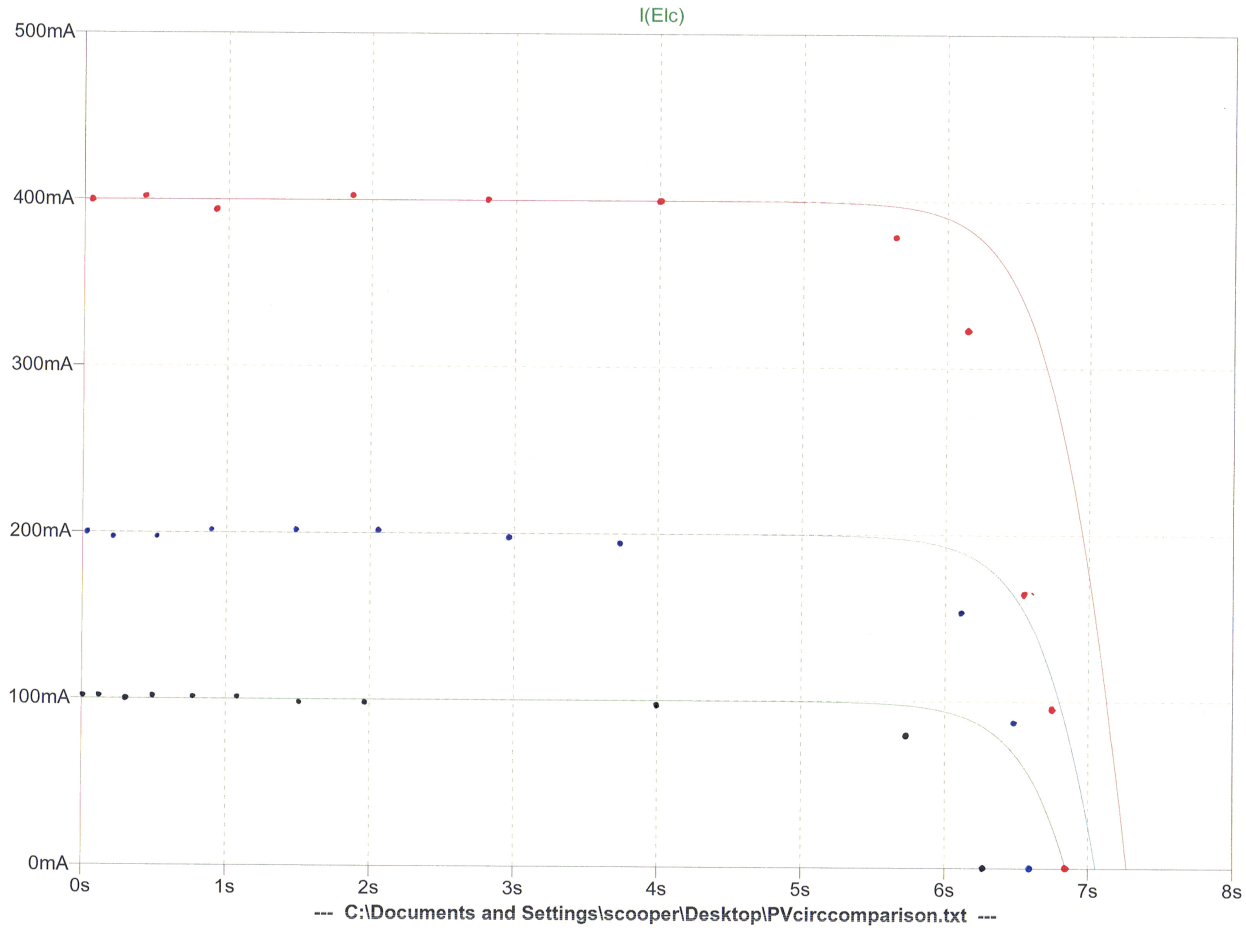

Fig. D.2: Experimental data points overlaid on SPICE simulation curves for PV Emulator Circuit

$R_{L(\Omega)}$	V(100mA$_{PV}$)	V(200mA$_{PV}$)	V(400mA$_{PV}$)
OC	6.29	6.57	6.83
75	5.67	6.32	6.78
19.2	1.905	3.76	6.15
15.0	1.496	2.965	5.59
10.0	1.021	2.025	4.02
7.1	0.719	1.429	2.836
4.2	0.430	0.855	1.712
2.3	0.2299	0.450	0.895
1.0	0.1020	0.1986	0.410
0.	0.0102	0.0200	0.0399
1.			

The SPICE text used for simulation of the PV Emulator follows:

```
.TITLE PV EMULATOR

V1 VCC 0 12V
D11 VCC V10 1N5401
D10 V10 V9 1N5401
R2 V9 VE 0.1
X1 VC VB VE TIP127
D9 VC V8 1N5401
D8 V8 V7 1N5401
D7 V7 V6 1N5401
D6 V6 V5 1N5401
D5 V5 V4 1N5401
D4 V4 V3 1N5401
D3 V3 V2 1N5401
D2 V2 V1 1N5401
D1 V1 0 1N5401

R3 VC VOUT 1
E2 VOUT 0 VALUE={TIME}

R1 VB VO 0.1
G1 VO 0 TABLE {V(V+,V-)} -0.001,0.2 0.001,-0.2
C1 VO V- 22nF
V2 V- 0 2.5
E1 V+ 0 VALUE={25*V(V9,VE)}

.MODEL 1n5401 D(IS=2.61339e-12 RS=0.0110501 N=1.20576 EG=0.6
+XTI=3.1271 BV=100 IBV=1e-05 CJO=1e-11 VJ=0.7 M=0.5 FC=0.5 TT=1e-09
+KF=0 AF=1)

********** Power BJT Electrical Model ******************
** Medium Power Linear Switching Application
```

```
** Complementary to TIP120/121/122
* Connections:    Collector
*                | Base
*                | |  Emitter
*                | | |

.SUBCKT TIP127    1  2  3
*
Q1 1 2 4 Q1model
Q2 1 4 3 Q2model 4.761
D1 1 3 Dmodel
R1 2 4 8.000E3
R2 4 3 120

.MODEL Dmodel D
+  IS   = 6.3512E-13 RS   = 0.7712053    IKF = 7.046441E-4
+  N    = 1          BV   = 120          IBV = 0.1
+  CJO  = 1E-12      VJ   = 0.75         M   = 0.33
+  FC   = 0.5

.MODEL Q1model PNP
+  IS   = 1.286E-12  BF   = 1.099E3      NF  = 1
+  VAF  = 75         IKF  = 3.510E-2     ISE = 7.098E-12
+  NE   = 1.44       BR   = 0.7076       NR  = 1
+  VAR  = 26         IKR  = 0.801        ISC = 5.1292E-12
+  NC   = 1.0        RB   = 26.90        RE  = 0.00001
+  RC   = 0.00473    EG   = 1.110        CJE = 8.176E-11
+  VJE  = 0.813      MJE  = 0.320        CJC = 9.670E-11
+  VJC  = 0.591      MJC  = 0.242        XCJC = 0.3807
+  FC   = 0.5

.MODEL Q2model PNP
+  IS   = 1.286E-12  BF   = 1.099E3      NF  = 1
+  VAF  = 75         IKF  = 3.510E-2     ISE = 7.098E-12
```

```
+ NE   = 1.44      BR   = 0.7076      NR  = 1
+ VAR  = 26        IKR  = 0.801       ISC = 5.1292E-12
+ NC   = 1.0       RB   = 26.90       RE  = 0.00001
+ RC   = 0.00473   EG   = 1.110       CJE = 8.176E-11
+ VJE  = 0.813     MJE  = 0.320       CJC  = 0
+ VJC  = 0.75      MJC  = 0.33        XCJC = 0.3807
+ FC   = 0.5
.ENDS
** Creation Nov-29-2002
** Fairchild Semiconductor

**********************************************
.OPTIONS RELTOL=1e-3 ABSTOL=1e-6 VNTOL=1e-6 METHOD=GEAR
.TRAN 0.0000001 25 0 0.00001 UIC

.END
```