Implementation of an LNA as a Preamplifier for a 7T MRI

By:

Daniel H. Miller Minkel

Luis D. Sanchez Martinez

Brendan M. Train

May 6, 2021

Major Qualifying Project submitted to the Faculty of:

WORCESTER POLYTECHNIC INSTITUTE

In partial fulfillment of the requirements for the degree of

Bachelor of Science

Advisor:

Professor Reinhold Ludwig

Abstract

This MQP report describes the implementation of a low noise amplifier (LNA) as a preamplifier for a 7T Magnetic Resonance Imaging (MRI) machine. The background explores the need for LNAs and the general noise, gain, and applications of LNAs. Our design targets a noise figure of at most 0.5dB in order to not corrupt the signal received by the 300 MHz MRI coil. We next discuss the testing of existing LNAs, as well as the design, assembly and testing process for our LNA. In our design process, we investigated the suitability of several designs and layouts for our amplifier. Also included in our report is a breakdown of the costs associated with the project, including the financial costs of testing materials and construction components, as well as the social and environmental impact of a theoretical large scale production run of this amplifier.

Table of Contents

List of Figures

List of Tables

1.0 Introduction

The modern world of smartphones, satellites, GPS, and medical imaging requires accurate transmission and reception of very faint, high frequency signals through noisy environments with little to no loss for effective functioning. In regards to magnetic resonance medical imaging, scanners using stronger magnetic fields which can accurately visualize and quantify functional changes in brain activities. [1] Currently, work is being done at Northeastern University to evaluate the ability of 7 Tesla (7T) MRI scanners to accurately gather this type of data. However, these higher field strength scanners require specialized amplifiers tuned to operate at the higher Larmor frequencies that result from increasing the strength of the magnetic field. Our group evaluated several existing amplifiers to determine their limitations when working with a higher strength 7T MRI system operating at approximately 300MHz, such as the one used at Northeastern University, and used that information to design an amplifier specifically for that MRI scanner.

2.0 Background

This section covers the functionality and some of the fundamental behavior of LNAs. A brief summary of some of the characteristics that are important considerations when working with these devices, such as linearity, noise, and gain, is also included. A study of relevant literature was also conducted to establish the equipment and standards being used, which established the best practices by which our amplifier was designed, constructed and evaluated.

2.1 Need for Low Noise Amplifier

The role of an LNA is to boost the power of an inputted analog signal to a sufficient level above the noise floor so that it can be put through additional processing steps. Therefore, the Noise Figure (NF) of an LNA directly limits the sensitivity of the receiver. The NF of a particular amplifier can be shown as a relationship between the input and output signal-to-noise ratio, which is shown by Figure [1]

$$NF = \frac{S/N(in)}{S/N(out)} \quad (1)$$

Here, S/N(in) is the input signal to noise ratio, and S/N(out) is the output signal to noise ratio of a general two-port network.

With this fact in mind, LNAs are designed with a focus on maintaining a low noise figure, often at the cost of reduced gain, as opposed to more common amplifiers, which frequently prioritize increases in gain over noise minimization. [2].

In the context of MRI equipment, LNAs are used as preamplifiers, responsible for amplification of the induced signal from the RF coils, before any other processing is performed. Minimizing noise is critical at this step, as any noise produced in this stage will be further

amplified through the rest of the signal chain. This means that MRI preamplifiers typically have lower gains (often below 20 dB) than could be produced by traditional amplifiers.

2.2 Definition of the LNA

In medical imaging and wireless applications, a LNA is an active network that increases the amplitude of weak RF signals to allow processing by a receiver chain. In order to prevent signal degradation, LNAs are typically placed as close as possible to the signal source to prevent interference or attenuation from being introduced in a transmission line. They are tuned with a focus on introducing a minimal amount of noise into the signal, usually by lowering the gain. LNAs are one of the most important circuit components present in radio and other signal receivers. Figure 1 is the block diagram of a typical LNA.

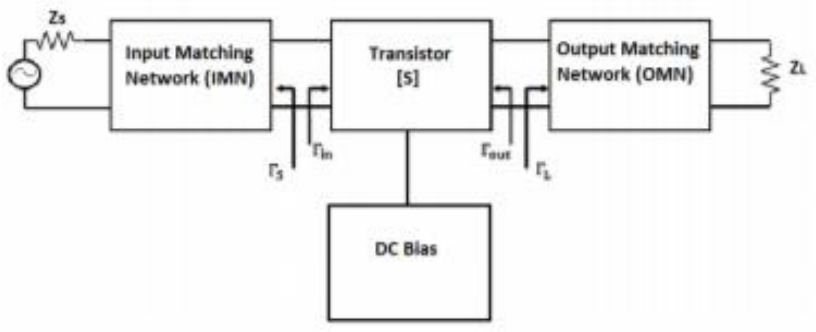


Figure 1: Block Diagram of a Typical LNA [3]

The block diagram in Figure 1 shows how a basic LNA is constructed. The general LNA topology is composed of three stages: 1. the Input Matching Network (IMN), 2. the actual Amplifier design block with the selected transistor [S], and 3. the Output Matching Network (OMN). In our case, the input is a Thevenin equivalent voltage model, consisting of an

equivalent source resistance and voltage, located on the left most side of the Figure 1 block diagram. The input and output matching networks typically consist of reactive elements including microstrip transmission lines, as well as capacitors and inductors, used to match the impedances of the amplifier to the source and load impedances of the device. Matching is needed to ensure optimal power transfer as well as maintaining the stability of the active device.

The transistor in the block diagram in Figure 1 represents the specific transistor that was selected for the LNA. The designers need to assess what type of transistor is needed according to their circuit specifications and requirements. The Scattering Parameters, or S-Parameters are linear, high-frequency system descriptors that are used to model the transistor block. Device manufacturers generally report four parameters: S(1,1), S(2,2), S(2,1), S(1,2) which are, respectively, input reflection coefficient, output reflection coefficient, forward voltage gain, and reverse voltage gain. The S-parameters will be used in part to assist the designer in choosing the matching element values needed to be placed around the active device (transistor) in order to achieve the desired amplifier performance. In RF engineering and when designing an amplifier we need to deal with high frequency, and thus it becomes essential to describe a network in terms of voltage and current waves rather than conventional voltages or currents. [4]

2.2.1 Linearity and Sensitivity

Depending on the application, the linearity of an LNA is of varying importance for the receiver. The main purpose of the LNA is to increase the received signal so it can be utilized for additional processing, and this task is compromised if the LNA preforms nonlinearly. [5] The non-linearity of LNAs is frequently a consideration when designing RF circuits, particularly in the front end of wireless receiver circuits. One of the main reasons is that the non-linearity of a

LNA can make the demodulating and decoding of a transmitted message more difficult. [6] In our application, however, non-linearity is less of a factor, as MRIs operate within narrow frequency bands. The sensitivity figure (given in dBm) expresses how effectively the receiver will capture incoming signals. The main purpose of medical MRIs is to capture weak induced signals from the RF coil and resolve them into detailed images of the various anatomical structures of the body. In order for the MRI scanner to produce clear images at the higher resolution of 7T MRIs, it is important that the receiver is as sensitive as possible, without introducing enough noise to drown out the small desired signal. In particular, the LNA that makes up the first stage of the reception signal chain must provide the maximum possible amplification without distorting or obscuring the target signal. The sensitivity of the minimum input signal is:

$$S = NF + n_0 + \frac{S}{N} \quad \text{(2)}$$

Adapted from [7], Equation (2) "denotes S as the minimum input signal in (dBm), where NF is the noise figure of the receiver in dB, S/N is in the output signal to noise ratio in dB, and n_0 is the thermal noise power of the receiver in (dBm)."

2.2.2 Noise

Noise in amplifiers can originate from a number of sources, each of which can broadly fall into the categories of external and internal noise. Internal noise is generated by the various components of the amplifier, while external noise originates from a noisy input signal [8].

2.2.2.1 Internal Noise

Internal noise can be caused by many different factors, but the most common types of noise are Johnson, shot, and transit time noise [8].

Johnson noise is caused by the thermal agitation of charge carriers in a circuit. In essence, charge carriers are agitated by the thermal conditions of their environment. Thus, depending on the exact temperature of the circuit, more noise is typically introduced as the temperature of an amplifier increases. Considering that amplifiers generate heat during operation, it is important to not only ensure that the amplifier is insulated from outside temperature changes but is also adequately cooled to prevent heat from increasing the temperature of the amplifier as it continues to operate.

Shot noise occurs because, at the subatomic level, the flow of electricity exists as the movement of electrons as discrete quantities of charge. When working with the extremely small voltages of the type that are frequently found when LNAs are employed, the discrete movement of charge carriers across the P-N junction is not entirely uniform and introduces a type of noise that is difficult to mitigate and must simply be accounted for when working with the signal output from the amplifier [9].

Transit time noise is a frequency dependent noise type that results from the delay introduced by the charge carriers as they move from input to output. At high frequencies, this transit time noise becomes prominent.

Most of these types of noise mechanisms are difficult to individually quantify, and even more difficult to effectively mitigate without the creation of custom transistors, a task which is outside the scope of this project. For our purposes, internal noise is best quantified by the noise figure (NF) which refers to the overall increase in noise throughout a signal chain. While we can

minimize this value by selecting components and design layouts appropriate for our application, there will be some unavoidable noise contributions that are introduced through these processes.

2.2.2.2 External Noise

External noise is more straightforward in its origins and there are methods of minimization. This type of noise consists of electromagnetic fluctuations induced by both manmade sources, as well as environmental influences including cosmic radiation and atmospheric noise. Environmental factors are unavoidable but may be mitigated by isolating components from external interference as much as possible using Faraday shielding, for example.

Man-made noise falls into two major categories, environmental and local. Environmental noise includes high frequency radio transmissions, as well as the electromagnetic field coupling induced by in wall electrical wiring. While some effort can be made to reduce this type of noise by eliminating nearby sources such as wireless routers or microwave ovens, many of these sources are unavoidable, and must simply be shielded from in a similar manner to natural environmental factors.

The other type of man-made noise comes from sources within the same piece of equipment or even within the same circuit as the device being isolated. Typical larger scale shielding is less practical, at this scale, so other methods must be employed. Equipment and circuitry can be designed by selecting components to minimize generated noise, and to physically separate the noise generating components from the noise sensitive components [10].

Taken as a whole, noise is frequently described in the form of a Signal to Noise Ratio (SNR); this value measures the relative power of the desired signal compared to the power of the noise that is also present. External noise can be a major contributor to a small SNR, and can be

mitigated with proper shielding, but not entirely eliminated. Also, important to consider is the Noise Figure (NF), discussed previously, which explicitly quantifies the noise added by the system. Taken together, these metrics help to quantify how much noise is being amplified or introduced into a signal by sources both within and outside of the signal chain and helps determine whether the increases in signal strength outweigh the increases in noise. While an ideal system would have a NF of 0 dB, indicating that no additional noise is introduced by a particular step in the signal chain, some increase in noise always occurs in real world amplifiers.

2.2.3 Gain

Gain is, at its most basic level, the quantization of the change in signal power from the input to the output of any electrical system. In the case of amplifiers, gain measures the increase in signal power from the input to the output terminals of the device. This gain is usually measured in decibels (dB).

When working with amplifiers, higher gain is generally better, but usually comes at the cost of increased noise. For LNAs, the main priority is minimizing noise, so LNAs typically see smaller per stage gains than other types of amplifiers. Current LNAs typically seek to maintain a noise figure of less than 1 dB, with gain usually measuring between 20 and 30 dB .

2.3 Applications of LNAs

LNAs are used in many applications, including systems which operate at higher (RF) frequencies, including cases where incoming signals are extremely faint, and where the introduction of noise can seriously impact the performance of later processing or analysis. However, LNAs typically have narrow frequency bands, and also typically exhibit lower gain than many other types of amplifiers.

LNAs are often used in wireless receivers, both in cellular communication devices, as well as medical scanners, where the input is typically a small signal at a fixed frequency, and where even small increases in noise can have serious impacts [11].

2.4 Literature Review

In order to establish the target gain and noise figures for our proposed amplifier, we investigated the current trends in amplifier design for MRI applications. Along with establishing a target for the key performance characteristics, this research gave us insight into the performance of amplifier components and designs currently employed in industry.

Yadav, S. [12] designed a LNA for a 1.5T MRI scanner using cascode technology. This LNA has a noise figure close to 0.6 dB with a gain greater than 20 dB at a frequency of 63.87 MHz (consistent with a 1.5T MRI system). While this amplifier is in the wrong frequency band for the 7T, 300 MHz application that this project is focused on, it helped to both establish a desired set of performance characteristics and provided a potential topology for consideration.

E. O. Farhat, et. al. [14] designed a Wideband CMOS LNA for low frequency applications (50-350 MHz). They utilized the inductive source degenerated topology in order to provide a much lower NF than some of its resistive based counter designs. The LNA has a noise figure close to 0.32 dB with a gain of 38 dB. While these values are excellent, the amplifier is based on a multi-stage cascode design, which increases complexity compared to a single stage amplifier.

Das, T [13] investigated several amplifier topologies, and discussed numerous design considerations for amplifiers, including transistor type and board type and layout. In particular, it

identified that, while Cascode designs are highly linear and typically have wide operating bandwidths, their NF is typically higher than a common source design.

Based on our review of literature, it was determined that a common source amplifier, while less stable and with narrower bandwidth than other amplifier designs, has the potential for a lower NF. For MRIs, where the operating frequency range is narrow, a narrow band amplifier with limited stability does not present any significant negatives, but the minimal NF is potentially beneficial.

Transistor selection was also considered, with a focus on HBTs, HEMTs, PHEMTs and MESFETs.

Pavlidis, D [19] found that, when designing LNAs, PHEMTs are usually preferred, as their deployment helps to minimize thermal noise, while also minimizing the reductions in gain required to remain below the target NF.

3.0 Project Statement and Objectives

The LNA is an important building block at the front end of the signal receiver chain found in MRI machines. The preamplifier is the first block after the RF receive coil that will accept the MR signal and amplify it, while introducing as little additional noise as possible. MR signals obtained by the RF coil rely on very little added noise during the amplification process in the front end in order to ultimately achieve high resolution imaging. Our project targeted the design and implementation of an LNA with a NF of less than 0.5dB at a frequency of 298 MHz in an attempt to improve the resolution and sensitivity of the Bruker BioSpec 70/20 MRI scanner at Northeastern University's Center For Translational NeuroImaging.

4.0 Methodology

In order to successfully develop a custom LNA for a higher frequency 7T MRI, research was conducted to evaluate the potential for various designs and components to reach the desired values for noise figure and gain. With this information, extensive simulations were conducted using Keysights PathWave Advanced Design System (ADS), to simulate and evaluate the performance of various amplifier designs.

This information was used to design a PCB, order components, and assemble a physical version of the simulated LNA. However, shipping delays meant the physical prototype LNA was not completed in time for testing to be performed. Ideally, laboratory testing would have been performed to evaluate the noise, gain, and power characteristics of both the prototype LNA, as well as a commercially available LNA 'demo board', to confirm that the prototype performed both in line with the simulations, and better than LNAs currently on the market.

4.1 Active Device Selection

The first step in the design process of our custom LNA was to select a suitable transistor based on the requirements outlined previously. The main considerations when selecting our transistor were the noise figure, the gain, and the operating frequency range of the transistor. We selected the ATF-54143 HEMT produced by Avago Technologies based on its low noise figure, relatively high gain, and low cost . These characteristics are broken down in Table 1

Table 1: LNA requirements and ATF-54143 specifications

	LNA Requirements	ATF-54143
Transistor Type	PHEMT	PHEMT
Frequency Range	298 MHz	0.1 - 10 GHz
Noise Figure (NF)	0.5 dB <	0.5 dB (at 0.3 GHz)
Gain	≈20 dB	16.6 dB
Power Consumption	200 mW	Max of 725 mW

To match the Lamor frequency of the Bruker BioSpec 70/20 MRI being used at Northeastern University, our amplifier must be designed with a center frequency of 298 MHz. The selected transistor, the ATF-54143, has a baseline NF of .15 dB at the target frequency. While the baseline gain of the transistor at this frequency is listed as 16.6 dB, Figure 2 indicates that the transistor has a Maximum Stable Gain (MSG) and Maximum Available Gain (MAG) of between 27 and 34 dB. This range is based upon an amplifier which has an identical input impedance to that of the signal source resistance. For our application, where our signal source already has an approximately matched impedance to the transistor, it should be possible to achieve an overall amplifier gain close to the MSG, without any decrease that might be introduced by a matching network. The typical scattering parameters, important for the stability analysis, as well as the reference biasing voltage (V_{DS}) and current (I_{DS}), are summarized in

Figure 2.

ATF-54143 Typical Scattering Parameters, $V_{DS} = 3V$, $I_{DS} = 40$ mA

Freq.	S_{11}			S_{21}		S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.99	-17.6	27.99	25.09	168.5	0.009	80.2	0.59	-12.8	34.45
0.5	0.83	-76.9	25.47	18.77	130.1	0.036	52.4	0.44	-54.6	27.17
0.9	0.72	-114	22.52	13.37	108	0.047	40.4	0.33	-78.7	24.54

Figure 2: ATF 54143 Typical S-Parameters

The selected device was incorporated into a circuit simulated in ADS, using a model provided by Avago [20]. The internal layout of the transistor model is shown in Figure 3:

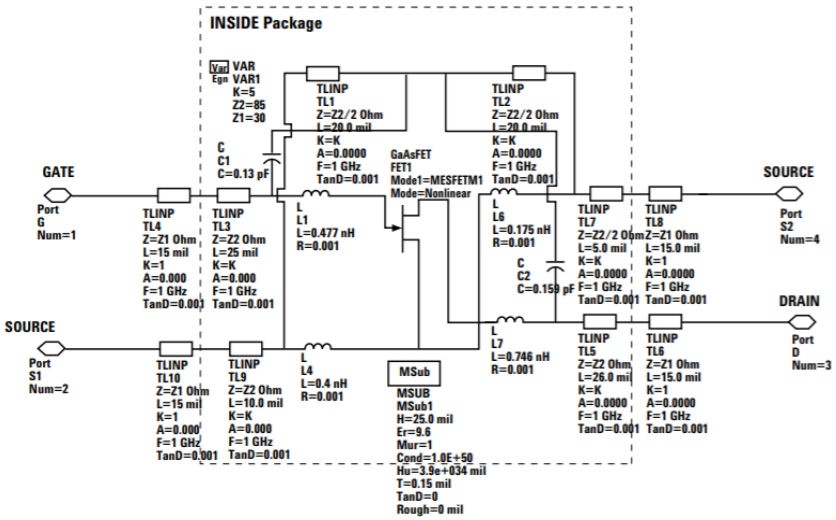


Figure 3: ATF-54143 layout ADS Model

Figure 3 shows the active FET device embedded by transmission line sections denoted by TLINP; they model bondwires at the gate-drain input and the drain-source output. In addition, inductive and capacitive coupling elements are seen, along with information regarding the substrate (MSub), such as board height, trace thickness, dielectric properties, loss tangent, conductivity, etc.

4.2 DC Bias and Stability

We imported the component ATF-54143 into our ADS simulator workspace and started the schematic design process by ensuring that the transistor had a DC biasing circuit to achieve the required DC operating points. According to the vendor [20] “the ATF-54143 enhancement mode PHEMT requires about a 0.6V potential between the gate and source for a nominal drain current of 60 mA” [18].

Once we established the appropriate DC bias conditions we added a shunt RC circuit to our LNA design to provide resistive loading and thus improve the stability of our circuit. We selected a value of 150 Ω and 2 pF, which was high enough to achieve unconditional stability within our operational frequency range, but not so high as to compromise the Noise Figure of our LNA. [21] Our main goal in the first stage of the design of the LNA schematic was to achieve a higher gain than our target (>20dB) as well as a slightly lower NF (<0.5dB) to have flexibility in our design in case we had to compromise a value in later stages of the design process. The addition of the RC shunt was to design our LNA to be unconditionally stable. The selected values then were a 150 Ω resistor and a 2 pF capacitor. In Figure 4 we can observe the circuit of our LNA and in Figure 5 the simulation results of the circuit.

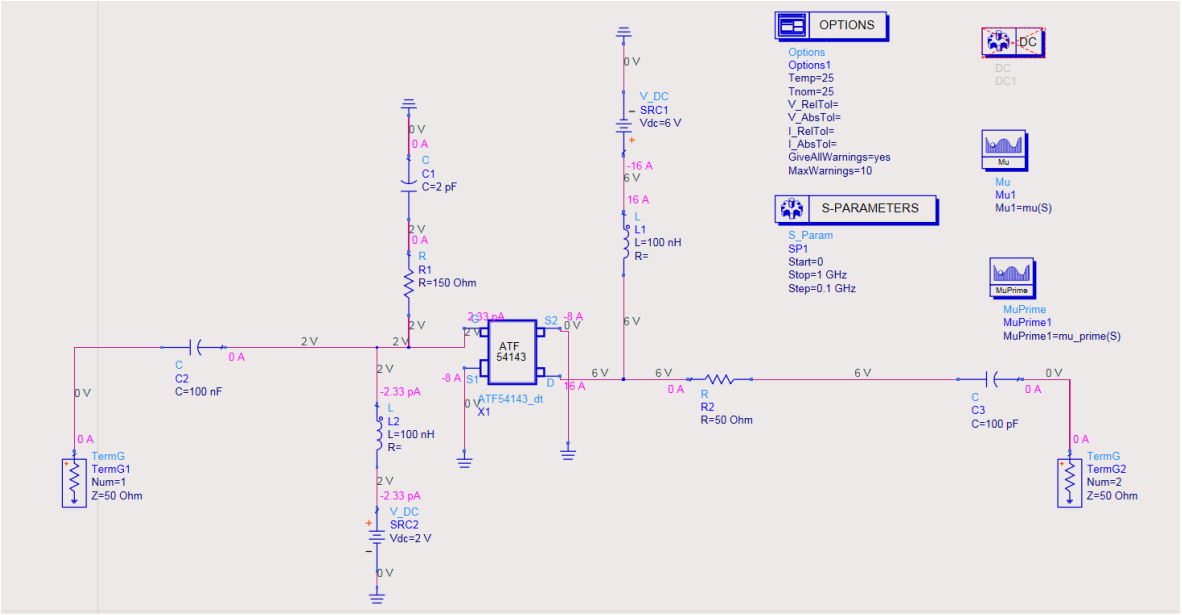


Figure 4: DC Bias and Stability Schematic of our LNA Circuit.

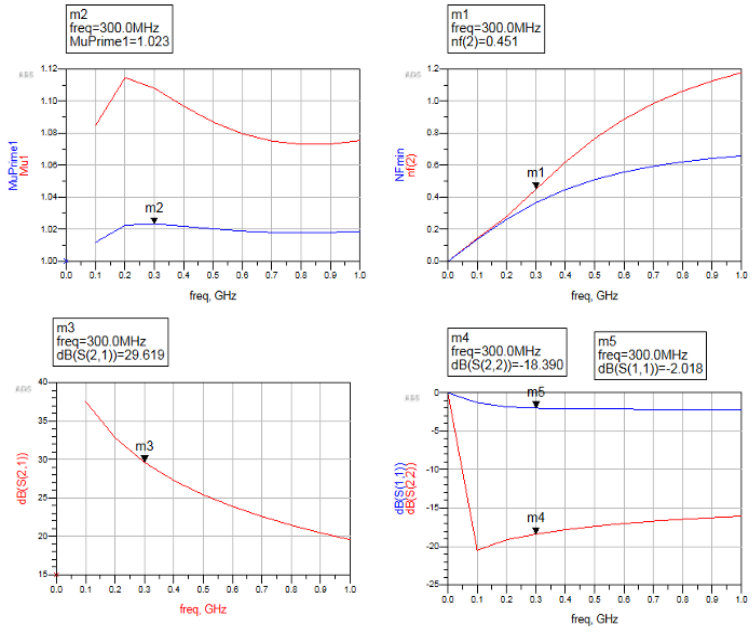


Figure 5: Simulation results; the four graphs are explained in the text.

In Figure 5 we have provided the results of the simulations conducted in Advanced Design System by Keysight Technologies. All simulations were conducted at a frequency of 300 MHz (defined by markers) and over a range of 0 to 1 GHz. For the purposes of the DC Bias and Stability simulation we modeled the following parameters depicted in Figure 5:

1) Stability analysis (upper left)
2) Noise Figure (upper right)
3) S(2,1) Forward Voltage Gain (lower left)
4) S(1,1), S(2,2) Input and Output Reflection Coefficients (lower right)

For our stability analysis we utilized the Mu prime measurement tool in ADS to assess the overall stability of our circuit. According to Keysight the Mu prime measurement "Returns the geometrically derived stability factor for the source" [22]. The results of this simulation can be observed in the upper left quadrant of Figure 5. We successfully achieved stability with a value of 1.023. In order for a circuit to be stable according to the measurement used the value has to be over 1.

Next, we wanted to simulate the Noise Figure since this is a key measurement for the design of our LNA. The Noise Figure simulation results can be observed in the upper right quadrant of Figure 5. We obtained a Noise Figure of 0.451dB at a frequency of 300 MHz. This is below our target of 0.5dB and very close to 0.38dB, the minimum Noise Figure of our active device

Another important measurement we conducted during the simulation was measuring the voltage gain S (2,1). This can be observed in the lower left quadrant of Figure 5. We achieved a voltage gain of 29.619 when operating at 300MHz. This gain is more than our target gain and this is very beneficial for our project.

4.3 PCB Layout

In this section, we will discuss the creation of our PCB prototype as well as how we planned to obtain our PCB.

4.3.1 PCB Prototype

In order to create our PCB layout, the LNA circuit schematic was recreated in an application called EasyEDA. We chose to use EasyEDA because it will convert circuit schematics in gerber layout files so ordering of the PCB is possible. Figure 6 shows the recreated circuit schematic in EasyEDA and Figure 7 shows the PCB prototype layout.

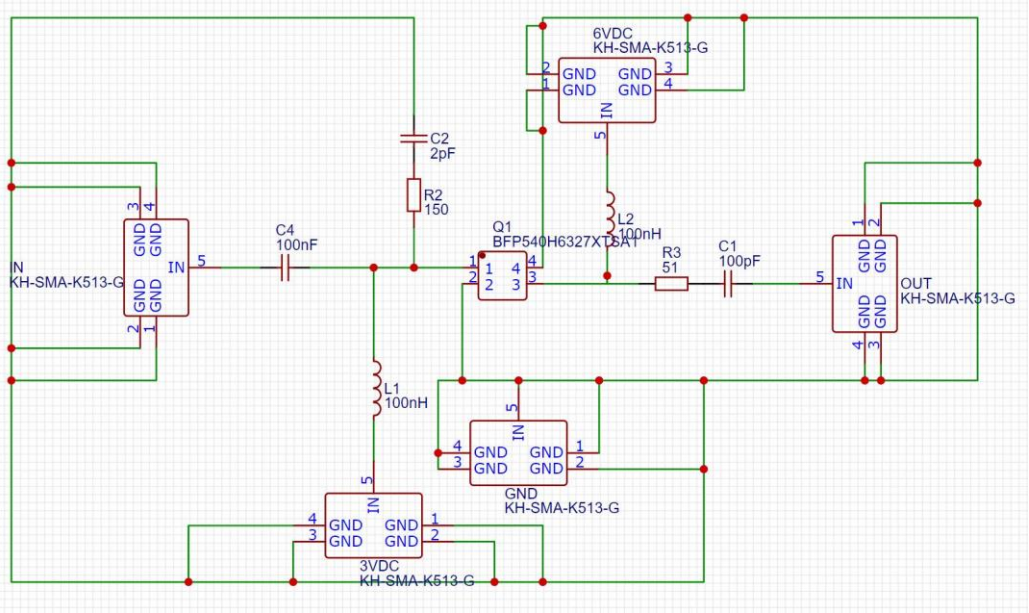


Figure 6: PCB schematic of the prototype LNA

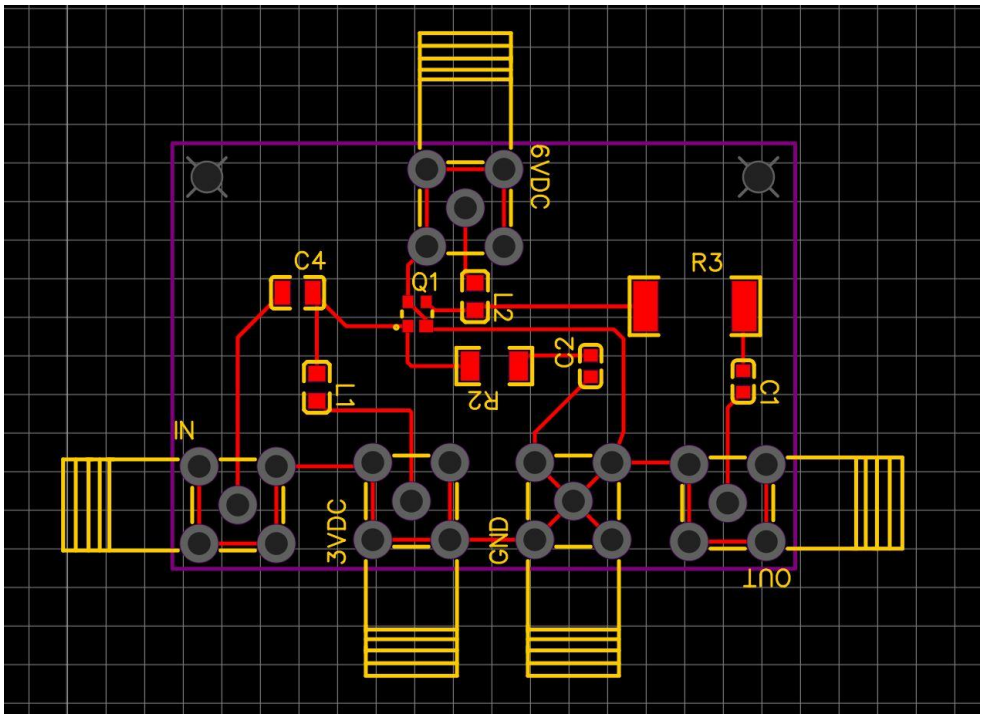


Figure 7: PCB Layout

4.3.2 JLCPCB

After the creation of the PCB prototype layout, we used JLCPCB to order our prototype board. JLCPCB populated everything on the PCB except for the transistor, since our active device is not a transistor that JLCPCB offers through its parts library.

4.4 Budgeting

In developing and testing the LNA described in this report, two key financial requirements were identified. The first is the acquisition of an existing, tuned LNA, frequently called a demo board. The second is all the costs associated with fabricating a PCB and assembling a functional circuit.

4.4.1 Reference LNA Acquisition

Early on in the project, it was determined that having at least one LNA demo board to validate the efficacy of the testing procedure, as well as provide a baseline which the LNA designed for the project should surpass in NF and Gain. Initially, attempts were made to borrow these boards, as their cost would prevent the purchase of more than one device. However, these inquiries failed to acquire any amplifiers, so a single amplifier was selected to purchase directly. Several amplifiers were considered, and ultimately, the Analog Devices HMC639ST89 was selected, due to its availability, and the fact that it is internally matched to 50 ohms, which allows for comparative testing without having to develop a custom matching network that might affect the measured performance as compared to the listed capabilities.

4.4.2 Prototype construction

The cost of PCB production and assembly is relatively low. JLCPCB [23], a custom PCB fabrication and ordering company, is capable of rapidly producing high quality PCBs and installing all of the components we require, except for the transistor. Their limited library of available parts meant that the only hand assembly our team had to perform was the installation of the transistor onto the board. Table 2 outlines the total cost of PCB fabrication, component acquisition, and assembly.

Table 2: PCB Assembly Cost Breakdown

Item	Part #	Unit Cost	Quantity	Total
Resistor (51 ohm)	0805W8F5102T5E	$0.09	1	$0.09
Resistor (150 ohm)	TC0525B1500T5E	$1.11	1	$1.11
Resistor (100 ohm)	TC0525D1000T5E	$.50	1	$0.50

Capacitor (2 pF)	0805CG2R0C500NT	$0.14	1	$0.14
Capacitor (100 pF)	CL10C101JB8NNNC	$0.24	1	$0.24
Inductor (100 nH)	SDCL1608CR10JTDF	$0.28	1	$0.28
SMA Connector	KH-SMA-K513-G	$0.42	5	$2.10
AD HMC639ST89	1127-1501-1-ND	$6.41	1	6.41
PCB Fabrication / Assembly		$5.00	1	$5.00
Total Cost				$15.87

Including a large margin for cost overruns, including rush assembly, the total cost of creating the PCB and assembling all the components is below $30 dollars.

4.4.3 Theoretical mass production

Transforming the prototype circuit into a commercial product suitable for mass production and use in functioning 7T MRI scanners involves several considerations. Most important is the requirement for LNAs being deployed in the vicinity of strong magnetic fields, such as those generated by MRI scanners, to use non-magnetic components. For the initial prototyping and testing conducted during the project, this requirement was eliminated to reduce the time and cost of prototyping. Non-magnetic components can cost 5-10 times more per unit than their magnetic counterparts, and are generally more difficult to acquire in small quantities as required for prototyping. For the purposes of mass production, this complication could be mitigated by working directly with manufacturers to reliably secure the required components, and at a reduced per unit cost given the relatively high quantity of orders.

5.0 Results

In this section, we look at the comparison between the prototype LNA and the reference LNA to show the success of the prototype LNA.

5.1 Simulated Reference LNA

In order to compare our prototype LNA to our reference LNA, we simulated the reference LNA using the same S-Parameters simulations as the prototype LNA. Figure 8 below shows circuit schematic was acquired from the datasheet for the Texas Instruments HMC639.

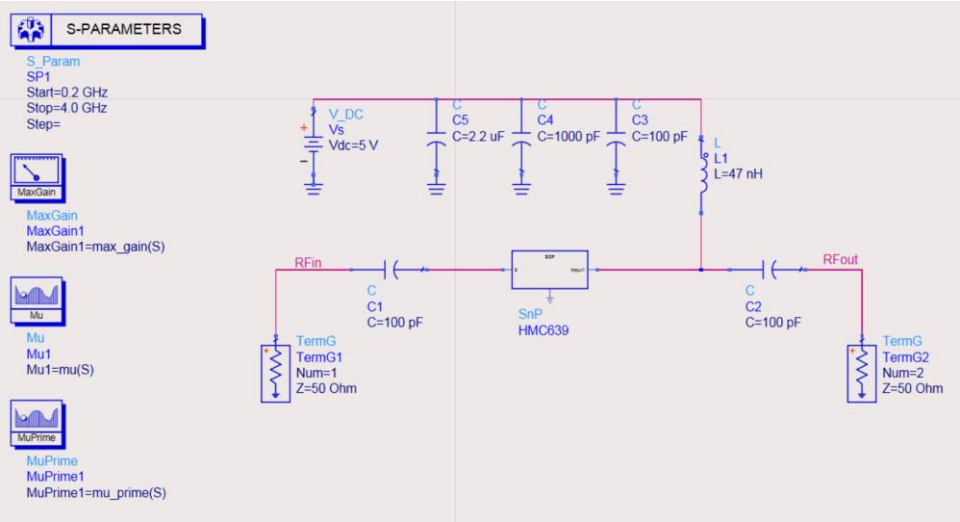


Figure 8: HMC639 Circuit Schematic

After the circuit schematic of the HMC639 was simulated, it was found out that the reference LNA massively underperforms at 297.4MHz with a gain of only 11.122 dB. Figure 9 shows the gain vs frequency graph for the Texas Instruments HMC639.

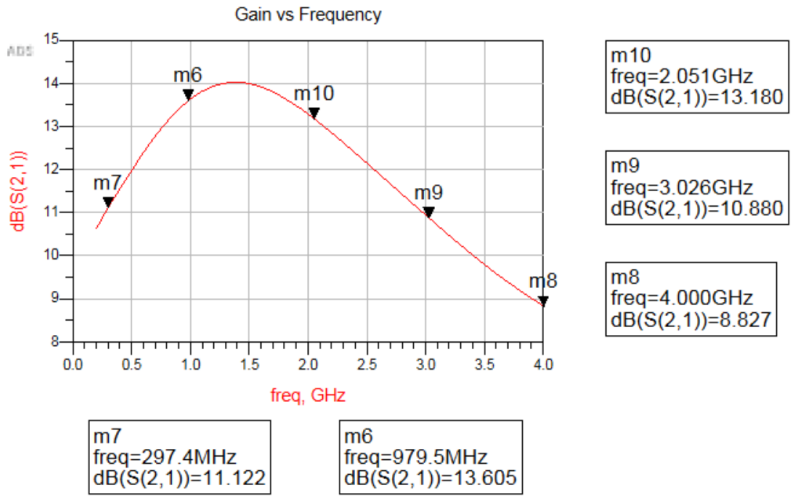


Figure 9: HMC639 Gain vs Frequency.

5.2 Reference vs Prototype

In this section, we will be comparing our prototype LNA with the reference LNA. The comparison will look at both gain and noise figure.

5.2.1 Gain Comparison

When simulated at approximately 300MHz, the prototype LNA reached a gain of 29.619 dB, while the reference LNA only achieves a gain of 11.122 dB. Our prototype LNA achieves such a high gain at 300MHz because it is designed for an extremely narrow bandwidth and is considered unconditionally stable by a very thin margin, across a much narrower bandwidth than our reference LNA. This means that if a different MRI operating at a frequency even slightly offset from our 298 MHz target attempts to make use of our amplifier design, the device will perform far worse than the reference LNA, and may not be stable at all.

5.2.2 Noise Figure Comparison

When simulated at approximately 300MHz, our prototype LNA has a noise figure of 0.451 dB. When looking at the datasheet, the reference LNA has a noise figure of approximately

3dB at 300MHz. We used the datasheet noise figure for the reference LNA because the ADS models that the manufacturer provided did not include the necessary information to perform noise simulations. The prototype achieves its low noise figure by minimizing the frequency range within which the device is expected to operate, in contrast to our reference LNA, which is designed to operate across a much broader frequency range, necessitating an increase in minimum noise figure.

6.0 Discussion

Due to various circumstances, most notably the delays caused by COVID-19, the entire timeline of the project was stretched, which meant that the scope of the project was significantly reduced from initial plans, and, ultimately, delays in the assembly of components required to construct our prototype meant that physical testing could not be completed within the timeframe of the project. However, the excellent performance of our simulated designs achieved our main objective of developing an amplifier to meet our specific performance goals.

6.1 Continuing Research

Although the project is completed, there are many avenues of research that would be beneficial if pursued. Key among these is completion of the physical prototype, and evaluating its performance under laboratory conditions.

The results of such laboratory testing would greatly aid in the development of a second prototype amplifier, constructed from non-magnetic components, and designed for use in a real-world MRI system. This field testing would go beyond the simple noise and gain objectives established for this project, and would help evaluate whether the prototype amplifier developed in this project actually resulted in increased effectiveness of an MRI, be it in image quality, scanning speed, or other areas.

Bibliography/References

[1] M. E. Ladd, P. Bachert, M. Meyerspeer, E. Moser, A. M. Nagel, D. G. Norris, S. Schmitter, O. Speck, S. Straub, and M. Zaiss, “Pros and cons of ultra-high-field MRI/MRS for human application,” Progress in Nuclear Magnetic Resonance Spectroscopy, vol. 109, pp. 1–50, 2018.

[2] *An Introduction to Low Noise Amplifier Specifications*. oneSDR, 2020. https://www.onesdr.com/2020/01/11/an-introduction-to-low-noise-amplifier-specifications/

[3] Mustafa A. Kabel, *Ultra-Low Noise Amplifier Design for Magnetic Resonance Imaging systems*. DTU Electro – Technical University of Denmark Electromagnetic Systems Group, 2017. https://arxiv.org/ftp/arxiv/papers/1706/1706.03507.pdf

[4] *S-Parameters.* Microwaves101, 2020. https://www.microwaves101.com/encyclopedias/s-parameters [Accessed: 2-Nov-2020].

[5] William R. Deal, Vesna Radisic, Yongxi Qian, Tatsuo Itoh, *Microwave Active Circuits and Integrated Antennas*, The Electrical Engineering Handbook, 2005. https://www.sciencedirect.com/science/article/pii/B9780121709600500487 [Accessed: 24-Oct-2020].

[6] Schweber B. , *Understanding the Basics of Low-Noise and Power Amplifiers in Wireless Designs.* Digi-Key Electronics, 2013. https://www.digikey.com/en/articles/understanding-the-basics-of-low-noise-and-power-amplifiers-in-wireless-designs

[7] Maxim Integrated Products, Inc, *IMPROVING RECEIVER SENSITIVITY WITH EXTERNAL LNA*, 2003. https://www.maximintegrated.com/en/design/technical-documents/app-notes/1/1836.html
[Accessed: 24-Oct-2020].

[8] S. V. Hum, “Noise in Radio Systems.” [Online]. Available: https://www.waves.utoronto.ca/prof/svhum/ece422/notes/21-noise.pdf.

[9] Perepelitsa, D., 2006. Johnson Noise And Shot Noise. [ebook] Boston: MIT Department of Physics, pp.1-2. Available at: <http://web.mit.edu/dvp/Public/noise.pdf> [Accessed 22 October 2020].

[10] Chandra Mohonta, S., Firoj Ali, M. and Sadeque, D., 2015. Study of Different Types of Noise and Its Effects in Communication Systems. International Journal of Engineering and Management Research, 5(2), pp.410-413.

[11]M. Bansal and Jyoti, "A review of various applications of low noise amplifier," 2017 International Conference on Innovations in Control, Communication and Information Systems (ICICCI), Greater Noida, India, 2017, pp. 1-4, doi: 10.1109/ICICCIS.2017.8660954. https://ieeexplore.ieee.org/document/8660954

[12] Shailesh H. Yadav, *Design of Low Noise Amplifier For MRI Scanner using Cascode Technology*. International Journal of Innovative Research in Computer and Communication Engineering, 2017.
http://www.ijircce.com/upload/2017/february/34_Design.pdf

[13] Das, T, *Practical Considerations for Low Noise Amplifier Design,* Freescale Semiconductor, 2013. https://www.nxp.com/docs/en/white-paper/RFLNAWP.pdf [Accessed: 24-Oct-2020].

[14] E. O. Farhat, K. Z. Adami, O. Casha, I. Grech and J. G. bij de Vaate, "Design of a wideband CMOS LNA for low frequency band SKA application," 2015 IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Cairo, 2015, pp. 567-571, doi: 10.1109/ICECS.2015.7440380.
https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7440380

[15] A. Azizan, S. A. Z. Murad, R. C. Ismail and M. N. M. Yasin, "A review of LNA topologies for wireless applications," 2014 2nd International Conference on Electronic Design (ICED), Penang, 2014, pp. 320-324, doi: 10.1109/ICED.2014.7015822.
https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7015822

[16] Malathi, D., Gomathi, M. Design of inductively degenerated common source RF CMOS Low Noise Amplifier. Sādhanā 44, 4 (2019). https://doi.org/10.1007/s12046-018-1017-5
https://www.ias.ac.in/article/fulltext/sadh/044/01/0004

[17] “Demoboard for BGU6104 low noise amplifier, ISM and LTE band,” Nxp.com. [Online]. Available: https://www.nxp.com/products/rf/rf-amplifiers-low-medium-power/low-noise-amplifiers-lnas/lnas-for-general-purpose/demoboard-for-bgu6104-low-noise-amplifier-ism-and-lte-band:OM17057. [Accessed: 24-Oct-2020].

[18] N. Shoaib, M. Ahmad and I. Mahmood, "Design, fabrication & testing of Low Noise Amplifier at Ku-Band," 2008 2nd International Conference on Advances in Space Technologies, Islamabad, Pakistan, 2008, pp. 18-23, doi: 10.1109/ICAST.2008.4747679.

[19] D. Pavlidis, “HBT vs. PHEMT vs. MESFET: What’s best and why,” Gaasmantech.com. [Online]. Available: https://gaasmantech.com/Digests/1999/PDF/42.pdf. [Accessed: 12-Apr-2021].

[20] Avago Technologies. “ATF-54143 Low Noise Enhancement Mode Pseudomorphic HEMT in a Surface Mount Plastic Package” AV01-0620EN AV02-0488EN - June 8, 2012

[21] Anurag Bhargava “Customer Success Manager at keysight technologies” https://www.linkedin.com/in/anurag-bhargava-b64239b/ [April 12, 2021]

[22] *mu prime() - mu prime() - Keysight Knowledge Center*. [Online]. Available: https://edadocs.software.keysight.com/pages/viewpage.action?pageId=5899027. [Accessed: 13-Apr-2021].

[23] JLCPCB, “JLCPCB,” https://jlcpcb.com/. [Online]. Available: https://jlcpcb.com/. [Accessed: 04-May-2021].

Appendix A: Datasheets of pre-existing LNAs

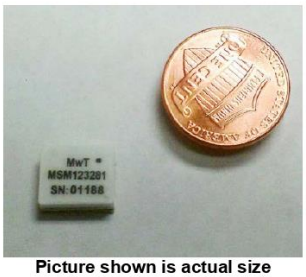
MicroWave Technology

MSM-064281 MSM-128281
MSM-123281 MSM-298281

MSM Series Datasheet
May, 2015

Features:

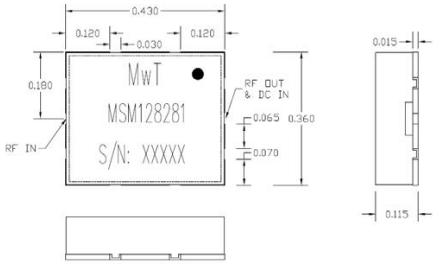
- **1.5T, 3T or 7T**
- **Low Noise Figure**
- **High Linearity**
- **Low Input Impedance**
- **Very Low Magnetism**
- **Low Power Consumption**
- **Miniature Size: 0.43”X0.36”X0.12”**



Picture shown is actual size

Specifications:

- Input impedance: 2 Ohm typical
- Input phase: 180±5º
- Max input protected power: 30dBm
- Gain: 28 dB
- DC Voltage: 10±0.5V
- Output return loss: -15dB
- NF: 0.45dB (0.55dB Max.)
- IP3: 20dBm
- DC current: 15 mA typical



Outline Drawing

Pin 1: RF Input
Pin 4: RF Output/DC Supply(C-option)
Pins 2,3,6: Ground
Pin 5: floating(C-option) or DC supply

Order information:
MSMFFFGG
MSM: Model
FFF: Frequency, 1.5T: 064 MHz, 3T: 123 MHz or 128 MHz, 7T: 298 MHz
GG: 28, 28dB of normal gain.

MicroWave Technology, Inc., 4268 Solar Way, Fremont, CA 94538
510-651-6700 eFAX 510-952-4000 EMAIL thunt@mwtinc.com

Low-Noise Pre-Amplifier for Magnetic Resonance Imaging (MRI)

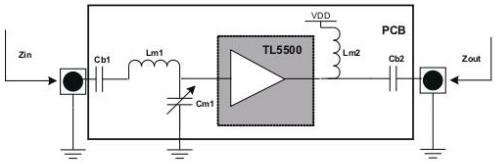
Check for Samples: TL5500

FEATURES

- **Non-Magnetic**
- **Suitable for 1.5T to 3.0T MRI applications**
- **Ultra Low Noise: NF ≤ 0.5dB**
- **Low Supply Voltage: +5V**
- **Low Power Consumption: ≤ 110mW**
- **Insertion Gain: ≥ 28dB**
- **High Accuracy:**
  - **Gain Flatness over BW: ±0.1dB**
  - **Gain Flatness over Temp: ±0.2dB**
- **High Linearity:**
  - **0.1dB Input CP: ≥ –25dBm**
- **SmalL Package: QFN-20, 4-mm × 4-mm**

APPLICATIONS

- **Medical Imaging, MRI**
  - **1.5T, 3T Systems**



RELATED PRODUCTS

DEVICE	DESCRIPTION
TPS715A01DRBT-NM	Non Magnetic, Single Output LDO, 80mA, Adj.(1.2 to 15V)
TPD2E001DRST-NM	Non Magnetic low-capacitance ±15-kV ESD-protection diode

DESCRIPTION

The TL5500 is a Low-Noise Amplifier suitable for MRI coil preamplifier module.

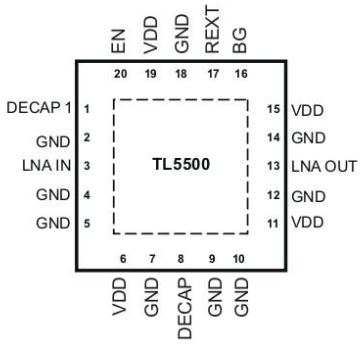
In combination with the external noise matching network the amplifier has very low noise performance, high power gain and high signal handling characteristics.

These features make it the ideal component for a variety of MRI systems from 1.5T to 3.0T.

The low power consumption makes this device suitable for proximity MRI coil applications, where the heat dissipation is a concern.

It uses a single supply of 5V allowing simple PCB design.

In conjunction with an external LDO, non-magnetic TPS715A01DRBT-NM, it can be used up to 10V supply.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TL5500	QFN-20	RGP	+10°C to +50°C	Cu Matte Sn	TL5500	TL5500RGPT-NM	Tape and Reel 250
						TL5500RGPR-NM	Tape and Reel 3.0k

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	RANGE	UNIT
Supply voltage, VDD	–0.3 to 6	V
Input voltage voltage on the pins: LNA IN, DECAP, REXT	–0.3 to 1.8	V
Input voltage on the in: DECAP 1	–0.3 to 3.3	V
Input voltage on the pin: LNA OUT	–0.3 to 6	V
Continuous Power dissipation	200	mW
Output Voltage	–0.3 to 6	V
Peak output current	TBD	mA
RF input power withstand (pulsed 15% duty-cycle)	+30	dBm
ESD rating, HBM	2K	V
ESD rating, CDM	500	V
Operating junction temperature range, any condition T_J	10 to 60	°C
Operating ambient temperature range, T_A	10 to 50	°C
Storage temperature range, T_{stg}	–40 to 125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appear at the end of this data sheet. This is the area where the trademarks for the entire data sheet are defined.

THERMAL INFORMATION

THERMAL METRIC(1)		TL5500 RGP 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	39	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	56.7	
θ_{JB}	Junction-to-board thermal resistance(4)	40.5	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.6	
ψ_{JB}	Junction-to-board characterization parameter(6)	12.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	5.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

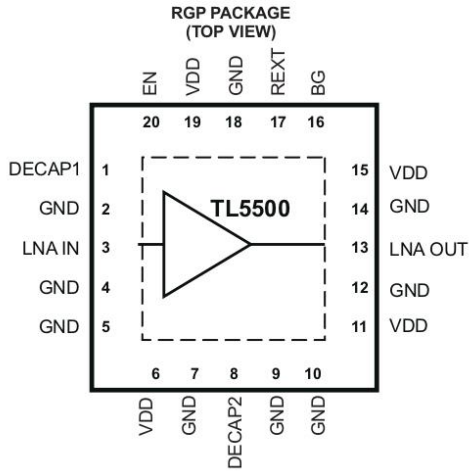
All specifications at T_A = 25°C, VDD = 5V, V_{ENABLE} = 5V, Rsource = 50Ω, Rload = 50Ω unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD	DC Supply voltage		4.75	5	5.25	V
IDD	DC Supply current		19	21.5	24	mA
Fo1	Operating frequency	Bo=1.5T, with dedicated input and output match		63.87		MHz
Fo2		Bo=3T, with dedicated input and output match		127.74		
BW	Frequency bandwidth	Around Fo		±0.5		MHz
G	Insertion gain (S21)	With dedicated input noise match	27	28	29	dB
	Gain flatness over BW				±0.1	dB
	Gain flatness over temperature	T_A = 10°C to 50°C			±0.2	dB
K	Stability factor	Measured in 50MHz BW around Fo	>1			
Γin	Input reflection coefficient (S11)	With dedicated input noise match	0.932	0.942	0.957	
		Phase can be tuned at desired value	≤160°	≤180°	≤160°	deg
	Input reflection phase accuracy	Around the tuned nominal phase		±1°		deg
Γout	Output reflection coefficient (S22)	With dedicated output match		–18	–17	dB
Grev	Reverse Gain (S12)			–56	–53	dB
NF	Noise figure at room temperature	With dedicated input noise match		<0.5	<0.6	dB
Γopt	Optimum source impedance reflection coefficient			0	0.1	
				<±120°		
0.1CP	0.1 dB Input compression point		–25	–22		dBm
1CP	1 dB Output compression point		+11.5	+12		dBm
OIP3	Output third-order intercept point	Two tones, frequency offset 100 kHz, Pout = –3dBm/Tone	+21			dBm
TR	Recovery time(1)	Output signal 90% settling time with input from 30dBm to –40dBm			50	µs
STAB	Long term signal stability(1)	1s ≤ t ≤ 6 min	0.5 0.1			dB rad

(1) This parameter is specified by lab characterization and design.

DEVICE INFORMATION

PIN OUT



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DECAP1		Decoupling bias point; bypass with 100pF (min)
2	GND		
3	LNA IN	I	LNA Input
4	GND		
5	GND		
6	VDD		Internal 5V bias voltage; bypass with 1nF (min)
7	GND		
8	DECAP2		Decoupling bias point; bypass with 100pF (min)
9	GND		
10	GND		
11	VDD		Internal 5V bias voltage; bypass with 1nF (min)
12	GND		
13	LNA OUT	O	LNA Output, external inductor load to VDD
14	GND		
15	VDD		Internal 5V bias voltage; bypass with 1nF (min)
16	BG		Not Used, Connect to GND
17	REXT	O	2% External bias resistor (155 ohms)
18	GND		
19	VDD		Internal 5V bias voltage; bypass with 1nF (min)
20	EN	I	Enable +5V (ON) or GND (OFF)

TYPICAL CHARACTERISTICS

At T_A = 25°C, VDD = 5V, V_{ENABLE} = 5V, Rsource = 50Ω, Rload = 50Ω (unless otherwise noted)

CURRENT CONSUMPTION

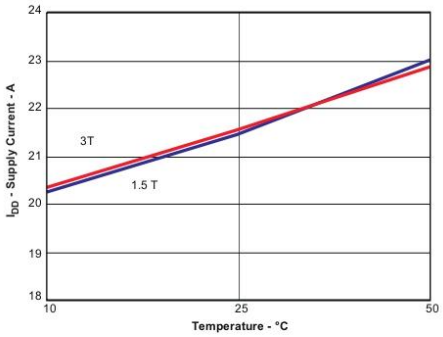


Figure 1.

GAIN SHIFT vs TEMPERATURE

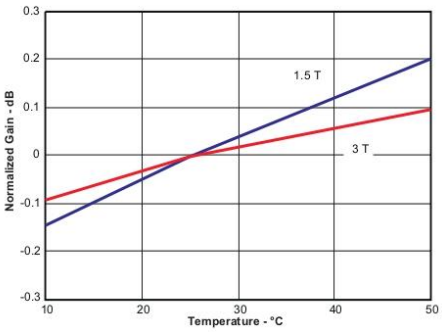


Figure 2.

SMALL SIGNAL GAIN – AC RESPONSE

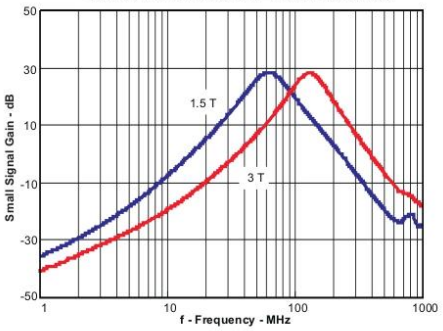


Figure 3.

GAIN SHIFT vs SUPPLY

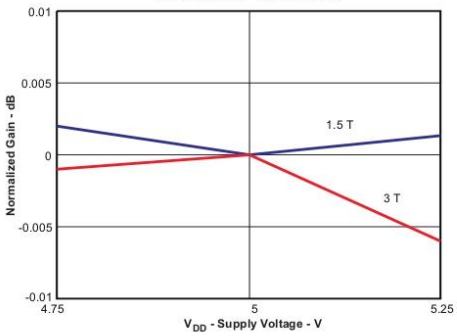


Figure 4.

GAIN PHASE – AC RESPONSE

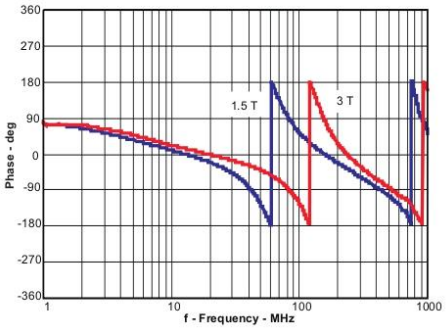


Figure 5.

GAIN PHASE SHIFT vs TEMPERATURE

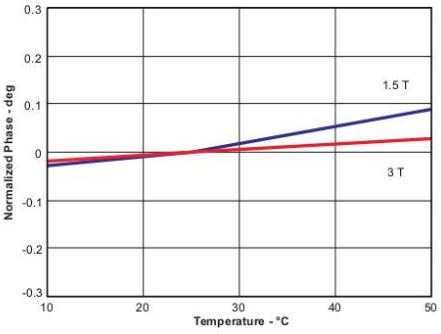


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, VDD = 5V, V_{ENABLE} = 5V, Rsource = 50Ω, Rload = 50Ω (unless otherwise noted)

SMALL SIGNAL GAIN – AC RESPONSE

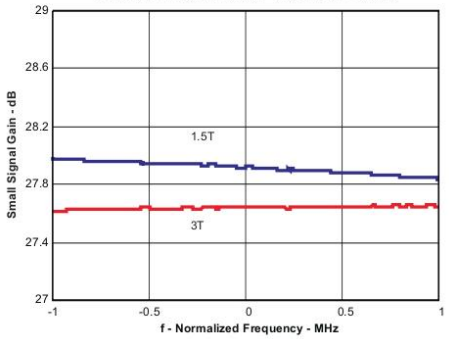


Figure 7.

GAIN PHASE – AC RESPONSE

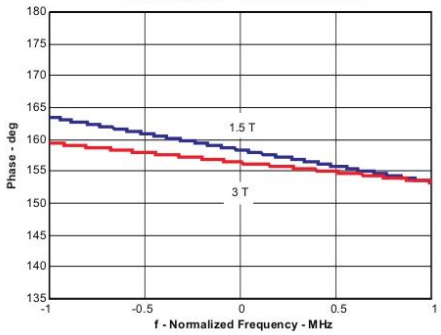


Figure 8.

INPUT REFLECTION COEFFICIENT

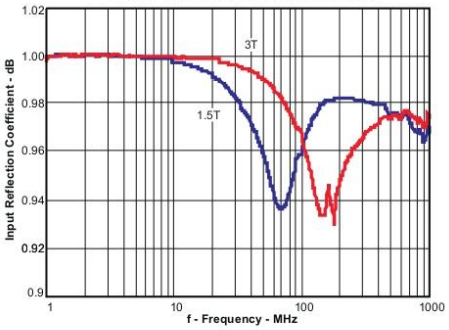


Figure 9.

INPUT REFLECTION COEFFICIENT

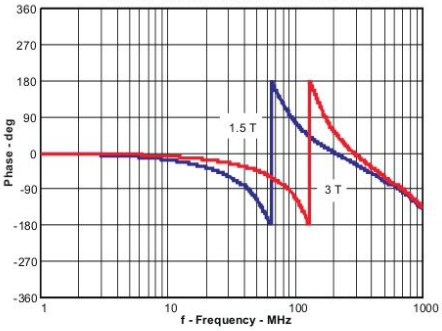


Figure 10.

OUTPUT REFLECTION COEFFICIENT

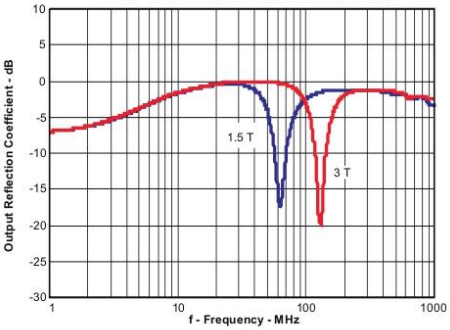


Figure 11.

OUTPUT REFLECTION COEFFICIENT

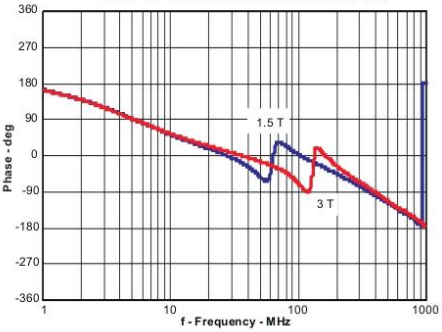


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, VDD = 5V, V_{ENABLE} = 5V, Rsource = 50Ω, Rload = 50Ω (unless otherwise noted)

REVERSE GAIN

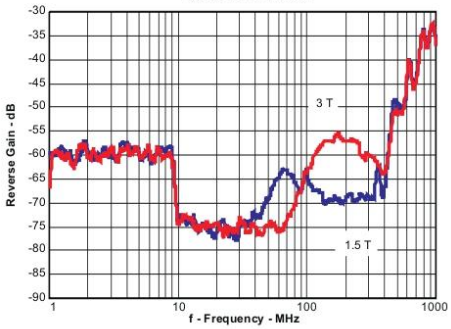


Figure 13.

REVERSE GAIN

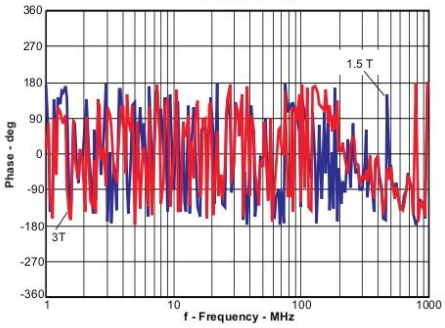


Figure 14.

INPUT REFLECTION COEFFICIENT vs TEMPERATURE

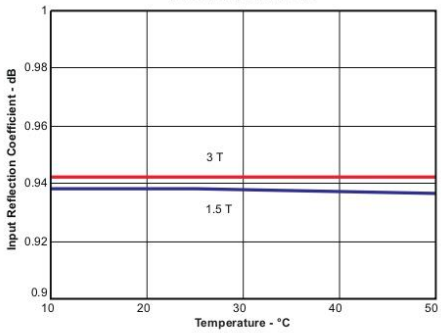


Figure 15.

INPUT RESISTANCE vs TEMPERATURE

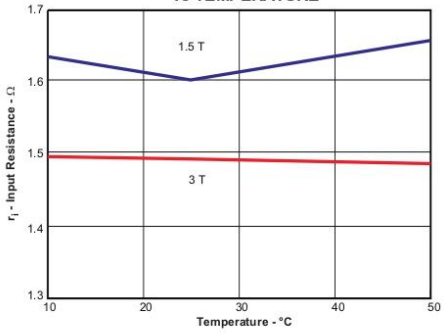


Figure 16.

OUTPUT REFLECTION COEFFICIENT vs TEMPERATURE

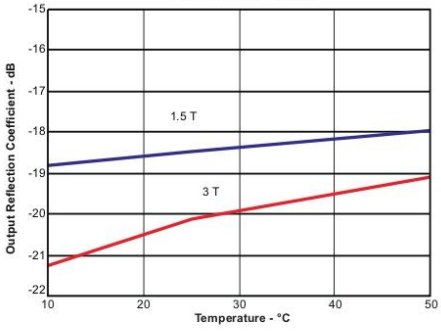


Figure 17.

INPUT REFLECTION COEFFICIENT vs TEMPERATURE

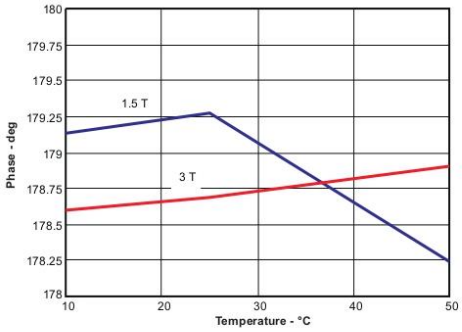


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, VDD = 5V, V_{ENABLE} = 5V, Rsource = 50Ω, Rload = 50Ω (unless otherwise noted)

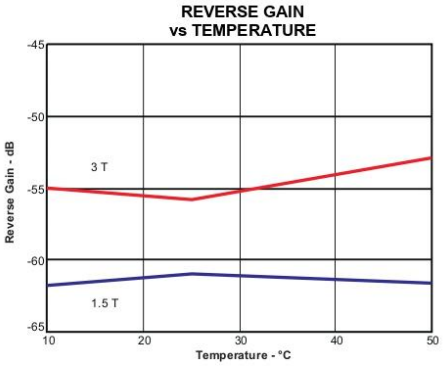


Figure 19.

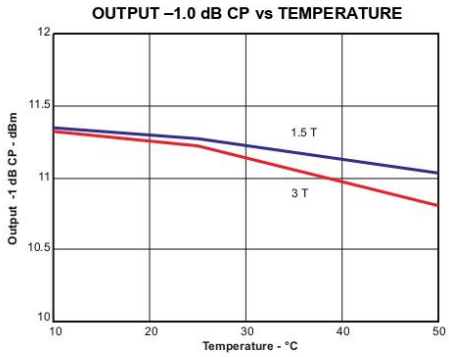


Figure 20.

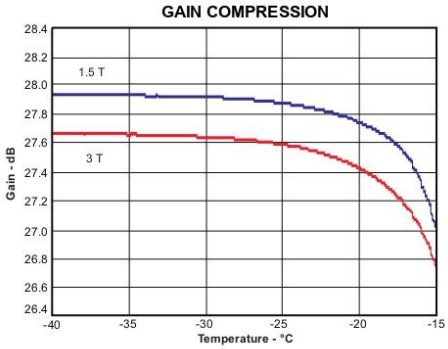


Figure 21.

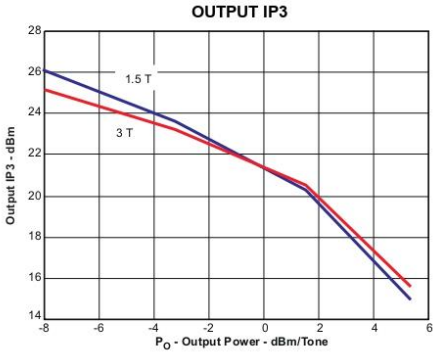


Figure 22.

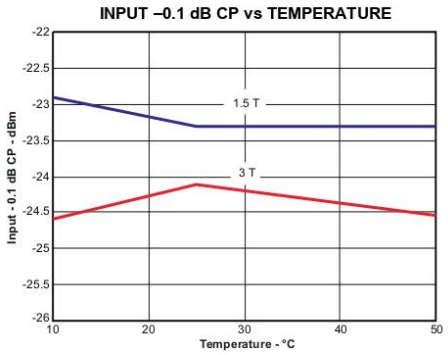


Figure 23.

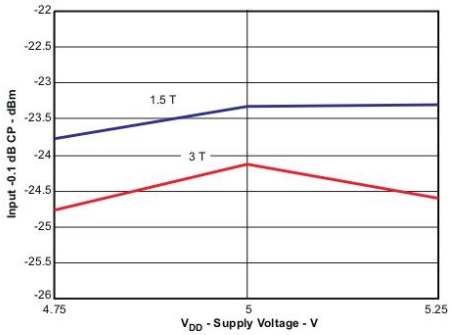


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, VDD = 5V, V_{ENABLE} = 5V, Rsource = 50Ω, Rload = 50Ω (unless otherwise noted)

OUTPUT –1.0 dB CP vs SUPPLY

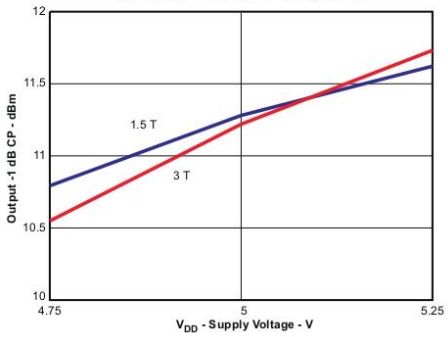


Figure 25.

NOISE FIGURE

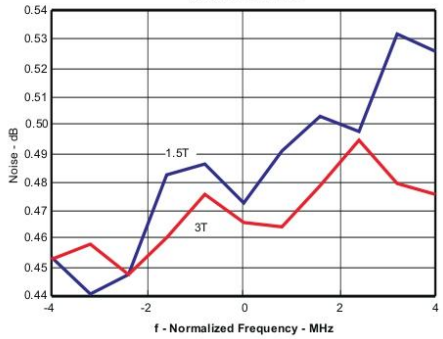


Figure 26.

OUTPUT IP3 vs TEMPERATURE
Pout = –3 dBm/TONE

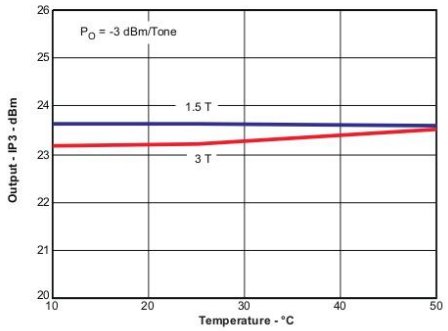


Figure 27.

STABILITY K-FACTOR

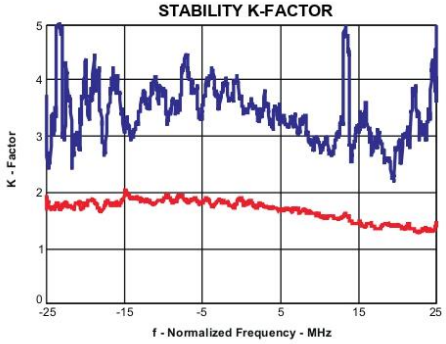


Figure 28.

TYPICAL CONNECTION DIAGRAM

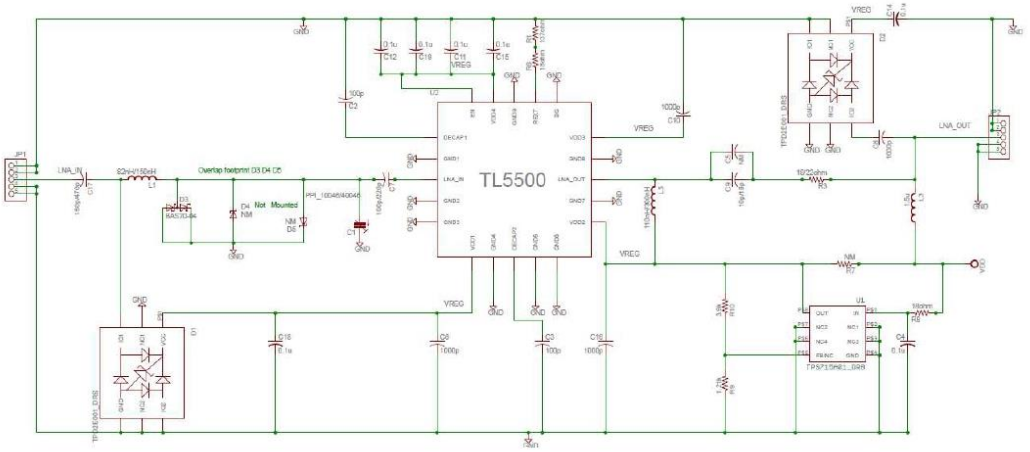


Figure 29. TL5500 Preamp Application Circuit: VDD = +5.5 V to +10 V (±5%)

The recommended application circuit for TL5500 is shown in Figure 29. The external components are described in Table 1 and they ensure correct functionality and performance for MRI-Coil preamplifier, with +10V or +5V supply, 1.5T or 3T frequencies.

The reference design in Figure 29 also ensures ESD protection against 15KV air discharge and 8KV contact, compliant with IEC 61000-4-2.

Supply Voltage and Bias

The bias resistor R1 and R6 are used to set the accurate internal bias current for TL5500.

The TL5500 can work in conjunction with non-magnetic linear regulator TPS71A01NDRBT-NM and extend the external supply operating voltage from +5.5V to +10V

If the user decides to use +5.0V supply (±5%), the linear regulator, together with R9 and R10, shall be not mounted.

With +5V supply the linear regulator stabilization capacitors (C4, C11, C12 and C19) can also be not mounted. The capacitor C15 can be mounted and set to 1000pF. The power supply must be properly decoupled close to the supply pins. The placement and the size of the decoupling capacitors are very important to achieve the optimum performances. The reference design in Figure 28 should be followed closely.

RF Matching

The input match, L1 and C1, transforms the IC input impedance into a low resistance, close to a short circuit. In the reverse direction, the input match transforms the 50Ω source into the optimum source impedance for the IC, ensuring the amplifiers operates close to the NFMIN region. Therefore the optimal noise performance is achieved when the reference design is connected to a 50Ω source. C7 and C17 are for DC blocking.

The output match simultaneously ensures accurate insertion gain (S21) and transforms the IC output impedance into 50Ω.

The LC component values and their placement are important to keep the performances optimized. It is highly recommended to follow the TL5500 reference design. Gerber files and schematics for the reference design are available upon request.

Overload Protection

The Schottky diode pair D3 ensure the protection of the application circuit from input overload, up to +30dBm.

Table 1. Bill Of Materials

COUT	Value at 1.5T (63.86 MHz)	Value at 3T (127.7 MHz)	Value at VDD = 5.5V to 10V ±5%	Value at VDD = 5V ±5%	Package	Manufacturer
C1	8.0pF – 40.0pF Trim Capacitor	2.0pF – 10.0pF Trim Capacitor	Use the values indicated in the Operating Frequency Columns		C1813	PassivePlus: PPI10046 (3T) PPI40046 (1.5T)
C2	100pF, 50V, 5%, X7R				C0402	Syfer: 0402-2-050-0101-J-X
C3	100pF, 50V, 5%, X7R				C0402	Syfer: 0402-2-050-0101-J-X
C4	0.1µF, 16V, 10%, X7R				C0603	Syfer: 0603-3-016-0104-K-X
C5	Not Mounted				C0402	
C6	1000pF, 50V, 5%, X7R				C0402	Syfer: 0402-2-050-0101-J-X
C7	220pF, 50V, 5%, COG	100pF, 50V, 5%, COG			C0603	Vishay: VJ0603-A-221-J-N-A-AT (1.5T) VJ0603-A-101-J-N-A-AT (3T)
C9	18pF, 50V, 2%, COG	10p, 50V, 2%, COG			C0402	Syfer: 0402-2-050-0180-G-C (1.5T) 0402-2-050-0100-C-C (3T)
C10	1000pF, 50V, 5%, X7R				C0402	Syfer: 0402-2-050-0102-J-X
C11	0.1uF, 16V, 10%, X7R			NOT MOUNTED	C0603	Syfer: 0603-3-016-0104-K-X
C12	0.1uF, 16V, 10%, X7R			NOT MOUNTED	C0603	Syfer: 0603-3-016-0104-K-X
C14	0.1uF, 16V, 10%, X7R		Use the values indicated in the Operating Frequency columns		C0603	Syfer: 0603-3-016-0104-K-X
C15	0.1µF, 16V, 10%, X7R			1000pf, 50V, 5%, X7R	C0603	Syfer: 0603-3-016-0104-K-X Syfer: 0603-3-050-0102-J-X
C16	1000pF, 50V, 5%, X7R		Use the values indicated in the Operating Frequency columns		C0402	Syfer: 0402-2-050-0102-J-X
C17	470pF, 50V, 5%, COG	180pf, 50V, 5%, COG			C0603	Vishay: VJ0603-A-181-J-N-A-AT (3T) VJ0603-A-471-J-N-A-AT (1.5T)
C18	0.1µF, 16V, 10%, X7R				C0603	Syfer: 0603-3-016-0104-K-X
C19	0.1µF 16V, 10%			NOT MOUNTED	C0603	Syfer: 0603-3-016-0104-K-X

Table 1. Bill Of Materials (continued)

COUT	Value at 1.5T (63.86 MHz)	Value at 3T (127.7 MHz)	Value at VDD = 5.5V to 10V ±5%	Value at VDD = 5V ±5%	Package	Manufacturer
D1	15KV ESD Diode		Use the values indicated in the Operating Frequency columns		DRS-8 3x3mm SON	TPD2E001DRSR-NM Texas Instruments
D2	15KV ESD Diode				DRS-8 3x3mm SON	TPD2E001DRSR-NM Texas Instruments
D3	Silicon Schottky Diode				SOT23	Infineon BAS70-04
D4	NOT MOUNTED				D0402	Microsemi PIN diode MPP4201-206-HS
D5	NOT MOUNTED				D0402	Microsemi PIN diode MPP4201-206-HS
L1	150nH, 2%	82nH, 2%			L1812	Coilcraft: 1812SMS-R15 LB (1.5T) 1812SMS-82N LB (3T)
L3	1500nH, 5%				L1008	Coilcraft: 1008CS-152X LB
L5	300nH, 2%	110nH, 2%			L0603	Coilcraft: 0603HP-R30X L (1.5T) 0603hp-R11X L (3T)
R1	137Ω, 1%				R0603	IMS: RC3-0603-1370F
R3	22Ω, 1%	18Ω, 1%			R0603	IMS: RC3-0603-22R0F (1.5T) RC3-0603-18R0F (3T)
R6	18Ω, 1%				R0603	IMS: RC3-0603-18R0F
R7	NOT MOUNTED		NOT MOUNTED	0Ω/solder bridge	R0402	
R8	18Ω, 1%				R0603	IMS: RC3-0603-18R0F
R9	1.2kΩ, 1%			NOT MOUNTED	R0402	IMS: RC3-0402-1201F
R10	3.9kΩ, 1%			NOT MOUNTED	R0402	IMS: RC3-0402-3901F
U1	LDO 80mA			NOT MOUNTED	DRB 3x3mm SON	Texas Instruments TPS715A01DRBT-NM
U2	Preamplifier				RGP 4x4mm QFN	Texas Instruments TL5500RGPR-NM
J1	5-pin header, 100mil					Samtec: ASP-142798-1 Non-Magnetic
J2	5-pin header, 100mil					Samtec: ASP-142798-1 Non-Magnetic

SUGGESTED PCB DESIGN

The suggested 4-layer PCB layout is shown in Figure 30

This design can accommodate either +5V and +10V supply by using different bill of material, as indicated in Table 1.

Suggested substrate material is FR4, with 2oz metal thickness. For non-magnetic finishing the user can choose Immersion Silver or Silver Palladium; The 4-layer description is given here below:

- Layer 1: Top Signal
- Layer 2: GND
- Layer 3: Power
- Layer 4: Bottom Signal

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The area under the chip is used for grounding and shall be connected to the ground plane (layer-2), with several vias for good thermal performance and sufficiently low inductance to ground.

In the TL5500 EVM reference designs, 14 vias are placed around the exposed die attached pad. These vias should be “tented” (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process.

The solder paste coverage should not be 100%. If it is, out gassing may occur during the reflow process, which may cause defects (splattering, solder balling). Using “tented” vias reduces the solder paste coverage below 100%.

Similar design practice should be used for the exposed die attached pad of linear regulator (U1), mounted on Layer-4.

The stack-up in Figure 31 may change if the final manufacturing data are different from the information used to create this one.

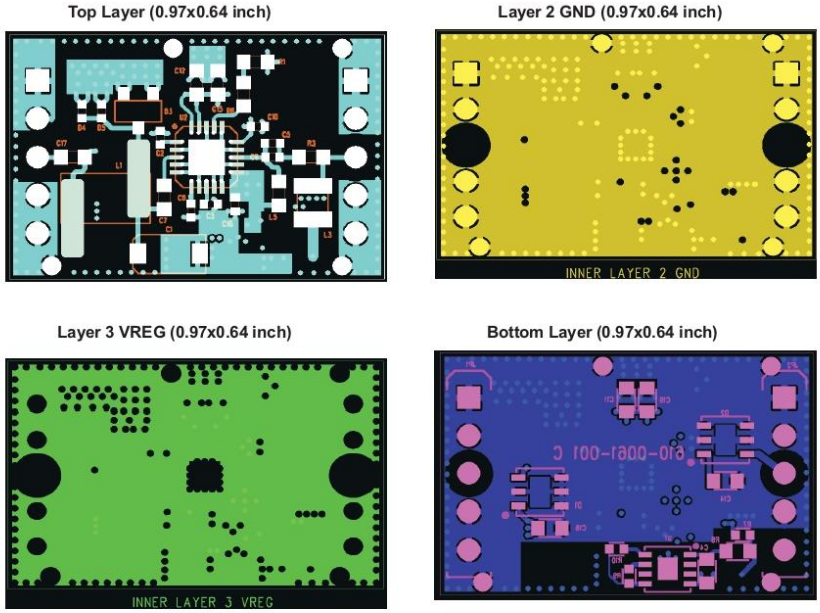
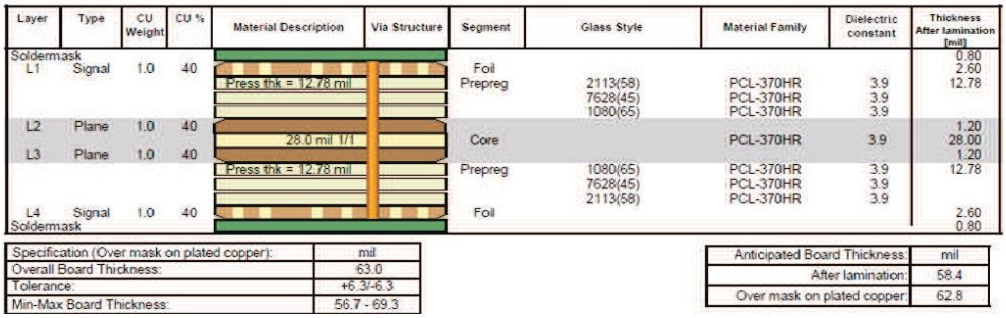


Figure 30. TL5500 Preamp PCB Layout



Layer	Type	CU Weight	CU %	Material Description	Via Structure	Segment	Glass Style	Material Family	Dielectric constant	Thickness After lamination [mil]
Soldermask										0.80
L1	Signal	1.0	40			Foil				2.60
				Press thk = 12.78 mil		Prepreg	2113(58)	PCL-370HR	3.9	12.78
							7628(45)	PCL-370HR	3.9	
							1080(65)	PCL-370HR	3.9	
L2	Plane	1.0	40							1.20
				28.0 mil 1/1		Core		PCL-370HR	3.9	28.00
L3	Plane	1.0	40							1.20
				Press thk = 12.78 mil		Prepreg	1080(65)	PCL-370HR	3.9	12.78
							7628(45)	PCL-370HR	3.9	
							2113(58)	PCL-370HR	3.9	
L4	Signal	1.0	40			Foil				2.60
Soldermask										0.80

Specification (Over mask on plated copper):	mil
Overall Board Thickness:	63.0
Tolerance:	+6.3/-6.3
Min-Max Board Thickness:	56.7 - 69.3

Anticipated Board Thickness:	mil
After lamination:	58.4
Over mask on plated copper:	62.8

Figure 31. PCB Stack up

REVISION HISTORY

Changes from Original (August 2010) to Revision A	Page
• Changed units in Typical Characteristics graphs to fix original typos. Hz unit to MHz as well as some X-axis numbering issues.	5

Changes from Revision A (October 2010) to Revision B	Page
• Updated Typical Characteristics graphs.	5
• Changed Bill of Materials table.	11

Changes from Revision B (November 2011) to Revision C	Page
• Updated PACKAGE/ORDERING INFORMATION table.	2
• Updated Typical Connection Diagram.	10

PACKAGINGINFORMATION

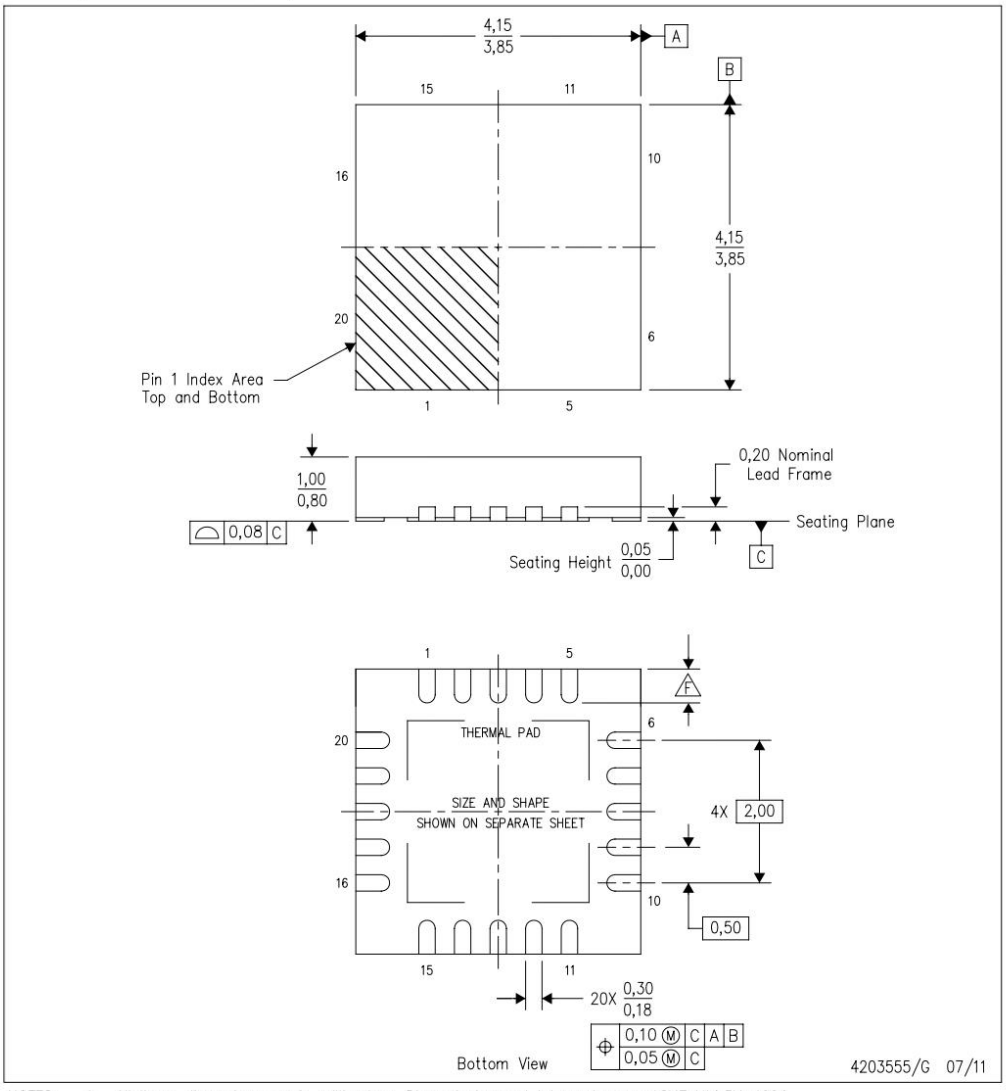
OrderableDevice	Status (1)	Package Type	Package Drawing	Pins	Package Qty	EcoPlan (2)	Lead/BallFinish	MSLPeakTemp (3)
TL5500RGPT-NM	ACTIVE	RGC	RGC	20	250	Green(RoHS& noSb/Br)	CU / Matte Sn	Level-1-260C-1 YEAR
TL5500RGPR-NM	ACTIVE	RGC	RGC	20	3000	Green(RoHS& noSb/Br)	CU / Matte Sn	Level-1-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) EcoPlan- The planned eco-friendly classification: Pb-Free(RoHS), Pb-Free(RoHSExempt), or Green(RoHS&noSb/Br)- please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free(RoHS): TI'sterms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures,TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free(RoHSExempt): This component has a RoHS exemption for either 1)lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green(RoHS&noSb/BTrI): defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine(Br) and Antimony(Sb) based flame retardants (BrorSb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

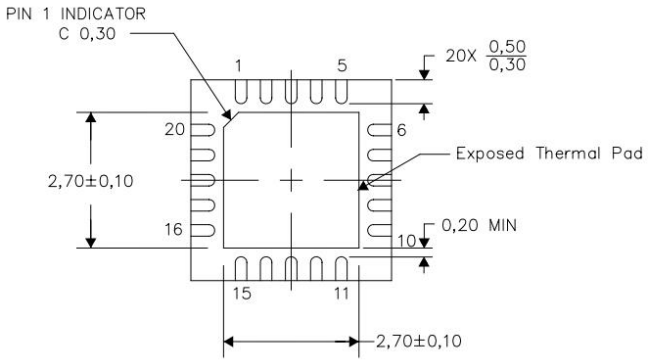
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206346–3/X 02/12

NOTES: A. All linear dimensions are in millimeters

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

WMA7RC

7T LOW NOISE PRE-AMPLIFIER

REV C
December 2014

Key Features

- 7T Frequency of 298 MHz
- 1.0 Ohm Input Impedance
- 0.40 dB Noise Figure
- 30.0 dBm Max P_{IN}
- 18.0 dBm Output IP_3
- 28.0 dB Gain
- 10.0 dBm P_{1dB}
- 1.22:1 Output VSWR
- Unconditional Stable, k>1
- Single Power Supply
- Non Magnetic

Product Description

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE

WMA7RC integrates WanTcom proprietary low noise amplifier technologies, high frequency micro electronic assembly techniques, and high reliability designs to realize optimum low noise figure, wideband, and high performances together. With single +10.0V DC operation, the amplifier has 1.0 Ohm input impedance and unconditional stable condition. The amplifier has 0.50" x 0.40" x 0.10" surface mount package.

Applications

- MRI
- RF Measurement
- Medical
- Current Sensor

Specifications

Summary of the key electrical specifications at room temperature

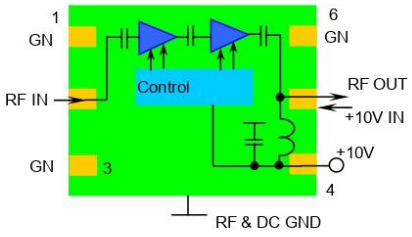
Index	Testing Item	Symbol	Test Constraints	Min	Nom	Max	Unit
1	Gain	S_{21}	298 MHz	27.5	28.0	28.5	dB
2	Gain Variation	ΔG	298 MHz +/- 1 MHz		+/-0.03	+/- 0.05	dB
3	Input Impedance	RE [Zin]	298 MHz		1.0	2.0	Ohm
		IM [Zin]	298 MHz	-2.0	0	2.0	Ohm
4	Output VSWR, 50 Ohm Impedance	SWR_2	298 MHz			1.22:1	Ratio
5	Reverse Isolation	S_{12}	298 MHz	60	70		dB
6	Noise Figure	NF	298 MHz		0.40	0.50	dB
7	Output Power 1dB Compression Point	P_{1dB}	298 MHz	8	10		dBm
8	Output-Third-Order Interception point	IP_3	Two-Tone, P_{out} = 0 dBm each, 1 MHz separation	16	18		dBm
9	Current Consumption	I_{dd}	V_{dd}= +10.0 V		18		mA
10	Power Supply Operating Voltage	V_{dd}		+7	+10	+12	V
11	Thermal Resistance	$R_{th,c}$	Junction to case			220	°C/W
12	Operating Temperature	T_o		+10		+60	°C
13	Maximum RF Input Power	$P_{IN, MAX}$	DC – 6.0 GHz, 10% Duty Cycle,			30	dBm
14	Saturate Recover Time	t_{sr}	10% to 90% from 30 dBm Pin		8	10	uS
15	ESD Protection, None Contact	V_{ESDN}	Output Ports			16	kV
16	ESD Protection, Direct Contact	V_{ESD}	Output Ports			6	kV

Absolute Maximum Ratings

Parameters	Units	Ratings
DC Power Supply Voltage	V	12.0
Drain Current	mA	30
Total Power Dissipation	mW	350
RF Input Power, 10% Duty Cycle	dBm	30
Channel Temperature	°C	150
Storage Temperature	°C	-65 ~ 150
Operating Temperature	°C	0 ~ +70
Thermal Resistance[1]	°C/W	220

Operation of this device beyond any one of these parameters may cause permanent damage.

Functional Block Diagram



[1] The last stage transistor dominates the heat dissipation. The drain bias voltage is +3.5V and the drain current is 10.0 mA. The total power dissipation of the last stage transistor is thus 35 mW. The junction temperature arise 0.035 x 220 = 7.7 (°C).

Specifications and information are subject to change without notice.

WanTcom, Inc ∘ Phone 01 952 448 6088 ∘ FAX: 01 952 448 7188 ∘ e-mail: sales@wantcominc.com ∘ Web site: www.wantcominc.com

Ordering Information

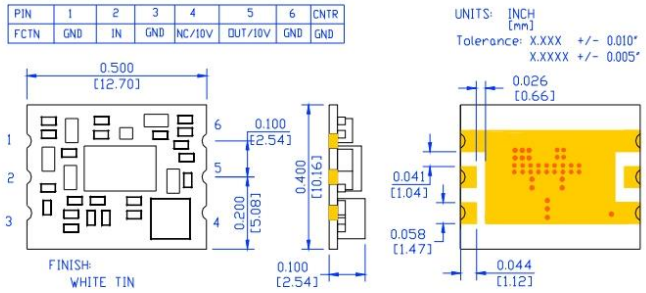
Model Number	WMA7RC

ESD tube is used for the packing. Contact factory for tape and reel packing option for higher volume order.

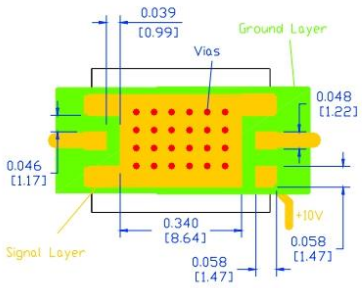
Typical Data

Preliminary

Outline



Foot Print/Mounting Layout



WanTcom, Inc • Phone 01 952 448 6088 • FAX: 01 952 448 7188 • e-mail: sales@wantcominc.com • Web site: www.wantcominc.com

Application Notes:

A. Motherboard Layout

The recommended motherboard layout is shown in diagram of **Foot Print/Mounting Layout**. Sufficient numbers of ground vias on center ground pad are essential for the RF grounding. The width of the 50-Ohm microstrip lines at the input and output RF ports may be different for different property of the substrate. The ground plane on the backside of the substrate is needed to connect the center ground pad through the vias. The ground plane is also essential for the 50-Ohm microstrip line launches at the input and output ports.

The +10V DC voltage is applied at Pin 4 or at the output Pin 5. There is a built-in bias-T at the output port to separate the RF output signal and input +10V DC power supply.

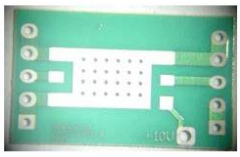


Fig. 1 Example of the motherboard

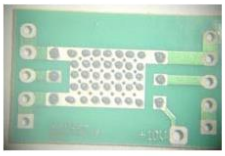


Fig. 2 Dispensed solder paste

Fig. 3 Assembled

B. Assembly

The regular low temperature and none clean solder paste such as SN63 is recommended. The high temperature solder has been used internally for the WHM series amplifier assembly. The melting temperature point of the high temperature solder is around 217 ~ 220 ^{0}C. Thus, melting temperature of the solder paste should be below 217 ^{0}C for assembling WHM series amplifier on the test board to reduce the possible damage. The temperature melting point of the SN63 solder paste is around 183 ^{0}C and is suitable for the assembly purpose.

The SN63 solder paste can be dispensed by a needle manually or driven by a compressed air. **Figure 2** shows the example of the dispensed solder paste pattern. Each solder paste dot is in the diameter of 0.005" ~ 0.010" (0.125 ~ 0.250 mm).

For volume assembly, a stencil with 0.006" (0.15 mm) is recommended to print the solder paste on the circuit board.

For more detail assembly process, refer to AN-109 at www.wantcominc.com website.

******

Appendix B: Information on Northeastern MRI

7T MRI at Northeastern:

A multipurpose research system for high-resolution magnetic resonance spectroscopy and imaging. The Bruker BioSpec 70/20 MRI is a multipurpose research system for high-resolution Magnetic Resonance Spectroscopy and Imaging. The system is equipped with 7 Tesla superconducting magnets designed with "Ultra Shielded Refrigerated" (USR) magnet technology. The USR technology significantly reduces the stray field to close to the magnet. The scanner has an actively shielded, high-performance BGA-S series gradient system with integrated shim coil. Superior performance on the following major characteristics can thus be achieved: Ultra high gradient strength, Very short gradient slew rates, Excellent gradient duty cycle (independent of shims and gradients), Optimal gradient linearity, Very high gradient shielding quality, Maximal shim strength.

Source: https://web.northeastern.edu/ctni/mri-scanner/

Appendix C: Amplifier Measurement Techniques.

Chapter 1

Device Characterization

1.1 Noise Measurement

1.1.1 Aim

The aim of experimental procedure is to generate a noise spectral density plot and a input-referred noise figure value for the whole system.

1.1.2 Equipment

Figure 1.1: (Left) MSOX3104T mixed-signal oscilloscope with FFT capability, (Right) SR570 LNA

- Low-noise threshold oscilloscope. Two options that can be used:
  - MSOX6004A Mixed Signal Oscilloscope (211b lab): 1GHz to 6GHz bandwidth, 115uVrms noise floor with 1mv/div at 1GHz
  - MSOX3104T Mixed Signal Oscilloscope (NECAMSID lab): up to 1GHz bandwidth (lower bandwidth not specified), 572.9uVrms noise floor with 20us/div at 1GHz, Has a FFT capability
- Stanford Research Center SR560 (Prof Petkie Lab): benchtop low-noise preamplifier with integrated filter, 0.03Hz to 1MHz bandwidth
- DC Voltage Supply

1.1.3 Method

Common Setup

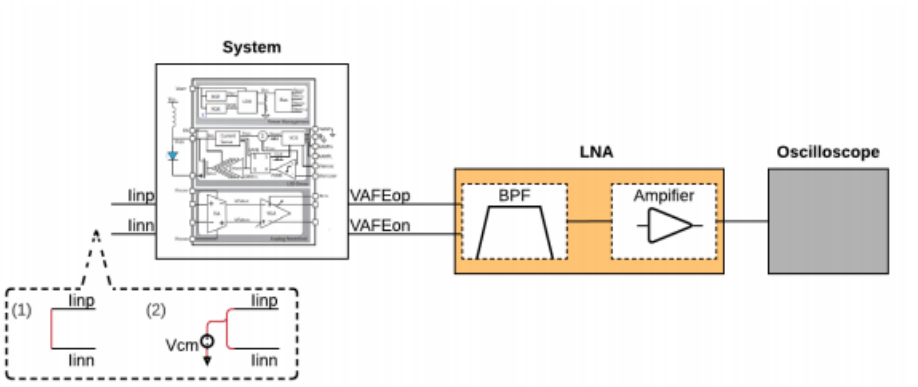


Figure 1.2: Noise measurement setup common to measuring both the noise spectral density and the noise figure

- Collect the required equipment including the LNA, oscilloscope, and DC power supply. Connect as shown in Figure 1.2.
- For the input of the system, there are two options that can be applied. Option 1 is shorting the Iin positive and negative terminals to get the voltage noise spectral density plot. Option 2 is connecting a VDD/2 DC source common mode to the inputs to get the current noise spectral density plot.
- Set the DC power supply to the system VDD and connect appropriately to the system
- Using the LNA, set the filter settings using the five buttons A through B referencing Figure 1.1(b). Using button A, set the rolloff to the bandpass filter configuration by pressing the button till the two '6 dB/oct' LEDs light up. Using button B and C, set the high-pass filter cutoff frequency to 'DC'. Similarly, using button D and E to set the low-pass filter cutoff frequency to 10kHz.
  - Justification: A 10kHz cutoff frequency will be high enough to identify the 1/f corner frequency of the system.
- For the rest of the LNA settings, set the LNA coupling to 'DC'. The source should be set to 'A-B' because of the differential output of the system being tested. The gain mode should be set to 'low noise'. The single-ended output of the LNA should be taken from the 50Ohm port. The gain can be set to x10, x100, x1000, or x10000. The gain setting should be set such that the amplitude at the output should be at minimum x10 greater than the thermal noise floor. This gain will be dependent on the input signal amplitude from the system being tested.
  - Note: The input of the LNA is differential but the output is single-ended.
  - Justification: The gain mode is set to 'low noise' because in this configuration the LNA gain is allocated to the front-end to ensure the low amplitude signals (in the nV range) are amplified above the noise floor and do not get obscured. The 50hm output port is used rather than the 600Ohm port because the latter is designed to drive high impedance loads which is not the case for this experimental setup. The gain setting is set with a hard minimum so that the signal is not obscured by the noise floor.
- Set the oscilloscope to 'DC coupling'.

Generating Noise Spectral Density Plot

- Connect the BNC connector side of the oscilloscope probe to channel 1. Use the fish hook probe tip to connect to the output of the LNA. Set the ground pin to ground. Press the 'auto scale' button to get the waveform within range.
- Use the horizontal adjustment knob to set the time to 10s. Use an appropriate time scale to achieve this.
  - Justification: A 10s time scale will include frequencies down to 0.1Hz are included in the noise spectral density plot.
- Press the 'FFT' button circled in red referencing Figure 1.1(a).

Calculate Input-Referred Noise Figure (NF)

- Connect the BNC connector side of the oscilloscope probe to channel 1. Use the fish hook probe tip to connect to the output of the LNA. Set the ground pin to ground. Press the 'auto scale' button to get the waveform within range.
- Click the 'Meas' button and set it to measure the maximum peak-to-peak voltage
- Going back to the *Common Setup* section, short the differential inputs of the system and ground them. Repeat the procedure to measure the maximum peak-to-peak voltage.
- Calculate the output-referred NF by taking the ratio of the noise produce by the system divided by the thermal noise when the system input is grounded.
- Calculate the input-referred NF by dividing the output-referred NF by the gain of the LNA.

1.2 Power Characterization

1.2.1 Aim

- To measure the power consumption of each sub-block, namely the power management unit, LED driver and analog front-end(AFE)
- To calculate the efficiency,power supply rejection ratio (PSRR), line and load regulations of the power management unit

1.2.2 Equipment and software

- Oscilloscope
  - Voltage probe x 2
  - Current Probe (High sensitivity probe for low current measurements)
- DC Source x 2
- Signal Generator
- Digital multimeter
- Vee Pro

1.2.3 Method

Characterization of the Power Management Unit

- Calculate the efficiency and power dissipation of the power management unit